YTM32B1MC0x Data Sheet

Support: YTM32B1MC03H0MLHT, YTM32B1MC03H0MLFT, YTM32B1MC03H0MFNR, YTM32B1MC03H0MFNIR

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Document Number: YTM32B1MC0x DS

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1 Features Summary

- AEC-Q100 qualified
- ASIL-B compliant
- RoHS compliant
- 32-bit Cortex-M33 without FPU and DSP, up to 80 MHz
- Debug functionality
  - Joint Test Action Group (IEEE 1149.1 standard)
  - Serial Wire Debug (SWD)
- Up to 128KB * 2 Program Flash (PFlash0/1)
  - Support ECC feature
  - Support OTA
  - Wide operating voltage ranges (2.97 ~ 5.5V) with fully functional Flash memory program/erase/read operations
- Up to 20KB DFlash
  - Support ECC feature
  - Support OTA
- Up to 32KB SRAM
  - Support ECC feature
- 8KB on-chip ROM supports secure boot
- Provide multiple clock sources including:
  - 80MHz Fast Internal RC Oscillator (FIRC)
  - 2MHz Slow Internal RC Oscillator (SIRC)
  - 4~40MHz Fast Crystal Oscillator (FXOSC)
  - 32KHz Low Power Oscillator (LPOCLK)
- Power Control Unit (PCU) with internal regulators capable of supporting multiple power modes including:
  - Active
  - Sleep
  - Deepsleep
  - Standby
- 4 DMA channels with up to 64 hardware trigger sources
- Analog modules providing precision mixed-signal capabilities, including:
  - One 12-bit, 1Msps SAR ADC, up to 27 external channels and 6 internal channels
  - On-chip Analog Comparator (ACMP) with 8-bit DAC, up to 8 channels
  - Temperature sensor
- Timers
  - One 4-channel Periodic Timer (pTMR)
  - One Low Power Timer (lpTMR)
  - Two 8-channel Enhanced Timer (eTMR)
  - One Multiple Pulse Width Modulation (MPWM)
- Serial communication interfaces
  - Two FlexCAN modules with FD
  - Three UART modules
  - Three SPI modules
  - Two I2C modules
- Security and Safety features are supported as follows:
  - Cyclic Redundancy Checker (CRC)
  - Hardware Cryptography Unit (HCU) which supports AES-128
  - True Random Number Generator (TRNG)
  - Clock Monitor Unit (CMU)
  - Watchdog (WDG)
  - External watchdog (EWDG)
  - ECC Management Unit (EMU)
- Human-machine interfaces
  - Up to 58 General-Purpose Input/Output (GPIO)
  - External interrupt
- I/O supporting 2.97 ~ 5.5V supply
- Temperature range:
  - Ambient operating temperature: -40 °C ~ 125 °C
- Package options
  - 64-pin LQFP
  - 48-pin LQFP
  - 48-pin QFN

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2 Overview

The YTM32B1Mx is a family of microcontrollers built on the latest ARM® Cortex®-M33, and it offers a broad range of memory, peripherals and package options.

The YTM32B1Mx family introduces new features and uses high performance, high reliability CMOS technology to provide substantial cost reduction and significant performance improvement.

YTM32B1MC0x series of devices are 32-bit general purpose automotive microcontrollers based on the ARM Cortex-M33 core. They offer superior performance, large memories and the most scalable peripherals in this class. This product series provide up to 80 MHz CPU performance, with up to 256KB PFlash, 20KB DFlash, 8KB ROM and 32KB SRAM.

3 Block Diagram

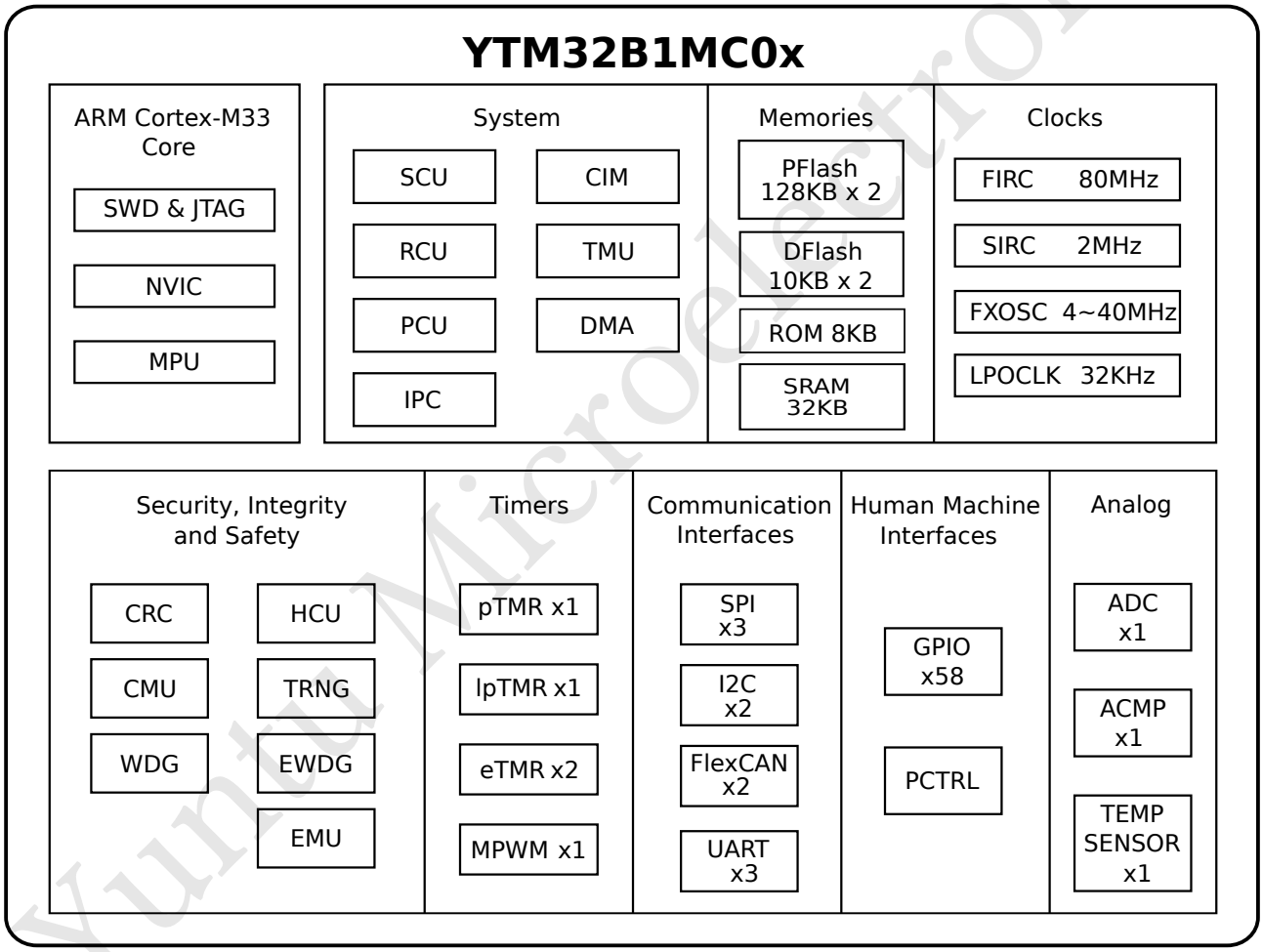


Figure 1: YTM32B1MC0x Block Diagram

4 Features

The following sections describe the high-level module features for YTM32B1MC0x device.

4.1 Core Modules

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4.1.1 ARM Cortex-M33

- ARM Cortex M33 core running up to 80 MHz
- ARMv8-M MPU for dynamic task protection (4 regions)
- Single cycle 32 x 32 bits multiply
- 3-stage pipeline, thumb-2 technology
- Binary compatible instruction set with the ARM Cortex M4/M7

4.1.2 Nested Vector Interrupt Controller (NVIC)

- Up to 76 interrupt sources
- Support 8 priority levels for interrupts with two bits in each IPRn registers
- Include a single non-maskable interrupt

4.1.3 Debug Controller

- 2-pin serial wire debug (SWD) provides external debugger interface
- Support JTAG port (IEEE 1149.1 standard)

4.2 System Modules

4.2.1 System Clock Unit (SCU)

- Fast internal RC oscillator(FIRC)
  - Up to 80 MHz
  - Default system boot clock source
  - Support trim for temperature and process
- Slow internal RC oscillator(SIRC)
  - Up to 2 MHz
  - Can be selected as system clock source
  - Always on unless it is forced to be disabled in Deepsleep and Standby mode
  - Support trim for process
- Fast crystal oscillator(FXOSC)
  - Support 4~40 MHz crystal
  - Can be selected as system clock source
  - Support bypass mode
- Low power oscillator(LPOCLK)
  - 32 KHz always on clock source
- Clock monitor unit(CMU)
  - SCU contains 2 CMU blocks
  - CMU monitors FIRC and FXOSC clock
  - SIRC clock is used as reference clock of CMU
  - CMU can detect frequency out of range, loss of checked clock and loss of reference clock
- SCU provides glitch free switcher to select system clock source
- SCU provides system clock dividers to generate core clock, fast bus clock and slow bus clock.

4.2.2 Power Control Unit (PCU)

- Combination of internal and external voltage regulator options, offering a variety of power modes
- Active POR providing brown-out detect
- Low voltage reset for all system relevant power domains (LVR)
- Low voltage detect (LVD) as an indication for software.

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4.2.3 Reset Control Unit (RCU)

- Record the reset sources of most recent resets.
- Configurable filter for reset pin.
- Reset pin filter can work in Active, Sleep, Deepsleep Standby mode.

4.2.4 IP Control (IPC)

- Peripheral Bus clock enable
- IPC clock source selection from multiple clock sources
- IPC clock divide values from 1 to 16
- Peripheral software reset

4.2.5 Direct Memory Access (DMA)

- All address range data transfer from source to destination
- Support separate source/destination data size configuration
- Word(32-bit), half word(16-bit), byte(8-bit) transfer size
- Support separate source/destination address offset configuration
- Address increase/decrease/keep selectable
- Up to 4 DMA channels
- Fix priority and round-robin arbitration
- Support channel to channel link
- Software/Hardware/Link trigger
- Up to 64 peripheral hardware triggers
- Internal data FIFO for data transfer
- Support update DMA transfer information from system memory after transfer complete
- Support data transfer loop and trigger loop

4.2.6 Trigger Multiplexer Unit (TMU)

- Allow software to select the trigger sources for peripherals as trigger sources

4.2.7 Chip Integration Module (CIM)

- System function configuration
- ADC/ACMP trigger synchronize selection
- Software trigger generate
- eTMR external clock and fault selection
- Flash memory and system RAM size configuration
- Package configuration

4.3 Memories

4.3.1 Embedded Flash Module (EFM)

- Program Flash (PFlash) support 256KB address space
  - PFlash support ECC 1-bit error correction and 2-bit error detetion (SEC-DED)
  - Support Read-While-Write and OTA (Over-The-Air) technology
- Data Flash (DFlash) support 20KB address space
  - DFlash support ECC 1-bit error correction and 2-bit error detetion (SEC-DED)

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  - Support read-while-write and OTA (Over-The-Air) technology
- Protection scheme against accidental program or erase operations
- Command protection function for authorization protection
- Optional interruptions on command completion and status update
- Support prefetch read to improve AHB read performace
- Support read buffer to improve AHB read performace

4.3.2 On-chip SRAM

- 32 KB SRAM with ECC supports single error correction (SEC) and double error detection (DED)

4.3.3 Read-Only Memory (ROM)

- 8KB on-chip memory map
- The ROM boot firmware is programmed by YTMicro to support the following two functions:Secure boot, System clock and watchdog configuration:
  - Run once the chip releases the reset signal of the CM33 core
  - Support the parsing of the configurable BVT (Boot Vector Table) stored in the Flash memory
- Secure Boot
  - Work as the root of trust
  - Support CMAC authorization of the customized code (i.e. bootloader, OTA) with the specified secure boot group configuration set in the BVT.(Note: The CMAC authorization is achieved by HCU.)
    * Support decryption of secure boot section configuration structure with the specified HCU AES key in secure boot group configuration
    * Support up to 8 secure boot section configurations (each includes the section start address, length and HCU AES key used for CMAC as well as CMAC stores address pointer)
  - The used HCU hardware user keys for secure boot section configuration structure encryption and CMAC authorization should be pre-programmed to HCU_NVR memory by the Car OEM or Tier-1 using the flash programmer
  - Support strict serial secure boot mode (enabled via BVT)
    * If CMAC authorization fails, the secure boot holds the CM33 core in static mode
  - Support normal serial secure boot mode (by default)
    * If CMAC authorization fails, the CM33 core continues to execute the bootloader and the applications, but all HCU hardware user keys will be disabled or fail to load.
- System clock and watchdog configuration
  - Support flexible system clock configuration for ROM boot via BCW (Boot Configuration Word) in BVT. For example, using 80MHz FIRC rather than the default 40MHz (FIRC/2) can reduce the boot time.
  - Support watchdog enable/disable function and timeout configuration for CM33 main core

4.4 Analog

4.4.1 Analog-to-Digital Converter (ADC)

- Contain 1 ADC instances
  - ADC0 supports up to 27 external analog input channels, and 5 internal channels
- Support 12-bit, 10-bit, 8-bit and 6-bit single-ended configurable resolution
- Up to 1 Msps for 12-bit resolution conversion performance
- Support DMA and conversion result FIFO with watermark
- Support multiple conversion modes

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  - Single mode
  - Continuous mode
  - Discontinuous mode
- Support software/hardware trigger for ADC start conversion
- Support two power saving modes
  - Wait mode: prevent ADC overrun when FIFO is full
  - Auto off mode: automatic control ADC power off
- Support watchdog for conversion result monitoring
- Support interrupt generate
  - Ready for conversion
  - End of sampling
  - End of conversion
  - End of sequence conversion
  - Overrun event
  - Watchdog event
  - Trigger source loss error event
- Support work and wake up when the chip is under sleep and deepsleep modes

4.4.2 Analog Comparator (ACMP)

- Up to 8 channels
- Operational over the entire supply range
- ACMP DAC Buffer inputs may range from rail to rail
- Programmable hysteresis control
- Selectable inversion on comparator output
- Function mode:
  - Common mode
  - Sample mode
  - Window mode
  - Continuous mode
    - One-shot mode
    - Loop mode
- All channels can be used to execute automatic comparison
- Support digital filter, the filter can be bypassed
- Two software selectable performance levels
  - Shorter propagation delay at the expense of higher power
  - Low power with longer propagation delay
- Functional in all power mode
- Support independent 8-bit DAC output to the comparator
- Support several interrupts
  - For common/sample/window mode
    - Generate interrupt on rising-edge, falling-edge or both edges of the comparator output
  - For continuous mode
    - Generate interrupt when the comparison results don't match with expectations
- Interrupt can be generated without any clock in common mode
- A comparison event can be selected to trigger DMA transfer

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4.5 Timer

4.5.1 Periodic Timer (pTMR)

- Timers can generate interrupts, and each channel can generate independent interrupt request
- Four channels of 32-bit timers, each timer has independent timeout periods
- Ability to stop in debug mode
- Support chain mode to connect multiple timer to a longer timer

4.5.2 Low Power Timer (lpTMR)

The features of the lpTMR module include:

- 16-bit time counter or pulse counter with compare
- Optional interrupt can generate asynchronous wakeup from any Low-power mode
- Hardware trigger output
- Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter
  - Rising-edge or falling-edge

4.5.3 Enhanced Timer (eTMR)

The common features contained in all eTMRs are listed below:

- Configurable final counter values
- Contain 8 channels
- Support two clock sources
  - Bus clock
  - External clock
- Support 7-bits clock prescaler
- Support four channel modes
  - Common timer
  - PWM mode
    - Independent mode for each channel
    - Complementary mode for each pair of channels
      - All channels support independent deadtime insertion
    - Channel output control (initialization, software control, mask control, fault control)
      - Support 4 fault input sources
      - Support fault input from TMU or pad
      - Support fault input polarity control
      - Support fault input filter
      - Support fault input stretch
      - Support fault event generated by combinational logic
    - Relevant registers have buffer registers and support loading mechanism
  - Output Compare mode
    - The output can be configured to set, clear or toggle on match point
  - Input Capture mode
    - Support rising edges, falling edges or dual edges capture

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    - Support input filter with a prescaler
    - Support capture test mode
- Support generating triggers
  - Output triggers with adjustable pulse width on match point
  - Output pulse with adjustable width by PWM
- Polarity control is available for each channel
- Support GTB (Global Time Base)
- Support several interrupts
  - Channel interrupt (capture interrupt and compare interrupt)
  - Counter overflow interrupt
  - Fault event interrupt
- Support DMA
- Support counter running under debug mode
- Supports hall sensor input
- Support input from ACMP

4.5.4 Multiple Pulse Width Modulation (MPWM)

- Each MPWM supports 8 channels
- Each channel contains a 16-bit counter independently
  - Configurable comparison value
  - Configurable period value
- Support clock prescaler(1, 2, 4, 8, 16, 32, 64, 128) independently
- Counting modes
  - Continuous mode
  - One shot mode
- Support counter starts counting by hardware trigger in one shot mode
- Support four channel modes
  - Common timer
  - PWM mode
    - Independent mode for each channel
    - Support edge-aligned PWM
    - Relevant registers have double buffer registers and support loading mechanism
    - Write operations to double buffer registers take effect immediately
  - Output Compare mode
    - The output can be configured to set, clear or toggle on match point
  - Input Capture mode
    - Support rising edge capture
    - Support falling edge capture
    - Support any edge capture
    - Support combination capture
  - Pulse count mode
- Support generating triggers on match point
- Polarity control is available for each channel
- Support several interrupts
  - Channel event interrupt

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  - Timer overflow event interrupt
- Support DMA
- Support hall sensor input
- Support input from ACMP
- Support counter running under debug mode

4.6 Security, Integrity and Safety

4.6.1 Cyclic Redundancy Check (CRC)

- The following CRC polynomials are implemented:
  - CRC4 (CRC-ITU):
    $X^4 + X + 1$
  - CRC8 (CRC-ITU):
    $X^8 + X^2 + X + 1$
  - CRC16 (CRC-CCITT):
    $X^{16} + X^{12} + X^5 + 1$
  - CRC32 (CRC-ethernet):
    $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable initial seed
- Optional bit-swap in one byte is available for input data
- Optional bit-swap in one word is available for output data
- Optional bit-inversion is available for output data
- 8/16/32-bit access for CRC input data

4.6.2 Hardware Cryptography Unit (HCU)

- Support 128-bit key length
- Support both encryption and decryption
- Support secure hardware key and flexible software key
- Support several algorithm engines
  - AES (ECB, CBC , CMAC)
- All data input/output are in little-endian format
- Support bit, byte and half-word data swapping
- Support DMA transport
- Support several interrupts
- Clock gating strategy is applied for engine core

4.6.3 True Random Number Generator (TRNG)

Features of the TRNG module include:

- Generate a 128-bit entropy
- Monobit test to limit the number of value 0 and 1
- Long run test to avoid continuous constant value
- 1 ring OSC with clock checker
- 3 interrupt source
  - Entropy valid interrupt
  - Frequency error interrupt
  - Hardware error interrupt

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4.6.4 ECC Management Unit (EMU)

- 1 channels of ECC injection and report
- Two-stage enable mechanism for ECC injection
- Correctable or uncorrectable error can be injected
- ECC error interrupt can be enabled with separated register bit
- The last ECC error data can be recorded into register

4.6.5 Watchdog (WDG)

- 16-bit countdown timer
- Functional clock can be selected from multiple clock sources
- Support regular or window servicing mode
- Support reset request or interrupt for the first timeout
- Hard and soft configuration lock bits

4.6.6 External Watchdog (EWDG)

- Independent functional clock source
- Programmable time-out period
- Windowed refresh option
- Provides robust check that program flow is faster than expected
- Programmable window
- Refresh operation should be done within 63 peripheral bus clock cycles
- An output pad EWDG_OUT_b is used to indicate operation error
- An input pad EWDG_IN is used for external circuit to control EWDG_OUT_b output directly

4.7 Communication Interfaces

4.7.1 Flexible Controller Area Network (FlexCAN)

- Full implementation of the CAN FD protocol and CAN Specification 2.0, Part B
  - Standard data frames
  - Extended data frames
  - Zero to sixty-four bytes data length
  - Programmable bit rate
  - Content-related addressing
- Compliant with the ISO 11898-1 standard
- Silicon-proven implementation passing ISO 16845-1:2016 CAN conformance tests
- Flexible mailboxes configurable to store 0 to 8, 16, 32, or 64 bytes data length
- Each mailbox configurable as receive or transmit, all supporting standard and extended messages
- Individual Rx Mask registers per mailbox
- Full-featured Legacy Rx FIFO with storage capacity for up to 6 CAN frames and automatic internal pointer handling with DMA support
- Full-featured Enhanced Rx FIFO with storage capacity for up to 32 CAN FD frames and automatic internal pointer handling with DMA support
- Transmission abort capability
- Flexible message buffers, totaling 128 message buffers of 8 bytes data length each, configurable as Rx or Tx
- Programmable clock source to the CAN Protocol Engine, either peripheral clock or oscillator clock
- RAM not used by reception or transmission structures can be used as general purpose RAM space
- Listen-Only mode capability

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- Programmable Loop-Back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Time stamp based on 16-bit free-running timer, with an optional external time tick or high-resolution 32-bit on-chip timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independence from the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Transceiver Delay Compensation feature when transmitting CAN FD messages at faster data rates
- Remote request frames may be managed automatically or by software
- CAN bit time settings and configuration bits can only be written in Freeze mode
- Tx mailbox status (lowest priority buffer or empty buffer)
- Identifier Acceptance Filter Hit Indicator (IDHIT) register for received frames
- SYNCH bit available in Error in Status 1 register to indicate that the FlexCAN is synchronous with CAN bus
- CRC status for transmitted message
- Legacy Rx FIFO Global Mask register
- Selectable priority between mailboxes and Rx FIFO during matching process
- Powerful Legacy Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard, or 512 partial (8 bit) IDs, with up to 32 ID Filter Table elements
- Powerful Enhanced Rx FIFO ID filtering, capable of matching incoming IDs against either 64 extended or 128 standard ID filter elements with three filtering schemes: mask + filter, range, and two filters without mask
- 100% backward compatibility with previous FlexCAN version
- Support in low power modes: Deepsleep mode and Standby mode

4.7.2 Universal Asynchronous Receiver/Transmitter (UART)

- Support LIN break send and detect
- Transmit/Receive FIFO
- Support Transmit/Receive via DMA
- Baudrate setting
- 1-bit or 2-bit STOP size
- 7-bit, 8-bit, 9-bit or 10-bit frame size
- Transmit/Receive polarity setting
- Receive data match
- Line idle, address match wakeup
- Support transmit/receive line switch
- Support hardware flow control (CTS/RTS)
- Support single wire mode

4.7.3 Serial Peripheral Interface (SPI)

- Support clock polarity and phase configuration

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- Configurable frame size
- Transmit/Receive FIFO
- Support Transmit/Receive via DMA
- Support Standard/Dual/Quad SPI mode
- Support I2S standard transfer
- Support Master and Slave mode

4.7.4 Inter-Integrated Circuit (I2C)

- Support standard, fast, fast plus, high speed and ultra fast mode
- Support 7-bit/10-bit address mode with master and slave
- Support SMBus mode
- Support multi-master arbitration and synchronization
- Support master and slave clock stretching
- Transmit/Receive FIFO (master only)
- Digital filter on both SCL and SDA pins
- Support transmit/receive via DMA

4.8 Human Machine Interface

4.8.1 General Purpose Input/Output (GPIO)

- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Direction register
- Inversion for data inputs
- Interrupt flag and enable registers for each pin
- Support for edge sensitive (rising, falling, both) or level sensitive (low, high)
- Asynchronous wake-up in low-power modes
- Pin interrupt is functional in all digital pin muxing modes
- Support getting state of the port in all digital pin muxing modes

4.8.2 Port Controller (PCTRL)

The PCTRL module has the following port control features:

- Individual pull control fields with pullup, pulldown, and pull-disable support
- Individual input passive filter field supporting enable and disable of the individual input passive filter on selected pins
- Individual drive strength field supporting low or high drive strength on selected pins
- Individual mux control field supporting analog or pin disabled, GPIO, and up to 6 chip-specific digital functions
- Individual digital filter for data inputs
- Individual lock function to avoid misoperation

5 Ordering Information

The following chips are available for ordering.

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Table 1: Ordering Table

Product	Memory		Package		IO and ADC channel		Communication
Part number	Flash(KB)	SRAM(KB)	Pin count	Package	GPIOs (Normal)	ADC channels	FlexCAN
YTM32B1MC03H0MLHT	256 KB	32 KB	64	LQFP	58	32	2
YTM32B1MC03H0MLFT	256 KB	32 KB	48	LQFP	43	25	2
YTM32B1MC03H0MFNR	256 KB	32 KB	48	QFN	43	25	2
YTM32B1MC03H0MFNIR	256 KB	32 KB	48	QFN	43	25	2

5.1 Part Number Information

Table 2: Part Number Field Description

Field	Description	Values							
YTM	Product Status	YTM: Qualified PTM: Prototype							
32	MCU Type	32: 32-bit							
B	Product Line	B: General D: Dashboard P: Powertrain V: Vision N: Network Z: High voltage, integrity							
1	Generation	1st generation production							
Mx	Level	Product Line							
		B			Hx: High end Mx: Middle end Lx: Low end				
		Z			Mx: Motor+LIN-PHY Lx: LIN-PHY Cx: CAN-PHY Tx: Touch-sensor Dx: LED Driver				
0	Major Revision	1st revision							
3	Memory Size		0	1	2	3	4	5	6
		Z	-	-	-	32K	48K	64K	128K
		H	1M	2M	4M	6M	8M	12M	16M
		M	-	-	128K	256K	512K	1M	2M
		L	-	-	-	32K	64K	128K	256K
H0	Reserved	Reserved							
M	Ambient Temperature	C: -40°C ~85°C V: -40°C ~105°C M: -40°C ~125°C W: -40°C ~150°C							
		Pins			LQFP	QFN	TSSOP	BGA	
		8			-	-	TB	-	-
		10			-	-	TC	-	-

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Table 2 continued from previous page

Field	Description	Values					
FN	Package	12	-	-	TD	-	-
		14	-	-	TE	-	-
		16	-	-	TF	-	-
		20	-	-	TH	-	-
		24	-	FK	-	-	-
		32	LE	FM	-	-	-
		48	LF	FN	-	-	-
		64	LH	FO	-	-	-
		100	LL	-	-	MH	-
		144	LQ	-	-	-	-
		176	LU	-	-	-	-
		208	-	-	-	MK	-
		257	-	-	-	MM	-
		289	-	-	-	MQ	-
		320	-	-	-	MR	-
		373	-	-	-	MS	-
		416	-	-	-	MT	-
		516	-	-	-	MV	-
I	Optional Mode	S: Single end mode D: Differential mode I: ISELED C: Cost Optimization X: ISELED and Cost Optimization					
R [1]	Packing	T: Trays/Tubes R: Tape and Reel					

1. The chip mark doesn't contain packing information

6 Electrical Characteristics

6.1 Ratings

6.1.1 Thermal Operating Characteristics

Symbol	Patameter	Value			Unit
		Min.	Typ.	Max.	
$T_{A\ M-Grade\ Part}$	Ambient temperature under bias	-40	–	125	°C
$T_{J\ M-Grade\ Part}$	Junction temperature under bias	-40	–	135	°C

6.1.2 Moisture Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	3	3		1

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1. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

6.1.3 ESD Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-4000	4000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	-500	500	V	
	Corner pins only	-750	750	V	
I_{LAT}	Latch-up current at ambient temperature of 125 °C	-100	100	mA	3
	Latch-up current at ambient temperature of 25 °C	-200	200	mA	

1. Determined according to JEDEC Standard JESD22-A114, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

6.2 DC Characteristics

6.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	-0.3	5.8[1]	V	
I_{VDD}	Maximum current into V_{DD}	–	70	mA	
V_{IO}	Digital/Analog IO Input voltage	-0.3	V_{DD} + 0.3	V	
I_O	Instantaneous maximum current of single pin	-25	25	mA	
V_{DDA}	Analog supply voltage	V_{DD} - 0.3	V_{DD} + 0.3	V	

1. 60 seconds lifetime - No restrictions i.e. the part is not held in reset and can switch.
10 hours lifetime - The part is held in reset by an external circuit i.e. the part cannot switch.

NOTE:

- The maximum ratings are the limits to which the device can be subjected without permanently damaging the device.
- The device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

6.2.2 Voltage and Current Operating Requirements

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Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.97	5.5	V	
V_{DDA}	Analog supply voltage	2.97	V_{DD}	V	
V_{REFH}	Reference voltage	2.97	V_{DDA}	V	
$V_{DD} - V_{DDA}$	V_{DD} to V_{DDA} differential voltage	-0.1	0.1	V	
I_{ICIO}[1]	Continuous DC input current (positive / negative) that can be injected into an I/O pin	-1	1	mA	
I_{ICcont}	Contiguous pin DC injection current — regional limit, includes sum of positive rejection currents of 16 contiguous pins	–	15	mA	
T_{ramp}	MCU supply ramp rate	5 V/100ms	100 V/ms	–	

1. All pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{SS} − 0.3V or greater than V_{DD} + 0.3V, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{SS}-0.3V-V_{IN})/|I_{ICIO}|$. The positive injection current limiting resistor is calculated as $R = [V_{IN}-(V_{DD}+0.3V)]/|I_{ICIO}|$. The actual resistor values should be an order of magnitude higher to tolerate transient voltages.

6.2.3 DC Electrical Specifications at 3.3V

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O supply voltage	2.97	3.3	4.0	V	
V_{ih}	Input buffer high voltage	0.7 * V_{DD}	–	V_{DD} + 0.3	V	
V_{il}	Input buffer low voltage	V_{SS} - 0.3	–	0.3 * V_{DD}	V	
V_{hys}	Input buffer hysteresis	0.06 * V_{DD}	–	–	V	
I_{oh}	Normal drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	5	12	–	mA	
I_{ol}	Normal drive I/O current sink capability measured when pad = 0.8V	5	15	–	mA	
I_{oh}	High drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	5	12	–	mA	
I_{ol}	High drive I/O current sink capability measured when pad = 0.8V	5	15	–	mA	
I_{leak}	Hi-Z (Off state) leakage current (per pin) @25°C	–	50	500	nA	
	Hi-Z (Off state) leakage current (per pin) @125°C	–	100	500	nA	
V_{OH}	Output high voltage					
	Normal drive pad (2.97V ≤ V_{DD} ≤ 4.0V, I_{OH} = -2.8mA)	V_{DD} - 0.8	–	V_{DD}	V	
V_{OL}	Output low voltage					
	Normal drive pad (2.97V ≤ V_{DD} ≤ 4.0V, I_{OL} = -2.8mA)	V_{SS}	–	0.8	V	

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Table 8 continued from previous page

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
I_{OLT}	Output low current total for all ports	–	–	50	mA	
I_{IN}	Input leakage current (per pin) for full temperature range					
	Normal pins	–	–	0.5	μA	
	High Drive pins	–	–	0.5	μA	
R_{PU}	Internal pull-up resistors	20	–	100	kΩ	
R_{PD}	Internal pull-down resistors	20	–	105	kΩ	

6.2.4 DC Electrical Specifications at 5.0V

Symbol	Patameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O supply voltage	4	5	5.5	V	
V_{ih}	Input buffer high voltage	0.65 * V_{DD}	–	V_{DD} + 0.3	V	
V_{il}	Input buffer low voltage	V_{SS} - 0.3	–	0.35 * V_{DD}	V	
V_{hys}	Input buffer hysteresis	0.06 * V_{DD}	–	–	V	
I_{oh}	Normal drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	10	17	–	mA	
I_{ol}	Normal drive I/O current sink capability measured when pad = 0.8V	10	20	–	mA	
I_{oh}	High drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	10	30	–	mA	
I_{ol}	High drive I/O current sink capability measured when pad = 0.8V	10	35	–	mA	
I_{leak}	Hi-Z (Off state) leakage current (per pin) @25°C	–	50	500	nA	
	Hi-Z (Off state) leakage current (per pin) @125°C	–	100	500	nA	
V_{OH}	Output high voltage					
	Normal drive pad (4.0V $\leq$ V_{DD} $\leq$ 5.5V, I_{OH} = -2.8mA)	V_{DD} - 0.8	–	V_{DD}	V	
V_{OL}	Output low voltage					
	Normal drive pad (4.0V $\leq$ V_{DD} $\leq$ 5.5V, I_{OL} = -2.8mA)	V_{SS}	–	0.8	V	
I_{OLT}	Output low current total for all ports	–	–	50	mA	
I_{IN}	Input leakage current (per pin) for full temperature range					
	Normal pins	–	–	0.5	μA	

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Symbol	Patameter	Value			Unit	Notes
		Min.	Typ.	Max.		
	High Drive pins	–	–	0.5	μA	
R_{PU}	Internal pull-up resistors	20	–	70	kΩ	
R_{PD}	Internal pull-down resistors	15	–	70	kΩ	

6.2.5 Power and Ground Pins

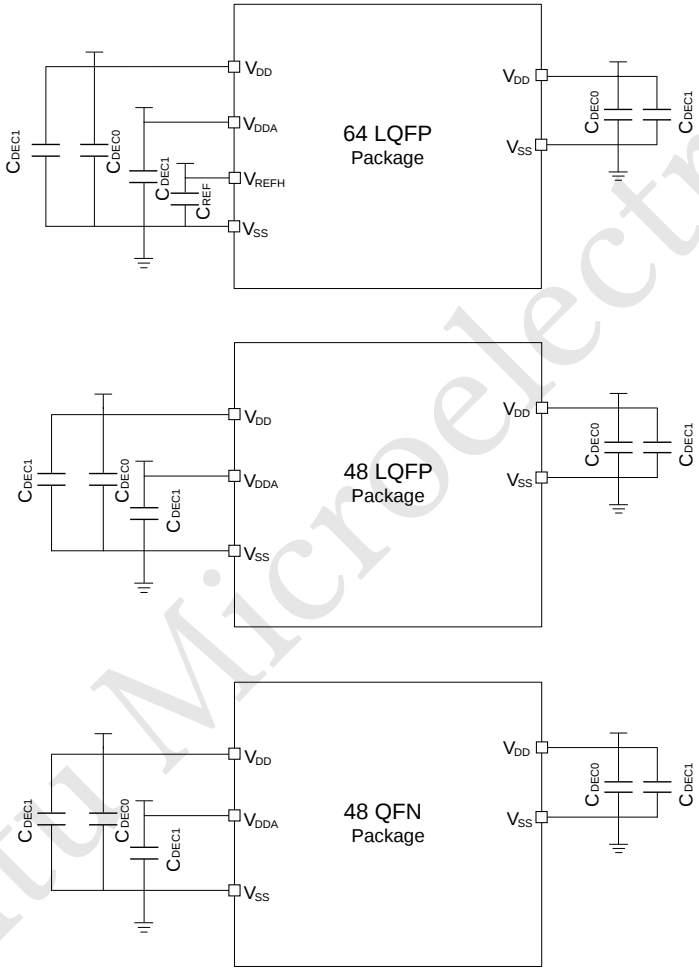


Figure 2: Pinout Decoupling

Symbol	Description	Min.	Typ.	Max.	Unit
C_{REF} [1,2,3]	ADC reference high decoupling capacitance	50	100	200	nF
C_{DEC0} [2,3,4]	Recommended decoupling capacitance	2.2	4.7	20	μF
C_{DEC1} [2,3,4]	Recommended decoupling capacitance	50	100	200	nF

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1. For improved performance, it is recommended to use 10 μF, 0.1 μF and 1nF capacitors in parallel.
2. All decoupling capacitors should be placed as close as possible to the corresponding supply and ground pins.
3. All decoupling capacitors must be low ESR ceramic capacitors(for example X7R type).
4. The requirement and value of C_{DEC} will be decided by the device application requirement.

6.2.6 LVR and LVD Operating Requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVR}	Rising and falling V_{DD} LVR detect voltage	–	2.5	2.7	V	
V_{LVD}	Falling low-voltage threshold(LVDCFG=5)	2.97	3.1	3.4	V	
	Falling low-voltage threshold(LVDCFG=10)	3.7	4.0	4.5	V	
V_{LVD_HYST}	LVD hysteresis(LVD5VHYS=01b)	-2	–	2	%	
	LVD hysteresis(LVD5VHYS=10b)	-4.2	–	4.2	%	
	LVD hysteresis(LVD5VHYS=11b)	-8.4	–	8.4	%	

6.2.7 Power Mode Transition Operating Behaviors

Description	System clock	Core, bus frequency	Min.	Typ.	Max.
SLEEP -> ACTIVE	FIRC	80M/40M	–	500ns	–
DEEPSLEEP -> ACTIVE	FIRC	80M/40M	–	20μs	–
STANDBY -> ACTIVE	FIRC	80M/40M	–	200μs	–
T_{POR}	FIRC(reset value)	80M/40M	–	900μs	–

6.2.8 Power Consumption

Mode	Symbol	Clock configuration	Description	Temperature	Min	Typ	Max	Units
ACTIVE	I_{DD_ACTIVE}	FIRC	Running while(1) loop in flash, all peripheral clock enabled. core @80MHz, bus @40MHz V_{DD}=5V	$\leq$ 25 ℃	–	15.0	35	mA
				$\leq$ 125 ℃	–	15.4	35	mA
			Running while(1) loop in flash, all peripheral clock disabled. core @80MHz, bus @40MHz V_{DD}=5V	$\leq$ 25 ℃	–	12.0	30	mA
				$\leq$ 125 ℃	–	12.6	30	mA
SLEEP	I_{DD_SLEEP}	–	Sleep mode current, V_{DD}=5V	$\leq$ 25 ℃	–	3.8	9	mA
				125 ℃	–	4	13	mA
DEEPSLEEP	$I_{DD_DEEPSLEEP}$	FIRC	Deepsleep mode current, V_{DD}=5V SIRC=1	$\leq$ 25 ℃	–	120.6	185	μA
				125 ℃	–	163.6	260	μA
			Deepsleep mode current, V_{DD}=5V SIRC=0	$\leq$ 25 ℃	–	101.8	165	μA
				125 ℃	–	143.4	240	μA
STANDBY	$I_{DD_STANDBY}$	FIRC	Standby mode current, V_{DD}=5V SIRC=1	$\leq$ 25 ℃	–	23.0	65	μA
				125 ℃	–	43.4	140	μA

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Mode	Symbol	Clock configuration	Description	Temperature	Min	Typ	Max	Units
			Standby mode current, V_{DD}=5V SIRC=0	$\leq$ 25 ℃	–	5	25	μA
				125 ℃	–	70	95	μA

6.2.9 Power Sequence

6.2.9.1 Power Up Sequence

Hardwares must follow sequence below to ensure that the chip is powered up properly.

1. VDD must be powered up first.
2. VDDA must be powered up later than or at the same time as VDD.
3. VREFH must be powered up later than or at the same time as VDDA.

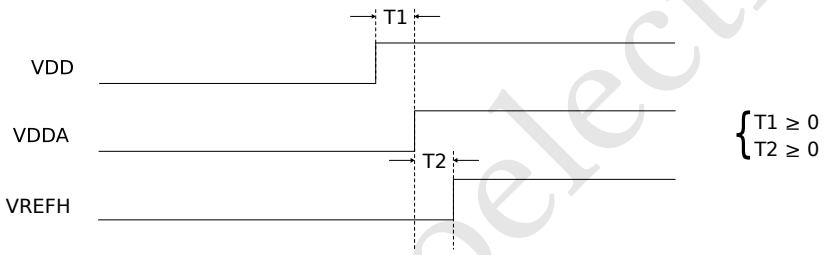


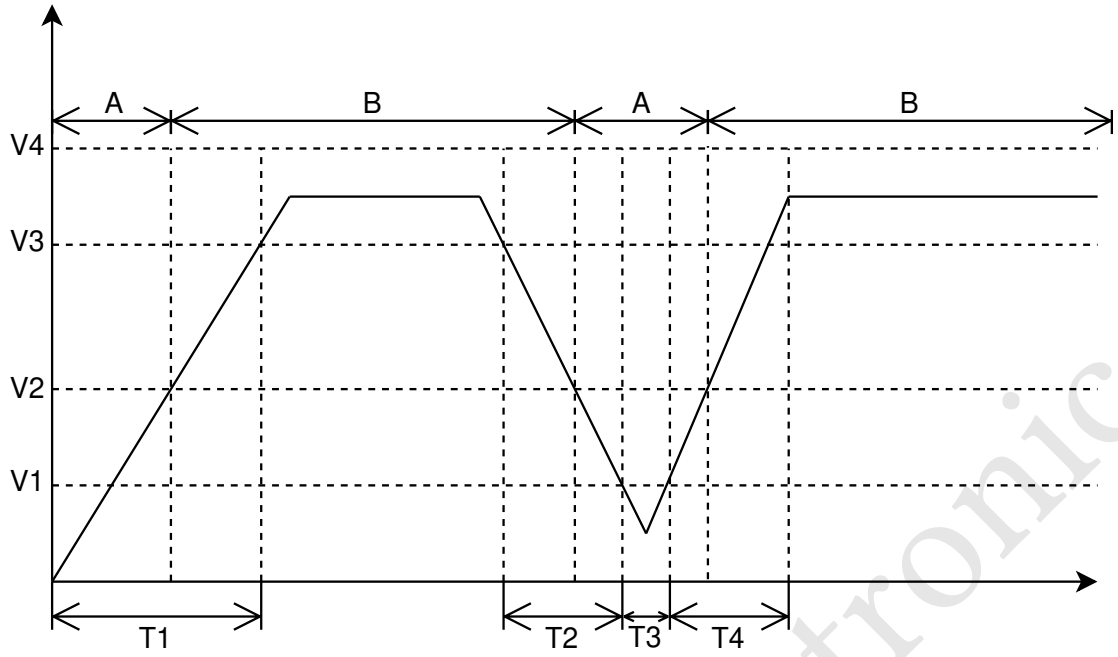
Figure 3: Power Sequence

6.2.9.2 Power Up Requirements

It is necessary to ensure that VDD meets the following timing during the power-up process of YTM32B1MC0x.

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A : There is no guarantee of proper functionality when the MCU is in uncertain status.

B : The MCU operates normally.

Figure 4: Power Up Requirements

Symbol	Name	Description	Unit (V)
V1	Restart threshold voltage	When restarting the MCU, VDD should keep below V1 for a period of T3.	0.9
V2	Minimum MCU operating voltage	The MCU starts working when the power supply reaches V2.	2.5
V3	Lower voltage limit of MCU operating normally	Minimum operating voltage for normal MCU operation and interaction with peripherals.	2.7
V4	Upper voltage limit of MCU operating normally	Maximum operating voltage for normal MCU operation and interaction with peripherals	5.5

Symbol	Name	Description	Requirement
T1	Power up time	Rising time of MCU VDD from 0V to V3	10 μs < T1 < 50ms
T2	Power down time	Drop time of MCU VDD from V3 to V1 during the MCU restart/power down process	10 μs < T2 < 500ms
T3	Restart threshold voltage retain time	Minimum duration of MCU VDD below V1, when restarting MCU	T3 > 100 μs
T4	Restart power up time	Rising time of MCU VDD normal operation from V1 to V3	10 μs < T4 < 50ms

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NOTE: The power-up process needs to be restarted if a VDD voltage drop occurs during the T1~T4 power-up process before the VDD voltage reaches the V2 voltage. Restarting the power-up of MCU needs to ensure that the voltage of VDD continues to drop below V1 and remains there for T3 time.

6.2.10 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance.

6.3 AC Characteristics

6.3.1 Power Supply Fluctuation Requirements

1. The power supply fluctuation must be maintained within ± 10% of the power supply voltage, and the fluctuation frequency should not exceed 100 KHz.
2. The maximum power supply fluctuation should not exceed ± 20% of the power supply voltage, and in this case, the fluctuation frequency should be less than 30 KHz.
3. Power supply fluctuations exceeding the above requirements may cause chip abnormalities and require a power-up process according to the requirements outlined in Power Up Requirements.

6.3.2 Device Clock Specifications

Symbol	Description	Min.	Typ.	Unit	Notes
f_{core}	System and core clock	–	80	MHz	
f_{bus}	Fast bus clock	–	80	MHz	
	Slow bus clock	–	40	MHz	

6.3.3 I/O Electrical Characteristics

6.3.3.1 AC Electrical Characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and the rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

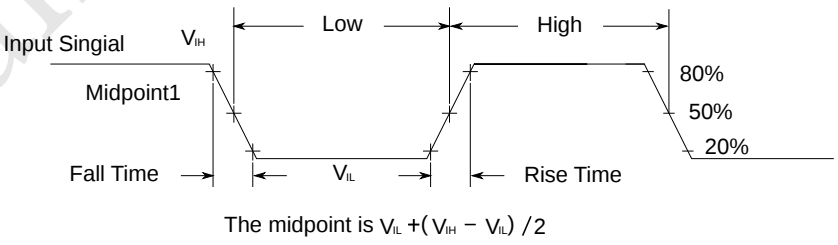


Figure 5: Input Signal Measurement Reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

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- C_L = 30pF loads
- Normal drive strength

6.4 Peripheral Operating Requirements and Behaviors

6.4.1 FXOSC(4~40MHz) Characteristics

The following diagram is Fast Crystal OSC circuit.

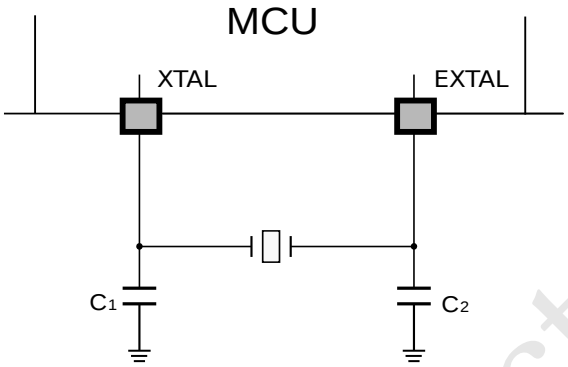


Figure 6: FXOSC Diagram

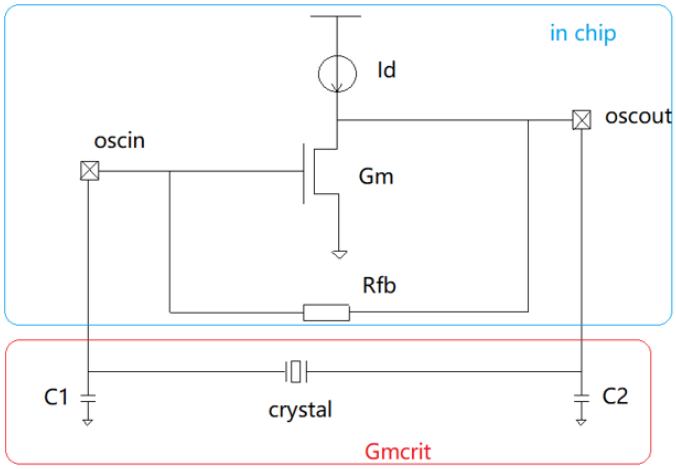
Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.97	–	5.5	V	
V_{IH}	Input high voltage – EXTAL pin in external clock mode, V_{DD}=5.5V	0.7*V_{DD}	–	V_{DD}	V	
	Input high voltage – EXTAL pin in external clock mode, V_{DD}=2.7V	0.7*V_{DD}	–	V_{DD}	V	
V_{IL}	Input low voltage – EXTAL pin in external clock mode, V_{DD}=5.5V	V_{SS}	–	0.3*V_{DD}	V	
	Input low voltage – EXTAL pin in external clock mode, V_{DD}=2.7V	V_{SS}	–	0.3*V_{DD}	V	
$T_{FXOSCSU}$	FXOSC startup time (40MHz oscillator)	–	1	–	ms	
D_{FXOSC}	Duty of FXOSC (40MHz oscillator)	40	–	60	%	
F_{FXOSC}	FXOSC frequency range	4	–	40	MHz	
C_1	Load capacitance	–	–	–	pF	1
C_2	Load capacitance	–	–	–	pF	
R_F	FXOSC internal feedback resistor	–	500	–	kΩ	
V_{PP}	Peak-to-peak amplitude of oscillation (40MHz oscillator) (alc_pd=0)	0.75	–	4.1	V	

1. Crystal oscillator circuit provides stable oscillations when g_{mXOSC} > 5 * gm_crit. The gm_crit is defined as: gm_crit=4 * (ESR + R_S) * $(2\pi F)^2$ * $(C_0 + C_L)^2$

where:

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- g_{mXOSC} is the transcondutance of the internal oscillator circuit
- ESR is the equivalent series resistance of the external crystal
- R_S is the series resistance connected between XTAL pin and external crystal for current limitation
- F is the external crystal oscillation frequency
- C_0 is the shunt capacitance of the external crystal
- C_L is the external crystal total load capacitance. $C_L = C_S + [\ C_1 * C_2 / (C_1 + C_2)\ ]$
- C_S is stray or parasitic capacitance on the pin due to any PCB traces
- C_1, C_2 external load capacitances on EXTAL and XTAL pins.



- The internal circuitry of the chip utilizes an Id current source as the load for the amplifier circuit, with an NMOS transistor serving as the amplifying transistor. When the gain (Gm) of the amplifying transistor is greater than the intrinsic gain (Gmcrit) of the external crystal oscillator, theoretically, the crystal oscillator will start to oscillate. Generally, it is required that Gm>5*Gmcrit.
- Rfb provides the DC bias point for the input terminal of the amplifying transistor.

Figure 7: Block Diagram of Crystal Oscillator Circuit

Table 18: Startup Time - Gain Selection for Gmxosc of 40MHz Crystal Oscillator Circuits (Simulation)

Gain Setting	Gm (at statup)			Unit
	Min.	Typ.	Max.	
0x0			0	mS
0x1	2.04	2.78	3.52	mS
0x2	4.06	5.54	7.01	mS
0x3	6.07	8.27	10.46	mS
0x4	8.07	10.98	13.88	mS
0x5	10.07	13.64	17.21	mS
0x6	12.03	16.29	20.54	mS
0x7	13.99	18.91	23.82	mS

6.4.2 FIRC(80MHz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{FIRC}	Fast internal reference frequency	–	80	–	MHz	

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Symbol	Description	Min.	Typ.	Max.	Unit	Notes
ACC_{FIRC}	FIRC frequency accuracy, factory trimmed, 25 °C	-1.5	–	1.5	%	
	FIRC frequence accuracy, factory trimmed, -40°C – 125°C	-3.0	–	2.0	%	
I_{FIRC}	FIRC operating current	–	350	–	μA	
$T_{Startup}$	Startup time	–	–	20	μs	

6.4.3 SIRC(2MHz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{SIRC}	Slow internal reference frequency	–	2	–	MHz	
ACC_{SIRC}	SIRC frequency accuracy, factory trimmed, 25 °C	-3	–	3	%	
	SIRC frequency accuracy, factory trimmed, 0 °C – 85 °C	-4	–	4	%	
	SIRC frequence accuracy, factory trimmed, −40 °C – 125 °C	-5	–	5	%	
I_{SIRC}	SIRC operating current	–	15	–	μA	
$T_{Startup}$	Startup time	–	20	50	μs	

6.4.4 LPO(32KHz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{LPO}	Low power oscillator frequency	–	32	–	KHz	
ACC_{LPO}	LPO frequency accuracy, factory trimmed, 25 °C	-10	–	10	%	
	LPO frequence accuracy, factory trimmed, −40 °C – 125 °C	-20	–	20	%	

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6.4.5 ADC Characteristics

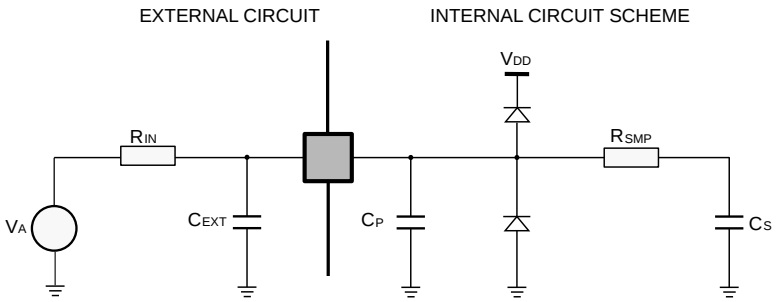


Figure 8: ADC Circuit

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
V_{DDA}	Analog supply voltage		2.97	5.0	5.5	V	
I_{VDDA}	Analog supply current		–	2	–	mA	
ΔV_{DDA}	V_{DD} - V_{DDA}		0	–	100	mV	
V_{REFH}	Reference voltage		2.97	–	V_{DDA}	V	
I_{REFH}	Reference current		–	–	800	μA	
V_{IN}	Input voltage		V_{SS}	–	V_{REFH}	V	
R_{SMP}	Sampling switch impedance		–	–	1.8	kΩ	
C_{EXT}	External capacitance		50	–	–	nF	
C_P	Pin Capacitance		–	6	–	pF	
C_S	Sampling capacitance		–	6	7	pF	

Symbol	Description	Test condition[1]	Min.	Typ.	Max.	Unit	Notes
$T_{STARTUP}$	Analog startup time		5	–	–	μs	
T_{SAMPLE}	Sampling time		200	–	2000	ns	
T_{sample_TS}	Tempsensor sampling time		500	–	2000	ns	

1. Theses parameters of this table can be configured by register, please refer to Reference Manual for details.

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit
DNL	Differential nonlinear	12-bit resolution	–	±1	–	LSB
INL	Integer nonlinear	12-bit resolution	–	±2	–	LSB
ACC_{tempS}	Temperature sensor accuracy		-10		10	°C
K[1]	Slope of temperature and voltage curve	ADC sampling frequncy @ 500kHz		637		°C/V

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Table 24 continued from previous page

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit
F_{ADC}[2]	ADC conversion clock		2		16	MHz

1. T = C - K*V, see Reference Manual for details.
2. ADC conversion clock = ADC function clock / [(ipc_divider +1) * (adc_clock_div +1)]

6.4.6 ACMP Characteristics

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
V_{ACMP}[1]	Analog supply voltage		2.97	5.0	5.5	V	
I_{ACMP}	Analog supply current		–	20	50	μA	Low Power Mode
$V_{INOFFSET}$	Analog input offset voltage		–	–	14	mV	MC Simulation
V_{IN}	Analog input voltage		V_{SS}	–	V_{DDA}	V	
V_{HYST0}	Analog comparator hysteresis 0		12	20	45	mV	
V_{HYST1}	Analog comparator hysteresis 1		20	40	85	mV	
V_{HYST2}	Analog comparator hysteresis 2		36	60	130	mV	
DAC_{DNL}	Differential nonlinear		–	±1	–	LSB	
R_{load_dacbuf}	DAC buffer resistance loading ability		10	–	–	kΩ	
C_{load_dacbuf}	DAC buffer capacitance loading ability		–	–	25	pF	

1. ACMP connects to VDD.

6.4.7 SPI Characteristics[1]

Num.	Symbol	Description	Conditions	Min.	Max.	Unit
	f_{func}[2]	Functional frequency	Slave	–	40	MHz
			Master	–	40	MHz
			Master Loopback[4]	–	40	MHz
1	f_{op}	Frequency of operation	Slave	–	10	MHz
			Master	–	20	MHz
			Master Loopback[4]	–	20	MHz
2	t_{SCK}	SCK period	Slave	100	–	ns
			Master	50	–	ns
			Master Loopback[4]	50	–	ns
3	t_{PCSSCK}[5]	PCS to SCK delay	Slave	–	–	ns
			Master	(PCSSCK+1) * t_{delay}[3] - 35	–	ns
			Master Loopback[4]	(PCSSCK+1) * t_{delay}[3] - 35	–	ns
4	t_{SCKPCS}[6]	After SCK delay	Slave	–	–	ns
			Master	(SCKPCS+1) * t_{delay}[3] - 35	–	ns
			Master Loopback[4]	(SCKPCS+1) * t_{delay}[3] - 35	–	ns
5	t_{WSCK}[7]	Clock (SCK) high or low time	Slave	t_{SCK}/2 - 1	t_{SCK}/2 + 1	ns

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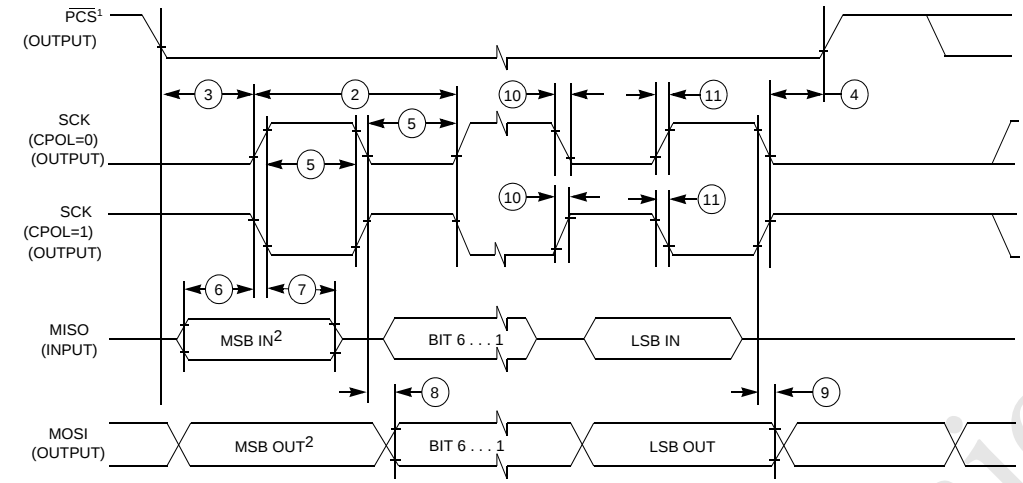
Table 26 continued from previous page

Num.	Symbol	Description	Conditions	Min.	Max.	Unit
			Master	$t_{SCK}/2$ - 1	$t_{SCK}/2$ + 1	ns
			Master Loopback[4]	$t_{SCK}/2$ - 1	$t_{SCK}/2$ + 1	ns
6	t_{setup}	Data setup time (inputs)	Slave	9	–	ns
			Master	14	–	ns
			Master Loopback[4]	6	–	ns
7	t_{holdin}	Data hold time (inputs)	Slave	0	–	ns
			Master	0	–	ns
			Master Loopback[4]	3	–	ns
8	t_{valid}	Data valid (after SCK edge)	Slave	–	25	ns
			Master	–	12	ns
			Master Loopback[4]	–	12	ns
9	$t_{holdout}$	Data hold time (outputs)	Slave	0	–	ns
			Master	0	–	ns
			Master Loopback[4]	0	–	ns
10	$t_{RI/FI}$	Rise/Fall time input	Slave	–	1	ns
			Master	–	1	ns
			Master Loopback[4]	–	1	ns
11	$t_{RO/FO}$	Rise/Fall time output	Slave	–	5	ns
			Master	–	5	ns
			Master Loopback[4]	–	5	ns

1. The trace length for the SCK pad should be kept as short as possible when used in Master loopback mode, and it does not support off-board communication.
2. f_{func} = SPI functional clock, which is generated from IPC.
3. $t_{delay} = (1/f_{op}) * 2^{TXCFG[PRESCALE]}$.
4. Master Loopback mode - In this mode SCK clock is delayed for sampling the input data which is enabled by setting SPI_CTRL[SPDEN] bit as 1.
5. Set the PCSSCK configuration bit as 0, for a minimum of 1 delay cycle of SPI delay clock, where PCSSCK ranges from 0 to 255.
6. Set the SCKPCS configuration bit as 0, for a minimum of 1 delay cycle of SPI delay clock, where SCKPCS ranges from 0 to 255.
7. While selecting odd dividers, ensure Duty Cycle is meeting this parameter.

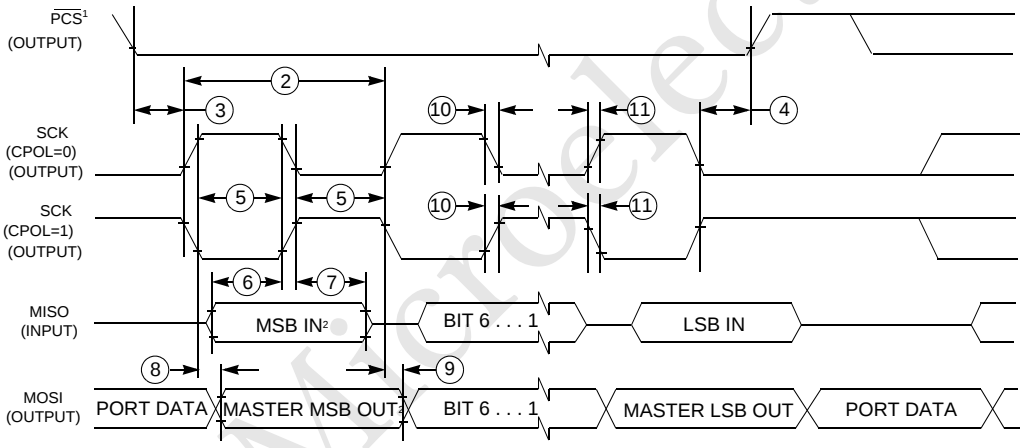
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1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 9: SPI Master Mode Timing (CHPA=0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 10: SPI Master Mode Timing (CHPA=1)

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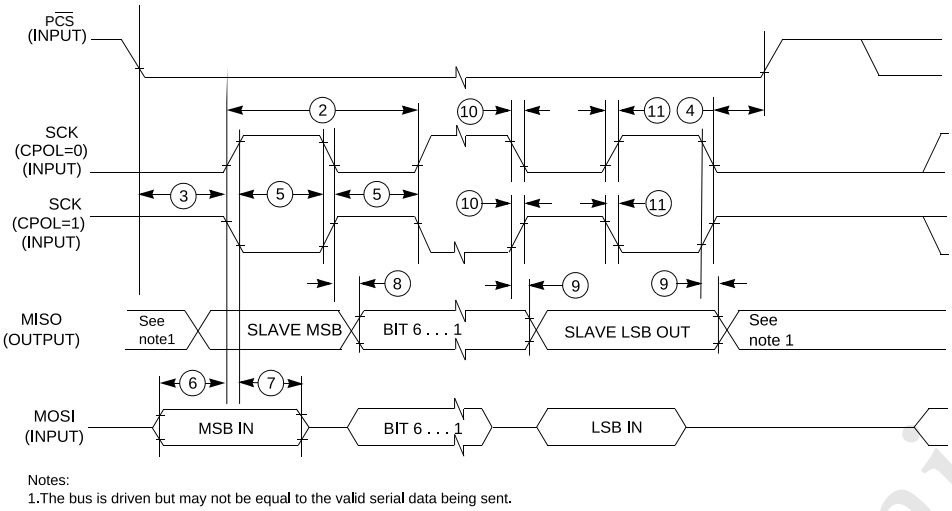


Figure 11: SPI Slave Mode Timing (CHPA=0)

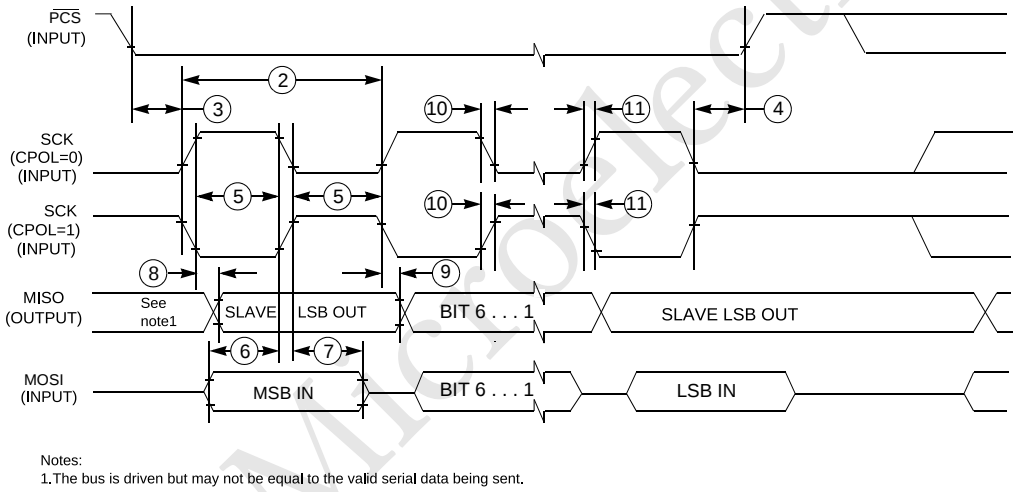


Figure 12: SPI Slave Mode Timing (CHPA=1)

6.4.8 NVM Specifications

6.4.8.1 Flash Command Timing Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
T_{pgm}	Program execution time	158.7	–	164.7	μs	
T_{sector_erase}	Sector erase execution time	2	–	3	ms	
T_{block_erase}	Block erase execution time	30	–	40	ms	

6.4.8.2 Reliability Specifications

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Symbol	Description	Min.	Max.	Unit	Notes
$t_{nvmretp}$	Data retention @25°C	20	–	years	
$t_{nvmcycp}$	Cycling endurance	100K	–	cycles	

6.4.9 Debug Module Electrical

6.4.9.1 SWD Electrical Specifications

Table 29: SWD Full Voltage Range Electricals

Symbol	Description	Min.	Typ.	Max.	Unit
T1	SWD_CLK frequency	–	–	20	MHz
T2	SWD_CLK cycle period	50	–	–	ns
T3	SWD_CLK pulse width	20	–	–	ns
T4	SWD_CLK rise and fall time	–	–	3	ns
T5	SWD_CLK input data setup time to SWD_CLK rise edge	8	–	–	ns
T6	SWD_CLK input data hold time after SWD_CLK rise edge	1.5	–	–	ns
T7	SWD_CLK high to SWD_DIO output data valid	–	–	35	ns
T8	SWD_CLK high to SWD_DIO output data Hi-Z	5	–	–	ns

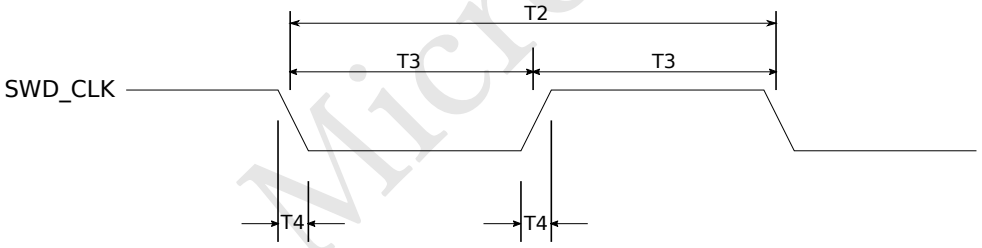


Figure 13: SWD Clock Timing

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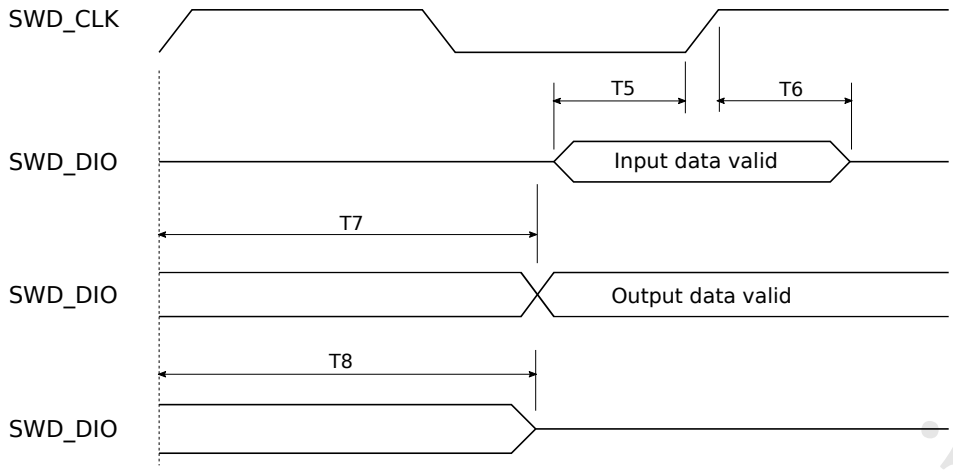


Figure 14: SWD Data Timing

6.4.9.2 JTAG Electrical Specifications

Table 30: JTAG Electrical Specifications

Symbol	Description	Active				Unit
		5.0V IO		3.3V IO		
		Min.	Max.	Min.	Max.	
J1	TCLK frequency					MHz
	Boundary Scan	–	20	–	20	
	JTAG	–	20	–	20	
J2	TCLK cycle period	1/J1	–	1/J1	–	ns
J3	TCLK clock pulse width					ns
	Boundary Scan	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	
	JTAG					
J4	TCLK rise and fall times	–	1	–	1	ns
J5	Boundary scan input data setup time to TCLK rise	5	–	5	–	ns
J6	Boundary scan input data hold time after TCLK rise	5	–	5	–	ns
J7	TCLK low to boundary scan output data valid	–	28	–	32	ns
J8	TCLK low to boundary scan output data invalid	0	–	0	–	ns
J9	TCLK low to boundary scan output high-Z	–	28	–	32	ns
J10	TMS, TDI input data setup time to TCLK rise	3	–	3	–	ns
J11	TMS, TDI input data hold time after TCLK rise	2	–	2	–	ns
J12	TCLK low to TDO data valid	–	28	–	32	ns
J13	TCLK low to TDO data invalid	0	–	0	–	ns
J14	TCLK low to TDO high-Z	–	28	–	28	ns

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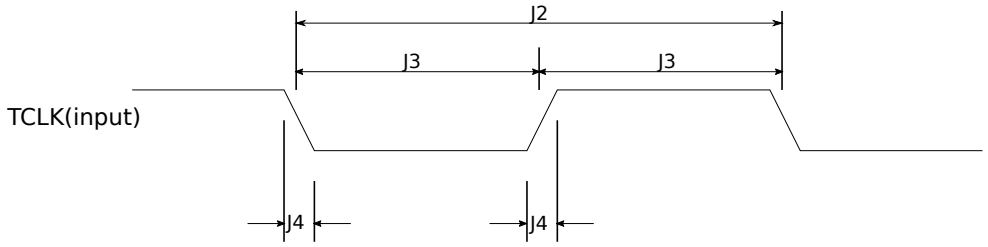


Figure 15: JTAG Clock Timing

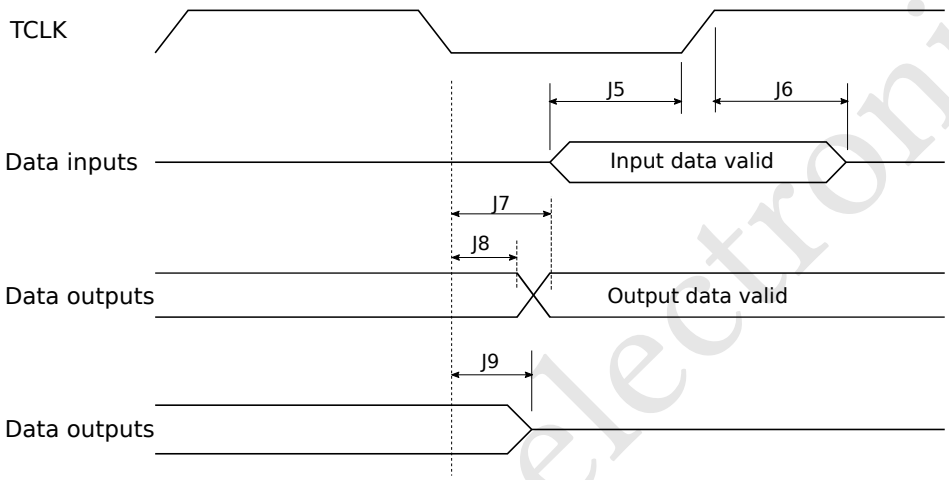


Figure 16: JTAG Data Timing

6.5 Thermal Attributes

Table 31: Thermal Characteristics

Package Family	Package Type	Thermal Resistance		Unit
		R_{JA}	R_{JC}	
LQFP	LQFP48L	78	16	°C/W
	LQFP64L	65	13	°C/W
QFN	QFN48L	30	9	°C/W

7 Pinouts

7.1 IO Signal Description

The pinouts signal description is as follows:

Table 32: Pinmux Table

64LQFP	48LQFP/48QFN	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	1	PTD_1	-	PTD_1	eTMR0_CH3	SPI1_SIN	MPWM0_CH1	I2C1_SCL	-	TMU_OUT2
2	2	PTD_0	-	PTD_0	eTMR0_CH2	SPI1_SCK	MPWM0_CH0	I2C1_SDA	-	TMU_OUT1

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Table 32 continued from previous page

64LQFP	48LQFP/48QFN	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
3	-	PTE_11	-	PTE_11	SPI2_PCS0	lpTMR0_ALT1	MPWM0_CH5	-	-	TMU_OUT5
4	-	PTE_10	-	PTE_10	SCU_CLKOUT	SPI2_PCS1	MPWM0_CH4	-	-	TMU_OUT4
5	3	PTE_5	-	PTE_5	TCLK_IN2	SPI1_PCS1	MPWM0_CH3	CAN0_TX	I2C0_SCL	EWDG_IN
6	4	PTE_4	-	PTE_4	eTMR0_FLT0	SPI1_PCS2	MPWM0_CH2	CAN0_RX	I2C0_SDA	EWDG_OUT_b
7	5	VDD	VDD	-	-	-	-	-	-	-
8	6	VDDA	VDDA	-	-	-	-	-	-	-
9	-	VREFH	VREFH	-	-	-	-	-	-	-
10	7	VSS	VSS	-	-	-	-	-	-	-
11	8	PTB_7	EXTAL	PTB_7	I2C0_SCL	-	-	UART2_TX	-	TMU_OUT2
12	9	PTB_6	XTAL	PTB_6	I2C0_SDA	-	-	UART2_RX	-	TMU_OUT1
13	-	PTE_3	-	PTE_3	eTMR0_FLT0	SPI1_SIN	-	-	TMU_IN6	ACMP0_OUT
14	10	PTD_16	-	PTD_16	eTMR0_CH1	-	SPI0_SIN	ACMP0_ACTIVE	-	-
15	11	PTD_15	-	PTD_15	eTMR0_CH0	-	SPI0_SCK	-	-	-
16	12	PTE_9	-	PTE_9	eTMR0_CH7	SPI1_SCK	-	-	-	-
17	13	PTE_8	ACMP0_IN3	PTE_8	eTMR0_CH6	-	-	-	-	-
18	14	PTB_5	-	PTB_5	eTMR0_CH5	SPI0_PCS1	SPI0_PCS0	SCU_CLKOUT	TMU_IN0	-
19	15	PTB_4	-	PTB_4	eTMR0_CH4	SPI0_SOUT	-	-	TMU_IN1	-
20	16	PTC_3	ADC0_SE11/ACMP0_IN4	PTC_3	eTMR0_CH3	CAN0_TX	UART0_TX	-	-	-
21	17	PTC_2	ADC0_SE10/ACMP0_IN5	PTC_2	eTMR0_CH2	CAN0_RX	UART0_RX	-	-	-
22	-	PTD_7	ACMP0_IN6	PTD_7	UART2_TX	eTMR0_CH3	-	-	-	-
23	-	PTD_6	ACMP0_IN7	PTD_6	UART2_RX	eTMR0_CH2	-	-	-	SPI0_PCS3
24	18	PTD_5	-	PTD_5	MPWM0_CH6	lpTMR0_ALT2	-	SCU_CLKOUT	TMU_IN7	SPI0_PCS1
25	19	PTC_1	ADC0_SE9	PTC_1	eTMR0_CH1	SPI2_SOUT	-	-	eTMR1_CH7	-
26	-	PTC_0	ADC0_SE8	PTC_0	eTMR0_CH0	SPI2_SIN	-	-	eTMR1_CH6	-
27	-	PTC_17	ADC0_SE15	PTC_17	eTMR1_FLT3	-	-	-	-	-
28	20	PTC_16	ADC0_SE14	PTC_16	eTMR1_FLT2	-	-	-	-	-
29	21	PTC_15	ADC0_SE13	PTC_15	eTMR1_CH3	SPI2_SCK	-	-	TMU_IN8	-
30	22	PTC_14	ADC0_SE12	PTC_14	eTMR1_CH2	SPI2_PCS0	-	-	TMU_IN9	-
31	23	PTB_3	ADC0_SE7	PTB_3	eTMR1_CH1	SPI0_SIN	eTMR1_QD_PHA	-	TMU_IN2	-
32	24	PTB_2	ADC0_SE6	PTB_2	eTMR1_CH0	SPI0_SCK	eTMR1_QD_PHB	-	TMU_IN3	-
33	25	PTB_1	ADC0_SE5	PTB_1	UART0_TX	SPI0_SOUT	TCLK_IN0	CAN0_TX	lpTMR0_ALT1	-
34	26	PTB_0	ADC0_SE4	PTB_0	UART0_RX	SPI0_PCS0	lpTMR0_ALT3	CAN0_RX	-	-
35	27	PTC_9	-	PTC_9	UART1_TX	eTMR1_FLT1	eTMR0_FLT1	UART0_RTS	-	-
36	28	PTC_8	DAC0_OUT	PTC_8	UART1_RX	eTMR1_FLT0	-	UART0_CTS	-	-
37	29	PTA_7	ADC0_SE3	PTA_7	eTMR0_FLT2	SPI1_PCS3	-	UART1_RTS	-	-
38	-	PTA_6	ADC0_SE2	PTA_6	eTMR0_FLT1	SPI1_PCS1	-	UART1_CTS	-	-
39	-	PTE_7	-	PTE_7	eTMR0_CH7	SPI1_PCS2	-	-	-	-
40	30	VSS	VSS	-	-	-	-	-	-	-
41	31	VDD	VDD	-	-	-	-	-	-	-
42	32	PTB_13	ADC0_SE24	PTB_13	eTMR0_CH1	-	-	UART1_CTS	-	-
43	-	PTB_12	ADC0_SE23	PTB_12	eTMR0_CH0	-	-	-	-	-
44	-	PTD_4	ADC0_SE22	PTD_4	eTMR0_FLT3	-	-	-	-	-
45	33	PTD_3	ADC0_SE19	PTD_3	MPWM0_CH5	SPI1_PCS0	I2C1_SCL	UART1_TX	TMU_IN4	CM33_NMI_b
46	34	PTD_2	ADC0_SE18	PTD_2	MPWM0_CH4	SPI1_SOUT	I2C1_SDA	UART1_RX	TMU_IN5	-
47	35	PTA_3	ADC0_SE17	PTA_3	MPWM0_CH1	I2C0_SCL	EWDG_IN	SPI2_SCK	UART0_TX	-
48	36	PTA_2	ADC0_SE16	PTA_2	MPWM0_CH0	I2C0_SDA	EWDG_OUT_b	SPI2_SIN	UART0_RX	-
49	37	PTA_1	ADC0_SE1/ACMP0_IN1	PTA_1	eTMR1_CH1	SPI2_SOUT	-	eTMR1_QD_PHA	UART0_RTS	TMU_OUT0
50	38	PTA_0	ADC0_SE0/ACMP0_IN0	PTA_0	MPWM0_CH7	SPI2_PCS0	-	eTMR1_QD_PHA	UART0_CTS	TMU_OUT3
51	39	PTC_7	ADC0_SE21	PTC_7	UART1_TX	CAN1_TX	MPWM0_CH3	SPI2_PCS2	eTMR1_QD_PHA	-
52	40	PTC_6	ADC0_SE20	PTC_6	UART1_RX	CAN1_RX	MPWM0_CH2	SPI2_PCS3	eTMR1_QD_PHB	-
53	-	PTE_6	ADC0_SE26	PTE_6	SPI0_PCS2	-	MPWM0_CH7	UART1_RTS	-	-
54	-	PTE_2	ADC0_SE25	PTE_2	SPI0_SOUT	lpTMR0_ALT3	MPWM0_CH6	UART1_CTS	-	-
55	41	PTA_13	-	PTA_13	eTMR1_CH7	CAN1_TX	-	UART2_TX	-	-
56	42	PTA_12	-	PTA_12	eTMR1_CH6	CAN1_RX	-	UART2_RX	-	-
57	43	PTA_11	-	PTA_11	eTMR1_CH5	-	-	ACMP0_ACTIVE	I2C1_SCL	-
58	44	PTA_10	-	PTA_10	eTMR1_CH4	-	-	-	I2C1_SDA	JTAG_TDO
59	-	PTE_1	-	PTE_1	SPI0_SIN	-	I2C1_SCL	SPI1_PCS0	eTMR1_FLT1	-
60	-	PTE_0	-	PTE_0	SPI0_SCK	TCLK_IN1	I2C1_SDA	SPI1_SOUT	eTMR1_FLT2	-
61	45	PTC_5	-	PTC_5	MPWM0_CH4	-	-	-	-	JTAG_TDI
62	46	PTC_4	ACMP0_IN2	PTC_4	eTMR1_CH0	-	-	EWDG_IN	eTMR1_QD_PHB	JTAG_TCK_SWD_CLK
63	47	PTA_5	-	PTA_5	-	TCLK_IN1	-	-	eTMR1_QD_PHB	RESET_b
64	48	PTA_4	-	PTA_4	-	-	ACMP0_OUT	EWDG_OUT_b	-	JTAG_TMS_SWD_IO

7.2 Packages

The information of package pinouts is as follows:

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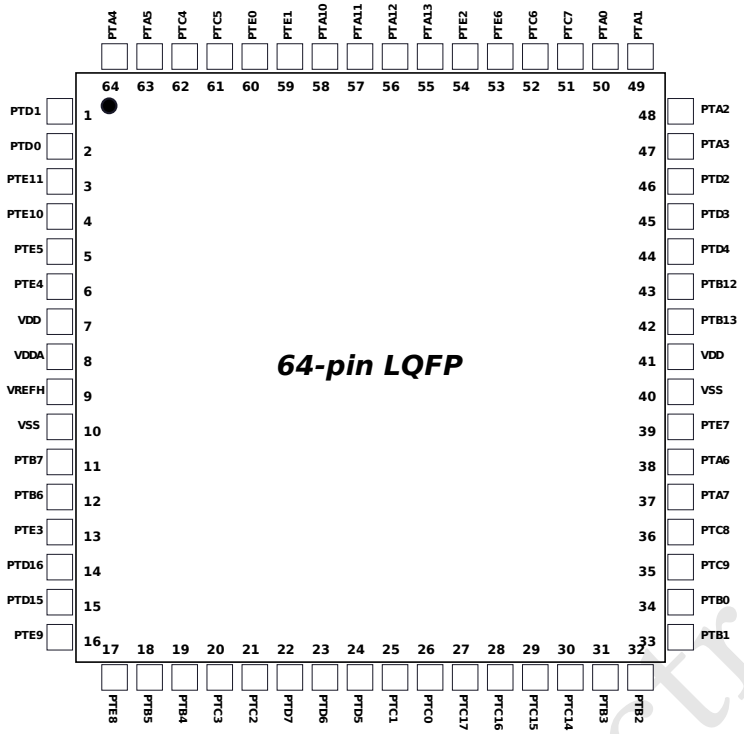


Figure 17: 64-pin LQFP Package

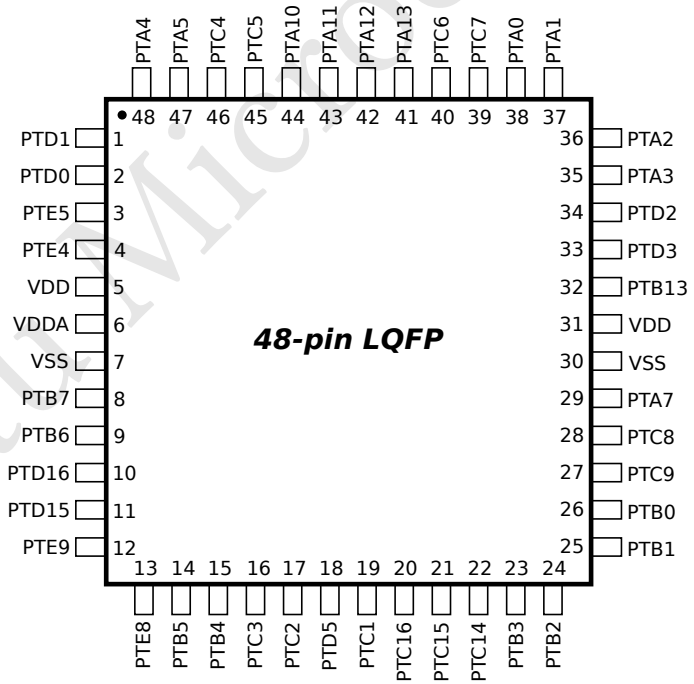


Figure 18: 48-pin LQFP Package

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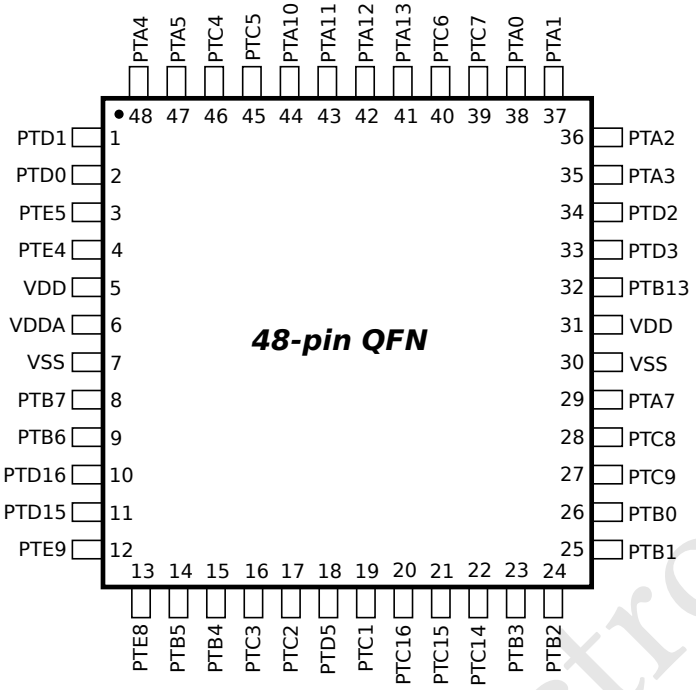


Figure 19: 48pin QFN

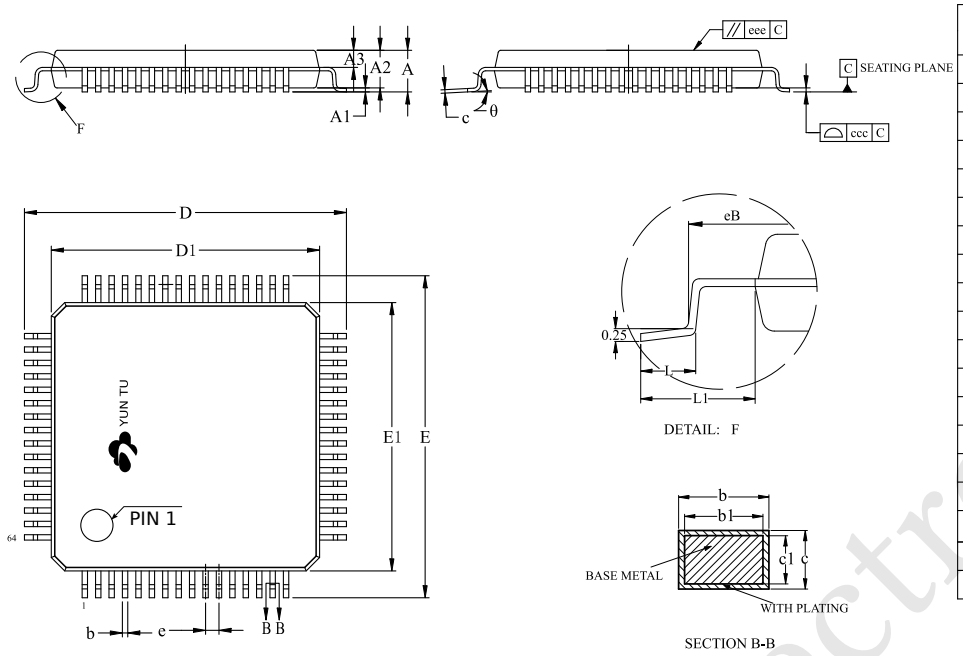
Note: The chip mark will not contain packing information(T/R)

7.3 Dimensions

Package dimensions are as follows:

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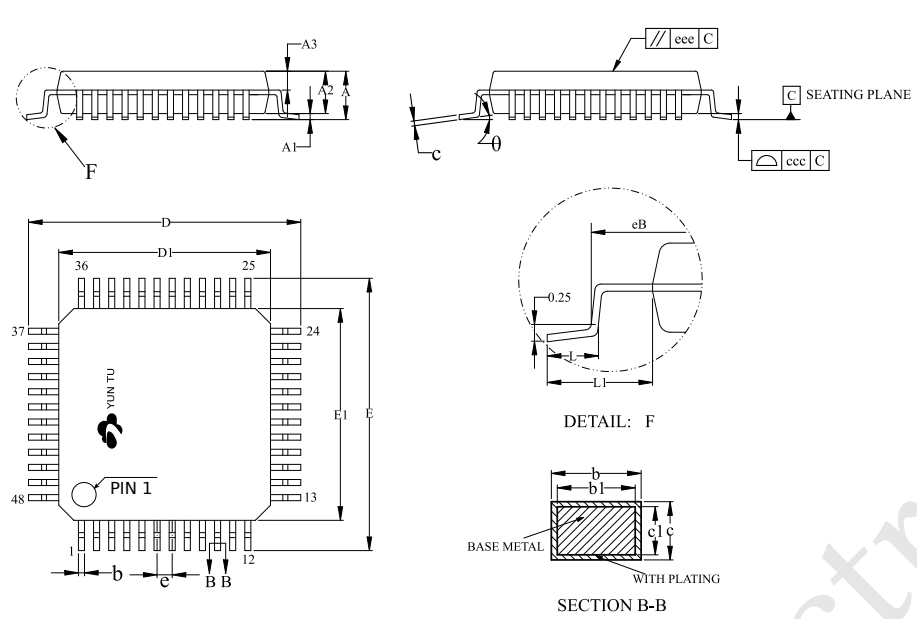


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
eB	11.05	—	11.25
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°
eee	0.10		
ccc	0.08		

Figure 20: 64pin LQFP

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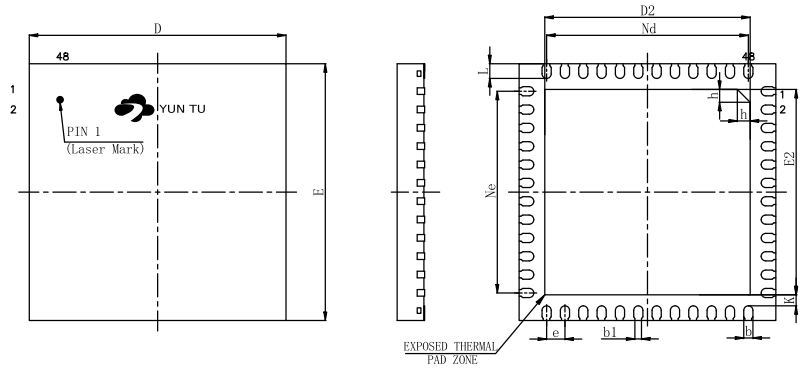


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	—	8.25
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°
eee	0.10		
ccc	0.08		

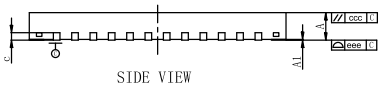
Figure 21: 48pin LQFP

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SYMBOL	MILLIMETER		
	MIN	NOM	MAX
● A	0.80	0.85	0.90
● A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.18REF	
c		0.203REF	
● D	6.90	7.00	7.10
D2	5.50	5.60	5.70
e		0.50BSC	
Ne		5.50BSC	
Nd		5.50BSC	
● E	6.90	7.00	7.10
E2	5.50	5.60	5.70
L	0.35	0.40	0.45
h	0.30	0.35	0.40
K		0.30REF	
ccc		0.10	
eee		0.08	



** **Special Design Note:**
The items maked with " ● " (A/D/E/A1) are key characteristics.
The above projects must comply with the management and control requirements of automotive electronic projects.

Figure 22: 48pin QFN

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Revision History

The following table provides a revision history for this document.

Rev.No.	Date	Substantive Change(s)
1.0	2023/12/25	Initial version
1.1	2023/1/23	In the chapter “Features Summary”, added the information of “RoHS compliant”. In the chapter “Block Diagram”, added the information of temperature sensor. In the subsection “DC Electrical Specifications at 3.3V”, updated the values of I_{IN} . In the subsection “DC Electrical Specifications at 5V”, updated the values of I_{IN} and I_{leak}. In the subsection “FIRC (80MHz) Characteristics”, updated the values. In the subsection “SIRC (2MHz) Characteristics”, updated the values. In the subsection “Power Consumption”, updated the values of SLEEP and STANDBY. In the subsection “ADC Characteristics”, added the information of temperature sensor and updated the values. In the subsection “ACMP Characteristics”, updated the values of I_{ACMP} and $V_{INOFFSET}$. In the section “Dimensions”, updated the figure of 48pin QFN.
1.2	2024/2/26	In the chapter “Ordering information”, updated the part number and ADC channels of “Ordering Table”. In the section “Part Number Information”, updated the table of “Part Number Field Description”. In the subsection “DC Electrical Specifications at 3.3V”, added the values of I_{leak} . In the subsection “DC Electrical Specifications at 5V”, updated the value of I_{leak}. In the subsubsection “Flash Command Timing Specifications”, updated the Min and Max values of T_{pgm}.
1.3	2024/7/17	In the subsection “Power and Ground Pins”, updated the figure and table. In the subsection “POR, LVR and LVD Operating Requirements”, updated the table. In the subsection “Power Sequence”, added the content about power up requirements. In the section of “Dimensions”, updated all package dimensions to the lateset version.
1.4	2025/5/7	Updated supply voltage 2.7V to 2.97V in the whole Data Sheet Added Min and Max value in subsection of “Moisture Handling Ratings” Updated Min and Max value in subsection of “ESD Handling Ratings” Updated the Max value of I_{VDD} in subsection of “Absolute Maximum Ratings” Added Min and Max value in subsection of “Voltage and Current Operating Requirements” Added Min and Max value in subsection of “DC Electrical Specifications at 3.3V” Added Min and Max value in subsection of “DC Electrical Specifications at 5.0V” Added Min and Max value in subsection of “Power and Ground Pins” Updated the Min value in subsubsection of “LVR and LVD Operating Requirements” Added Min and Max value in subsection of “Power Consumption” Added the whole subsection of “Power Supply Fluctuation Requirements” Added Min and Max value in subsection of “FXOSC(4-40MHz) Characteristics” Added Min and Max value in subsection of “FIRC(48MHz) Characteristics” Added Max value of $T_{Startup}$ in subsection of “SIRC(2MHz) Characteristics” Removed the subsubsection of “Flash High Voltage Current Behaviors” Updated the Min value in subsubsection of “Reliability Specifications” Added Min and Max value in subsection of “ADC Characteristics” Added Min and Max value in subsection of “ACMP Characteristics” Added the whole subsection of “SPI Characteristics” Added R_{JC} data in section of “Thermal Attributes” Added the PIN1 location and YUNTU logo to the section of “Dimensions”

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