## *Table of Contents-*

1. GENERAL DESCRIPTION ..... 6
2. FEATURES ..... 6
3. ORDER INFORMATION ..... 6
4. BALL ASSIGNMENT ..... 7
5. BALL CONFIGURATION ..... 8
5.1 Ball Description ..... 8
5.2 Addressing Table ..... 9
6. BLOCK DIAGRAM ..... 10
7. FUNCTIONAL DESCRIPTION ..... 11
7.1 Simplified LPDDR2 State Diagram ..... 11
7.1.1 Simplified LPDDR2 Bus Interface State Diagram ..... 12
7.2 Power-up, Initialization, and Power-Off ..... 13
7.2.1 Power Ramp and Device Initialization ..... 13
7.2.2 Timing Parameters for Initialization ..... 15
7.2.3 Power Ramp and Initialization Sequence ..... 15
7.2.4 Initialization after Reset (without Power ramp) ..... 16
7.2.5 Power-off Sequence ..... 16
7.2.6 Timing Parameters Power-Off ..... 16
7.2.7 Uncontrolled Power-Off Sequence ..... 16
7.3 Mode Register Definition ..... 17
7.3.1 Mode Register Assignment and Definition ..... 17
7.3.1.1 Mode Register Assignment ..... 17
7.3.2 MR0_Device Information (MA[7:0] = 00H) ..... 18
7.3.3 MR1_Device Feature 1 (MA[7:0] = 01H) ..... 18
7.3.3.1 Burst Sequence by Burst Length (BL), Burst Type (BT), and Warp Control (WC) ..... 19
7.3.3.2 Non Wrap Restrictions ..... 19
7.3.4 MR2_Device Feature 2 (MA[7:0] = 02H) ..... 20
7.3.5 MR3_I/O Configuration 1 (MA[7:0] = 03H) ..... 20
7.3.6 MR4_Device Temperature (MA[7:0] = 04H) ..... 20
7.3.7 MR5_Basic Configuration 1 (MA[7:0] = 05H) ..... 21
7.3.8 MR6_Basic Configuration 2 (MA[7:0] = 06H) ..... 21
7.3.9 MR7_Basic Configuration 3 (MA[7:0] = 07H) ..... 21
7.3.10 MR8_Basic Configuration 4 (MA[7:0] = 08H) ..... 21
7.3.11 MR9_Test Mode (MA[7:0] = 09H) ..... 21
7.3.12 MR10_Calibration (MA[7:0] = 0AH) ..... 22
7.3.13 MR16_PASR_Bank Mask (MA[7:0] = 10H) ..... 22
7.3.14 MR32_DQ Calibration Pattern A (MA[7:0] = 20H) ..... 23
7.3.15 MR40_DQ Calibration Pattern B (MA[7:0] = 28H) ..... 23
7.3.16 MR63_Reset (MA[7:0] = 3FH): MRW only ..... 23
7.4 Command Definitions and Timing Diagrams ..... 23
7.4.1 Activate Command ..... 23
7.4.1.1 Activate Command Cycle: tRCD = 3, tRP = 3, tRRD = 2 ..... 23
7.4.1.2 Command Input Setup and Hold Timing ..... 24
7.4.1.3 CKE Input Setup and Hold Timing ..... 24
7.4.2 Read and Write Access Modes ..... 25
7.4.3 Burst Read Command ..... 25
7.4.3.1 Data Output (Read) Timing (tDQSCKmax) ..... 25
7.4.3.2 Data Output (Read) Timing (tDQSCKmin) ..... 26
7.4.3.3 Burst Read: RL = 5, BL = 4, tDQSCK > tCK ..... 26
7.4.3.4 Burst Read: RL = 3, BL = 8, tDQSCK < tCK ..... 27
7.4.3.5 LPDDR2: tDQSCKDL Timing ..... 27
7.4.3.6 LPDDR2: tDQSCKDM Timing ..... 28

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7.4.3.7 LPDDR2: tDQSCKDS Timing ..... 28
7.4.3.8 Burst Read Followed by Burst Write: RL = 3, WL = 1, BL = 4 ..... 29
7.4.3.9 Seamless Burst Read: RL = 3, BL= 4, tCCD = 2 ..... 29
7.4.4 Reads Interrupted by a Read ..... 30
7.4.4.1 Read Burst Interrupt Example: RL = 3, BL= 8, tCCD = 2 ..... 30
7.4.5 Burst Write Operation ..... 30
7.4.5.1 Data Input (Write) Timing ..... 31
7.4.5.2 Burst Write: WL = 1, BL= 4 ..... 31
7.4.5.3 Burst Write Followed by Burst Read: RL = 3, WL= 1, BL= 4 ..... 32
7.4.5.4 Seamless Burst Write: WL= 1, BL = 4, tCCD = 2 ..... 32
7.4.6 Writes Interrupted by a Write ..... 33
7.4.6.1 Write Burst Interrupt Timing: WL = 1, BL = 8, tCCD = 2 ..... 33
7.4.7 Burst Terminate ..... 33
7.4.7.1 Burst Write Truncated by BST: WL = 1, BL = 16 ..... 34
7.4.7.2 Burst Read Truncated by BST: RL = 3, BL = 16 ..... 34
7.4.8 Write Data Mask ..... 35
7.4.8.1 Write Data Mask Timing ..... 35
7.4.9 Precharge Operation ..... 36
7.4.9.1 Bank Selection for Precharge by Address Bits ..... 36
7.4.10 Burst Read Operation Followed by Precharge ..... 36
7.4.10.1 Burst Read Followed by Precharge: RL = 3, BL = 8, RU(tRTP(min)/tCK) = 2 ..... 37
7.4.10.2 Burst Read Followed by Precharge: RL = 3, BL = 4, RU(tRTP(min)/tCK) = 3 ..... 37
7.4.11 Burst Write Followed by Precharge ..... 38
7.4.11.1 Burst Write Followed by Precharge: WL = 1, BL = 4 ..... 38
7.4.12 Auto Precharge Operation ..... 39
7.4.13 Burst Read with Auto-Precharge ..... 39
7.4.13.1 Burst Read with Auto-Precharge: RL = 3, BL = 4, RU(tRTP(min)/tCK) = 2 ..... 39
7.4.14 Burst Write with Auto-Precharge ..... 40
7.4.14.1 Burst Write with Auto-Precharge: WL = 1, BL = 4 ..... 40
7.4.14.2 Precharge & Auto Precharge Clarification ..... 41
7.4.15 Refresh Command ..... 42
7.4.15.1 Command Scheduling Separations Related to Refresh ..... 42
7.4.16 LPDDR2 SDRAM Refresh Requirements ..... 43
7.4.16.1 Definition of tSRF ..... 43
7.4.16.2 Regular, Distributed Refresh Pattern ..... 44
7.4.16.3 Allowable Transition from Repetitive Burst Refresh ..... 45
7.4.16.4 NOT-Allowable Transition from Repetitive Burst Refresh ..... 45
7.4.16.5 Recommended Self-Refresh Entry and Exit ..... 46
7.4.16.6 All Bank Refresh Operation ..... 46
7.4.17 Self Refresh Operation ..... 47
7.4.18 Partial Array Self-Refresh: Bank Masking ..... 48
7.4.19 Mode Register Read Command ..... 49
7.4.19.1 Mode Register Read Timing Example: RL = 3, tMRR = 2 ..... 49
7.4.19.2 Read to MRR Timing Example: RL = 3, tMRR = 2 ..... 50
7.4.19.3 Burst Write Followed by MRR: RL = 3, WL = 1, BL = 4 ..... 50
7.4.20 Temperature Sensor ..... 51
7.4.20.1 Temperature Sensor Timing ..... 52
7.4.20.2 DQ Calibration ..... 52
7.4.20.3 MR32 and MR40 DQ Calibration Timing Example: RL = 3, tMRR = 2 ..... 53
7.4.21 Mode Register Write Command ..... 54
7.4.21.1 Mode Register Write Timing Example: RL = 3, tMRW = 5 ..... 54
7.4.21.2 Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW) ..... 54
7.4.22 Mode Register Write Reset (MRW Reset) ..... 55
7.4.23 Mode Register Write ZQ Calibration Command ..... 55
7.4.23.1 ZQ Calibration Initialization Timing Example ..... 56
7.4.23.2 ZQ Calibration Short Timing Example ..... 56



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7.4.23.3 ZQ Calibration Long Timing Example ..... 57
7.4.23.4 ZQ Calibration Reset Timing Example ..... 57
7.4.23.5 ZQ External Resistor Value, Tolerance, and Capacitive Loading ..... 58
7.4.24 Power-Down ..... 58
7.4.24.1 Basic Power Down Entry and Exit Timing ..... 58
7.4.24.2 CKE Intensive Environment ..... 59
7.4.24.3 Refresh to Refresh Timing with CKE Intensive Environment ..... 59
7.4.24.4 Read to Power-Down Entry ..... 60
7.4.24.5 Read with Auto Precharge to Power-Down Entry ..... 60
7.4.24.6 Write to Power-Down Entry ..... 61
7.4.24.7 Write with Auto Precharge to Power-Down Entry ..... 61
7.4.24.8 Refresh Command to Power-Down Entry ..... 62
7.4.24.9 Activate Command to Power-Down Entry ..... 62
7.4.24.10 Precharge/Precharge-All Command to Power-Down Entry ..... 62
7.4.24.11 Mode Register Read to Power-Down Entry ..... 63
7.4.24.12 MRW Command to Power-Down Entry ..... 63
7.4.25 Deep Power-Down ..... 63
7.4.25.1 Deep Power Down Entry and Exit Timing ..... 64
7.4.26 Input Clock Stop and Frequency Change ..... 64
7.4.27 No Operation Command ..... 65
7.5 Truth Tables ..... 65
7.5.1 Command Truth Table ..... 66
7.5.2 CKE Truth Table ..... 67
7.5.3 Current State Bank n - Command to Bank n Truth Table ..... 68
7.5.4 Current State Bank n - Command to Bank m Truth Table ..... 70
7.5.5 Data Mask Truth Table ..... 71
8. ELECTRICAL CHARACTERISTIC ..... 72
8.1 Absolute Maximum DC Ratings ..... 72
8.2 AC & DC Operating Conditions ..... 72
8.2.1 Recommended DC Operating Conditions ..... 72
8.2.1.1 Recommended DC Operating Conditions ..... 72
8.2.2 Input Leakage Current ..... 73
8.2.3 Operating Temperature Conditions ..... 73
8.2.4 AC and DC Input Measurement Levels ..... 73
8.2.4.1 AC and DC Logic Input Levels for Single-Ended Signals ..... 73
8.2.4.1.1 Single-Ended AC and DC Input Levels for CA and CS_n Inputs ..... 73
8.2.4.1.2 Single-Ended AC and DC Input Levels for CKE ..... 74
8.2.4.1.3 Single-Ended AC and DC Input Levels for DQ and DM ..... 74
8.2.4.2 Vref Tolerances ..... 74
8.2.4.2.1 VRef(DC) Tolerance and VRef AC-Noise Limits ..... 75
8.2.4.3 Input Signal ..... 76
8.2.4.3.1 LPDDR2-800/1066 Input Signal ..... 76
8.2.4.4 AC and DC Logic Input Levels for Differential Signals ..... 77
8.2.4.4.1 Differential Signal Definition ..... 77
8.2.4.4.2 Differential swing requirements for clock (CK_t - CK_c) and strobe (DQS_t - DQS_c) ..... 77
8.2.4.5 Single-Ended Requirements for Differential Signals ..... 78
8.2.4.6 Differential Input Cross Point Voltage ..... 79
8.2.4.7 Slew Rate Definitions for Single-Ended Input Signals ..... 80
8.2.4.8 Slew Rate Definitions for Differential Input Signals ..... 80
8.2.5 AC and DC Output Measurement Levels ..... 81
8.2.5.1 Single Ended AC and DC Output Levels ..... 81
8.2.5.2 Differential AC and DC Output Levels ..... 81
8.2.5.3 Single Ended Output Slew Rate ..... 81
8.2.5.4 Differential Output Slew Rate ..... 83
8.2.5.5 Overshoot and Undershoot Specifications ..... 84


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8.2.6 Output buffer Characteristics ..... 85
8.2.6.1 HSUL_12 Driver Output Timing Reference Load ..... 85
8.2.6.2 $RON_{PU}$ and $RON_{PD}$ Resistor Definition ..... 85
8.2.6.3 $RON_{PU}$ and $RON_{PD}$ Characteristics with ZQ Calibration ..... 86
8.2.6.4 Output Driver Temperature and Voltage Sensitivity ..... 86
8.2.6.5 $RON_{PU}$ and $RON_{PD}$ Characteristics without ZQ Calibration ..... 87
8.2.6.6 RZQ I-V Curve ..... 88
8.2.6.7 Input/Output Capacitance ..... 90
8.3 IDD Specification Parameters and Test Conditions ..... 91
8.3.1 IDD Measurement Conditions ..... 91
8.3.1.1 Definition of Switching for CA Input Signals ..... 91
8.3.1.2 Definition of Switching for IDD4R ..... 92
8.3.1.3 Definition of Switching for IDD4W ..... 92
8.3.2 IDD Specifications ..... 93
8.3.2.1 LPDDR2 IDD Specification Parameters and Operating Conditions, -40°C~85°C (x16, x32) ..... 93
8.3.2.2 IDD6 Partial Array Self-Refresh Current, (x16, x32) ..... 95
8.4 Clock Specification ..... 95
8.4.1 Definition for tCK(avg) and nCK ..... 95
8.4.2 Definition for tCK(abs) ..... 95
8.4.3 Definition for tCH(avg) and tCL(avg) ..... 96
8.4.4 Definition for tJIT(per) ..... 96
8.4.5 Definition for tJIT(cc) ..... 96
8.4.6 Definition for tERR(nper) ..... 96
8.4.7 Definition for Duty Cycle Jitter tJIT(duty) ..... 97
8.4.8 Definition for tCK(abs), tCH(abs) and tCL(abs) ..... 97
8.5 Period Clock Jitter ..... 97
8.5.1 Clock Period Jitter Effects on Core Timing Parameters ..... 97
8.5.1.1 Cycle Time De-rating for Core Timing Parameters ..... 97
8.5.1.2 Clock Cycle De-rating for Core Timing Parameters ..... 98
8.5.2 Clock Jitter Effects on Command/Address Timing Parameters ..... 98
8.5.3 Clock Jitter Effects on Read Timing Parameters ..... 98
8.5.3.1 tRPRE ..... 98
8.5.3.2 tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS) ..... 98
8.5.3.3 tQSH, tQSL ..... 98
8.5.3.4 tRPST ..... 99
8.5.4 Clock Jitter Effects on Write Timing Parameters ..... 99
8.5.4.1 tDS, tDH ..... 99
8.5.4.2 tDSS, tDSH ..... 99
8.5.4.3 tDQSS ..... 99
8.6 Refresh Requirements ..... 100
8.6.1 Refresh Requirement Parameters ..... 100
8.7 AC Timings ..... 101
8.7.1 LPDDR2 AC Timing ..... 101
8.7.2 CA and CS_n Setup, Hold and Derating ..... 106
8.7.2.1 CA and CS_n Setup and Hold Base-Values for 1V/nS ..... 106
8.7.2.2 Derating Values LPDDR2 tIS/tIH - AC/DC Based AC220 ..... 107
8.7.2.3 Required Time tVAC above VIH(ac) {below VIL(ac)} for Valid Transition ..... 107
8.7.2.4 Nominal Slew Rate and tVAC for Setup Time tIS for CA and CS_n with Respect to Clock ..... 108
8.7.2.5 Nominal Slew Rate for Hold Time tIH for CA and CS_n with Respect to Clock ..... 109
8.7.2.6 Tangent Line for Setup Time tIS for CA and CS_n with Respect to Clock ..... 110
8.7.2.7 Tangent Line for Hold Time tIH for CA and CS_n with Respect to Clock ..... 111
8.7.3 Data Setup, Hold and Slew Rate Derating ..... 112
8.7.3.1 Data Setup and Hold Base-Values ..... 112
8.7.3.2 Derating Values LPDDR2 tDS/tDH - AC/DC Based AC220 ..... 113
8.7.3.3 Required Time tVAC above VIH(ac) {below VIL(ac)} for Valid Transition ..... 113


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8.7.3.4 Nominal Slew Rate and tVAC for Setup Time tDS for DQ with Respect to Strobe ..... 114
8.7.3.5 Nominal Slew Rate for Hold time tDH for DQ with Respect to Strobe ..... 115
8.7.3.6 Tangent Line for Setup Time tDS for DQ with Respect to Strobe ..... 116
8.7.3.7 Tangent Line for Hold Time tDH for DQ with Respect to Strobe ..... 117
9. PACKAGE DIMENSIONS ..... 118
10. REVISION HISTORY ..... 119


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## 1. GENERAL DESCRIPTION

LPDDR2 is a high-speed SDRAM device internally configured as a 4-Bank memory. These devices contains 256Mb has 268,435,456 bits.

All LPDDR2 devices use a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

For LPDDR2 devices, accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

## 2. FEATURES

- $V_{DD1}$ = 1.7~1.95V
- $V_{DD2}$/$V_{DDCA}$/$V_{DDQ}$ = 1.14V~1.30V
- Data width: x16 / x32
- Clock rate: up to 533 MHz
- Data rate: up to 1066 Mbs
- Four-bit prefetch DDR architecture
- Four internal banks
- Programmable READ and WRITE latencies (RL/WL)
- Programmable burst lengths: 4, 8, or 16
- Auto refresh: All bank refresh mode only
- Partial Array Self-Refresh (PASR):
  All bank or per bank, bank mask is supported but segment mask is not supported
- Precharge command: All bank or per bank
- Read with auto-precharge
- Write with auto-precharge
- Deep Power Down Mode (DPD Mode)
- Programmable output buffer driver strength
- Data mask (DM) for write data
- Clock Stop capability during idle periods
- Double data rate for data output
- Differential clock inputs
- Bidirectional differential data strobe
- Interface: HSUL_12
- JEDEC LPDDR2-S4B compliance
- Support package:
  Single channel: VFBGA 134 ball (10mm x11.5mm)
- Operating Temperature Range:
  -40°C ≤ $T_{CASE}$ ≤ 85°C
  -25°C ≤ $T_{CASE}$ ≤ 85°C

## 3. ORDER INFORMATION

| Part Number | VDD1/VDD2/VDDQ | I/O Width | Package | Others |
|---|---|---|---|---|
| W978H6KBVX2I | 1.8V/1.2V/1.2V | 16 | VFBGA 134 ball | LPDDR2-800, -40°C~85°C |
| W978H2KBVX2I | 1.8V/1.2V/1.2V | 32 | VFBGA 134 ball | LPDDR2-800, -40°C~85°C |
| W978H6KBVX1I | 1.8V/1.2V/1.2V | 16 | VFBGA 134 ball | LPDDR2-1066, -40°C~85°C |
| W978H2KBVX1I | 1.8V/1.2V/1.2V | 32 | VFBGA 134 ball | LPDDR2-1066, -40°C~85°C |
| W978H6KBVX2E | 1.8V/1.2V/1.2V | 16 | VFBGA 134 ball | LPDDR2-800, -25°C~85°C |
| W978H2KBVX2E | 1.8V/1.2V/1.2V | 32 | VFBGA 134 ball | LPDDR2-800, -25°C~85°C |
| W978H6KBVX1E | 1.8V/1.2V/1.2V | 16 | VFBGA 134 ball | LPDDR2-1066, -25°C~85°C |
| W978H2KBVX1E | 1.8V/1.2V/1.2V | 32 | VFBGA 134 ball | LPDDR2-1066, -25°C~85°C |


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## 4. BALL ASSIGNMENT

**[Top View]**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | DNU | DNU | | | | | | | DNU | DNU | A |
| B | DNU | NC | NC | | VDD2 | VDD1 | DQ31<br>NC | DQ29<br>NC | DQ26<br>NC | DNU | B |
| C | VDD1 | VSS | NC | | VSS | VSSQ | VDDQ | DQ25<br>NC | VSSQ | VDDQ | C |
| D | VSS | VDD2 | ZQ0 | | VDDQ | DQ30<br>NC | DQ27<br>NC | DQS3_t<br>NC | DQS3_c<br>NC | VSSQ | D |
| E | VSSCA | CA9 | CA8 | | DQ28<br>NC | DQ24<br>NC | DM3<br>NC | DQ15 | VDDQ | VSSQ | E |
| F | VDDCA | CA6 | CA7 | | VSSQ | DQ11 | DQ13 | DQ14 | DQ12 | VDDQ | F |
| G | VDD2 | CA5 | Vref(CA) | | DQS1_c | DQS1_t | DQ10 | DQ9 | DQ8 | VSSQ | G |
| H | VDDCA | VSS | CK_c | | DM1 | VDDQ | | | | | H |
| J | VSSCA | NC | CK_t | | VSSQ | VDDQ | VDD2 | VSS | Vref(DQ) | | J |
| K | CKE0 | NC | NC | | DM0 | VDDQ | | | | | K |
| L | CS0_n | NC | NC | | DQS0_c | DQS0_t | DQ5 | DQ6 | DQ7 | VSSQ | L |
| M | CA4 | CA3 | CA2 | | VSSQ | DQ4 | DQ2 | DQ1 | DQ3 | VDDQ | M |
| N | VSSCA | VDDCA | CA1 | | DQ19<br>NC | DQ23<br>NC | DM2<br>NC | DQ0 | VDDQ | VSSQ | N |
| P | VSS | VDD2 | CA0 | | VDDQ | DQ17<br>NC | DQ20<br>NC | DQS2_t<br>NC | DQS2_c<br>NC | VSSQ | P |
| R | VDD1 | VSS | NC | | VSS | VSSQ | VDDQ | DQ22<br>NC | VSSQ | VDDQ | R |
| T | DNU | NC | NC | | VDD2 | VDD1 | DQ16<br>NC | DQ18<br>NC | DQ21<br>NC | DNU | T |
| U | DNU | DNU | | | | | | | DNU | DNU | U |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |

| Ball Definition where 2 labe's are present | |
|---|---|
| 1st Row | x32 device |
| 2nd Row | x16 device |

- LPDDR2 DQ
- LPDDR2 CA
- Power
- Ground
- Do Not Use /NC
- ZQ
- Clock


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# 5. BALL CONFIGURATION

## 5.1 Ball Description

| Name | Type | Description |
|---|---|---|
| CK_t, CK_c | Input | **Clock:** CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge.<br>Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c. |
| CKE | Input | **Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions.<br>CKE is considered part of the command code. See 7.5.1 **"Command Truth Table"** for command code descriptions.<br>CKE is sampled at the positive Clock edge. |
| CS_n | Input | **Chip Select:** CS_n is considered part of the command code. See 7.5.1 **"Command Truth Table"** for command code descriptions.<br>CS_n is sampled at the positive Clock edge. |
| CA[9:0] | Input | **DDR Command/Address Inputs:** Uni-directional command/address bus inputs.<br>CA is considered part of the command code. See 7.5.1 **"Command Truth Table"** for command code descriptions. |
| DQ[n:0] | I/O | **Data Inputs/Output:** Bi-directional data bus. n=15 for 16 bits DQ; n=31 for 32 bits DQ. |
| DQSn_t, DQSn_c | I/O | **Data Strobe (Bi-directional, Differential):**<br>The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data.<br>For x16, DQS0_t and DQS0_c correspond to the data on DQ0-7; DQS1_t and DQS1_c to the data on DQ8-15.<br>For x32 DQS0_t and DQS0_c correspond to the data on DQ0-7; DQS1_t and DQS1_c to the data on DQ8-15; DQS2_t and DQS2_c to the data on DQ16-23; DQS3_t and DQS3_c to the data on DQ24-31. |
| DMn | Input | **Input Data Mask:**<br>DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS_t. Although DM is for input only, the DM loading shall match the DQ and DQS (or DQS_c).<br>DM0 is the input data mask signal for the data on DQ0-7.<br>For x16 and x32 devices, DM1 is the input data mask signal for the data on DQ8-15.<br>For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31. |
| $V_{DD1}$ | Supply | **Core Power Supply 1:** Power supply for core. |
| $V_{DD2}$ | Supply | **Core Power Supply 2:** Power supply for core. |
| $V_{DDCA}$ | Supply | **Input Receiver Power Supply:** Power supply for CA[n:0], CKE, CS_n, CK_t, and CK_c input buffers. |
| $V_{DDQ}$ | Supply | **I/O Power Supply:** Power supply for Data input/output buffers. |
| $V_{REF(CA)}$ | Supply | **Reference Voltage for CA Command and Control Input Receiver:** Reference voltage for all CA[n:0], CKE, CS_n, CK_t, and CK_c input buffers. |
| $V_{REF(DQ)}$ | Supply | **Reference Voltage for DQ Input Receiver:** Reference voltage for all Data input buffers. |
| $V_{SS}$ | Supply | **Ground** |
| $V_{SSCA}$ | Supply | **Ground for CA Input Receivers** |
| $V_{SSQ}$ | Supply | **I/O Ground** |
| ZQ | I/O | **Reference Pin for Output Drive Strength Calibration** |

**Note:** Data includes DQ and DM.


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## 5.2 Addressing Table

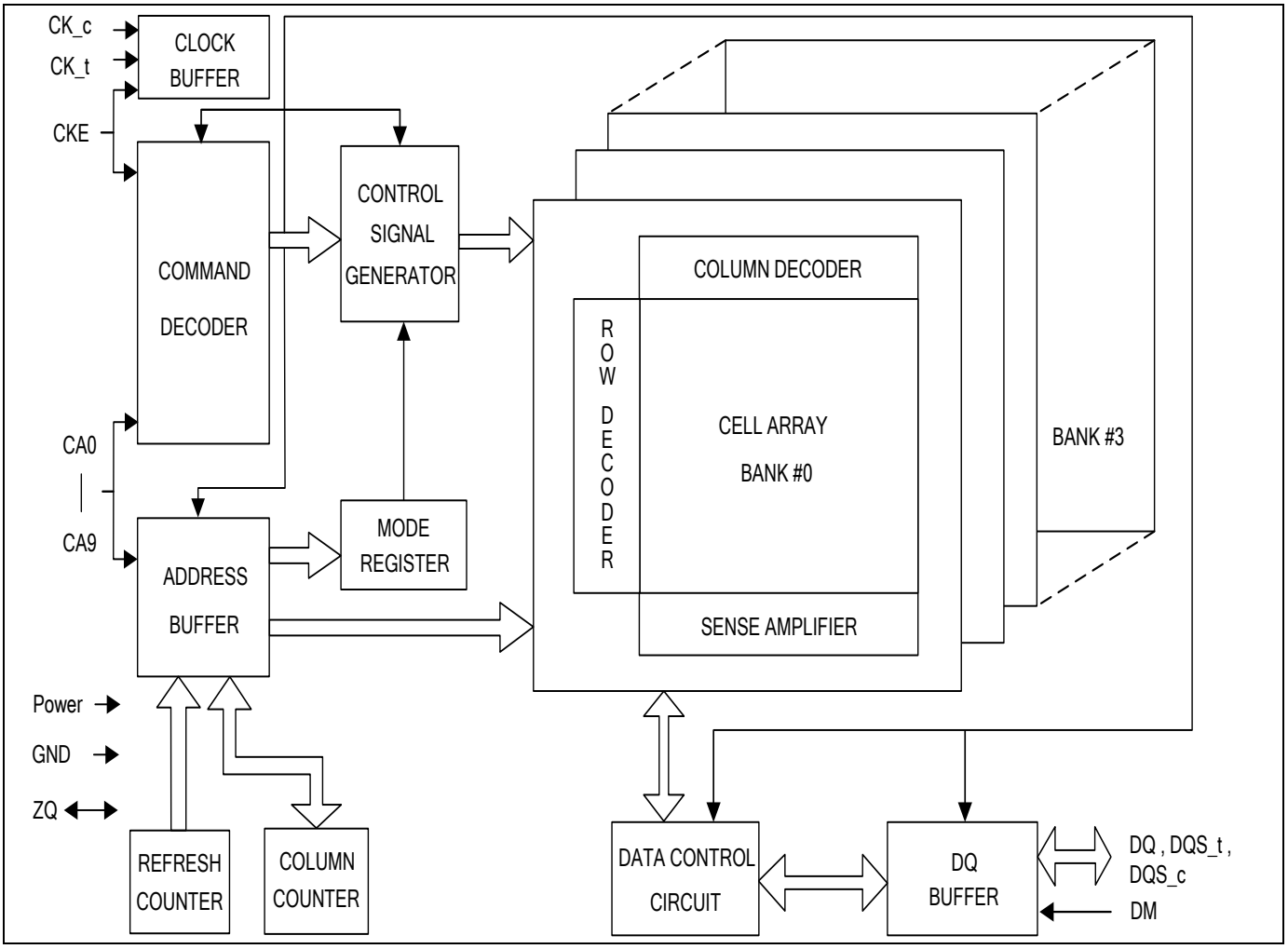
| Density | | 256Mb |
|---|---|---|
| Number of Banks | | 4 |
| Bank Addresses | | BA0-BA1 |
| x16 | Row Addresses | R0-R12 |
| | Column Addresses*1 | C0-C8 |
| x32 | Row Addresses | R0-R12 |
| | Column Addresses*1 | C0-C7 |

**Notes:**

1. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
2. Row and Column Address values on the CA bus that are not used are “don’t care”.


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## 6. BLOCK DIAGRAM



# 7. FUNCTIONAL DESCRIPTION

LPDDR2-S4 devices use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4n-bit-wide, one-clock-cycle data transfer at the internal SDRAM core and four corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Prior to normal operation, the LPDDR2 device must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

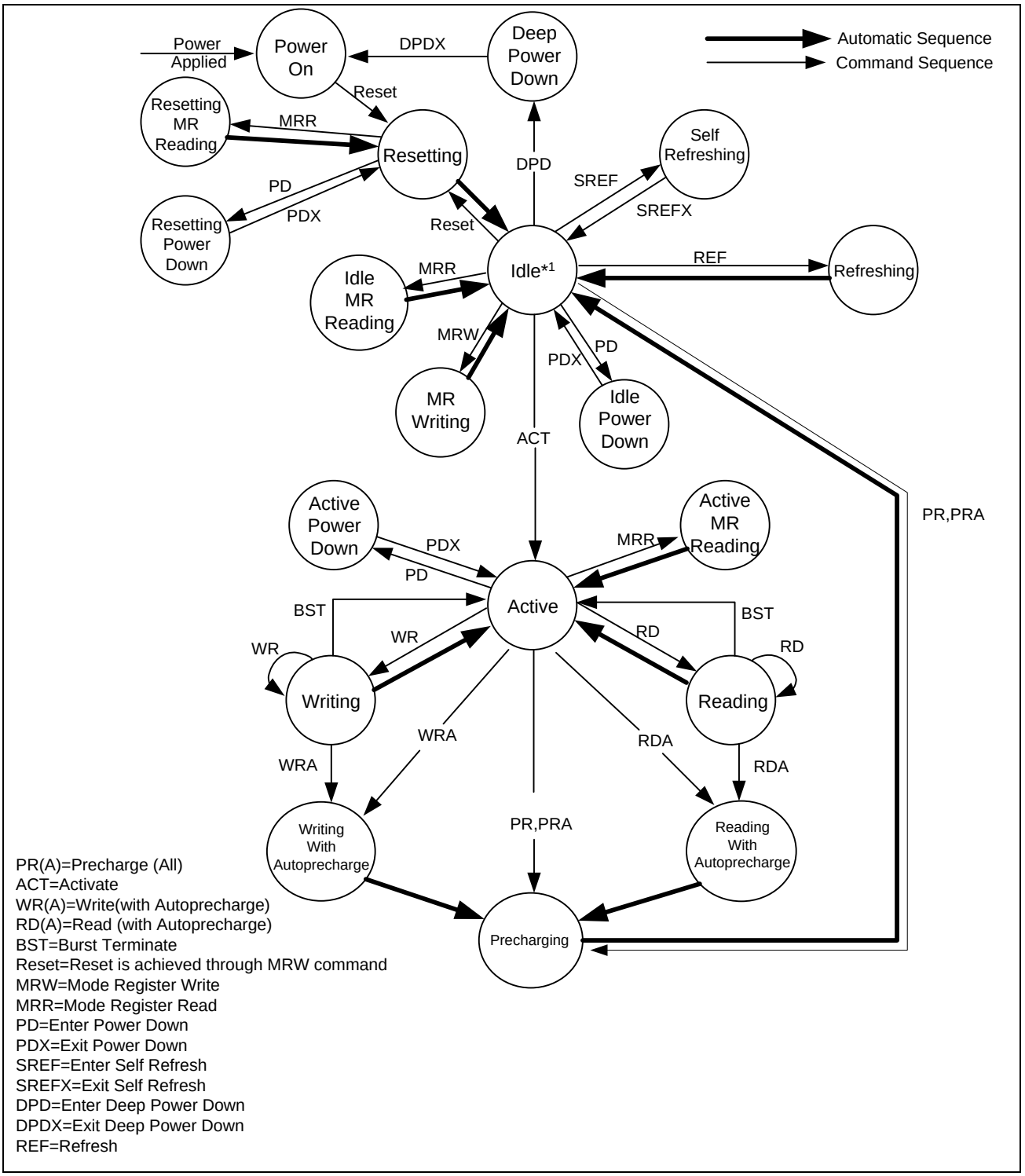
## 7.1 Simplified LPDDR2 State Diagram

LPDDR2-SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.


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### 7.1.1 Simplified LPDDR2 Bus Interface State Diagram




**Note:** For LPDDR2-SDRAM in the Idle state, all banks are precharged.

## 7.2 Power-up, Initialization, and Power-Off

The LPDDR2 Devices must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

### 7.2.1 Power Ramp and Device Initialization

The following sequence shall be used to power up an LPDDR2 device. Unless specified otherwise, these steps are mandatory.

**1. Power Ramp**

While applying power (after Ta), CKE shall be held at a logic low level (≤ 0.2 x $V_{DDCA}$), all other inputs shall be between $V_{IL}$min and $V_{IH}$max. The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.

On or before the completion of the power ramp (Tb) CKE must be held low.

DQ, DM, DQS_t and DQS_c voltage levels must be between $V_{SSQ}$ and $V_{DDQ}$ during voltage ramp to avoid latchup. CK_t, CK_c, CS_n, and CA input levels must be between $V_{SSCA}$ and $V_{DDCA}$ during voltage ramp to avoid latch-up.

The following conditions apply:

Ta is the point where any power supply first reaches 300mV.

After Ta is reached, $V_{DD1}$ must be greater than $V_{DD2}$ - 200mV.

After Ta is reached, $V_{DD1}$ and $V_{DD2}$ must be greater than $V_{DDCA}$ - 200mV.

After Ta is reached, $V_{DD1}$ and $V_{DD2}$ must be greater than $V_{DDQ}$ - 200mV.

After Ta is reached, $V_{REF}$ must always be less than all other supply voltages.

The voltage difference between any of $V_{SS}$, $V_{SSQ}$, and $V_{SSCA}$ pins may not exceed 100mV.

The above conditions apply between Ta and power-off (controlled or uncontrolled).

Tb is the point when all supply voltages are within their respective min/max operating conditions. Reference voltages shall be within their respective min/max operating conditions a minimum of 5 clocks before CKE goes high.

For supply and reference voltage operating conditions, see 8.2.1.1 **"Recommended DC Operating Conditions"** table.

Power ramp duration $t_{INIT0}$ (Tb - Ta) must be no greater than 20 mS.

**2. CKE and clock**

Beginning at Tb, CKE must remain low for at least $t_{INIT1}$ = 100 nS, after which it may be asserted high. Clock must be stable at least $t_{INIT2}$ = 5 x $t_{CK}$ prior to the first low to high transition of CKE (Tc). CKE, CS_n and CA inputs must observe setup and hold time ($t_{IS}$, $t_{IH}$) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).

The clock period shall be within the range defined for $t_{CKb}$ (18 nS to 100 nS), if any Mode Register Reads are performed. Mode Register Writes can be sent at normal clock operating frequencies so long as all AC Timings are met. Furthermore, some AC parameters (e.g. $t_{DQSCK}$) may have relaxed timings (e.g. $t_{DQSCKb}$) before the system is appropriately configured.

While keeping CKE high, issue NOP commands for at least $t_{INIT3}$ = 200 µS. (Td).


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**3. Reset command**

After tINIT3 is satisfied, a MRW(Reset) command shall be issued (Td). The memory controller may optionally issue a Precharge-All command prior to the MRW Reset command. Wait for at least tINIT4 = 1 µS while keeping CKE asserted and issuing NOP commands.

**4. Mode Registers Reads and Device Auto-Initialization (DAI) polling:**

After tINIT4 is satisfied (Te) only MRR commands and power-down entry/exit commands are allowed. Therefore, after Te, CKE may go low in accordance to Power-Down entry and exit specification (see section 7.4.24 **"Power-Down"**).

The MRR command may be used to poll the DAI-bit to acknowledge when Device Auto-Initialization is complete or the memory controller shall wait a minimum of tINIT5 before proceeding.

As the memory output buffers are not properly configured yet, some AC parameters may have relaxed timings before the system is appropriately configured.

After the DAI-bit (MR#0, "DAI") is set to zero "DAI complete" by the memory device, the device is in idle state (Tf). The state of the DAI status bit can be determined by an MRR command to MR#0.

The LPDDR2 SDRAM device will set the DAI-bit no later than tINIT5 (10 µS) after the Reset command. The memory controller shall wait a minimum of tINIT5 or until the DAI-bit is set before proceeding.

After the DAI-Bit is set, it is recommended to determine the device type and other device characteristics by issuing MRR commands (MR0 "Device Information" etc.).

**5. ZQ Calibration:**

After tINIT5 (Tf), an MRW ZQ Initialization Calibration command may be issued to the memory (MR10). This command is used to calibrate the LPDDR2 output drivers (RON) over process, voltage, and temperature. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection. In systems in which more than one LPDDR2 device exists on the same bus, the controller must not overlap ZQ Calibration commands. The device is ready for normal operation after tZQINIT.

**6. Normal Operation:**

After tZQINIT (Tg), MRW commands may be used to properly configure the memory, for example the output buffer driver strength, latencies etc. Specifically, MR1, MR2, and MR3 shall be set to configure the memory for the target frequency and memory configuration.

The LPDDR2 device will now be in IDLE state and ready for any valid command.

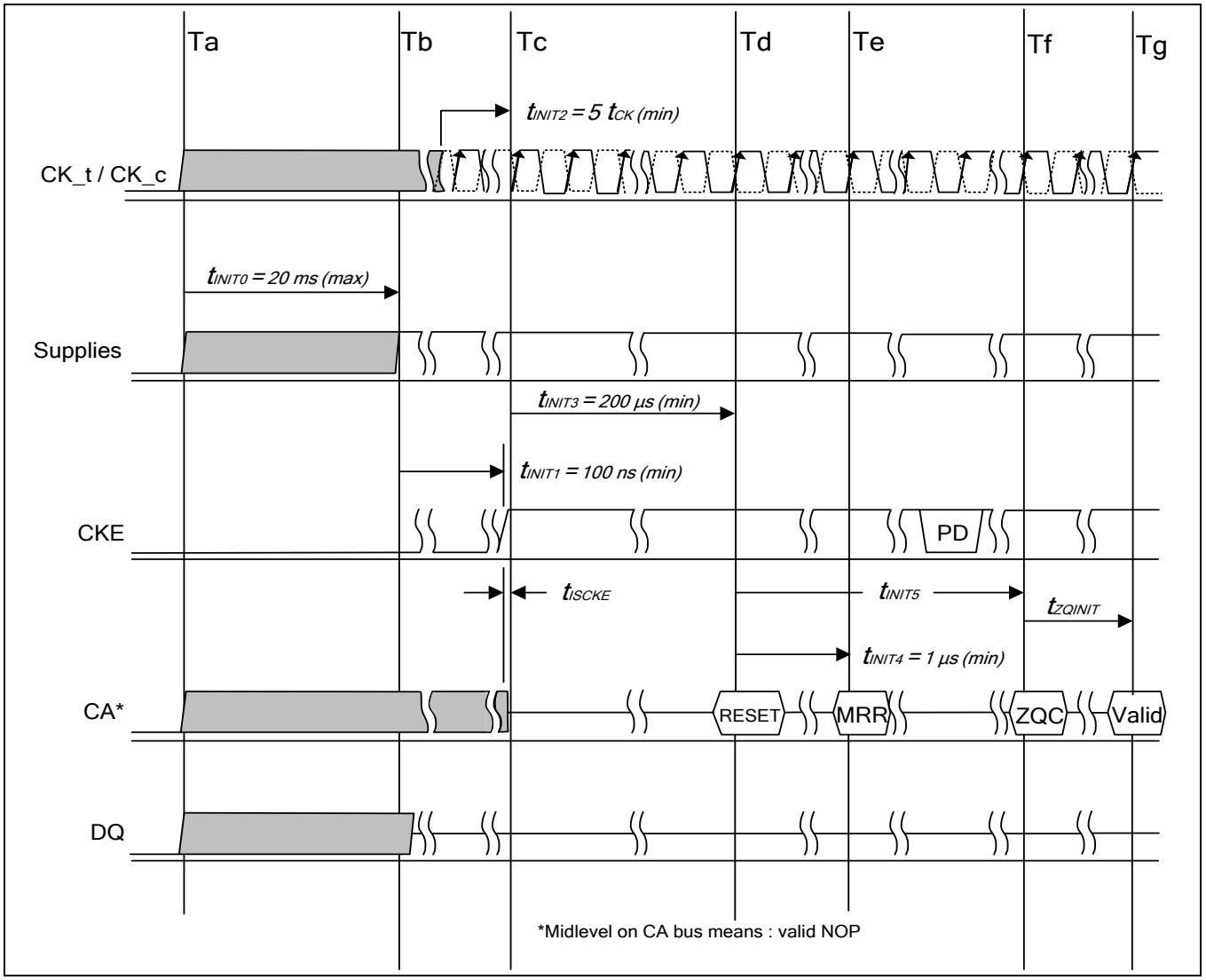
After Tg, the clock frequency may be changed according to the clock frequency change procedure described in section 7.4.26 **"Input Clock Stop and Frequency Change"**.


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### 7.2.2 Timing Parameters for Initialization

| Symbol | Value | | Unit | Comment |
|---|---|---|---|---|
| | min | max | | |
| tINIT0 | | 20 | mS | Maximum Power Ramp Time |
| tINIT1 | 100 | | nS | Minimum CKE low time after completion of power ramp |
| tINIT2 | 5 | | tCK | Minimum stable clock before first CKE high |
| tINIT3 | 200 | | µS | Minimum Idle time after first CKE assertion |
| tINIT4 | 1 | | µS | Minimum Idle time after Reset command |
| tINIT5 | | 10 | µS | Maximum duration of Device Auto-Initialization |
| tZQINIT | 1 | | µS | ZQ Initial Calibration for LPDDR2-S4 |
| tCKb | 18 | 100 | nS | Clock cycle time during boot |

### 7.2.3 Power Ramp and Initialization Sequence





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### 7.2.4 Initialization after Reset (without Power ramp)

If the RESET command is issued outside the power up initialization sequence, the reinitialization procedure shall begin with step 3 (Td).

### 7.2.5 Power-off Sequence

The following sequence shall be used to power off the LPDDR2 device.

While removing power, CKE shall be held at a logic low level (≤ 0.2 x $V_{DDCA}$), all other inputs shall be between $V_{IL}$min and $V_{IH}$max. The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.

DQ, DM, DQS_t and DQS_c voltage levels must be between $V_{SSQ}$ and $V_{DDQ}$ during power off sequence to avoid latch-up. CK_t, CK_c, CS_n and CA input levels must be between $V_{SSCA}$ and $V_{DDCA}$ during power off sequence to avoid latch-up.

Tx is the point where any power supply decreases under its minimum value specified in 8.2.1.1 **"Recommended DC Operating Conditions"** table.

Tz is the point where all power supplies are below 300 mV. After Tz, the device is powered off.

The time between Tx and Tz ($t_{POFF}$) shall be less than 2s.

The following conditions apply:
Between Tx and Tz, $V_{DD1}$ must be greater than $V_{DD2}$ - 200 mV.
Between Tx and Tz, $V_{DD1}$ and $V_{DD2}$ must be greater than $V_{DDCA}$ - 200 mV.
Between Tx and Tz, $V_{DD1}$ and $V_{DD2}$ must be greater than $V_{DDQ}$ - 200 mV.
Between Tx and Tz, $V_{REF}$ must always be less than all other supply voltages.
The voltage difference between any of $V_{SS}$, $V_{SSQ}$, and $V_{SSCA}$ pins may not exceed 100 mV.
For supply and reference voltage operating conditions, see 8.2.1.1 **"Recommended DC Operating Conditions"** table.

### 7.2.6 Timing Parameters Power-Off

| Symbol | Value | | Unit | Comment |
|---|---|---|---|---|
| | min | max | | |
| $t_{POFF}$ | - | 2 | s | Maximum Power-Off Ramp Time |

### 7.2.7 Uncontrolled Power-Off Sequence

The following sequence shall be used to power off the LPDDR2 device under uncontrolled condition.

Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table. After turning off all power supplies, any power supply current capacity must be zero, except for any static charge remaining in the system.

Tz is the point where all power supply first reaches 300 mV. After Tz, the device is powered off.
The time between Tx and Tz ($t_{POFF}$) shall be less than 2s. The relative levels between supply voltages are uncontrolled during this period.

$V_{DD1}$ and $V_{DD2}$ shall decrease with a slope lower than 0.5 V/µS between Tx and Tz.

Uncontrolled power off sequence can be applied only up to 400 times in the life of the device.


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## 7.3 Mode Register Definition

### 7.3.1 Mode Register Assignment and Definition

Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written.

Mode Register Read command shall be used to read a register. Mode Register Write command shall be used to write a register.

#### 7.3.1.1 Mode Register Assignment

| MR# | MA[7:0] | Function | Access | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | $00_H$ | Device Info. | R | (RFU) | | | RZQI | | DNVI | DI | DAI |
| 1 | $01_H$ | Device Feature 1 | W | nWR (for AP) | | | WC | BT | BL | | |
| 2 | $02_H$ | Device Feature 2 | W | (RFU) | | | | | RL & WL | | |
| 3 | $03_H$ | I/O Config-1 | W | (RFU) | | | | | DS | | |
| 4 | $04_H$ | Refresh Rate | R | TUF | (RFU) | | | | Refresh Rate | | |
| 5 | $05_H$ | Basic Config-1 | R | LPDDR2 Manufacturer ID | | | | | | | |
| 6 | $06_H$ | Basic Config-2 | R | Revision ID1 | | | | | | | |
| 7 | $07_H$ | Basic Config-3 | R | Revision ID2 | | | | | | | |
| 8 | $08_H$ | Basic Config-4 | R | I/O width | | Density | | | | Type | |
| 9 | $09_H$ | Test Mode | W | Vendor-Specific Test Mode | | | | | | | |
| 10 | $0A_H$ | I/O Calibration | W | Calibration Code | | | | | | | |
| 11-15 | $0B_H$~$0F_H$ | (reserved) | - | (RFU) | | | | | | | |
| 16 | $10_H$ | PASR_Bank | W | Bank Mask | | | | | | | |
| 17 | $11_H$ | (Reserved) | W | (RFU) | | | | | | | |
| 18-19 | $12_H$~$13_H$ | (Reserved) | - | (RFU) | | | | | | | |
| 20-31 | 14h – 1Fh | Reserved for NVM | | | | | | | | | |
| 32 | 20H | DQ Calibration Pattern A | R | See 7.4.20.2 **“DQ Calibration”** | | | | | | | |
| 33-39 | $21_H$~$27_H$ | (Do Not Use) | - | | | | | | | | |
| 40 | 28H | DQ Calibration Pattern B | R | See 7.4.20.2 **“DQ Calibration”** | | | | | | | |
| 41-47 | $29_H$~$2F_H$ | (Do Not Use) | - | | | | | | | | |
| 48-62 | $30_H$~$3E_H$ | (Reserved) | - | (RFU) | | | | | | | |
| 63 | 3FH | Reset | W | X | | | | | | | |
| 64-126 | $40_H$~$7E_H$ | (Reserved) | - | (RFU) | | | | | | | |
| 127 | 7FH | (Do Not Use) | - | | | | | | | | |
| 128-190 | $80_H$~$BE_H$ | (Reserved for Vendor Use) | - | (RFU) | | | | | | | |
| 191 | BFH | (Do Not Use) | - | | | | | | | | |
| 192-254 | $C0_H$~$FE_H$ | (Reserved for Vendor Use) | - | (RFU) | | | | | | | |
| 255 | FFH | (Do Not Use) | - | | | | | | | | |

**Notes:**

1. RFU bits shall be set to ‘0’ during Mode Register writes.
2. RFU bits shall be read as ‘0’ during Mode Register reads.
3. All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS shall be toggled.
4. All Mode Registers that are specified as RFU shall not be written.
5. Writes to read-only registers shall have no impact on the functionality of the device.


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### 7.3.2 MR0_Device Information (MA[7:0] = 00H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| (RFU) | | | RZQI | | DNVI | DI | DAI |

| | | | |
|---|---|---|---|
| DAI (Device Auto-Initialization Status) | Read-only | OP0 | **$0_b$:** DAI complete<br>**$1_b$:** DAI still in progress |
| DI (Device Information) | Read-only | OP1 | **$0_b$:** S4 SDRAM |
| DNVI (Data Not Valid Information) | Read-only | OP2 | **$0_b$:** LPDDR2 SDRAM will not implement DNV functionality |
| RZQI (Built in Self Test for RZQ Information) | Read-only | OP[4:3] | **00b:** RZQ self test not executed.<br>**01b:** ZQ-pin may connect to VDDCA or float<br>**10b:** ZQ-pin may short to GND<br>**11b:** ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDDCA or float nor short to GND) |

**Notes:**
1. RZQI will be set upon completion of the MRW ZQ Initialization Calibration command.
2. If ZQ is connected to VDDCA to set default calibration by user, OP[4:3] shall be read as 01. If user does not want to connect ZQ pin to VDDCA, but OP[4:3] is read as 01 or 10, it might indicate a ZQ-pin assembly error. It is recommended that the assembly error being corrected first.
3. In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 as defined above), the LPDDR2 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
4. In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e., 240 Ohm ± 1%).

### 7.3.3 MR1_Device Feature 1 (MA[7:0] = 01H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| nWR (for AP) | | | WC | BT | BL | | |

| | | | | |
|---|---|---|---|---|
| BL | Write-only | OP[2:0] | **$010_b$:** BL4 (default)<br>**$011_b$:** BL8<br>**$100_b$:** BL16<br>**All others:** Reserved | |
| BT | Write-only | OP3 | **$0_b$:** Sequential (default)<br>**$1_b$:** Interleaved | |
| WC | Write-only | OP4 | **$0_b$:** Wrap (default)<br>**1 b:** No wrap (allowed for SDRAM BL4 only) | |
| nWR | Write-only | OP[7:5] | **$001_b$:** nWR=3 (default)<br>**$010_b$:** nWR=4<br>**011b:** nWR=5<br>**$100_b$:** nWR=6<br>**$101_b$:** nWR=7<br>**$110_b$:** nWR=8<br>**All others:** Reserved | 1 |

**Note:**
1. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).


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### 7.3.3.1 Burst Sequence by Burst Length (BL), Burst Type (BT), and Warp Control (WC)

| C3 | C2 | C1 | C0 | WC | BT | BL | Burst Cycle Number and Burst Address Sequence | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| X | X | 0b | 0b | wrap | any | 4 | 0 | 1 | 2 | 3 | | | | | | | | | | | | |
| X | X | 1b | 0b | | | | 2 | 3 | 0 | 1 | | | | | | | | | | | | |
| X | X | X | 0b | nw | any | | y | y+1 | y+2 | y+3 | | | | | | | | | | | | |
| X | 0b | 0b | 0b | wrap | seq | 8 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | | | | | | |
| X | 0b | 1b | 0b | | | | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | | | | | | | | |
| X | 1b | 0b | 0b | | | | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | | | | | | | | |
| X | 1b | 1b | 0b | | | | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | | | | | | | | |
| X | 0b | 0b | 0b | | int | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | | | | | | |
| X | 0b | 1b | 0b | | | | 2 | 3 | 0 | 1 | 6 | 7 | 4 | 5 | | | | | | | | |
| X | 1b | 0b | 0b | | | | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | | | | | | | | |
| X | 1b | 1b | 0b | | | | 6 | 7 | 4 | 5 | 2 | 3 | 0 | 1 | | | | | | | | |
| X | X | X | 0b | nw | any | | **illegal (not allowed)** | | | | | | | | | | | | | | | |
| 0b | 0b | 0b | 0b | wrap | seq | 16 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| 0b | 0b | 1b | 0b | | | | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | 0 | 1 |
| 0b | 1b | 0b | 0b | | | | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 |
| 0b | 1b | 1b | 0b | | | | 6 | 7 | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 |
| 1b | 0b | 0b | 0b | | | | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 1b | 0b | 1b | 0b | | | | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 1b | 1b | 0b | 0b | | | | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B |
| 1b | 1b | 1b | 0b | | | | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D |
| X | X | X | 0b | | int | | **illegal (not allowed)** | | | | | | | | | | | | | | | |
| X | X | X | 0b | nw | any | | **illegal (not allowed)** | | | | | | | | | | | | | | | |

**Notes:**

1. C0 input is not present on CA bus. It is implied zero.
2. For BL=4, the burst address represents C[1: 0].
3. For BL=8, the burst address represents C[2:0].
4. For BL=16, the burst address represents C[3:0].
5. For no-wrap (nw), BL4, the burst shall not cross the page boundary and shall not cross sub-page boundary. The variable y may start at any address with C0 equal to 0 and may not start at any address shown in table below.

### 7.3.3.2 Non Wrap Restrictions

| Bus Width | 256Mb |
|---|---|
| Not across full page boundary | |
| x16 | 1FE, 1FF, 000, 001 |
| x32 | FE, FF, 00, 01 |
| Not across sub page boundary | |
| x16 | 0FE, 0FF, 100, 101 |
| x32 | None |

**Note:** Non-wrap BL=4 data-orders shown above are prohibited.

### 7.3.4 MR2_Device Feature 2 (MA[7:0] = 02H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| (RFU) | | | | RL & WL | | | |

| | | | |
|---|---|---|---|
| RL & WL | Write-only | OP[3:0] | **0001b:** RL = 3 / WL = 1 (default)<br>**0010b:** RL = 4 / WL = 2<br>**0011b:** RL = 5 / WL = 2<br>**0100b:** RL = 6 / WL = 3<br>**0101b:** RL = 7 / WL = 4<br>**0110b:** RL = 8 / WL = 4<br>**All others:** Reserved |

### 7.3.5 MR3_I/O Configuration 1 (MA[7:0] = 03H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| (RFU) | | | | DS | | | |

| | | | |
|---|---|---|---|
| DS | Write-only | OP[3:0] | **$0000_b$:** Reserved<br>**$0001_b$:** 34.3-ohm typical<br>**$0010_b$:** 40-ohm typical (default)<br>**$0011_b$:** 48-ohm typical<br>**$0100_b$:** 60-ohm typical<br>**$0101_b$:** Reserved for 68.6-ohm typical<br>**$0110_b$:** 80-ohm typical<br>**$0111_b$:** 120-ohm typical<br>**All others:** Reserved |

### 7.3.6 MR4_Device Temperature (MA[7:0] = 04H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| TUF | (RFU) | | | | SDRAM Refresh Rate | | |

| | | | |
|---|---|---|---|
| SDRAM Refresh Rate | Read-only | OP[2:0] | **$000_b$:** SDRAM Low temperature operating limit exceeded<br>**001b:** 4x tREFI, 4x tREFW<br>**$010_b$:** 2x tREFI, 2x tREFW<br>**$011_b$:** 1x tREFI, 1x tREFW (≤ 85°C)<br>**$100_b$:** Reserved<br>**$101_b$:** 0.25x tREFI, 0.25x tREFW, do not de-rate SDRAM AC timing<br>**$110_b$:** 0.25x tREFI, 0.25x tREFW, de-rate SDRAM AC timing<br>**$111_b$:** SDRAM High temperature operating limit exceeded |
| Temperature Update Flag (TUF) | Read-only | OP7 | **$0_b$:** OP[2:0] value has not changed since last read of MR4.<br>**$1_b$:** OP[2:0] value has changed since last read of MR4. |

**Notes:**

1. A Mode Register Read from MR4 will reset OP7 to '0'.
2. OP7 is reset to '0' at power-up.
3. If OP2 equals '1', the device temperature is greater than 85°C.
4. OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.
5. LPDDR2 might not operate properly when OP[2:0] = 000b or 111b.
6. For specified operating temperature range and maximum operating temperature, refer to **"Operating Temperature Conditions"** table.
7. LPDDR2 devices must be derated by adding 1.875 nS to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating value in **"LPDDR2 AC Timing"** table. Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.
8. The recommended frequency for reading MR4 is provided in **"Temperature Sensor"** section.


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### 7.3.7 MR5_Basic Configuration 1 (MA[7:0] = 05H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| LPDDR2 Manufacturer ID | | | | | | | |

| | | | |
|---|---|---|---|
| LPDDR2 Manufacturer ID | Read-only | OP[7:0] | 0000 1000b: Winbond |

### 7.3.8 MR6_Basic Configuration 2 (MA[7:0] = 06H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| Revision ID1 | | | | | | | |

| | | | |
|---|---|---|---|
| Revision ID1 | Read-only | OP[7:0] | 00000000b: A-version |

**Note:** MR6 is Vendor Specific.

### 7.3.9 MR7_Basic Configuration 3 (MA[7:0] = 07H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| Revision ID2 | | | | | | | |

| | | | |
|---|---|---|---|
| Revision ID2 | Read-only | OP[7:0] | 00000000b: A-version |

**Note:** MR7 is Vendor Specific.

### 7.3.10 MR8_Basic Configuration 4 (MA[7:0] = 08H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| I/O width | | Density | | | | Type | |

| | | | |
|---|---|---|---|
| Type | Read-only | OP[1:0] | **00b:** S4 SDRAM |
| Density | Read-only | OP[5:2] | **0010b:** 256Mb |
| I/O width | Read-only | OP[7:6] | **00b:** x32<br>**01b:** x16 |

### 7.3.11 MR9_Test Mode (MA[7:0] = 09H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| Vendor-specific Test Mode | | | | | | | |


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### 7.3.12 MR10_Calibration (MA[7:0] = 0AH)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| Calibration Code | | | | | | | |

| | | | |
|---|---|---|---|
| Calibration Code | Write-only | OP[7:0] | **0xFF:** Calibration command after initialization<br>**0xAB:** Long calibration<br>**0x56:** Short calibration<br>**0xC3:** ZQ Reset<br>**others:** Reserved |

**Notes:**

1. Host processor shall not write MR10 with "Reserved" values.
2. LPDDR2 devices shall ignore calibration command when a "Reserved" value is written into MR10.
3. See AC timing table for the calibration latency.
4. If ZQ is connected to VSSCA through RZQ, either the ZQ calibration function (see section 7.4.23 **"Mode Register Write ZQ Calibration Command"**) or default calibration (through the ZQreset command) is supported. If ZQ is connected to VDDCA, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.
5. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

### 7.3.13 MR16_PASR_Bank Mask (MA[7:0] = 10H)

| | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|
| S4 SDRAM | Reserved | | | | Bank Mask | | | |

| | | | |
|---|---|---|---|
| Bank [3:0] Mask | Write-only | OP[3:0] | **0b:** self-refresh enable to the bank (=unmasked, default)<br>**1b:** self-refresh blocked (=masked)<br>**OP0:** bank 0<br>**OP1:** bank 1<br>**OP2:** bank 2<br>**OP3:** bank 3 |
| Reserved | Write-only | OP[7:4] | Reserved. Any value written to OP[7:4] are ignored by LPDDR2. |

**Note:** The MR16 is used to control which bank or banks are to be masked or unmasked in self-refresh mode. It has no effect in auto-refresh mode because LPDDR2 256Mb device does not support per-bank refresh in auto-refresh mode.

| OP | Bank Mask | 4-Bank S4 SDRAM |
|---|---|---|
| 0 | XXXXXXX1 | Bank 0 |
| 1 | XXXXXX1X | Bank 1 |
| 2 | XXXXX1XX | Bank 2 |
| 3 | XXXX1XXX | Bank 3 |
| 4 | - | - |
| 5 | - | - |
| 6 | - | - |
| 7 | - | - |


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### 7.3.14 MR32_DQ Calibration Pattern A (MA[7:0] = 20H)

Reads to MR32 return DQ Calibration Pattern "A". See section 7.4.20.2 **"DQ Calibration"**.

### 7.3.15 MR40_DQ Calibration Pattern B (MA[7:0] = 28H)

Reads to MR40 return DQ Calibration Pattern "B". See section 7.4.20.2 **"DQ Calibration"**.

### 7.3.16 MR63_Reset (MA[7:0] = 3FH): MRW only

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

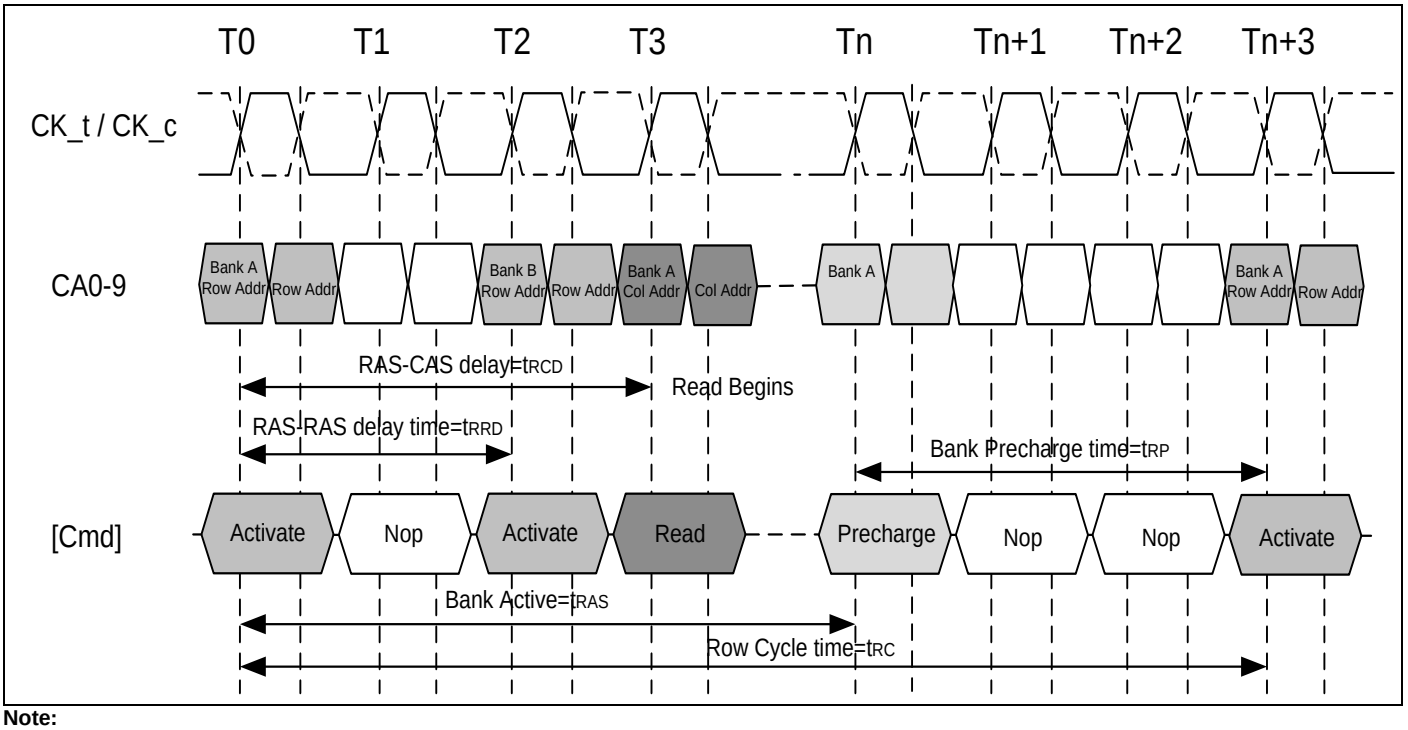
For additional information on MRW RESET see section 7.4.21 **"Mode Register Write Command"**.

## 7.4 Command Definitions and Timing Diagrams

### 7.4.1 Activate Command

The SDRAM Activate command is issued by holding CS_n LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses are used to select the desired bank. The row addresses are used to determine which row to activate in the selected bank. The Activate command must be applied before any Read or Write operation can be executed. The LPDDR2 SDRAM can accept a read or write command at time $t_{RCD}$ after the activate command is sent. Once a bank has been activated it must be precharged before another Activate command can be applied to the same bank. The bank active and precharge times are defined as $t_{RAS}$ and $t_{RP}$, respectively. The minimum time interval between successive Activate commands to the same bank is determined by the RAS cycle time of the device ($t_{RC}$). The minimum time interval between Activate commands to different banks is $t_{RRD}$.

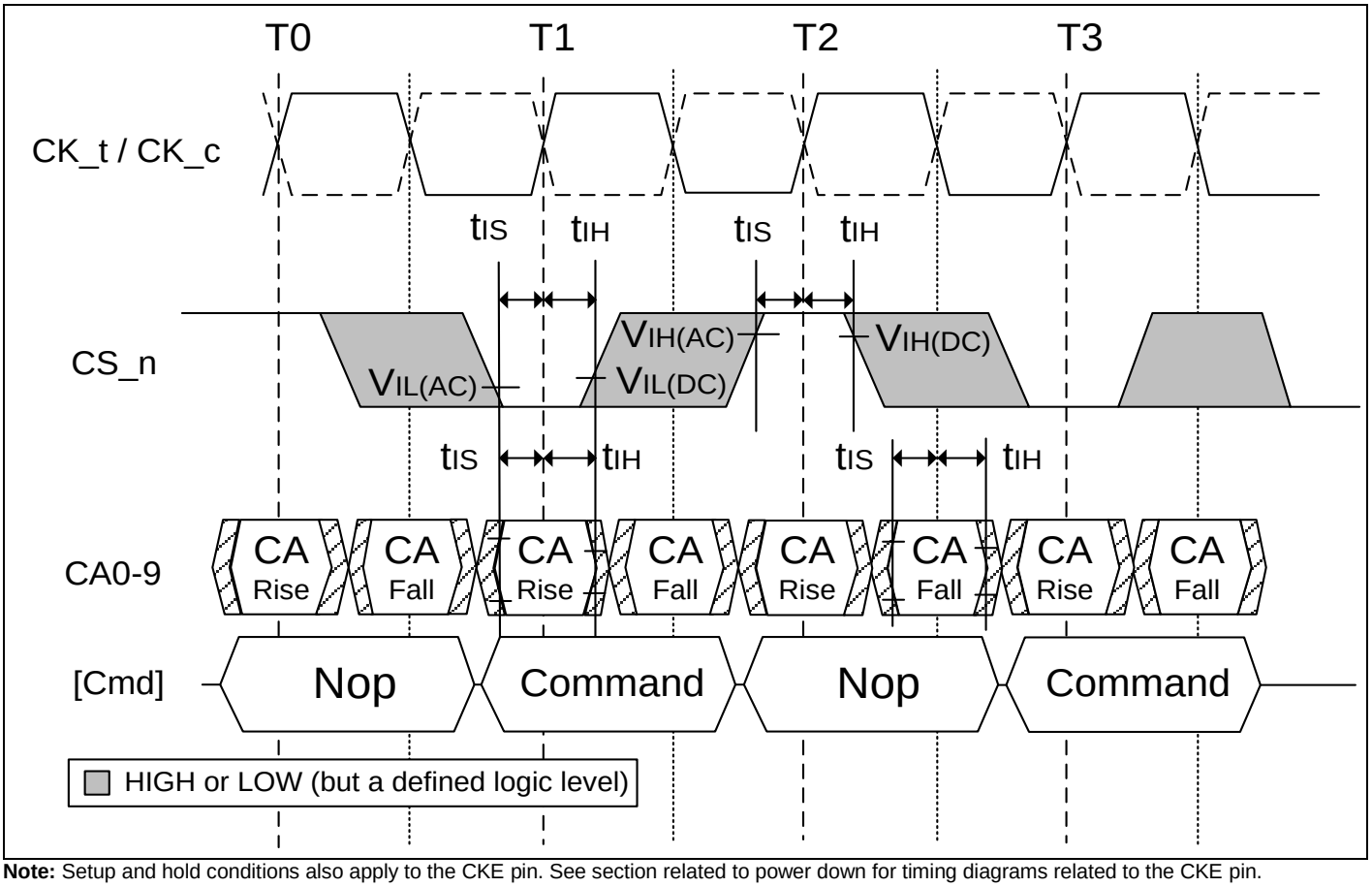
#### 7.4.1.1 Activate Command Cycle: $t_{RCD}$ = 3, $t_{RP}$ = 3, $t_{RRD}$ = 2




**Note:**

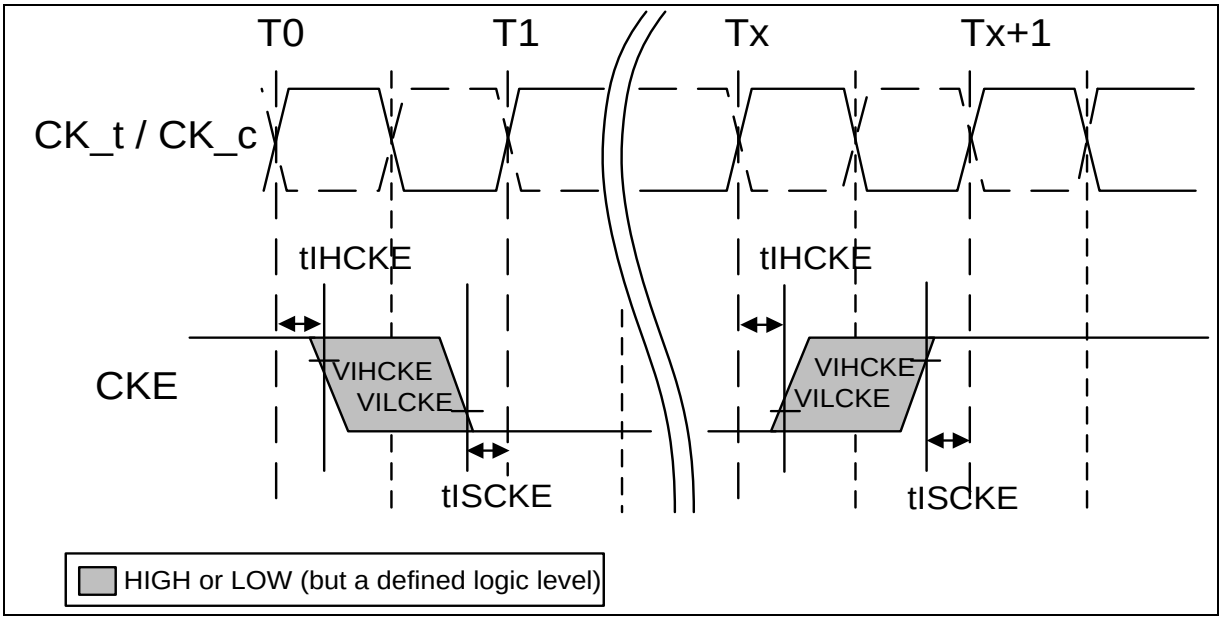
A Precharge-All command uses $t_{RPab}$ timing, while a Single Bank Precharge command uses $t_{RPpb}$ timing. In this figure, $t_{RP}$ is used to denote either an All-bank Precharge or a Single Bank Precharge

#### 7.4.1.2 Command Input Setup and Hold Timing




**Note:** Setup and hold conditions also apply to the CKE pin. See section related to power down for timing diagrams related to the CKE pin.

#### 7.4.1.3 CKE Input Setup and Hold Timing




**Notes:**
1. After CKE is registered LOW, CKE signal level shall be maintained below $V_{ILCKE}$ for $t_{CKE}$ specification (LOW pulse width).
2. After CKE is registered HIGH, CKE signal level shall be maintained above $V_{IHCKE}$ for $t_{CKE}$ specification (HIGH pulse width).


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### 7.4.2 Read and Write Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting CS_n LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a READ operation (CA2 HIGH) or a WRITE operation (CA2 LOW).

The LPDDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles.

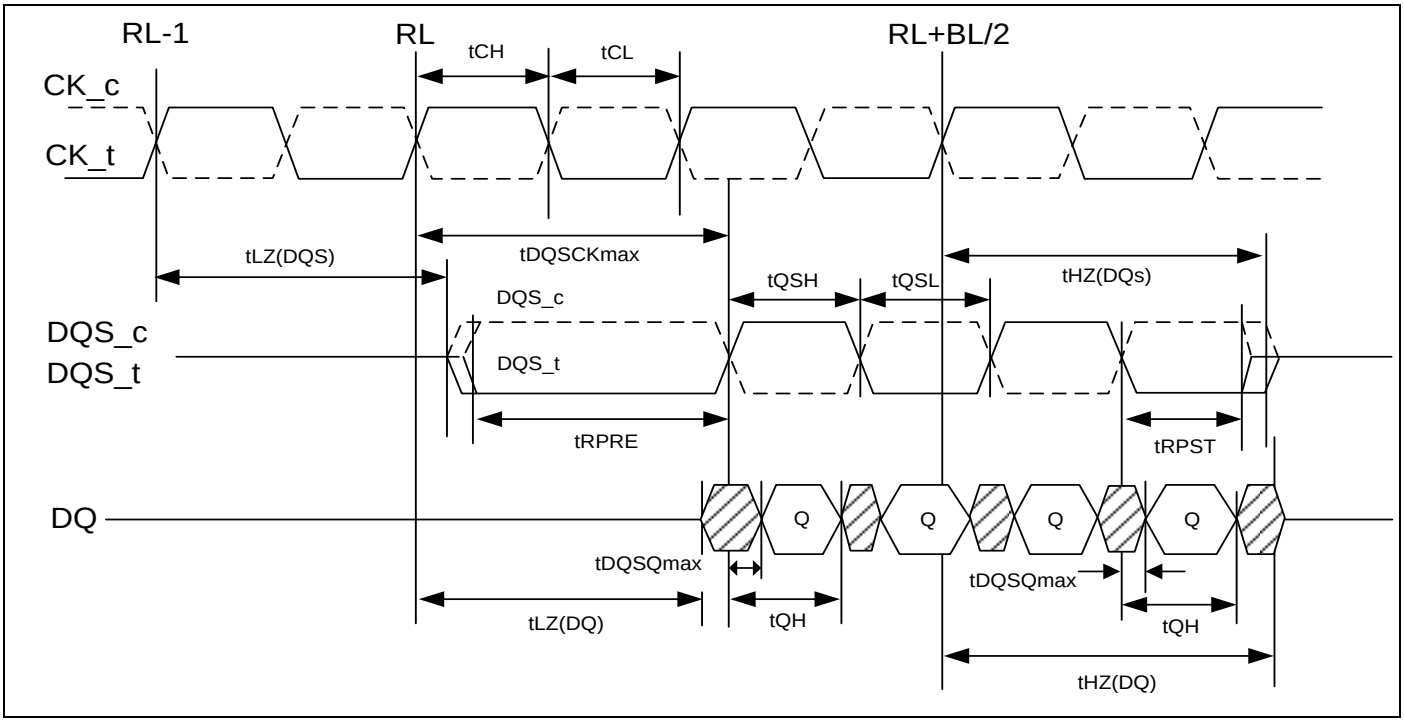
A new burst access must not interrupt the previous 4-bit burst operation in case of BL = 4 setting. In case of BL = 8 and BL = 16 settings, Reads may be interrupted by Reads and Writes may be interrupted by Writes provided that this occurs on even clock cycles after the Read or Write command and $t_{CCD}$ is met.

### 7.4.3 Burst Read Command

The Burst Read command is initiated by having CS_n LOW, CA0 HIGH, CA1 LOW and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Read Latency (RL) is defined from the rising edge of the clock on which the Read Command is issued to the rising edge of the clock from which the $t_{DQSCK}$ delay is measured. The first valid datum is available RL * $t_{CK}$ + $t_{DQSCK}$ + $t_{DQSQ}$ after the rising edge of the clock where the Read Command is issued. The data strobe output is driven LOW $t_{RPRE}$ before the first rising valid strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin edge aligned with the data strobe. The RL is programmed in the mode registers.

Timings for the data strobe are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

#### 7.4.3.1 Data Output (Read) Timing ($t_{DQSCKmax}$)

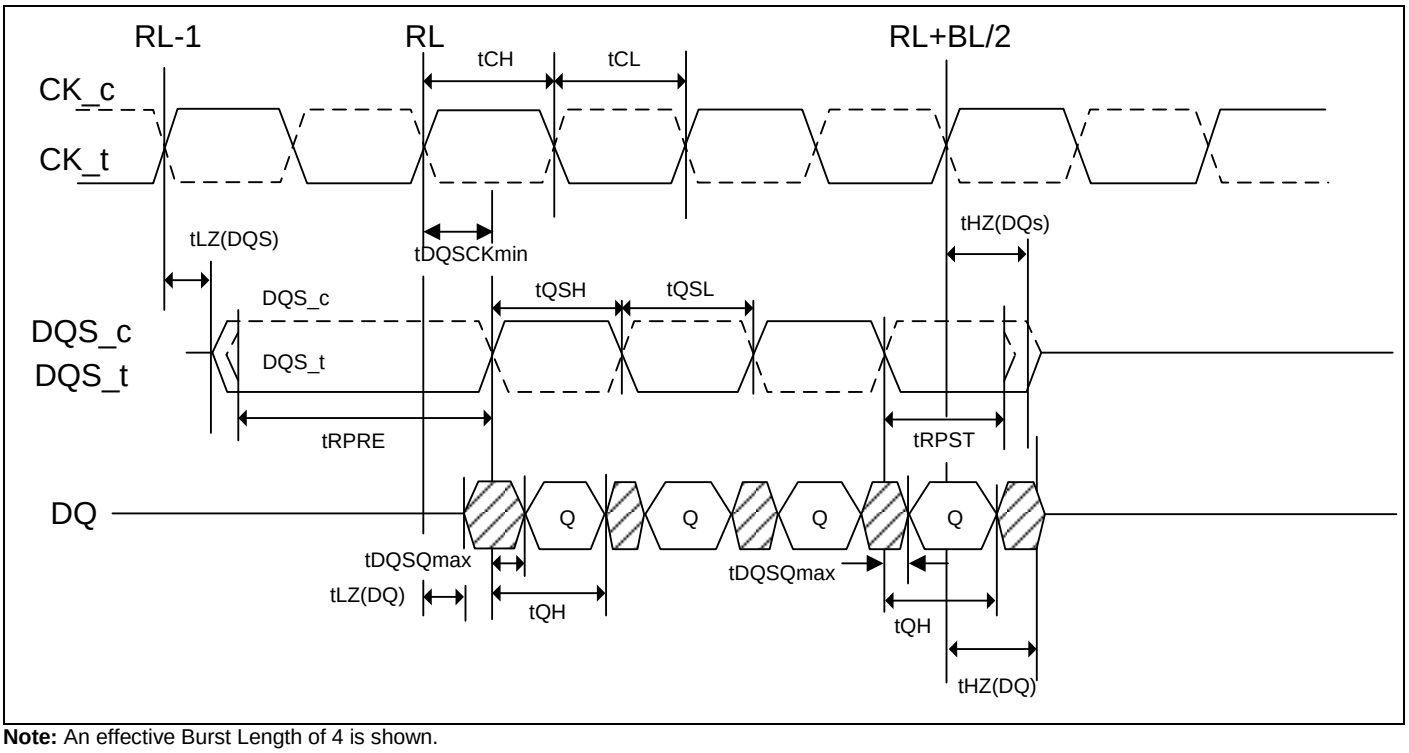



**Notes:**

1. $t_{DQSCK}$ may span multiple clock periods.
2. An effective Burst Length of 4 is shown.

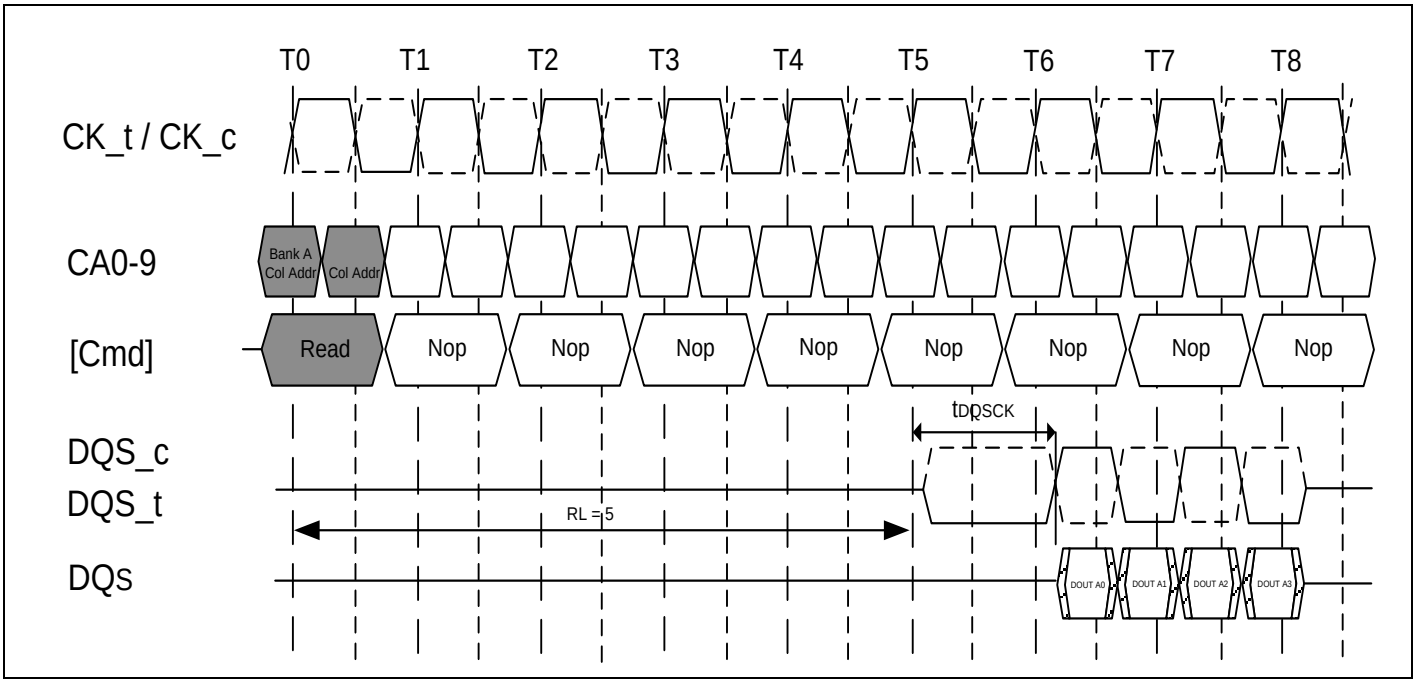

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### 7.4.3.2 Data Output (Read) Timing ($t_{DQSCKmin}$)

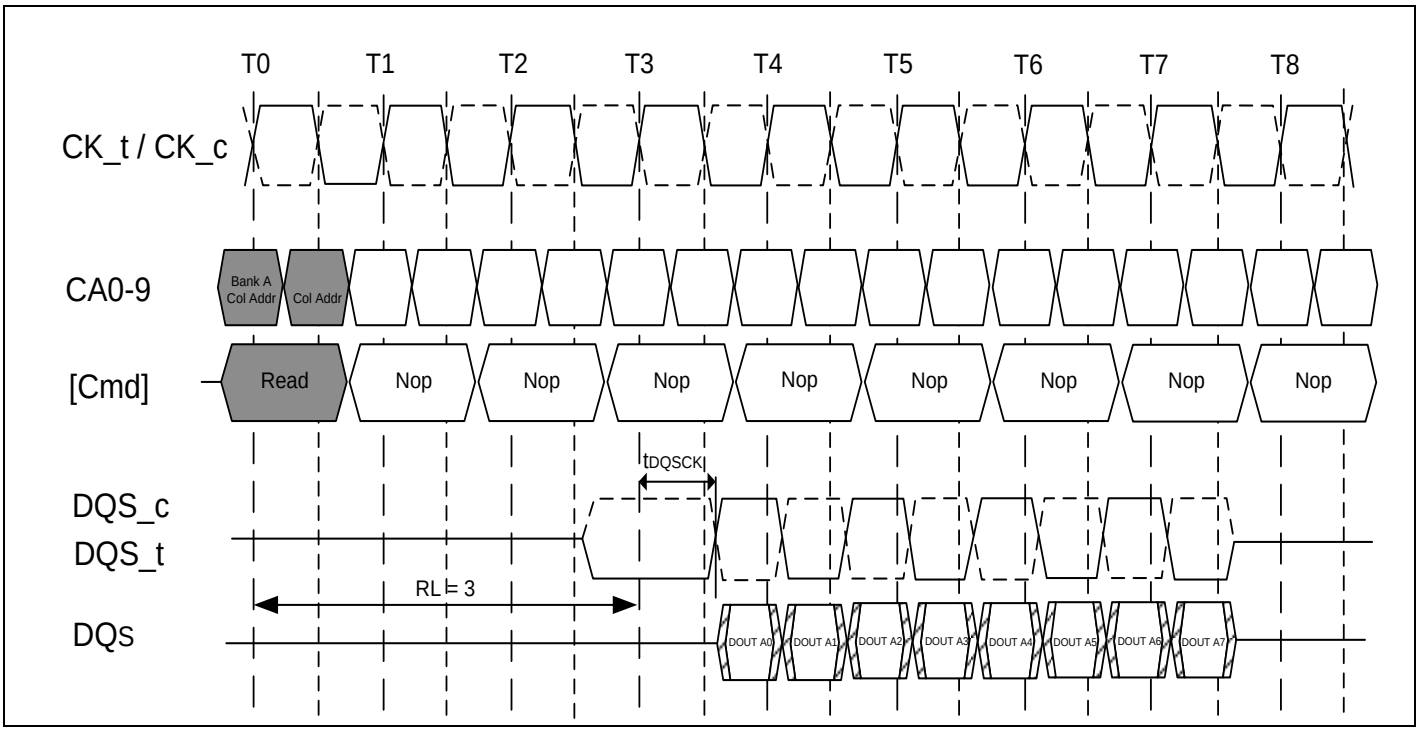



**Note:** An effective Burst Length of 4 is shown.

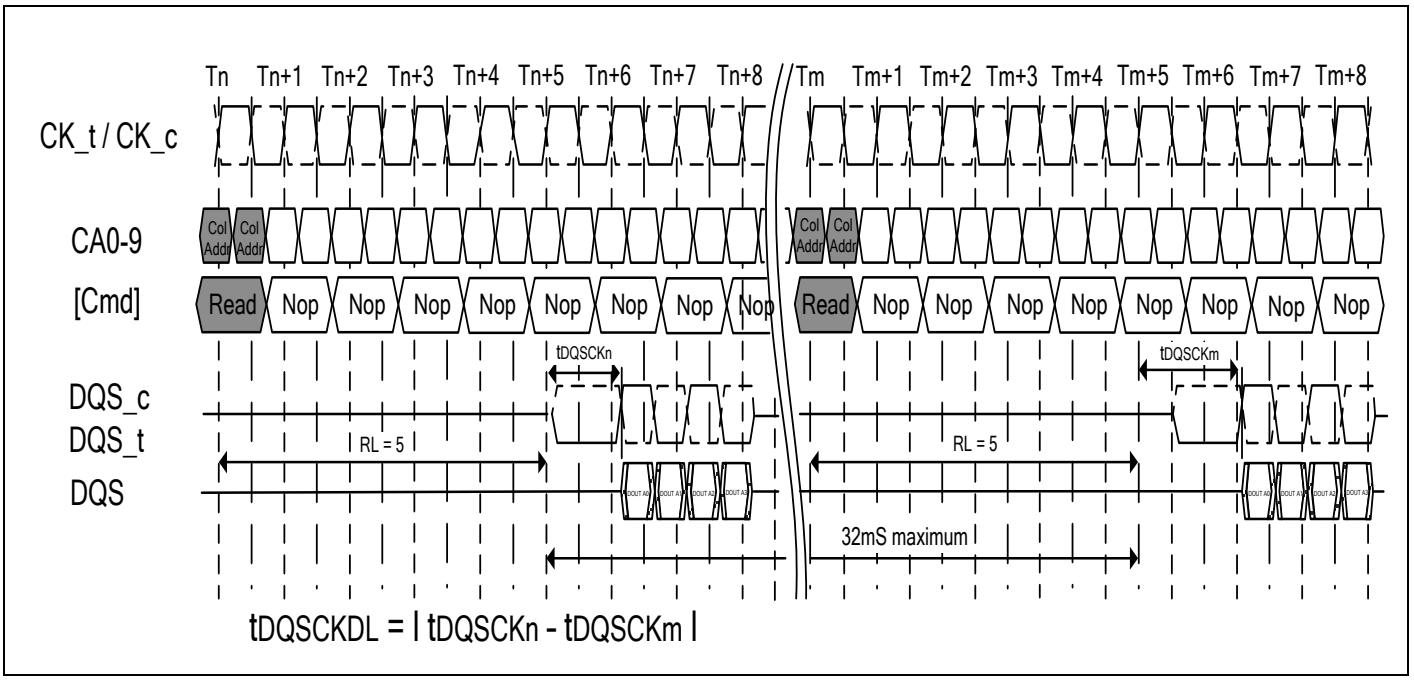
### 7.4.3.3 Burst Read: RL = 5, BL = 4, $t_{DQSCK} > t_{CK}$



#### 7.4.3.4 Burst Read: RL = 3, BL = 8, $t_{DQSCK} < t_{CK}$



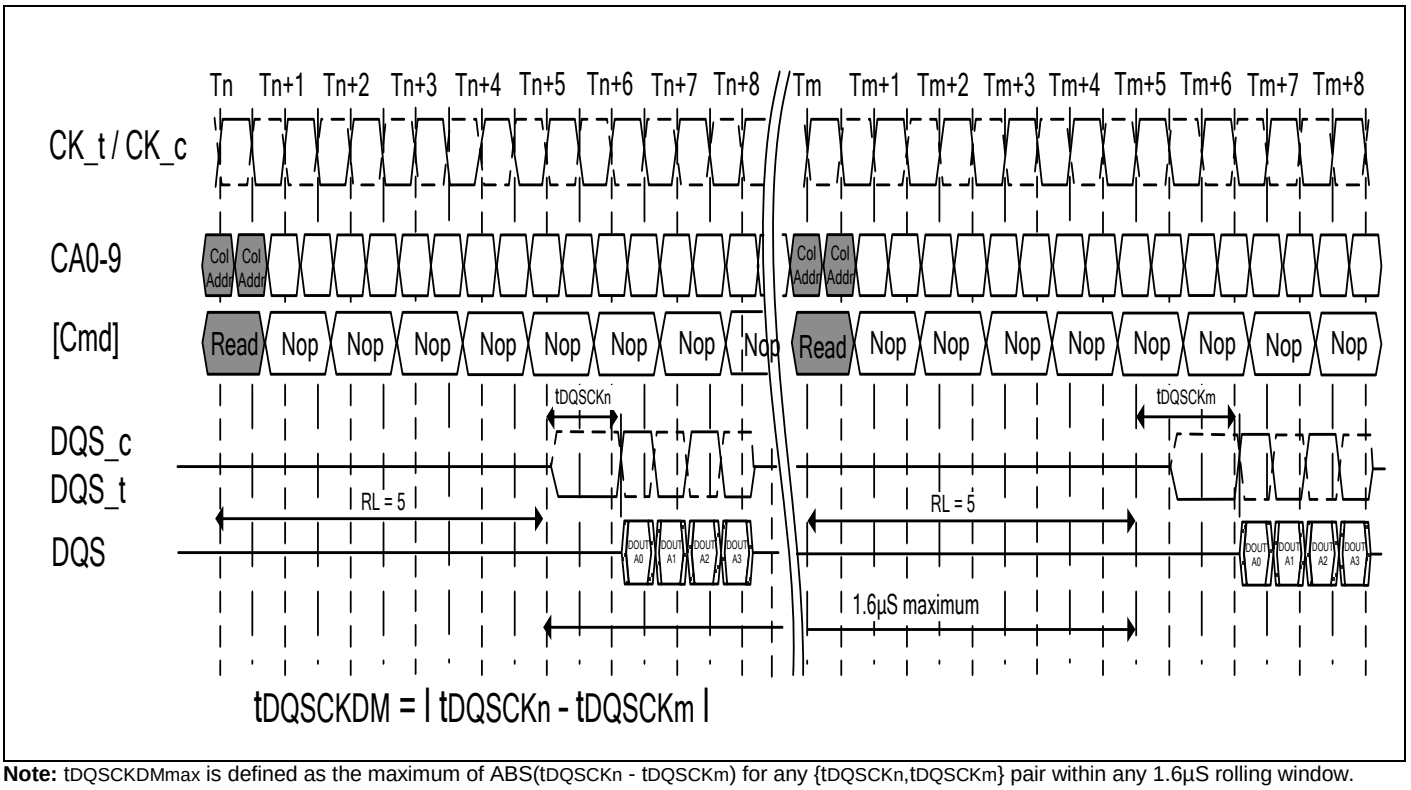

#### 7.4.3.5 LPDDR2: $t_{DQSCKDL}$ Timing




**Note:** $t_{DQSCKDLmax}$ is defined as the maximum of ABS($t_{DQSCKn}$ - $t_{DQSCKm}$) for any {$t_{DQSCKn}$ ,$t_{DQSCKm}$} pair within any 32mS rolling window.

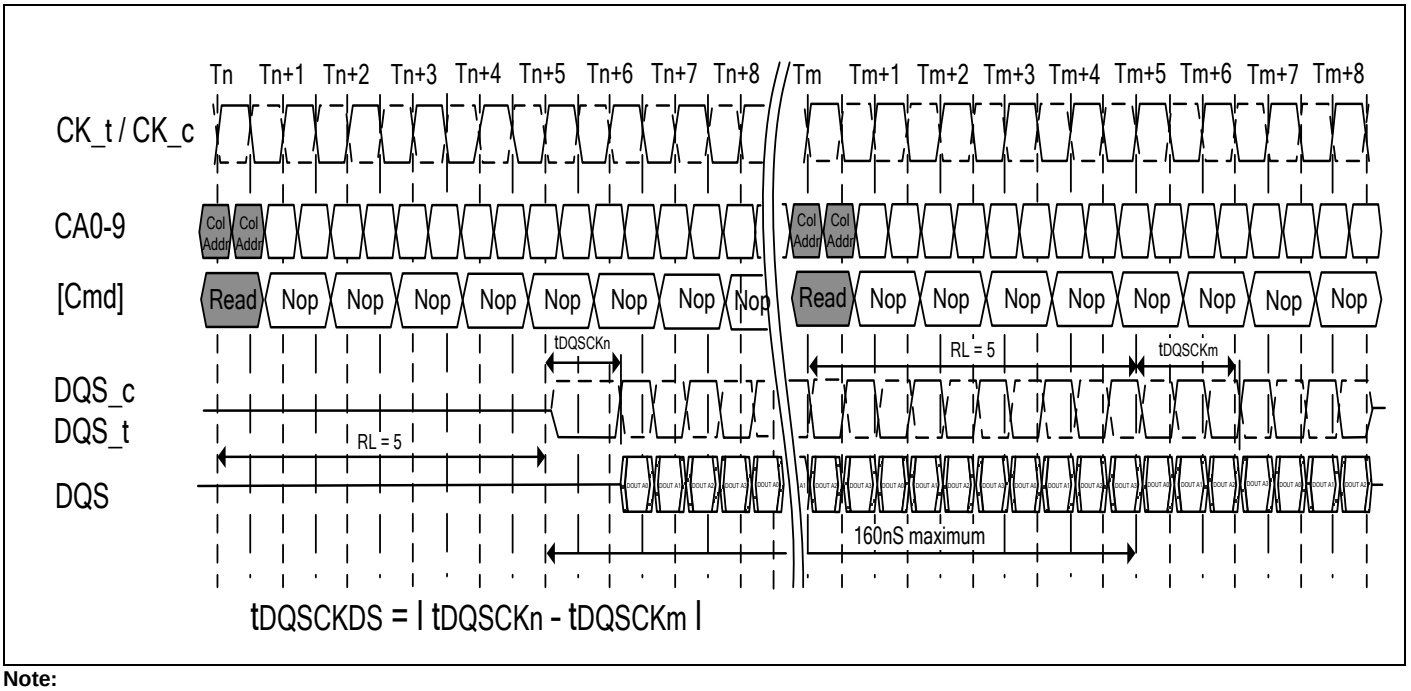

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### 7.4.3.6 LPDDR2: tDQSCKDM Timing




**Note:** tDQSCKDMmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn,tDQSCKm} pair within any 1.6µS rolling window.

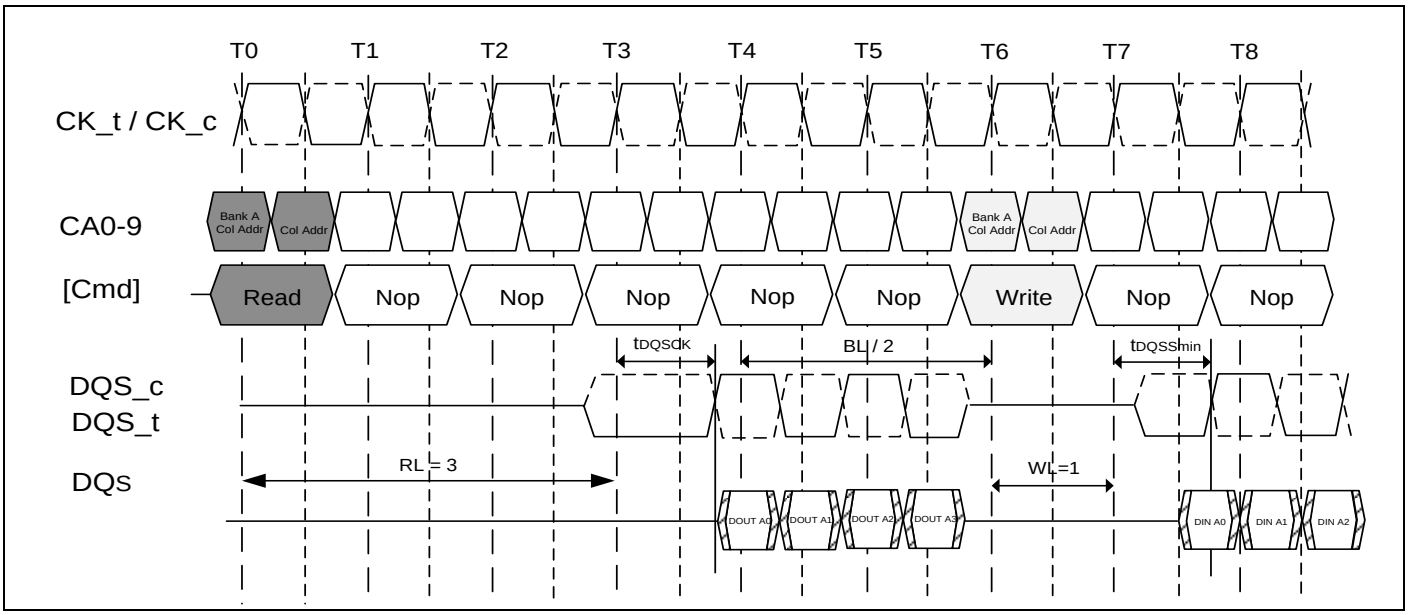
### 7.4.3.7 LPDDR2: tDQSCKDS Timing




**Note:**
tDQSCKDSmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn ,tDQSCKm} pair for reads within a consecutive burst within any 160nS rolling window

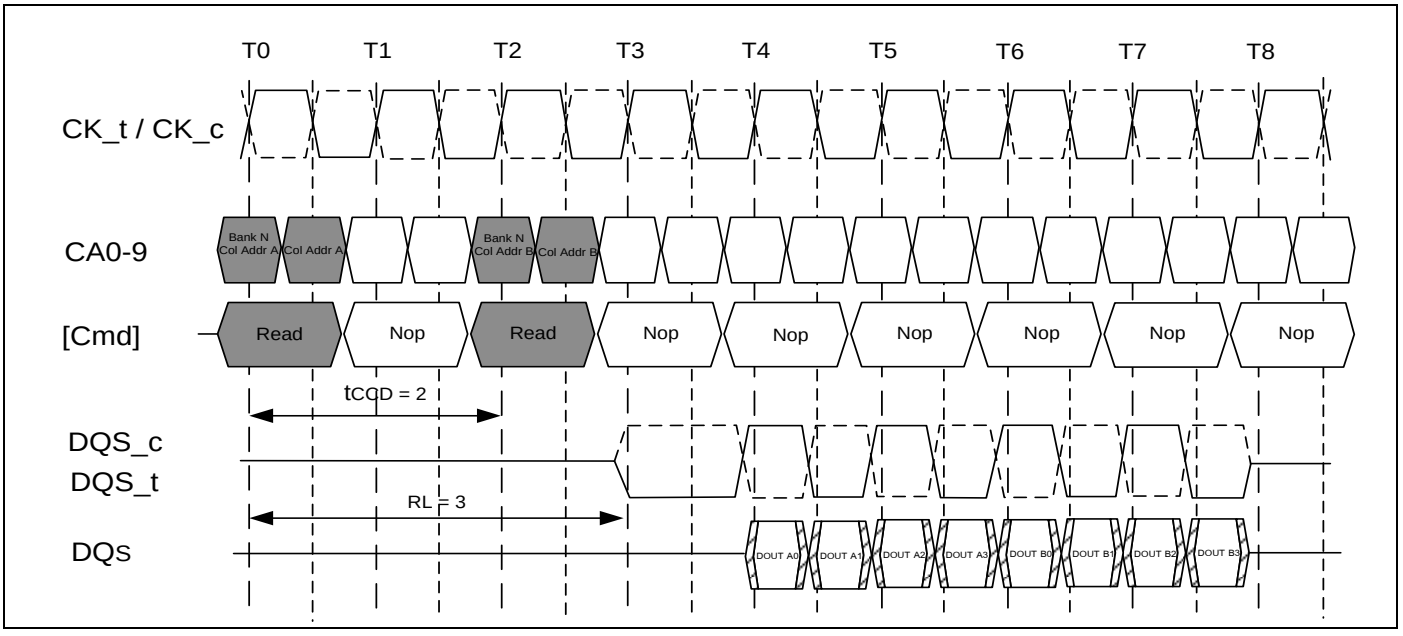

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#### 7.4.3.8 Burst Read Followed by Burst Write: RL = 3, WL = 1, BL = 4




The minimum time from the burst read command to the burst write command is defined by the Read Latency (RL) and the Burst Length (BL). Minimum read to write latency is RL + RU($t_{DQSCKmax}/t_{CK}$) + BL/2 + 1 - WL clock cycles. Note that if a read burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated read burst should be used as "BL" to calculate the minimum read to write delay.

#### 7.4.3.9 Seamless Burst Read: RL = 3, BL= 4, $t_{CCD}$ = 2



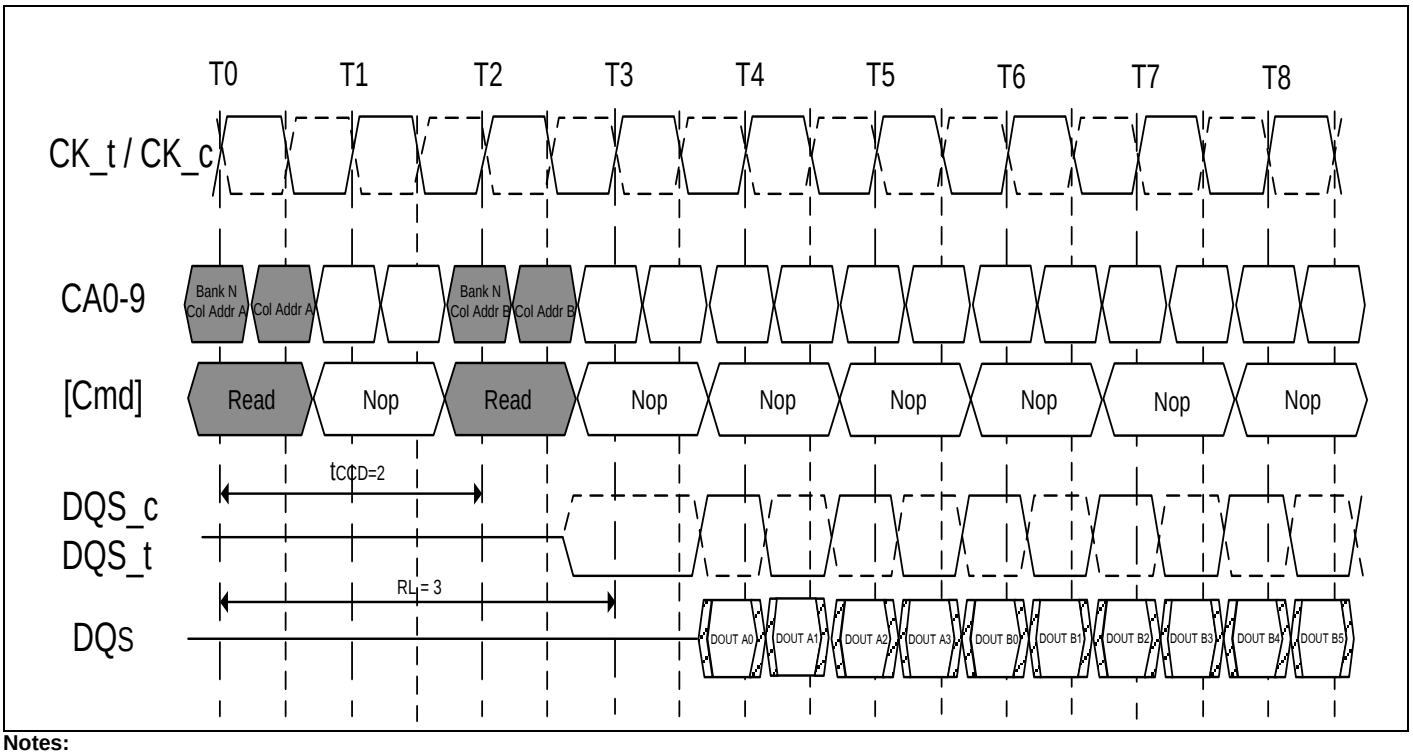

The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, every 4 clocks for BL = 8 operation, and every 8 clocks for BL=16 operation.

For LPDDR2-SDRAM, this operation is allowed regardless of whether the accesses read the same or different banks as long as the banks are activated.

### 7.4.4 Reads Interrupted by a Read

For LPDDR2-S4 device, burst read can be interrupted by another read on even clock cycles after the Read command, provided that $t_{CCD}$ is met.

#### 7.4.4.1 Read Burst Interrupt Example: RL = 3, BL= 8, $t_{CCD}$ = 2




**Notes:**

1. For LPDDR2-S4 devices, read burst interrupt function is only allowed on burst of 8 and burst of 16.
2. For LPDDR2-S4 devices, read burst interrupt may occur on any clock cycle after the initial read command, provided that $t_{CCD}$ is met.
3. Reads can only be interrupted by other reads or the BST command.
4. Read burst interruption is allowed to any bank inside DRAM.
5. Read burst with Auto-Precharge is not allowed to be interrupted.
6. The effective burst length of the first read equals two times the number of clock cycles between the first read and the interrupting read.

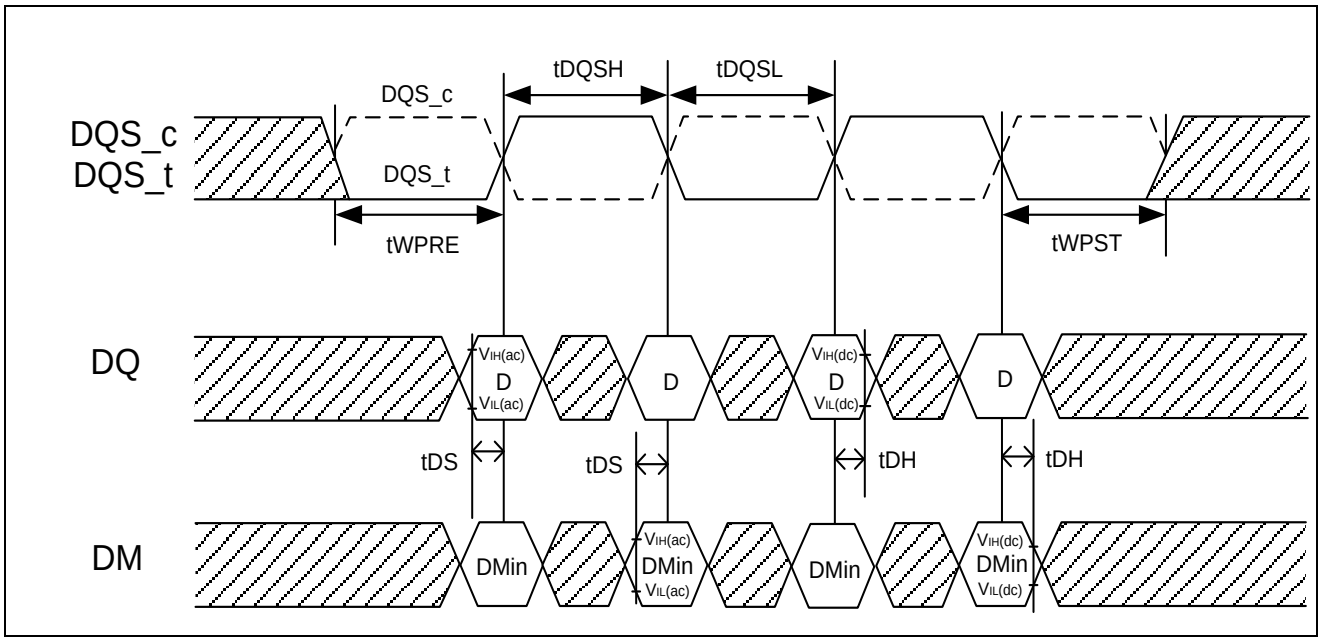
### 7.4.5 Burst Write Operation

The Burst Write command is initiated by having CS_n LOW, CA0 HIGH, CA1 LOW and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Write Latency (WL) is defined from the rising edge of the clock on which the Write Command is issued to the rising edge of the clock from which the $t_{DQSS}$ delay is measured. The first valid data must be driven WL * $t_{CK}$ + $t_{DQSS}$ from the rising edge of the clock from which the Write command is issued. The data strobe signal (DQS) should be driven LOW $t_{WPRE}$ prior to the data input. The data bits of the burst cycle must be applied to the DQ pins $t_{DS}$ prior to the respective edge of the DQS_t, DQS_c and held valid until $t_{DH}$ after that edge. The burst data are sampled on successive edges of the DQS_t, DQS_c until the burst length is completed, which is 4, 8, or 16 bit burst.

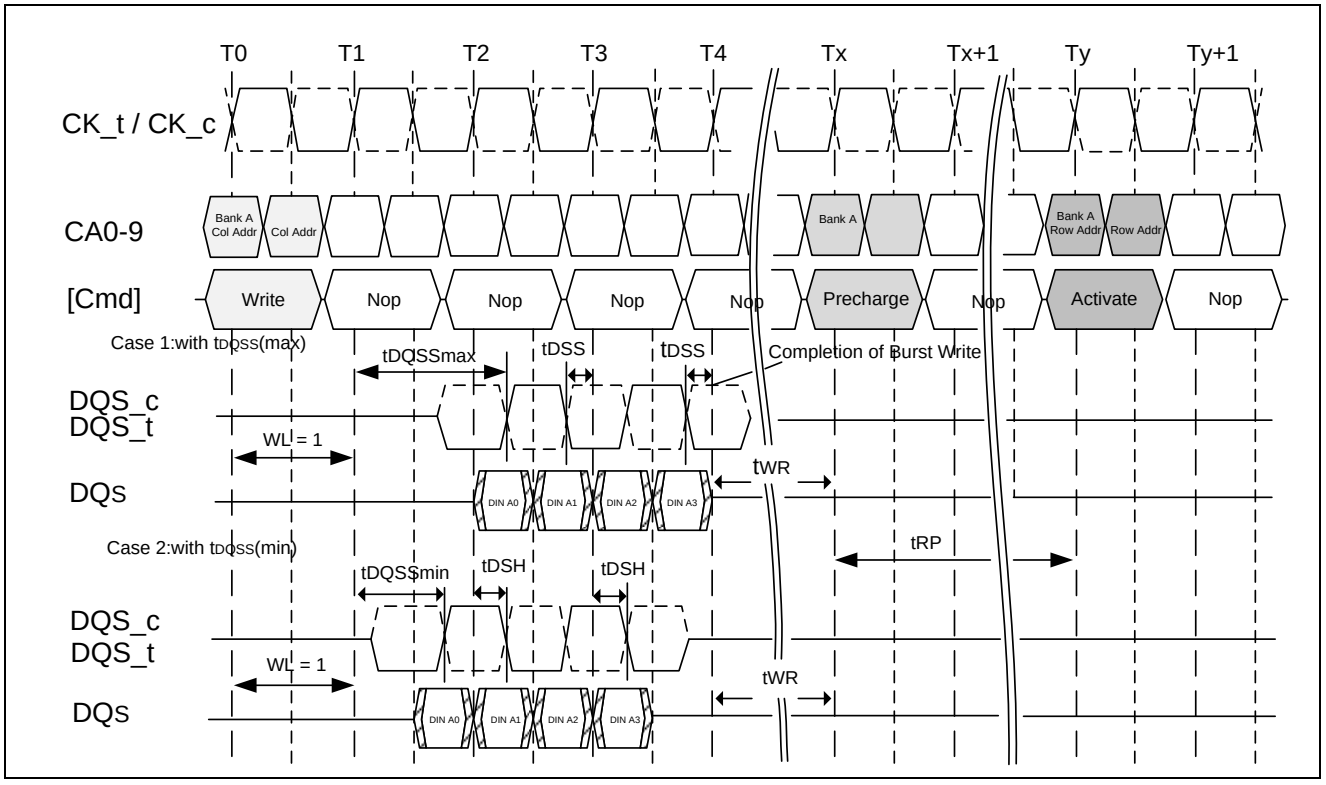
For LPDDR2-SDRAM devices, $t_{WR}$ must be satisfied before a precharge command to the same bank may be issued after a burst write operation.

Input timings are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

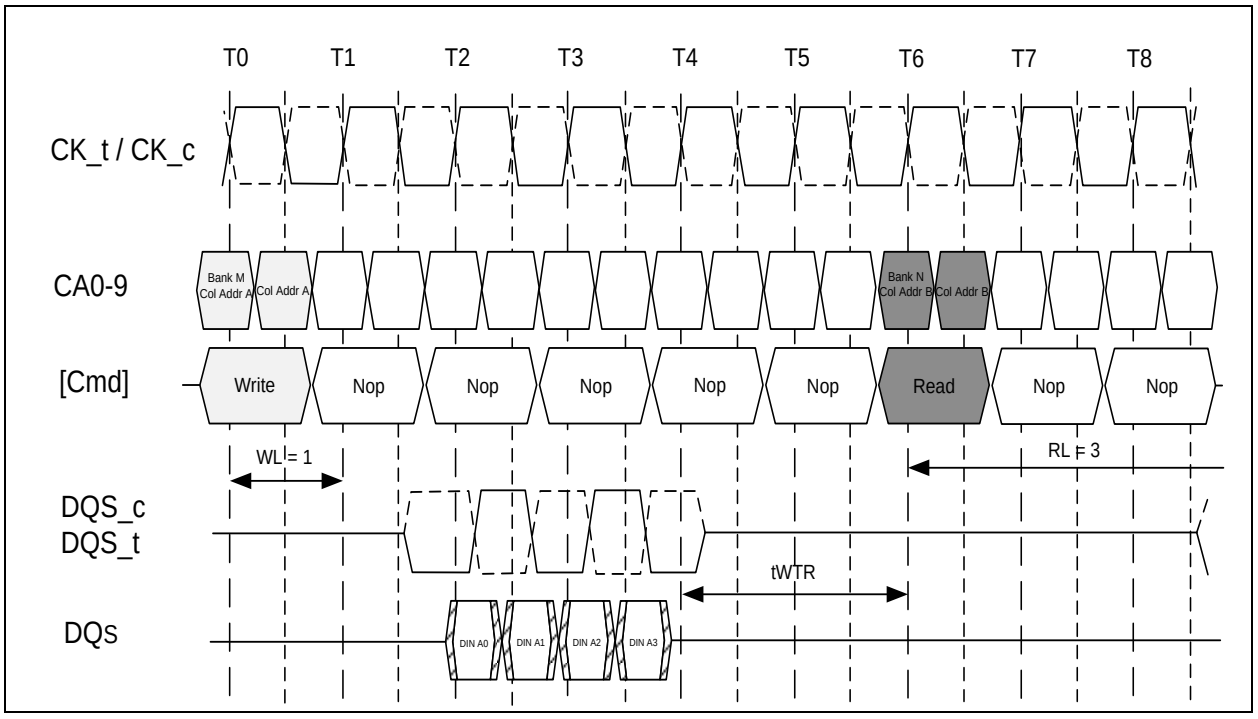
#### 7.4.5.1 Data Input (Write) Timing




#### 7.4.5.2 Burst Write: WL = 1, BL= 4



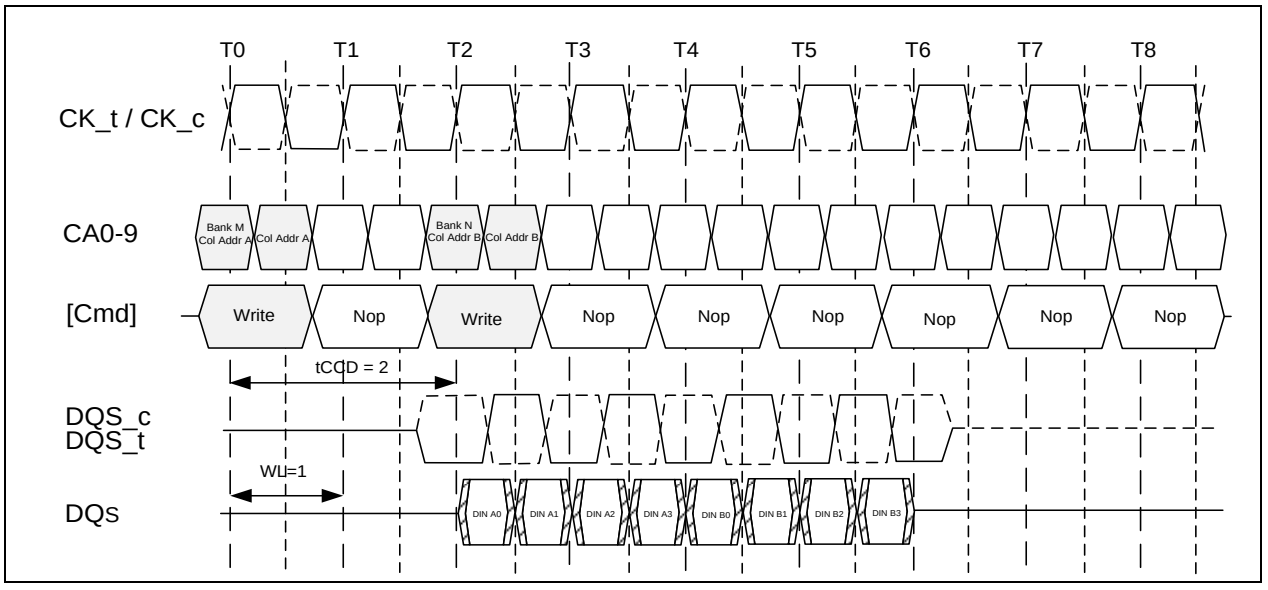
### 7.4.5.3 Burst Write Followed by Burst Read: RL = 3, WL= 1, BL= 4




**Notes:**

1. The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU( tWTR/tCK)].
2. tWTR starts at the rising edge of the clock after the last valid input datum.
3. If a write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated write burst should be used as "BL" to calculate the minimum write to read delay.

### 7.4.5.4 Seamless Burst Write: WL= 1, BL = 4, tCCD = 2



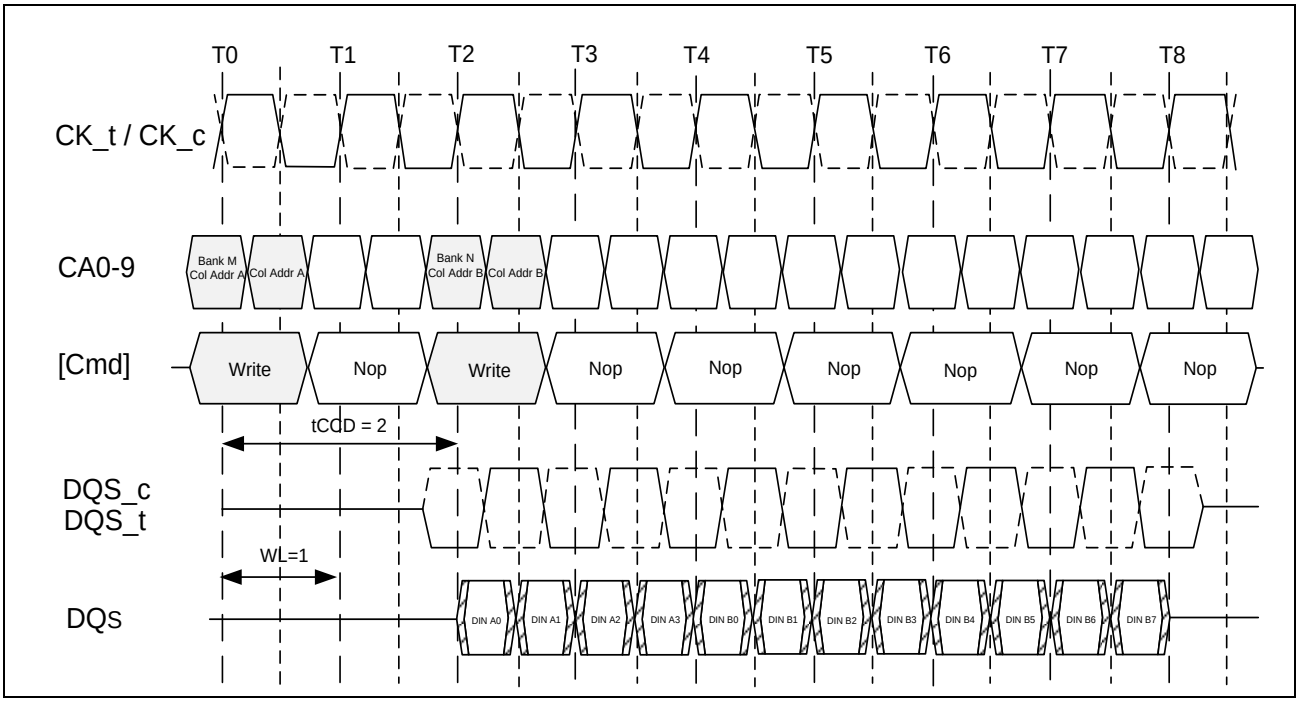

**Note:**

The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL = 16 operation. This operation is allowed regardless of same or different banks as long as the banks are activated

### 7.4.6 Writes Interrupted by a Write

For LPDDR2-S4 devices, burst writes can only be interrupted by another write on even clock cycles after the write command, provided that $t_{CCD(min)}$ is met.

#### 7.4.6.1 Write Burst Interrupt Timing: WL = 1, BL = 8, $t_{CCD}$ = 2




**Notes:**

1. For LPDDR2-S4 devices, write burst interrupt function is only allowed on burst of 8 and burst of 16.
2. For LPDDR2-S4 devices, write burst interrupt may only occur on even clock cycles after the previous write commands, provided that $t_{CCD(min)}$ is met.
3. Writes can only be interrupted by other writes or the BST command.
4. Write burst interruption is allowed to any bank inside DRAM.
5. Write burst with Auto-Precharge is not allowed to be interrupted.
6. The effective burst length of the first write equals two times the number of clock cycles between the first write and the interrupting write.

### 7.4.7 Burst Terminate

The Burst Terminate (BST) command is initiated by having CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of clock. A Burst Teminate command may only be issued to terminate an active Read or Write burst. Therefore, a Burst Terminate command may only be issued up to and including BL/2 - 1 clock cycles after a Read or Write command. The effective burst length of a Read or Write command truncated by a BST command is as follows:

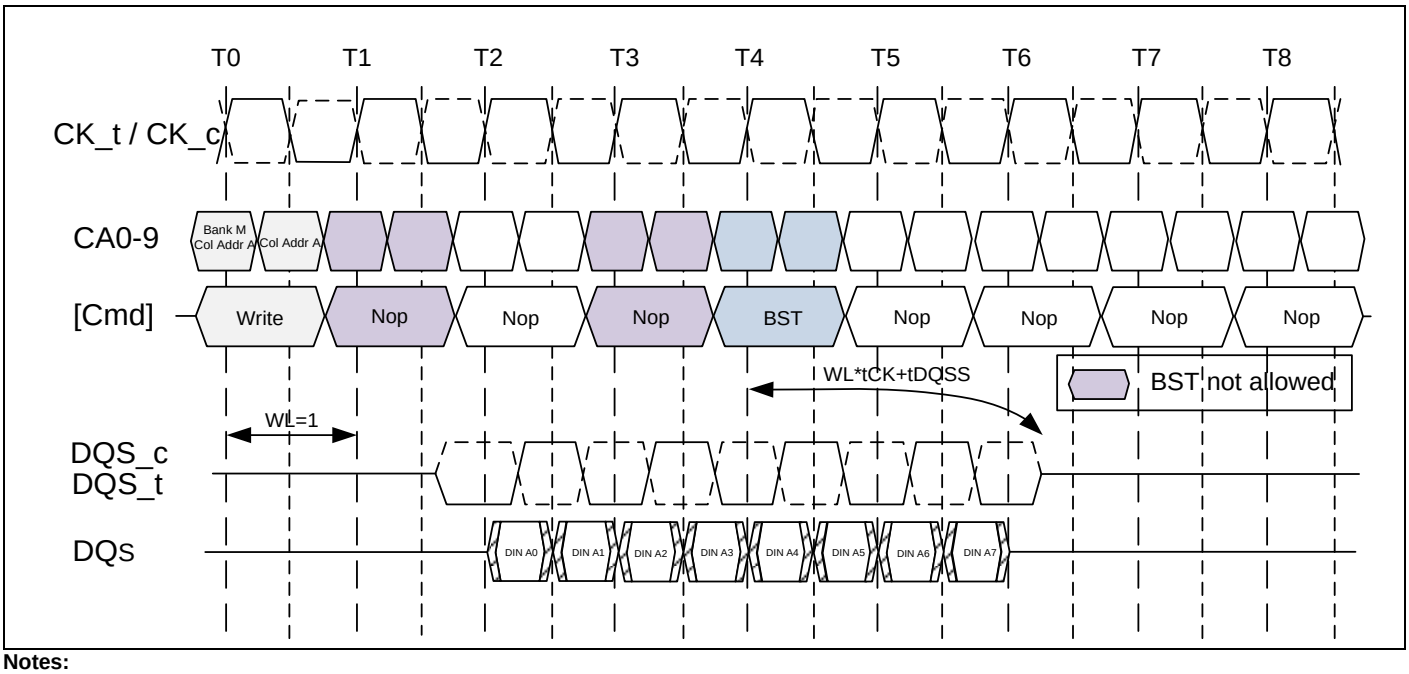
Effective burst length = 2 x {Number of clock cycles from the Read or Write Command to the BST command}

Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as “BL” to calculate the minimum read to write or write to read delay.

The BST command only affects the most recent read or writes command. The BST command truncates an ongoing read burst RL * $t_{CK}$ + $t_{DQSCK}$ + $t_{DQSQ}$ after the rising edge of the clock where the Burst Terminate command is issued. The BST command truncates an on going write burst WL * $t_{CK}$ + $t_{DQSS}$ after the rising edge of the clock where the Burst Terminate command is issued.

For LPDDR2-S4 devices, the 4-bit prefetch architecture allows the BST command to be issued on an even number of clock cycles after a Write or Read command. Therefore, the effective burst length of a Read or Write command truncated by a BST command is an integer multiple of 4.

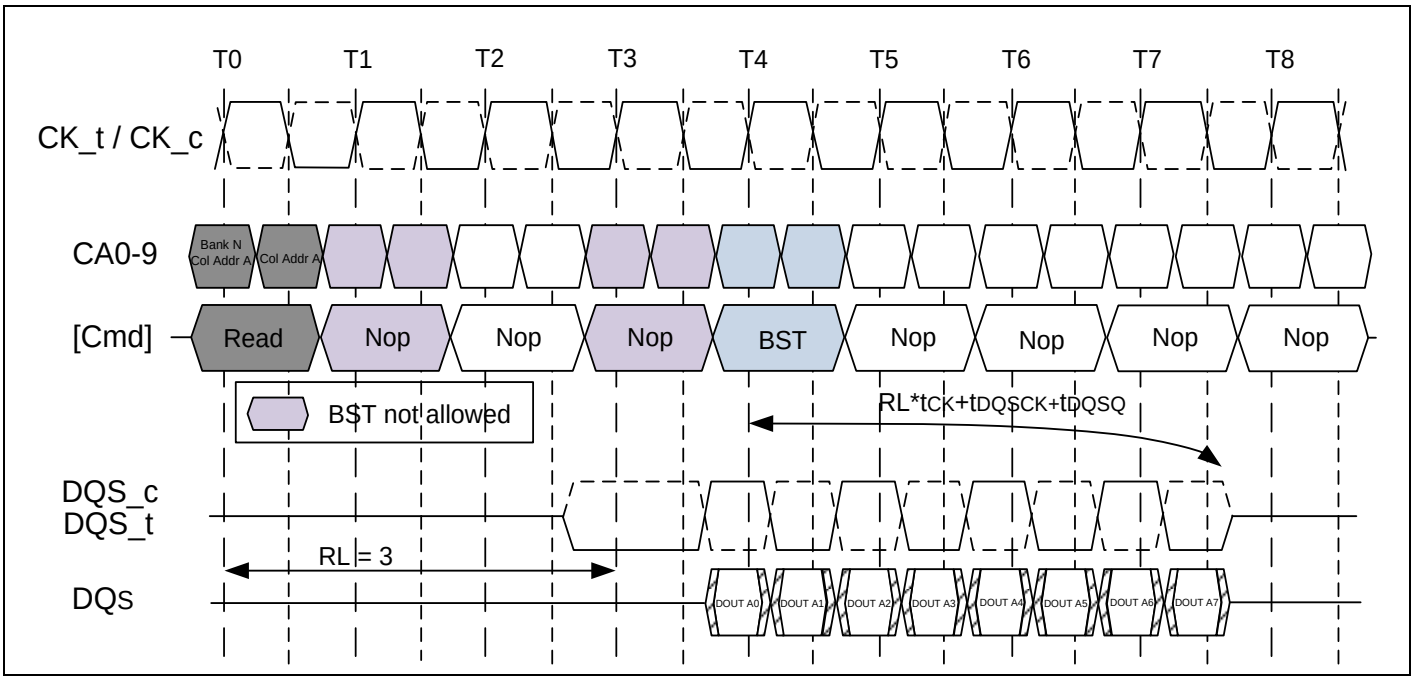
### 7.4.7.1 Burst Write Truncated by BST: WL = 1, BL = 16




**Notes:**

1. The BST command truncates an ongoing write burst WL * tCK + tDQSS after the rising edge of the clock where the Burst Terminate command is issued.
2. For LPDDR2-S4 devices, BST can only be issued at even number of clock cycles after the Write command.
3. Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

### 7.4.7.2 Burst Read Truncated by BST: RL = 3, BL = 16




**Notes:**

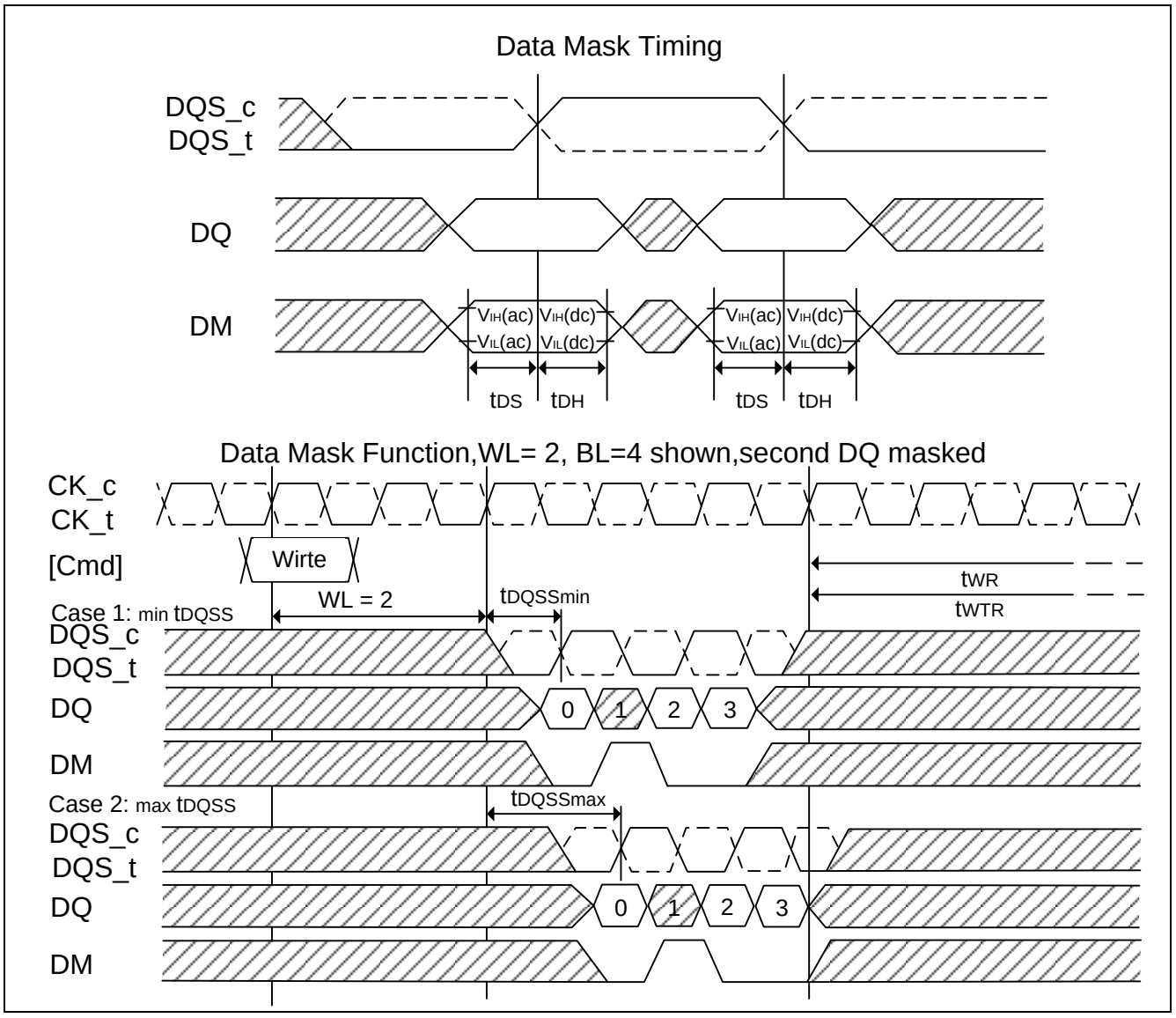
1. The BST command truncates an ongoing read burst RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Burst Terminate command is issued.
2. For LPDDR2-S4 devices, BST can only be issued at even number of clock cycles after the Read command.
3. Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

### 7.4.8 Write Data Mask

One write data mask (DM) pin for each data byte (DQ) will be supported on LPDDR2 devices, consistent with the implementation on LPDDR SDRAMs. Each data mask (DM) may mask its respective data byte (DQ) for any given cycle of the burst. Data mask has identical timings on write operations as the data bits, though used as input only, is internally loaded identically to data bits to insure matched system timing.

See 7.4.14.2 **"Precharge & Auto Precharge Clarification"** table for Write to Precharge timings.

#### 7.4.8.1 Write Data Mask Timing



### 7.4.9 Precharge Operation

The Precharge command is used to precharge or close a bank that has been activated. The Precharge command is initiated by having CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. For 4-bank devices, the AB flag, and the bank address bits, BA0 and BA1 are used to determine which bank(s) to precharge. The bank(s) will be available for a subsequent row access $t_{RPab}$ after an All-Bank Precharge command is issued and $t_{RPpb}$ after a Single-Bank Precharge command is issued.

For 4-bank devices, the Row Precharge time ($t_{RP}$) for an All-Bank Precharge ($t_{RPab}$) is equal to the Row Precharge time for a Single-Bank Precharge ($t_{RPpb}$).

#### 7.4.9.1 Bank Selection for Precharge by Address Bits

| AB (CA4r) | BA1 (CA8r) | BA0 (CA7r) | Precharged Bank(s) 4-bank device |
|---|---|---|---|
| 0 | 0 | 0 | Bank 0 only |
| 0 | 0 | 1 | Bank 1 only |
| 0 | 1 | 0 | Bank 2 only |
| 0 | 1 | 1 | Bank 3 only |
| 1 | DON'T CARE | DON'T CARE | All Banks |

### 7.4.10 Burst Read Operation Followed by Precharge

For the earliest possible precharge, the precharge command may be issued BL/2 clock cycles after a Read command. For an untruncated burst, BL is the value from the Mode Register. For a truncated burst, BL is the effective burst length. A new bank active (command) may be issued to the same bank after the Row Precharge time ($t_{RP}$). A precharge command cannot be issued until after $t_{RAS}$ is satisfied.

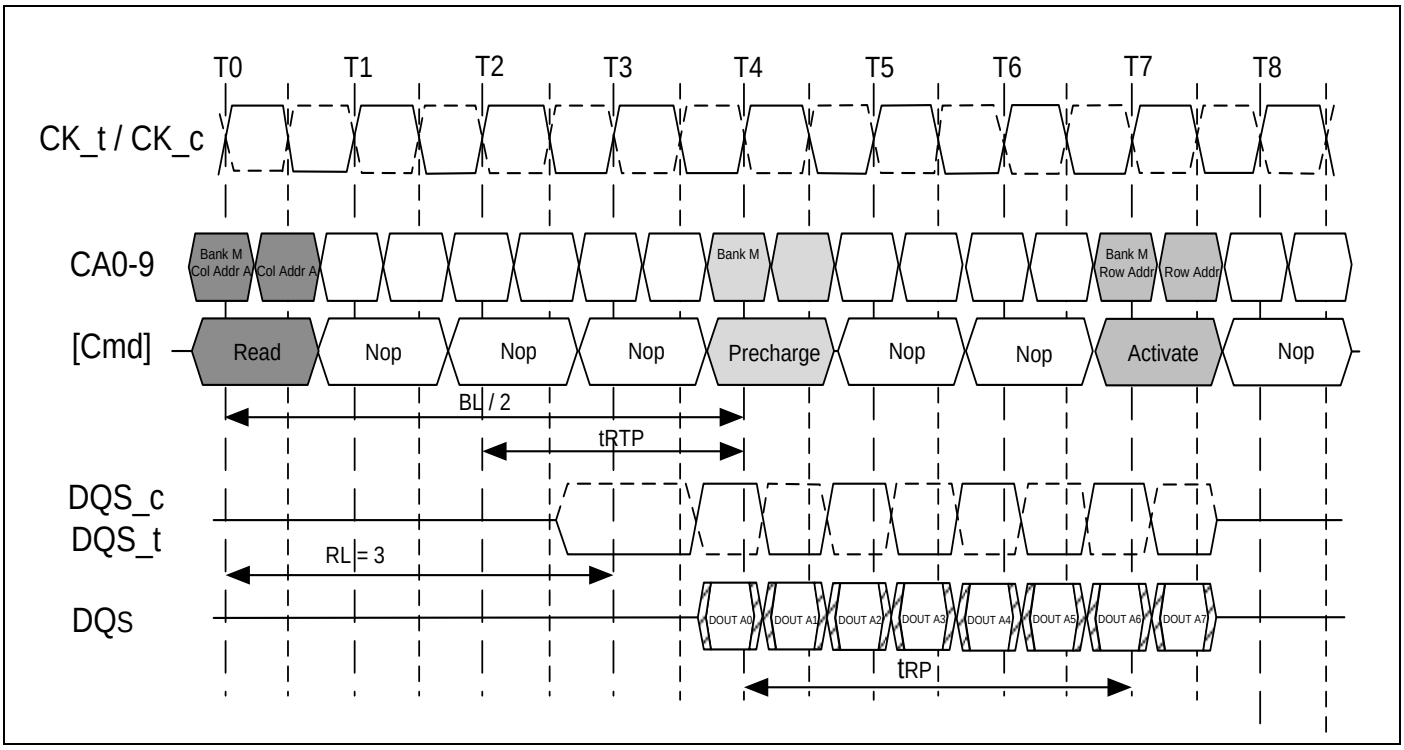
For LPDDR2-S4 devices, the minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read command. This time is called $t_{RTP}$ (Read to Precharge).

For LPDDR2-S4 devices, $t_{RTP}$ begins BL/2 - 2 clock cycles after the Read command. If the burst is truncated by a BST command or a Read command to a different bank, the effective "BL" shall be used to calculate when $t_{RTP}$ begins.

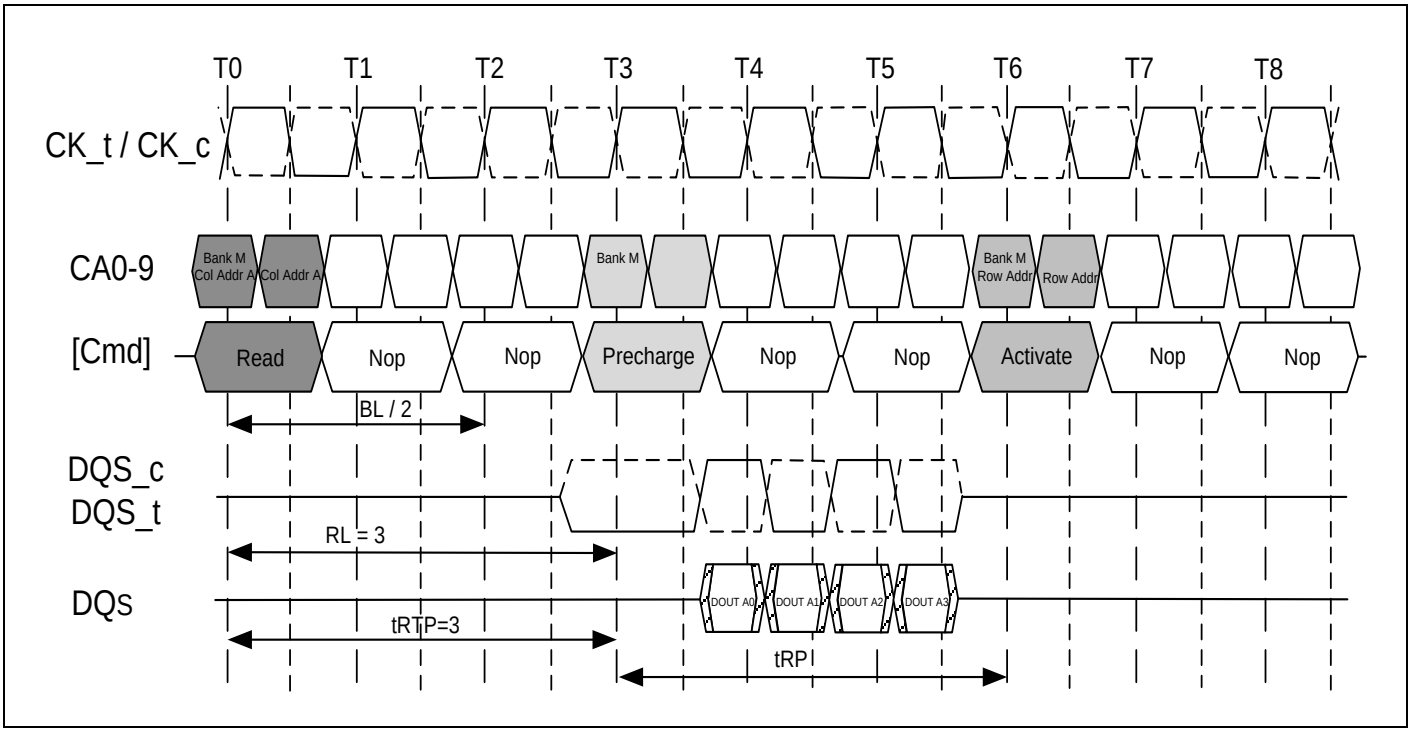
See 7.4.14.2 **"Precharge & Auto Precharge Clarification"** table for Read to Precharge timings.


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### 7.4.10.1 Burst Read Followed by Precharge: RL = 3, BL = 8, RU($t_{RTP(min)}/t_{CK}$) = 2




### 7.4.10.2 Burst Read Followed by Precharge: RL = 3, BL = 4, RU($t_{RTP(min)}/t_{CK}$) = 3



### 7.4.11 Burst Write Followed by Precharge

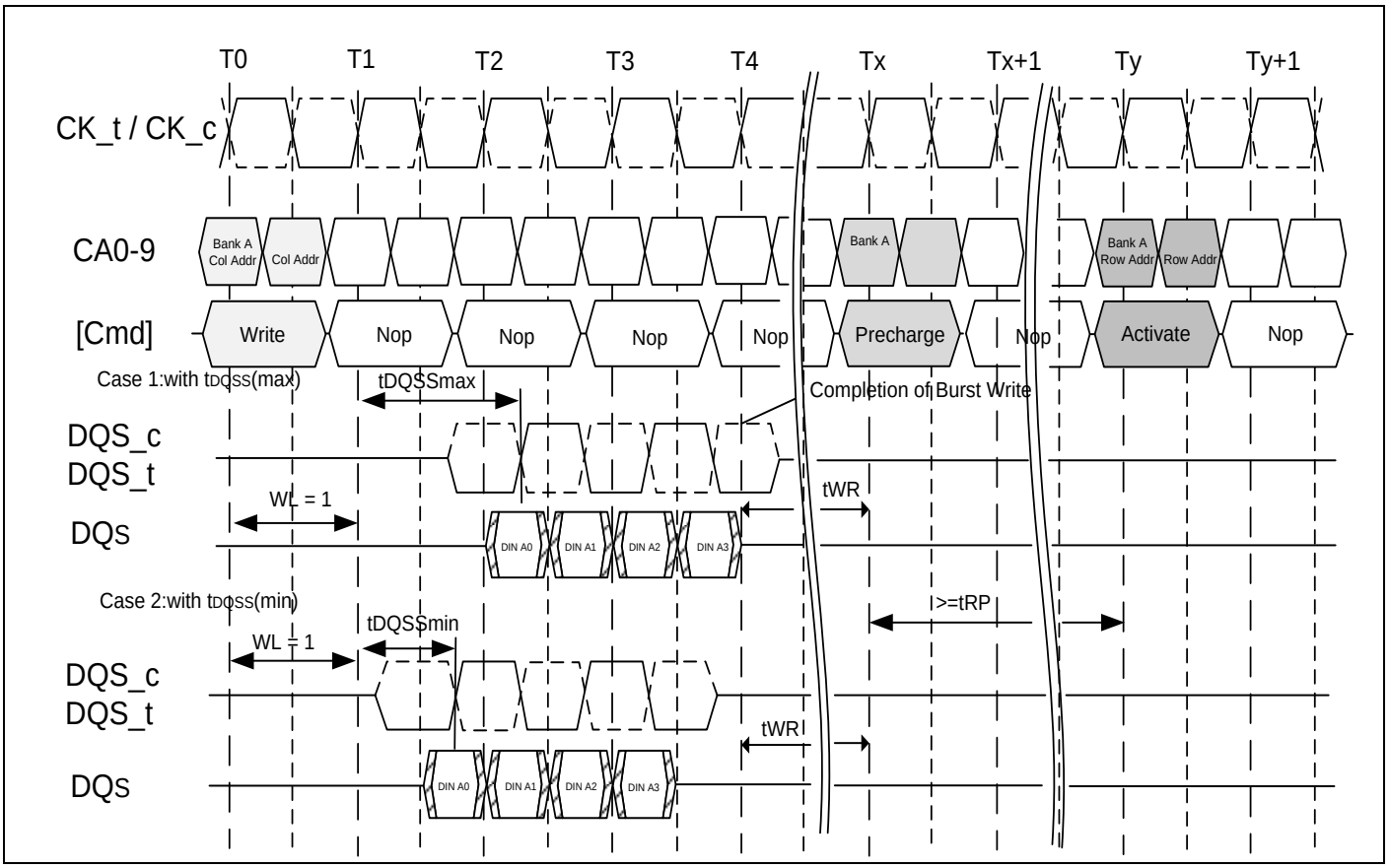
For write cycles, a delay must be satisfied from the time of the last valid burst input data until the Precharge command may be issued. This delay is known as the write recovery time (tWR) referenced from the completion of the burst write to the precharge command. No Precharge command to the same bank should be issued prior to the tWR delay.

LPDDR2-S4 devices write data to the array in prefetch quadruples (prefetch = 4). The beginning of an internal write operation may only begin after a prefetch group has been latched completely. Therefore, the write recovery time (tWR) starts at different boundaries.

The minimum Write to Precharge command spacing to the same bank is WL + BL/2 + 1 + RU(tWR/tCK) clock cycles. For an untruncated burst, BL is the value from the Mode Register. For a truncated burst, BL is the effective burst length.

See 7.4.14.2 **"Precharge & Auto Precharge Clarification"** table for Write to Precharge timings.

#### 7.4.11.1 Burst Write Followed by Precharge: WL = 1, BL = 4



### 7.4.12 Auto Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is given to the LPDDR2 SDRAM, the AP bit (CA0f) may be set to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle.

If AP is LOW when the Read or Write command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the Read or Write command is issued, then the auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon Read or Write latency) thus improving system performance for random data access.

### 7.4.13 Burst Read with Auto-Precharge

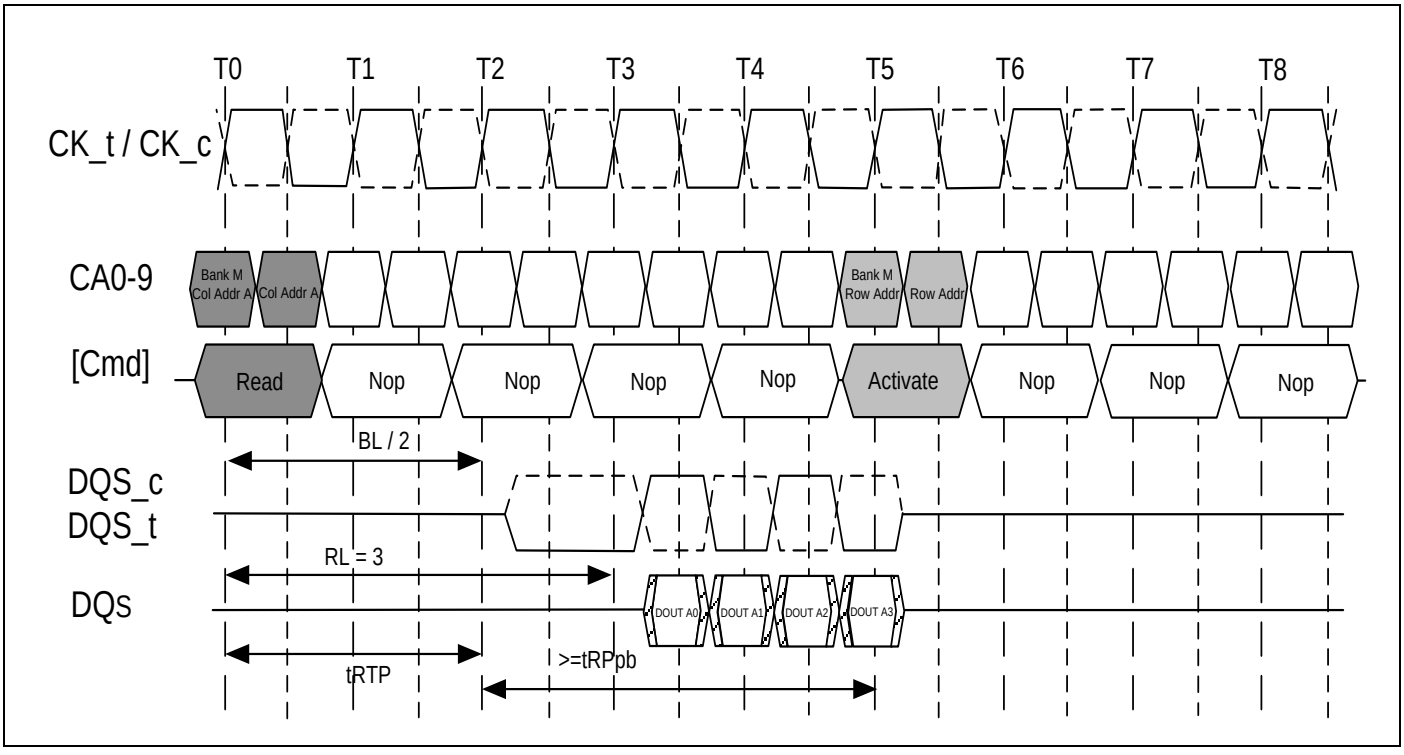
If AP (CA0f) is HIGH when a Read Command is issued, the Read with Auto-Precharge function is engaged.

LPDDR2-S4 devices start an Auto-Precharge operation on the rising edge of the clock BL/2 or BL/2 - 2 + RU(tRTP/tCK) clock cycles later than the Read with AP command, whichever is greater. Refer to section 7.4.14.2 **"Precharge & Auto Precharge Clarification"** table for equations related to Auto-Precharge for LPDDR2-S4.

A new bank Activate command may be issued to the same bank if both of the following two conditions are satisfied simultaneously.

- The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time (tRC) from the previous bank activation has been satisfied.

#### 7.4.13.1 Burst Read with Auto-Precharge: RL = 3, BL = 4, RU(tRTP(min)/tCK) = 2



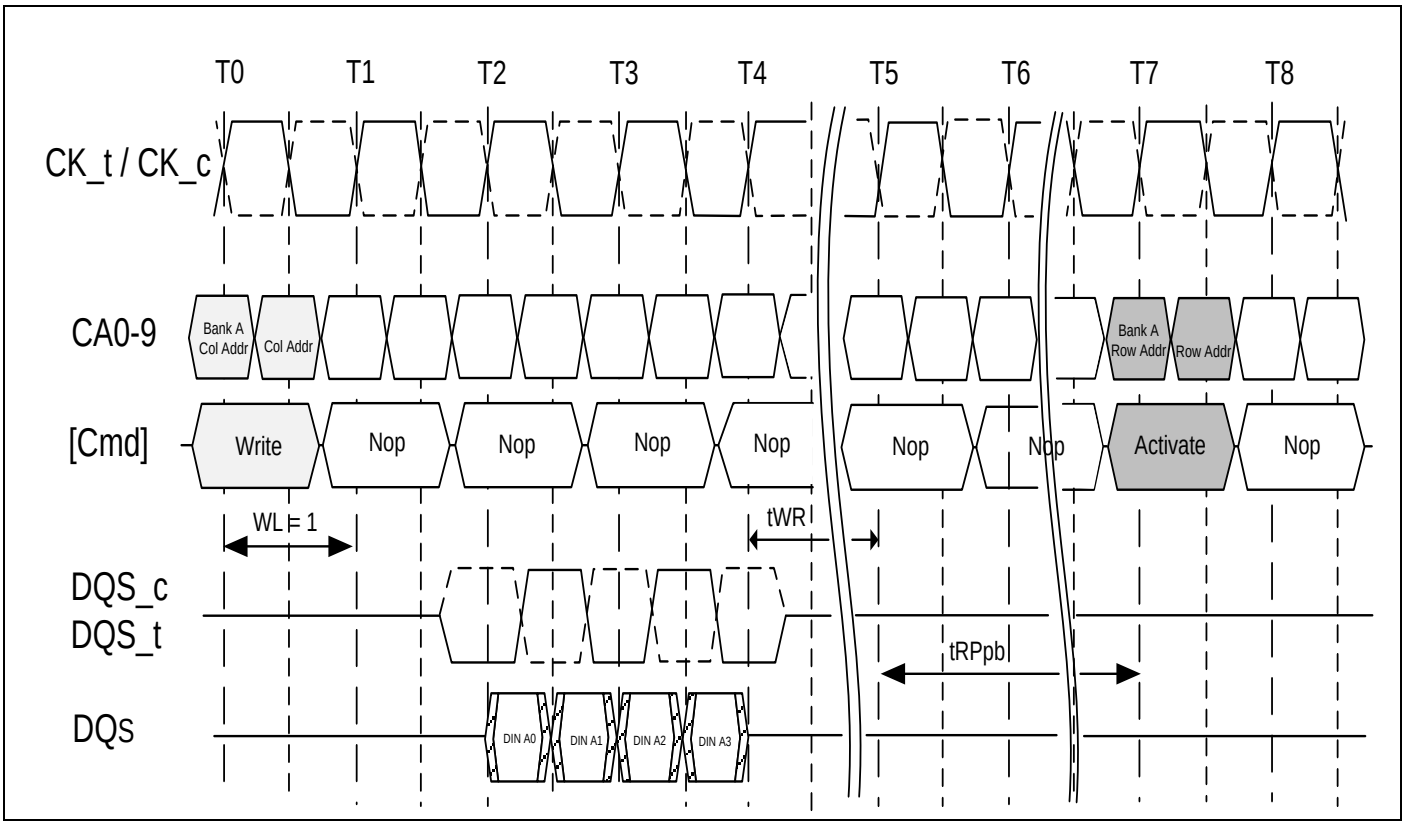
### 7.4.14 Burst Write with Auto-Precharge

If AP (CA0f) is HIGH when a Write Command is issued, the Write with Auto-Precharge function is engaged. The LPDDR2 SDRAM starts an Auto Precharge operation on the rising edge which is tWR cycles after the completion of the burst write.

A new bank activate (command) may be issued to the same bank if both of the following two conditions are satisfied.

- The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time (tRC) from the previous bank activation has been satisfied.

#### 7.4.14.1 Burst Write with Auto-Precharge: WL = 1, BL = 4





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### 7.4.14.2 Precharge & Auto Precharge Clarification

| From Command | To Command | Minimum Delay between "From Command" to "To Command" | Unit | Notes |
|---|---|---|---|---|
| Read | Precharge (to same Bank as Read) | BL/2 + max(2, RU(tRTP/tCK)) - 2 | CLK | 1 |
| | Precharge All | BL/2 + max(2, RU(tRTP/tCK)) - 2 | CLK | 1 |
| BST (for Reads) | Precharge (to same Bank as Read) | 1 | CLK | 1 |
| | Precharge All | 1 | CLK | 1 |
| Read w/AP | Precharge (to same Bank as Read w/AP) | BL/2 + max(2, RU(tRTP/tCK)) - 2 | CLK | 1, 2 |
| | Precharge All | BL/2 + max(2, RU(tRTP/tCK)) - 2 | CLK | 1 |
| | Activate (to same Bank as Read w/AP) | BL/2 + max(2, RU(tRTP/tCK)) - 2 + RU(tRPpb/tCK) | CLK | 1 |
| | Write or Write w/AP (same bank) | Illegal | CLK | 3 |
| | Write or Write w/AP (different bank) | RL + BL/2 + RU(tDQSCKmax/tCK) - WL + 1 | CLK | 3 |
| | Read or Read w/AP (same bank) | Illegal | CLK | 3 |
| | Read or Read w/AP (different bank) | BL/2 | CLK | 3 |
| Write | Precharge (to same Bank as Write) | WL + BL/2 + RU(tWR/tCK) + 1 | CLK | 1 |
| | Precharge All | WL + BL/2 + RU(tWR/tCK) + 1 | CLK | 1 |
| BST (for Writes) | Precharge (to same Bank as Write) | WL + RU(tWR/tCK) + 1 | CLK | 1 |
| | Precharge All | WL + RU(tWR/tCK) + 1 | CLK | 1 |
| Write w/AP | Precharge (to same Bank as Write w/AP) | WL + BL/2+ RU(tWR/tCK) + 1 | CLK | 1 |
| | Precharge All | WL + BL/2 + RU(tWR/tCK) + 1 | CLK | 1 |
| | Activate (to same Bank as Write w/AP) | WL + BL/2 + RU(tWR/tCK) + 1 + RU(tRPpb/tCK) | CLK | 1 |
| | Write or Write w/AP (same bank) | Illegal | CLK | 3 |
| | Write or Write w/AP (different bank) | BL/2 | CLK | 3 |
| | Read or Read w/AP (same bank) | Illegal | CLK | 3 |
| | Read or Read w/AP (different bank) | WL + BL/2 + RU(tWTR/tCK) + 1 | CLK | 3 |
| Precharge | Precharge (to same Bank as Precharge) | 1 | CLK | 1 |
| | Precharge All | 1 | CLK | 1 |
| Precharge All | Precharge | 1 | CLK | 1 |
| | Precharge All | 1 | CLK | 1 |

**Notes:**

1. For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after tRP depending on the latest precharge command issued to that bank.
2. Any command issued during the specified minimum delay time is illegal.
3. After Read with AP, seamless read operations to different banks are supported. After Write with AP, seamless write operations to different banks are supported. Read w/AP and Write w/AP may not be interrupted or truncated.


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### 7.4.15 Refresh Command

The Refresh command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of clock. Per Bank Refresh is initiated by having CA3 LOW at the rising edge of clock.

An All Bank Refresh command, REFab performs a refresh operation to all banks. All banks have to be in Idle state when REFab is issued (for instance, by Precharge all-bank command). REFab also synchronizes the bank count between the controller and the SDRAM to zero.

As shown in 7.4.15.1 **"Command Scheduling Separations Related to Refresh"** table, the REFab command may not be issued to the memory until the following conditions have been met:

a) The $t_{RFCab}$ has been satisfied after the prior REFab command

b) The $t_{RP}$ has been satisfied after prior Precharge commands

When the All Bank refresh cycle has completed, all banks will be in the Idle state.

As shown in 7.4.15.1 **"Command Scheduling Separations Related to Refresh"** table, after issuing REFab:

a) The $t_{RFCab}$ latency must be satisfied before issuing an ACTIVATE command

b) The $t_{RFCab}$ latency must be satisfied before issuing a REFab command

#### 7.4.15.1 Command Scheduling Separations Related to Refresh

| Symbol | minimum delay from | to |
|---|---|---|
| $t_{RFCab}$ | REFab | REFab |
| | | Activate cmd to any bank |
| $t_{RRD}$ | Activate | Activate cmd to different bank than prior Activate |
| **Note:** A bank must be in the Idle state before it is refreshed. | | |


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### 7.4.16 LPDDR2 SDRAM Refresh Requirements

(1) Minimum number of Refresh commands:

The LPDDR2 SDRAM requires a minimum number of R Refresh (REFab) commands within any rolling Refresh Window ($t_{REFW}$ = 32 mS @ MR4[2:0] = "011" or $T_{CASE} \leq 85°C$). The required minimum number of Refresh commands and resulting average refresh interval ($t_{REFI}$) are given in 8.6.1 **"Refresh Requirement Parameters"** table. See Mode Register 4 for $t_{REFW}$ and $t_{REFI}$ refresh multipliers at different MR4 settings.

(2) Burst Refresh limitation:

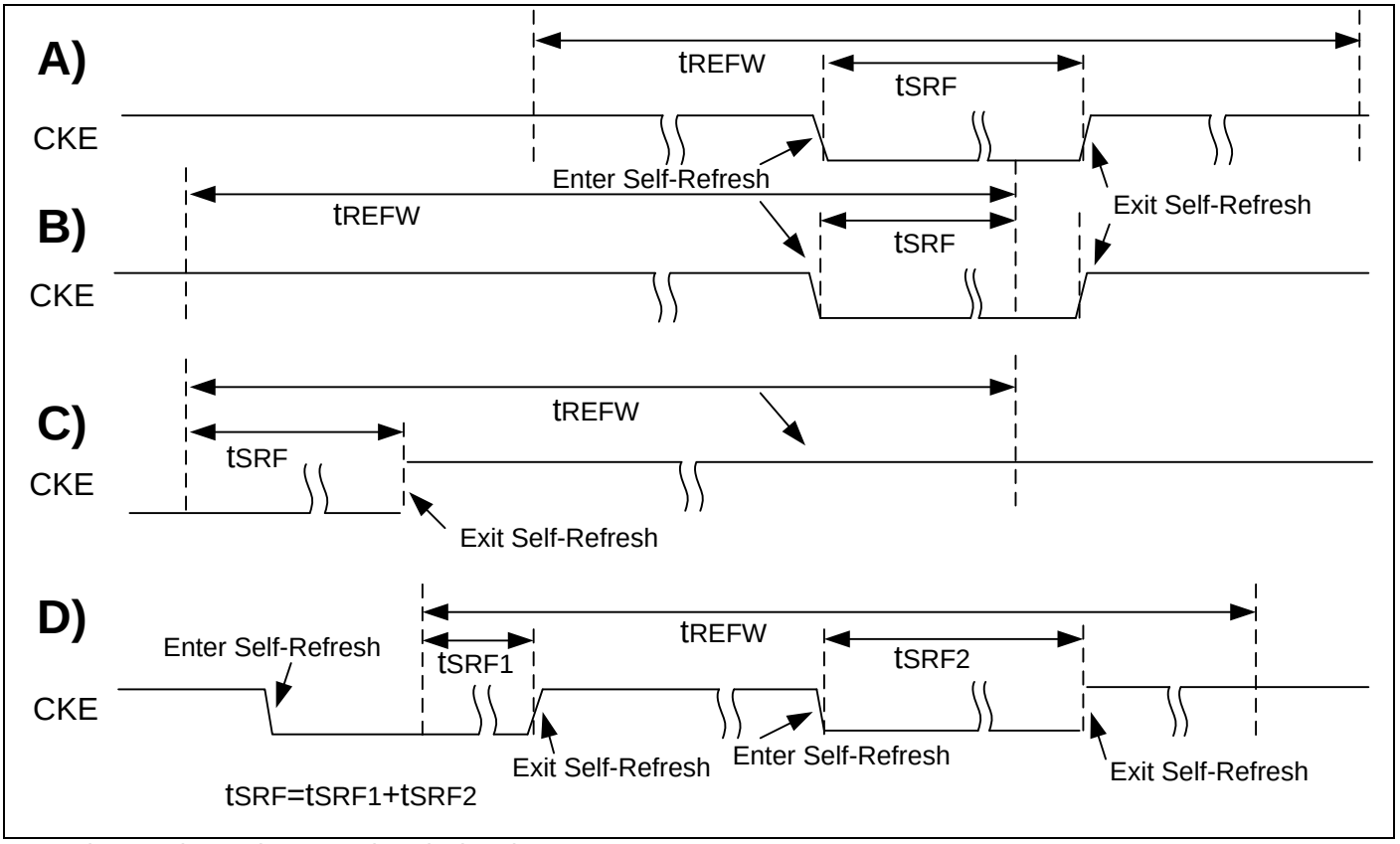
To limit maximum current consumption, a maximum of 8 REFab commands may be issued in any rolling $t_{REFBW}$ ($t_{REFBW}$ = 4 x 8 x $t_{RFCab}$).

(3) Refresh Requirements and Self-Refresh:

If any time within a refresh window is spent in Self-Refresh Mode, the number of required Refresh commands in this particular window is reduced to:

**R* = R - RU{tSRF / tREFI} = R - RU{R * tSRF / tREFW}**; where RU stands for the round-up function.

#### 7.4.16.1 Definition of $t_{SRF}$




Several examples on how $t_{SRF}$ is calculated:

A: with the time spent in Self-Refresh Mode fully enclosed in the Refresh Window ($t_{REFW}$).

B: at Self-Refresh entry.

C: at Self-Refresh exit.

D: with several different intervals spent in Self Refresh during one $t_{REFW}$ interval.

In contrast to JESD79 and JESD79-2 and JESD79-3 compliant SDRAM devices, LPDDR2-S4 devices allow significant flexibility in scheduling REFRESH commands, as long as the boundary conditions above are met. In the most straight forward case a REFRESH command should be scheduled every $t_{REFI}$. In this case Self-Refresh may be entered at any time.
The users may choose to deviate from this regular refresh pattern e.g., to enable a period where no refreshes are required. As an example, using a 1Gb LPDDR2-S4 device, the user can choose to issue a refresh burst of 4096 REFRESH commands with the maximum allowable rate (limited by $t_{REFBW}$) followed by a long time without any REFRESH commands, until the refresh window is complete, then repeating this sequence. The achievable time without REFRESH commands is given by $t_{REFW}$ - (R / 8) * $t_{REFBW}$ = $t_{REFW}$ - R * 4 * $t_{RFCab}$.@ $T_{CASE}$ ≤ 85°C this can be up to 32 mS - 4096 * 4 * 130 nS ≈ 30 mS.

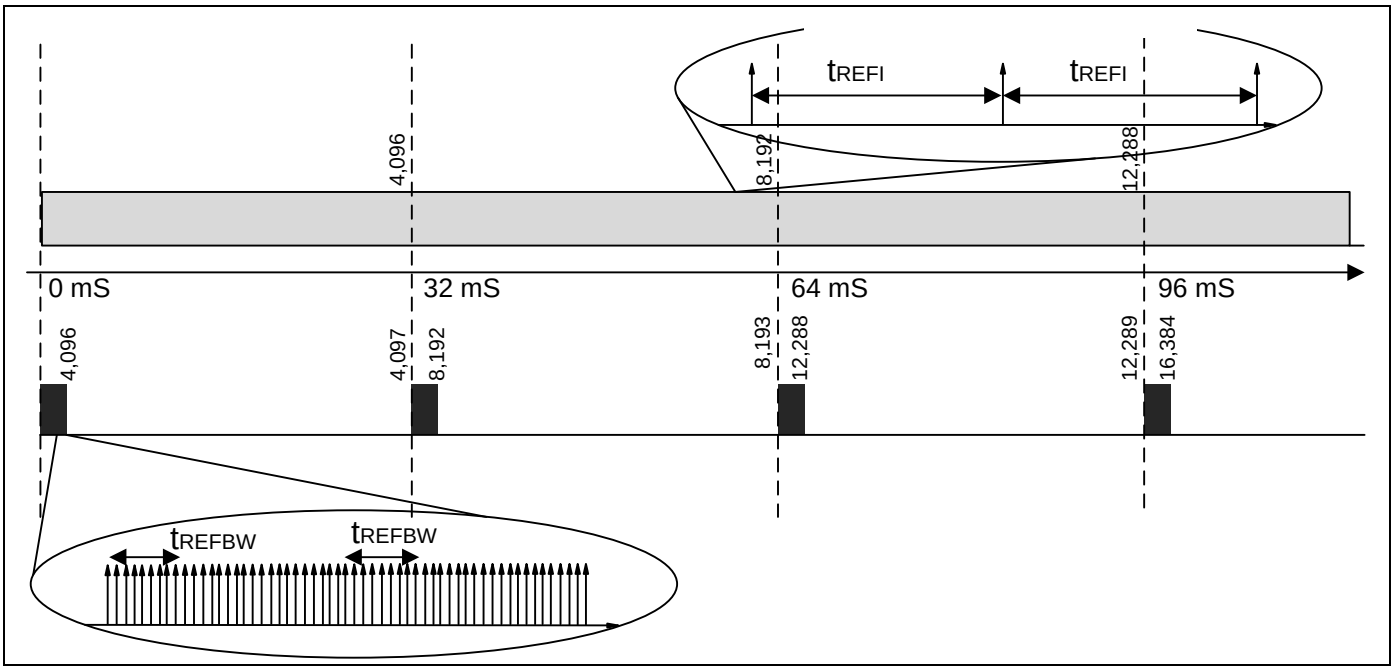
While both - the regular and the burst/pause - patterns can satisfy the refresh requirements per rolling refresh interval, if they are repeated in every subsequent 32 mS window, extreme care must be taken when transitioning from one pattern to another to satisfy the refresh requirement in every rolling refresh window during the transition.

Figure of **7.4.16.3** shows an example of an allowable transition from a burst pattern to a regular, distributed pattern. If this transition happens directly after the burst refresh phase, all rolling $t_{REFW}$ intervals will have at least the required number of REFRESH commands.

Figure of **7.4.16.4** shows an example of a non-allowable transition. In this case the regular refresh pattern starts after the completion of the pause-phase of the burst/pause refresh pattern. For several rolling $t_{REFW}$ intervals the minimum number of REFRESH commands is not satisfied.

The understanding of the pattern transition is extremely relevant (even if in normal operation only one pattern is employed), as in Self-Refresh-Mode a regular, distributed refresh pattern has to be assumed, which is reflected in the equation for R* above. Therefore it is recommended to enter Self-Refresh-Mode ONLY directly after the burst-phase of a burst/pause refresh pattern as indicated in figure of **7.4.16.5** and begin with the burst phase upon exit from Self-Refresh.

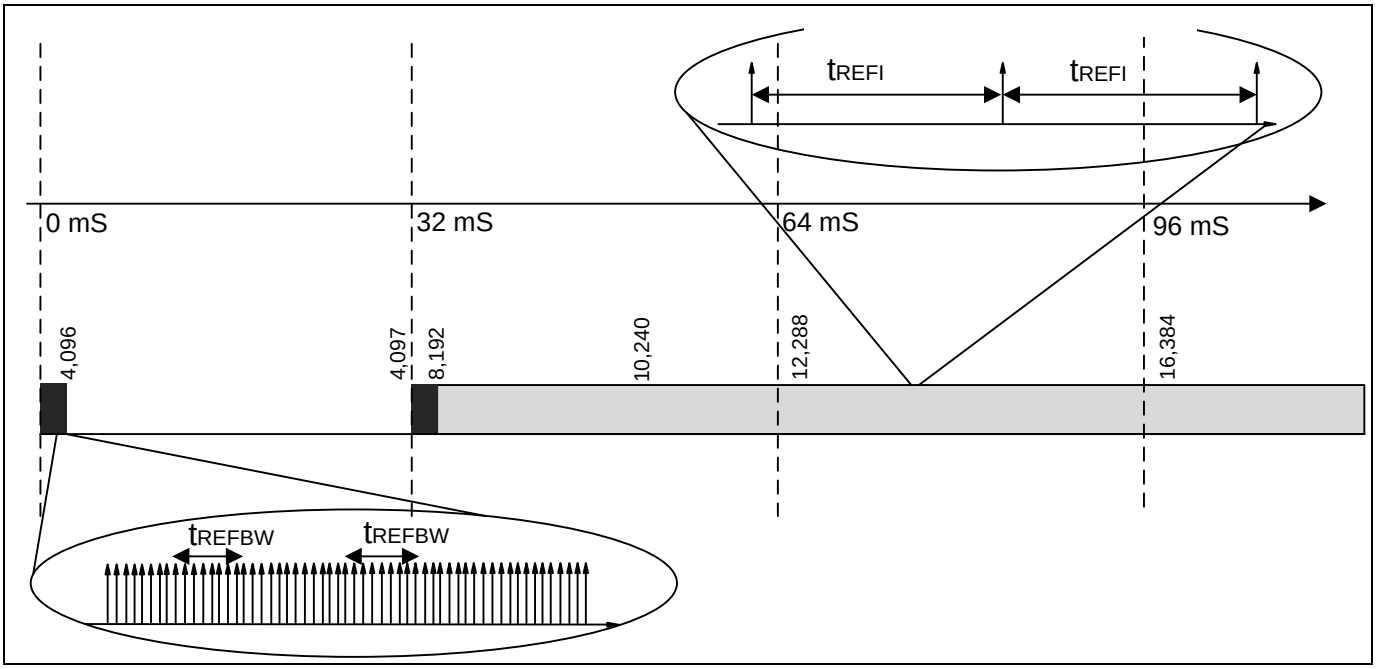
### 7.4.16.2 Regular, Distributed Refresh Pattern




**Notes:**

1. Compared to repetitive burst Refresh with subsequent Refresh pause.
2. For an example, in a 1Gb LPDDR2 device at $T_{CASE}$ ≤ 85°C, the distributed refresh pattern would have one REFRESH command per 7.8 µS; the burst refresh pattern would have an average of one refresh command per 0.52 µS followed by ≈30 mS without any REFRESH command.

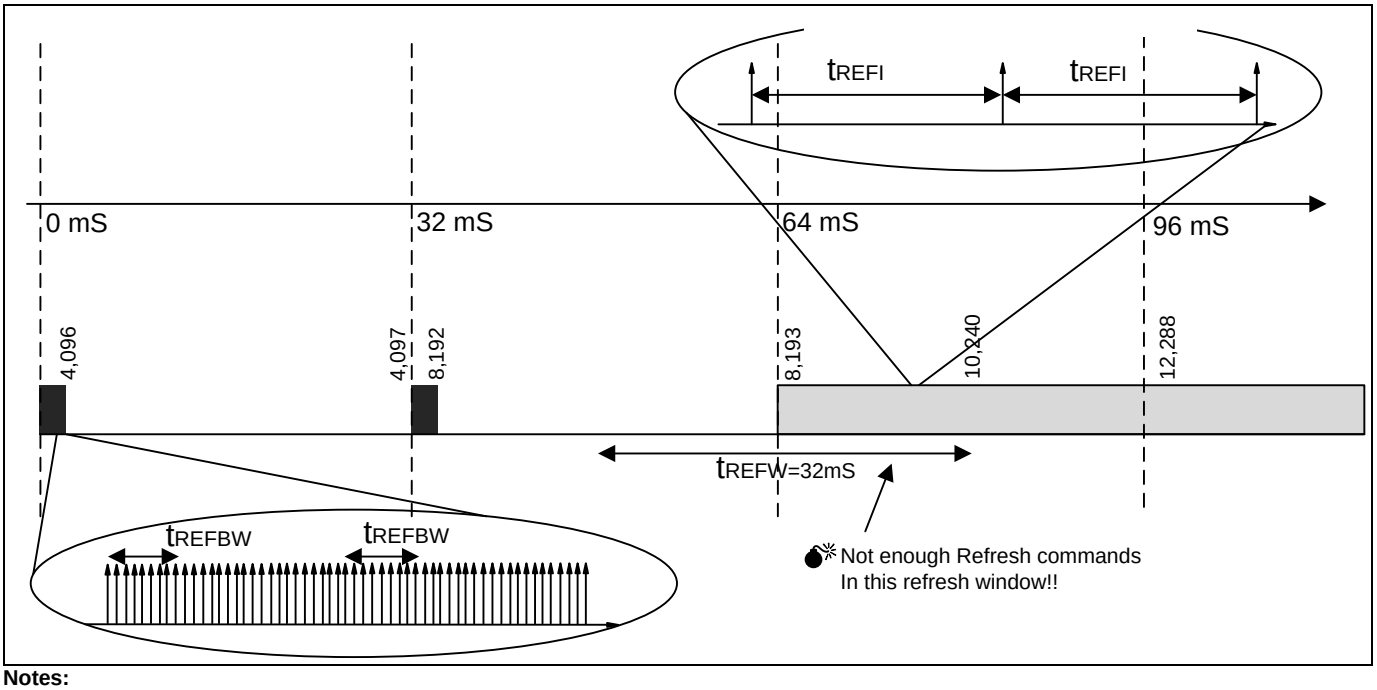
### 7.4.16.3 Allowable Transition from Repetitive Burst Refresh




**Notes:**

1. Shown with subsequent Refresh pause to regular distributed Refresh pattern.
2. For an example, in a 1Gb LPDDR2 device at $T_{CASE} \leq 85°C$, the distributed refresh pattern would have one REFRESH command per 7.8 µS; the burst refresh pattern would have an average of one refresh command per 0.52 µS followed by ≈30 mS without any REFRESH command.

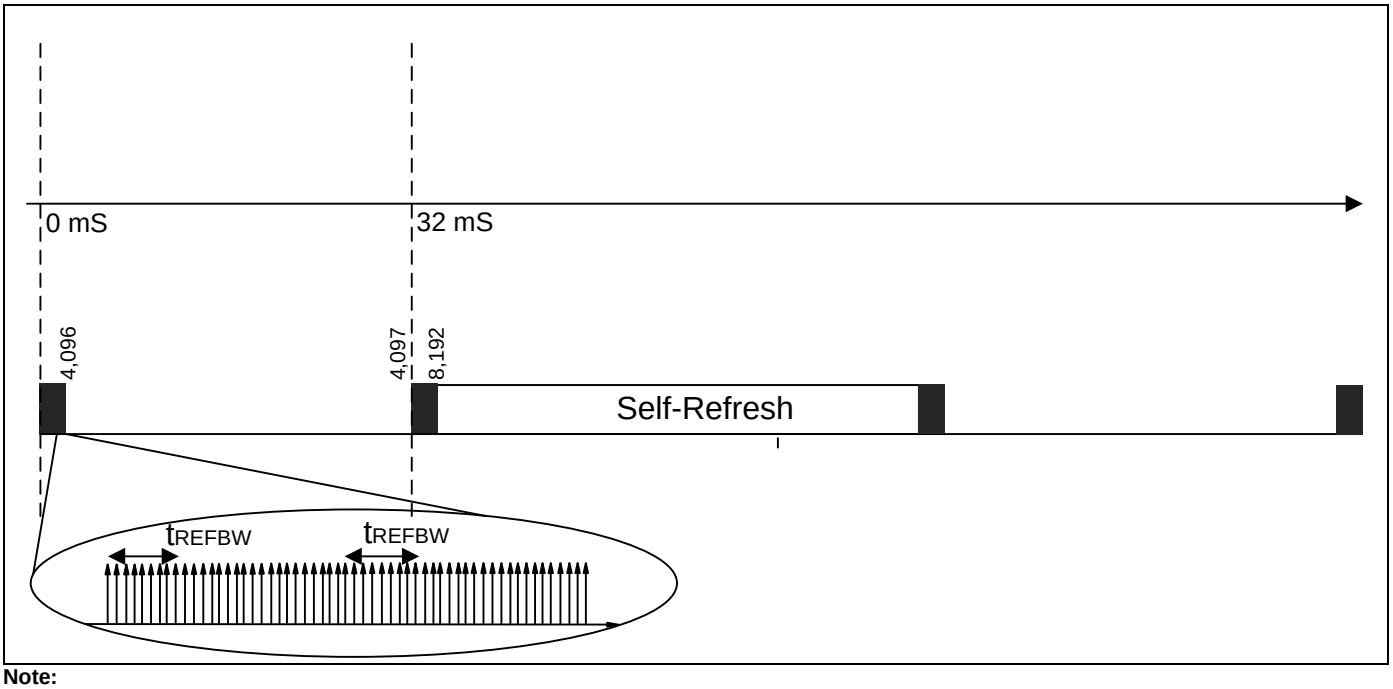
### 7.4.16.4 NOT-Allowable Transition from Repetitive Burst Refresh




**Notes:**

1. Shown with subsequent Refresh pause to regular distributed Refresh pattern.
2. Only ≈2048 REFRESH commands (< R which is 4096) in the indicated $t_{REFW}$ window.

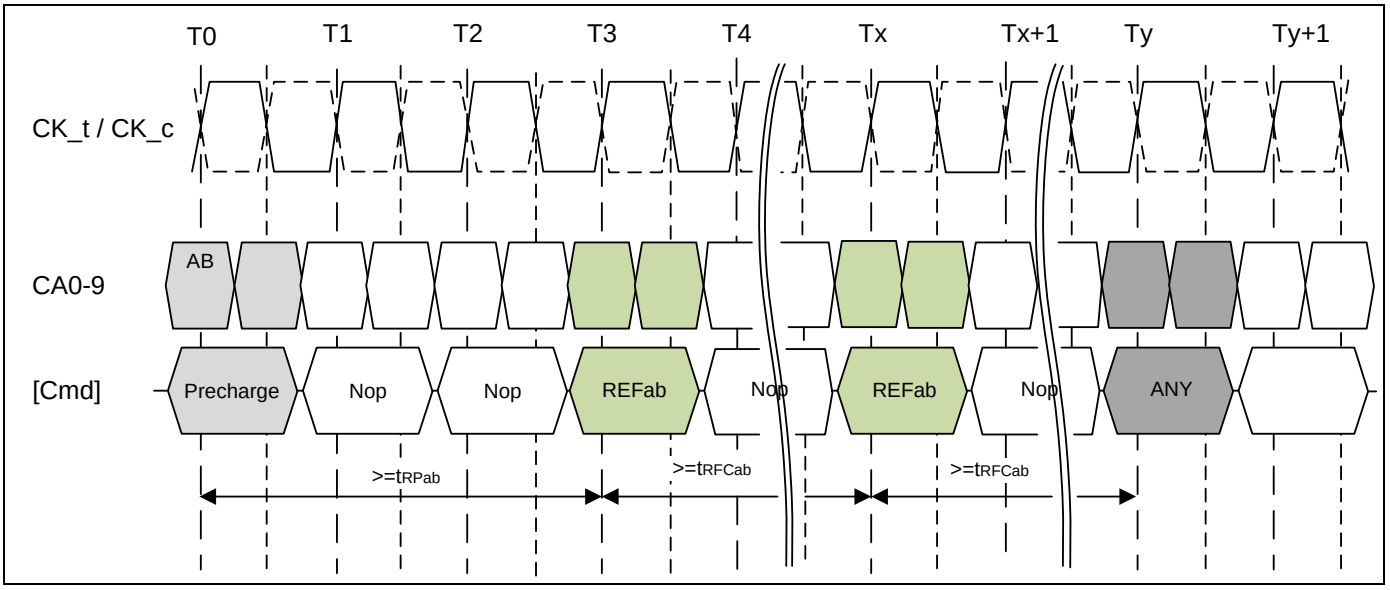
### 7.4.16.5 Recommended Self-Refresh Entry and Exit




**Note:**

1. In conjunction with a Burst/Pause Refresh patterns.

### 7.4.16.6 All Bank Refresh Operation





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### 7.4.17 Self Refresh Operation

The Self Refresh command can be used to retain data in the LPDDR2 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the LPDDR2 SDRAM retains data without external clocking. The LPDDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having CKE LOW, CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode.

LPDDR2-S4 devices can operate in Self Refresh in either the Standard or Extended Temperature Ranges. LPDDR2-S4 devices will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperatures and higher temperatures.

Once the LPDDR2 SDRAM has entered Self Refresh mode, all of the external signals except CKE, are “don’t care”. For proper self refresh operation, power supply pins ($V_{DD1}$, $V_{DD2}$, and $V_{DDCA}$) must be at valid levels. $V_{DDQ}$ may be turned off during Self-Refresh. Prior to exiting Self-Refresh, $V_{DDQ}$ must be within specified limits. $V_{refDQ}$ and $V_{refCA}$ may be at any level within minimum and maximum levels (see section 8.1 **“Absolute Maximum DC Ratings”** table). However prior to exit Self-Refresh, $V_{refDQ}$ and $V_{refCA}$ must be within specified limits (see section 8.2.1.1 **“Recommended DC Operating Conditions”** table). The SDRAM initiates a minimum of one all-bank refresh command internally within $t_{CKESR}$ period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the LPDDR2 SDRAM must remain in Self Refresh mode is $t_{CKESR}$. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock shall be stable and within specified limits for a minimum of 2 clock cycles prior to CKE going back HIGH. Once Self Refresh Exit is registered, a delay of at least $t_{XSR}$ must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period $t_{XSR}$ for proper operation except for self refresh re-entry. NOP commands must be registered on each positive clock edge during the Self Refresh exit interval $t_{XSR}$.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, it is required that at least one Refresh command (one all-bank) is issued before entry into a subsequent Self Refresh.


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For LPDDR2 SDRAM, the maximum duration in power-down mode is only limited by the refresh requirements outlined in section 7.4.16 **"LPDDR2 SDRAM Refresh Requirements"**, since no refresh operations are performed in power-down mode.

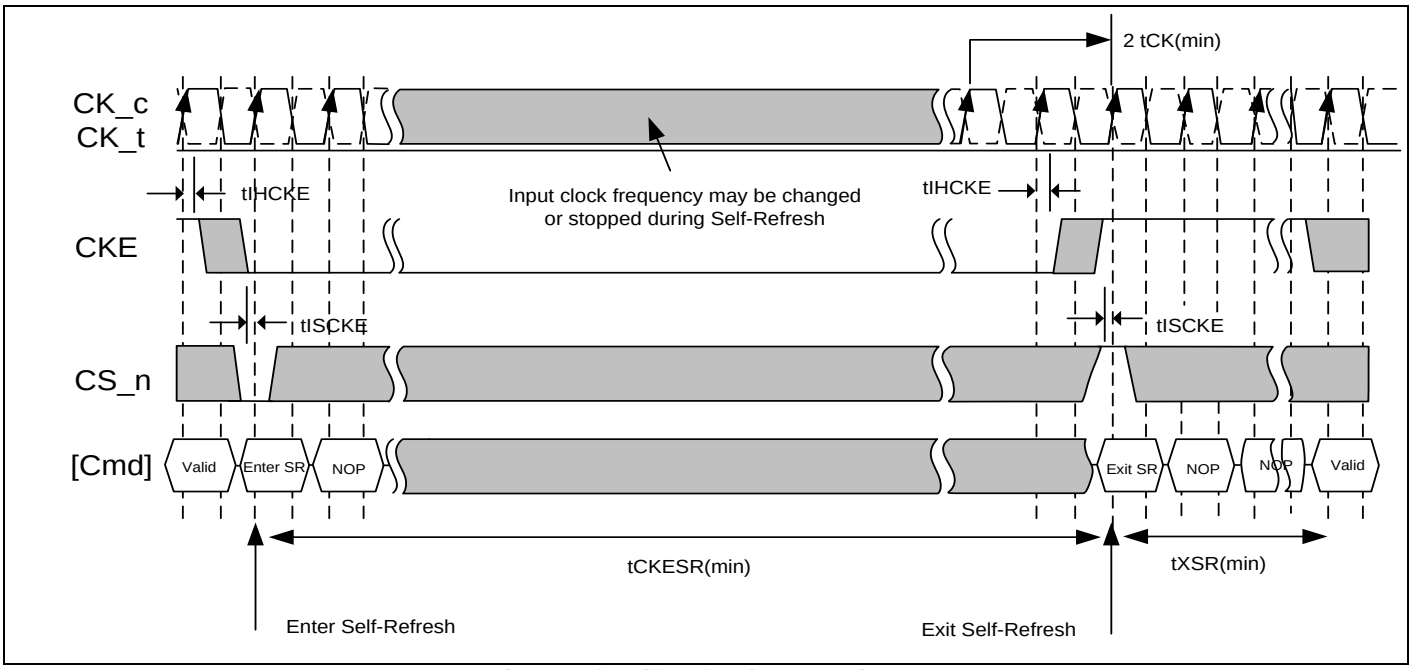



**Figure of Self Refresh Operation**

**Notes:**

1. Input clock frequency may be changed or stopped during self-refresh, provided that upon exiting self-refresh, a minimum of 2 clocks of stable clock are provided and the clock frequency is between the minimum and maximum frequency for the particular speed grad
2. Device must be in the "All banks idle" state prior to entering Self Refresh mode.
3. $t_{XSR}$ begins at the rising edge of the clock after CKE is driven HIGH.
4. A valid command may be issued only after $t_{XSR}$ is satisfied. NOPs shall be issued during $t_{XSR}$.

### 7.4.18 Partial Array Self-Refresh: Bank Masking

Each bank of LPDDR2 SDRAM can be independently configured whether a self refresh operation is taking place. One mode register unit of 4 bits accessible via MRW command is assigned to program the bank masking status of each bank up to 4 banks. For bank masking bit assignments, see section 7.3.13 Mode Register 16 **"MR16_PASR_Bank Mask (MA[7:0] = 10H)"**.

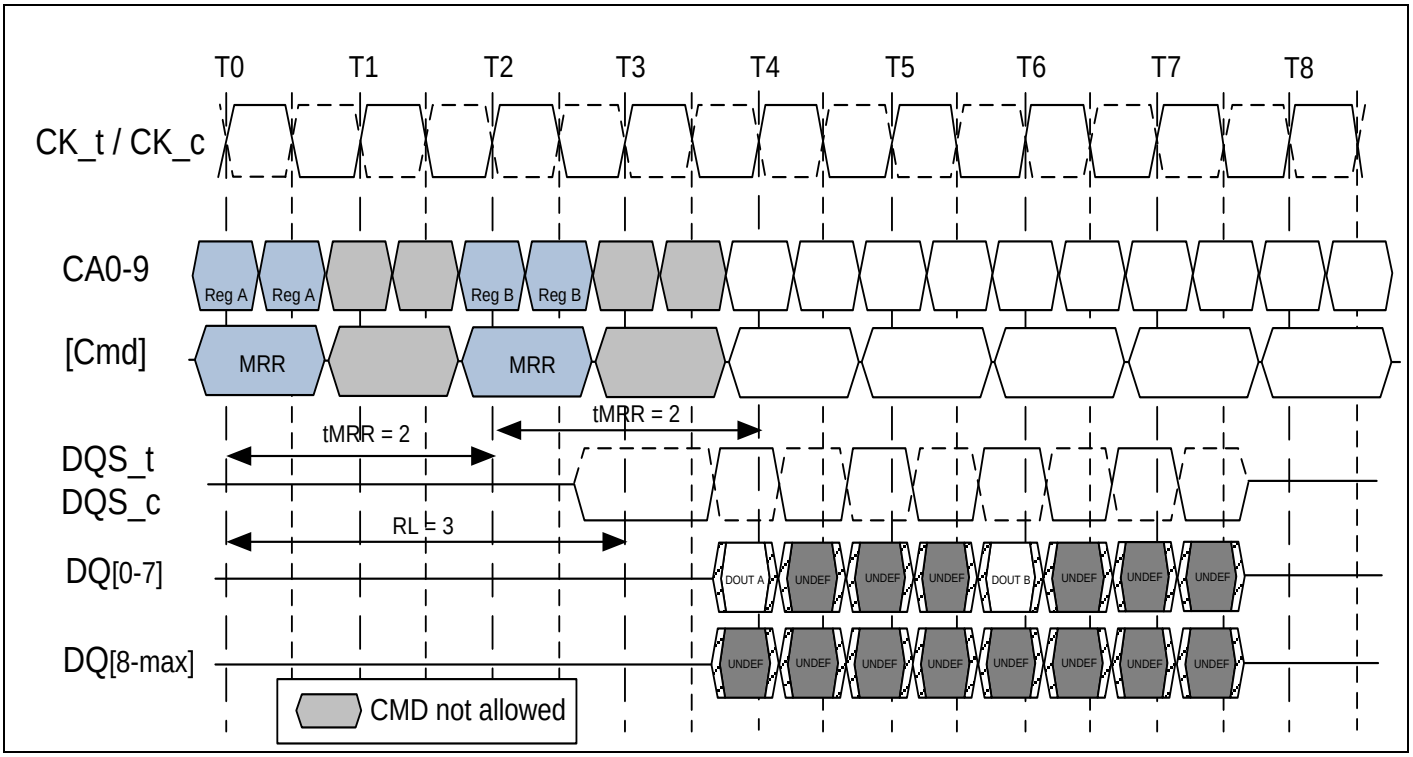
The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to the entire bank is blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, a coupled mask bit has to be programmed, "unmasked". When a bank mask bit is unmasked, a refresh to a bank is determined by the programmed status of segment mask bits.

### 7.4.19 Mode Register Read Command

The Mode Register Read command is used to read configuration and status data from mode registers. The Mode Register Read (MRR) command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r- CA4r}. The mode register contents are available on the first data beat of DQ[0:7], RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Mode Register Read Command is issued. Subsequent data beats contain valid, but undefined content, except in the case of the DQ Calibration function DQC, where subsequent data beats contain valid content as described in section 7.4.20.2 **"DQ Calibration"**. All DQS_t, DQS_c shall be toggled for the duration of the Mode Register Read burst.

The MRR command has a burst length of four. The Mode Register Read operation (consisting of the MRR command and the corresponding data traffic) shall not be interrupted. The MRR command period (tMRR) is 2 clock cycles. Mode Register Reads to reserved and write-only registers shall return valid, but undefined content on all data beats and DQS_t, DQS_c shall be toggled.

#### 7.4.19.1 Mode Register Read Timing Example: RL = 3, tMRR = 2

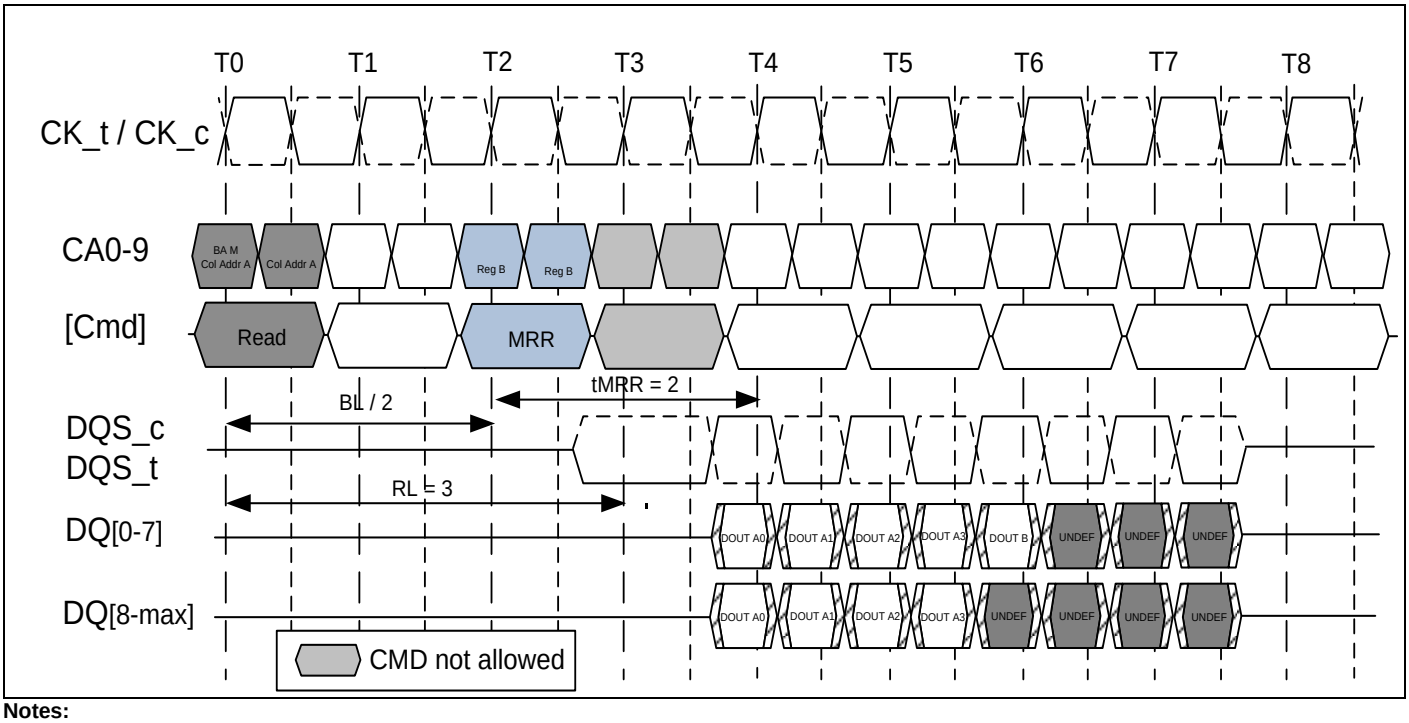



**Notes:**

1. Mode Register Read has a burst length of four.
2. Mode Register Read operation shall not be interrupted.
3. Mode Register data is valid only on DQ[0-7] on the first beat. Subsequent beats contain valid, but undefined data. DQ[8-max] contain valid, but undefined data for the duration of the MRR burst.
4. The Mode Register Command period is tMRR. No command (other than Nop) is allowed during this period.
5. Mode Register Reads to DQ Calibration registers MR32 and MR40 are described in the section on DQ Calibration.
6. Minimum Mode Register Read to write latency is RL + RU(tDQSCKmax/tCK) + 4/2 + 1 - WL clock cycles.
7. Minimum Mode Register Read to Mode Register Write latency is RL + RU(tDQSCKmax/tCK) + 4/2 + 1 clock cycles.

The MRR command shall not be issued earlier than BL/2 clock cycles after a prior Read command and WL + 1 + BL/2 + RU( tWTR/tCK) clock cycles after a prior Write command, because read-bursts and write-bursts shall not be truncated by MRR. Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as "BL".

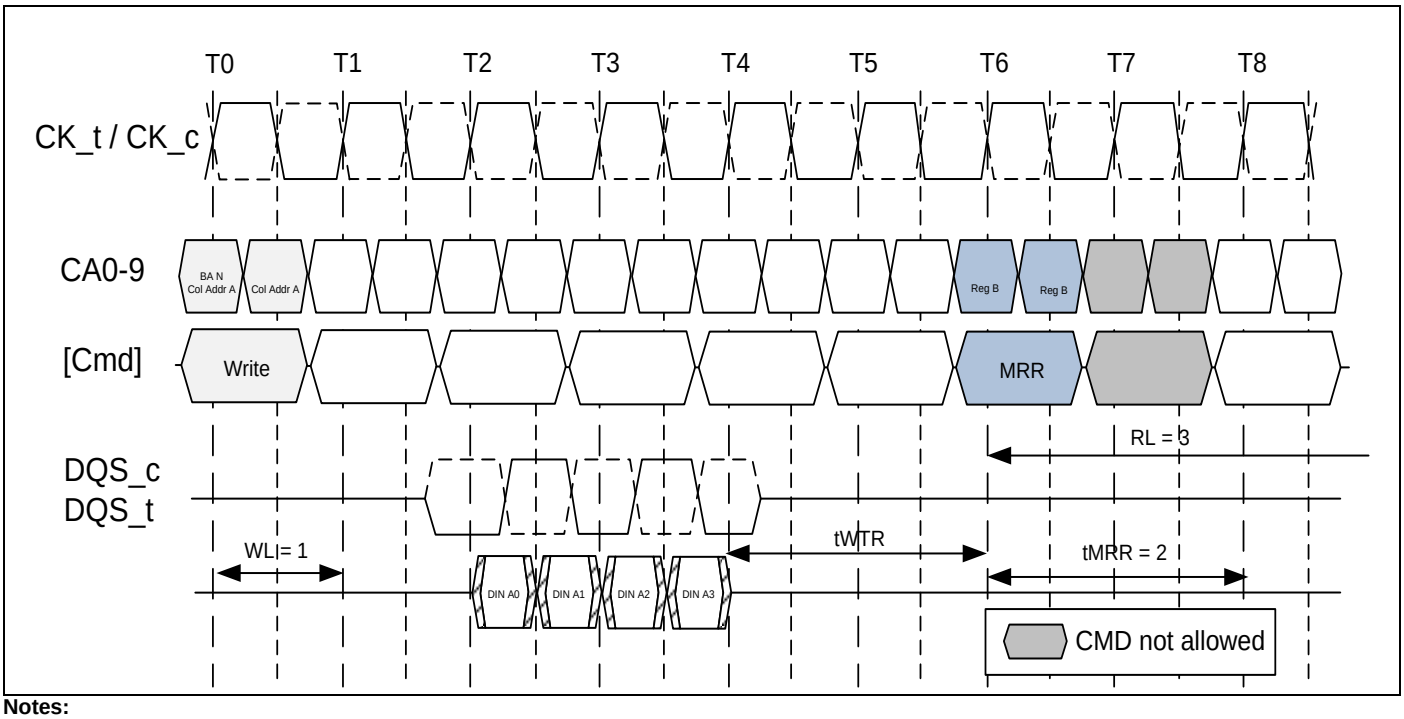
### 7.4.19.2 Read to MRR Timing Example: RL = 3, tMRR = 2




**Notes:**

1. The minimum number of clocks from the burst read command to the Mode Register Read command is BL/2.
2. The Mode Register Read Command period is tMRR. No command (other than Nop) is allowed during this period.

### 7.4.19.3 Burst Write Followed by MRR: RL = 3, WL = 1, BL = 4




**Notes:**

1. The minimum number of clock cycles from the burst write command to the Mode Register Read command is [WL + 1 + BL/2 + RU( tWTR/tCK)].
2. The Mode Register Read Command period is tMRR. No command (other than Nop) is allowed during this period.

### 7.4.20 Temperature Sensor

LPDDR2 SDRAM features a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing derating is required in the Extended Temperature Range and/or monitor the operating temperature. Either the temperature sensor or the device operating temperature (See 8.2.3 **"Operating Temperature Conditions"** table) may be used to determine whether operating temperature requirements are being met.

LPDDR2 devices shall monitor device temperature and update MR4 according to $t_{TSI}$. Upon exiting self-refresh or power-down, the device temperature status bits shall be no older than $t_{TSI}$.

When using the temperature sensor, the actual device case temperature may be higher than the operating temperature specification (See 8.2.3 **"Operating Temperature Conditions"** table) that applies for the Standard or Extended Temperature Ranges. For example, $T_{CASE}$ may be above 85°C when MR4[2:0] equals 011b.

To assure proper operation using the temperature sensor, applications should consider the following factors:

TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2°C.

ReadInterval is the time period between MR4 reads from the system.

TempSensorInterval ($t_{TSI}$) is maximum delay between internal updates of MR4.

SysRespDelay is the maximum time between a read of MR4 and the response by the system.

LPDDR2 devices shall allow for a 2°C temperature margin between the point at which the device temperature enters the Extended Temperature Range and point at which the controller re-configures the system accordingly.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$TempGradient \times (ReadInterval + tTSI + SysRespDelay) \leq 2°C$$

**Table of Temperature Sensor**

| Symbol | Parameter | Max/Min | Value | Unit |
|---|---|---|---|---|
| TempGradient | System Temperature Gradient | Max | System Dependent | °C/S |
| ReadInterval | MR4 Read Interval | Max | System Dependent | mS |
| $t_{TSI}$ | Temperature Sensor Interval | Max | 32 | mS |
| SysRespDelay | System Response Delay | Max | System Dependent | mS |
| TempMargin | Device Temperature Margin | Max | 2 | ºC |

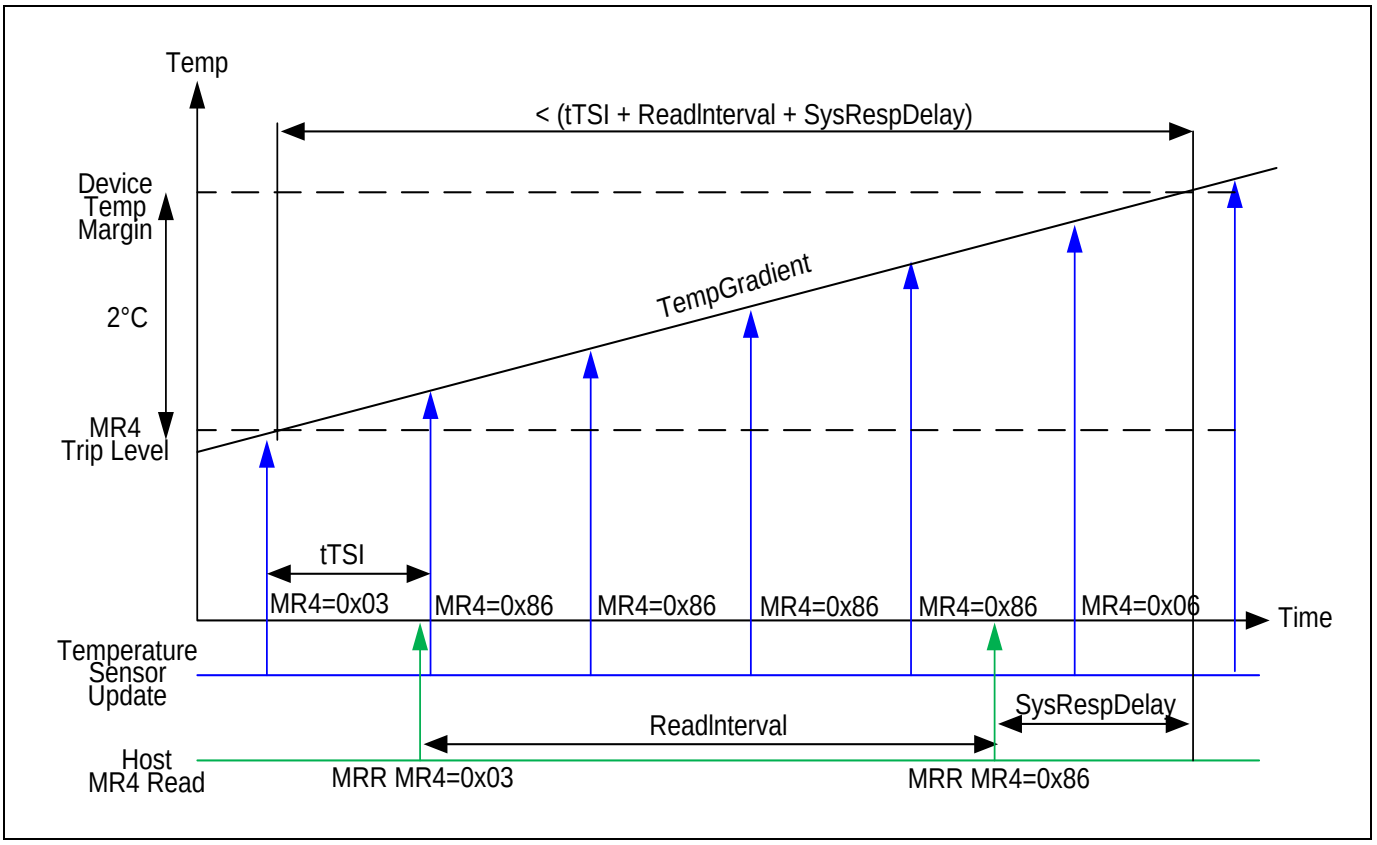
For example, if TempGradient is 10°C/s and the SysRespDelay is 1 mS:

$$10°C/s \times (ReadInterval + 32mS + 1mS) \leq 2°C$$

In this case, ReadInterval shall be no greater than 167 mS.


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#### 7.4.20.1 Temperature Sensor Timing




#### 7.4.20.2 DQ Calibration

LPDDR2 device features a DQ Calibration function that outputs one of two predefined system timing calibration patterns. A Mode Register Read to MR32 (Pattern “A”) or MR40 (Pattern “B”) will return the specified pattern on DQ[0] and DQ[8] for x16 devices, and DQ[0], DQ[8], DQ[16], and DQ[24] for x32 devices.

For x16 devices, DQ[7:1] and DQ[15:9] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst.

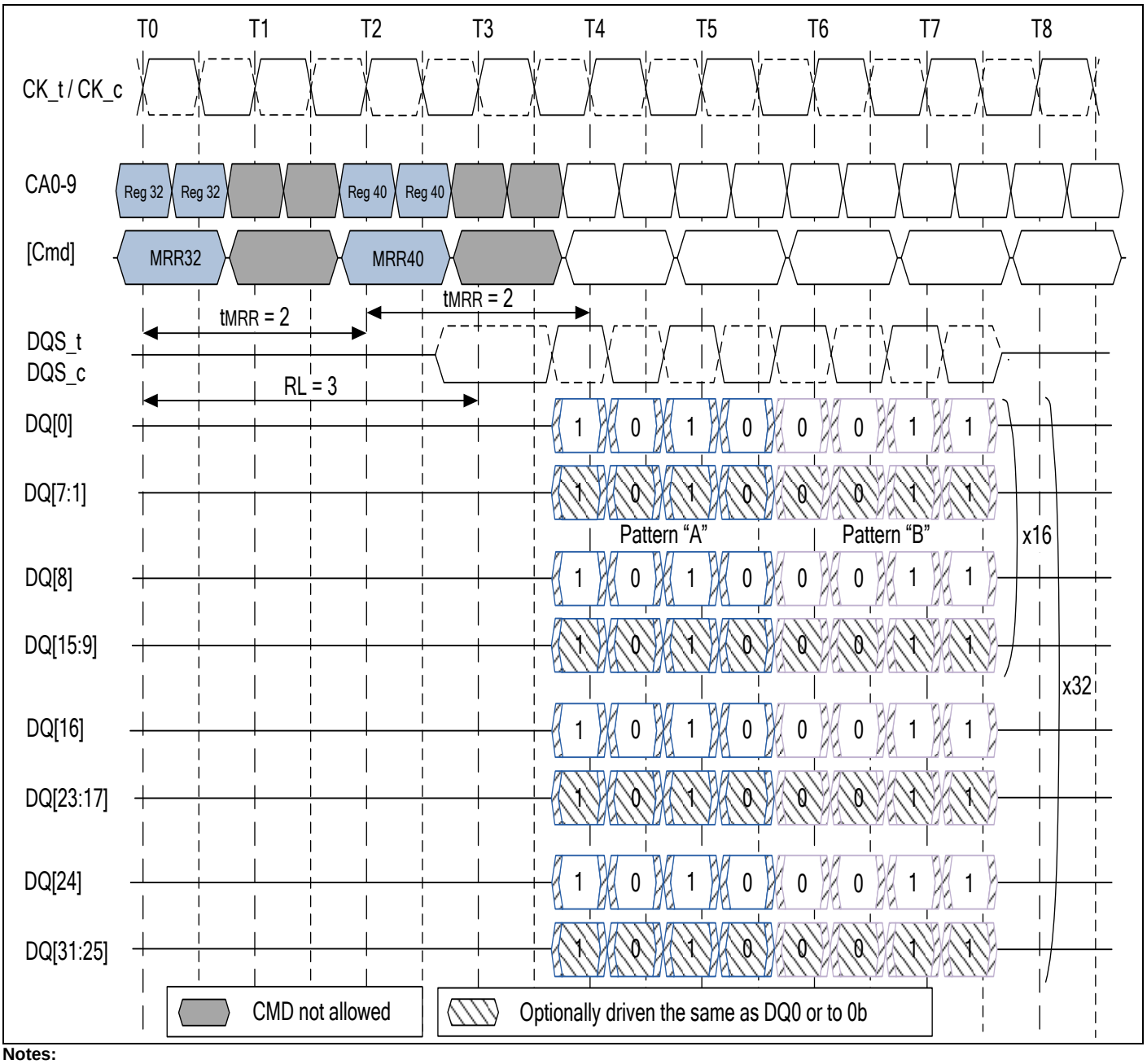
For LPDDR2-S4 devices, MRR DQ Calibration commands may only occur in the Idle state.

**Table of Data Calibration Pattern Description**

| Pattern | MR# | Bit Time 0 | Bit Time 1 | Bit Time 2 | Bit Time 3 | Description |
|---|---|---|---|---|---|---|
| Pattern A | MR32 | 1 | 0 | 1 | 0 | Read to MR32 return DQ calibration pattern A |
| Pattern B | MR40 | 0 | 0 | 1 | 1 | Read to MR40 return DQ calibration pattern B |


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### 7.4.20.3 MR32 and MR40 DQ Calibration Timing Example: RL = 3, tMRR = 2




**Notes:**

1. Mode Register Read has a burst length of four.
2. Mode Register Read operation shall not be interrupted.
3. Mode Register Reads to MR32 and MR40 drive valid data on DQ[0] during the entire burst. For x16 devices, DQ[8] shall drive the same information as DQ[0] during the burst. For x32 devices, DQ[8], DQ[16], and DQ[24] shall drive the same information as DQ[0] during the burst.
4. For x16 devices, DQ[7:1] and DQ[15:9] may optionally drive the same information as DQ[0] or they may drive 0b during the burst.
   For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or they may drive 0b during the burst.
5. The Mode Register Command period is tMRR. No command (other than Nop) is allowed during this period.

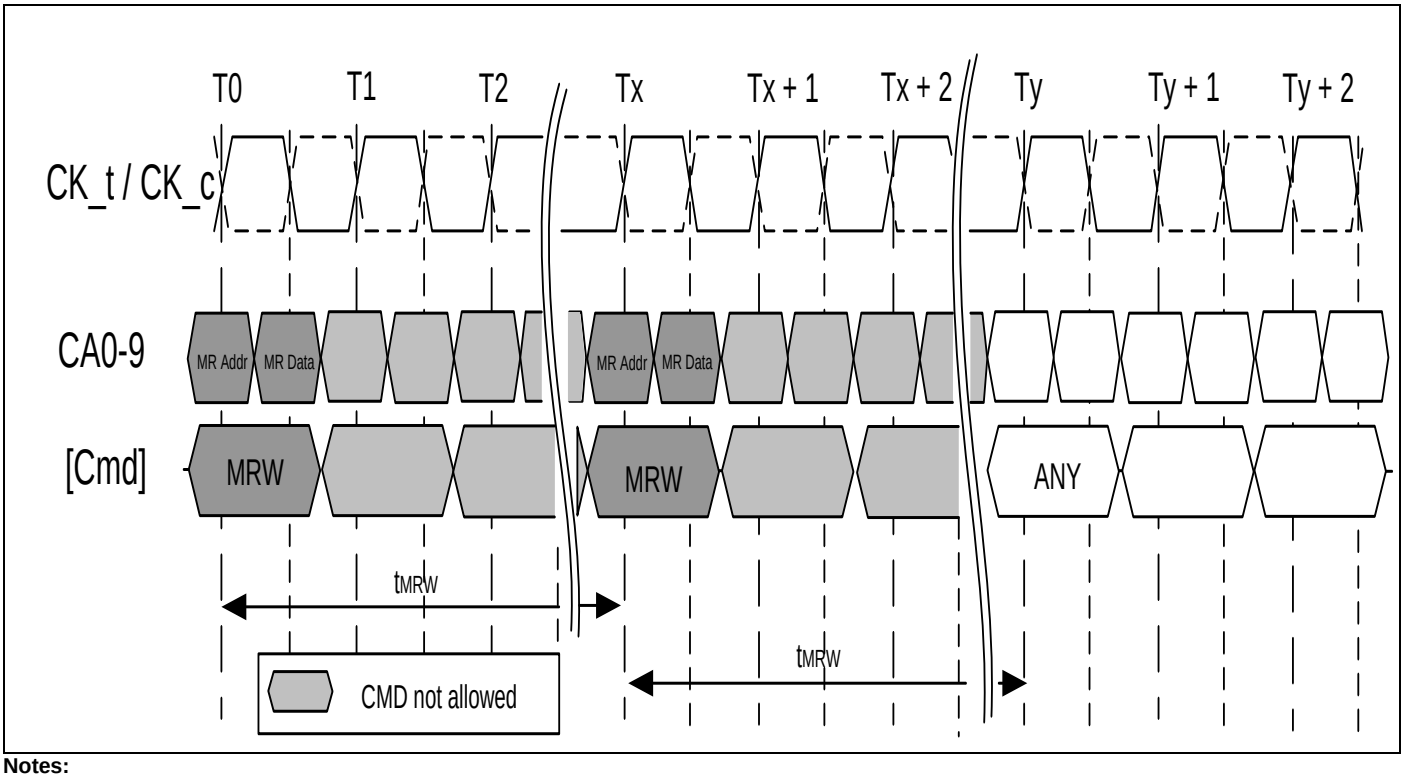

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### 7.4.21 Mode Register Write Command

The Mode Register Write command is used to write configuration data to mode registers. The Mode Register Write (MRW) command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The data to be written to the mode register is contained in CA9f-CA2f. The MRW command period is defined by $t_{MRW}$. Mode Register Writes to read-only registers shall have no impact on the functionality of the device.

For LPDDR2-S4 devices, the MRW may only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in the idle precharge state is to issue a Precharge-All command.

#### 7.4.21.1 Mode Register Write Timing Example: RL = 3, $t_{MRW}$ = 5




**Notes:**

1. The Mode Register Write Command period is $t_{MRW}$. No command (other than Nop) is allowed during this period.
2. At time Ty, the device is in the idle state.

#### 7.4.21.2 Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)

| Current State | Command | Intermediate State | Next State |
|---|---|---|---|
| All Banks Idle | MRR | Mode Register Reading (All Banks Idle) | All Banks Idle |
| | MRW | Mode Register Writing (All Banks Idle) | All Banks Idle |
| | MRW (RESET) | Resetting (Device Auto-Initialization) | All Banks Idle |
| Bank(s) Active | MRR | Mode Register Reading (Bank(s) Active) | Bank(s) Active |
| | MRW | Not Allowed | Not Allowed |
| | MRW (RESET) | Not Allowed | Not Allowed |

### 7.4.22 Mode Register Write Reset (MRW Reset)

Any MRW command issued to MRW63 initiates an MRW Reset. The MRW Reset command brings the device to the Device Auto-Initialization (Resetting) State in the Power-On Initialization sequence (see step 3 in sections 7.2.1 **"Power Ramp and Device Initialization"**). The MRW Reset command may be issued from the Idle state for LPDDR2-S4 devices. This command resets all Mode Registers to their default values. No commands other than NOP may be issued to the LPDDR2 device during the MRW Reset period ($t_{INIT4}$). After MRW Reset, boot timings must be observed until the device initialization sequence is complete and the device is in the Idle state. Array data for LPDDR2-S4 devices are undefined after the MRW Reset command.

For the timing diagram related to MRW Reset, refer to 7.2.3 **"Power Ramp and Initialization Sequence"** figure.

### 7.4.23 Mode Register Write ZQ Calibration Command

The MRW command is also used to initiate the ZQ Calibration command. The ZQ Calibration command is used to calibrate the LPDDR2 output drivers (RON) over process, temperature, and voltage. LPDDR2-S4 devices support ZQ Calibration.

There are four ZQ Calibration commands and related timings times, $t_{ZQINIT}$, $t_{ZQRESET}$, $t_{ZQCL}$, and $t_{ZQCS}$. $t_{ZQINIT}$ corresponds to the initialization calibration, $t_{ZQRESET}$ for resetting ZQ setting to default, $t_{ZQCL}$ is for long calibration, and $t_{ZQCS}$ is for short calibration. See Mode Register 10 (MR10) for description on the command codes for the different ZQ Calibration commands.

The Initialization ZQ Calibration (ZQINIT) shall be performed for LPDDR2-S4 devices. This Initialization Calibration achieves a RON accuracy of ±15%. After initialization, the ZQ Long Calibration may be used to re-calibrate the system to a RON accuracy of ±15%. A ZQ Short Calibration may be used periodically to compensate for temperature and voltage drift in the system.

The ZQReset Command resets the RON calibration to a default accuracy of ±30% across process, voltage, and temperature. This command is used to ensure RON accuracy to ±30% when ZQCS and ZQCL are not used.

One ZQCS command can effectively correct a minimum of 1.5% (ZQCorrection) of RON impedance error within $t_{ZQCS}$ for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity'. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.

One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the LPDDR2 is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

where TSens = max(dRONdT) and VSens = max(dRONdV) define the LPDDR2 temperature and voltage sensitivities.

For example, if TSens = 0.75% / °C, VSens = 0.20% / mV, Tdriftrate = 1°C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$

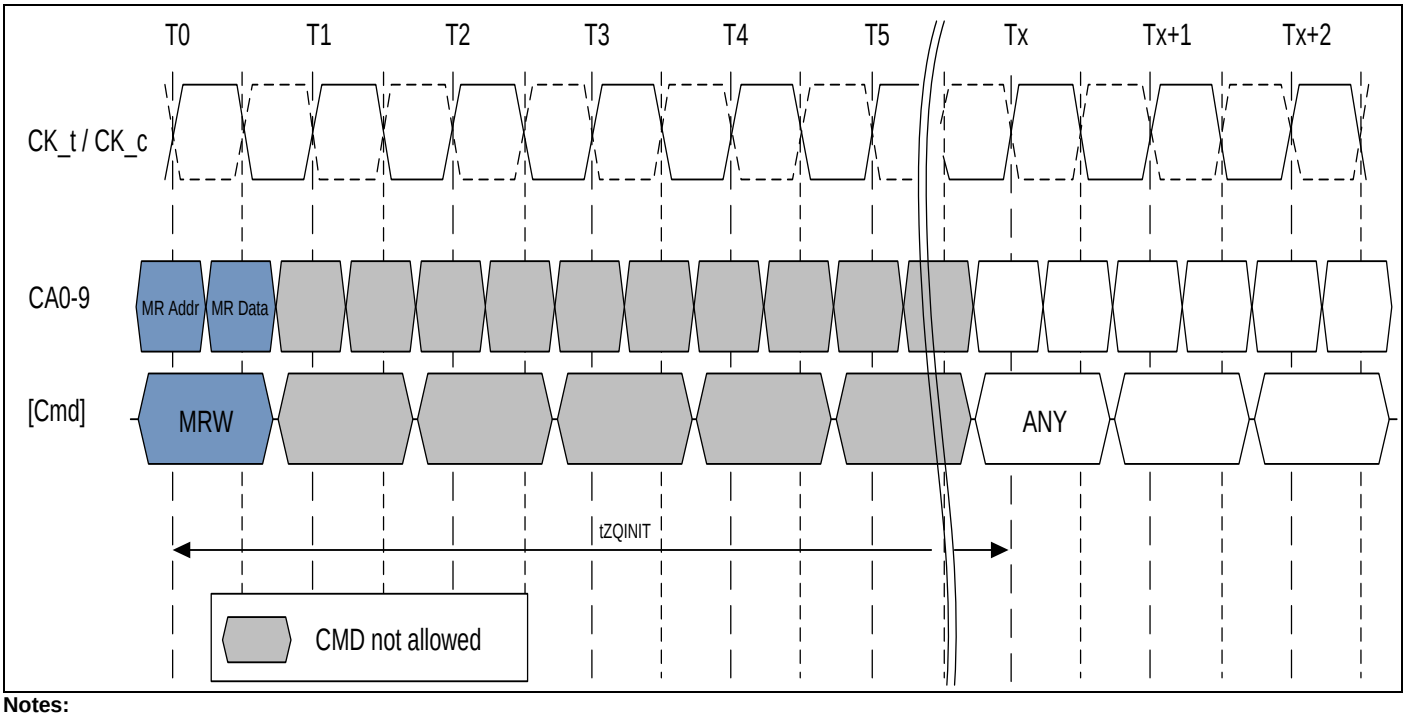
For LPDDR2-S4 devices, a ZQ Calibration command may only be issued when the device is in Idle state with all banks precharged.

No other activities can be performed on the LPDDR2 data bus during the calibration period ($t_{ZQINIT}$, $t_{ZQCL}$, $t_{ZQCS}$). The quiet time on the LPDDR2 data bus helps to accurately calibrate RON. There is no required quiet time after the ZQ Reset command. If multiple devices share a single ZQ Resistor, only one device may be calibrating at any given time. After calibration is achieved, the LPDDR2 device shall disable the ZQ pin's current consumption path to reduce power.

In systems that share the ZQ resistor between devices, the controller must not allow overlap of $t_{ZQINIT}$, $t_{ZQCS}$, or $t_{ZQCL}$ between the devices. ZQ Reset overlap is allowed. If the ZQ resistor is absent from the system, ZQ shall be connected to $V_{DDCA}$. In this case, the LPDDR2 device shall ignore ZQ calibration commands and the device will use the default calibration settings (See section 8.2.6.5 **"RONPU and RONPD Characteristics without ZQ Calibration"** Output Driver DC Electrical Characteristics without ZQ Calibration table).


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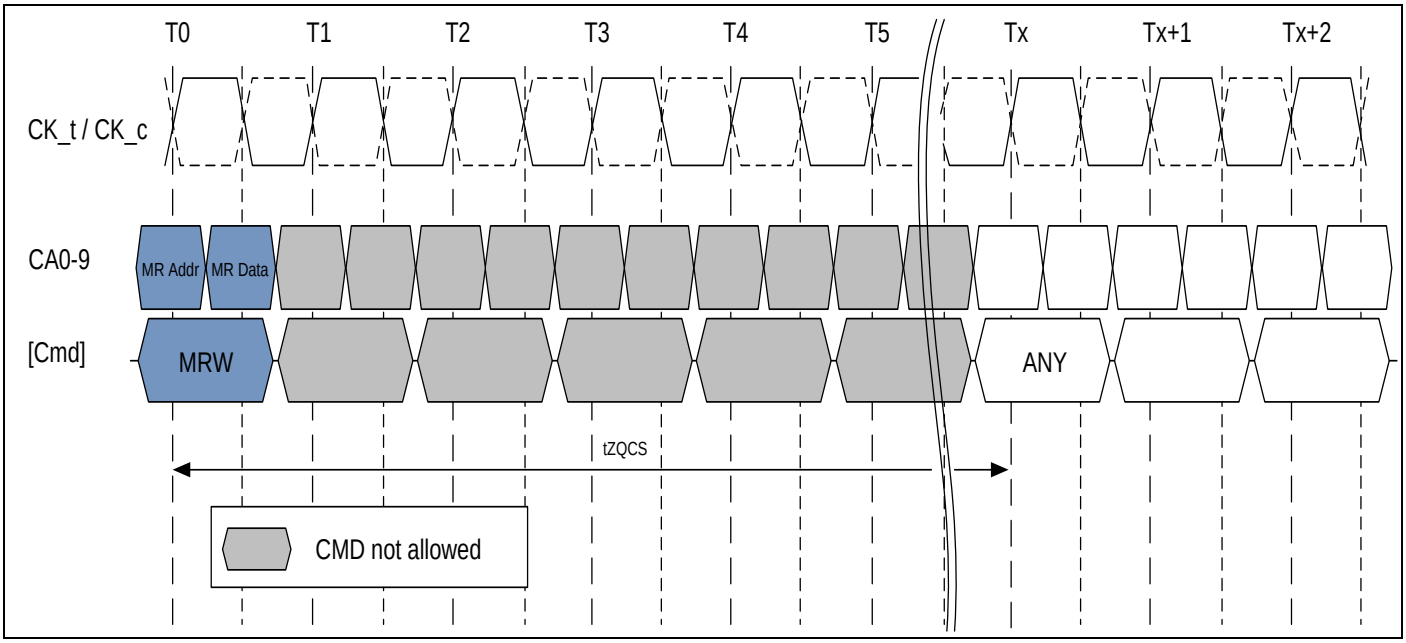
### 7.4.23.1 ZQ Calibration Initialization Timing Example




**Notes:**

1. The ZQ Calibration Initialization period is tZQINIT. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

### 7.4.23.2 ZQ Calibration Short Timing Example

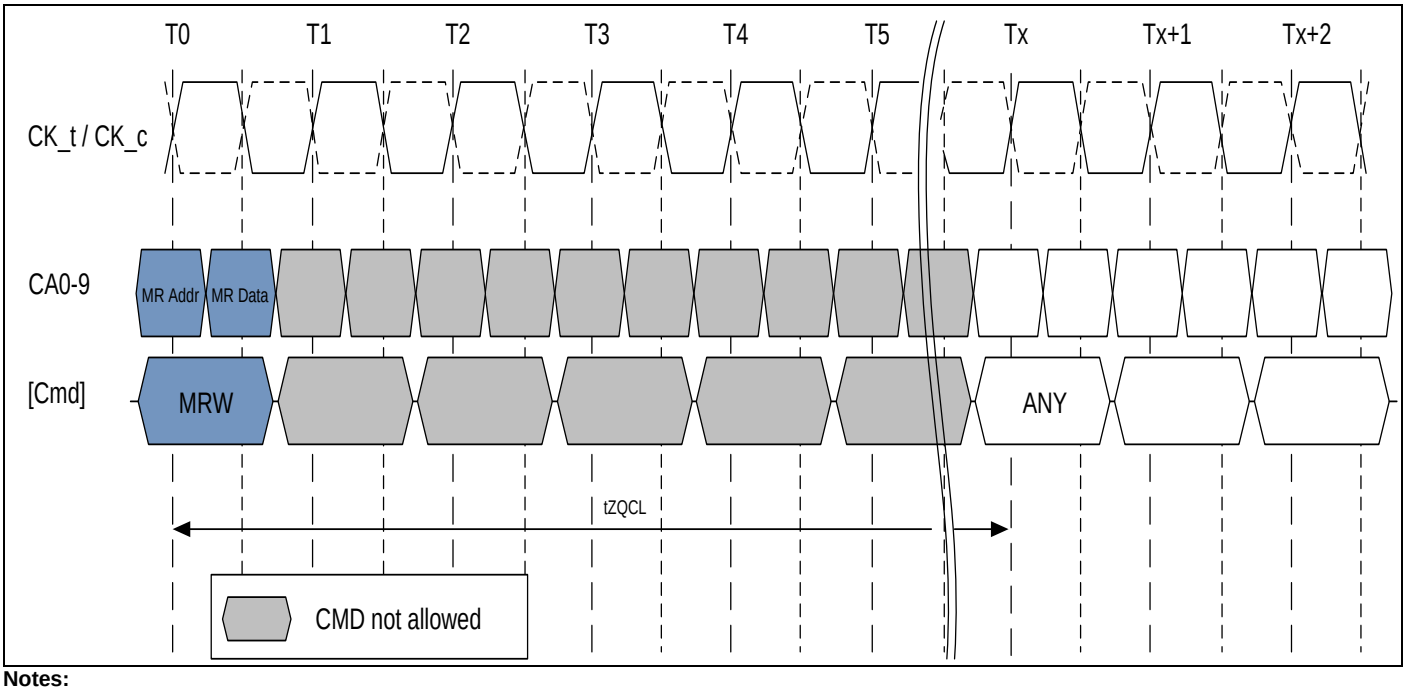



**Notes:**

1. The ZQ Calibration Short period is tZQCS. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.


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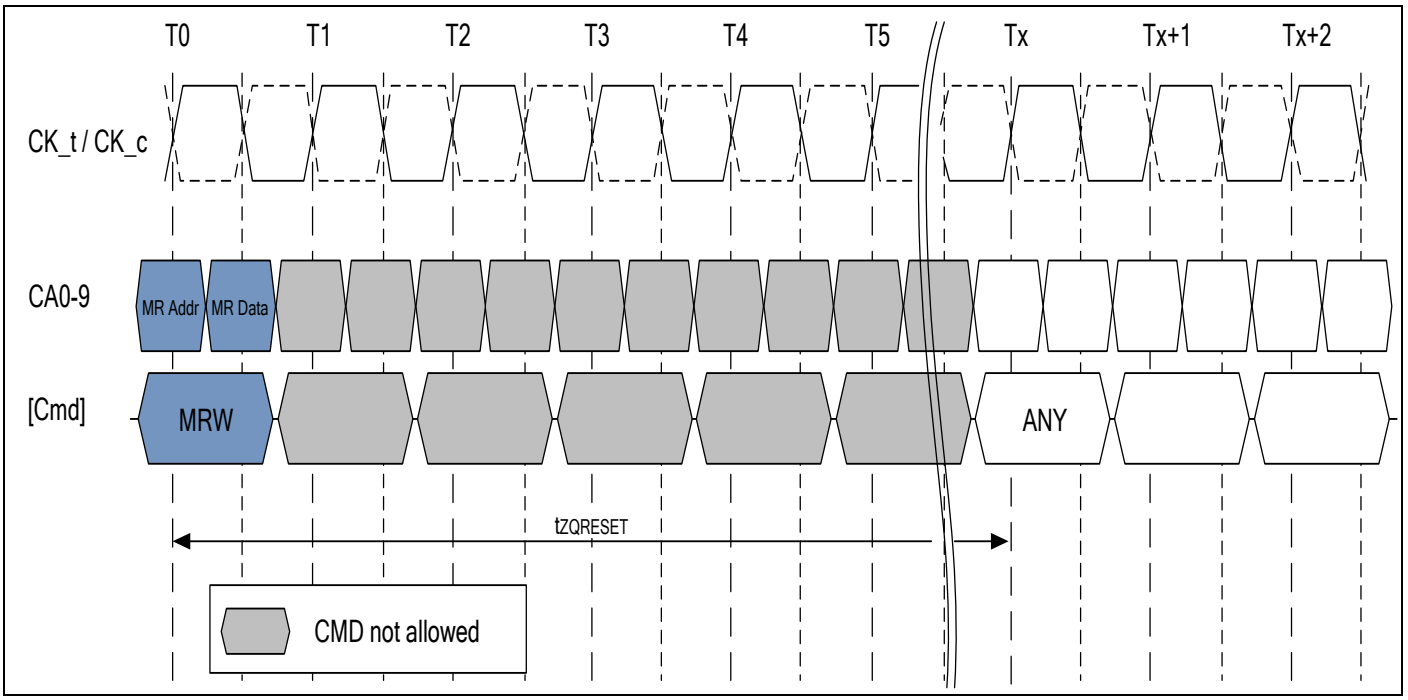
### 7.4.23.3 ZQ Calibration Long Timing Example




**Notes:**

1. The ZQ Calibration Long period is tZQCL. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

### 7.4.23.4 ZQ Calibration Reset Timing Example




**Notes:**

1. The ZQ Calibration Reset period is tZQRESET. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.


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#### 7.4.23.5 ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ Calibration function, a 240 Ohm ± 1% tolerance external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each LPDDR2 device or one resistor can be shared between multiple LPDDR2 devices if the ZQ calibration timings for each LPDDR2 device do not overlap. The total capacitive loading on the ZQ pin must be limited (See section 8.2.6.7 **"Input/Output Capacitance"** table).

### 7.4.24 Power-Down

For LPDDR2 SDRAM, power-down is synchronously entered when CKE is registered LOW and CS_n HIGH at the rising edge of clock. CKE must be registered HIGH in the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress. CKE is allowed to go LOW while any of other operations such as row activation, precharge, autoprecharge, or refresh is in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in the following pages with details for entry into power down.

For LPDDR2 SDRAM, if power-down occurs when all banks are idle, this mode is referred to as idle power- down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.

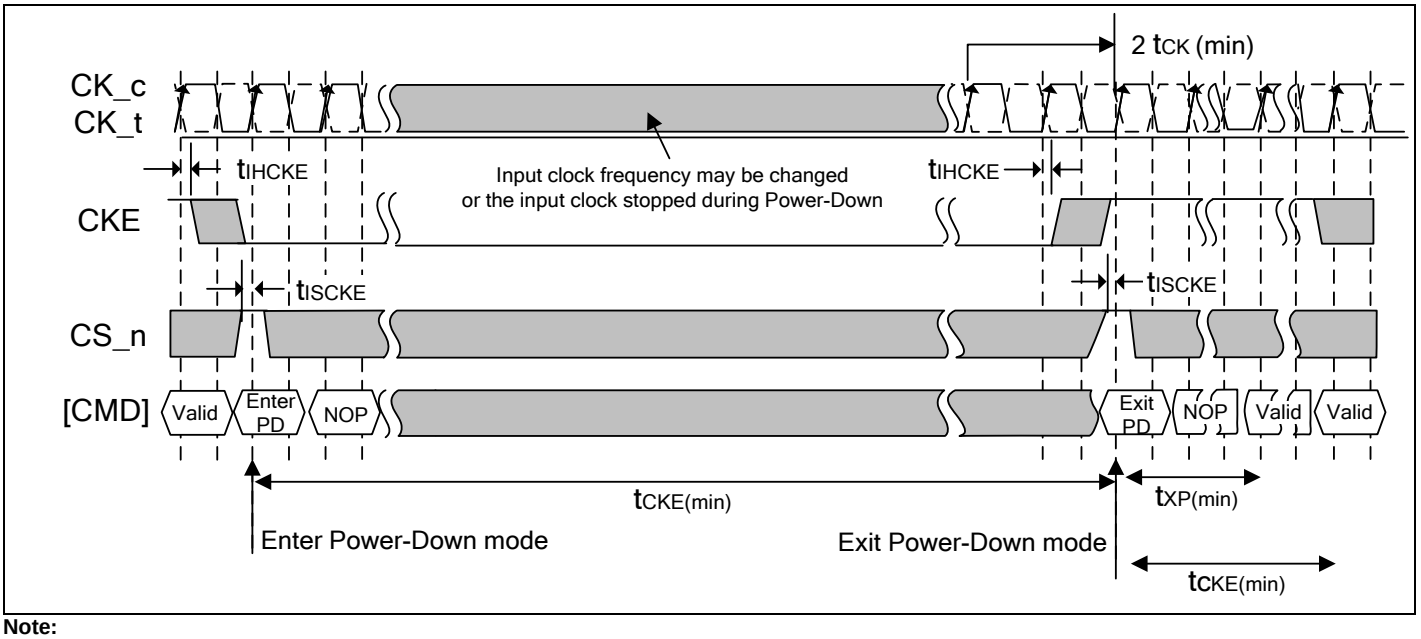
Entering power-down deactivates the input and output buffers, excluding CK_t, CK_c, and CKE. In power-down mode, CKE must be maintained LOW while all other input signals are "Don't Care". CKE LOW must be maintained until tCKE has been satisfied. VREF must be maintained at a valid level during power down.

VDDQ may be turned off during power down. If VDDQ is turned off, then VREFDQ must also be turned off. Prior to exiting power down, both VDDQ and VREFDQ must be within their respective min/max operating ranges (See 8.2.1.1 **"Recommended DC Operating Conditions"** table).

For LPDDR2 SDRAM, the maximum duration in power-down mode is only limited by the refresh requirements outlined in section 7.4.16 **"LPDDR2 SDRAM Refresh Requirements"**, as no refresh operations are performed in power-down mode.

The power-down state is exited when CKE is registered HIGH. The controller shall drive CS_n HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP after CKE goes HIGH. Power-down exit latency is defined in section 8.7.1 **"LPDDR2 AC Timing"** table.

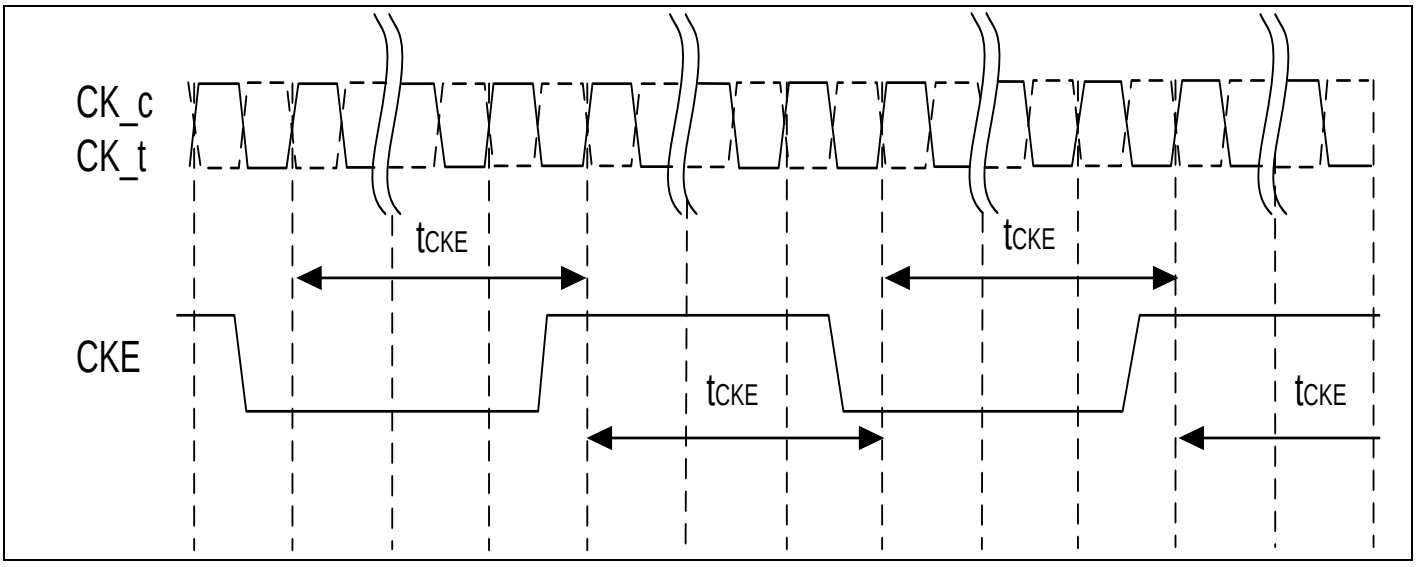
#### 7.4.24.1 Basic Power Down Entry and Exit Timing



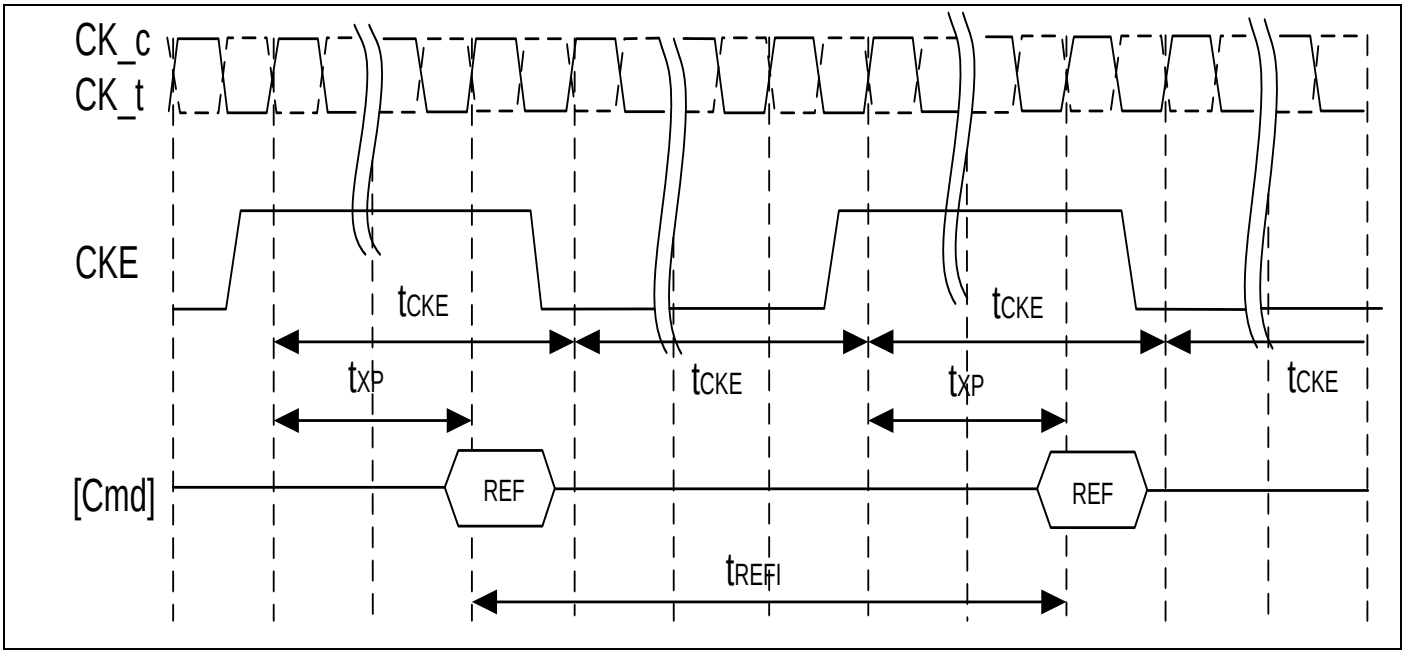

**Note:**

Input clock frequency may be changed or the input clock stopped during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

#### 7.4.24.2 CKE Intensive Environment



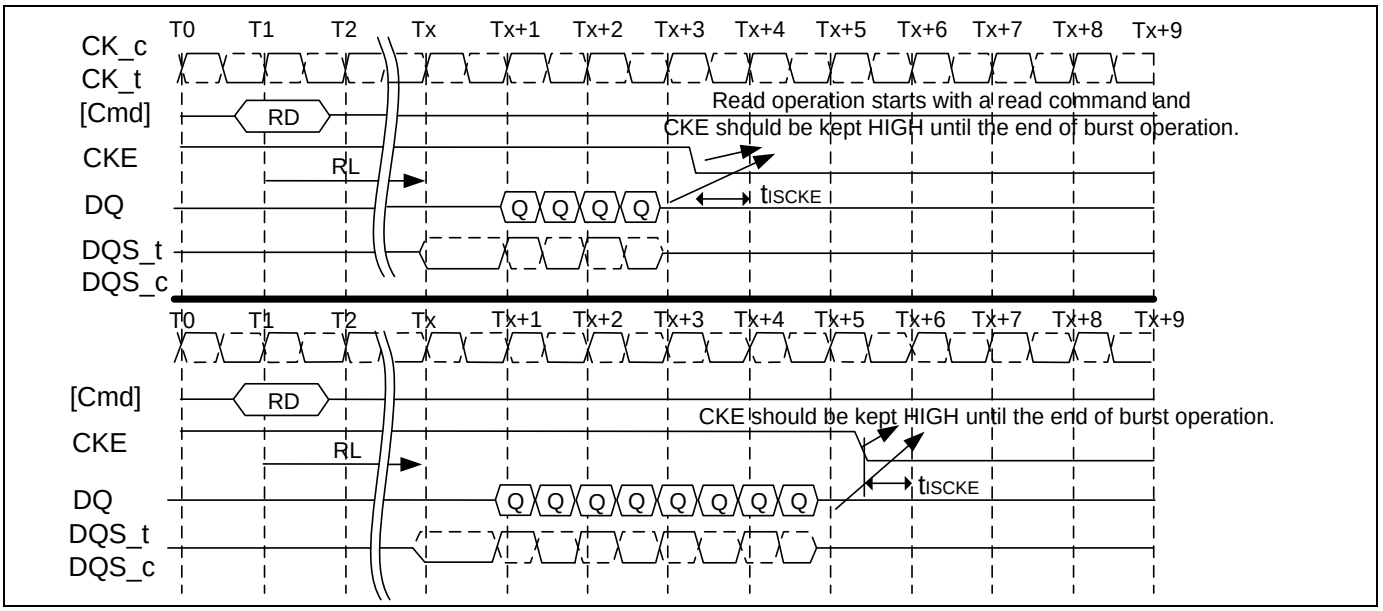

#### 7.4.24.3 Refresh to Refresh Timing with CKE Intensive Environment




**Note:**
The pattern shown above can repeat over a long period of time. With this pattern, LPDDR2 SDRAM guarantees all AC and DC timing & voltage specifications with temperature and voltage drift.

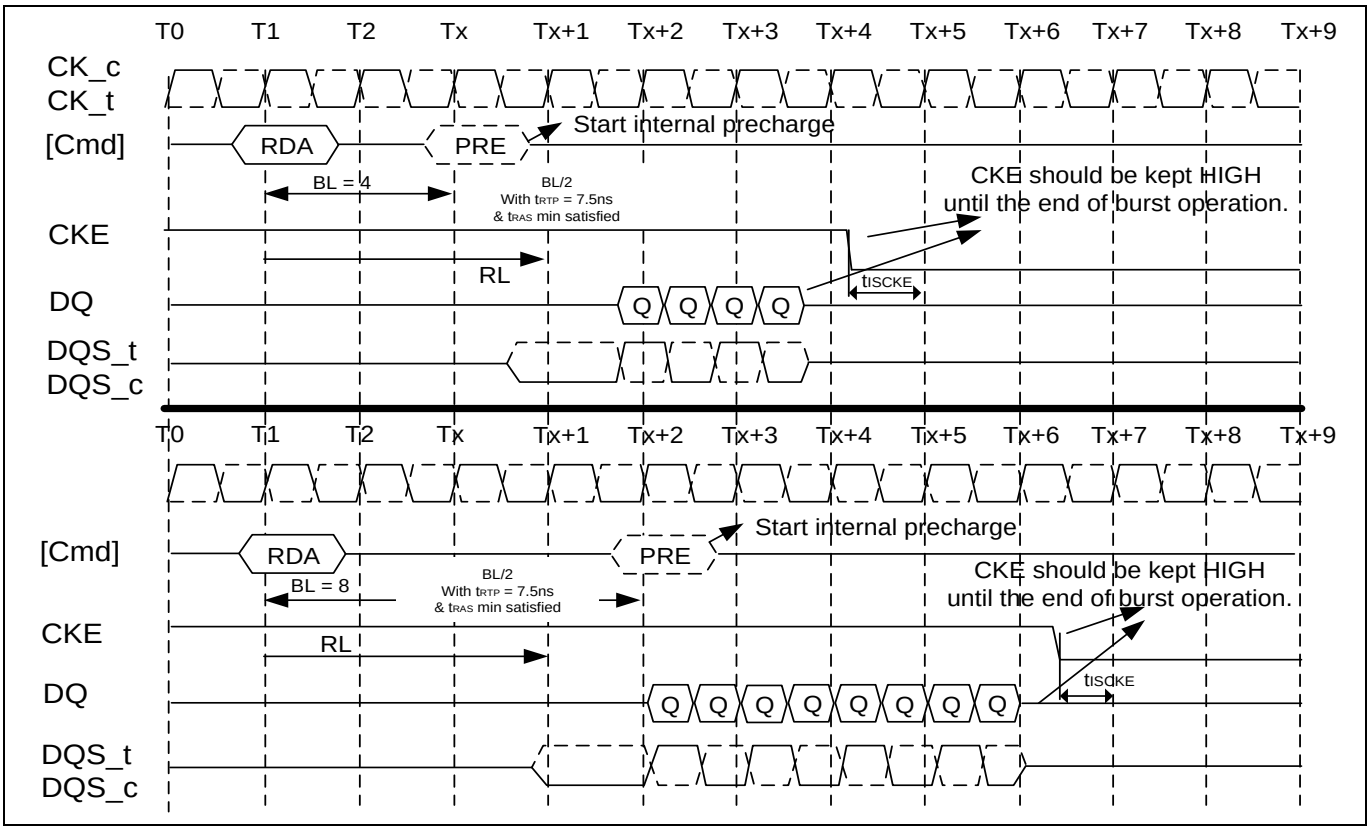

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### 7.4.24.4 Read to Power-Down Entry



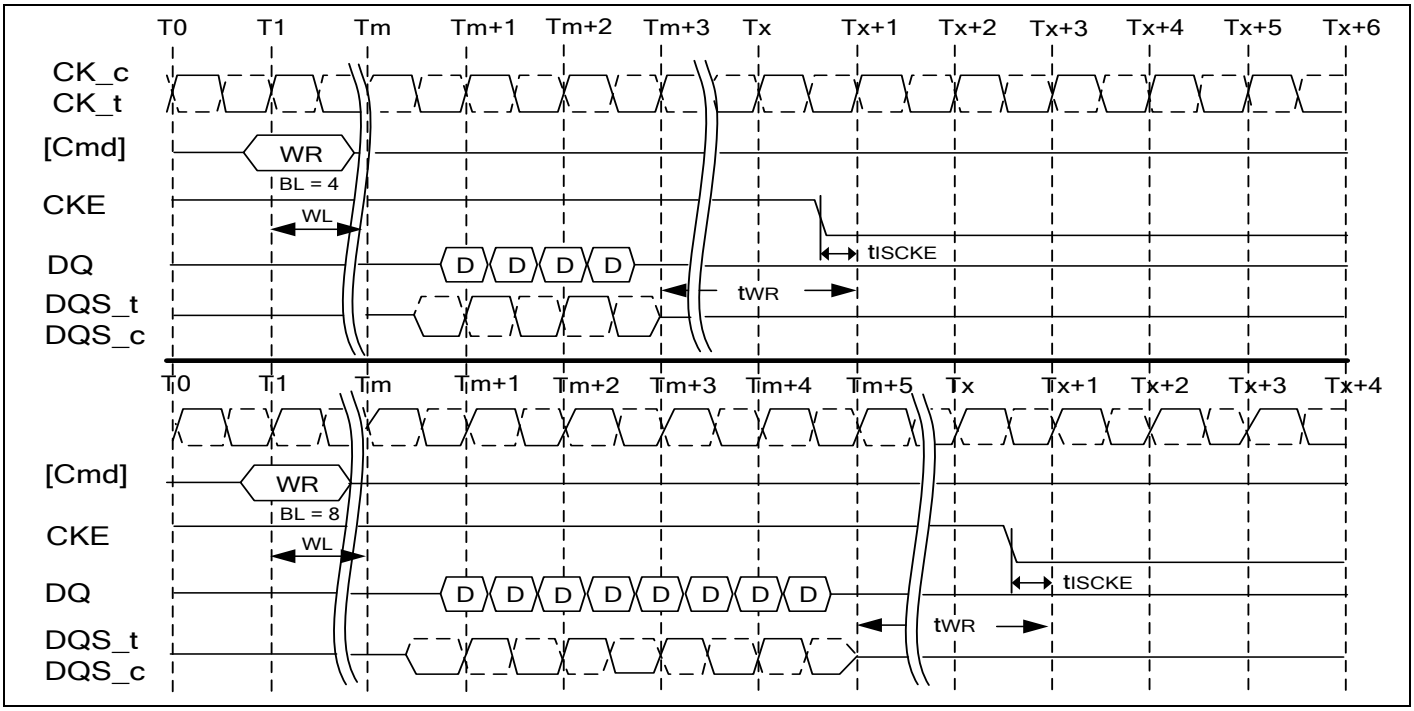

**Note:**
CKE may be registered LOW RL + RU(tDQSCK(MAX)/tCK)+ BL/2 + 1 clock cycles after the clock on which the Read command is registered.

### 7.4.24.5 Read with Auto Precharge to Power-Down Entry




**Note:**
CKE may be registered LOW RL + RU(tDQSCK(MAX)/tCK)+ BL/2 + 1 clock cycles after the clock on which the Read command is registered.

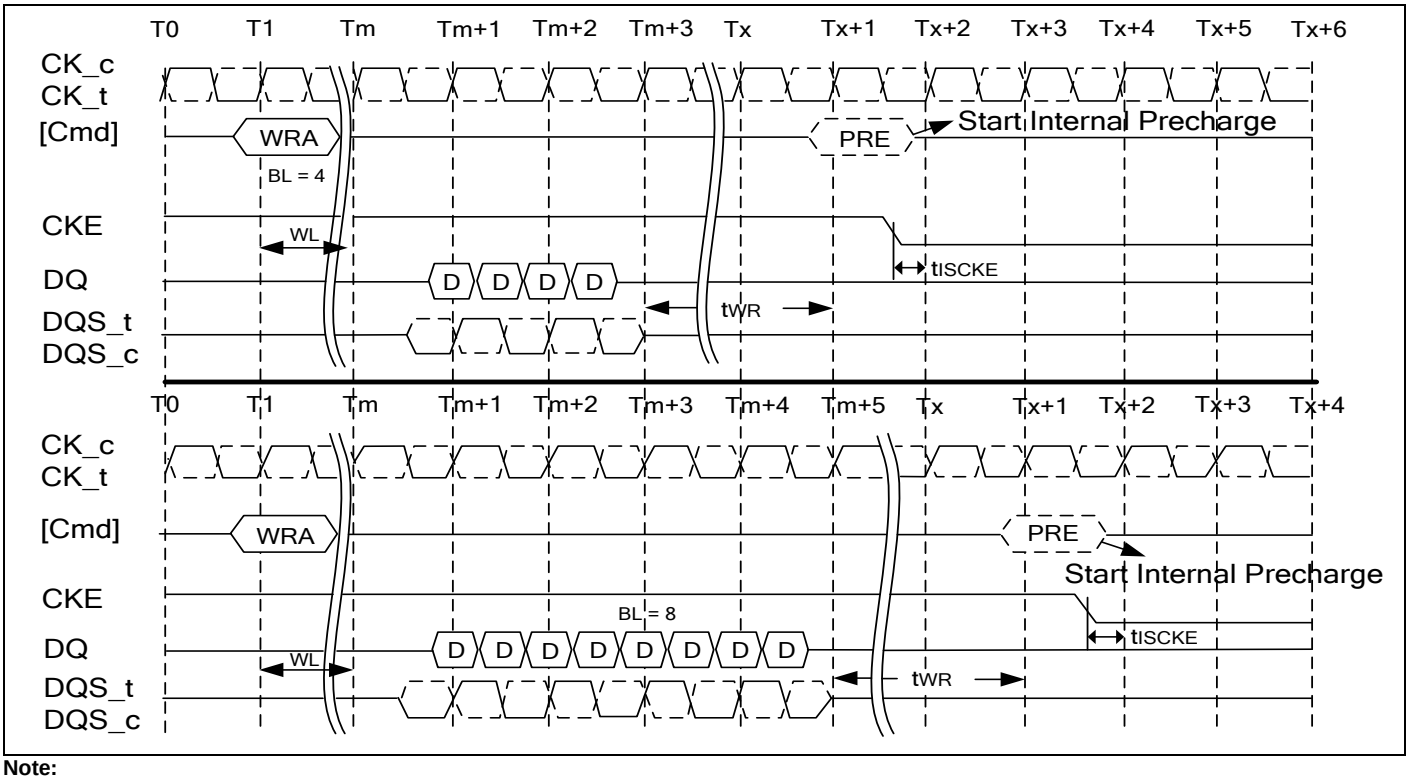
### 7.4.24.6 Write to Power-Down Entry




**Note:**

CKE may be registered LOW WL + 1 + BL/2 + RU(tWR/tCK) clock cycles after the clock on which the Write command is registered.

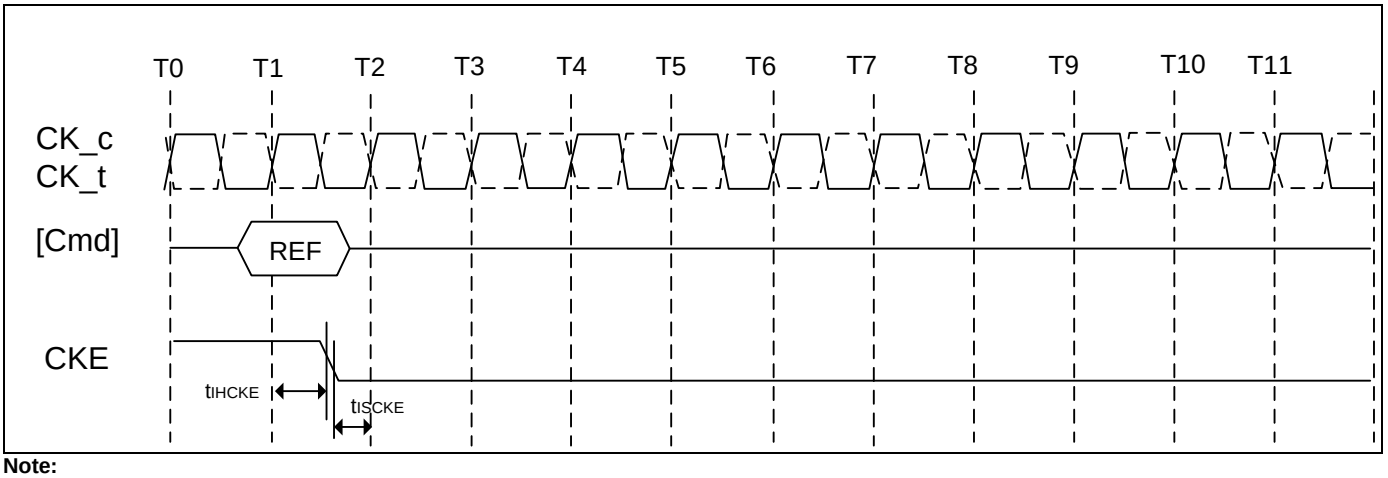
### 7.4.24.7 Write with Auto Precharge to Power-Down Entry




**Note:**

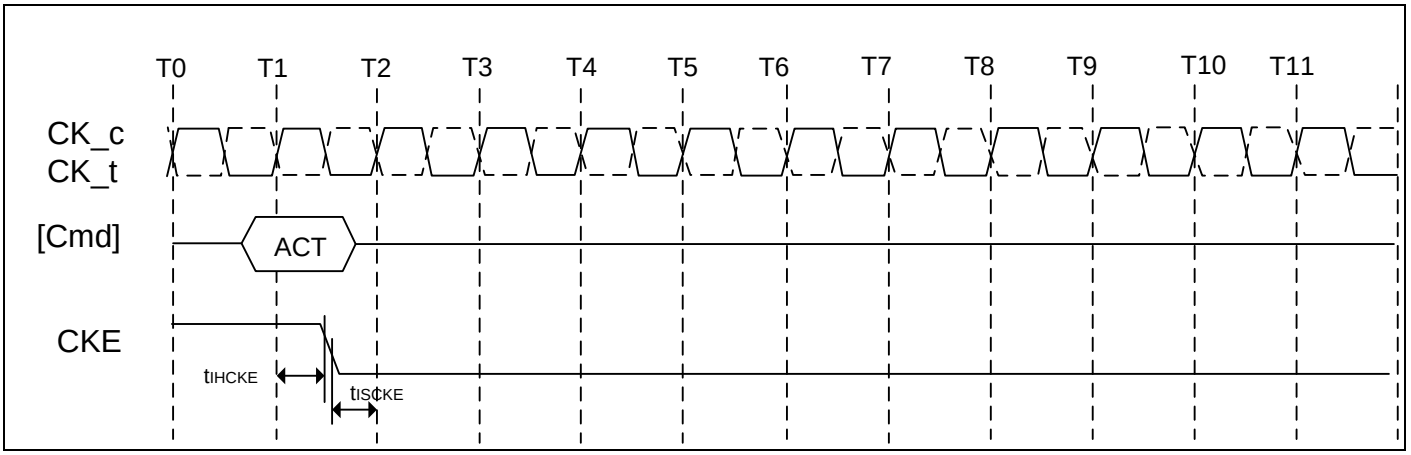
CKE may be registered LOW WL + 1 + BL/2 + RU(tWR/tCK) + 1 clock cycles after the Write command is registered.

### 7.4.24.8 Refresh Command to Power-Down Entry



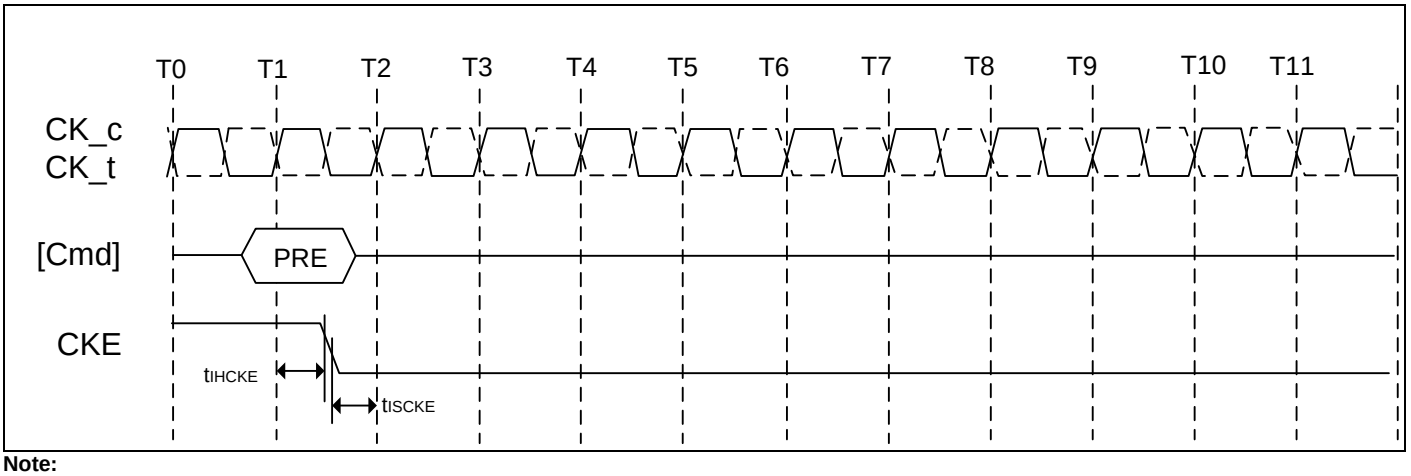

**Note:**
CKE may go LOW tIHCKE after the clock on which the Refresh command is registered.

### 7.4.24.9 Activate Command to Power-Down Entry




**Note:**
CKE may go LOW tIHCKE after the clock on which the Activate command is registered.

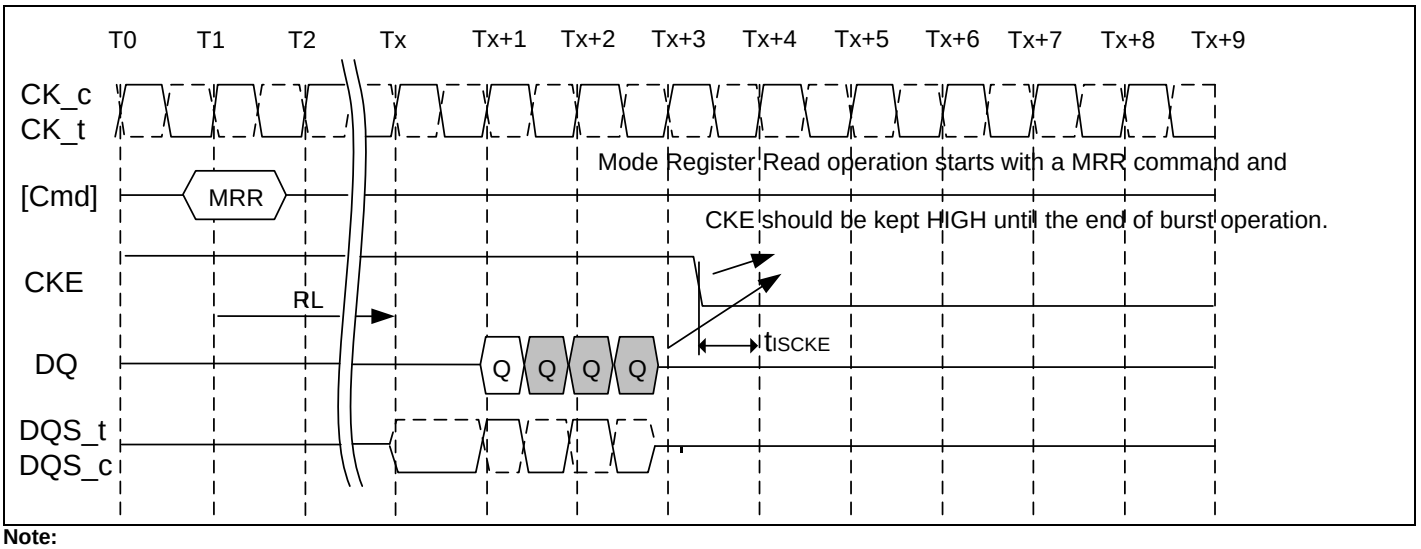
### 7.4.24.10 Precharge/Precharge-All Command to Power-Down Entry




**Note:**
CKE may go LOW tIHCKE after the clock on which the Precharge/Precharge-All command is registered.


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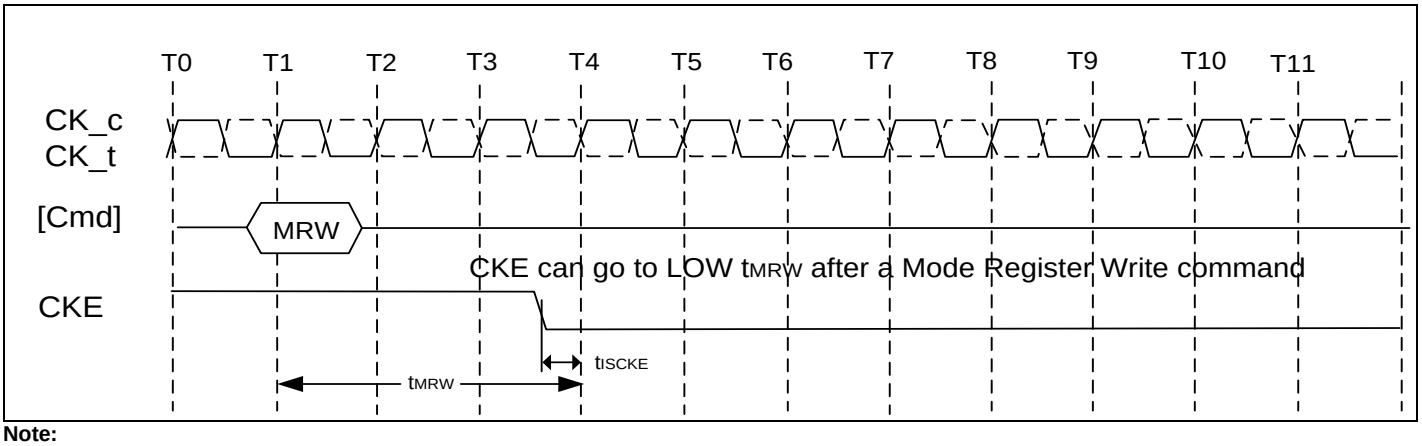
### 7.4.24.11 Mode Register Read to Power-Down Entry




**Note:**

CKE may be registered LOW RL + RU($t_{DQSCK(MAX)}/t_{CK}$)+ BL/2 + 1 clock cycles after the clock on which the Mode Register Read command is registered.

### 7.4.24.12 MRW Command to Power-Down Entry




**Note:**

CKE may be registered LOW $t_{MRW}$ after the clock on which the Mode Register Write command is registered.

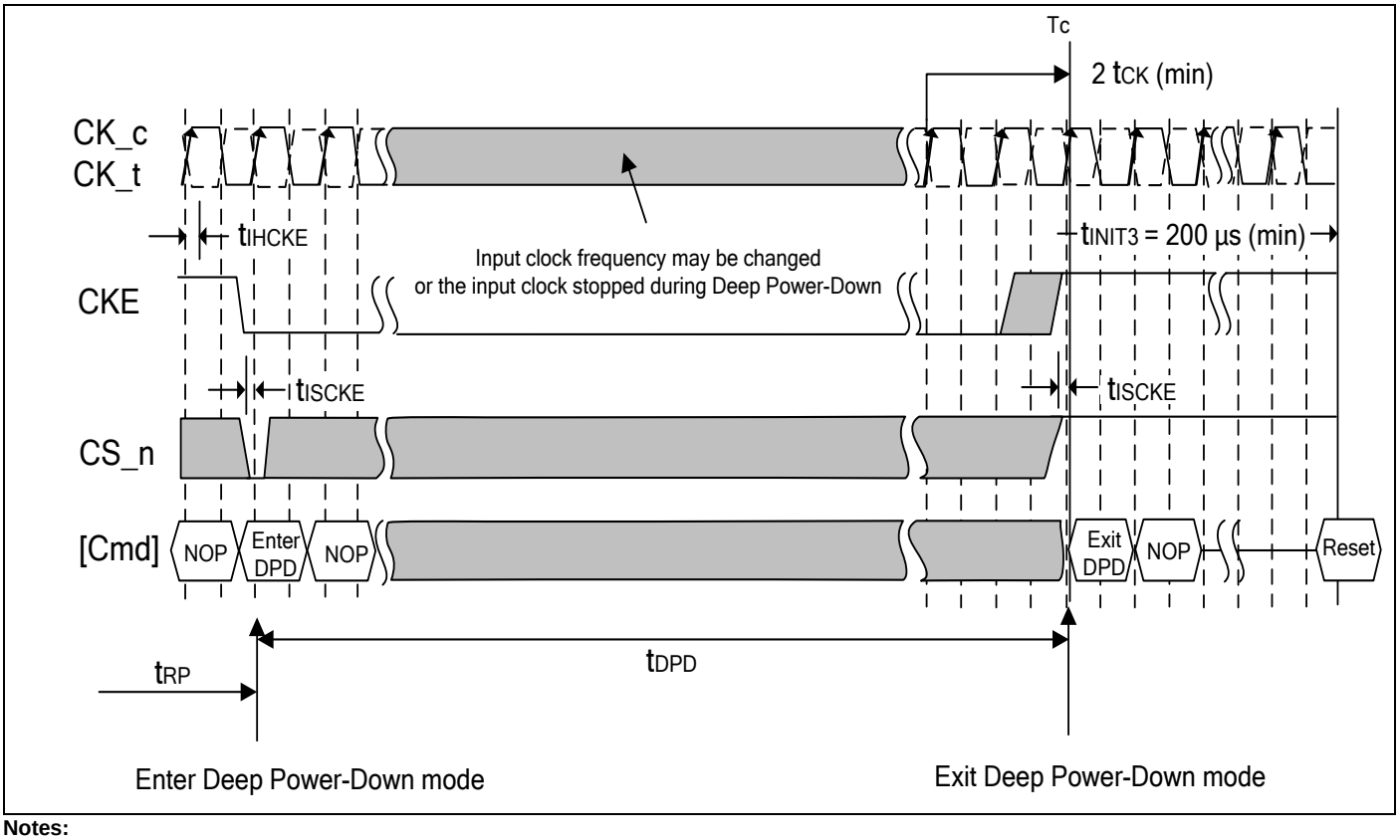
### 7.4.25 Deep Power-Down

Deep Power-Down is entered when CKE is registered LOW with CS_n LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of clock. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress. All banks must be in idle state with no activity on the data bus prior to entering the Deep Power Down mode. During Deep Power-Down, CKE must be held LOW.

In Deep Power-Down mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry may be disabled within the SDRAM. All power supplies must be within specified limits prior to exiting Deep Power-Down. $V_{REFDQ}$ and $V_{REFCA}$ may be at any level within minimum and maximum levels (See 8.1 **"Absolute Maximum DC Ratings"**). However prior to exiting Deep Power-Down, Vref must be within specified limits (See 8.2.1.1 **"Recommended DC Operating Conditions"**).

The contents of the SDRAM may be lost upon entry into Deep Power-Down mode.
The Deep Power-Down state is exited when CKE and CS_n are registered HIGH, while meeting $t_{ISCKE}$ with a stable clock input. The SDRAM must be fully re-initialized by controller as described in the Power up initialization Sequence. The SDRAM is ready for normal operation after the initialization sequence.

#### 7.4.25.1 Deep Power Down Entry and Exit Timing




**Notes:**

1. Initialization sequence may start at any time after $T_C$.
2. $t_{INIT3}$ and $T_C$ refer to timings in the LPDDR2 initialization sequence. For more detail, see section 7.2 **"Power-up, Initialization, and Power-Off"**.
3. Input clock frequency may be changed or the input clock stopped during deep power-down, provided that upon exiting deep power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to deep power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

### 7.4.26 Input Clock Stop and Frequency Change

LPDDR2 devices support input clock frequency change during CKE LOW under the following conditions:

- $t_{CK(abs)min}$ is met for each clock cycle;
- Refresh Requirements apply during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- Any Activate, or Precharge commands have executed to completion prior to changing the frequency;
- The related timing conditions ($t_{RCD}$, $t_{RP}$) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2 clock cycles prior to CKE going HIGH.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE LOW under the following conditions:
• CK_t is held LOW and CK_c is held HIGH during clock stop;
• Refresh Requirements apply during clock stop;
• During clock stop, only REFab commands may be executing;
• Any Activate, or Precharge commands have executed to completion prior to stopping the clock;
• The related timing conditions ($t_{RCD}$, $t_{RP}$) have been met prior to stopping the clock;
• The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
• The clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2 clock cycles prior to CKE going HIGH.

LPDDR2 devices support input clock frequency change during CKE HIGH under the following conditions:
• $t_{CK(abs)min}$ is met for each clock cycle;
• Refresh Requirements apply during clock frequency change;
• Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
• The related timing conditions ($t_{RCD}$, $t_{WR}$, $t_{WRA}$, $t_{RP}$, $t_{MRW}$, $t_{MRR}$, etc.) have been met prior to changing the frequency;
• CS_n shall be held HIGH during clock frequency change;
• During clock frequency change, only REFab commands may be executing;
• The LPDDR2 device is ready for normal operation after the clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of $2t_{CK} + t_{XP}$.
After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE HIGH under the following conditions:
• CK_t is held LOW and CK_c is held HIGH during clock stop;
• CS_n shall be held HIGH during clock stop;
• Refresh Requirements apply during clock stop;
• During clock stop, only REFab commands may be executing;
• Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock;
• The related timing conditions ($t_{RCD}$, $t_{WR}$, $t_{WRA}$, $t_{RP}$, $t_{MRW}$, $t_{MRR}$, etc.) have been met prior to stopping the clock;
• The LPDDR2 device is ready for normal operation after the clock is restarted and satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of $2t_{CK} + t_{XP}$.

### 7.4.27 No Operation Command

The purpose of the No Operation command (NOP) is to prevent the LPDDR2 device from registering any unwanted command between operations. Only when the CKE level is constant for clock cycle N-1 and clock cycle N, a NOP command may be issued at clock cycle N. A NOP command has two possible encodings:
1. CS_n HIGH at the clock rising edge N.
2. CS_n LOW and CA0, CA1, CA2 HIGH at the clock rising edge N.
The No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

## 7.5 Truth Tables

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the Banks.

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

### 7.5.1 Command Truth Table

| Command | Command Pins | | | DDR CA Pins (10) | | | | | | | | | | CK_t EDGE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | CKE | | CS_N | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | CA7 | CA8 | CA9 | |
| | CK_t(n-1) | CK_t(n) | | | | | | | | | | | | |
| MRW | H | H | L | L | L | L | L | MA0 | MA1 | MA2 | MA3 | MA4 | MA5 | ↑ |
| | | | X | MA6 | MA7 | OP0 | OP1 | OP2 | OP3 | OP4 | OP5 | OP6 | OP7 | ↓ |
| MRR | H | H | L | L | L | L | H | MA0 | MA1 | MA2 | MA3 | MA4 | MA5 | ↑ |
| | | | X | MA6 | MA7 | X | | | | | | | | ↓ |
| Refresh (all bank) | H | H | L | L | L | H | H | X | | | | | | ↑ |
| | | | X | X | | | | | | | | | | ↓ |
| Enter Self Refresh | H | L | L | L | L | H | X | | | | | | | ↑ |
| | X | | X | X | | | | | | | | | | ↓ |
| Activate (bank) | H | H | L | L | H | R8 | R9 | R10 | R11 | R12 | BA0 | BA1 | X | ↑ |
| | | | X | R0 | R1 | R2 | R3 | R4 | R5 | R6 | R7 | X | X | ↓ |
| Write (bank) | H | H | L | H | L | L | RFU | RFU | C1 | C2 | BA0 | BA1 | X | ↑ |
| | | | X | AP*[3,4] | C3 | C4 | C5 | C6 | C7 | C8 | X | X | X | ↓ |
| Read (bank) | H | H | L | H | L | H | RFU | RFU | C1 | C2 | BA0 | BA1 | X | ↑ |
| | | | X | AP*[3,4] | C3 | C4 | C5 | C6 | C7 | C8 | X | X | X | ↓ |
| Precharge (per bank, all bank) | H | H | L | H | H | L | H | AB*[12] | X | X | BA0 | BA1 | X | ↑ |
| | | | X | X | | | | | | | | | | ↓ |
| BST | H | H | L | H | H | L | L | X | | | | | | ↑ |
| | | | X | X | | | | | | | | | | ↓ |
| Enter Deep Power Down | H | L | L | H | H | L | X | | | | | | | ↑ |
| | X | | X | X | | | | | | | | | | ↓ |
| NOP | H | H | L | H | H | H | X | | | | | | | ↑ |
| | | | X | X | | | | | | | | | | ↓ |
| Maintain PD,SREF,DPD (NOP) | L | L | L | H | H | H | X | | | | | | | ↑ |
| | | | X | X | | | | | | | | | | ↓ |
| NOP | H | H | H | X | | | | | | | | | | ↑ |
| | | | X | X | | | | | | | | | | ↓ |
| Maintain PD,SREF,DPD (NOP) | L | L | H | X | | | | | | | | | | ↑ |
| | | | X | X | | | | | | | | | | ↓ |
| Enter Power Down | H | L | H | X | | | | | | | | | | ↑ |
| | X | | X | X | | | | | | | | | | ↓ |
| Exit PD, SREF,DPD | L | H | H | X | | | | | | | | | | ↑ |
| | X | | X | X | | | | | | | | | | ↓ |

**Notes:**
1. All LPDDR2 commands are defined by states of CS_n, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2. For LPDDR2 SDRAM, Bank addresses BA0 and BA1 (BA) determine which bank is to be operated upon.
3. AP is significant only to SDRAM.
4. AP "high" during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.
5. "X" means "H or L (but a defined logic level)".
6. Self refresh exit and Deep Power Down exit are asynchronous.
7. $V_{REF}$ must be between 0 and $V_{DDQ}$ during Self Refresh and Deep Power Down operation.
8. CAxr refers to command/address bit "x" on the rising edge of clock.
9. CAxf refers to command/address bit "x" on the falling edge of clock.
10. CS_n and CKE are sampled at the rising edge of clock.
11. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
12. AB "high" during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is do-not-care.

### 7.5.2 CKE Truth Table

| Device Current State*3 | CKEn-1*1 | CKEn*1 | CS_n*2 | Command n*4 | Operation n*4 | Device Next State | Notes |
|---|---|---|---|---|---|---|---|
| Active Power Down | L | L | X | X | Maintain Active Power Down | Active Power Down | |
| | L | H | H | NOP | Exit Active Power Down | Active | 6, 9 |
| Idle Power Down | L | L | X | X | Maintain Idle Power Down | Idle Power Down | |
| | L | H | H | NOP | Exit Idle Power Down | Idle | 6, 9 |
| Resetting Power Down | L | L | X | X | Maintain Resetting Power Down | Resetting Power Down | |
| | L | H | H | NOP | Exit Resetting Power Down | Idle or Resetting | 6, 9, 12 |
| Deep Power Down | L | L | X | X | Maintain Deep Power Down | Deep Power Down | |
| | L | H | H | NOP | Exit Deep Power Down | Power On | 8 |
| Self Refresh | L | L | X | X | Maintain Self Refresh | Self Refresh | |
| | L | H | H | NOP | Exit Self Refresh | Idle | 7, 10 |
| Bank(s) Active | H | L | H | NOP | Enter Active Power Down | Active Power Down | |
| All Banks Idle | H | L | H | NOP | Enter Idle Power Down | Idle Power Dow | |
| | H | L | L | Enter Self Refresh | Enter Self Refresh | Self Refresh | |
| | H | L | L | Deep Power Down | Enter Deep Power Down | Deep Power Down | |
| Resetting | H | L | H | NOP | Enter Resetting Power Down | Resetting Power Down | |
| Others states | H | H | Refer to the Command Truth Table | | | | |

**Notes:**
1. "CKEn" is the logic state of CKE at clock rising edge n; "CKEn-1" was the state of CKE at the previous clock edge.
2. "CS_n" is the logic state of CS_n at the clock rising edge n;
3. "Current state" is the state of the LPDDR2 device immediately prior to clock edge n.
4. "Command n" is the command registered at clock edge N, and "Operation n" is a result of "Command n".
5. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
6. Power Down exit time ($t_{XP}$) should elapse before a command other than NOP is issued.
7. Self-Refresh exit time ($t_{XSR}$) should elapse before a command other than NOP is issued.
8. The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
9. The clock must toggle at least once during the $t_{XP}$ period.
10. The clock must toggle at least once during the $t_{XSR}$ time.
11. X' means 'Don't care'.
12. Upon exiting Resetting Power Down, the device will return to the Idle state if $t_{INIT5}$ has expired.


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### 7.5.3 Current State Bank n - Command to Bank n Truth Table

| Current State | Command | Operation | Next State | Notes |
|---|---|---|---|---|
| Any | NOP | Continue previous operation | Current State | |
| Idle | ACTIVATE | Select and activate row | Active | |
| | Refresh (All Bank) | Begin to refresh | Refreshing (All Bank) | 6 |
| | MRW | Load value to Mode Register | MR Writing | 6 |
| | MRR | Read value from Mode Register | Idle MR Reading | |
| | Reset | Begin Device Auto-Initialization | Resetting | 6, 7 |
| | Precharge | Deactivate row in bank or banks | Precharging | 8, 14 |
| Row Active | Read | Select column, and start read burst | Reading | |
| | Write | Select column, and start write burst | Writing | |
| | MRR | Read value from Mode Register | Active MR Reading | |
| | Precharge | Deactivate row in bank or banks | Precharging | 8 |
| Reading | Read | Select column, and start new read burst | Reading | 9, 10 |
| | Write | Select column, and start write burst | Writing | 9, 10, 11 |
| | BST | Read burst terminate | Active | 12 |
| Writing | Write | Select column, and start new write burst | Writing | 9, 10 |
| | Read | Select column, and start read burst | Reading | 9, 10, 13 |
| | BST | Write burst terminate | Active | 12 |
| Power On | Reset | Begin Device Auto-Initialization | Resetting | 6, 8 |
| Resetting | MRR | Read value from Mode Register | Resetting MR Reading | |

**Notes:**

1. The table applies when both CKEn-1 and CKEn are HIGH, and after $t_{XSR}$ or $t_{XP}$ has been met if the previous state was Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State Definitions:

   Idle: The bank or banks have been precharged, and $t_{RP}$ has been met.

   Active: A row in the bank has been activated, and $t_{RCD}$ has been met. No data bursts / accesses and no register accesses are in progress.

   Reading: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

   Writing: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state and 7.5.3 **"Current State Bank n - Command to Bank n Truth Table"**, and according to 7.5.4 **"Current State Bank n - Command to Bank m Truth Table"**.

   Precharging: starts with the registration of a Precharge command and ends when $t_{RP}$ is met. Once $t_{RP}$ is met, the bank will be in the idle state.

   Row Activating: starts with registration of an Activate command and ends when $t_{RCD}$ is met. Once $t_{RCD}$ is met, the bank will be in the 'Active' state.

   Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when $t_{RP}$ has been met. Once $t_{RP}$ has been met, the bank will be in the idle state.

   Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when $t_{RP}$ has been met. Once $t_{RP}$ is met, the bank will be in the idle state.


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5. The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.

   Refreshing (All Bank): starts with registration of a Refresh (All Bank) command and ends when $t_{RFCab}$ is met. Once $t_{RFCab}$ is met, the device will be in an 'all banks idle' state.

   Idle MR Reading: starts with the registration of a MRR command and ends when $t_{MRR}$ has been met. Once $t_{MRR}$ has been met, the bank will be in the Idle state.

   Resetting MR Reading: starts with the registration of a MRR command and ends when $t_{MRR}$ has been met. Once $t_{MRR}$ has been met, the bank will be in the Resetting state.

   Active MR Reading: starts with the registration of a MRR command and ends when $t_{MRR}$ has been met. Once $t_{MRR}$ has been met, the bank will be in the Active state.

   MR Writing: starts with the registration of a MRW command and ends when $t_{MRW}$ has been met. Once $t_{MRW}$ has been met, the bank will be in the Idle state.

   Precharging All: starts with the registration of a Precharge-All command and ends when $t_{RP}$ is met. Once $t_{RP}$ is met, the bank will be in the idle state.
6. Not bank-specific; requires that all banks are idle and no bursts are in progress.
7. Not bank-specific reset command is achieved through Mode Register Write command.
8. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for pre- charging.
9. A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.
10. The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
11. A Write command may be applied after the completion of the Read burst; otherwise, a BST must be used to end the Read prior to asserting a Write command.
12. Not bank-specific. Burst Terminate (BST) command affects the most recent read/write burst started by the most recent Read/Write command, regardless of bank.
13. A Read command may be applied after the completion of the Write burst; otherwise, a BST must be used to end the Write prior to asserting a Read command.
14. If a Precharge command is issued to a bank in the Idle state, $t_{RP}$ shall still apply.


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### 7.5.4 Current State Bank n - Command to Bank m Truth Table

| Current State of Bank n | Command for Bank m | Operation | Next State for Bank m | Notes |
|---|---|---|---|---|
| Any | NOP | Continue previous operation | Current State of Bank m | |
| Idle | Any | Any command allowed to Bank m | - | 18 |
| Row Activating, Active, or Precharging | Activate | Select and activate row in Bank m | Active | 7 |
| | Read | Select column, and start read burst from Bank m | Reading | 8 |
| | Write | Select column, and start write burst to Bank m | Writing | 8 |
| | Precharge | Deactivate row in bank or banks | Precharging | 9 |
| | MRR | Read value from Mode Register | Idle MR Reading or Active MR Reading | 10, 11, 13 |
| | BST | Read or Write burst terminate an ongoing Read/Write from/to Bank m | Active | 18 |
| Reading (Autoprecharge disabled) | Read | Select column, and start read burst from Bank m | Reading | 8 |
| | Write | Select column, and start write burst to Bank m | Writing | 8, 14 |
| | Activate | Select and activate row in Bank m | Active | |
| | Precharge | Deactivate row in bank or banks | Precharging | 9 |
| Writing (Autoprecharge disabled) | Read | Select column, and start read burst from Bank m | Reading | 8, 16 |
| | Write | Select column, and start write burst to Bank m | Writing | 8 |
| | Activate | Select and activate row in Bank m | Active | |
| | Precharge | Deactivate row in bank or banks | Precharging | 9 |
| Reading with Autoprecharge | Read | Select column, and start read burst from Bank m | Reading | 8, 15 |
| | Write | Select column, and start write burst to Bank m | Writing | 8, 14, 15 |
| | Activate | Select and activate row in Bank m | Active | |
| | Precharge | Deactivate row in bank or banks | Precharging | 9 |
| Writing with Autoprecharge | Read | Select column, and start read burst from Bank m | Reading | 8, 15, 16 |
| | Write | Select column, and start write burst to Bank m | Writing | 8, 15 |
| | Activate | Select and activate row in Bank m | Active | |
| | Precharge | Deactivate row in bank or banks | Precharging | 9 |
| Power On | Reset | Begin Device Auto-Initialization | Resetting | 12, 17 |
| Resetting | MRR | Read value from Mode Register | Resetting MR Reading | |

**Notes:**

1. The table applies when both CKEn-1 and CKEn are HIGH, and after $t_{XSR}$ or $t_{XP}$ has been met if the previous state was Self Refresh or Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State Definitions:
   Idle: the bank has been precharged, and $t_{RP}$ has been met.
   Active: a row in the bank has been activated, and $t_{RCD}$ has been met. No data bursts/accesses and no register accesses are in progress.
   Reading: a Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Writing: a Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.


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4. Refresh, Self-Refresh, and Mode Register Write commands may only be issued when all bank are idle.
5. A Burst Terminate (BST) command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:

   Idle MR Reading: starts with the registration of a MRR command and ends when $t_{MRR}$ has been met. Once $t_{MRR}$ has been met, the bank will be in the Idle state.

   Resetting MR Reading: starts with the registration of a MRR command and ends when $t_{MRR}$ has been met. Once $t_{MRR}$ has been met, the bank will be in the Resetting state.

   Active MR Reading: starts with the registration of a MRR command and ends when $t_{MRR}$ has been met. Once $t_{MRR}$ has been met, the bank will be in the Active state.

   MR Writing: starts with the registration of a MRW command and ends when $t_{MRW}$ has been met. Once $t_{MRW}$ has been met, the bank will be in the Idle state.
7. $t_{RRD}$ must be met between Activate command to Bank n and a subsequent Activate command to Bank m.
8. Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.
9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for pre- charging.
10. MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when $t_{RCD}$ is met).
11. MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when $t_{RP}$ is met.
12. Not bank-specific; requires that all banks are idle and no bursts are in progress.
13. The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon $t_{RCD}$ and $t_{RP}$ respectively.
14. A Write command may be applied after the completion of the Read burst; otherwise a BST must be issued to end the Read prior to asserting a Write command.
15. Read with auto precharge enabled or a Write with auto precharge enabled may be followed by any valid command to other banks provided that the timing restrictions in 7.4.14.2 **"Precharge & Auto Precharge Clarification"** table are followed.
16. A Read command may be applied after the completion of the Write burst; otherwise, a BST must be issued to end the Write prior to asserting a Read command.
17. Reset command is achieved through Mode Register Write command.
18. BST is allowed only if a Read or Write burst is ongoing.

### 7.5.5 Data Mask Truth Table

| Name (Functional) | DM | DQs | Note |
|---|---|---|---|
| Write enable | L | Valid | 1 |
| Write inhibit | H | X | 1 |

**Note:**

1. Used to mask write data, provided coincident with the corresponding data.


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# 8. ELECTRICAL CHARACTERISTIC

## 8.1 Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $V_{DD1}$ supply voltage relative to $V_{SS}$ | $V_{DD1}$ | -0.4 | +2.3 | V | 2 |
| $V_{DD2}$ supply voltage relative to $V_{SS}$ | $V_{DD2}$ | -0.4 | +1.6 | V | 2 |
| $V_{DDCA}$ supply voltage relative to $V_{SSCA}$ | $V_{DDCA}$ | -0.4 | +1.6 | V | 2, 4 |
| $V_{DDQ}$ supply voltage relative to $V_{SSQ}$ | $V_{DDQ}$ | -0.4 | +1.6 | V | 2, 3 |
| Voltage on any ball relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | -0.4 | +1.6 | V | |
| Storage Temperature | $T_{STG}$ | -55 | +125 | °C | 5 |

**Notes:**

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. See “Power Ramp” in section 7.2.1 **“Power Ramp and Device Initialization”** for relationships between power supplies.
3. $V_{REFDQ} \leq 0.6 \times V_{DDQ}$; however, $V_{REFDQ}$ may be $\geq V_{DDQ}$ provided that $V_{REFDQ} \leq 300mV$.
4. $V_{REFCA} \leq 0.6 \times V_{DDCA}$; however, $V_{REFCA}$ may be $\geq V_{DDCA}$ provided that $V_{REFCA} \leq 300mV$.
5. Storage Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.

## 8.2 AC & DC Operating Conditions

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

### 8.2.1 Recommended DC Operating Conditions

#### 8.2.1.1 Recommended DC Operating Conditions

| Symbol | LPDDR2-S4B | | | DRAM | Unit |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| $V_{DD1}$ | 1.70 | 1.80 | 1.95 | Core Power1 | V |
| $V_{DD2}$ | 1.14 | 1.20 | 1.30 | Core Power2 | V |
| $V_{DDCA}$ | 1.14 | 1.20 | 1.30 | Input Buffer Power | V |
| $V_{DDQ}$ | 1.14 | 1.20 | 1.30 | I/O Buffer Power | V |

**Notes:**

1. $V_{DD1}$ uses significantly less power than $V_{DD2}$.
2. All parts list in section 3 order information table will not guarantee to meet functional and AC specification if the DC operation conditions out of range mentioned in above table.


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### 8.2.2 Input Leakage Current

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input Leakage current<br>For CA, CKE, CS_n, CK_t, CK_c<br>Any input 0V ≤ $V_{IN}$ ≤ $V_{DDCA}$<br>(All other pins not under test = 0V) | $I_L$ | -2 | 2 | µA | 2 |
| $V_{REF}$ supply leakage current<br>$V_{REFDQ}$ = $V_{DDQ}$/2 or $V_{REFCA}$ = $V_{DDCA}$/2<br>(All other pins not under test = 0V) | $I_{VREF}$ | -1 | 1 | µA | 1 |

**Notes:**

1. The minimum limit requirement is for testing purposes. The leakage current on $V_{REFCA}$ and $V_{REFDQ}$ pins should be minimal.
2. Although DM is for input only, the DM leakage shall match the DQ and DQS_t/DQS_c output leakage specification.

### 8.2.3 Operating Temperature Conditions

| Parameter/Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Standard | $T_{OPER}$ | -40 | 85 | °C |
| Extended | | 85 | 115 | °C |

**Notes:**

1. Operating Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.
2. Some applications require operation of LPDDR2 in the maximum temperature conditions in the Extended Temperature Range between 85°C and 115°C case temperature. For LPDDR2 devices, some derating is necessary to operate in this range. See the MR4 Device Temperature (MA[7:0] = 04h) table.
3. Either the device operating temperature or the temperature sensor (See section 7.4.20 **"Temperature Sensor"**) may be used to set an appropriate refresh rate, determine the need for AC timing derating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the $T_{OPER}$ rating that applies for the Standard or Extended Temperature Ranges. For example, $T_{CASE}$ may be above 85ºC when the temperature sensor indicates a temperature of less than 85°C.
4. All parts list in section 3 order information table will not guarantee to meet functional and AC specification if operating temperature out of the range in order information table.

### 8.2.4 AC and DC Input Measurement Levels

#### 8.2.4.1 AC and DC Logic Input Levels for Single-Ended Signals

##### 8.2.4.1.1 Single-Ended AC and DC Input Levels for CA and CS_n Inputs

| Symbol | Parameter | LPDDR2-800/1066 | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $V_{IHCA}$(AC) | AC input logic high | Vref + 0.220 | Note 2 | V | 1, 2 |
| $V_{ILCA}$(AC) | AC input logic low | Note 2 | Vref - 0.220 | V | 1, 2 |
| $V_{IHCA}$(DC) | DC input logic high | Vref + 0.130 | $V_{DDCA}$ | V | 1 |
| $V_{ILCA}$(DC) | DC input logic low | $V_{SSCA}$ | Vref - 0.130 | V | 1 |
| $V_{RefCA}$(DC) | Reference Voltage for CA and CS_n inputs | 0.49 * $V_{DDCA}$ | 0.51 * $V_{DDCA}$ | V | 3, 4 |

**Notes:**

1. For CA and CS_n input only pins. Vref = $V_{refCA(DC)}$.
2. See section 8.2.5.5 **"Overshoot and Undershoot Specifications"**.
3. The ac peak noise on $V_{RefCA}$ may not allow $V_{RefCA}$ to deviate from $V_{RefCA(DC)}$ by more than ± 1% $V_{DDCA}$ (for reference: approx. ± 12 mV).
4. For reference: approx. $V_{DDCA}$/2 ± 12 mV.


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#### 8.2.4.1.2 Single-Ended AC and DC Input Levels for CKE

| Symbol | Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| $V_{IHCKE}$ | CKE Input High Level | 0.8 * VDDCA | Note 1 | V | 1 |
| $V_{ILCKE}$ | CKE Input Low Level | Note 1 | 0.2 * VDDCA | V | 1 |
| **Note 1:** See section 8.2.5.5 **"Overshoot and Undershoot Specifications"**. | | | | | |

#### 8.2.4.1.3 Single-Ended AC and DC Input Levels for DQ and DM

| Symbol | Parameter | LPDDR2-1066/LPDDR2-800 | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $V_{IHDQ}$(AC) | AC input logic high | Vref + 0.220 | Note 2 | V | 1, 2 |
| $V_{ILDQ}$(AC) | AC input logic low | Note 2 | Vref - 0.220 | V | 1, 2 |
| $V_{IHDQ}$(DC) | DC input logic high | Vref + 0.130 | VDDQ | V | 1 |
| $V_{ILDQ}$(DC) | DC input logic low | VSSQ | Vref - 0.130 | V | 1 |
| $V_{RefDQ}$(DC) | Reference Voltage for DQ, DM inputs | 0.49 * VDDQ | 0.51 * VDDQ | V | 3, 4 |

**Notes:**

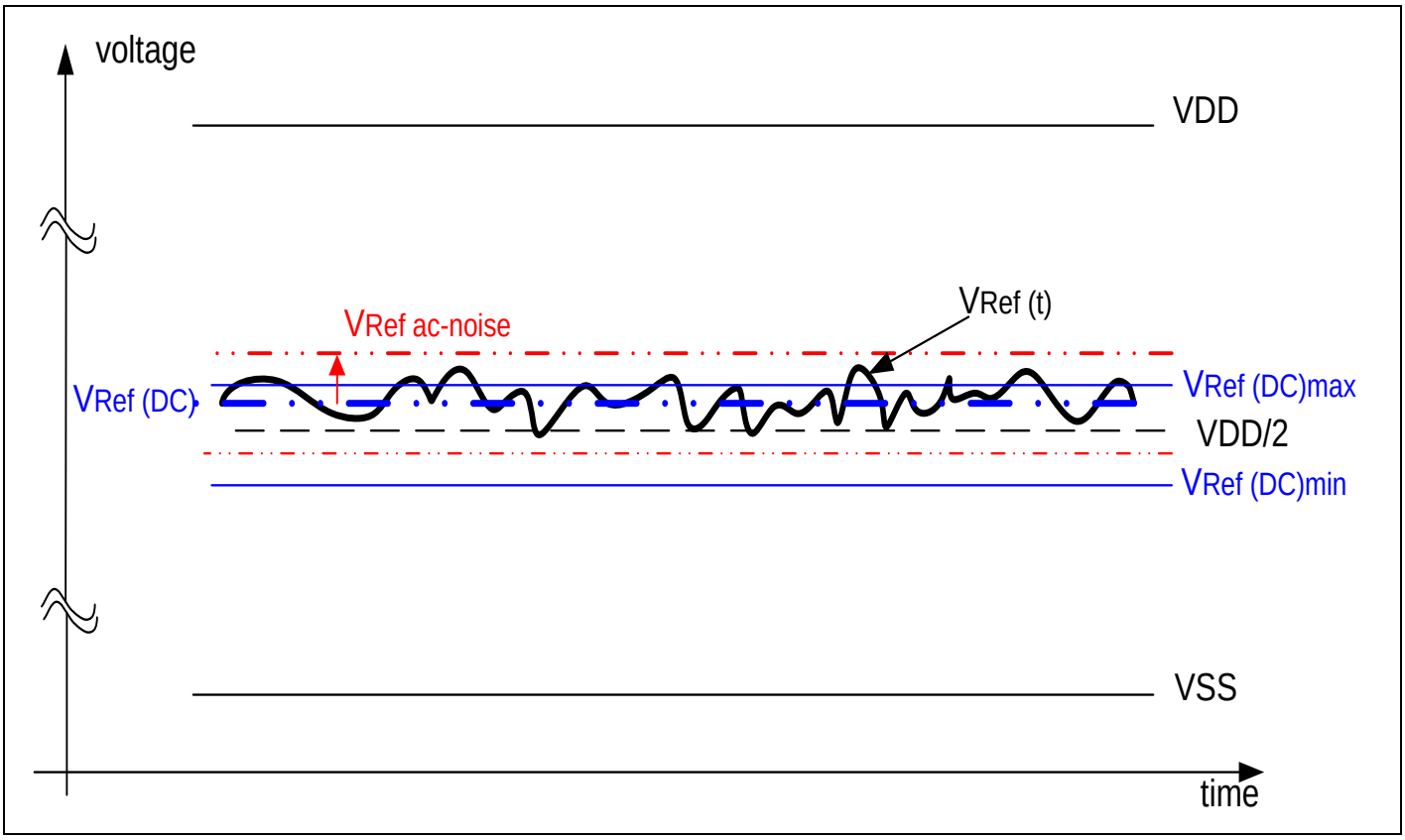
1. For DQ input only pins. Vref = $V_{refDQ}$(DC).
2. See section 8.2.5.5 **"Overshoot and Undershoot Specifications"**.
3. The ac peak noise on $V_{RefDQ}$ may not allow VRefDQ to deviate from $V_{RefDQ(DC)}$ by more than ± 1% VDDQ (for reference: approx. ±12 mV).
4. For reference: approx. VDDQ/2 ± 12 mV.

### 8.2.4.2 Vref Tolerances

The DC tolerance limits and ac-noise limits for the reference voltages VRefCA and VRefDQ are illustrated in below **"VRef(DC) Tolerance and VRef AC-Noise Limits"** figure. It shows a valid reference voltage VRef(t) as a function of time. (VRef stands for VRefCA and VRefDQ likewise). VDD stands for VDDCA for VRefCA and VDDQ for VRefDQ. VRef(DC) is the linear average of VRef(t) over a very long period of time (e.g. 1 sec) and is specified as a fraction of the linear average of VDDQ or VDDCA also over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in 8.2.4.1.1 **"Single-Ended AC and DC Input Levels for CA and CS_n Inputs"** table. Furthermore VRef(t) may temporarily deviate from VRef(DC) by no more than ± 1% VDD. Vref(t) cannot track noise on VDDQ or VDDCA if this would send Vref outside these specifications.


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#### 8.2.4.2.1 VRef(DC) Tolerance and VRef AC-Noise Limits




The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$ and $V_{IL(DC)}$ are dependent on $V_{Ref}$.

"$V_{Ref}$" shall be understood as $V_{Ref(DC)}$, as defined in above **"VRef(DC) Tolerance and VRef AC-Noise Limits"** figure.

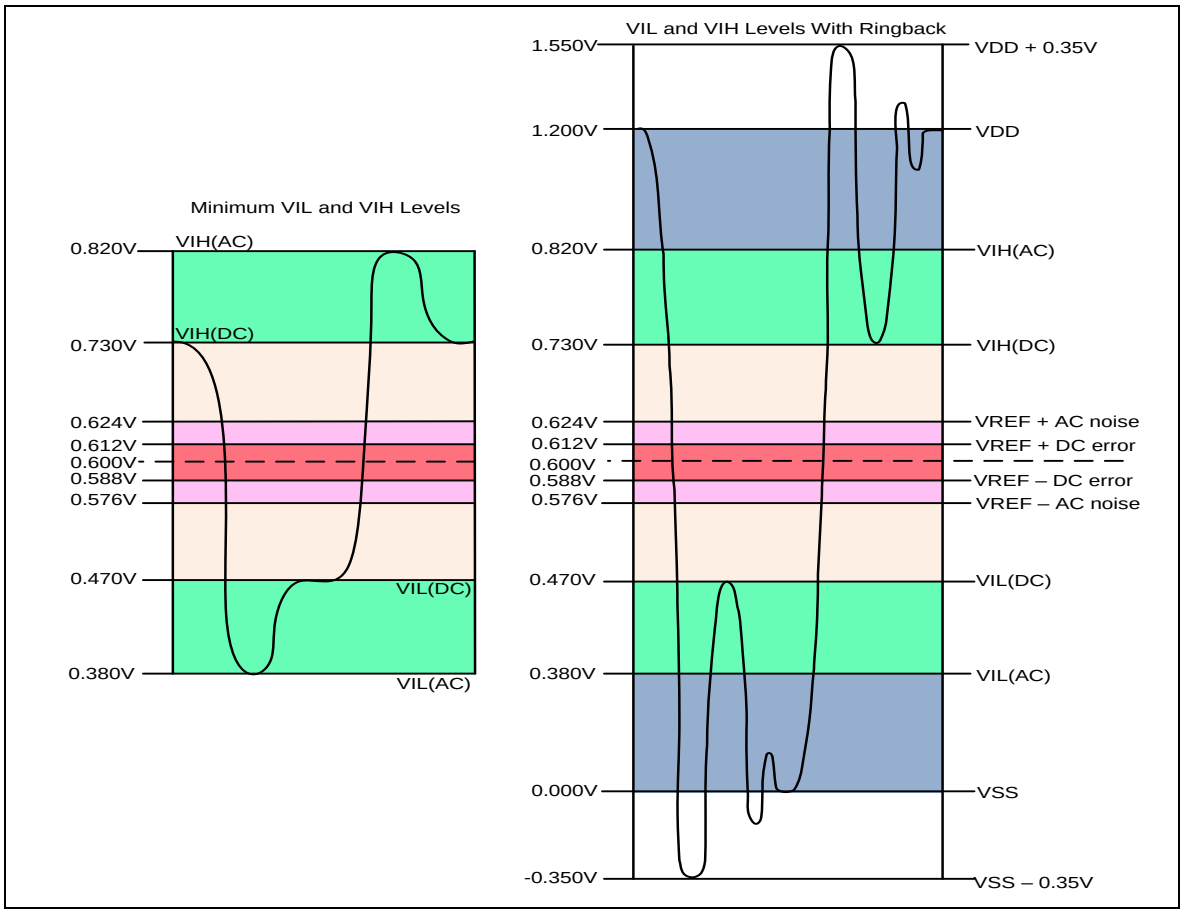
This clarifies that dc-variations of $V_{Ref}$ affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. Devices will function correctly with appropriate timing deratings with $V_{REF}$ outside these specified levels so long as $V_{REF}$ is maintained between 0.44 x $V_{DDQ}$ (or $V_{DDCA}$) and 0.56 x $V_{DDQ}$ (or $V_{DDCA}$) and so long as the controller achieves the required single-ended AC and DC input levels from instantaneous VRef (see 8.2.4.1.1 **"Single-Ended AC and DC Input Levels for CA and CS_n Inputs"** table and 8.2.4.1.3 **"Single-Ended AC and DC Input Levels for DQ and DM"** table) Therefore, system timing and voltage budgets need to account for $V_{REF}$ deviations outside of this range.

This also clarifies that the LPDDR2 setup/hold specification and derating values need to include time and voltage associated with $V_{Ref}$ ac-noise. Timing and voltage effects due to ac-noise on $V_{Ref}$ up to the specified limit (± 1% of $V_{DD}$) are included in LPDDR2 timings and their associated deratings.


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### 8.2.4.3 Input Signal

#### 8.2.4.3.1 LPDDR2-800/1066 Input Signal




**Notes:**

1. Numbers reflect nominal values.
2. For CA0-9, CK_t, CK_c, and CS_n, $V_{DD}$ stands for $V_{DDCA}$. For DQ, DM, DQS_t, and DQS_c, $V_{DD}$ stands for $V_{DDQ}$.
3. For CA0-9, CK_t, CK_c, and CS_n, $V_{SS}$ stands for $V_{SSCA}$. For DQ, DM, DQS_t, and DQS_c, $V_{SS}$ stands for $V_{SSQ}$.


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#### 8.2.4.4 AC and DC Logic Input Levels for Differential Signals

##### 8.2.4.4.1 Differential Signal Definition

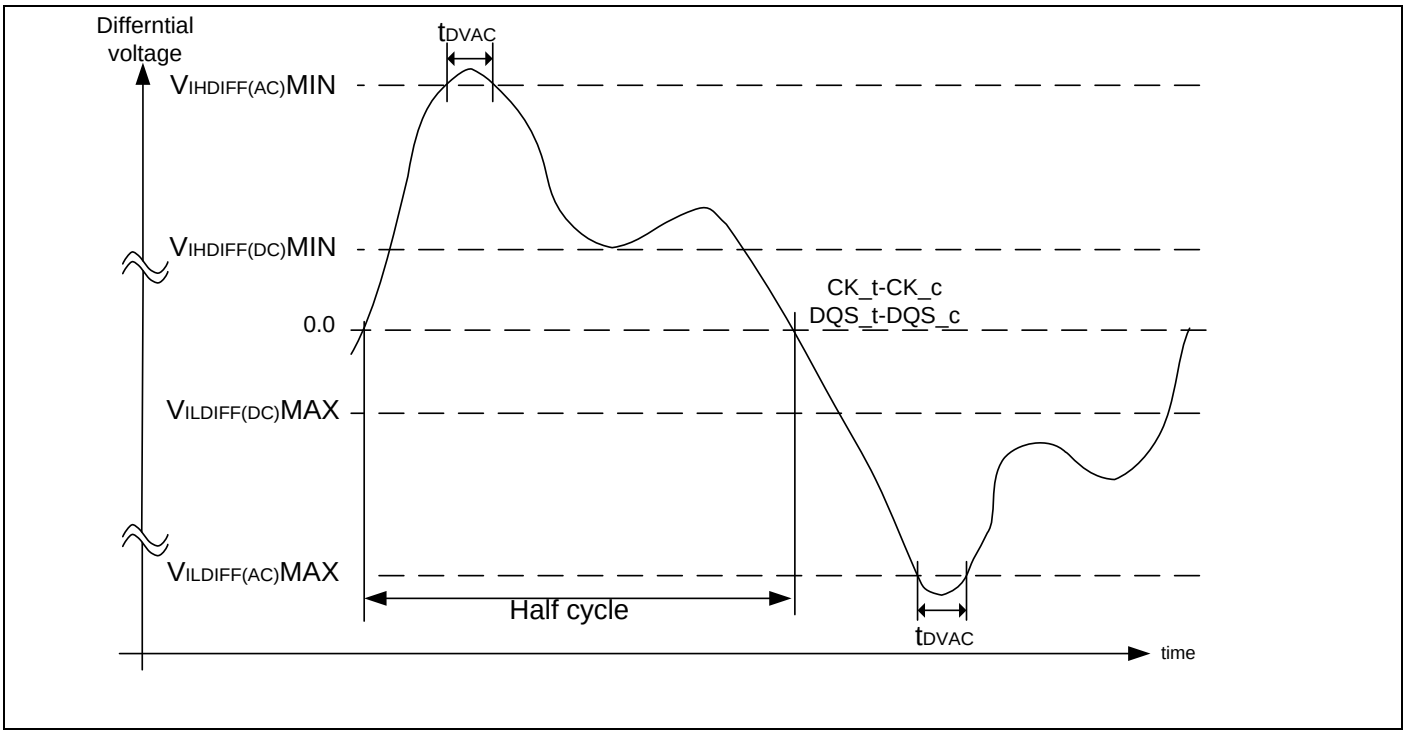



**Figure of Definition of Differential AC-Swing and "Time above AC-Level" $t_{DVAC}$**

##### 8.2.4.4.2 Differential swing requirements for clock (CK_t - CK_c) and strobe (DQS_t - DQS_c)

**Table of Differential AC and DC Input Levels**

| Symbol | Parameter | LPDDR2-800/1066 | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| VIHdiff(dc) | Differential input high | 2 x (VIH(dc) - Vref) | Note 3 | V | 1 |
| VILdiff(dc) | Differential input logic low | Note 3 | 2 x (VIL(dc) - Vref) | V | 1 |
| VIHdiff(ac) | Differential input high ac | 2 x (VIH(ac) - Vref) | Note 3 | V | 2 |
| VILdiff(ac) | Differential input low ac | Note 3 | 2 x (VIL(ac) - Vref) | V | 2 |

**Notes:**

1. Used to define a differential signal slew-rate. For CK_t - CK_c use VIH/VIL(dc) of CA and VREFCA; for DQS_t - DQS_c, use VIH/VIL(dc) of DQs and VREFDQ; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.
2. For CK_t - CK_c use VIH/VIL(ac) of CA and VREFCA; for DQS_t - DQS_c, use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK_t, CK_c, DQS_t, and DQS_c need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.2.5.5 **"Overshoot and Undershoot Specifications"**.
4. For CK_t and CK_c, Vref = VrefCA(DC). For DQS_t and DQS_c, Vref = VrefDQ(DC).


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**Table of Allowed Time before Ringback ($t_{DVAC}$) for CK_t - CK_c and DQS_t - DQS_c**

| Slew Rate [V/nS] | $t_{DVAC}$ [pS] @ $\|V_{IHdiff(ac)}$ or $V_{ILdiff(ac)}\|$ = 440mV |
|---|---|
| > 4.0 | 175 |
| 4.0 | 170 |
| 3.0 | 167 |
| 2.0 | 163 |
| 1.8 | 162 |
| 1.6 | 161 |
| 1.4 | 159 |
| 1.2 | 155 |
| 1.0 | 150 |
| < 1.0 | 150 |

#### 8.2.4.5 Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (CK_t, DQS_t, CK_c, or DQS_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c shall meet $V_{SEH}$(ac)min / $V_{SEL}$(ac)max in every half-cycle.

DQS_t, DQS_c shall meet $V_{SEH}$(ac)min / $V_{SEL}$(ac)max in every half-cycle preceding and following a valid transition.

Note that the applicable ac-levels for CA and DQ's are different per speed-bin.

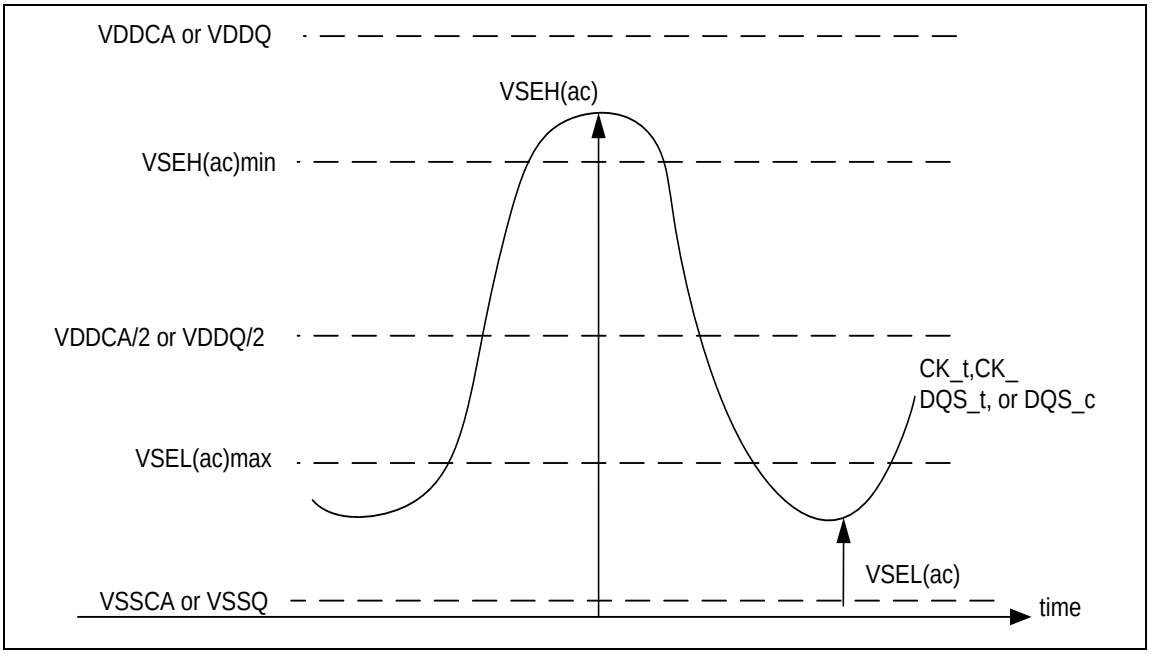



**Figure of Single-Ended Requirement for Differential Signals**


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Note that while CA and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to $V_{DDQ}/2$ for DQS_t, DQS_c and $V_{DDCA}/2$ for CK_t, CK_c; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach $V_{SEL}$(ac)max, $V_{SEH}$(ac)min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

The signal ended requirements for CK_t, CK_c, DQS_t and DQS_c are found in 8.2.4.1.1 **"Single-Ended AC and DC Input Levels for CA and CS_n Inputs"** table and 8.2.4.1.3 **"Single-Ended AC and DC Input Levels for DQ and DM"** table, respectively.

**Table of Single-Ended Levels for CK_t, DQS_t, CK_c, DQS_c**

| Symbol | Parameter | LPDDR2-800/1066 | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $V_{SEH(AC)}$ | Single-ended high-level for strobes | ($V_{DDQ}/2$) + 0.220 | Note 3 | V | 1, 2 |
| | Single-ended high-level for CK_t, CK_c | ($V_{DDCA}/2$) + 0.220 | Note 3 | V | 1, 2 |
| $V_{SEL(AC)}$ | Single-ended low-level for strobes | Note 3 | ($V_{DDQ}/2$) - 0.220 | V | 1, 2 |
| | Single-ended low-level for CK_t, CK_c | Note 3 | ($V_{DDCA}/2$) - 0.220 | V | 1, 2 |

**Notes:**

1. For CK_t, CK_c use $V_{SEH}/V_{SEL}$(ac) of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use $V_{IH}/V_{IL}$(ac) of DQs.
2. $V_{IH}$(ac)/$V_{IL}$(ac) for DQs is based on $V_{REFDQ}$; $V_{SEH}$(ac)/$V_{SEL}$(ac) for CA is based on $V_{REFCA}$; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits ($V_{IH}$(dc) max, $V_{IL}$(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 8.2.5.5 **"Overshoot and Undershoot Specifications"**.

### 8.2.4.6 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK_t, CK_c and DQS_t, DQS_c) must meet the requirements of above Single-ended levels for CK_t, DQS_t, CK_c, DQS_c table. The differential input cross point voltage $V_{IX}$ is measured from the actual cross point of true and complement signals to the midlevel between of $V_{DD}$ and $V_{SS}$.

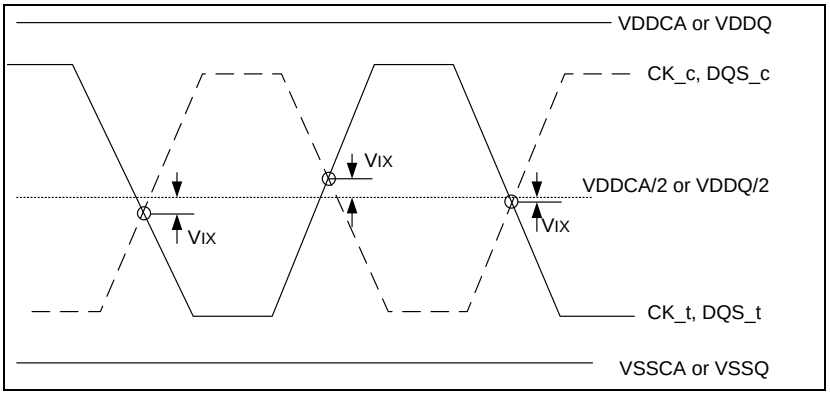



**Figure of Vix Definition**


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**Table of Cross Point Voltage for Differential Input Signals (CK, DQS)**

| Symbol | Parameter | LPDDR2-800/1066 | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $V_{IXCA}$ | Differential Input Cross Point Voltage relative to $V_{DDCA}/2$ for CK_t, CK_c | - 120 | 120 | mV | 1, 2 |
| $V_{IXDQ}$ | Differential Input Cross Point Voltage relative to $V_{DDQ}/2$ for DQS_t, DQS_c | - 120 | 120 | mV | 1, 2 |

**Notes:**

1. The typical value of $V_{IX(AC)}$ is expected to be about 0.5 × $V_{DD}$ of the transmitting device, and $V_{IX(AC)}$ is expected to track variations in $V_{DD}$. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.
2. For CK_t and CK_c, $V_{ref}$ = $V_{refCA(DC)}$. For DQS_t and DQS_c, $V_{ref}$ = $V_{refDQ(DC)}$.

### 8.2.4.7 Slew Rate Definitions for Single-Ended Input Signals

See section 8.7.2 **"CA and CS_n Setup, Hold and Derating"** for single-ended slew rate definitions for address and command signals.

See section 8.7.3 **"Data Setup, Hold and Slew Rate Derating"** for single-ended slew rate definitions for data signals.

### 8.2.4.8 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK_t, CK_c and DQS_t, DQS_c) are defined and measured as shown in below table and figure.

**Table of Differential Input Slew Rate Definition**

| Description | Measured | | Defined by |
|---|---|---|---|
| | from | to | |
| Differential input slew rate for rising edge (CK_t - CK_c and DQS_t - DQS_c). | $V_{ILdiffmax}$ | $V_{IHdiffmin}$ | [$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTRdiff |
| Differential input slew rate for falling edge (CK_t - CK_c and DQS_t - DQS_c). | $V_{IHdiffmin}$ | $V_{ILdiffmax}$ | [$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTFdiff |
| **Note:** The differential signal (i.e. CK_t - CK_c and DQS_t - DQS_c) must be linear between these thresholds. | | | |

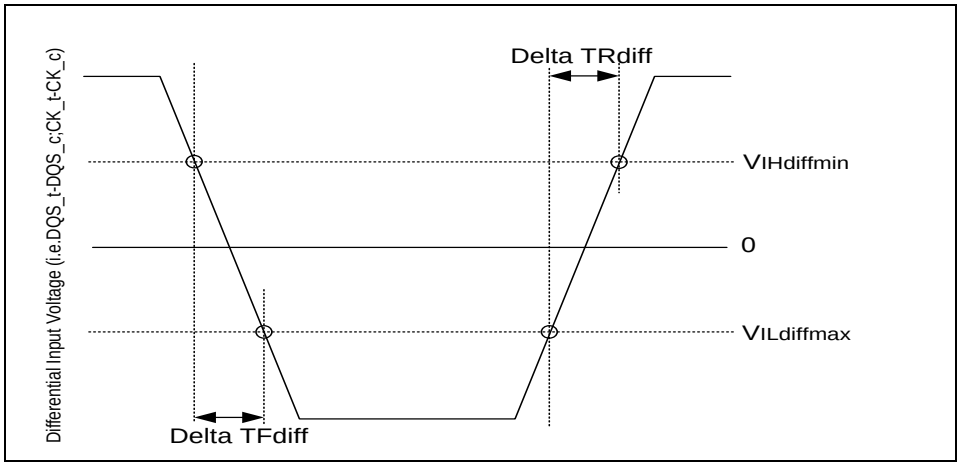



**Figure of Differential Input Slew Rate Definition for DQS_t, DQS_c and CK_t, CK_c**


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### 8.2.5 AC and DC Output Measurement Levels

#### 8.2.5.1 Single Ended AC and DC Output Levels

**Table of Single-Ended AC and DC Output Levels**

| Symbol | Parameter | LPDDR2-800/1066 | | Unit | Notes |
|---|---|---|---|---|---|
| $V_{OH(DC)}$ | DC output high measurement level (for IV curve linearity) | 0.9 x $V_{DDQ}$ | | V | 1 |
| $V_{OL(DC)}$ | DC output low measurement level (for IV curve linearity) | 0.1 x $V_{DDQ}$ | | V | 2 |
| $V_{OH(AC)}$ | AC output high measurement level (for output slew rate) | $V_{REFDQ}$ + 0.12 | | V | |
| $V_{OL(AC)}$ | AC output low measurement level (for output slew rate) | $V_{REFDQ}$ - 0.12 | | V | |
| $I_{OZ}$ | Output Leakage current (DQ, DM, DQS_t, DQS_c) (DQ, DQS_t, DQS_c are disabled;0V ≤ Vout ≤ VDDQ) | Min | -5 | µA | |
| | | Max | +5 | | |
| $MM_{PUPD}$ | Delta RON between pull-up and pull-down for DQ/DM | Min | -15 | % | |
| | | Max | +15 | | |

**Notes:**

1. $I_{OH}$ = -0.1mA.
2. $I_{OL}$ = +0.1mA.

#### 8.2.5.2 Differential AC and DC Output Levels

**Table of Differential AC and DC Output Levels of (DQS_t, DQS_c)**

| Symbol | Parameter | LPDDR2-800/1066 | Unit | Notes |
|---|---|---|---|---|
| $V_{OHdiff(AC)}$ | AC differential output high measurement level (for output SR) | + 0.20 x $V_{DDQ}$ | V | |
| $V_{OLdiff(AC)}$ | AC differential output low measurement level (for output SR) | - 0.20 x $V_{DDQ}$ | V | |

**Notes:**

1. $I_{OH}$ = -0.1mA.
2. $I_{OL}$ = +0.1mA.

#### 8.2.5.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in below table and figure.

**Table of Single-Ended Output Slew Rate Definition**

| Description | Measured | | Defined by |
|---|---|---|---|
| | from | to | |
| Single-ended output slew rate for rising edge | $V_{OL(AC)}$ | $V_{OH(AC)}$ | [$V_{OH(AC)}$ - $V_{OL(AC)}$] / DeltaTRse |
| Single-ended output slew rate for falling edge | $V_{OH(AC)}$ | $V_{OL(AC)}$ | [$V_{OH(AC)}$ - $V_{OL(AC)}$] / DeltaTFse |
| **Note:** Output slew rate is verified by design and characterization, and may not be subject to production test. | | | |


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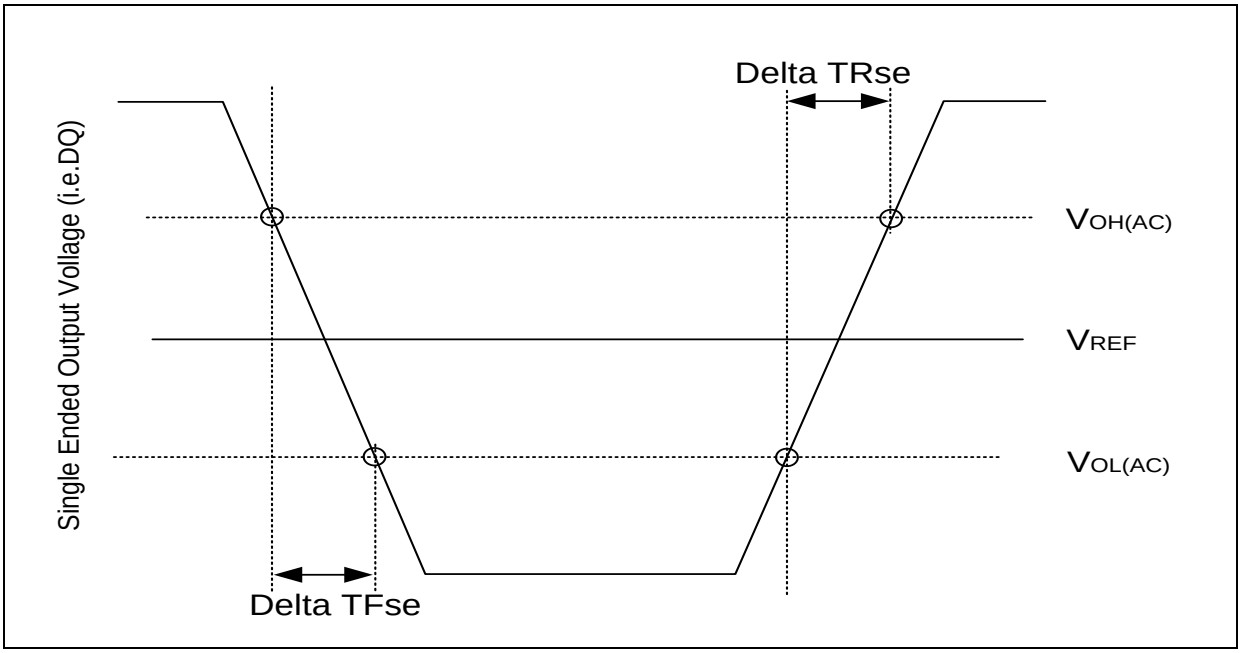



**Figure of Single Ended Output Slew Rate Definition**

**Table of Output Slew Rate (Single-Ended)**

| Symbol | Parameter | LPDDR2-800/1066 | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| SRQse | Single-ended Output Slew Rate (RON = 40Ω ± 30%) | 1.5 | 3.5 | V/nS |
| SRQse | Single-ended Output Slew Rate (RON = 60Ω ± 30%) | 1.0 | 2.5 | V/nS |
| | Output slew-rate matching Ratio (Pull-up to Pull-down) | 0.7 | 1.4 | |

**Description:**

**SR:** Slew Rate

**Q:** Query Output (like in DQ, which stands for Data-in, Query-Output)

**se:** Single-ended Signals

**Notes:**

1. Measured with output reference load.
2. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
3. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.
4. Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic high and 1/2 of DQ signals per data byte driving logic low.


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### 8.2.5.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OLdiff(AC)}$ and $V_{OHdiff(AC)}$ for differential signals as shown in below table and figure.

**Table of Differential Output Slew Rate Definition**

| Description | Measured | | Defined by |
|---|---|---|---|
| | from | to | |
| Differential output slew rate for rising edge | $V_{OLdiff(AC)}$ | $V_{OHdiff(AC)}$ | [$V_{OHdiff(AC)}$ - $V_{OLdiff(AC)}$] / DeltaTRdiff |
| Differential output slew rate for falling edge | $V_{OHdiff(AC)}$ | $V_{OLdiff(AC)}$ | [$V_{OHdiff(AC)}$ - $V_{OLdiff(AC)}$] / DeltaTFdiff |
| **Note:** Output slew rate is verified by design and characterization, and may not be subject to production test. | | | |

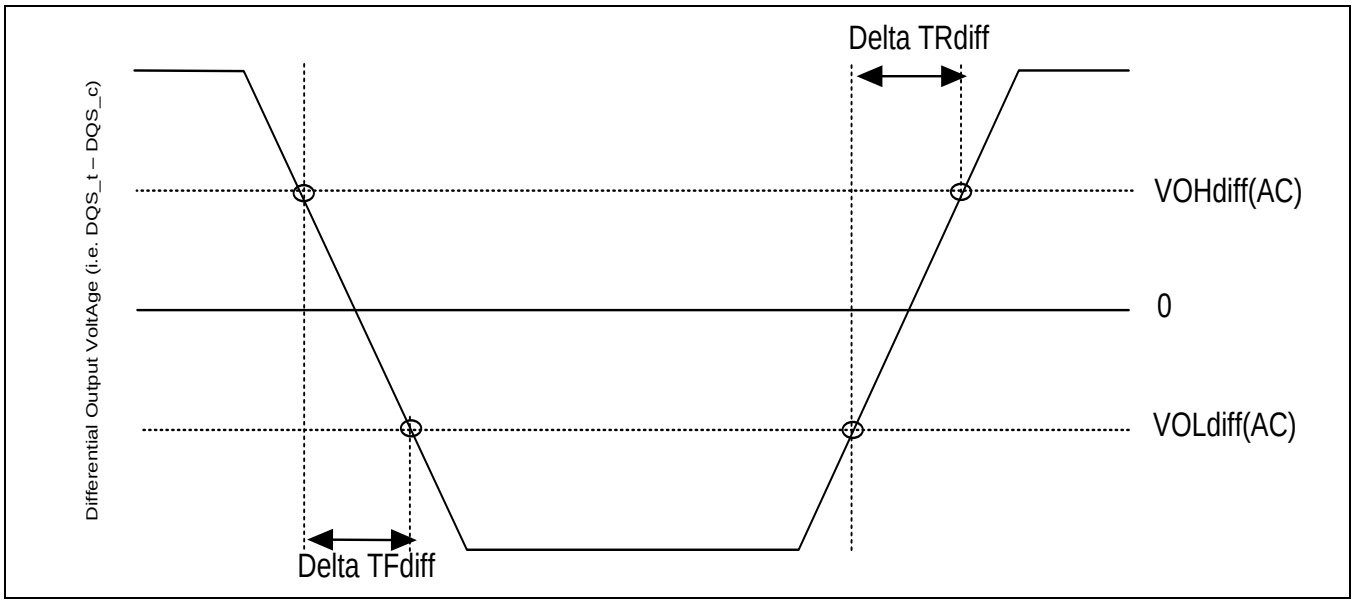



**Figure of Differential Output Slew Rate Definition**

**Table of Differential Output Slew Rate**

| Symbol | Parameter | LPDDR2-800/1066 | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| SRQdiff | Differential Output Slew Rate ($R_{ON}$ = 40Ω ± 30%) | 3.0 | 7.0 | V/nS |
| SRQdiff | Differential Output Slew Rate ($R_{ON}$ = 60Ω ± 30%) | 2.0 | 5.0 | V/nS |

**Description:**

**SR:** Slew Rate

**Q:** Query Output (like in DQ, which stands for Data-in, Query-Output)

**diff:** differential Signals

**Notes:**

1. Measured with output reference load.
2. The output slew rate for falling and rising edges is defined and measured between $V_{OLdiff(AC)}$ and $V_{OHdiff(AC)}$.
3. Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.


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### 8.2.5.5 Overshoot and Undershoot Specifications

**Table of AC Overshoot/Undershoot Specification**

| Parameter | | LPDDR2 | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | 1066 | 933 | 800 | 667 | 533 | 400 | 333 | |
| Maximum peak amplitude allowed for overshoot area. (See figure below) | Max | 0.35 | | | | | | | V |
| Maximum peak amplitude allowed for undershoot area. (See figure below) | Max | 0.35 | | | | | | | V |
| Maximum area above VDD. (See figure below) | Max | 0.15 | 0.17 | 0.20 | 0.24 | 0.30 | 0.40 | 0.48 | V-nS |
| Maximum area below VSS. (See figure below) | Max | 0.15 | 0.17 | 0.20 | 0.24 | 0.30 | 0.40 | 0.48 | V-nS |
| (CA0-9, CS_n, CKE, CK_t, CK_c, DQ, DQS_t, DQS_c, DM)<br>**Notes:**<br>1. For CA0-9, CK_t, CK_c, CS_n, and CKE, VDD stands for VDDCA. For DQ, DM, DQS_t, and DQS_c, VDD stands for VDDQ.<br>2. For CA0-9, CK_t, CK_c, CS_n, and CKE, VSS stands for VSSCA. For DQ, DM, DQS_t, and DQS_c, VSS stands for VSSQ.<br>3. Maximum peak amplitude values are referenced from actual VDD and VSS values.<br>4. Maximum area values are referenced from maximum operating VDD and VSS values. | | | | | | | | | |

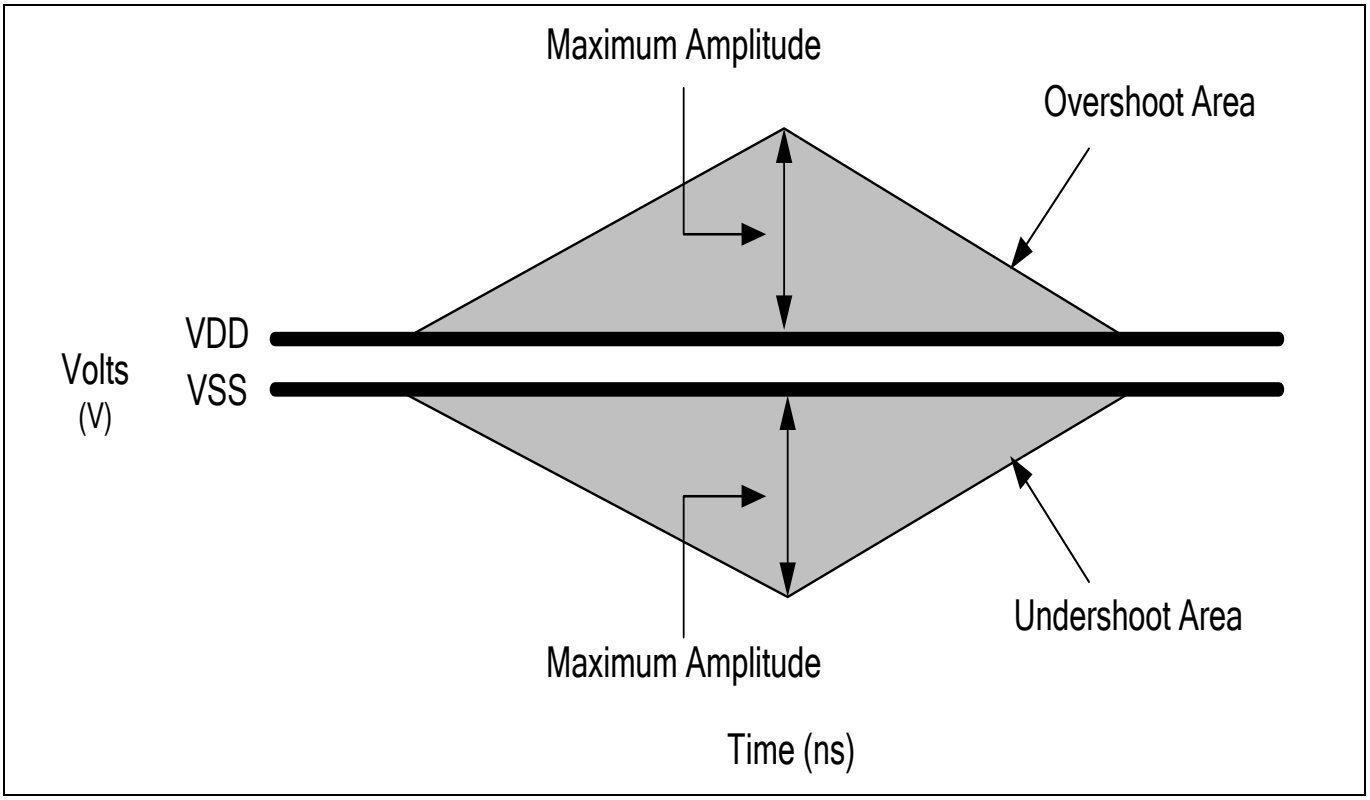



**Figure of Overshoot and Undershoot Definition**

**Notes:**
1. For CA0-9, CK_t, CK_c, CS_n, and CKE, VDD stands for VDDCA. For DQ, DM, DQS_t, and DQS_c, VDD stands for VDDQ.
2. For CA0-9, CK_t, CK_c, CS_n, and CKE, VSS stands for VSSCA. For DQ, DM, DQS_t, and DQS_c, VSS stands for VSSQ.
3. Maximum peak amplitude values are referenced from actual VDD and VSS values.
4. Maximum area values are referenced from maximum operating VDD and VSS values.


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### 8.2.6 Output buffer Characteristics

#### 8.2.6.1 HSUL_12 Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

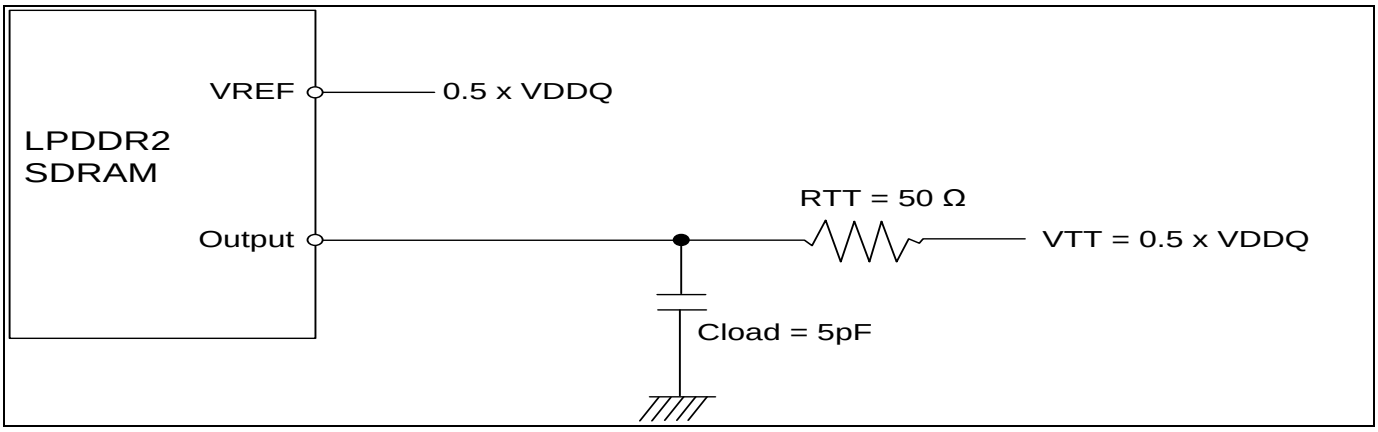



**Figure of HSUL_12 Driver Output Reference Load for Timing and Slew Rate**

**Note:**

All output timing parameter values (like $t_{DQSCK}$, $t_{DQSQ}$, $t_{QHS}$, $t_{HZ}$, $t_{RPRE}$ etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

#### 8.2.6.2 $RON_{PU}$ and $RON_{PD}$ Resistor Definition

$$RONPU = \frac{(VDDQ - Vout)}{ABS(Iout)}$$

Note: This is under the condition that $RON_{PD}$ is turned off

$$RONPD = \frac{Vout}{ABS(Iout)}$$

Note: This is under the condition that $RON_{PU}$ is turned off

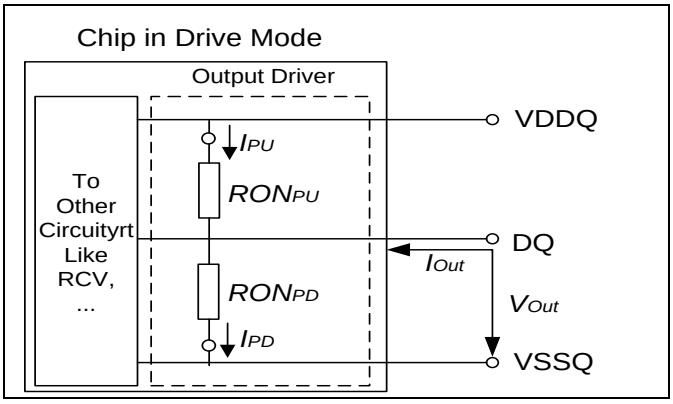



**Figure of Output Driver Definition of Voltages and Currents**

### 8.2.6.3 $RON_{PU}$ and $RON_{PD}$ Characteristics with ZQ Calibration

Output driver impedance RON is defined by the value of the external reference resistor RZQ. Nominal RZQ is 240Ω.

**Table of Output Driver DC Electrical Characteristics with ZQ Calibration**

| $RON_{NOM}$ | Resistor | Vout | Min | Nom | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 34.3Ω | RON34PD | 0.5 x VDDQ | 0.85 | 1.00 | 1.15 | RZQ/7 | 1, 2, 3, 4 |
| | RON34PU | 0.5 x VDDQ | 0.85 | 1.00 | 1.15 | RZQ/7 | 1, 2, 3, 4 |
| 40.0Ω | RON40PD | 0.5 x VDDQ | 0.85 | 1.00 | 1.15 | RZQ/6 | 1, 2, 3, 4 |
| | RON40PU | 0.5 x VDDQ | 0.85 | 1.00 | 1.15 | RZQ/6 | 1, 2, 3, 4 |
| 48.0Ω | RON48PD | 0.5 x VDDQ | 0.85 | 1.00 | 1.15 | RZQ/5 | 1, 2, 3, 4 |
| | RON48PU | 0.5 x VDDQ | 0.85 | 1.00 | 1.15 | RZQ/5 | 1, 2, 3, 4 |
| 60.0Ω | RON60PD | 0.5 x VDDQ | 0.85 | 1.00 | 1.15 | RZQ/4 | 1, 2, 3, 4 |
| | RON60PU | 0.5 x VDDQ | 0.85 | 1.00 | 1.15 | RZQ/4 | 1, 2, 3, 4 |
| 80.0Ω | RON80PD | 0.5 x VDDQ | 0.85 | 1.00 | 1.15 | RZQ/3 | 1, 2, 3, 4 |
| | RON80PU | 0.5 x VDDQ | 0.85 | 1.00 | 1.15 | RZQ/3 | 1, 2, 3, 4 |
| 120.0Ω | RON120PD | 0.5 x VDDQ | 0.85 | 1.00 | 1.15 | RZQ/2 | 1, 2, 3, 4 |
| | RON120PU | 0.5 x VDDQ | 0.85 | 1.00 | 1.15 | RZQ/2 | 1, 2, 3, 4 |
| Mismatch between pull-up and pull-down | $MM_{PUPD}$ | | -15.00 | | +15.00 | % | 1, 2, 3, 4, 5 |

**Notes:**

1. Across entire operating temperature range, after calibration.
2. RZQ = 240Ω.
3. The tolerance limits are specified after calibration with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
4. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x $V_{DDQ}$.
5. Measurement definition for mismatch between pull-up and pull-down: MMPUPD: Measure $RON_{PU}$ and $RON_{PD}$, both at 0.5 x VDDQ:

$$MMPUPD = \frac{RONPU - RONPD}{RONNOM} \text{ x } 100$$

For example, with MMPUPD(max) = 15% and RONPD = 0.85, RONPU must be less than 1.0.

### 8.2.6.4 Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the tables shown below.

**Table of Output Driver Sensitivity Definition**

| Resistor | Vout | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $RON_{PD}$ | 0.5 x VDDQ | 85 – (dR ONdT ×\|ΔT\| ) – (dRON d V × \|ΔV\| ) | 115 + (dRONdT ×\| ΔT\| )+(dRONdV × \|ΔV\|) | % | 1, 2 |
| $RON_{PU}$ | | | | | |

**Notes:**

1. ΔT = T–T (@calibration), ΔV=V–V(@ calibration).
2. dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

**Table of Output Driver Temperature and Voltage Sensitivity**

| Symbol | Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| dRONdT | RON Temperature Sensitivity | 0.00 | 0.75 | % / °C | |
| dRONdV | RON Voltage Sensitivity | 0.00 | 0.20 | % / mV | |


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#### 8.2.6.5 $RON_{PU}$ and $RON_{PD}$ Characteristics without ZQ Calibration

Output driver impedance RON is defined by design and characterization as default setting.

**Table of Output Driver DC Electrical Characteristics without ZQ Calibration**

| $RON_{NOM}$ | Resistor | Vout | Min | Nom | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 34.3Ω | RON34PD | 0.5 x $V_{DDQ}$ | 24 | 34.3 | 44.6 | Ω | 1 |
| | RON34PU | 0.5 x $V_{DDQ}$ | 24 | 34.3 | 44.6 | Ω | 1 |
| 40.0Ω | RON40PD | 0.5 x $V_{DDQ}$ | 28 | 40 | 52 | Ω | 1 |
| | RON40PU | 0.5 x $V_{DDQ}$ | 28 | 40 | 52 | Ω | 1 |
| 48.0Ω | RON48PD | 0.5 x $V_{DDQ}$ | 33.6 | 48 | 62.4 | Ω | 1 |
| | RON48PU | 0.5 x $V_{DDQ}$ | 33.6 | 48 | 62.4 | Ω | 1 |
| 60.0Ω | RON60PD | 0.5 x $V_{DDQ}$ | 42 | 60 | 78 | Ω | 1 |
| | RON60PU | 0.5 x $V_{DDQ}$ | 42 | 60 | 78 | Ω | 1 |
| 80.0Ω | RON80PD | 0.5 x $V_{DDQ}$ | 56 | 80 | 104 | Ω | 1 |
| | RON80PU | 0.5 x $V_{DDQ}$ | 56 | 80 | 104 | Ω | 1 |
| 120.0Ω | RON120PD | 0.5 x $V_{DDQ}$ | 84 | 120 | 156 | Ω | 1 |
| | RON120PU | 0.5 x $V_{DDQ}$ | 84 | 120 | 156 | Ω | 1 |

**Note:** Across entire operating temperature range, without calibration.


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### 8.2.6.6 RZQ I-V Curve

**Table of RZQ I-V Curve**

| Voltage[V] | RON = 240Ω (RZQ) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Pull-Down | | | | Pull-Up | | | |
| | Current [mA] / RON [Ohms] | | | | Current [mA] / RON [Ohms] | | | |
| | default value after ZQReset | | With Calibration | | default value after ZQReset | | With Calibration | |
| | Min | Max | Min | Max | Min | Max | Min | Max |
| | [mA] | [mA] | [mA] | [mA] | [mA] | [mA] | [mA] | [mA] |
| 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| 0.05 | 0.19 | 0.32 | 0.21 | 0.26 | -0.19 | -0.32 | -0.21 | -0.26 |
| 0.10 | 0.38 | 0.64 | 0.40 | 0.53 | -0.38 | -0.64 | -0.40 | -0.53 |
| 0.15 | 0.56 | 0.94 | 0.60 | 0.78 | -0.56 | -0.94 | -0.60 | -0.78 |
| 0.20 | 0.74 | 1.26 | 0.79 | 1.04 | -0.74 | -1.26 | -0.79 | -1.04 |
| 0.25 | 0.92 | 1.57 | 0.98 | 1.29 | -0.92 | -1.57 | -0.98 | -1.29 |
| 0.30 | 1.08 | 1.86 | 1.17 | 1.53 | -1.08 | -1.86 | -1.17 | -1.53 |
| 0.35 | 1.25 | 2.17 | 1.35 | 1.79 | -1.25 | -2.17 | -1.35 | -1.79 |
| 0.40 | 1.40 | 2.46 | 1.52 | 2.03 | -1.40 | -2.46 | -1.52 | -2.03 |
| 0.45 | 1.54 | 2.74 | 1.69 | 2.26 | -1.54 | -2.74 | -1.69 | -2.26 |
| 0.50 | 1.68 | 3.02 | 1.86 | 2.49 | -1.68 | -3.02 | -1.86 | -2.49 |
| 0.55 | 1.81 | 3.30 | 2.02 | 2.72 | -1.81 | -3.30 | -2.02 | -2.72 |
| 0.60 | 1.92 | 3.57 | 2.17 | 2.94 | -1.92 | -3.57 | -2.17 | -2.94 |
| 0.65 | 2.02 | 3.83 | 2.32 | 3.15 | -2.02 | -3.83 | -2.32 | -3.15 |
| 0.70 | 2.11 | 4.08 | 2.46 | 3.36 | -2.11 | -4.08 | -2.46 | -3.36 |
| 0.75 | 2.19 | 4.31 | 2.58 | 3.55 | -2.19 | -4.31 | -2.58 | -3.55 |
| 0.80 | 2.25 | 4.54 | 2.70 | 3.74 | -2.25 | -4.54 | -2.70 | -3.74 |
| 0.85 | 2.30 | 4.74 | 2.81 | 3.91 | -2.30 | -4.74 | -2.81 | -3.91 |
| 0.90 | 2.34 | 4.92 | 2.89 | 4.05 | -2.34 | -4.92 | -2.89 | -4.05 |
| 0.95 | 2.37 | 5.08 | 2.97 | 4.23 | -2.37 | -5.08 | -2.97 | -4.23 |
| 1.00 | 2.41 | 5.20 | 3.04 | 4.33 | -2.41 | -5.20 | -3.04 | -4.33 |
| 1.05 | 2.43 | 5.31 | 3.09 | 4.44 | -2.43 | -5.31 | -3.09 | -4.44 |
| 1.10 | 2.46 | 5.41 | 3.14 | 4.52 | -2.46 | -5.41 | -3.14 | -4.52 |
| 1.15 | 2.48 | 5.48 | 3.19 | 4.59 | -2.48 | -5.48 | -3.19 | -4.59 |
| 1.20 | 2.50 | 5.55 | 3.23 | 4.65 | -2.50 | -5.55 | -3.23 | -4.65 |


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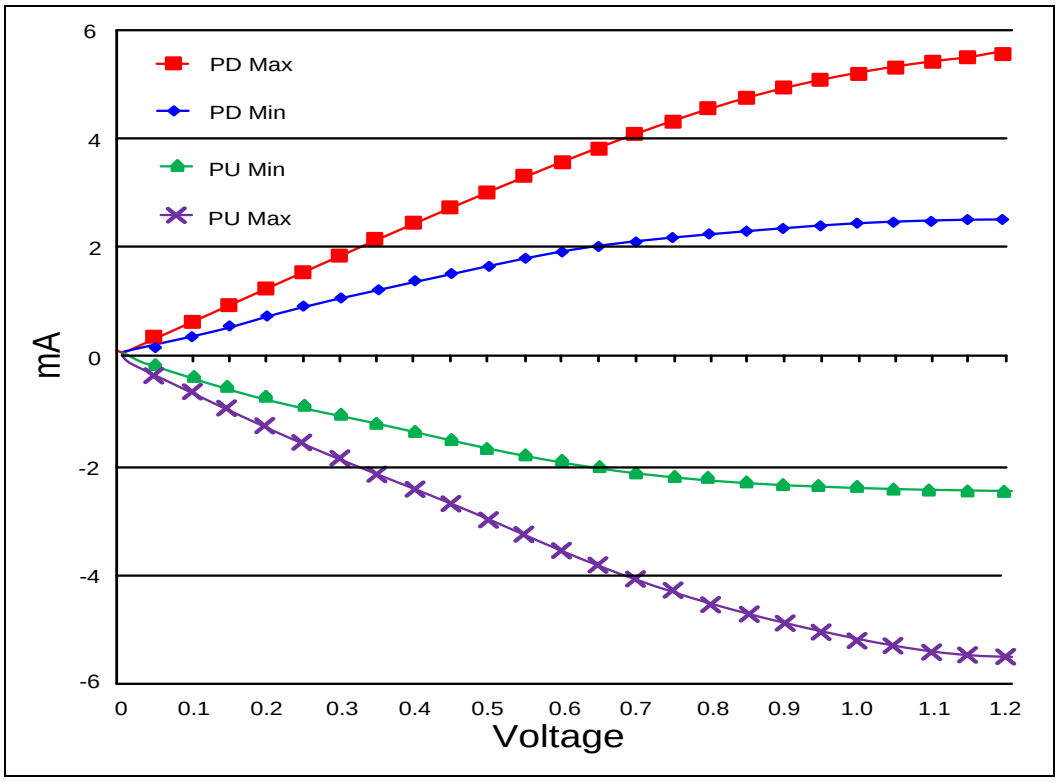



**Figure of RON = 240 Ohms IV Curve after ZQReset**

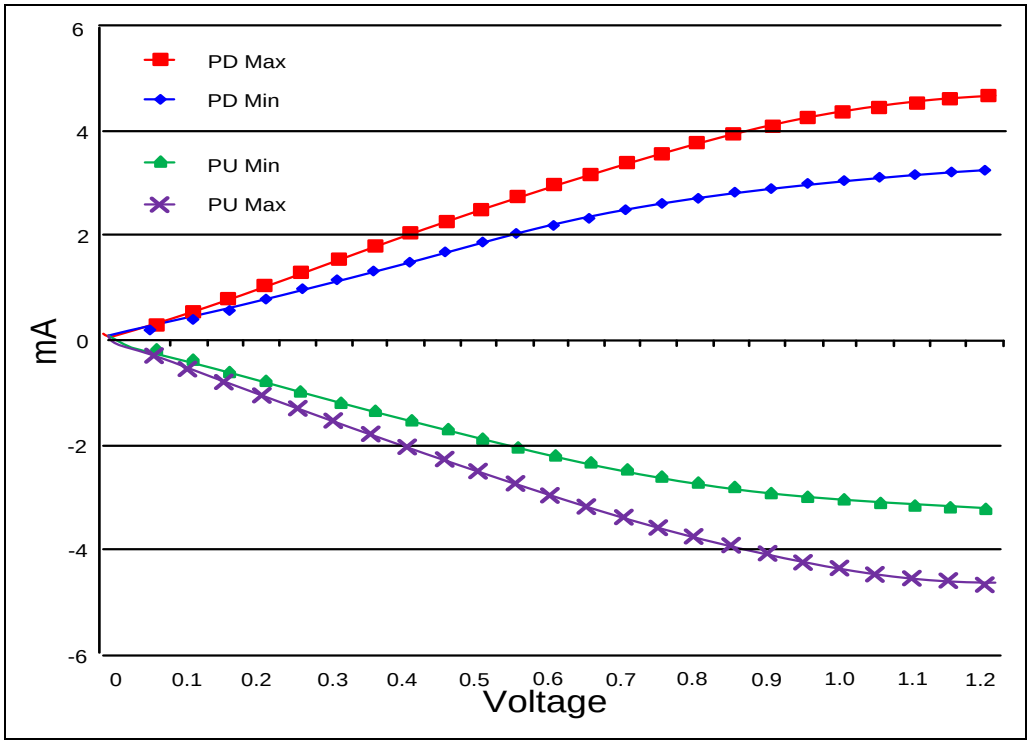



**Figure of RON = 240 Ohms IV Curve after Calibration**

### 8.2.6.7 Input/Output Capacitance

**Table of Input/Output Capacitance**

| Parameter | Symbol | Min | Max | Units | Note |
|---|---|---|---|---|---|
| Package Input capacitance, CK_t and CK_c | $C_{PKGCK}$ | 1 | 3 | pF | 1, 2 |
| Package Input capacitance delta, CK_t and CK_c | $C_{DPKGCK}$ | 0 | 0.2 | pF | 1, 2, 3 |
| Package Input capacitance, all other input-only pins | $C_{PKGI}$ | 1 | 3 | pF | 1, 2, 4 |
| Package Input capacitance delta, all other input-only pins | $C_{DPKGI}$ | -0.5 | 0.5 | pF | 1, 2, 5 |
| Package Input/output capacitance, DQ, DM, DQS_t, DQS_c | $C_{PKGIO}$ | 1.25 | 3.5 | pF | 1, 2, 7 |
| Package Input/output capacitance delta, DQS_t, DQS_c | $C_{DPKGDQS}$ | 0 | 0.25 | pF | 1, 2, 6 |
| Package Input/output capacitance delta, DQ, DM | $C_{DPKGIO}$ | -0.5 | 0.5 | pF | 1, 2, 7 |
| Package Input/output capacitance, ZQ Pin | $C_{PKGZQ}$ | 0 | 3.5 | pF | 1, 2 |

($T_{OPER}$; $V_{DDQ}$ = 1.14- 1.3V; $V_{DDCA}$ = 1.14-1.3V; $V_{DD1}$ = 1.7-1.95V, LPDDR2-S4 $V_{DD2}$ = 1.14-1.3V).

**Notes:**

1. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with $V_{DD1}$, $V_{DD2}$, $V_{DDQ}$, $V_{SS}$, $V_{SSCA}$, $V_{SSQ}$ applied and all other pins floating.
2. This parameter applies to package only (does not include die capacitance). This value is vendor specific.
3. Absolute value of CPKGCK_t - CPKGCK_c.
4. CPKGI applies to CS_n, CKE, CA0-CA9
5. CDPKGI = CPKGI - 0.5 * (CPKGDQS_t + CPKGDQS_c).
6. Absolute value of CPKGDQS_t and CPKGDQS_c.
7. CDPKGIO = CPKGIO - 0.5 * (CPKGDQS_t + CPKGDQS_c) in byte lane.
8. Maximum external load capacitance on ZQ pin, including packaging, board, pin, resistor, and other LPDDR2 devices: 5 pF.


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## 8.3 IDD Specification Parameters and Test Conditions

### 8.3.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables:

LOW: $V_{IN} \leq V_{IL(DC)}$ MAX
HIGH: $V_{IN} \geq V_{IH(DC)}$ MIN
STABLE: Inputs are stable at a HIGH or LOW level
SWITCHING: See tables below.

#### 8.3.1.1 Definition of Switching for CA Input Signals

| Switching for CA | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | CK_t (RISING) / Ck_C (FALLING) | CK_t (FALLING) / Ck_C (RISING) | CK_t (RISING) / Ck_C (FALLING) | CK_t (FALLING) / Ck_C (RISING) | CK_t (RISING) / Ck_C (FALLING) | CK_t (FALLING) / Ck_C (RISING) | CK_t (RISING) / Ck_C (FALLING) | CK_t (FALLING) / Ck_C (RISING) |
| Cycle | N | | N+1 | | N+2 | | N+3 | |
| CS_n | HIGH | | HIGH | | HIGH | | HIGH | |
| CA0 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA1 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |
| CA2 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA3 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |
| CA4 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA5 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |
| CA6 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA7 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |
| CA8 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA9 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |

**Notes:**

1. CS_n must always be driven HIGH.
2. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3. The above pattern (N, N+1, N+2, N+3...) is used continuously during IDD measurement for IDD values that require SWITCHING on the CA bus.


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### 8.3.1.2 Definition of Switching for IDD4R

| Clock | CKE | CS_n | Clock Cycle Number | Command | CA0-CA2 | CA3-CA9 | All DQ |
|---|---|---|---|---|---|---|---|
| Rising | HIGH | LOW | N | Read_Rising | HLH | LHLHLHL | L |
| Falling | HIGH | LOW | N | Read_Falling | LLL | LLLLLLL | L |
| Rising | HIGH | HIGH | N + 1 | NOP | LLL | LLLLLLL | H |
| Falling | HIGH | HIGH | N + 1 | NOP | HLH | HLHLLHL | L |
| Rising | HIGH | LOW | N + 2 | Read_Rising | HLH | HLHLLHL | H |
| Falling | HIGH | LOW | N + 2 | Read_Falling | LLL | HHHHHHH | H |
| Rising | HIGH | HIGH | N + 3 | NOP | LLL | HHHHHHH | H |
| Falling | HIGH | HIGH | N + 3 | NOP | HLH | LHLHLHL | L |

**Notes:**

1. Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2. The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4R.

### 8.3.1.3 Definition of Switching for IDD4W

| Clock | CKE | CS_n | Clock Cycle Number | Command | CA0-CA2 | CA3-CA9 | All DQ |
|---|---|---|---|---|---|---|---|
| Rising | HIGH | LOW | N | Write_Rising | HLL | LHLHLHL | L |
| Falling | HIGH | LOW | N | Write_Falling | LLL | LLLLLLL | L |
| Rising | HIGH | HIGH | N + 1 | NOP | LLL | LLLLLLL | H |
| Falling | HIGH | HIGH | N + 1 | NOP | HLH | HLHLLHL | L |
| Rising | HIGH | LOW | N + 2 | Write_Rising | HLL | HLHLLHL | H |
| Falling | HIGH | LOW | N + 2 | Write_Falling | LLL | HHHHHHH | H |
| Rising | HIGH | HIGH | N + 3 | NOP | LLL | HHHHHHH | H |
| Falling | HIGH | HIGH | N + 3 | NOP | HLH | LHLHLHL | L |

**Notes:**

1. Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2. Data masking (DM) must always be driven LOW.
3. The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4W.


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### 8.3.2 IDD Specifications

#### 8.3.2.1 LPDDR2 IDD Specification Parameters and Operating Conditions, -40°C~85°C (x16, x32)

| Parameter/Condition | Symbol | Power Supply | 400 MHz | 533 MHz | Unit | Notes |
|---|---|---|---|---|---|---|
| **Operating one bank active-precharge current:** | $IDD0_1$ | VDD1 | 4 | 4 | mA | 1 |
| $t_{CK}$ = $t_{CK(avg)min}$; $t_{RC}$ = $t_{RCmin}$; | $IDD0_2$ | VDD2 | 22.5 | 22.5 | mA | 1 |
| CKE is HIGH;<br>CS_n is HIGH between valid commands;<br>CA bus inputs are SWITCHING;<br>Data bus inputs are STABLE | $IDD0_{IN}$ | VDDCA<br>VDDQ | 5.5 | 5.5 | mA | 1, 2 |
| **Idle power-down standby current:** | $IDD2P_1$ | VDD1 | 300 | 300 | µA | 1 |
| $t_{CK}$ = $t_{CK(avg)min}$; | $IDD2P_2$ | VDD2 | 400 | 400 | µA | 1 |
| CKE is LOW; CS_n is HIGH;<br>All banks/RBs idle;<br>CA bus inputs are SWITCHING;<br>Data bus inputs are STABLE | $IDD2P_{IN}$ | VDDCA<br>VDDQ | 35 | 35 | µA | 1, 2 |
| **Idle power-down standby current with clock stop:** | $IDD2PS_1$ | VDD1 | 300 | 300 | µA | 1 |
| CK_t =LOW, CK_c =HIGH; | $IDD2PS_2$ | VDD2 | 400 | 400 | µA | 1 |
| CKE is LOW; CS_n is HIGH;<br>All banks/RBs idle;<br>CA bus inputs are STABLE;<br>Data bus inputs are STABLE | $IDD2PS_{IN}$ | VDDCA<br>VDDQ | 35 | 35 | µA | 1, 2 |
| **Idle non power-down standby current:** | $IDD2N_1$ | VDD1 | 0.3 | 0.3 | mA | 1 |
| $t_{CK}$ = $t_{CK(avg)min}$; | $IDD2N_2$ | VDD2 | 10 | 12 | mA | 1 |
| CKE is HIGH; CS_n is HIGH;<br>All banks/RBs idle;<br>CA bus inputs are SWITCHING;<br>Data bus inputs are STABLE | $IDD2N_{IN}$ | VDDCA<br>VDDQ | 4.1 | 4.1 | mA | 1, 2 |
| **Idle non power-down standby current with clock stop:** | $IDD2NS_1$ | VDD1 | 0.3 | 0.3 | mA | 1 |
| CK_t =LOW, CK_c =HIGH; | $IDD2NS_2$ | VDD2 | 9 | 11 | mA | 1 |
| CKE is HIGH; CS_n is HIGH;<br>All banks/RBs idle;<br>CA bus inputs are STABLE;<br>Data bus inputs are STABLE | $IDD2NS_{IN}$ | VDDCA<br>VDDQ | 4.1 | 4.1 | mA | 1, 2 |
| **Active power-down standby current:** | $IDD3P_1$ | VDD1 | 500 | 500 | µA | 1 |
| $t_{CK}$ = $t_{CK(avg)min}$; | $IDD3P_2$ | VDD2 | 500 | 500 | µA | 1 |
| CKE is LOW; CS_n is HIGH;<br>One bank/RB active;<br>CA bus inputs are SWITCHING;<br>Data bus inputs are STABLE | $IDD3P_{IN}$ | VDDCA<br>VDDQ | 35 | 35 | µA | 1, 2 |
| **Active power-down standby current with clock stop:** | $IDD3PS_1$ | VDD1 | 500 | 500 | µA | 1 |
| CK_t=LOW, CK_c=HIGH; | $IDD3PS_2$ | VDD2 | 500 | 500 | µA | 1 |
| CKE is LOW; CS_n is HIGH;<br>One bank/RB active;<br>CA bus inputs are STABLE;<br>Data bus inputs are STABLE | $IDD3PS_{IN}$ | VDDCA<br>VDDQ | 35 | 35 | µA | 1, 2 |
| **Active non power-down standby current:** | $IDD3N_1$ | VDD1 | 0.5 | 0.5 | mA | 1 |
| $t_{CK}$ = $t_{CK(avg)min}$; | $IDD3N_2$ | VDD2 | 12.6 | 14 | mA | 1 |
| CKE is HIGH; CS_n is HIGH;<br>One bank/RB active;<br>CA bus inputs are SWITCHING;<br>Data bus inputs are STABLE | $IDD3N_{IN}$ | VDDCA<br>VDDQ | 4.1 | 4.1 | mA | 1, 2 |
| **Active non power-down standby current with clock stop:** | $IDD3NS_1$ | VDD1 | 0.5 | 0.5 | mA | 1 |
| CK_t=LOW, CK_c=HIGH; | $IDD3NS_2$ | VDD2 | 11 | 12.6 | mA | 1 |
| CKE is HIGH; CS_n is HIGH;<br>One bank/RB active;<br>CA bus inputs are STABLE;<br>Data bus inputs are STABLE | $IDD3NS_{IN}$ | VDDCA<br>VDDQ | 4.1 | 4.1 | mA | 1, 2 |


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| Parameter/Condition | Symbol | Power Supply | 400 MHz | 533 MHz | Unit | Notes |
|---|---|---|---|---|---|---|
| **Operating burst read current:** | $IDD4R_1$ | VDD1 | 1.2 | 1.2 | mA | 1 |
| $t_{CK} = t_{CK(avg)min}$; | $IDD4R_2$ | VDD2 | 150 | 160 | mA | 1 |
| CS_n is HIGH between valid commands;<br>One bank/RB active;<br>BL = 4; RL = RLmin;<br>CA bus inputs are SWITCHING;<br>50% data change each burst transfer | $IDD4R_{IN}$ | VDDCA | 4.1 | 4.1 | mA | 1 |
| **Operating burst write current:** | $IDD4W_1$ | VDD1 | 1.2 | 1.2 | mA | 1 |
| $t_{CK} = t_{CK(avg)min}$; | $IDD4W_2$ | VDD2 | 175 | 175 | mA | 1 |
| CS_n is HIGH between valid commands;<br>One bank/RB active;<br>BL = 4; WL = WLmin;<br>CA bus inputs are SWITCHING;<br>50% data change each burst transfer | $IDD4W_{IN}$ | VDDCA<br>VDDQ | 19.1 | 19.1 | mA | 1, 2 |
| **All Bank Refresh Burst current:** | $IDD5_1$ | VDD1 | 14 | 14 | mA | 1 |
| $t_{CK} = t_{CK(avg)min}$; | $IDD5_2$ | VDD2 | 40 | 40 | mA | 1 |
| CKE is HIGH between valid commands;<br>$t_{RC} = t_{RFCabmin}$;<br>Burst refresh;<br>CA bus inputs are SWITCHING;<br>Data bus inputs are STABLE; | $IDD5_{IN}$ | VDDCA<br>VDDQ | 4.1 | 4.1 | mA | 1, 2 |
| **All Bank Refresh Average current:** | $IDD5AB_1$ | VDD1 | 0.9 | 0.9 | mA | 1 |
| $t_{CK} = t_{CK(avg)min}$; | $IDD5AB_2$ | VDD2 | 12 | 12 | mA | 1 |
| CKE is HIGH between valid commands;<br>$t_{RC} = t_{REFI}$;<br>CA bus inputs are SWITCHING;<br>Data bus inputs are STABLE; | $IDD5AB_{IN}$ | VDDCA<br>VDDQ | 4.1 | 4.1 | mA | 1, 2 |
| **Deep Power-Down current:** | $IDD8_1$ | VDD1 | 10 | 10 | µA | 1 |
| CK_t=LOW, CK_c=HIGH; | $IDD8_2$ | VDD2 | 10 | 10 | µA | 1 |
| CKE is LOW;<br>CA bus inputs are STABLE;<br>Data bus inputs are STABLE; | $IDD8_{IN}$ | VDDCA<br>VDDQ | 35 | 35 | µA | 1, 2 |

**Notes:**

1. $I_{DD}$ values published are the maximum of the distribution of the arithmetic mean.
2. Measured currents are the summation of $V_{DDQ}$ and $V_{DDCA}$.
3. $I_{DD}$ current specifications are tested after the device is properly initialized.


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#### 8.3.2.2 IDD6 Partial Array Self-Refresh Current, (x16, x32)

| Parameter | | Symbol | Power Supply | 400 MHz | 533 MHz | Condition | Unit |
|---|---|---|---|---|---|---|---|
| IDD6 Partial Array Self-Refresh Current | Full Array | $IDD6_1$ | VDD1 | 500 | 500 | **Self refresh current**<br>CK_t=LOW, CK_c=HIGH;<br>CKE is LOW;<br>CA bus inputs are STABLE;<br>Data bus inputs are STABLE; | µA |
| | | $IDD6_2$ | VDD2 | 600 | 600 | | |
| | | $IDD6_{IN}$ | VDDCA<br>VDDQ | 35 | 35 | | |
| | 1/2 Array | $IDD6_1$ | VDD1 | 450 | 450 | | µA |
| | | $IDD6_2$ | VDD2 | 500 | 500 | | |
| | | $IDD6_{IN}$ | VDDCA<br>VDDQ | 35 | 35 | | |
| | 1/4 Array | $IDD6_1$ | VDD1 | 400 | 400 | | µA |
| | | $IDD6_2$ | VDD2 | 450 | 450 | | |
| | | $IDD6_{IN}$ | VDDCA<br>VDDQ | 35 | 35 | | |

**Notes:**
1. LPDDR2-S4 SDRAM uses the same PASR scheme & IDD6 current value categorization as LPDDR (JESD209).
2. IDD values published are the maximum of the distribution of the arithmetic mean.

## 8.4 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR2 device.

### 8.4.1 Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left[\sum_{j=1}^{N} tCK_j\right] / N$$

$$where \qquad N = 200$$

Unit 'tCK(avg)' represents the actual clock average tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.

tCK(avg) may change by up to ± 1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

### 8.4.2 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.

tCK(abs) is not subject to production test.


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### 8.4.3 Definition for $t_{CH(avg)}$ and $t_{CL(avg)}$

$t_{CH(avg)}$ is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left[\sum_{j=1}^{N} tCH_j\right] / (N \times tCK(avg))$$

$$where \qquad N = 200$$

$t_{CL(avg)}$ is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left[\sum_{j=1}^{N} tCL_j\right] / (N \times tCK(avg))$$

$$where \qquad N = 200$$

### 8.4.4 Definition for $t_{JIT(per)}$

$t_{JIT(per)}$ is the single period jitter defined as the largest deviation of any signal $t_{CK}$ from $t_{CK(avg)}$.
$t_{JIT(per)}$ = Min/max of {$t_{CKi}$ - $t_{CK(avg)}$ where i = 1 to 200}.
$t_{JIT(per)}$,act is the actual clock jitter for a given system.
$t_{JIT(per)}$,allowed is the specified allowed clock period jitter.
$t_{JIT(per)}$ is not subject to production test.

### 8.4.5 Definition for $t_{JIT(cc)}$

$t_{JIT(cc)}$ is defined as the absolute difference in clock period between two consecutive clock cycles.
$t_{JIT(cc)}$ = Max of |{$t_{CK_{i+1}}$ - $t_{CK_i}$}|.
$t_{JIT(cc)}$ defines the cycle to cycle jitter.
$t_{JIT(cc)}$ is not subject to production test.

### 8.4.6 Definition for $t_{ERR(nper)}$

$t_{ERR(nper)}$ is defined as the cumulative error across n multiple consecutive cycles from $t_{CK(avg)}$.
$t_{ERR(nper)}$,act is the actual clock jitter over n cycles for a given system.
$t_{ERR(nper)}$,allowed is the specified allowed clock period jitter over n cycles.
$t_{ERR(nper)}$ is not subject to production test.

$$tERR(nper) = \left[\sum_{j=i}^{i+n-1} tCK_j\right] - n \times tCK(avg)$$

$t_{ERR(nper)}$,min can be calculated by the formula shown below:

$$tERR(nper), min = (1 + 0.68LN(n)) \times tJIT(per), min$$

$t_{ERR(nper)}$,max can be calculated by the formula shown below:

$$tERR(nper), max = (1 + 0.68LN(n)) \times tJIT(per), max$$

Using these equations, $t_{ERR(nper)}$ tables can be generated for each $t_{JIT(per)}$,act value.


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### 8.4.7 Definition for Duty Cycle Jitter $t_{JIT(duty)}$

$t_{JIT(duty)}$ is defined with absolute and average specification of $t_{CH}$ / $t_{CL}$.

$t_{JIT(duty),min} = MIN((tCH(abs),min - tCH(avg),min),(tCL(abs),min - tCL(avg),min)) \times tCK(avg)$

$tJIT(duty),max = MAX((tCH(abs),max - tCH(avg),max),(tCL(abs),max - tCL(avg),max)) \times tCK(avg)$

### 8.4.8 Definition for $t_{CK(abs)}$, $t_{CH(abs)}$ and $t_{CL(abs)}$

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

**Table of Definition for $t_{CK(abs)}$, $t_{CH(abs)}$, and $t_{CL(abs)}$**

| Parameter | Symbol | Min | Unit |
|---|---|---|---|
| Absolute Clock Period | tCK(abs) | tCK(avg),min + tJIT(per),min | pS |
| Absolute Clock HIGH Pulse Width | tCH(abs) | tCH(avg),min + tJIT(duty),min / tCK(avg)min | tCK(avg) |
| Absolute Clock LOW Pulse Width | tCL(abs) | tCL(avg),min + tJIT(duty),min / tCK(avg)min | tCK(avg) |

**Notes:**

1. $t_{CK(avg),min}$ is expressed is pS for this table.
2. $t_{JIT(duty),min}$ is a negative value.

## 8.5 Period Clock Jitter

LPDDR2 devices can tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter ($t_{JIT(per)}$) in excess of the values found in section 8.7.1 **"LPDDR2 AC Timing"** table and how to determine cycle time de-rating and clock cycle de-rating.

### 8.5.1 Clock Period Jitter Effects on Core Timing Parameters ($t_{RCD}$, $t_{RP}$, $t_{RTP}$, $t_{WR}$, $t_{WRA}$, $t_{WTR}$, $t_{RC}$, $t_{RAS}$, $t_{RRD}$, $t_{FAW}$)

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR2 device is characterized and verified to support $t_{nPARAM} = RU\{t_{PARAM} / t_{CK(avg)}\}$.

When the device is operated with clock jitter outside specification limits, the number of clocks or $t_{CK(avg)}$ may need to be increased based on the values for each core timing parameter.

#### 8.5.1.1 Cycle Time De-rating for Core Timing Parameters

For a given number of clocks ($t_{nPARAM}$), for each core timing parameter, average clock period ($t_{CK(avg)}$) and actual cumulative period error ($t_{ERR}(t_{nPARAM}),act$) in excess of the allowed cumulative period error ($t_{ERR}(t_{nPARAM}),allowed$), the equation below calculates the amount of cycle time de-rating (in nS) required if the equation results in a positive value for a core timing parameter ($t_{CORE}$).

$$CycleTimeDerating = MAX\left\{\left(\frac{tPARAM + tERR(tnPARAM), act - tERR(tnPARAM), allowed}{tnPARAM} - tCK(avg)\right), 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

#### 8.5.1.2 Clock Cycle De-rating for Core Timing Parameters

For a given number of clocks ($t_{nPARAM}$) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter ($t_{JIT(per)}$).

For a given number of clocks ($t_{nPARAM}$), for each core timing parameter, average clock period ($t_{CK(avg)}$) and actual cumulative period error ($t_{ERR(nPARAM),act}$) in excess of the allowed cumulative period error ($t_{ERR(nPARAM),allowed}$), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter ($t_{CORE}$).

$$ClockCycleDerating = RU\left\{\frac{tPARAM + tERR(tnPARAM), act - tERR(tnPARAM), allowed}{tCK(avg)}\right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

### 8.5.2 Clock Jitter Effects on Command/Address Timing Parameters ($t_{IS}$, $t_{IH}$, $t_{ISCKE}$, $t_{IHCKE}$, $t_{ISb}$, $t_{IHb}$, $t_{ISCKEb}$, $t_{IHCKEb}$)

These parameters are measured from a command/address signal (CKE, CS, CA0 - CA9) transition edge to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$, as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

### 8.5.3 Clock Jitter Effects on Read Timing Parameters

#### 8.5.3.1 $t_{RPRE}$

When the device is operated with input clock jitter, $t_{RPRE}$ needs to be de-rated by the actual period jitter ($t_{JIT(per),act,max}$) of the input clock in excess of the allowed period jitter ($t_{JIT(per),allowed,max}$). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9 - \left(\frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)}\right)$$

For example,
if the measured jitter into a LPDDR2-800 device has $t_{CK(avg)}$ = 2500 pS, $t_{JIT(per),act,min}$ = -172 pS and $t_{JIT(per),act,max}$ = + 193 pS, then
$t_{RPRE,min,derated}$ = 0.9 - ($t_{JIT(per),act,max}$ - $t_{JIT(per),allowed,max}$)/$t_{CK(avg)}$ = 0.9 - (193 - 100)/2500= .8628 $t_{CK(avg)}$

#### 8.5.3.2 $t_{LZ(DQ)}$, $t_{HZ(DQ)}$, $t_{DQSCK}$, $t_{LZ(DQS)}$, $t_{HZ(DQS)}$

These parameters are measured from a specific clock edge to a data signal (DMn, DQm.: n=0,1,2,3. m=0–31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$.

#### 8.5.3.3 $t_{QSH}$, $t_{QSL}$

These parameters are affected by duty cycle jitter which is represented by $t_{CH(abs)min}$ and $t_{CL(abs)min}$.
$t_{QSH(abs)min}$ = $t_{CH(abs)min}$ – 0.05
$t_{QSL(abs)min}$ = $t_{CL(abs)min}$ – 0.05
These parameters determine absolute Data-Valid window at the LPDDR2 device pin.
Absolute min data-valid window @ LPDDR2 device pin =
min { ( $t_{QSH(abs)}$min * $t_{CK(avg)}$min – $t_{DQSQ}$max – $t_{QHS}$max ) , ( $t_{QSL(abs)}$min * $t_{CK(avg)}$min – $t_{DQSQ}$max – $t_{QHS}$max ) }
This minimum data-valid window shall be met at the target frequency regardless of clock jitter.


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#### 8.5.3.4 tRPST

tRPST is affected by duty cycle jitter which is represented by tCL(abs). Therefore tRPST(abs)min can be specified by tCL(abs)min.

tRPST(abs)min = tCL(abs)min – 0.05 = tQSL(abs)min

### 8.5.4 Clock Jitter Effects on Write Timing Parameters

#### 8.5.4.1 tDS, tDH

These parameters are measured from a data signal (DMn, DQm.: n=0,1,2,3. m=0–31) transition edge to its respective data strobe signal (DQSn_t, DQSn_c: n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

#### 8.5.4.2 tDSS, tDSH

These parameters are measured from a data strobe signal (DQSx_t, DQSx_c) crossing to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

#### 8.5.4.3 tDQSS

This parameter is measured from a data strobe signal (DQSx_t, DQSx_c) crossing to the subsequent clock signal (CK_t/CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual period jitter tJIT(per),act of the input clock in excess of the allowed period jitter tJIT(per),allowed.

$$tDQSS(min,\ derated) = 0.75 - \frac{tJIT(per),act,min - tJIT(per),allowed,min}{tCK(avg)}$$

$$tDQSS(max,\ derated) = 1.25 - \frac{tJIT(per),act,max - tJIT(per),allowed,max}{tCK(avg)}$$

For example,

if the measured jitter into a LPDDR2-800 device has tCK(avg) = 2500 pS, tJIT(per),act,min = -172 pS and tJIT(per),act,max = + 193 pS, then

tDQSS,(min,derated) = 0.75 - (tJIT(per),act,min - tJIT(per),allowed,min)/tCK(avg) = 0.75 - (-172 + 100)/2500 = .7788 tCK(avg)

and

tDQSS,(max,derated) = 1.25 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 1.25 - (193 - 100)/2500 = 1.2128 tCK(avg)


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## 8.6 Refresh Requirements

### 8.6.1 Refresh Requirement Parameters

| Parameter | | Symbol | 256Mb | Unit |
|---|---|---|---|---|
| Number of Banks | | | 4 | |
| Refresh Window $T_{CASE} \leq 85°C$ | | $t_{REFW}$ | 32 | mS |
| Required number of REFRESH commands (min) | | R | 4,096 | |
| Average time between REFRESH commands (for reference only) $T_{CASE} \leq 85°C$ | REFab | $t_{REFI}$ | 7.8 | µS |
| Refresh Cycle time | | $t_{RFCab}$ | 90 | nS |
| Burst Refresh Window = 4 x 8 x $t_{RFCab}$ | | $t_{REFBW}$ | 2.88 | µS |


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## 8.7 AC Timings

### 8.7.1 LPDDR2 AC Timing

(Note 6 apply to the entire table)

| Parameter | Symbol | min / max | min tCK | Data Rate | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 1066 | 933 | 800 | 667 | 533 | 400 | 333 | |
| Max. Frequency[*4] | | ~ | | 533 | 466 | 400 | 333 | 266 | 200 | 166 | MHz |
| **Clock Timing** | | | | | | | | | | | |
| Average Clock Period | tCK(avg) | MIN | | 1.875 | 2.15 | 2.5 | 3 | 3.75 | 5 | 6 | nS |
| | | MAX | | 100 | | | | | | | |
| Average high pulse width | tCH(avg) | MIN | | 0.45 | | | | | | | tCK(avg) |
| | | MAX | | 0.55 | | | | | | | |
| Average low pulse width | tCL(avg) | MIN | | 0.45 | | | | | | | tCK(avg) |
| | | MAX | | 0.55 | | | | | | | |
| Absolute Clock Period | tCK(abs) | MIN | | tCK(avg)min + tJIT(per)min | | | | | | | pS |
| Absolute clock HIGH pulse width (with allowed jitter) | tCH(abs), allowed | MIN | | 0.43 | | | | | | | tCK(avg) |
| | | MAX | | 0.57 | | | | | | | |
| Absolute clock LOW pulse width (with allowed jitter) | tCL(abs), (allowed) | MIN | | 0.43 | | | | | | | tCK(avg) |
| | | MAX | | 0.57 | | | | | | | |
| Clock Period Jitter (with allowed jitter) | tJIT(per), (allowed) | MIN | | -90 | -95 | -100 | -110 | -120 | -140 | -150 | pS |
| | | MAX | | 90 | 95 | 100 | 110 | 120 | 140 | 150 | |
| Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter) | tJIT(cc), allowed | MAX | | 180 | 190 | 200 | 220 | 240 | 280 | 300 | pS |
| Duty cycle Jitter (with allowed jitter) | tJIT(duty), allowed | MIN | | MIN ((tCH(abs),min - tCH(avg),min), (tCL(abs),min - tCL(avg),min)) * tCK(avg) | | | | | | | pS |
| | | MAX | | MAX ((tCH(abs),max - tCH(avg),max), (tCL(abs),max - tCL(avg),max)) * tCK(avg) | | | | | | | pS |
| Cumulative error across 2 cycles | tERR(2per), (allowed) | MIN | | -132 | -140 | -147 | -162 | -177 | -206 | -221 | pS |
| | | MAX | | 132 | 140 | 147 | 162 | 177 | 206 | 221 | |
| Cumulative error across 3 cycles | tERR(3per), (allowed) | MIN | | -157 | -166 | -175 | -192 | -210 | -245 | -262 | pS |
| | | MAX | | 157 | 166 | 175 | 192 | 210 | 245 | 262 | |
| Cumulative error across 4 cycles | tERR(4per), (allowed) | MIN | | -175 | -185 | -194 | -214 | -233 | -272 | -291 | pS |
| | | MAX | | 175 | 185 | 194 | 214 | 233 | 272 | 291 | |
| Cumulative error across 5 cycles | tERR(5per), (allowed) | MIN | | -188 | -199 | -209 | -230 | -251 | -293 | -314 | pS |
| | | MAX | | 188 | 199 | 209 | 230 | 251 | 293 | 314 | |
| Cumulative error across 6 cycles | tERR(6per), (allowed) | MIN | | -200 | -211 | -222 | -244 | -266 | -311 | -333 | pS |
| | | MAX | | 200 | 211 | 222 | 244 | 266 | 311 | 333 | |
| Cumulative error across 7 cycles | tERR(7per), (allowed) | MIN | | -209 | -221 | -232 | -256 | -279 | -325 | -348 | pS |
| | | MAX | | 209 | 221 | 232 | 256 | 279 | 325 | 348 | |
| Cumulative error across 8 cycles | tERR(8per), (allowed) | MIN | | -217 | -229 | -241 | -266 | -290 | -338 | -362 | pS |
| | | MAX | | 217 | 229 | 241 | 266 | 290 | 338 | 362 | |
| Cumulative error across 9 cycles | tERR(9per), (allowed) | MIN | | -224 | -237 | -249 | -274 | -299 | -349 | -374 | pS |
| | | MAX | | 224 | 237 | 249 | 274 | 299 | 349 | 374 | |
| Cumulative error across 10 cycles | tERR(10per), (allowed) | MIN | | -231 | -244 | -257 | -282 | -308 | -359 | -385 | pS |
| | | MAX | | 231 | 244 | 257 | 282 | 308 | 359 | 385 | |
| Cumulative error across 11 cycles | tERR(11per), (allowed) | MIN | | -237 | -250 | -263 | -289 | -316 | -368 | -395 | pS |
| | | MAX | | 237 | 250 | 263 | 289 | 316 | 368 | 395 | |
| Cumulative error across 12 cycles | tERR(12per), (allowed) | MIN | | -242 | -256 | -269 | -296 | -323 | -377 | -403 | pS |
| | | MAX | | 242 | 256 | 269 | 296 | 323 | 377 | 403 | |
| Cumulative error across n = 13, 14 . . . 49, 50 cycles | tERR(nper), (allowed) | MIN | | tERR(nper),allowed,min = (1 + 0.68ln(n)) * tJIT(per),allowed,min | | | | | | | pS |
| | | MAX | | tERR(nper),allowed,max = (1 + 0.68ln(n)) * tJIT(per),allowed,max | | | | | | | |


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| Parameter | Symbol | min / max | min tCK | Data Rate | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 1066 | 933 | 800 | 667 | 533 | 400 | 333 | |
| **ZQ Calibration Parameters** | | | | | | | | | | | |
| Initialization Calibration Time | tZQINIT | MIN | | 1 | | | | | | | µS |
| Full Calibration Time | tZQCL | MIN | 6 | 360 | | | | | | | nS |
| Short Calibration Time | tZQCS | MIN | 6 | 90 | | | | | | | nS |
| Calibration Reset Time | tZQRESET | MIN | 3 | 50 | | | | | | | nS |
| **Read Parameters*11** | | | | | | | | | | | |
| DQS output access time from CK_t/CK_c | tDQSCK | MIN | | 2500 | | | | | | | pS |
| | | MAX | | 5500 | | | | | | | |
| DQSCK Delta Short*15 | tDQSCKDS | MAX | | 330 | 380 | 450 | 540 | 670 | 900 | 1080 | pS |
| DQSCK Delta Medium*16 | tDQSCKDM | MAX | | 680 | 780 | 900 | 1050 | 1350 | 1800 | 1900 | pS |
| DQSCK Delta Long*17 | tDQSCKDL | MAX | | 920 | 1050 | 1200 | 1400 | 1800 | 2400 | - | pS |
| DQS - DQ skew | tDQSQ | MAX | | 200 | 220 | 240 | 280 | 340 | 400 | 500 | pS |
| Data hold skew factor | tQHS | MAX | | 230 | 260 | 280 | 340 | 400 | 480 | 600 | pS |
| DQS Output High Pulse Width | tQSH | MIN | | tCH(abs) - 0.05 | | | | | | | tCK(avg) |
| DQS Output Low Pulse Width | tQSL | MIN | | tCL(abs) - 0.05 | | | | | | | tCK(avg) |
| Data Half Period | tQHP | MIN | | min(tQSH, tQSL) | | | | | | | tCK(avg) |
| DQ / DQS output hold time from DQS | tQH | MIN | | tQHP - tQHS | | | | | | | pS |
| Read preamble*12,*13 | tRPRE | MIN | | 0.9 | | | | | | | tCK(avg) |
| Read postamble*12,*14 | tRPST | MIN | | tCL(abs) - 0.05 | | | | | | | tCK(avg) |
| DQS low-Z from clock*12 | tLZ(DQS) | MIN | | tDQSCK(MIN) - 300 | | | | | | | pS |
| DQ low-Z from clock*12 | tLZ(DQ) | MIN | | tDQSCK(MIN) - (1.4 * tQHS(MAX)) | | | | | | | pS |
| DQS high-Z from clock*12 | tHZ(DQS) | MAX | | tDQSCK(MAX) - 100 | | | | | | | pS |
| DQ high-Z from clock*12 | tHZ(DQ) | MAX | | tDQSCK(MAX) + (1.4 * tDQSQ(MAX)) | | | | | | | pS |
| **Write Parameters*11** | | | | | | | | | | | |
| DQ and DM input hold time (Vref based) | tDH | MIN | | 210 | 235 | 270 | 350 | 430 | 480 | 600 | pS |
| DQ and DM input setup time (Vref based) | tDS | MIN | | 210 | 235 | 270 | 350 | 430 | 480 | 600 | pS |
| DQ and DM input pulse width | tDIPW | MIN | | 0.35 | | | | | | | tCK(avg) |
| Write command to 1st DQS latching transition | tDQSS | MIN | | 0.75 | | | | | | | tCK(avg) |
| | | MAX | | 1.25 | | | | | | | |
| DQS input high-level width | tDQSH | MIN | | 0.4 | | | | | | | tCK(avg) |
| DQS input low-level width | tDQSL | MIN | | 0.4 | | | | | | | tCK(avg) |
| DQS falling edge to CK setup time | tDSS | MIN | | 0.2 | | | | | | | tCK(avg) |
| DQS falling edge hold time from CK | tDSH | MIN | | 0.2 | | | | | | | tCK(avg) |
| Write postamble | tWPST | MIN | | 0.4 | | | | | | | tCK(avg) |
| Write preamble | tWPRE | MIN | | 0.35 | | | | | | | tCK(avg) |
| **CKE Input Parameters** | | | | | | | | | | | |
| CKE min. pulse width (high and low pulse width) | tCKE | MIN | 3 | 3 | | | | | | | tCK(avg) |
| CKE input setup time | tISCKE*2 | MIN | | 0.25 | | | | | | | tCK(avg) |
| CKE input hold time | tIHCKE*3 | MIN | | 0.25 | | | | | | | tCK(avg) |


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| Parameter | Symbol | min / max | min tCK | Data Rate | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 1066 | 933 | 800 | 667 | 533 | 400 | 333 | |
| **Command Address Input Parameters[*11]** | | | | | | | | | | | |
| Address and control input setup time (Vref based) | tIS[*1] | MIN | | 220 | 250 | 290 | 370 | 460 | 600 | 740 | pS |
| Address and control input hold time (Vref based) | tIH[*1] | MIN | | 220 | 250 | 290 | 370 | 460 | 600 | 740 | pS |
| Address and control input pulse width | tIPW | MIN | | 0.40 | | | | | | | tCK(avg) |
| **Boot Parameters (10 MHz - 55 MHz)[*5, 7, 8]** | | | | | | | | | | | |
| Clock Cycle Time | tCKb | MAX | | 100 | | | | | | | nS |
| | | MIN | | 18 | | | | | | | |
| CKE Input Setup Time | tISCKEb | MIN | | 2.5 | | | | | | | nS |
| CKE Input Hold Time | tIHCKEb | MIN | | 2.5 | | | | | | | nS |
| Address & Control Input Setup Time | tISb | MIN | | 1150 | | | | | | | pS |
| Address & Control Input Hold Time | tIHb | MIN | | 1150 | | | | | | | pS |
| DQS Output Data Access Time from CK_t/CK_c | tDQSCKb | MIN | | 2.0 | | | | | | | nS |
| | | MAX | | 10.0 | | | | | | | |
| Data Strobe Edge to Output Data Edge tDQSQb - 1.2 | tDQSQb | MAX | | 1.2 | | | | | | | nS |
| Data Hold Skew Factor | tQHSb | MAX | | 1.2 | | | | | | | nS |
| **Mode Register Parameters** | | | | | | | | | | | |
| MODE REGISTER Write command period | tMRW | MIN | 5 | 5 | | | | | | | tCK(avg) |
| Mode Register Read command period | tMRR | MIN | 2 | 2 | | | | | | | tCK(avg) |
| **LPDDR2 SDRAM Core Parameters[*9]** | | | | | | | | | | | |
| Read Latency | RL | MIN | 3 | 8 | 7 | 6 | 5 | 4 | 3 | 3 | tCK(avg) |
| Write Latency | WL | MIN | 1 | 4 | 4 | 3 | 2 | 2 | 1 | 1 | tCK(avg) |
| ACTIVE to ACTIVE command period | tRC | MIN | | tRAS + tRPab (with all-bank Precharge)<br>tRAS + tRPpb (with per-bank Precharge) | | | | | | | nS |
| CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh) | tCKESR | MIN | 3 | 15 | | | | | | | nS |
| Self refresh exit to next valid command delay | tXSR | MIN | 2 | tRFCab + 10 | | | | | | | nS |
| Exit power down to next valid command delay | tXP | MIN | 2 | 7.5 | | | | | | | nS |
| CAS to CAS delay | tCCD | MIN | 2 | 2 | | | | | | | tCK(avg) |
| Internal Read to Precharge command delay | tRTP | MIN | 2 | 7.5 | | | | | | | nS |
| RAS to CAS Delay | tRCD | Fast | 3 | 15 | | | | | | | nS |
| Row Precharge Time (single bank) | tRPpb | Fast | 3 | 15 | | | | | | | nS |
| Row Precharge Time (all banks) | tRPab 4-bank | Fast | 3 | 15 | | | | | | | nS |
| Row Active Time | tRAS | MIN | 3 | 42 | | | | | | | nS |
| | | MAX | - | 70 | | | | | | | µS |
| Write Recovery Time | tWR | MIN | 3 | 15 | | | | | | | nS |
| Internal Write to Read Command Delay | tWTR | MIN | 2 | 7.5 | | | | | 10 | | nS |
| Active bank A to Active bank B | tRRD | MIN | 2 | 10 | | | | | | | nS |
| Four Bank Activate Window | tFAW | MIN | 8 | 50 | | | | | | 60 | nS |
| Minimum Deep Power Down Time | tDPD | MIN | | 500 | | | | | | | µS |


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| Parameter | Symbol | min / max | min tCK | Data Rate | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 1066 | 933 | 800 | 667 | 533 | 400 | 333 | |
| **LPDDR2 Temperature De-Rating** | | | | | | | | | | | |
| tDQSCK De-Rating | tDQSCK (Derated) | MAX | | 5620 | 6000 | | | | | | pS |
| Core Timings Temperature De-Rating | tRCD (Derated) | MIN | | tRCD + 1.875 | | | | | | | nS |
| | tRC (Derated) | MIN | | tRC + 1.875 | | | | | | | nS |
| | tRAS (Derated) | MIN | | tRAS + 1.875 | | | | | | | nS |
| | tRP (Derated) | MIN | | tRP + 1.875 | | | | | | | nS |
| | tRRD (Derated) | MIN | | tRRD + 1.875 | | | | | | | nS |

**Notes:**

1. Input set-up/hold time for signal (CA[0:n], CS_n).
2. CKE input setup time is measured from CKE reaching high/low voltage level to CK_t/CK_c crossing.
3. CKE input hold time is measured from CK_t/CK_c crossing to CKE reaching high/low voltage level.
4. Frequency values are for reference only. Clock cycle time (tCK) shall be used to determine device capabilities.
5. To guarantee device operation before the LPDDR2 device is configured a number of AC boot timing parameters are defined in this table. Boot parameter symbols have the letter b appended, e.g. tCK during boot is tCKb.
6. Frequency values are for reference only. Clock cycle time (tCK or tCKb) shall be used to determine device capabilities.
7. The SDRAM will set some Mode register default values upon receiving a RESET (MRW) command as specified in “Mode Register Definition”.
8. The output skew parameters are measured with Ron default settings into the reference load.
9. The min tCK column applies only when tCK is greater than 6nS for LPDDR2-S4 devices.
10. All AC timings assume an input slew rate of 1V/nS.
11. Read, Write, and Input Setup and Hold values are referenced to Vref.
12. For low-to-high and high-to-low transitions, the timing reference will be at the point when the signal crosses VTT. tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ) ), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ) ). Below “HSUL_12 Driver Output Reference Load for Timing and Slew Rate” figure shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.


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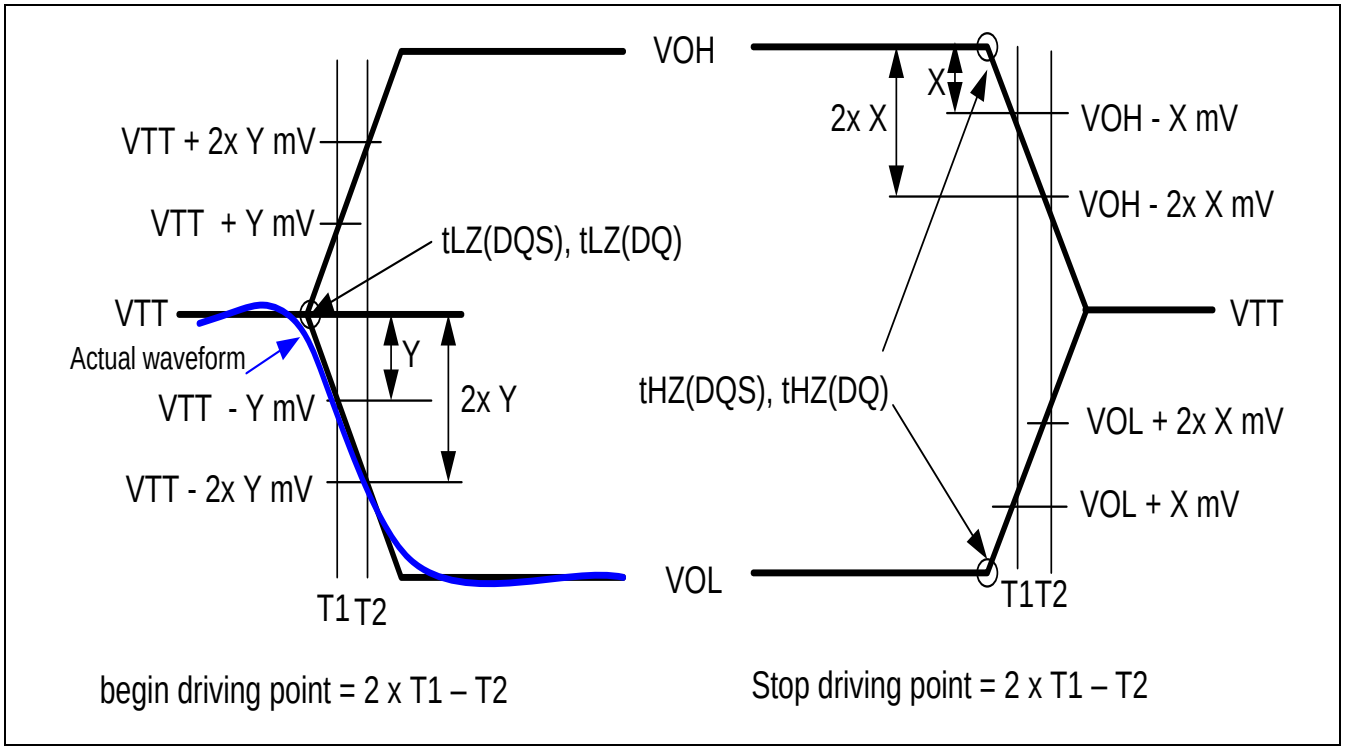



**Figure of HSUL_12 Driver Output Reference Load for Timing and Slew Rate**

The parameters $t_{LZ(DQS)}$, $t_{LZ(DQ)}$, $t_{HZ(DQS)}$, and $t_{HZ(DQ)}$ are defined as single-ended. The timing parameters $t_{RPRE}$ and $t_{RPST}$ are determined from the differential signal DQS_t-DQS_c.

13. Measured from the start driving of DQS_t - DQS_c to the start driving the first rising strobe edge.
14. Measured from the from start driving the last falling strobe edge to the stop driving DQS_t , DQS_c.
15. $t_{DQSCKDS}$ is the absolute value of the difference between any two $t_{DQSCK}$ measurements (within a byte lane) within a contiguous sequence of bursts within a 160nS rolling window. $t_{DQSCKDS}$ is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.
16. $t_{DQSCKDM}$ is the absolute value of the difference between any two $t_{DQSCK}$ measurements (within a byte lane) within a 1.6µS rolling window. $t_{DQSCKDM}$ is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.
17. $t_{DQSCKDL}$ is the absolute value of the difference between any two $t_{DQSCK}$ measurements (within a byte lane) within a 32mS rolling window. $t_{DQSCKDL}$ is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.
18. All parts list in section 3 order information table will not guarantee to meet functional and AC specification if the $t_{CK(avg)}$ out of range mentioned in above table.

### 8.7.2 CA and CS_n Setup, Hold and Derating

For all input signals (CA and CS_n) the total $t_{IS}$ (setup time) and $t_{IH}$ (hold time) required is calculated by adding the data sheet $t_{IS(base)}$ and $t_{IH(base)}$ value (see 8.7.2.1 **"CA and CS_n Setup and Hold Base-Values for 1V/nS"** table) to the $\Delta t_{IS}$ and $\Delta t_{IH}$ derating value (see 8.7.2.2 **"Derating Values LPDDR2 tIS/tIH - AC/DC Based AC220"** table). Example: $t_{IS}$ (total setup time) = $t_{IS(base)}$ + $\Delta t_{IS}$.

Setup ($t_{IS}$) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)min}$. Setup ($t_{IS}$) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)max}$. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value (see 8.7.2.4 **"Nominal Slew Rate and tVAC for Setup Time tIS for CA and CS_n with Respect to Clock"** figure). If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see 8.7.2.6 **"Tangent Line for Setup Time tIS for CA and CS_n with Respect to Clock"** figure).

Hold ($t_{IH}$) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)max}$ and the first crossing of $V_{REF(dc)}$. Hold ($t_{IH}$) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)min}$ and the first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc to $V_{REF(dc)}$ region', use nominal slew rate for derating value (see 8.7.2.5 **"Nominal Slew Rate for Hold Time tIH for CA and CS_n with Respect to Clock"** figure). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see 8.7.2.7 **"Tangent Line for Hold Time tIH for CA and CS_n with Respect to Clock"** figure).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time $t_{VAC}$ (see 8.7.2.3 **"Required Time tVAC above VIH(ac) {below VIL(ac)} for Valid Transition"** table).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in 8.7.2.2 **"Derating Values LPDDR2 tIS/tIH - AC/DC Based AC220"** table, the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

#### 8.7.2.1 CA and CS_n Setup and Hold Base-Values for 1V/nS

| Unit [pS] | LPDDR2-1066 | LPDDR2-800 | reference |
|---|---|---|---|
| $t_{IS(base)}$ | 0 | 70 | $V_{IH/L(ac)} = V_{REF(dc)} \pm 220mV$ |
| $t_{IH(base)}$ | 90 | 160 | $V_{IH/L(dc)} = V_{REF(dc)} \pm 130mV$ |

**Note:** ac/dc referenced for 1V/nS CA and CS_n slew rate and 2V/nS differential CK_t-CK_c slew rate.


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### 8.7.2.2 Derating Values LPDDR2 tIS/tIH - AC/DC Based AC220

| ΔtIS, ΔtIH derating in [pS] AC/DC based<br>AC220 Threshold -> VIH(ac)=VREF(dc)+220mV, VIL(ac)=VREF(dc)-220mV<br>DC130 Threshold -> VIH(dc)=VREF(dc)+130mV, VIL(dc)=VREF(dc)-130mV | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CA, CS_n Slew Rate V/nS | CK_t,CK_c Differential Slew Rate | | | | | | | | | | | | | | | |
| | 4.0 V/nS | | 3.0 V/nS | | 2.0 V/nS | | 1.8 V/nS | | 1.6 V/nS | | 1.4 V/nS | | 1.2 V/nS | | 1.0 V/nS | |
| | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH |
| 2.0 | 110 | 65 | 110 | 65 | 110 | 65 | - | - | - | - | - | - | - | - | - | - |
| 1.5 | 74 | 43 | 73 | 43 | 73 | 43 | 89 | 59 | - | - | - | - | - | - | - | - |
| 1.0 | 0 | 0 | 0 | 0 | 0 | 0 | 16 | 16 | 32 | 32 | - | - | - | - | - | - |
| 0.9 | - | - | -3 | -5 | -3 | -5 | 13 | 11 | 29 | 27 | 45 | 43 | - | - | - | - |
| 0.8 | - | - | - | - | -8 | -13 | 8 | 3 | 24 | 19 | 40 | 35 | 56 | 55 | - | - |
| 0.7 | - | - | - | - | - | - | 2 | -6 | 18 | 10 | 34 | 26 | 50 | 46 | 66 | 78 |
| 0.6 | - | - | - | - | - | - | - | - | 10 | -3 | 26 | 13 | 42 | 33 | 58 | 65 |
| 0.5 | - | - | - | - | - | - | - | - | - | - | 4 | -4 | 20 | 16 | 36 | 48 |
| 0.4 | - | - | - | - | - | - | - | - | - | - | - | - | -7 | 2 | 17 | 34 |

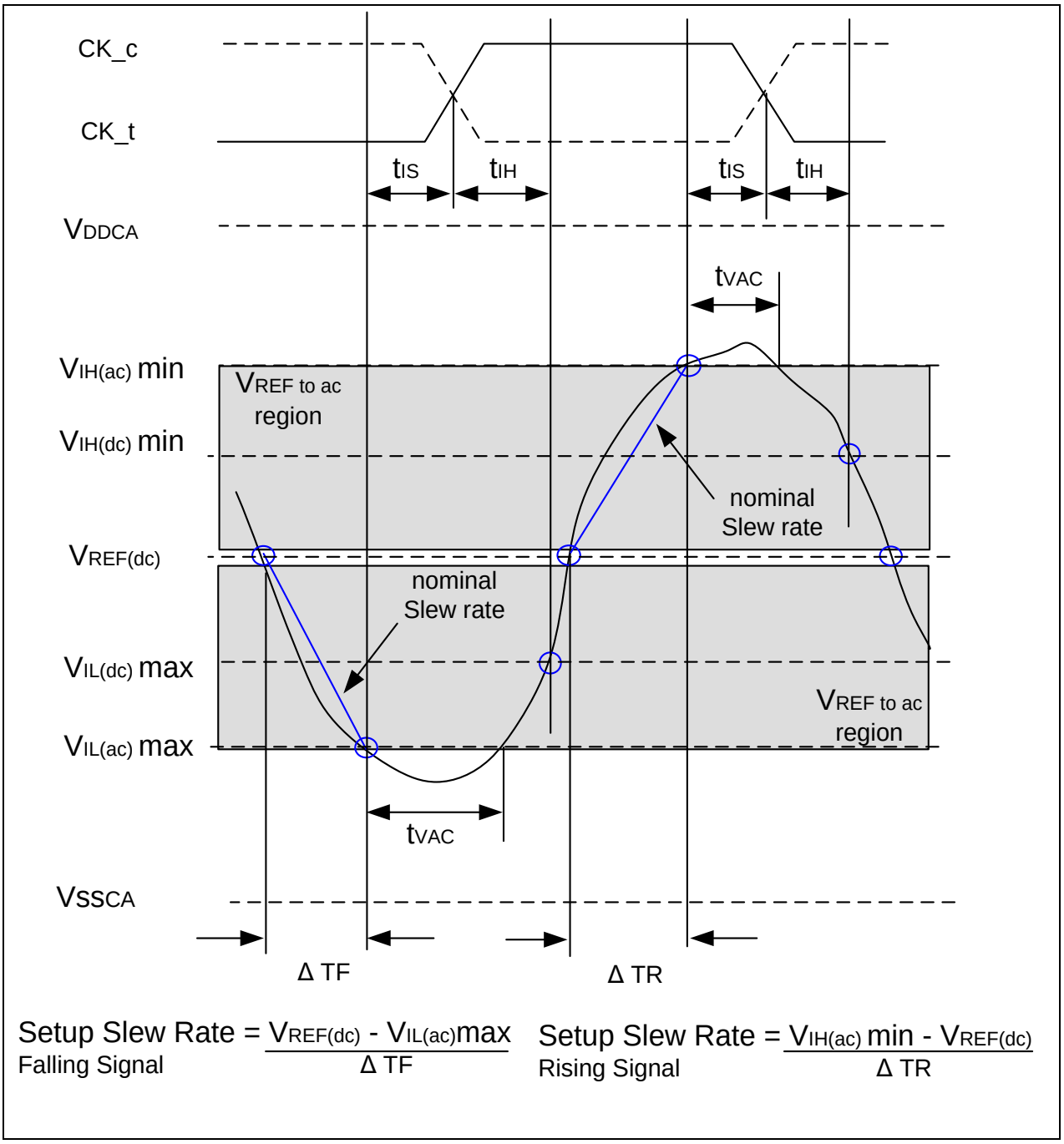
**Note:** Cell contents '-' are defined as not supported.

### 8.7.2.3 Required Time tVAC above VIH(ac) {below VIL(ac)} for Valid Transition

| Slew Rate [V/nS] | tVAC @ 220mV [pS] | |
|---|---|---|
| | min | max |
| > 2.0 | 175 | - |
| 2.0 | 170 | - |
| 1.5 | 167 | - |
| 1.0 | 163 | - |
| 0.9 | 162 | - |
| 0.8 | 161 | - |
| 0.7 | 159 | - |
| 0.6 | 155 | - |
| 0.5 | 150 | - |
| <0.5 | 150 | - |


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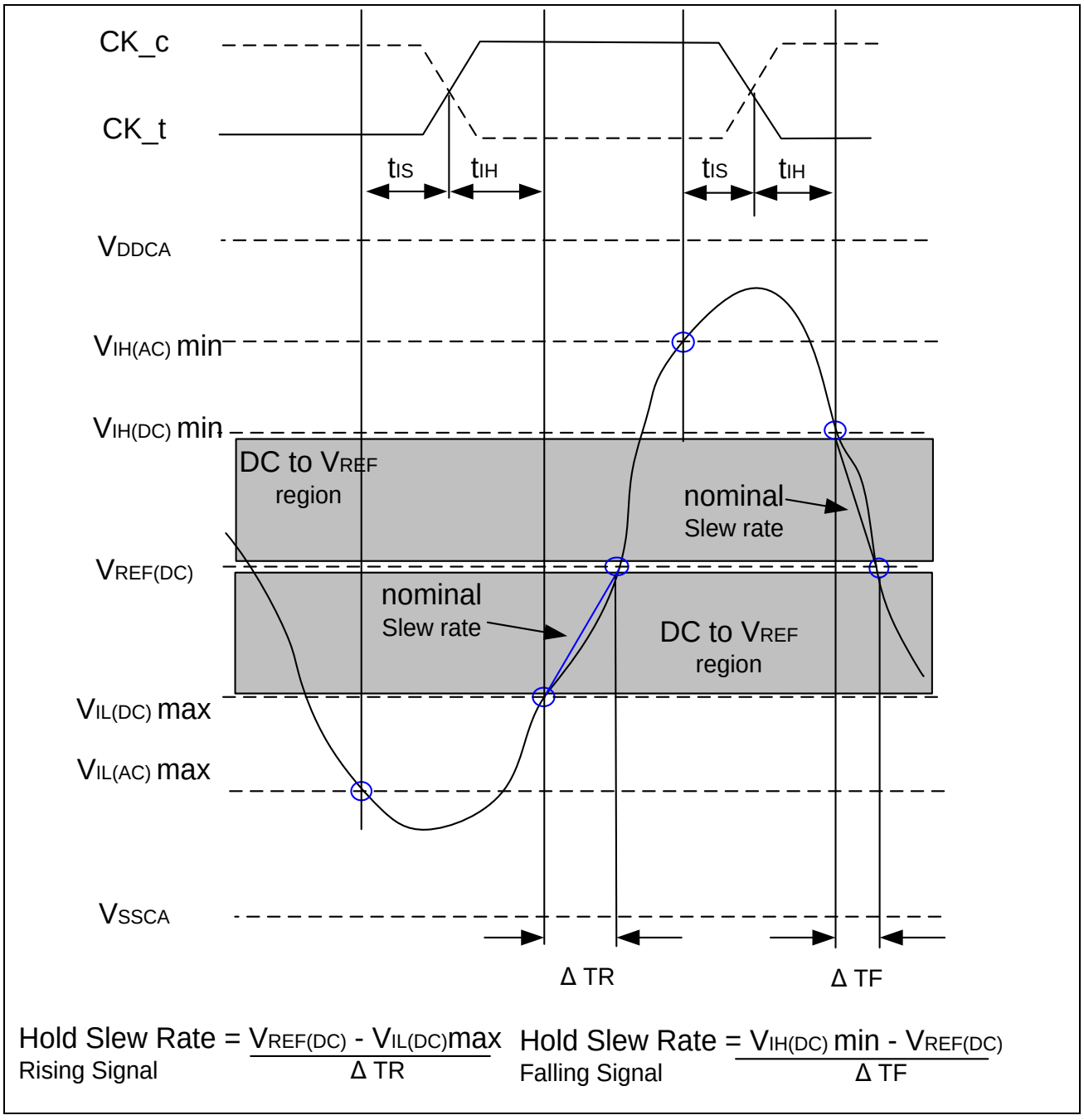
#### 8.7.2.4 Nominal Slew Rate and tVAC for Setup Time tIS for CA and CS_n with Respect to Clock





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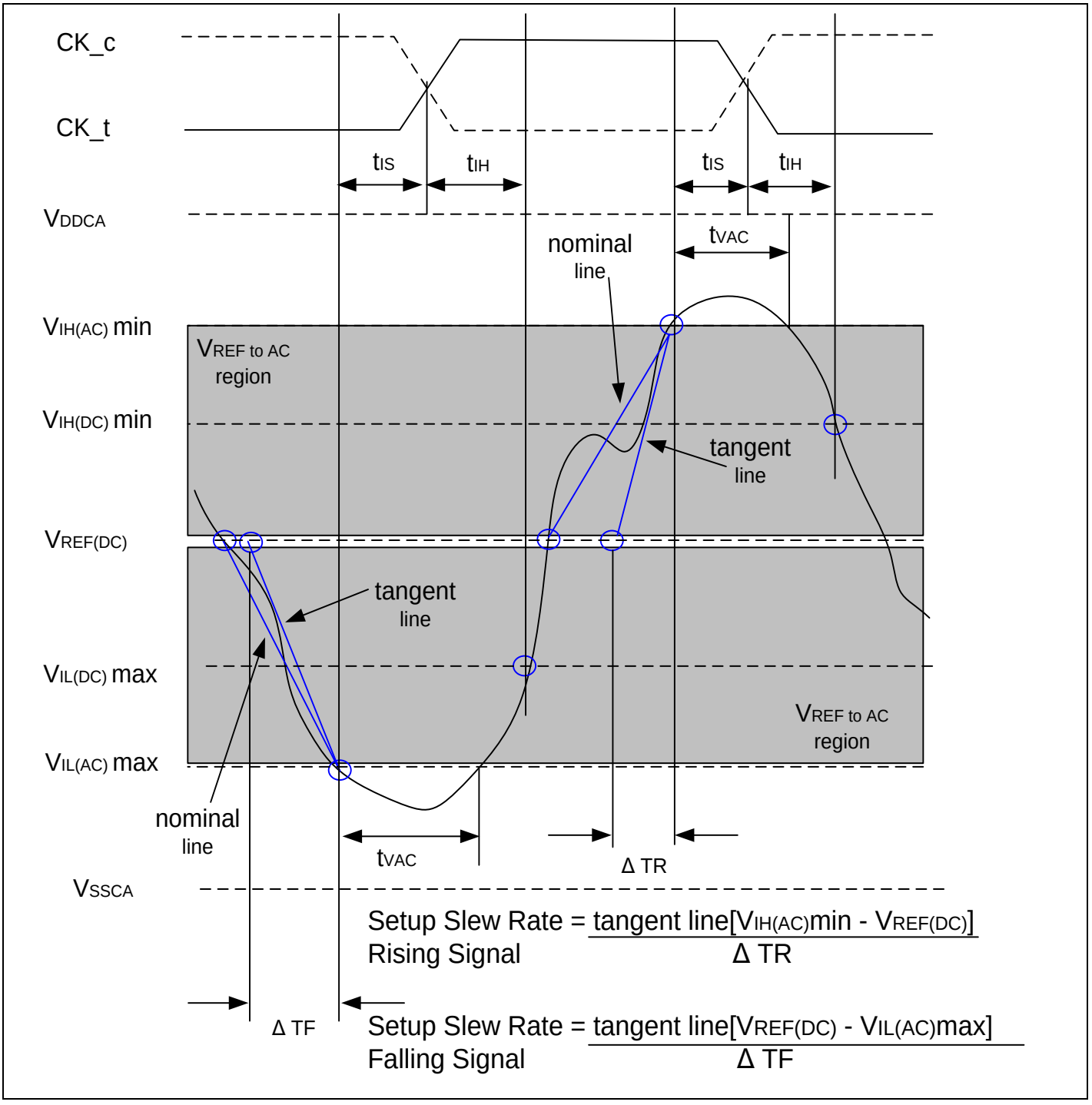
### 8.7.2.5 Nominal Slew Rate for Hold Time tIH for CA and CS_n with Respect to Clock





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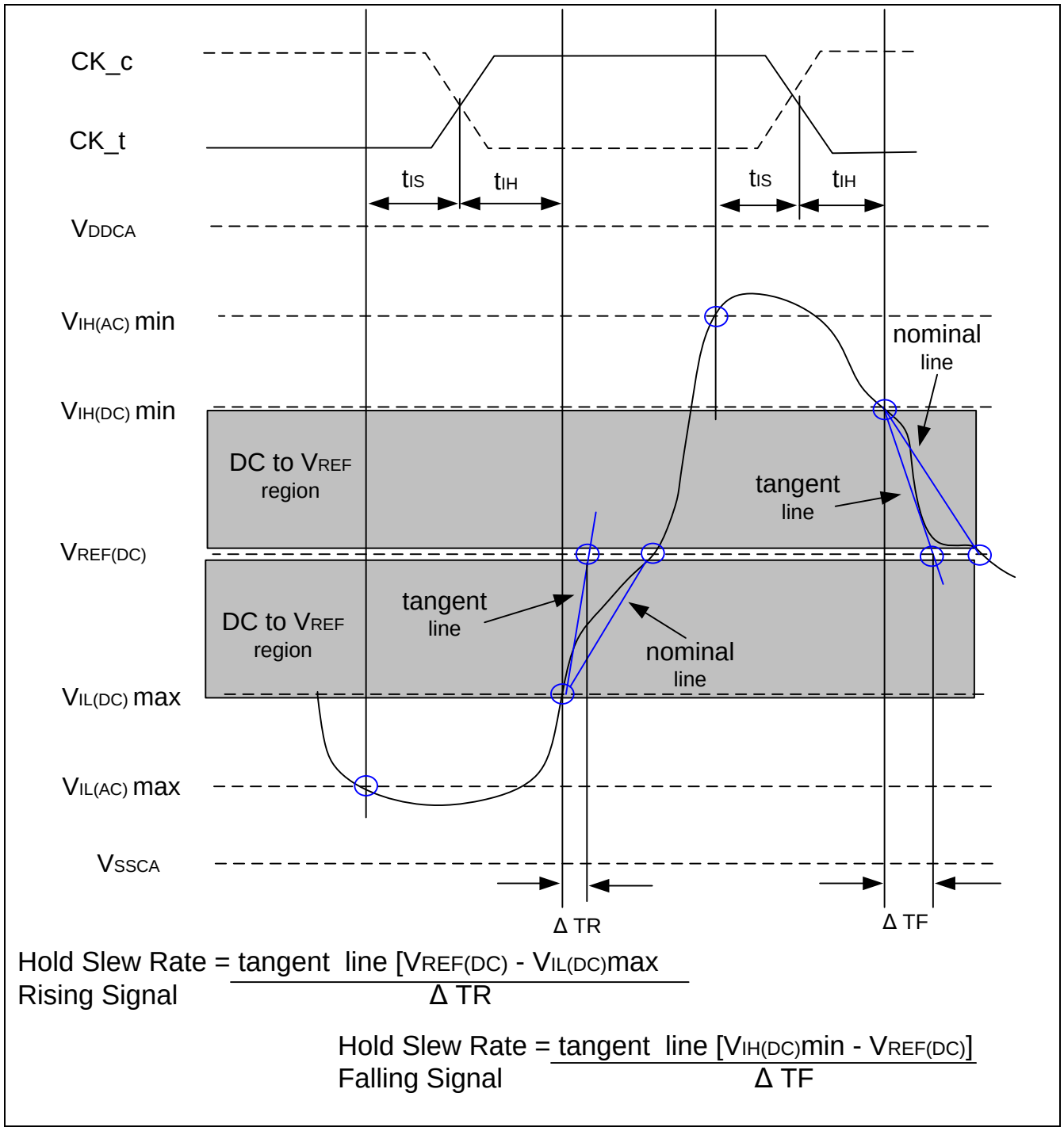
### 8.7.2.6 Tangent Line for Setup Time tIS for CA and CS_n with Respect to Clock





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### 8.7.2.7 Tangent Line for Hold Time $t_{IH}$ for CA and CS_n with Respect to Clock




$$\text{Hold Slew Rate}_{\text{Rising Signal}} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(DC)}\text{max}}{\Delta \text{ TR}}$$

$$\text{Hold Slew Rate}_{\text{Falling Signal}} = \frac{\text{tangent line } [V_{IH(DC)}\text{min} - V_{REF(DC)}]}{\Delta \text{ TF}}$$


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### 8.7.3 Data Setup, Hold and Slew Rate Derating

For all input signals (DQ, DM) the total $t_{DS}$ (setup time) and $t_{DH}$ (hold time) required is calculated by adding the data sheet $t_{DS(base)}$ and $t_{DH(base)}$ value (see 8.7.3.1 **"Data Setup and Hold Base-Values"** table) to the $\Delta t_{DS}$ and $\Delta t_{DH}$ (see 8.7.3.2 **"Derating Values LPDDR2 tDS/tDH - AC/DC Based AC220"** table) derating value respectively. Example: $t_{DS}$ (total setup time) = $t_{DS}$(base) + $\Delta t_{DS}$.

Setup ($t_{DS}$) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)min}$. Setup ($t_{DS}$) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)maX}$ (see 8.7.3.4 **"Nominal Slew Rate and tVAC for Setup Time tDS for DQ with Respect to Strobe"** figure). If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see 8.7.3.6 **"Tangent Line for Setup Time tDS for DQ with Respect to Strobe"** figure).

Hold ($t_{DH}$) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)}$max and the first crossing of $V_{REF(dc)}$. Hold ($t_{DH}$) nominal slew rate for a falling sig5nal is defined as the slew rate between the last crossing of $V_{IH(dc)min}$ and the first crossing of $V_{REF(dc)}$ (see 8.7.3.5 **"Nominal Slew Rate for Hold time tDH for DQ with Respect to Strobe"** figure). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see 8.7.3.7 **"Tangent Line for Hold Time tDH for DQ with Respect to Strobe"** figure).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time $t_{VAC}$ (see 8.7.3.3 **"Required Time tVAC above VIH(ac) {below VIL(ac)} for Valid Transition"** table).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in 8.7.3.2 **"Derating Values LPDDR2 tDS/tDH - AC/DC Based AC220"** table, the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

#### 8.7.3.1 Data Setup and Hold Base-Values

| Unit [pS] | LPDDR2-1066 | LPDDR2-800 | reference |
|---|---|---|---|
| $t_{DS(base)}$ | -10 | 50 | $V_{IH/L(ac)} = V_{REF(dc)} \pm 220mV$ |
| $t_{DH(base)}$ | 80 | 140 | $V_{IH/L(dc)} = V_{REF(dc)} \pm 130mV$ |

**Note:** ac/dc referenced for 1V/nS DQ,DM slew rate and 2V/nS differential DQS_t-DQS_c slew rate.


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### 8.7.3.2 Derating Values LPDDR2 tDS/tDH - AC/DC Based AC220

| ΔtDS, ΔDH derating in [pS] AC/DC based a<br>AC220 Threshold -> VIH(ac) = VREF(dc) + 220mV, VIL(ac) = VREF(dc) - 220mV<br>DC130 Threshold -> VIH(dc) = VREF(dc) + 130mV, VIL(dc) = VREF(dc) - 130mV | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DQ, DM Slew Rate V/nS | DQS_t, DQS_c Differential Slew Rate | | | | | | | | | | | | | | | |
| | 4.0 V/nS | | 3.0 V/nS | | 2.0 V/nS | | 1.8 V/nS | | 1.6 V/nS | | 1.4 V/nS | | 1.2 V/nS | | 1.0 V/nS | |
| | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH |
| 2.0 | 110 | 65 | 110 | 65 | 110 | 65 | - | - | - | - | - | - | - | - | - | - |
| 1.5 | 74 | 43 | 73 | 43 | 73 | 43 | 89 | 59 | - | - | - | - | - | - | - | - |
| 1.0 | 0 | 0 | 0 | 0 | 0 | 0 | 16 | 16 | 32 | 32 | - | - | - | - | - | - |
| 0.9 | - | - | -3 | -5 | -3 | -5 | 13 | 11 | 29 | 27 | 45 | 43 | - | - | - | - |
| 0.8 | - | - | - | - | -8 | -13 | 8 | 3 | 24 | 19 | 40 | 35 | 56 | 55 | - | - |
| 0.7 | - | - | - | - | - | - | 2 | -6 | 18 | 10 | 34 | 26 | 50 | 46 | 66 | 78 |
| 0.6 | - | - | - | - | - | - | - | - | 10 | -3 | 26 | 13 | 42 | 33 | 58 | 65 |
| 0.5 | - | - | - | - | - | - | - | - | - | - | 4 | -4 | 20 | 16 | 36 | 48 |
| 0.4 | - | - | - | - | - | - | - | - | - | - | - | - | -7 | 2 | 17 | 34 |

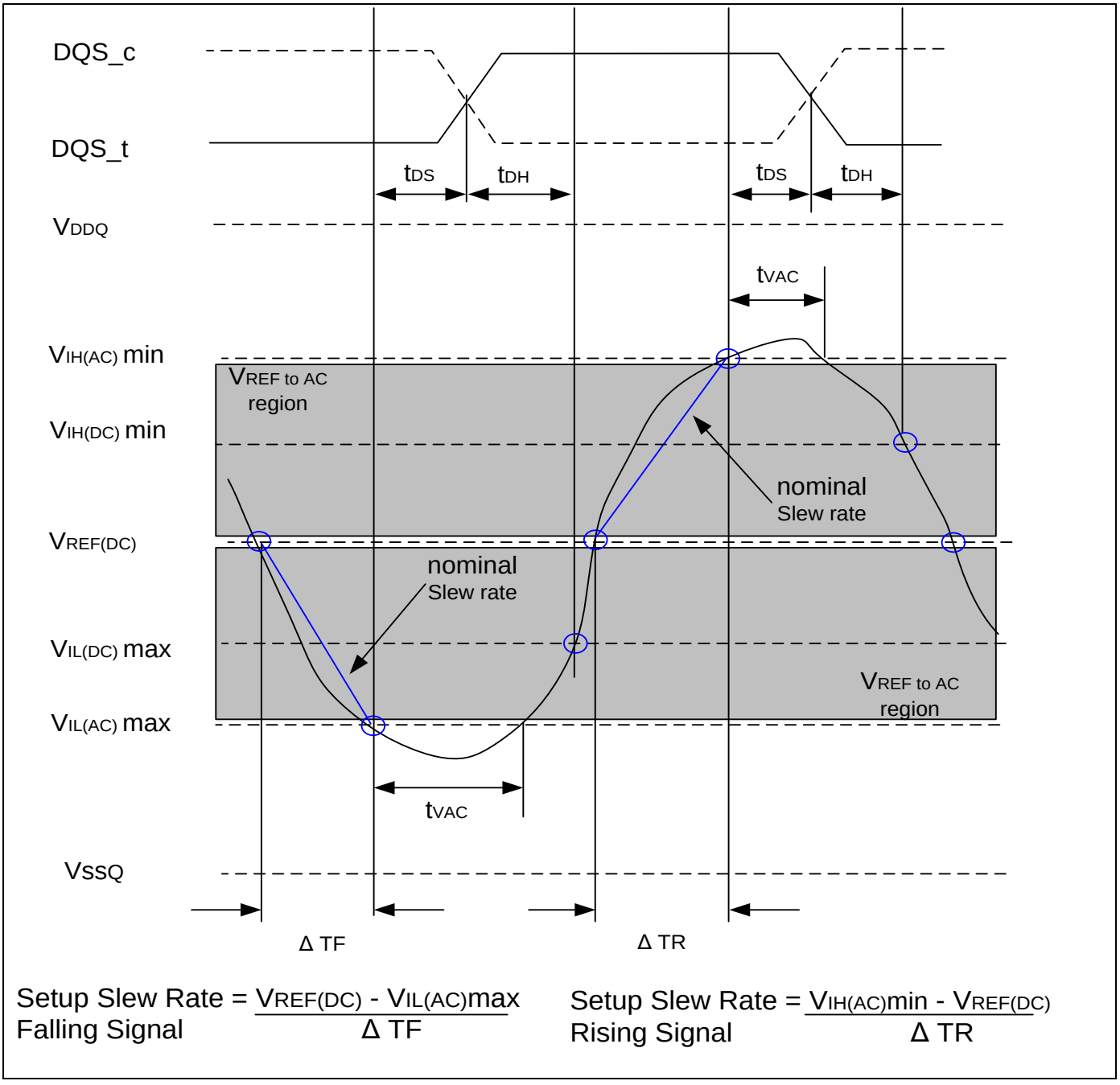
**Note:** Cell contents '-' are defined as not supported.

### 8.7.3.3 Required Time tVAC above VIH(ac) {below VIL(ac)} for Valid Transition

| Slew Rate [V/nS] | tVAC @ 220mV [pS] | |
|---|---|---|
| | min | max |
| > 2.0 | 175 | - |
| 2.0 | 170 | - |
| 1.5 | 167 | - |
| 1.0 | 163 | - |
| 0.9 | 162 | - |
| 0.8 | 161 | - |
| 0.7 | 159 | - |
| 0.6 | 155 | - |
| 0.5 | 150 | - |
| <0.5 | 150 | - |


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#### 8.7.3.4 Nominal Slew Rate and tVAC for Setup Time tDS for DQ with Respect to Strobe

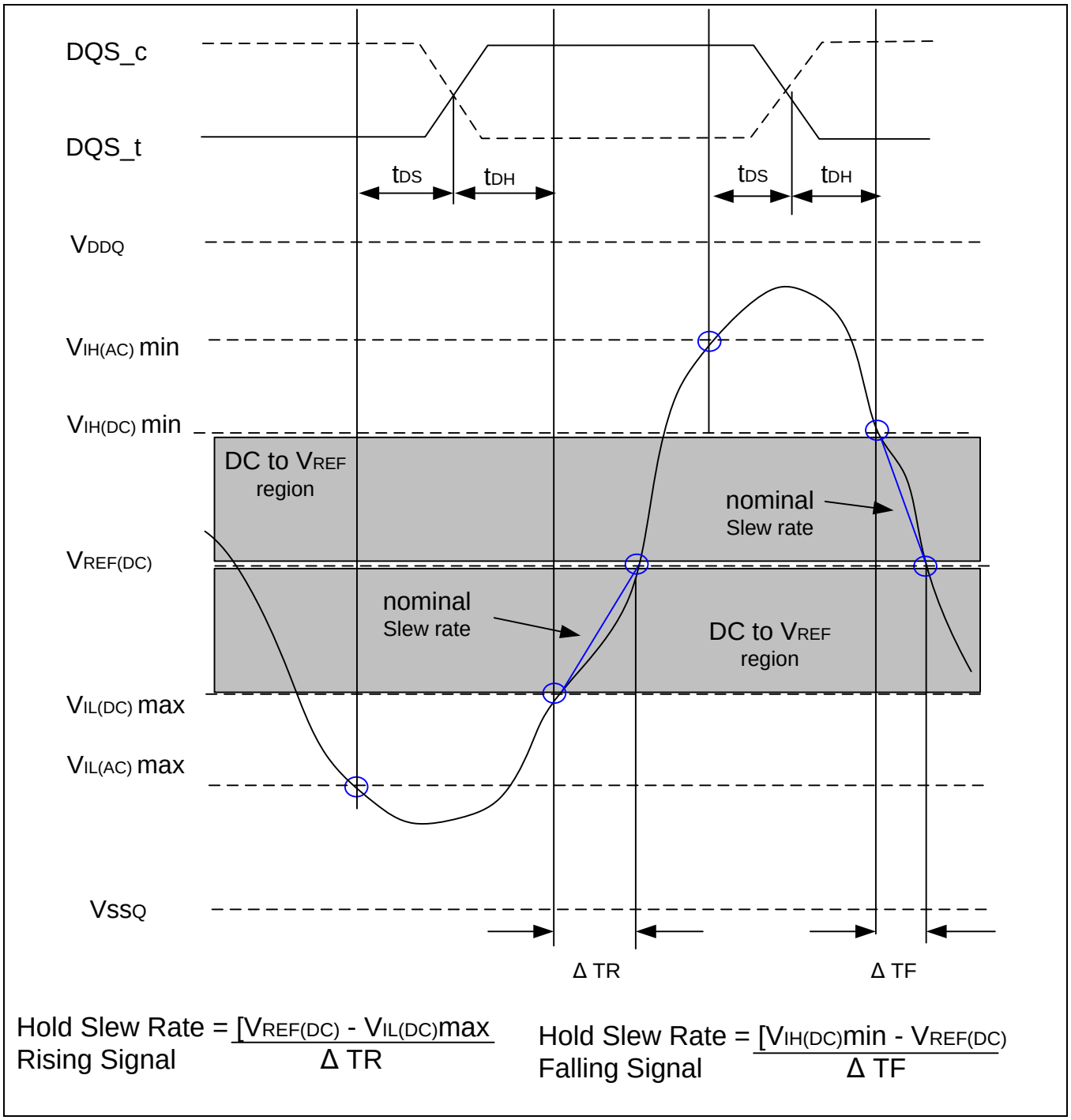



Setup Slew Rate = $\frac{V_{REF(DC)} - V_{IL(AC)max}}{\Delta TF}$ Falling Signal

Setup Slew Rate = $\frac{V_{IH(AC)min} - V_{REF(DC)}}{\Delta TR}$ Rising Signal


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### 8.7.3.5 Nominal Slew Rate for Hold time tDH for DQ with Respect to Strobe

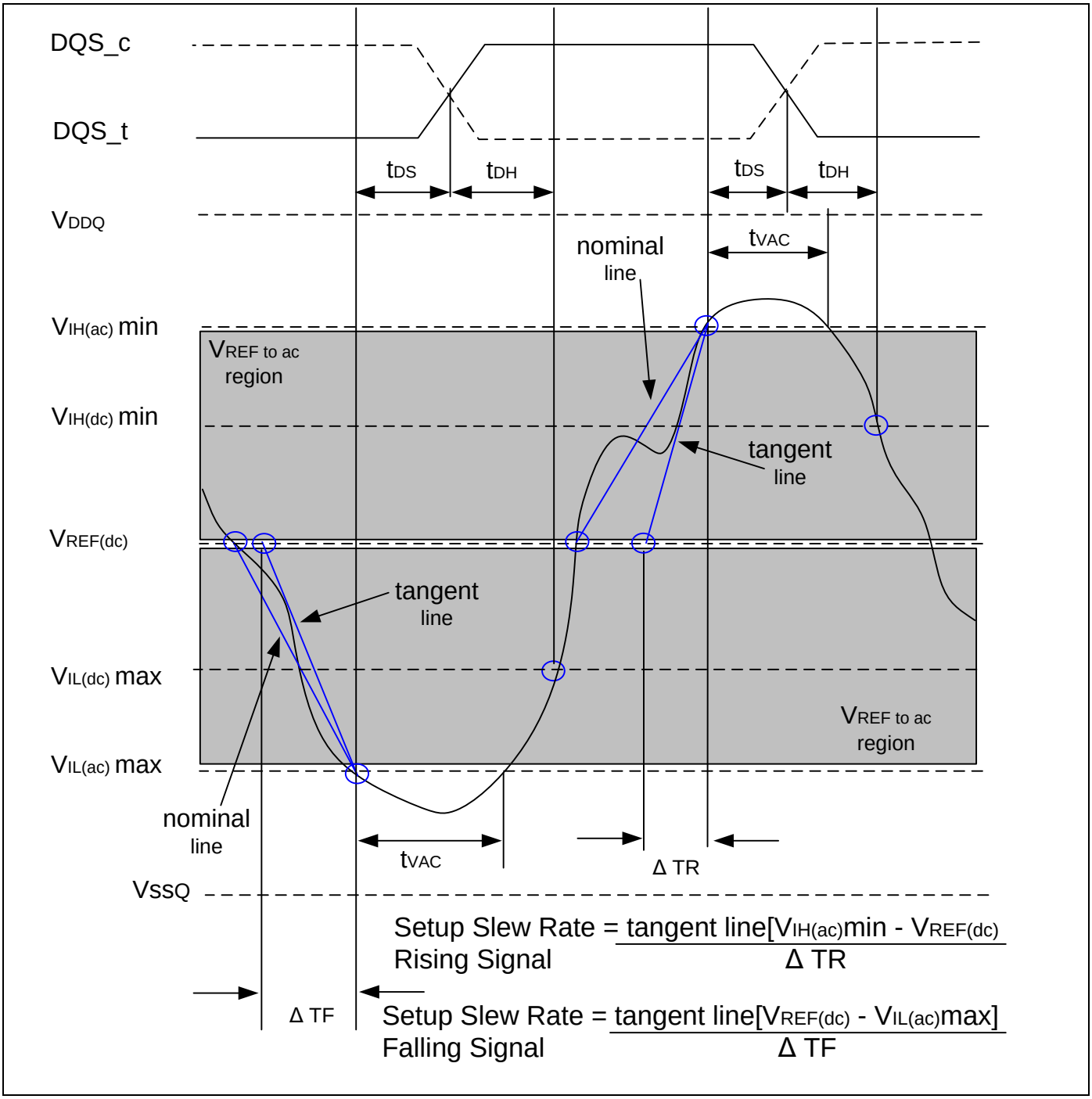



$$\text{Hold Slew Rate}_{\text{Rising Signal}} = \frac{[V_{REF(DC)} - V_{IL(DC)}\text{max}}{\Delta\ TR}$$

$$\text{Hold Slew Rate}_{\text{Falling Signal}} = \frac{[V_{IH(DC)}\text{min} - V_{REF(DC)}}{\Delta\ TF}$$


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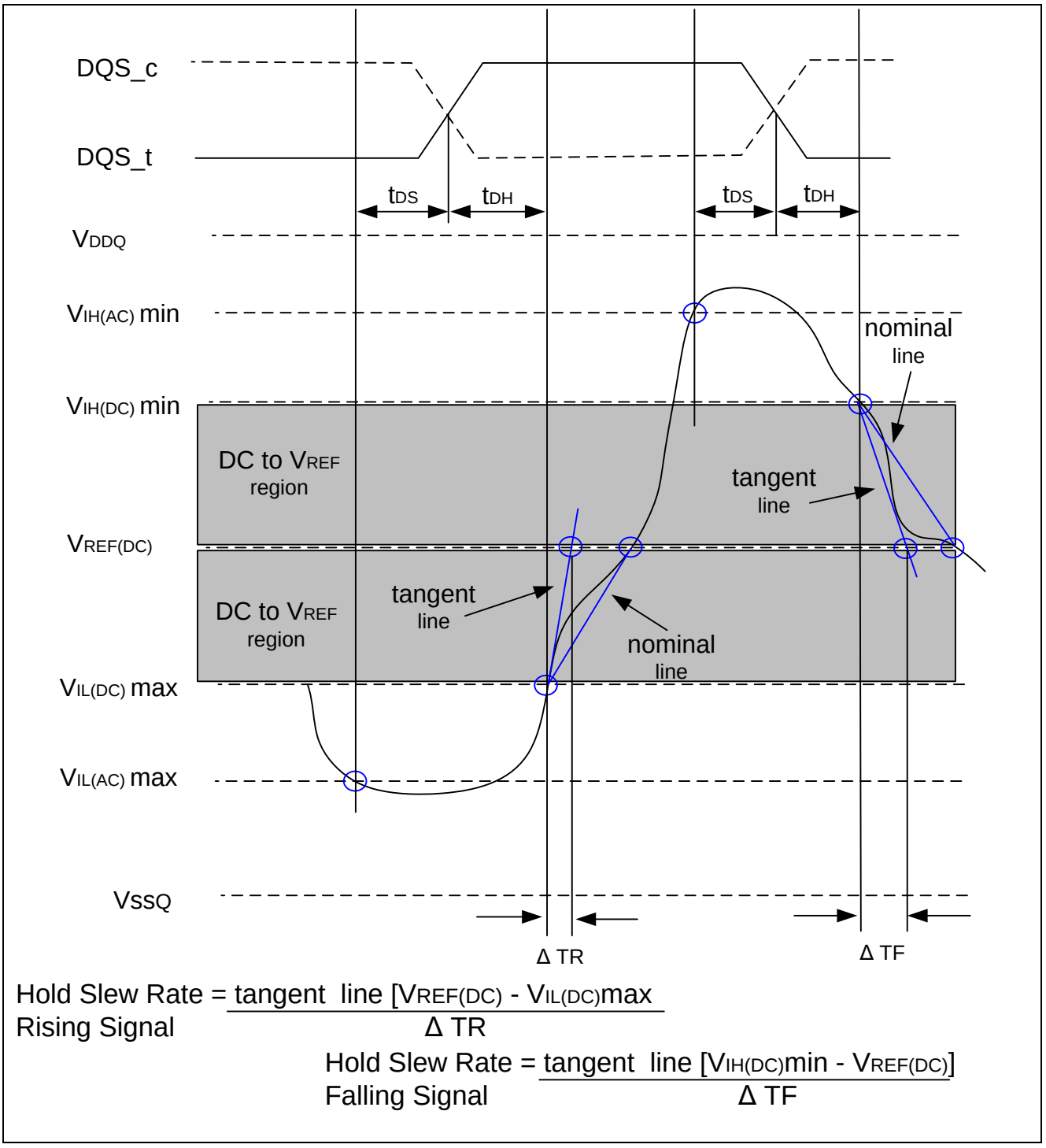
### 8.7.3.6 Tangent Line for Setup Time tDS for DQ with Respect to Strobe





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### 8.7.3.7 Tangent Line for Hold Time tDH for DQ with Respect to Strobe



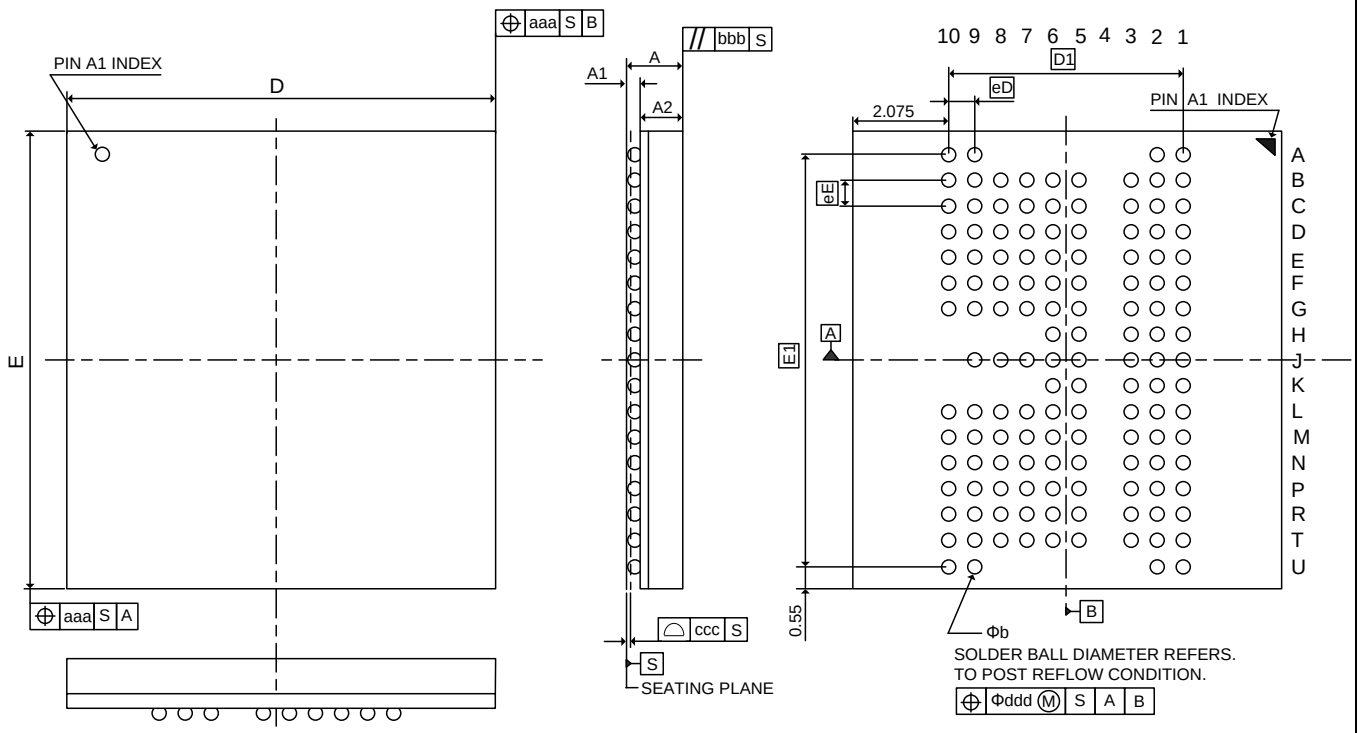

$$\text{Hold Slew Rate}_{\text{Rising Signal}} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(DC)}\text{max}}{\Delta \text{ TR}}$$

$$\text{Hold Slew Rate}_{\text{Falling Signal}} = \frac{\text{tangent line } [V_{IH(DC)}\text{min} - V_{REF(DC)}]}{\Delta \text{ TF}}$$

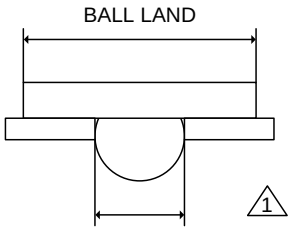

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## 9. PACKAGE DIMENSIONS

### Package Outline VFBGA 134 Ball (10x11.5 mm$^2$, Ball pitch: 0.65mm, Ø=0.40mm)




| SYMBOL | DIMENSION (MM) | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.27 | 0.32 | 0.37 |
| A2 | 0.53 | 0.58 | 0.63 |
| b | 0.35 | 0.40 | 0.45 |
| D | 9.90 | 10.00 | 10.10 |
| E | 11.40 | 11.50 | 11.60 |
| D1 | 5.85 BSC. | | |
| E1 | 10.40 BSC. | | |
| eD | 0.65 BSC. | | |
| eE | 0.65 BSC. | | |
| aaa | 0.15 | | |
| bbb | --- | --- | 0.10 |
| ccc | --- | --- | 0.08 |
| ddd | --- | --- | 0.08 |




**Note:**
1. Ball land: 0.45mm, Ball opening: 0.35mm.
2. PCB Ball land suggested ≤ 0.35mm.


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## 10. REVISION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---|---|---|---|
| A01-001 | May 22, 2014 | All | Initial formal datasheet |
| A01-002 | Jun. 28, 2019 | 6 | Remove eight WFBGA168 part numbers in order information |
| | | 7 | Remove WFBGA168 ball assignment figure |
| | | 118 | Remove WFBGA168 package outline drawing figure |

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