16M × 8 BANKS × 8 BIT DDR3 SDRAM

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1. GENERAL DESCRIPTION

The W631GG8MB is a 1G bits DDR3 SDRAM, organized as 16,777,216 words × 8 banks × 8 bits. This device achieves high speed transfer rates up to 2133 MT/s (DDR3-2133) for various applications. This device is sorted into the following speed grades: -09, -11, -12, -15, 09I, 11I, 12I, 15I, 09J, 11J, 12J and 15J.

The -09 ,09I and 09J speed grades are compliant to the DDR3-2133 (14-14-14) specification (The 09I industrial grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 95°C, the 09J industrial plus grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 105°C).

The -11 ,11I and 11J speed grades are compliant to the DDR3-1866 (13-13-13) specification (The 11I industrial grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 95°C, the 11J industrial plus grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 105°C).

The -12, 12I and 12J speed grades are compliant to the DDR3-1600 (11-11-11) specification (The 12I industrial grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 95°C, the 12J industrial plus grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 105°C).

The -15, 15I and 15J speed grades are compliant to the DDR3-1333 (9-9-9) specification (The 15I industrial grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 95°C, the 15J industrial plus grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 105°C).

The W631GG8MB is designed to comply with the following key DDR3 SDRAM features such as posted CAS#, programmable CAS# Write Latency (CWL), ZQ calibration, on die termination and asynchronous reset. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and CK# falling). All I/Os are synchronized with a differential DQS-DQS# pair in a source synchronous fashion.

2. FEATURES

- Power Supply: V_{DD}, V_{DDQ} = 1.5V ± 0.075V
- Double Data Rate architecture: two data transfers per clock cycle
- Eight internal banks for concurrent operation
- 8 bit prefetch architecture
- CAS Latency: 5, 6, 7, 8, 9, 10, 11, 13 and 14
- Burst length 8 (BL8) and burst chop 4 (BC4) modes: fixed via mode register (MRS) or selectable On-The-Fly (OTF)
- Programmable read burst ordering: interleaved or nibble sequential
- Bi-directional, differential data strobes (DQS and DQS#) are transmitted / received with data
- Edge-aligned with read data and center-aligned with write data
- DLL aligns DQ and DQS transitions with clock
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge, data and data mask are referenced to both edges of a differential data strobe pair (double data rate)
- Posted CAS with programmable additive latency (AL = 0, CL - 1 and CL - 2) for improved command, address and data bus efficiency
- Read Latency = Additive Latency plus CAS Latency (RL = AL + CL)
- Auto-precharge operation for read and write bursts

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- Refresh, Self-Refresh, Auto Self-refresh (ASR) and Partial array self refresh (PASR)
- Precharged Power Down and Active Power Down
- Data masks (DM) for write data
- Programmable CAS Write Latency (CWL) per operating frequency
- Write Latency WL = AL + CWL
- Multi purpose register (MPR) for readout a predefined system timing calibration bit sequence
- System level timing calibration support via write leveling and MPR read pattern
- ZQ Calibration for output driver and ODT using external reference resistor to ground
- Asynchronous RESET# pin for Power-up initialization sequence and reset function
- Programmable on-die termination (ODT) for data, data mask and differential strobe pairs
- Dynamic ODT mode for improved signal integrity and preselectable termination impedances during writes
- 1K Byte page size
- Interface: SSTL_15
- Packaged in VFBGA 78 Ball (8x10.5 mm^2 with thickness of 1.0 mm), using lead free materials with RoHS compliant

3. ORDER INFORMATION

PART NUMBER	SPEED GRADE	OPERATING TEMPERATURE
W631GG8MB-09	DDR3-2133 (14-14-14)	0°C ≤ T_{CASE} ≤ 95°C
W631GG8MB09I	DDR3-2133 (14-14-14)	-40°C ≤ T_{CASE} ≤ 95°C
W631GG8MB09J	DDR3-2133 (14-14-14)	-40°C ≤ T_{CASE} ≤ 105°C
W631GG8MB-11	DDR3-1866 (13-13-13)	0°C ≤ T_{CASE} ≤ 95°C
W631GG8MB11I	DDR3-1866 (13-13-13)	-40°C ≤ T_{CASE} ≤ 95°C
W631GG8MB11J	DDR3-1866 (13-13-13)	-40°C ≤ T_{CASE} ≤ 105°C
W631GG8MB-12	DDR3-1600 (11-11-11)	0°C ≤ T_{CASE} ≤ 95°C
W631GG8MB12I	DDR3-1600 (11-11-11)	-40°C ≤ T_{CASE} ≤ 95°C
W631GG8MB12J	DDR3-1600 (11-11-11)	-40°C ≤ T_{CASE} ≤ 105°C
W631GG8MB-15	DDR3-1333 (9-9-9)	0°C ≤ T_{CASE} ≤ 95°C
W631GG8MB15I	DDR3-1333 (9-9-9)	-40°C ≤ T_{CASE} ≤ 95°C
W631GG8MB15J	DDR3-1333 (9-9-9)	-40°C ≤ T_{CASE} ≤ 105°C

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4. KEY PARAMETERS

Speed Bin			DDR3-2133		DDR3-1866		DDR3-1600		DDR3-1333		Unit
CL-nRCD-nRP			14-14-14		13-13-13		11-11-11		9-9-9		
Part Number Extension			-09/09I/09J		-11/11I/11J		-12/12I/12J		-15/15I/15J		
Parameter		Sym.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum operating frequency using maximum allowed settings for Sup_CL and Sup_CWL		f_{CKMAX}	–	1066	–	933	–	800	–	667	MHz
Internal read command to first data		t_{AA}	13.09	20	13.91	20	13.75 (13.125)*5	20	13.5 (13.125)*5	20	nS
ACT to internal read or write delay time		t_{RCD}	13.09	–	13.91	–	13.75 (13.125)*5	–	13.5 (13.125)*5	–	nS
PRE command period		t_{RP}	13.09	–	13.91	–	13.75 (13.125)*5	–	13.5 (13.125)*5	–	nS
ACT to ACT or REF command period		t_{RC}	46.09	–	47.91	–	48.75 (48.125)*5	–	49.5 (49.125)*5	–	nS
ACT to PRE command period		t_{RAS}	33	9 * t_{REFI}	34	9 * t_{REFI}	35	9 * t_{REFI}	36	9 * t_{REFI}	nS
CL = 5	CWL = 5	$t_{CK(AVG)}$	3.0	3.3	3.0	3.3	3.0	3.3	3.0	3.3	nS
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	2.5	3.3	nS
CL = 7	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	Reserved		1.875	< 2.5	1.875	< 2.5	nS
CL = 8	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	nS
CL = 9	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	Reserved		1.5	< 1.875	1.5	< 1.875	nS
CL = 10	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	nS
CL = 11	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	Reserved		1.25	< 1.5	Reserved		nS
CL = 13	CWL = 9	$t_{CK(AVG)}$	1.07	< 1.25	1.07	< 1.25	Reserved		Reserved		nS
CL = 14	CWL = 10	$t_{CK(AVG)}$	0.938	< 1.07	Reserved		Reserved		Reserved		nS
Supported CL Settings		Sup_CL	5, 6, 7, 8, 9, 10, 11, 13, 14		5, 6, 8, 10, 13		5, 6, (7), 8, (9), 10, 11		5, 6, (7), 8, 9, 10		nCK
Supported CWL Settings		Sup_CWL	5, 6, 7, 8, 9, 10		5, 6, 7, 9		5, 6, 7, 8		5, 6, 7		nCK
Average periodic refresh Interval	-40°C ≤ T_{CASE} ≤ 85°C	t_{REFI}	–	7.8*2, 3	–	7.8*2, 3	–	7.8*2, 3	–	7.8*2, 3	µS
	0°C ≤ T_{CASE} ≤ 85°C		–	7.8*1	–	7.8*1	–	7.8*1	–	7.8*1	µS
	85°C < T_{CASE} ≤ 95°C		–	3.9*4	–	3.9*4	–	3.9*4	–	3.9*4	µS
	95°C < T_{CASE} ≤ 105°C		–	3.9*4	–	3.9*4	–	3.9*4	–	3.9*4	µS
Operating One Bank Active-Precharge Current		I_{DD0}	–	130	–	115	–	105	–	95	mA
Operating One Bank Active-Read-Precharge Current		I_{DD1}	–	160	–	140	–	130	–	115	mA
Operating Burst Read Current		I_{DD4R}	–	170	–	150	–	140	–	120	mA
Operating Burst Write Current		I_{DD4W}	–	190	–	170	–	150	–	130	mA
Burst Refresh Current		I_{DD5B}	–	170	–	160	–	150	–	140	mA
Normal Temperature Self-Refresh Current		I_{DD6}	–	10	–	10	–	10	–	10	mA
Operating Bank Interleave Current		I_{DD7}	–	245	–	215	–	195	–	175	mA

Notes: (Field value contents in blue font or parentheses are optional AC parameter and CL setting)

1. All speed grades support 0°C ≤ T_{CASE} ≤ 85°C with full JEDEC AC and DC specifications.
2. The -09, -11, -12 and -15 speed grades, -40°C ≤ T_{CASE} < 0°C is not available.
3. The 09I, 09J, 11I, 11J, 12I, 12J, 15I and 15J speed grades support -40°C ≤ T_{CASE} ≤ 85°C with full JEDEC AC and DC specifications.
4. The -09, 09I, -11, 11I, -12, 12I, -15 and 15I speed grades, T_{CASE} is able to extend to 95°C. The 09J, 11J, 12J and 15J speed grades, T_{CASE} is able to extend to 105°C. They are with doubling Auto Refresh commands in frequency to a 32 mS period (t_{REFI} = 3.9 µS), it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0_b and MR2 A7 = 1_b) or enable the Auto Self-Refresh mode (ASR) (MR2 A6 = 1_b, MR2 A7 is don't care).
5. For devices supporting optional down binning to CL=7 and CL=9, t_{AA}/t_{RCD}/t_{RP} min must be 13.125 nS or lower. SPD settings must be programmed to match. For example, DDR3-1333 (9-9-9) devices supporting down binning to DDR3-1066 (7-7-7) should program 13.125 nS in SPD bytes for t_{AA}min (Byte 16), t_{RCD}min (Byte 18), and t_{RP}min (Byte 20). DDR3-1600 (11-11-11) devices supporting down binning to DDR3-1333 (9-9-9) or DDR3-1066 (7-7-7) should program 13.125 nS in SPD bytes for t_{AA}min (Byte16), t_{RCD}min (Byte 18), and t_{RP}min (Byte 20). Once t_{RP} (Byte 20) is programmed to 13.125 nS, t_{RC}min (Byte 21, 23) also should be programmed accordingly. For example, 49.125nS (t_{RAS}min + t_{RP}min = 36 nS + 13.125 nS) for DDR3-1333 (9-9-9) and 48.125 nS (t_{RAS}min + t_{RP}min = 35 nS + 13.125 nS) for DDR3-1600 (11-11-11).

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5. BALL CONFIGURATION

1	2	3	4	5	6	7	8	9
VSS	VDD	NC		A		NU/TDQS#	VSS	VDD
VSS	VSSQ	DQ0		B		DM/TDQS	VSSQ	VDDQ
VDDQ	DQ2	DQS		C		DQ1	DQ3	VSSQ
VSSQ	DQ6	DQS#		D		VDD	VSS	VSSQ
VREFDQ	VDDQ	DQ4		E		DQ7	DQ5	VDDQ
NC	VSS	RAS#		F		CK	VSS	NC
ODT	VDD	CAS#		G		CK#	VDD	CKE
NC	CS#	WE#		H		A10/AP	ZQ	NC
VSS	BA0	BA2		J		NC	VREFCA	VSS
VDD	A3	A0		K		A12/BC#	BA1	VDD
VSS	A5	A2		L		A1	A4	VSS
VDD	A7	A9		M		A11	A6	VDD
VSS	RESET#	A13		N		NC	A8	VSS

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6. BALL DESCRIPTION

BALL NUMBER	SYMBOL	TYPE	DESCRIPTION
F7, G7	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
G9	CKE	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power Down and Self-Refresh operation (all banks idle), or Active Power Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After V_{REFCA} and V_{REFDQ} have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE, are disabled during power down. Input buffers, excluding CKE, are disabled during Self-Refresh.
H2	CS#	Input	Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.
G1	ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQS, DQS# and DM/TDQS, NU/TDQS# (When TDQS is enabled via Mode Register A11=1 in MR1) signal. The ODT signal will be ignored if Mode Registers MR1 and MR2 are programmed to disable ODT and during Self Refresh.
F3, G3, H3	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
B7	DM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. The function of DM or TDQS/TDQS# is enabled by Mode Register A11 setting in MR1.
J2, K8, J3	BA0−BA2	Input	Bank Address Inputs: BA0−BA2 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
K3, L7, L3, K2, L8, L2, M8, M2, N8, M3, H7, M7, K7, N3	A0−A13	Input	Address Inputs: Provide the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC# have additional functions; see below). The address inputs also provide the op-code during Mode Register Set command. Row address: A0−A13. Column address: A0−A9.
H7	A10/AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Auto-precharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Auto-precharge; LOW: no Auto-precharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
K7	A12/BC#	Input	Burst Chop: A12/BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See section 9.1 **"Command Truth Table"** on page 94 for details.
N2	RESET#	Input	Active Low Asynchronous Reset: Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD}, RESET# active is destructive to data contents.

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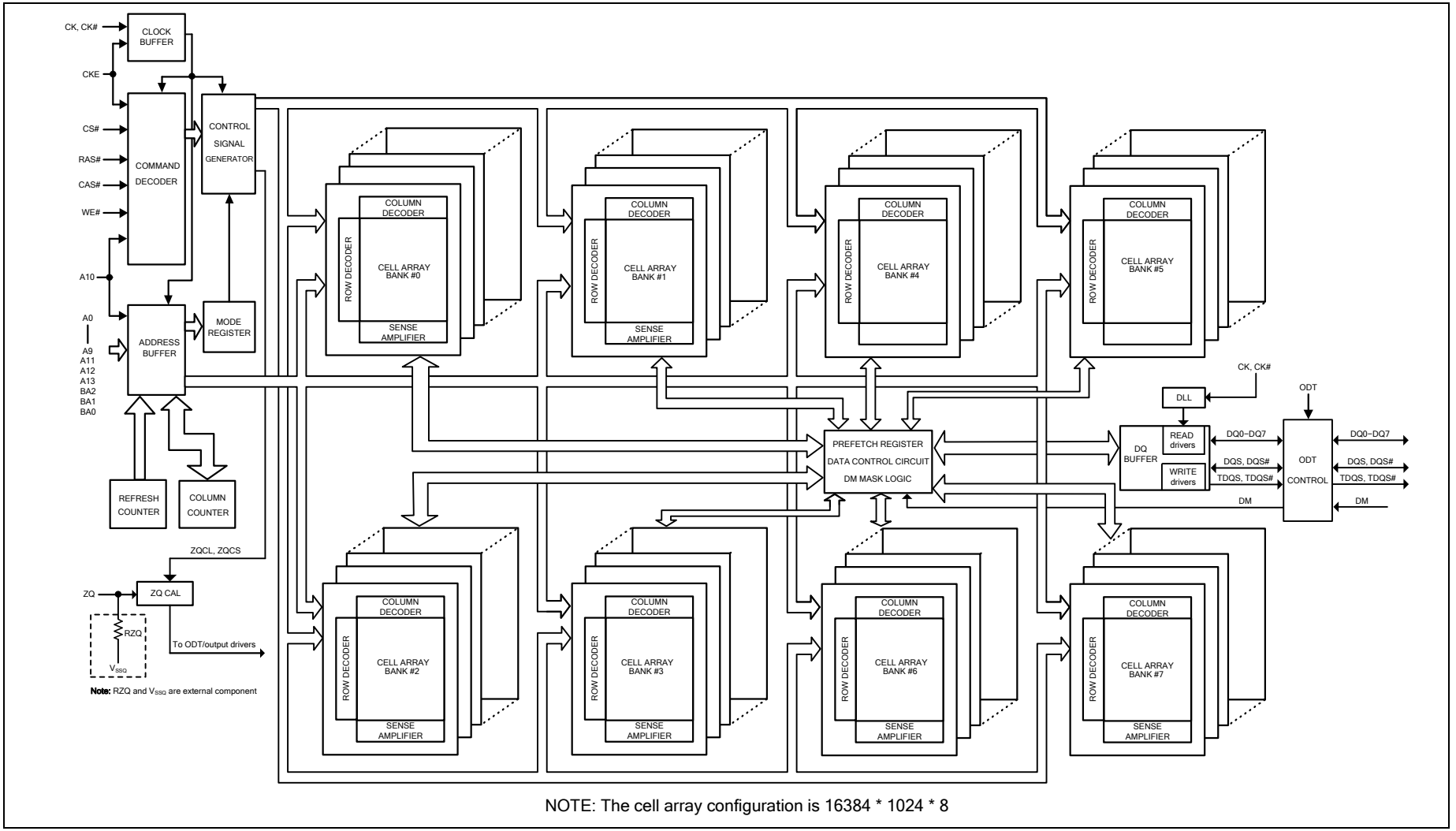
B3, C7,C2, C8, E3, E8, D2, E7	DQ0−DQ7	Input/Output	Data Input/Output: Bi-directional data bus.
C3, D3	DQS, DQS#	Input/Output	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. DQS is paired with DQS# to provide differential pair signaling to the system during read and write data transfer. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
B7, A7	TDQS, TDQS#	Output	Termination Data Strobe: When TDQS enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/TDQS# that is applied to DQS/DQS#. When TDQS disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and TDQS# is not used.
A2, A9, D7, G2, G8, K1, K9, M1, M9	VDD	Supply	Power Supply: 1.5V ± 0.075V.
A1, A8, B1, D8, F2, F8, J1, J9, L1, L9, N1, N9	VSS	Supply	Ground.
B9, C1, E2, E9	VDDQ	Supply	DQ Power Supply: 1.5V ± 0.075V.
B2, B8, C9, D1, D9	VSSQ	Supply	DQ Ground.
E1	VREFDQ	Supply	Reference voltage for DQ.
J8	VREFCA	Supply	Reference voltage for Control, Command and Address inputs.
H8	ZQ	Supply	External reference ball for output drive and On-Die Termination Impedance calibration: This ball needs an external 240Ω ± 1% external resistor (RZQ), connected from this ball to ground to perform ZQ calibration.
A3, F1, F9, H1, H9, J7, N7	NC		No Connect: No internal electrical connection is present.

Note:

Input only balls (BA0-BA2, A0-A13, RAS#, CAS#, WE#, CS#, CKE, ODT and RESET#) do not supply termination.

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7. BLOCK DIAGRAM



NOTE: The cell array configuration is 16384 * 1024 * 8

8. FUNCTIONAL DESCRIPTION

8.1 Basic Functionality

The DDR3 SDRAM is a high-speed dynamic random-access memory internally configured as an eight-bank DRAM. The DDR3 SDRAM uses an 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated (BA0-BA2 select the bank; A0-A13 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

8.2 RESET and Initialization Procedure

8.2.1 Power-up Initialization Sequence

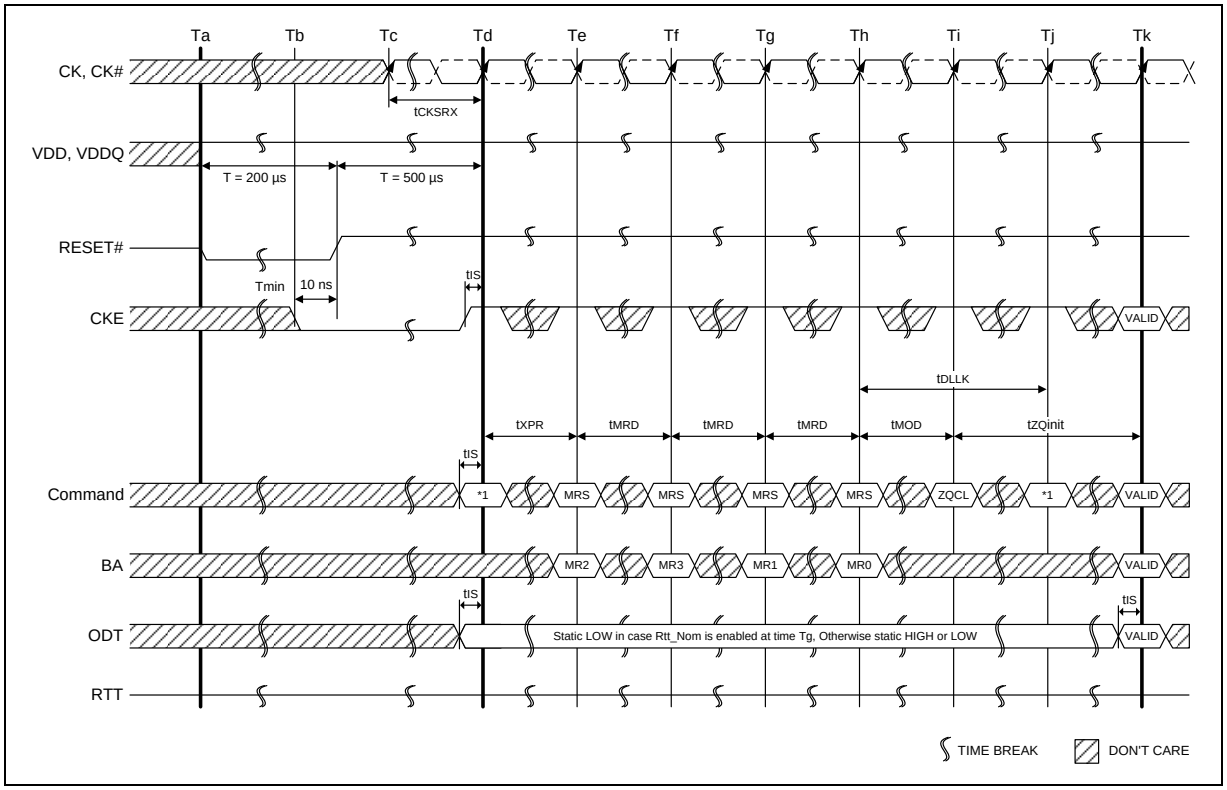
The following sequence is required for POWER UP and Initialization.

1. Apply power (RESET# is recommended to be maintained below 0.2 * V_{DD}; all other inputs may be undefined). RESET# needs to be maintained for minimum 200 µS with stable power. CKE is pulled "Low" anytime before RESET# being de-asserted (min. time 10 nS). The power voltage ramp time between 300 mV to V_{DD} min. must be no greater than 200 mS; and during the ramp, $V_{DD} \geq V_{DDQ}$ and (V_{DD} - V_{DDQ}) < 0.3 Volts.
   - V_{DD} and V_{DDQ} are driven from a single power converter output, AND
   - The voltage levels on all pins other than V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side. In addition, V_{TT} is limited to 0.95 V max once power ramp is finished, AND
   - V_{REF} tracks $V_{DDQ}/2$.

   OR
   - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}.
   - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} & V_{REF}.
   - The voltage levels on all pins other than V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.
2. After RESET# is de-asserted, wait for another 500 µS until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clocks (CK, CK#) need to be started and stabilized for at least 10 nS or 5 t_{CK} (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (t_{IS}) must be met. Also, a NOP or Deselect command must be registered (with t_{IS} set up time to clock) before CKE goes active. Once the CKE is registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of t_{DLLK} and t_{ZQinit}.

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4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as RESET# is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after RESET# deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If Rtt_Nom is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. (tXPR=max (tXS ; 5 * tCK)
6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide “Low” to BA0 and BA2, “High” to BA1.)
7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide “Low” to BA2, “High” to BA0 and BA1.)
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue “DLL Enable” command, provide “Low” to A0, “High” to BA0 and “Low” to BA1-BA2).
9. Issue MRS Command to load MR0 with all application settings and “DLL reset”. (To issue DLL reset command, provide “High” to A8 and “Low” to BA0-2).
10. Issue ZQCL command to starting ZQ calibration.
11. Wait for both tDLLK and tZQinit completed.
12. The DDR3 SDRAM is now ready for normal operation.



Note:

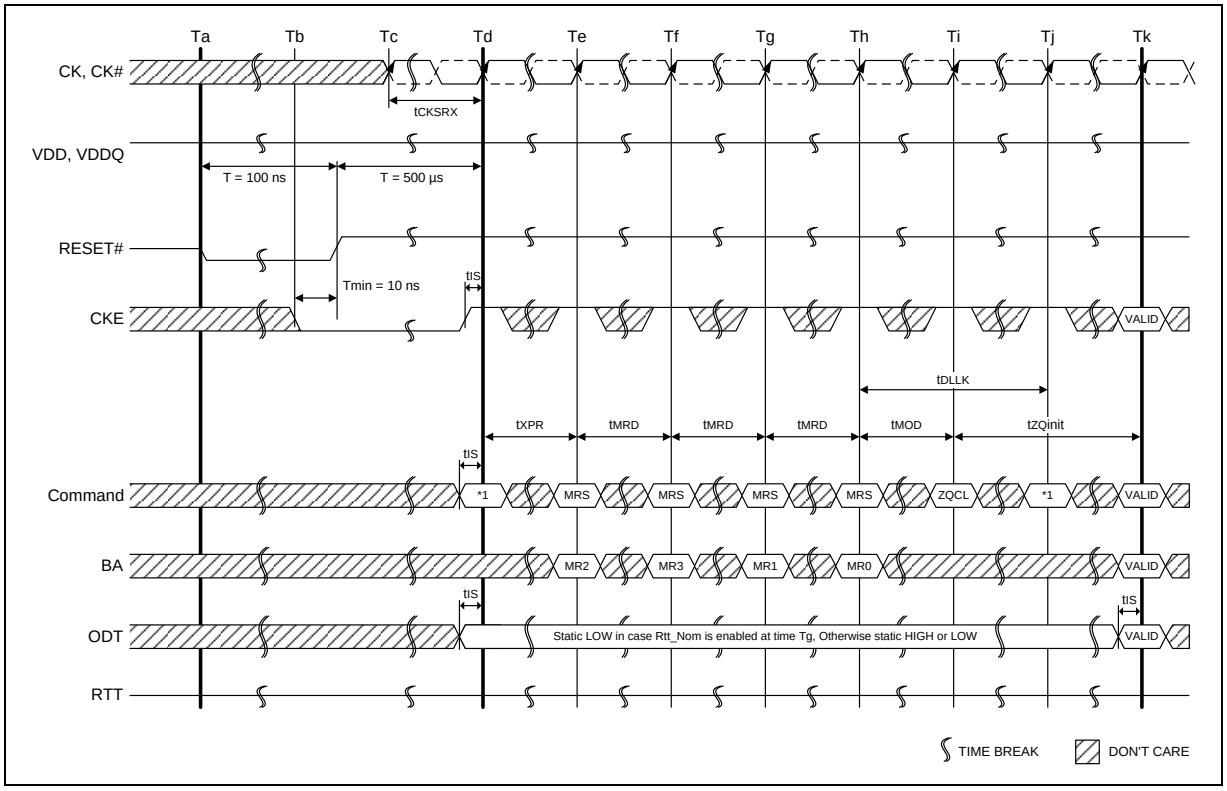
1. From time point “Td” until “Tk” NOP or DES commands must be applied between MRS and ZQCL commands.

Figure 1 – Reset and Initialization Sequence at Power-on Ramping

8.2.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below 0.2 * VDD anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100 nS. CKE is pulled “LOW” before RESET being de-asserted (min. time 10 nS).
2. Follow Power-up Initialization Sequence steps 2 to 11.
3. The Reset sequence is now completed; DDR3 SDRAM is ready for normal operation.



Note:

1. From time point “Td” until “Tk” NOP or DES commands must be applied between MRS and ZQCL commands.

Figure 2 – Reset Procedure at Power Stable Condition

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8.3 Programming the Mode Registers

For application flexibility, various functions, features, and modes are programmable in four Mode Registers, provided by the DDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (MR#) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e., written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which mean these commands can be executed any time after power-up without affecting the array contents.

The mode register set command cycle time, t_{MRD} is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in Figure 3.

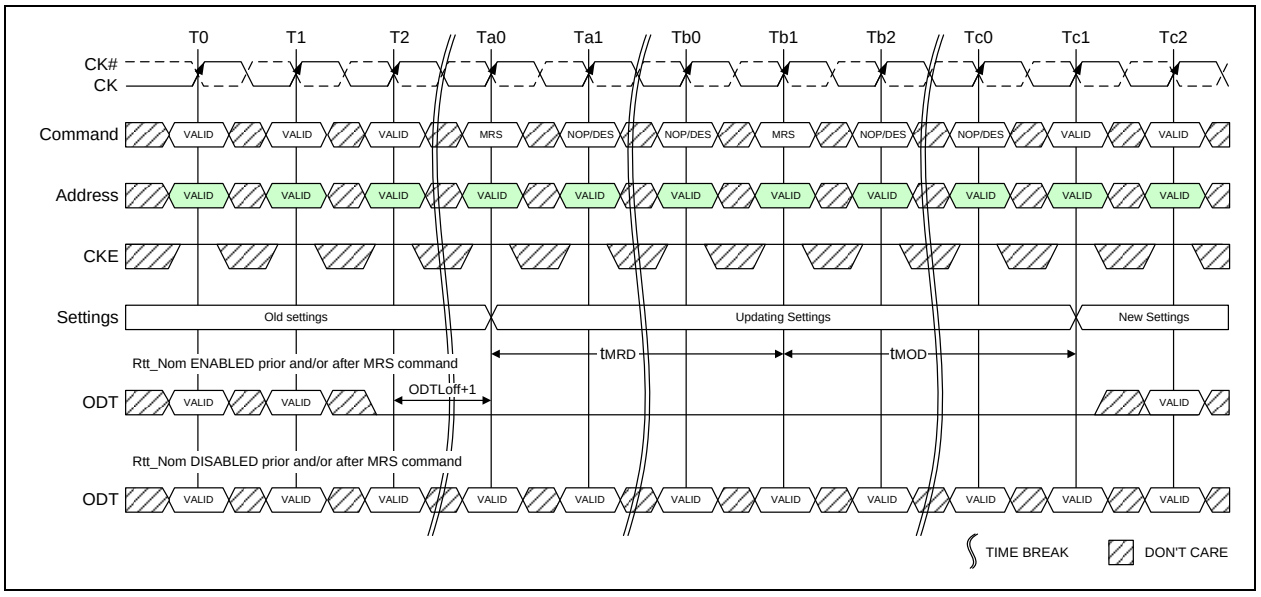


Figure 3 – t_{MRD} Timing

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The MRS command to Non-MRS command delay, tMOD is required for the DRAM to update the features, except DLL reset, and is the minimum time required from a MRS command to a non-MRS command excluding NOP and DES shown in Figure 4.

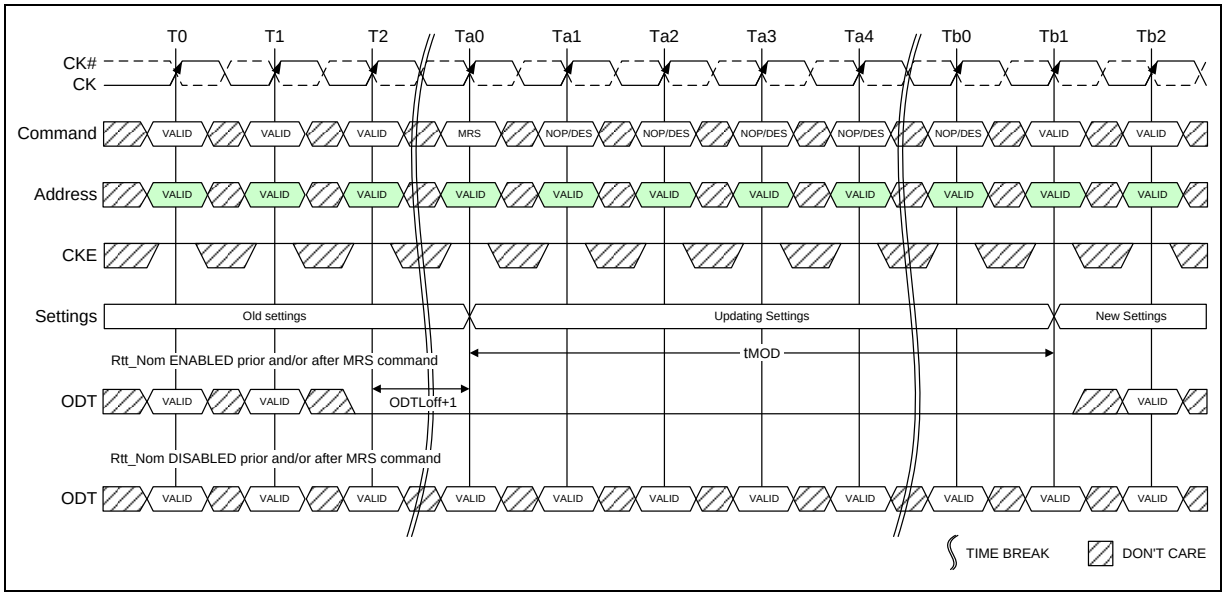


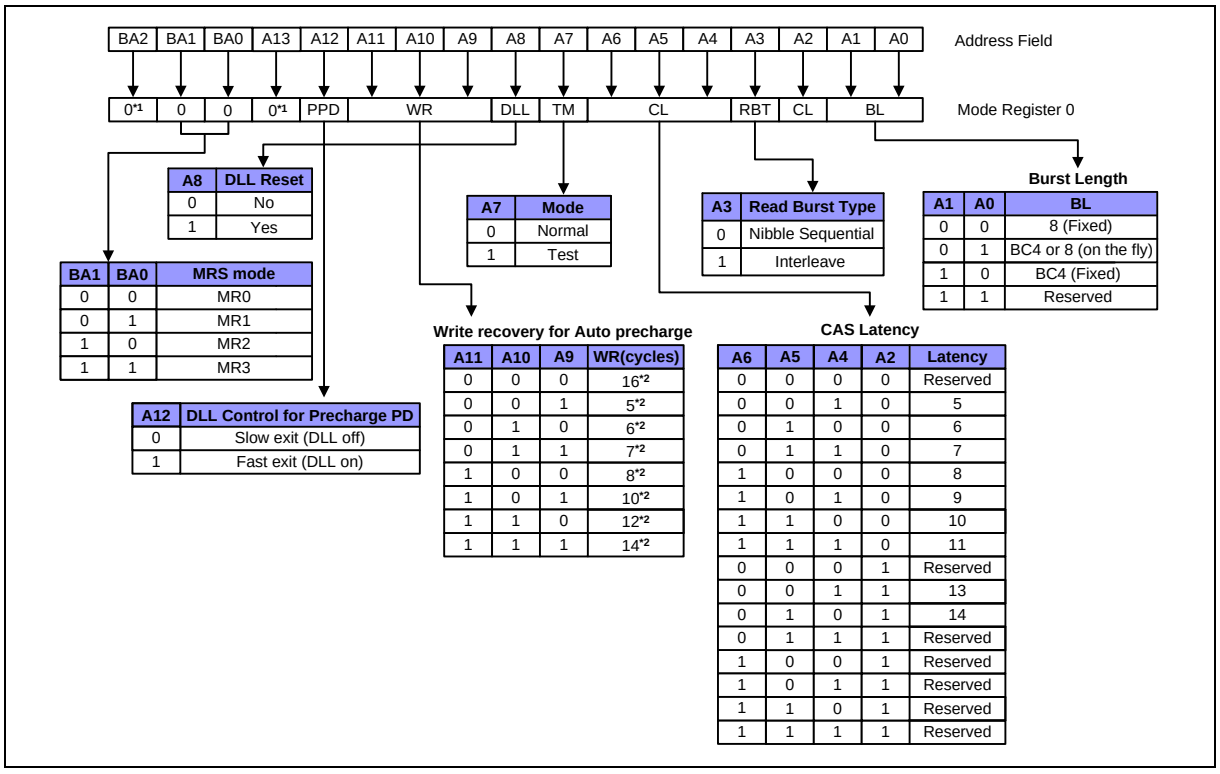
Figure 4 – tMOD Timing

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. If the Rtt_Nom Feature is enabled in the Mode Register prior and/or after a MRS command, the ODT signal must continuously be registered LOW ensuring RTT is in an off state prior to the MRS command. The ODT signal may be registered high after tMOD has expired. If the Rtt_Nom feature is disabled in the Mode Register prior and after a MRS command, the ODT signal can be registered either LOW or HIGH before, during and after the MRS command. The mode registers are divided into various fields depending on the functionality and/or modes.

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8.3.1 Mode Register MR0

The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge Power Down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0, BA1 and BA2, while controlling the states of address pins according to the Figure 5 below.



Notes:

1. BA2 and A13 are reserved for future use and must be programmed to "0" during MRS.
2. WR (write recovery for Auto precharge)min in clock cycles is calculated by dividing t_{WR} (in nS) by t_{CK} (in nS) and rounding up to the next integer: WRmin[cycles] = Roundup(t_{WR}[nS] / $t_{CK(avg)}$[nS]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with t_{RP} to determine t_{DAL}.
3. The table only shows the encodings for a given CAS Latency. For actual supported CAS Latency, please refer to **"Speed Bins"** tables for each frequency.
4. The table only shows the encodings for Write Recovery. For actual Write recovery timing, please refer to AC timing table.

Figure 5 – MR0 Definition

8.3.1.1 Burst Length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in Figure 5. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in Table 1. The burst length is defined by bits A0-A1. Burst length options include fixed BC4, fixed BL8 and 'on the fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC#.

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Table 1 – Burst Type and Burst Order

Burst Length	READ/ WRITE	Starting Column Address (A2, A1, A0)	Burst type = Sequential (decimal) A3 = 0	Burst type = Interleaved (decimal) A3 = 1	NOTES
4 Chop	READ	0 0 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1, 2, 3
		0 0 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	1, 2, 3
		0 1 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	1, 2, 3
		0 1 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	1, 2, 3
		1 0 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	1, 2, 3
		1 0 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	1, 2, 3
		1 1 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	1, 2, 3
		1 1 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	1, 2, 3
	WRITE	0,V,V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1, 2, 4, 5
		1,V,V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	1, 2, 4, 5
8	READ	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	2
		0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	2
		0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	2
		1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	2
		1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	2
		1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	2
		1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	2
	WRITE	V,V,V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2, 4

Notes:

1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC#, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.
2. 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
3. T: Output driver for data and strobes are in high impedance.
4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X: Don't Care.

8.3.1.2 CAS Latency

The CAS Latency is defined by MR0 (bits A2, A4, A5 and A6) as shown in Figure 5. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half-clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); RL = AL + CL. For more information on the supported CL and AL settings based on the operating clock frequency, refer to section 10.15 **"Speed Bins"** on page 134. For detailed Read operation refer to section 8.13 **"READ Operation"** on page 43.

8.3.1.3 Test Mode

The normal operating mode is selected by MR0 (bit A7 = 0) and all other bits set to the desired values shown in Figure 5. Programming bit A7 to a '1' places the DDR3 SDRAM into a test mode that is only used by the DRAM Manufacturer and should NOT be used. No operations or functionality is specified if A7 = 1.

8.3.1.4 DLL Reset

The DLL Reset bit is self-clearing, meaning that it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time that the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e., Read commands or ODT synchronous operations).

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8.3.1.5 Write Recovery

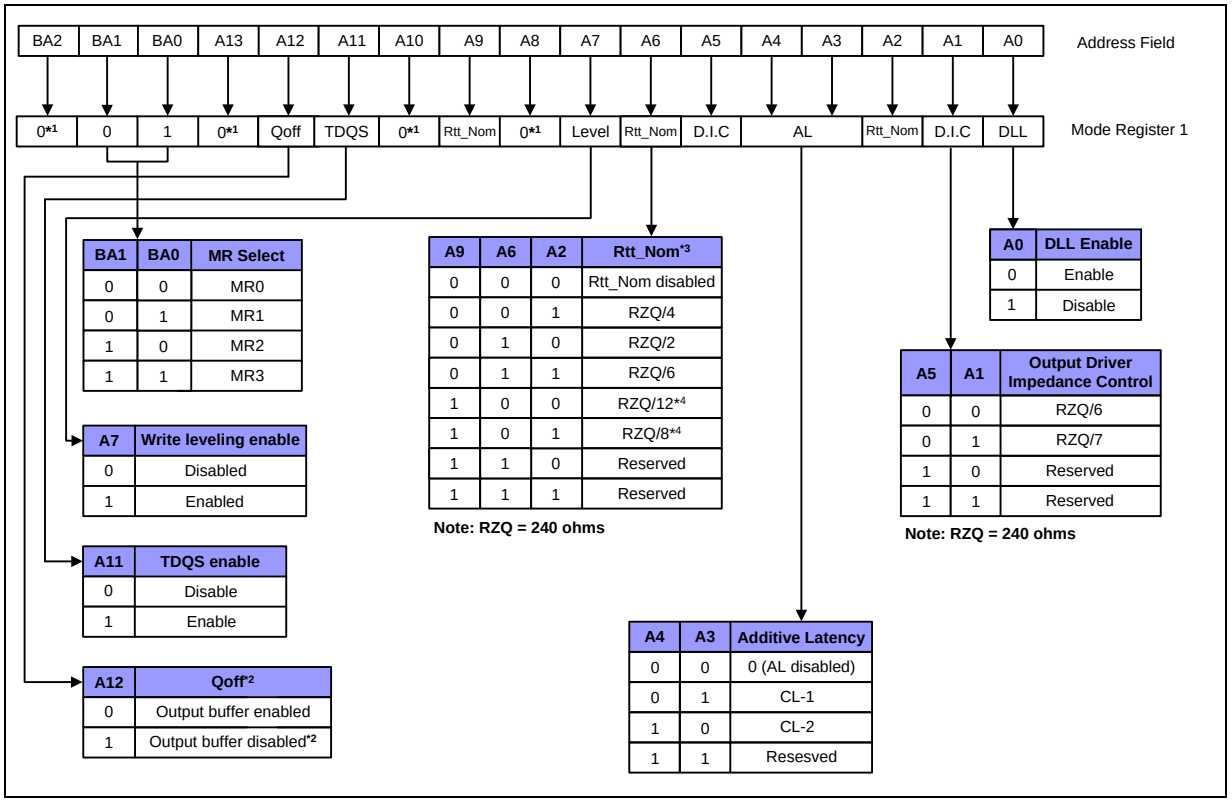
The programmed WR value MR0 (bits A9, A10 and A11) is used for the auto precharge feature along with t_{RP} to determine t_{DAL}. WR (write recovery for auto-precharge) min in clock cycles is calculated by dividing t_{WR} (in nS) by $t_{CK(avg)}$ (in nS) and rounding up to the next integer: WRmin[cycles] = Roundup(t_{WR}[nS]/$t_{CK(avg)}$[nS]). The WR must be programmed to be equal to or larger than t_{WR}(min).

8.3.1.6 Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power down mode. When MR0 (A12 = 0), or 'slow-exit', the DLL is frozen after entering precharge power down (for potential power savings) and upon exit requires t_{XPDLL} to be met prior to the next valid command. When MR0 (A12 = 1), or 'fast-exit', the DLL is maintained after entering precharge power down and upon exiting power down requires t_{XP} to be met prior to the next valid command.

8.3.2 Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, Rtt_Nom impedance, additive latency, Write leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA0 and low on BA1 and BA2, while controlling the states of address pins according to the Figure 6 below.



Notes:

1. BA2, A8, A10 and A13 are reserved for future use and must be programmed to "0" during MRS.
2. Outputs disabled - DQs, DQSs, DQS#s.
3. In Write leveling Mode (MR1 A[7] = 1) with MR1 A[12]=1, all Rtt_Nom settings are allowed; in Write Leveling Mode (MR1 A[7] = 1) with MR1 A[12]=0, only Rtt_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.
4. If Rtt_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

Figure 6 – MR1 Definition

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8.3.2.1 DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1 (A0 = 0), the DLL is automatically disabled when entering Self Refresh operation and is automatically re-enabled upon exit of Self Refresh operation. Any time the DLL is enabled and subsequently reset, t_{DLLK} clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the t_{DQSCK}, t_{AON} or t_{AOF} parameters. During t_{DLLK}, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, except when Rtt_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation refer to section 8.6 **"DLL-off Mode"** on page 25.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the Rtt_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2 {A10, A9} = {0,0}, to disable Dynamic ODT externally.

8.3.2.2 Output Driver Impedance Control

The output driver impedance of the DDR3 SDRAM device is selected by MR1 (bits A1 and A5) as shown in Figure 6.

8.3.2.3 ODT RTT Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmed in MR1. A separate value (Rtt_WR) may be programmed in MR2 to enable a unique RTT value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

8.3.2.4 Additive Latency (AL)

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown in Table 2.

Table 2 – Additive Latency (AL) Settings

A4	A3	AL
0	0	0 (AL Disabled)
0	1	CL - 1
1	0	CL - 2
1	1	Reserved

Note:

AL has a value of CL - 1 or CL - 2 as per the CL values programmed in the MR0 register.

8.3.2.5 Write leveling

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain t_{DQSS}, t_{DSS}, and t_{DSH} specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew. See section 8.9 **"Write Leveling"** on page 30 for more details.

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8.3.2.6 Output Disable

The DDR3 SDRAM outputs may be enabled/disabled by MR1 (bit A12) as shown in Figure 6. When this feature is enabled (A12 = 1), all output pins (DQs, DQS, DQS#, etc.) are disconnected from the device, thus removing any loading of the output drivers. This feature may be useful when measuring module power, for example. For normal operation, A12 should be set to '0'.

8.3.2.7 TDQS, TDQS#

TDQS (Termination Data Strobe) provides additional termination resistance outputs that may be useful in some system configurations. When enabled via the mode register, the same termination resistance function is applied to the TDQS/TDQS# pins that is applied to the DQS/DQS# pins.

In contrast to the RDQS function of DDR2 SDRAM, TDQS provides the termination resistance function only. The data strobe function of RDQS is not provided by TDQS.

The TDQS and DM functions share the same pin. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided and the TDQS# pin is not used. See Table 3 for details.

Table 3 – TDQS, TDQS# Function Matrix

MR1 (A11)	DM / TDQS	NU / TDQS#
0 (TDQS Disabled)	DM	Hi-Z
1 (TDQS Enabled)	TDQS	TDQS#

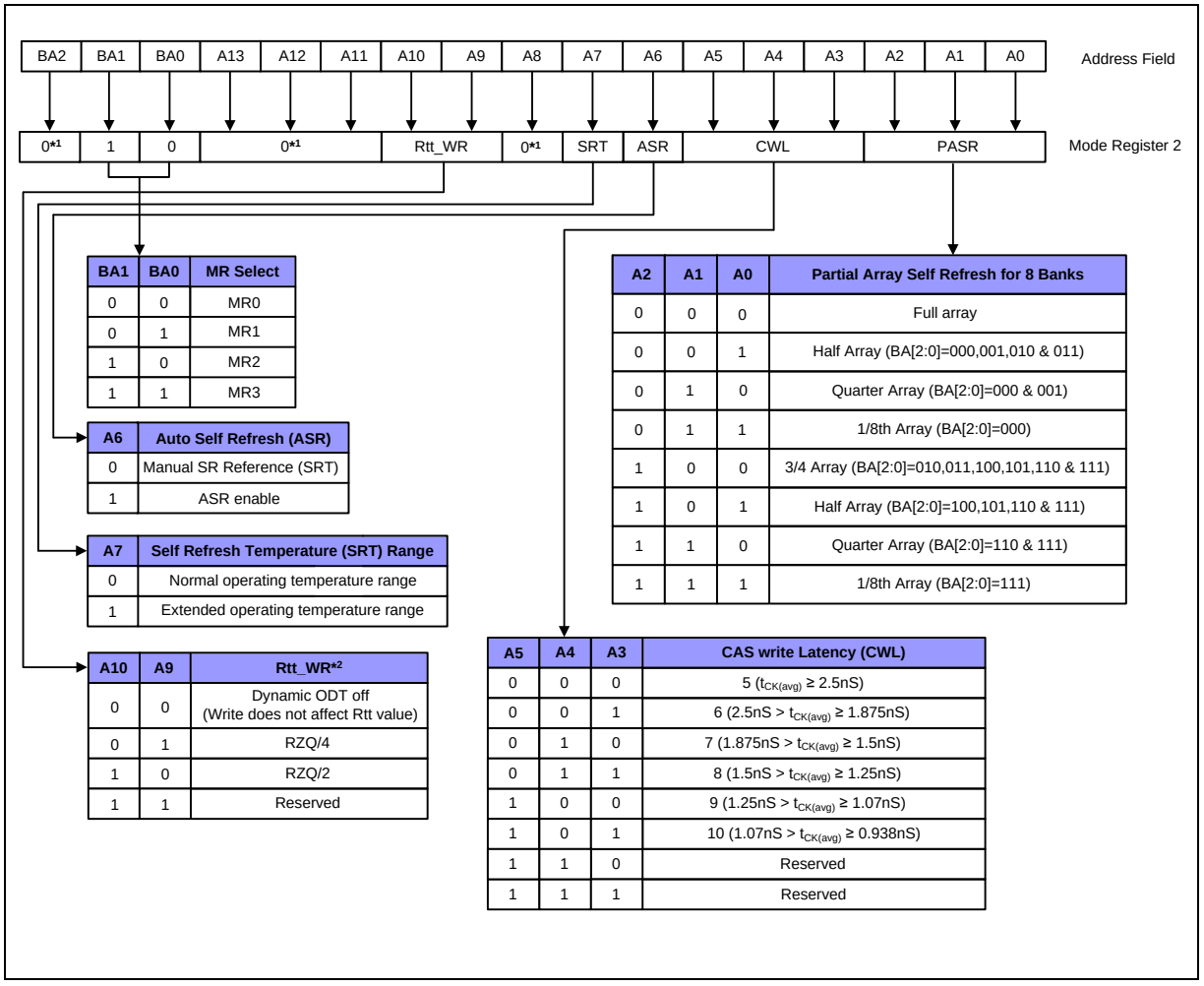
Notes:

1. If TDQS is enabled, the DM function is disabled.
2. When not used, TDQS function can be disabled to save termination power.

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8.3.3 Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the Figure 7 below.



BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A6	Auto Self Refresh (ASR)
0	Manual SR Reference (SRT)
1	ASR enable

A7	Self Refresh Temperature (SRT) Range
0	Normal operating temperature range
1	Extended operating temperature range

A10	A9	Rtt_WR*2
0	0	Dynamic ODT off (Write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

A2	A1	A0	Partial Array Self Refresh for 8 Banks
0	0	0	Full array
0	0	1	Half Array (BA[2:0]=000,001,010 & 011)
0	1	0	Quarter Array (BA[2:0]=000 & 001)
0	1	1	1/8th Array (BA[2:0]=000)
1	0	0	3/4 Array (BA[2:0]=010,011,100,101,110 & 111)
1	0	1	Half Array (BA[2:0]=100,101,110 & 111)
1	1	0	Quarter Array (BA[2:0]=110 & 111)
1	1	1	1/8th Array (BA[2:0]=111)

A5	A4	A3	CAS write Latency (CWL)
0	0	0	5 ($t_{CK(avg)} \geq 2.5nS$)
0	0	1	6 ($2.5nS > t_{CK(avg)} \geq 1.875nS$)
0	1	0	7 ($1.875nS > t_{CK(avg)} \geq 1.5nS$)
0	1	1	8 ($1.5nS > t_{CK(avg)} \geq 1.25nS$)
1	0	0	9 ($1.25nS > t_{CK(avg)} \geq 1.07nS$)
1	0	1	10 ($1.07nS > t_{CK(avg)} \geq 0.938nS$)
1	1	0	Reserved
1	1	1	Reserved

Notes:

1. BA2, A8, A11~A13 are reserved for future use and must be programmed to “0” during MRS.
2. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled. During write leveling, Dynamic ODT is not available.

Figure 7 – MR2 Definition

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8.3.3.1 Partial Array Self Refresh (PASR)

If PASR (Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified address range shown in Figure 7 will be lost if Self Refresh is entered. Data integrity will be maintained if tREFI conditions are met and no Self Refresh command is issued.

8.3.3.2 CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5), as shown in Figure 7. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data.

DDR3 SDRAM does not support any half-clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL = AL + CWL. For more information on the supported CWL and AL settings based on the operating clock frequency, refer to section 10.15 **"Speed Bins"** on page 134. For detailed Write operation refer to section 8.14 **"WRITE Operation"** on page 56.

8.3.3.3 Auto Self Refresh (ASR) and Self Refresh Temperature (SRT)

DDR3 SDRAM must support Self Refresh operation at all supported temperatures. Applications requiring Self Refresh operation in the Extended Temperature Range must use the ASR function or program the SRT bit appropriately.

When ASR enabled, DDR3 SDRAM automatically provides Self Refresh power management functions for all supported operating temperature values. If not enabled, the SRT bit must be programmed to indicate TOPER during subsequent Self Refresh operation.

ASR = 0, Self Refresh rate is determined by SRT bit A7 in MR2.

ASR = 1, Self Refresh rate is determined by on-die thermal sensor. SRT bit A7 in MR2 is don't care.

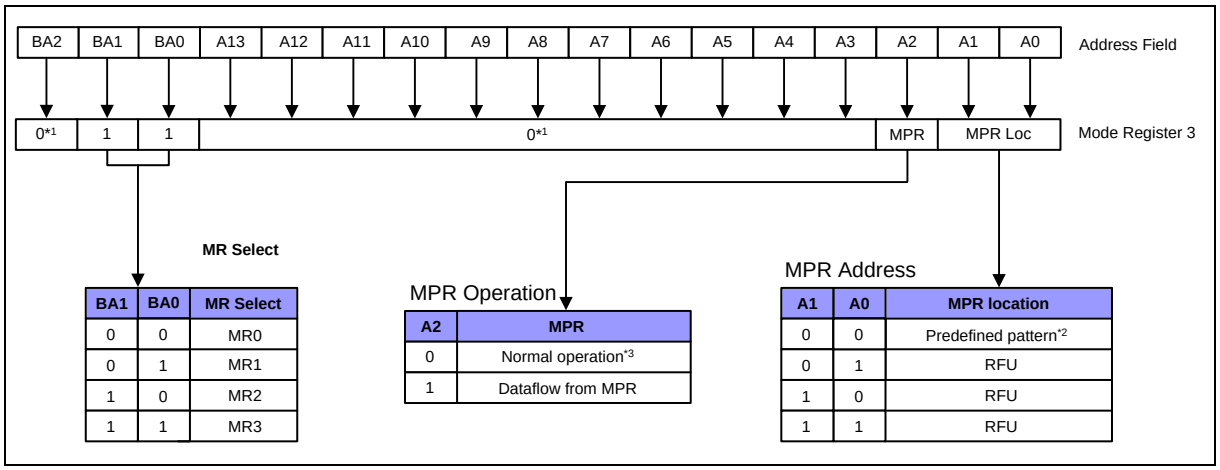
8.3.3.4 Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature **"Dynamic ODT"**. In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT settings. In Write leveling mode, only Rtt_Nom is available. For details on Dynamic ODT operation, refer to section 8.19.3 **"Dynamic ODT"** on page 83.

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8.3.4 Mode Register MR3

The Mode Register MR3 controls Multi purpose registers. The Mode Register 3 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the Figure 8 below.



Notes:

1. BA2, A3~A13 are reserved for future use and must be programmed to "0" during MRS.
2. The predefined pattern will be used for read synchronization.
3. When MPR control is set for normal operation (MR3 A[2] = 0) then MR3 A[1:0] will be ignored.

Figure 8 – MR3 Definition

8.3.4.1 Multi Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and t_{RP} met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Power Down mode, Self Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode. For detailed MPR operation refer to section 8.10 **"Multi Purpose Register"** on page 34.

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8.4 No OPeration (NOP) Command

The No OPeration (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP (CS# LOW and RAS#, CAS#, and WE# HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

8.5 Deselect Command

The DESELECT function (CS# HIGH) prevents new commands from being executed by the DDR3 SDRAM. The DDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

8.6 DLL-off Mode

DDR3 DLL-off mode is entered by setting MR1 bit A0 to “1”; this will disable the DLL for subsequent operations until A0 bit is set back to “0”. The MR1 A0 bit for DLL control can be switched either during initialization or later. Refer to section 8.8 **“Input clock frequency change”** on page 28.

The DLL-off Mode operations listed below are an optional feature for DDR3. The maximum clock frequency for DLL-off Mode is specified by the parameter $t_{CK(DLL_OFF)}$. There is no minimum frequency limit besides the need to satisfy the refresh interval, t_{REFI}.

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=6 and CWL=6.

DLL-off mode will affect the Read data Clock to Data Strobe relationship (t_{DQSCK}), but not the Data Strobe to Data relationship (t_{DQSQ}, t_{QH}). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where t_{DQSCK} starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode t_{DQSCK} starts (AL+CL - 1) cycles after the read command. Another difference is that t_{DQSCK} may not be small compared to t_{CK} (it might even be larger than t_{CK}) and the difference between t_{DQSCK} min and t_{DQSCK} max is significantly larger than in DLL-on mode.

The timing relations on DLL-off mode READ operation is shown in the following Timing Diagram (CL=6, BL=8):

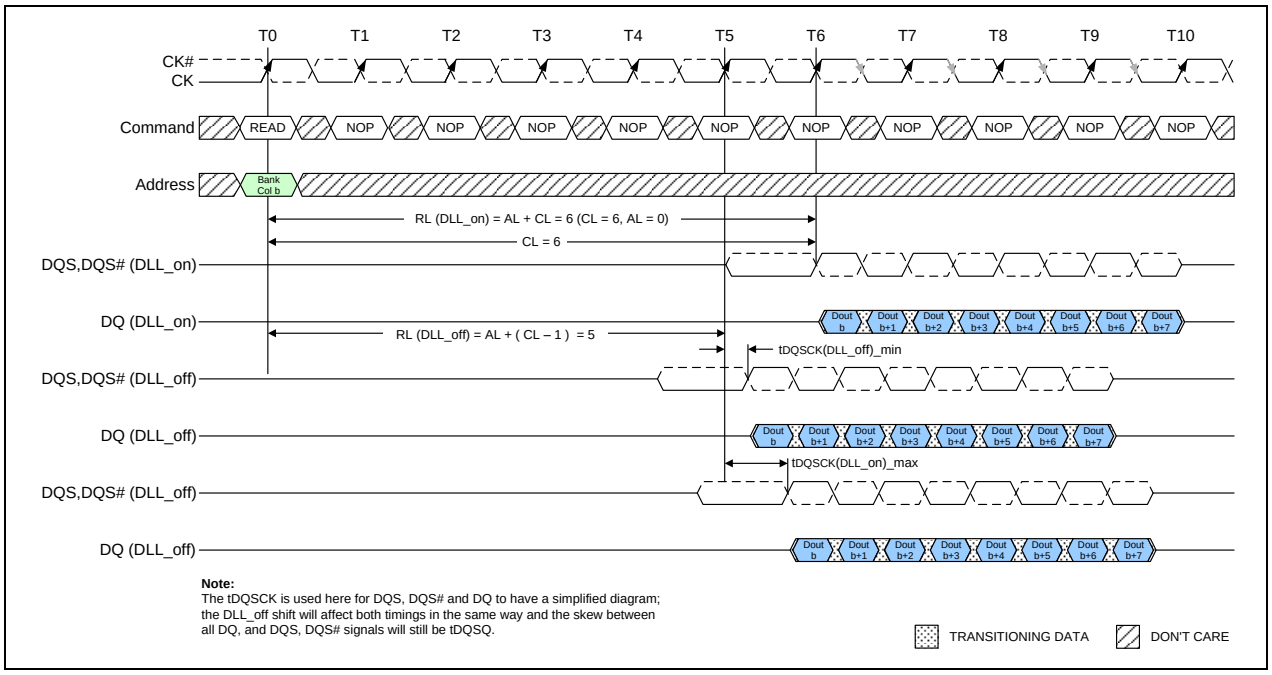


Figure 9 – DLL-off mode READ Timing Operation

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8.7 DLL on/off switching procedure

DDR3 DLL-off mode is entered by setting MR1 bit A0 to "1"; this will disable the DLL for subsequent operations until A0 bit is set back to "0".

8.7.1 DLL "on" to DLL "off" Procedure

To switch from DLL "on" to DLL "off" requires the frequency to be changed during Self-Refresh, as outlined in the following procedure:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled, and DRAMs On-die Termination resistors, RTT, must be in high impedance state before MRS to MR1 to disable the DLL.)
2. Set MR1 bit A0 to "1" to disable the DLL.
3. Wait tMOD.
4. Enter Self Refresh Mode; wait until (tCKSRE) is satisfied.
5. Change frequency, in guidance with section 8.8 **"Input clock frequency change"** on page 28.
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If both ODT features were disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
8. Wait tXS, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. A ZQCL command may also be issued after tXS).
9. Wait for tMOD, then DRAM is ready for next command.

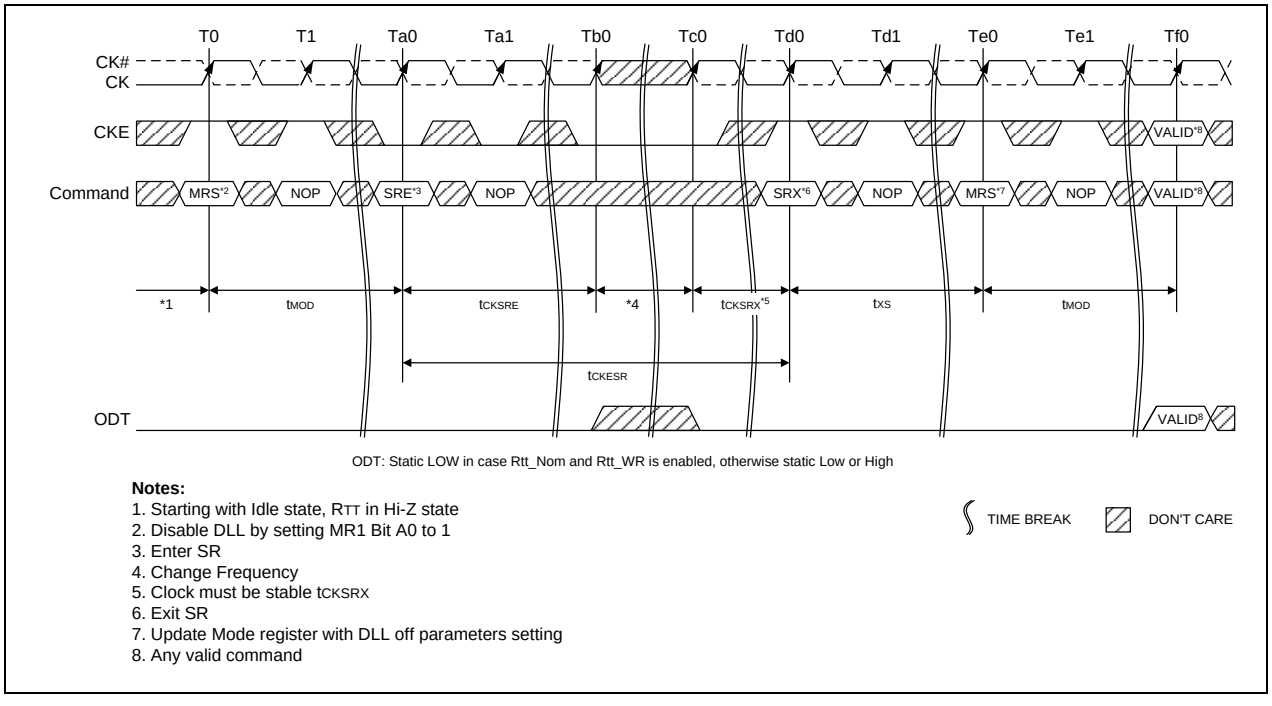


Figure 10 – DLL Switch Sequence from DLL-on to DLL-off

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8.7.2 DLL "off" to DLL "on" Procedure

To switch from DLL "off" to DLL "on" (with required frequency change) during Self-Refresh:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors (RTT) must be in high impedance state before Self-Refresh mode is entered.)
2. Enter Self Refresh Mode, wait until tCKSRE satisfied.
3. Change frequency, in guidance with section 8.8 **"Input clock frequency change"** on page 28.
4. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until tDLLK timings from subsequent DLL Reset command is satisfied. If both ODT features are disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
6. Wait tXS, then set MR1 bit A0 to "0" to enable the DLL.
7. Wait tMRD, then set MR0 bit A8 to "1" to start DLL Reset.
8. Wait tMRD, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. After tMOD satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK.)
9. Wait for tMOD, then DRAM is ready for next command (Remember to wait tDLLK after DLL Reset before applying command requiring a locked DLL!). In addition, wait also for tZQoper in case a ZQCL command was issued.

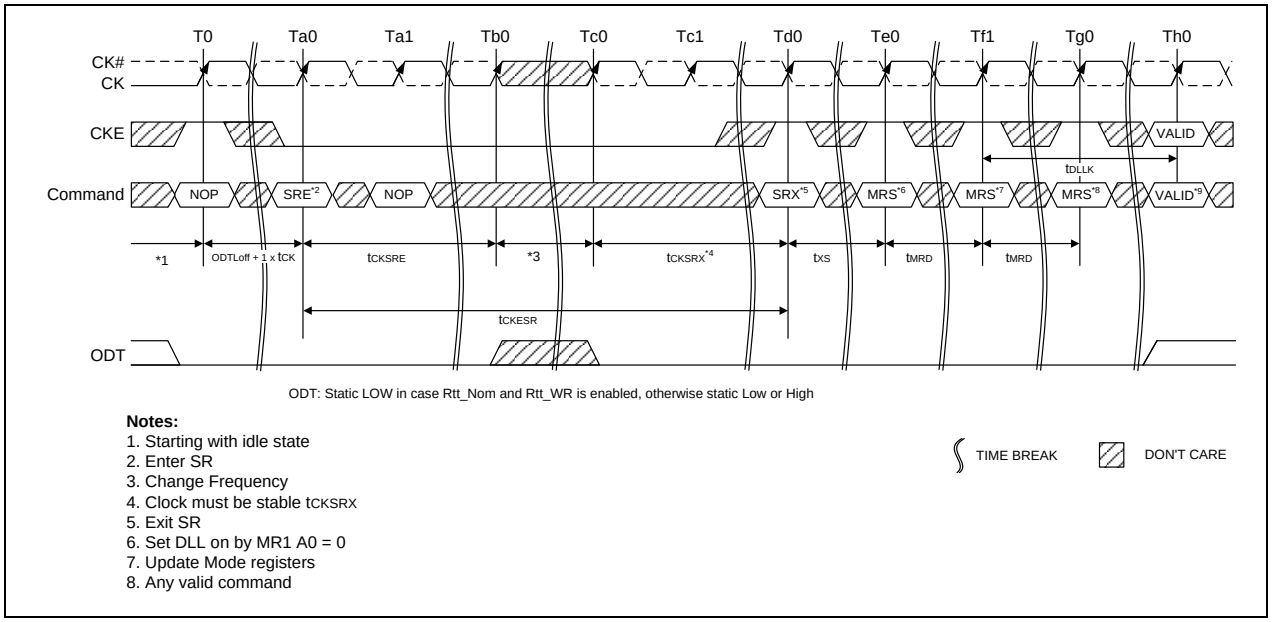


Figure 11 – DLL Switch Sequence from DLL Off to DLL On

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8.8 Input clock frequency change

Once the DDR3 SDRAM is initialized, the DDR3 SDRAM requires the clock to be “stable” during almost all states of normal operation. This means that, once the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under two conditions: (1) Self-Refresh mode and (2) Precharge Power-down mode. Outside of these two modes, it is illegal to change the clock frequency.

8.8.1 Frequency change during Self-Refresh

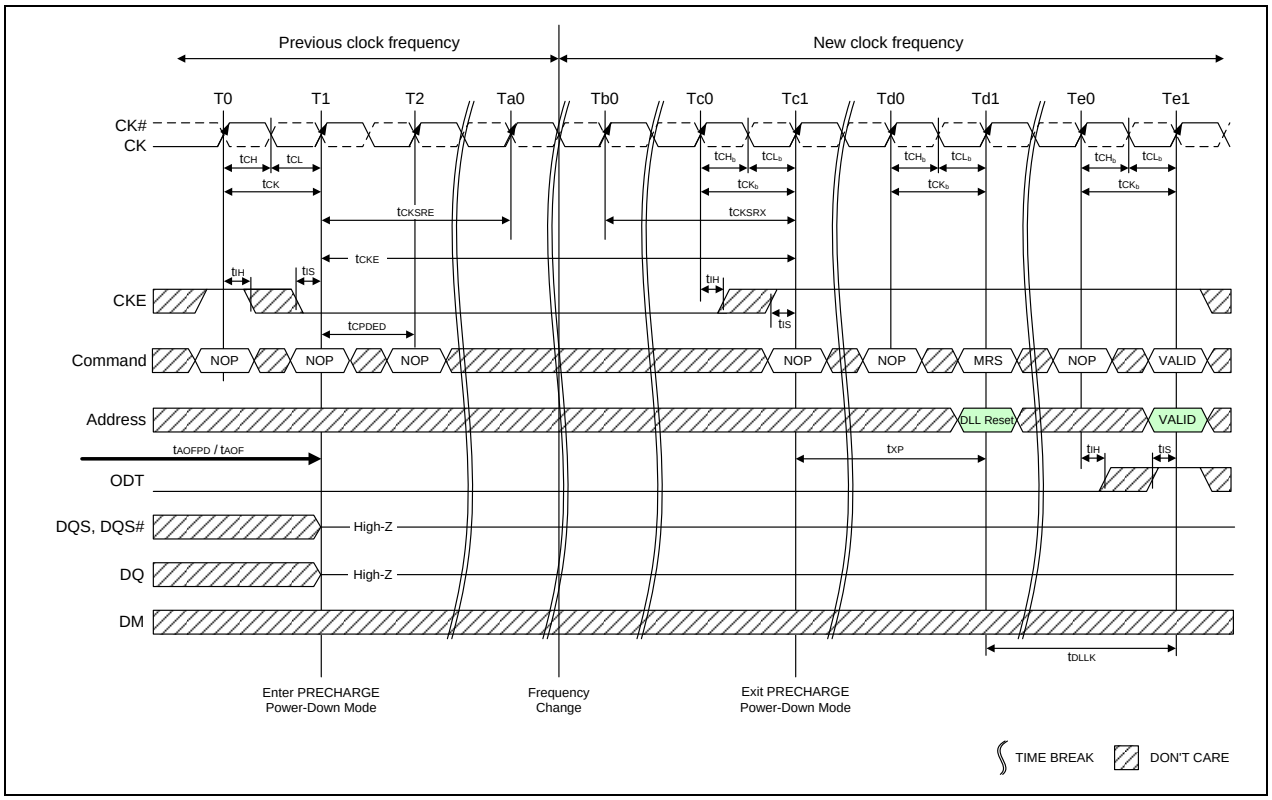
For the first condition, once the DDR3 SDRAM has been successfully placed in to Self-Refresh mode and t_{CKSRE} has been satisfied, the state of the clock becomes a don't care. Once a don't care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to t_{CKSRX}. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined in see section 8.16 **“Self-Refresh Operation”** on page 67.

The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on mode -> DLL_off mode transition sequence; refer to section 8.7 **“DLL on/off switching procedure”** on page 26.

8.8.2 Frequency change during Precharge Power-down

The second condition is when the DDR3 SDRAM is in Precharge Power-down mode (either fast exit mode or slow exit mode). If the Rtt_Nom feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring R_{TT} is in an off state. If the Rtt_Nom feature was disabled in the mode register prior to entering Precharge power down mode, R_{TT} will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case. A minimum of t_{CKSRE} must occur after CKE goes LOW before the clock frequency may change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, ODT and CKE must be held at stable LOW levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM t_{CKSRX} before Precharge Power-down may be exited; after Precharge Power-down is exited and t_{XP} has expired, the DLL must be RESET via MRS. Depending on the new clock frequency, additional MRS commands may need to be issued to appropriately set the WR, CL, and CWL with CKE continuously registered high. During DLL re-lock period, ODT must remain LOW and CKE must remain HIGH. After the DLL lock time, the DRAM is ready to operate with new clock frequency. This process is depicted in Figure 12 on page 29.

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Notes:

1. Applicable for both SLOW EXIT and FAST EXIT Precharge Power-down.
2. tAOFPD and tAOF must be satisfied and outputs High-Z prior to T1; refer to ODT timing section for exact requirements.
3. If the Rtt_Nom feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state, as shown in Figure 9. If the Rtt_Nom feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case.

Figure 12 – Change Frequency during Precharge Power-down

8.9 Write Leveling

For better signal integrity, the DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew.

The memory controller can use the 'write leveling' feature and feedback from the DDR3 SDRAM to adjust the DQS - DQS# to CK - CK# relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS - DQS# to align the rising edge of DQS - DQS# with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK - CK#, sampled with the rising edge of DQS - DQS#, through the DQ bus. The controller repeatedly delays DQS - DQS# until a transition from 0 to 1 is detected. The DQS - DQS# delay established though this exercise would ensure tDQSS specification.

Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS - DQS# signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in section 10.16 **"AC Characteristics"** in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown in Figure 13.

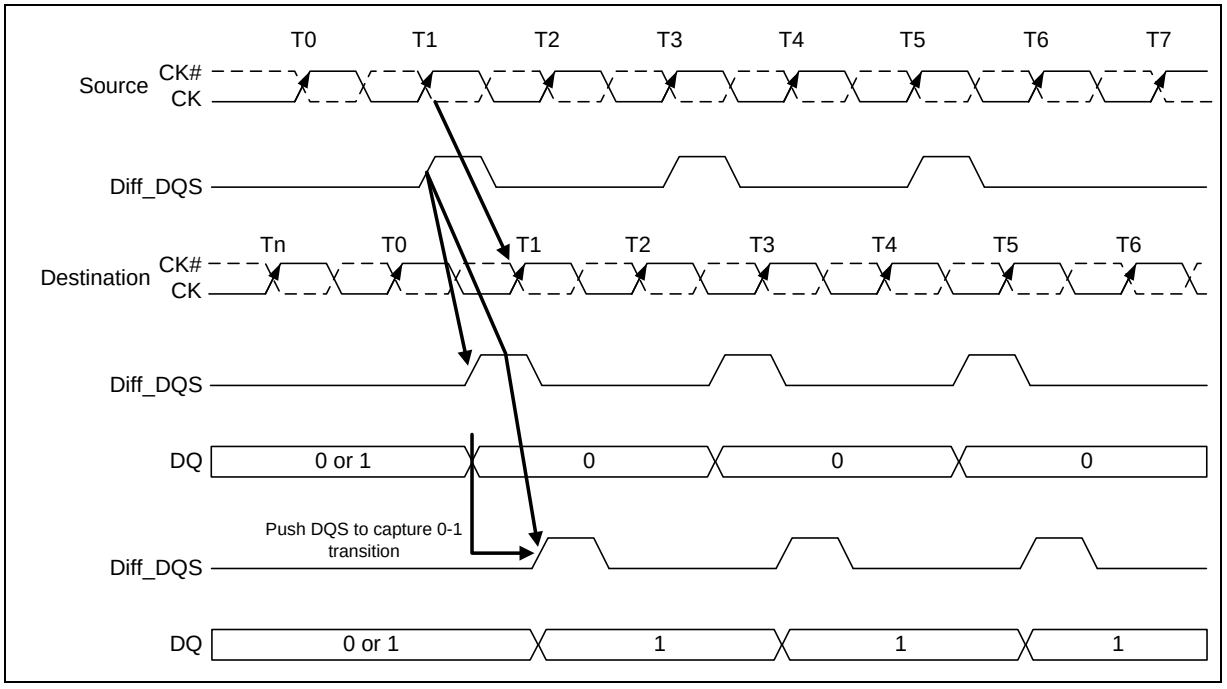


Figure 13 – Write Leveling Concept

DQS - DQS# driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

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8.9.1 DRAM setting for write leveling & DRAM termination function in that mode

DRAM enters into Write leveling mode if A7 in MR1 set 'High' and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set 'Low' (Table 4). Note that in write leveling mode, only DQS/DQS# terminations are activated and deactivated via ODT pin, unlike normal operation (Table 5).

Table 4 – MR setting involved in the leveling procedure

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

Table 5 – DRAM termination function in the leveling mode

ODT pin @DRAM	DQS/DQS# termination	DQs termination
De-asserted	Off	Off
Asserted	On	Off

Note:

In Write Leveling Mode with its output buffer disabled (MR1 A[7] = 1 with MR1 A[12] = 1) all Rtt_Nom settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1 A[7] = 1 with MR1 A[12] = 0) only Rtt_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

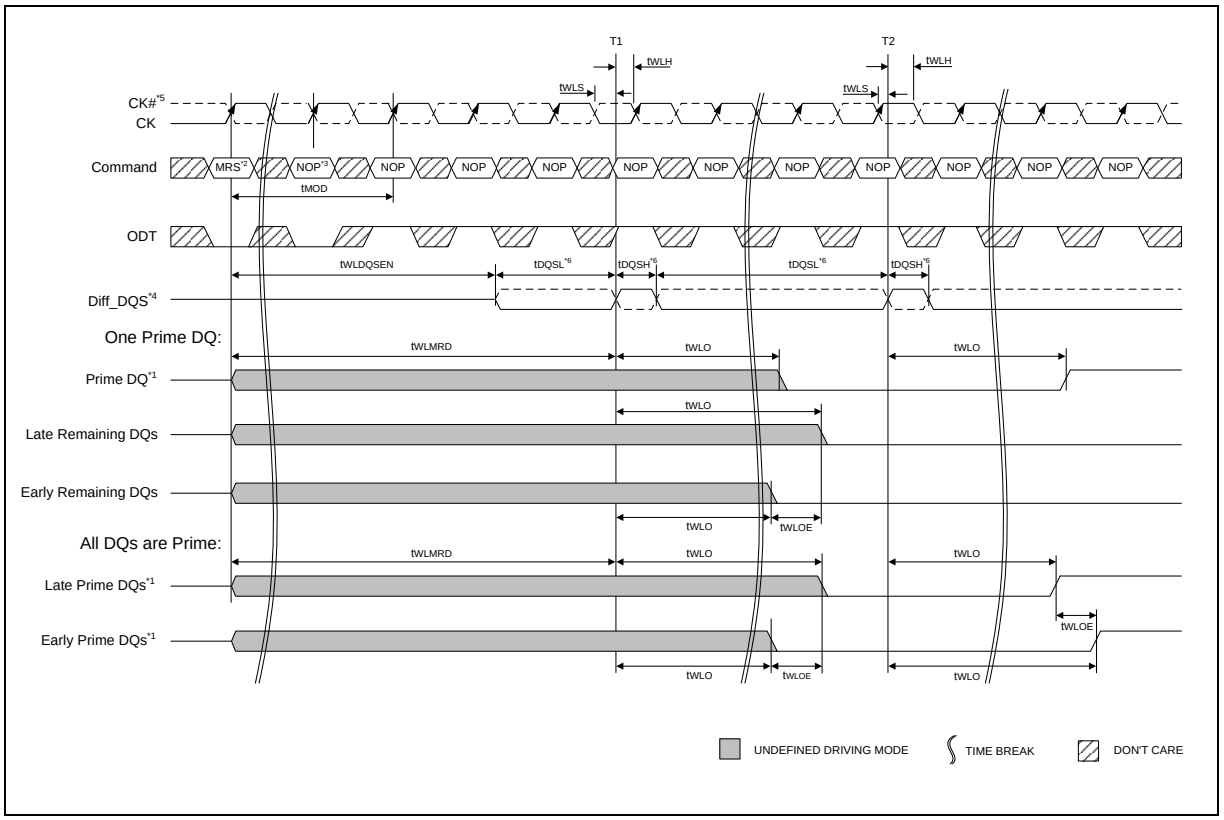
8.9.2 Write Leveling Procedure

The Memory controller initiates Leveling mode of all DRAMs by setting bit 7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only NOP or DESELECT commands are allowed, as well as an MRS command to change Qoff bit (MR1[A12]) and an MRS command to exit write leveling (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7]=0) may also change MR1 bits of A12, A11, A9, A6, A5, A2 and A1. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The Controller may assert ODT after t_{MOD}, at which time the DRAM is ready to accept the ODT signal.

The Controller may drive DQS low and DQS# high after a delay of $t_{WLDQSEN}$, at which time the DRAM has applied on-die termination on these signals. After t_{DQSL} and t_{WLMRD}, the controller provides a single DQS, DQS# edge which is used by the DRAM to sample CK - CK# driven from controller. t_{WLMRD}(max) timing is controller dependent.

DRAM samples CK - CK# status with rising edge of DQS - DQS# and provides feedback on all the DQ bits asynchronously after t_{WLO} timing. Either one or all data bits ("prime DQ bit(s)") provide the leveling feedback. The DRAM's remaining DQ bits are driven Low statically after the first sampling procedure. There is a DQ output uncertainty of t_{WLOE} defined to allow mismatch on DQ bits. The t_{WLOE} period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS/DQS#) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS - DQS# delay setting and launches the next DQS/DQS# pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS - DQS# delay setting and write leveling is achieved for the device. Figure 14 describes the timing diagram and parameters for the overall Write Leveling procedure.

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Notes:

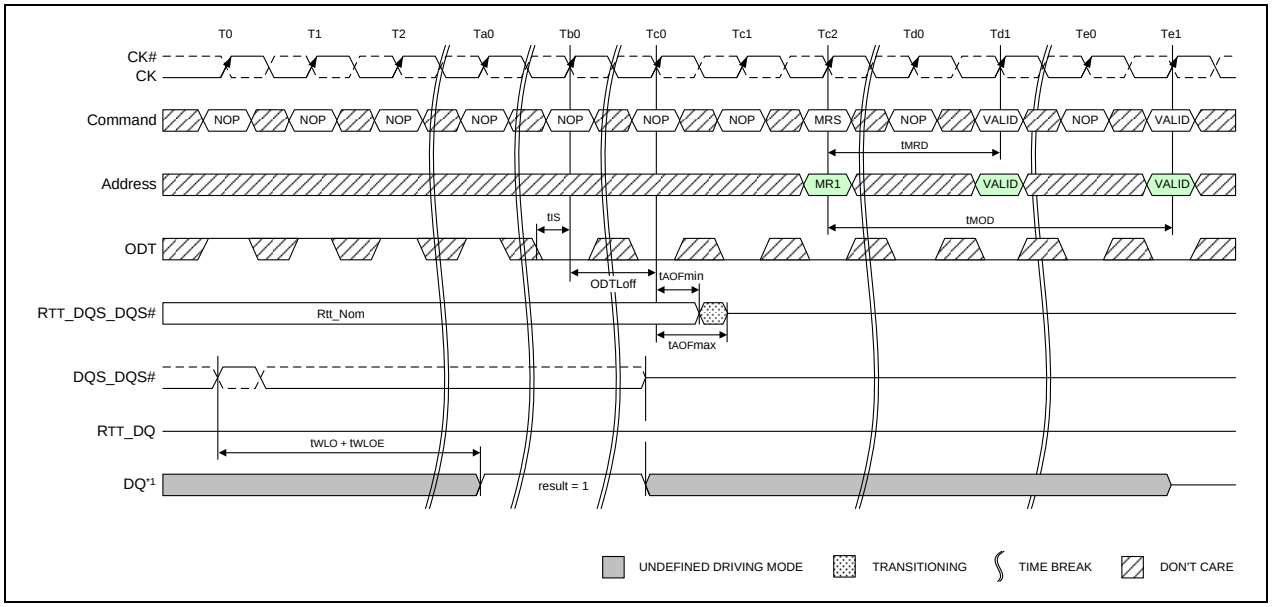
1. DRAM has the option to drive leveling feedback on a prime DQ or all DQs. If feedback is driven only on one DQ, the remaining DQs must be driven low, as shown in above Figure, and maintained at this state throughout the leveling procedure.
2. MRS: Load MR1 to enter write leveling mode.
3. NOP: NOP or Deselect.
4. Diff_DQS is the differential data strobe (DQS, DQS#). Timing reference points are the zero crossings. DQS is shown with solid line, DQS# is shown with dotted line.
5. CK, CK#: CK is shown with solid dark line, where as CK# is drawn with dotted line.
6. DQS, DQS# needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent.

Figure 14 – Timing details of Write leveling sequence [DQS - DQS# is capturing CK - CK# low at T1 and CK - CK# high at T2]

8.9.3 Write Leveling Mode Exit

The following sequence describes how the Write Leveling Mode should be exited:

1. After the last rising strobe edge (see ~T0), stop driving the strobe signals (see ~Tc0). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until t_{MOD} after the respective MR command (Te1).
2. Drive ODT pin low (t_{IS} must be satisfied) and continue registering low. (see Tb0).
3. After the RTT is switched off, disable Write Level Mode via MRS command (see Tc2).
4. After t_{MOD} is satisfied (Te1), any valid command may be registered. (MR commands may be issued after t_{MRD} (Td1).



Note:

1. The DQ result = 1 between Ta0 and Tc0 is a result of the DQS, DQS# signals capturing CK high just after the T0 state.

Figure 15 – Timing details of Write leveling exit

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8.10 Multi Purpose Register

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. The basic concept of the MPR is shown in Figure 16.

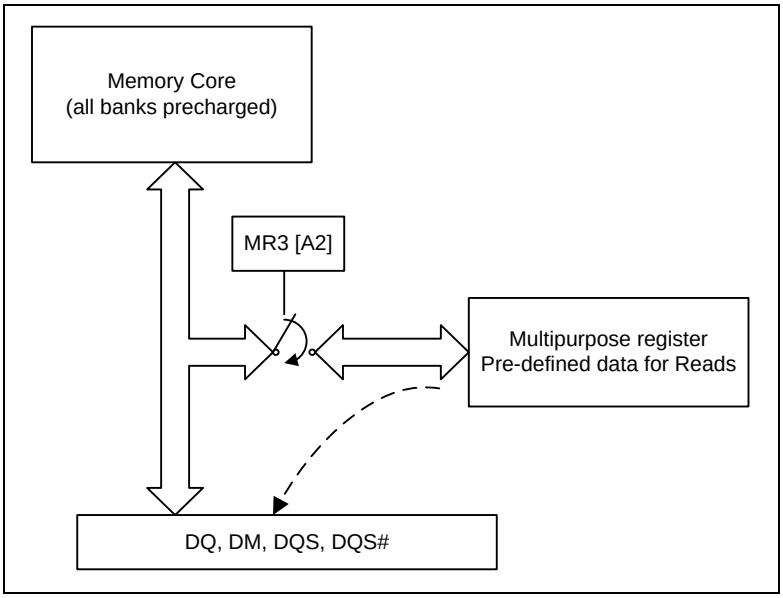


Figure 16 – MPR Block Diagram

To enable the MPR, a Mode Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1, as shown in Table 6. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and t_{RP} met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. The resulting operation, when a RD or RDA command is issued, is defined by MR3 bits A[1:0] when the MPR is enabled as shown in Table 7. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Note that in MPR mode RDA has the same functionality as a READ command which means the auto precharge part of RDA is ignored. Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

Table 6 – MPR Functional Description of MR3 Bits

MR3 A[2]	MR3 A[1:0]	Function
MPR	MPR-Loc	
0b	don't care (0b or 1b)	Normal operation, no MPR transaction All subsequent Reads will come from DRAM array All subsequent Write will go to DRAM array
1b	See Table 7	Enable MPR mode, subsequent RD/RDA commands defined by MR3 A[1:0]

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8.10.1 MPR Functional Description

- One bit wide logical interface via all DQ pins during READ operation.
- Register Read:
  - —DQ[0] drives information from MPR
  - —DQ[7:1] either drive the same information as DQ [0], or they drive 0b
- Addressing during for Multi Purpose Register reads for all MPR agents:
  - — BA[2:0]: Don't care
  - — A[1:0]: A[1:0] must be equal to '00'b. Data read burst order in nibble is fixed
  - — A[2]: A[2] selects the burst order

    For BL=8, A[2] must be equal to 0b, burst order is fixed to [0,1,2,3,4,5,6,7], *)

    For Burst Chop 4 cases, the burst order is switched on nibble base

    A[2]=0b, Burst order: 0,1,2,3 *)

    A[2]=1b, Burst order: 4,5,6,7 *)
  - — A[9:3]: Don't care
  - — A10/AP: Don't care
  - — A12/BC#: Selects burst chop mode on-the-fly, if enabled within MR0
  - — A11 and A13: Don't care
- Regular interface functionality during register reads:
  - — Support two Burst Ordering which are switched with A2 and A[1:0]=00b
  - — Support of read burst chop (MRS and on-the-fly via A12/BC#)
  - — All other address bits (remaining column address bits including A10, all bank address bits) will be ignored by the DDR3 SDRAM
  - — Regular read latencies and AC timings apply
  - — DLL must be locked prior to MPR Reads

Note: *) Burst order bit 0 is assigned to LSB and burst order bit 7 is assigned to MSB of the selected MPR agent.

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8.10.2 MPR Register Address Definition

Table 7 provides an overview of the available data locations, how they are addressed by MR3 A[1:0] during a MRS to MR3, and how their individual bits are mapped into the burst order bits during a Multi Purpose Register Read.

Table 7 – MPR Readouts and Burst Order Bit Mapping

MR3 A[2]	MR3 A[1:0]	Function	Burst Length	Read Address A[2:0]	Burst Order and Data Pattern
1b	00b	Read Pre-defined Pattern for System Calibration	BL8	000b	Burst order 0,1,2,3,4,5,6,7 Pre-defined Data Pattern [0,1,0,1,0,1,0,1]
			BC4	000b	Burst order 0,1,2,3 Pre-defined Data Pattern [0,1,0,1]
			BC4	100b	Burst order 4,5,6,7 Pre-defined Data Pattern [0,1,0,1]
1b	01b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1b	10b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1b	11b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7

Note: Burst order bit 0 is assigned to LSB and the burst order bit 7 is assigned to MSB of the selected MPR agent.

8.10.3 Relevant Timing Parameters

The following AC timing parameters are important for operating the Multi Purpose Register: t_{RP}, t_{MRD}, t_{MOD}, and t_{MPRR}. For more details refer to section 10.16 **"AC Characteristics"** on page 139.

8.10.4 Protocol Example

Protocol Example (This is one example):

Read out pre-determined read-calibration pattern.

Description: Multiple reads from Multi Purpose Register, in order to do system level read timing calibration based on pre-determined and standardized pattern.

Protocol Steps:

- Precharge All.
- Wait until t_{RP} is satisfied.
- Set MRS, "MR3 A[2] = 1b" and "MR3 A[1:0] = 00b".

  This redirects all subsequent reads and load pre-defined pattern into Multi Purpose Register.
- Wait until t_{MRD} and t_{MOD} are satisfied (Multi Purpose Register is then ready to be read). During the period MR3 A[2] =1, no data write operation is allowed.

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- Read:

  A[1:0] = ‘00’b (Data burst order is fixed starting at nibble, always 00b here)

  A[2] = ‘0’b (For BL=8, burst order is fixed as 0,1,2,3,4,5,6,7)

  A12/BC# = 1 (use regular burst length of 8)

  All other address pins (including BA[2:0] and A10/AP): don't care

- After RL = AL + CL, DRAM bursts out the pre-defined Read Calibration Pattern.
- Memory controller repeats these calibration reads until read data capture at memory controller is optimized.
- After end of last MPR read burst, wait until t_{MPRR} is satisfied.
- Set MRS, “MR3 A[2] = 0b” and “MR3 A[1:0] = don't care” to the normal DRAM state.

  All subsequent read and write accesses will be regular reads and writes from/to the DRAM array.
- Wait until t_{MRD} and t_{MOD} are satisfied.
- Continue with “regular” DRAM commands, like activate a memory bank for regular read or write access,...

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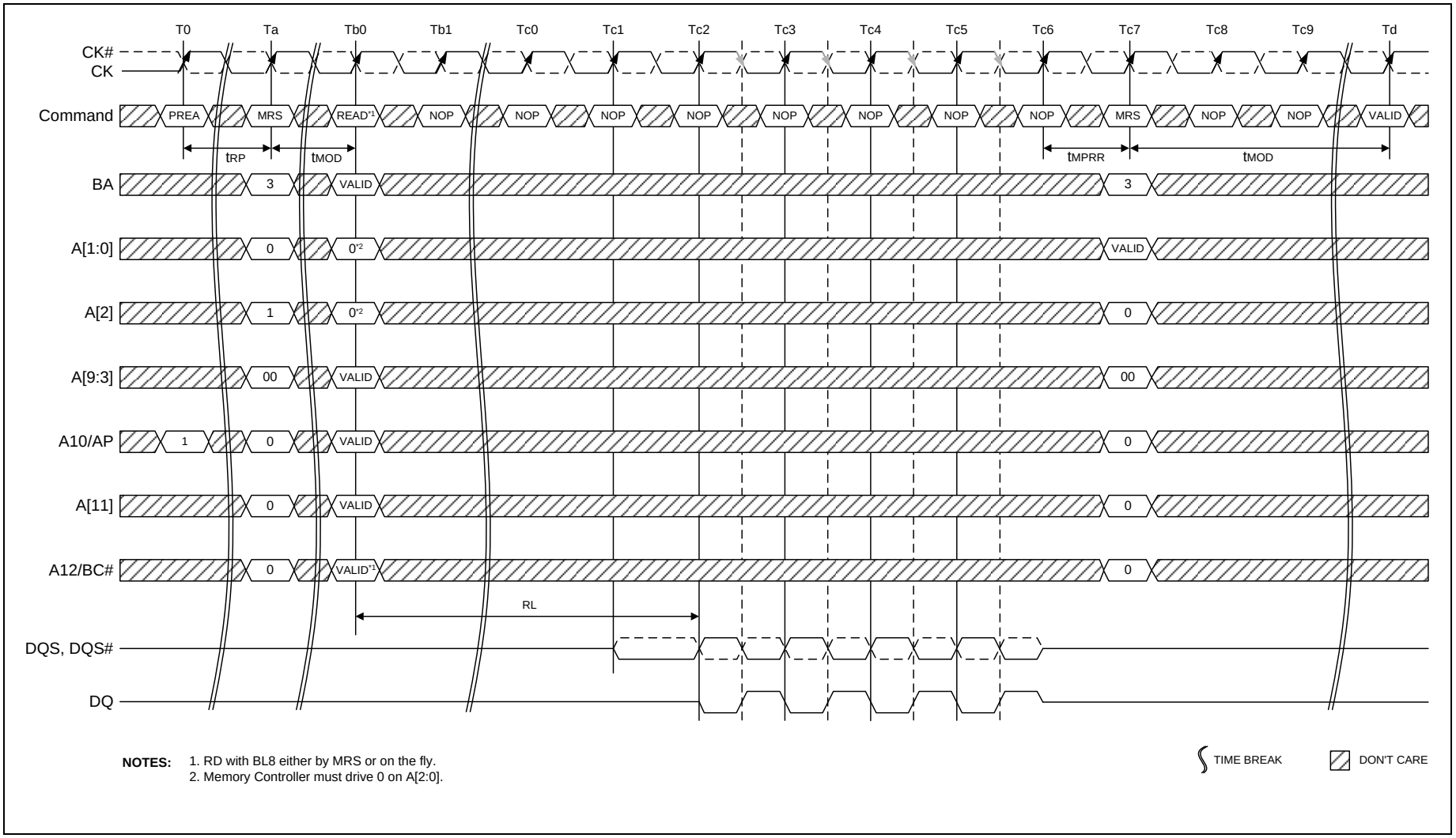


Figure 17 – MPR Readout of pre-defined pattern, BL8 fixed burst order, single readout

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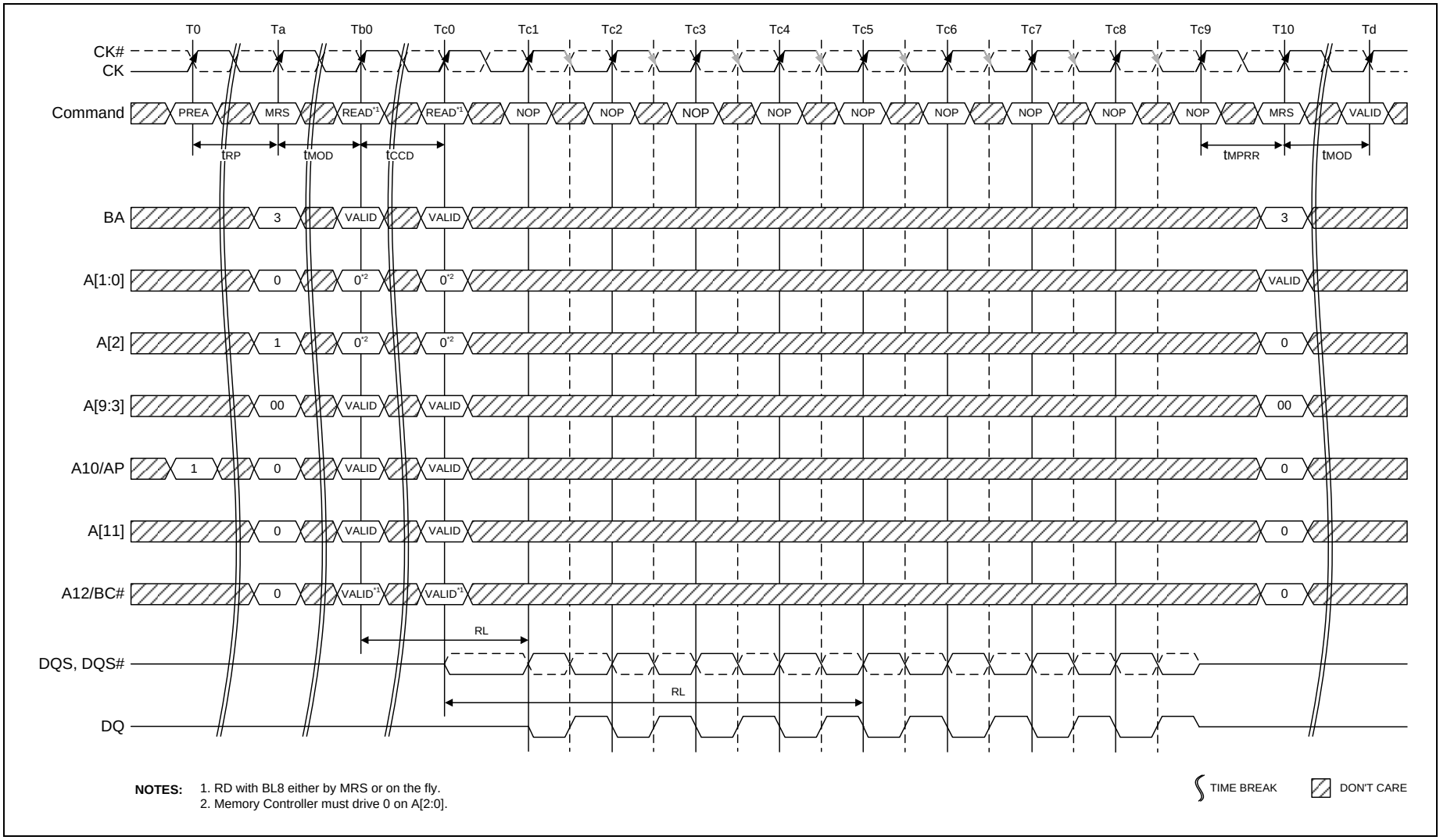
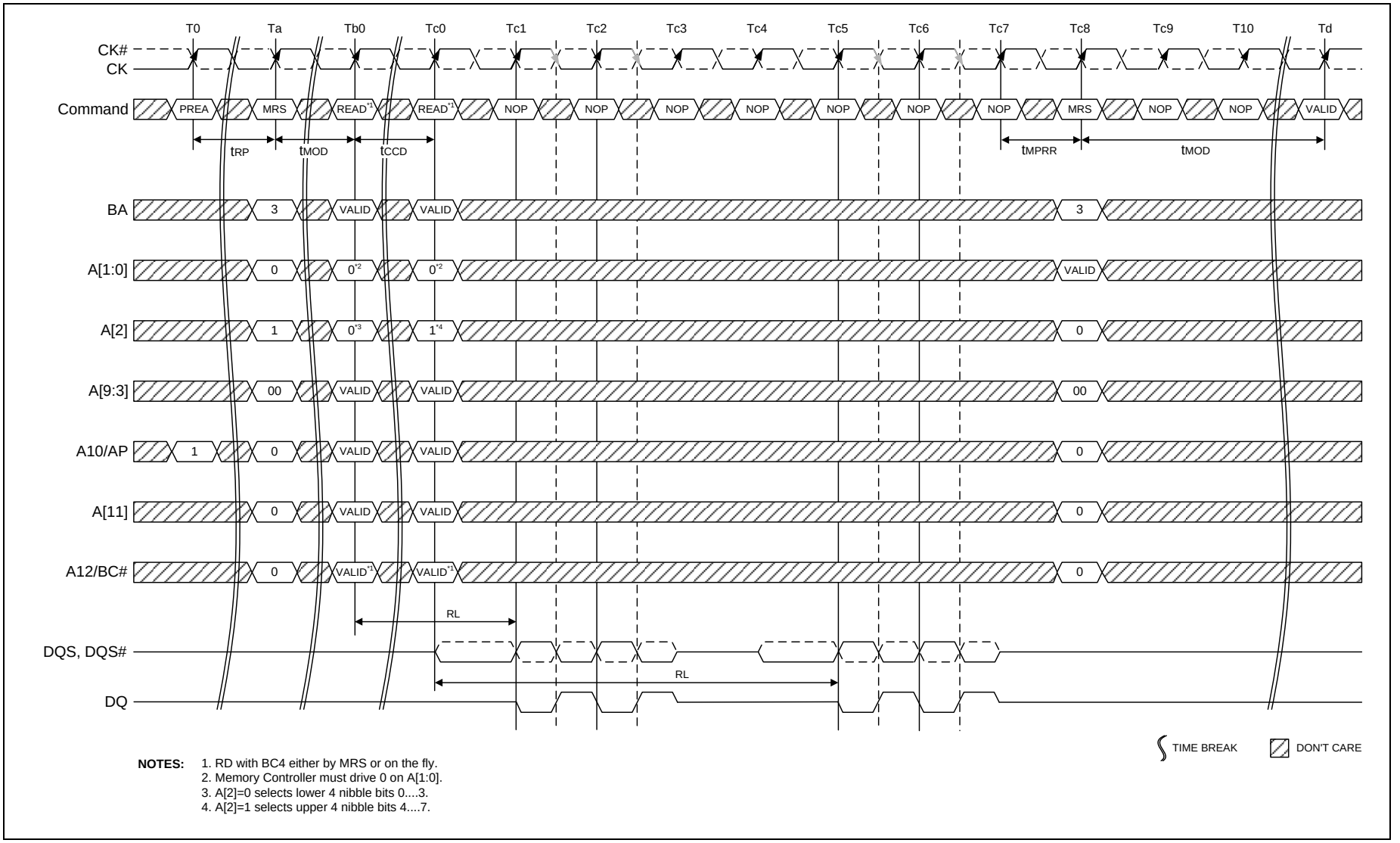


Figure 18 – MPR Readout of pre-defined pattern, BL8 fixed burst order, back-to-back readout

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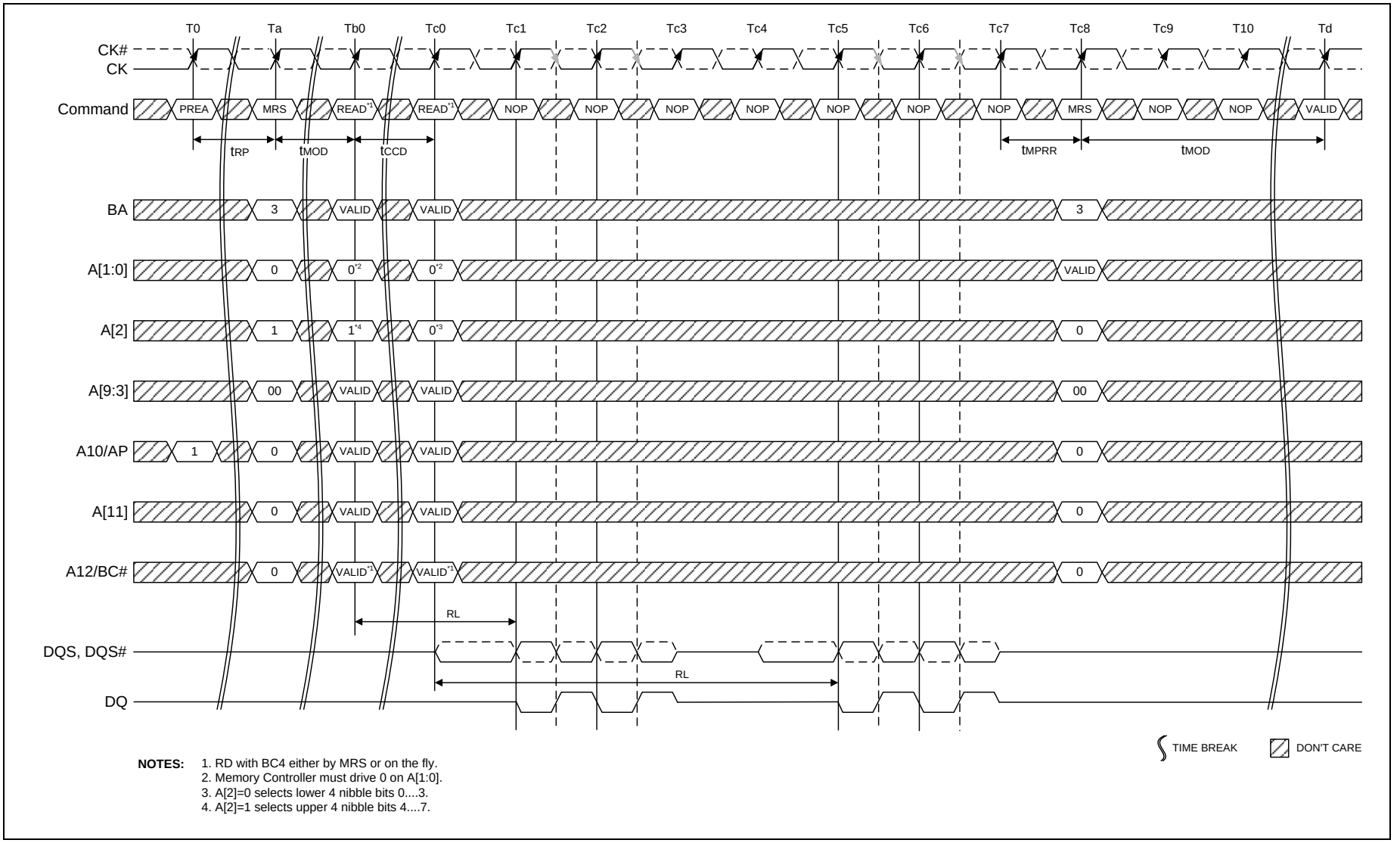
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NOTES:
1. RD with BC4 either by MRS or on the fly.
2. Memory Controller must drive 0 on A[1:0].
3. A[2]=0 selects lower 4 nibble bits 0....3.
4. A[2]=1 selects upper 4 nibble bits 4....7.

Figure 19 – MPR Readout pre-defined pattern, BC4, lower nibble then upper nibble

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NOTES:
1. RD with BC4 either by MRS or on the fly.
2. Memory Controller must drive 0 on A[1:0].
3. A[2]=0 selects lower 4 nibble bits 0....3.
4. A[2]=1 selects upper 4 nibble bits 4....7.

Figure 20 – MPR Readout of pre-defined pattern, BC4, upper nibble then lower nibble

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8.11 ACTIVE Command

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0-BA2 inputs selects the bank, and the address provided on inputs A0-A13 selects the row. This row remains active (or opens) for accesses until a precharge command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

8.12 PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (t_{RP}) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

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8.13 READ Operation

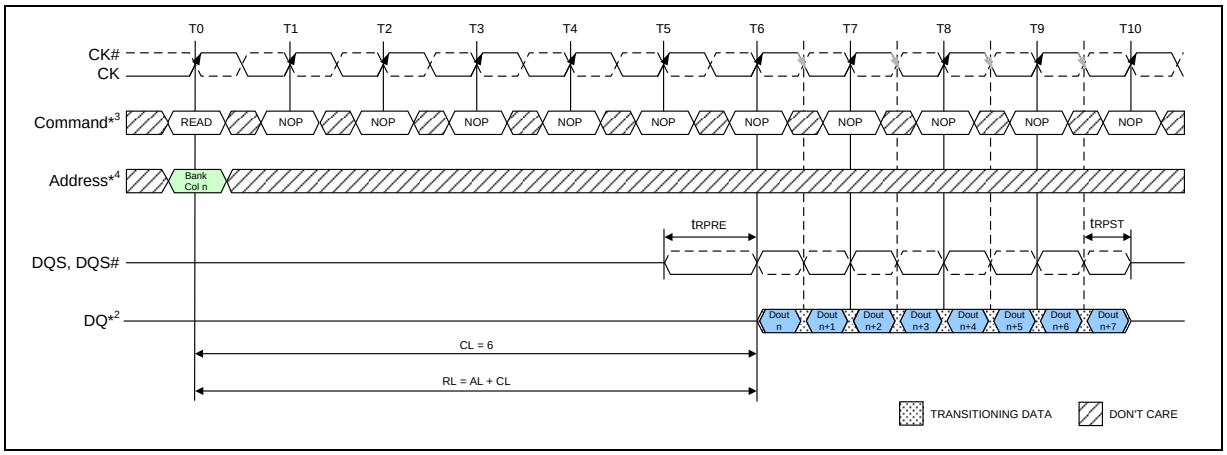
8.13.1 READ Burst Operation

During a READ or WRITE command, DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).

A12 = 0, BC4 (BC4 = burst chop, t_{CCD} = 4)

A12 = 1, BL8

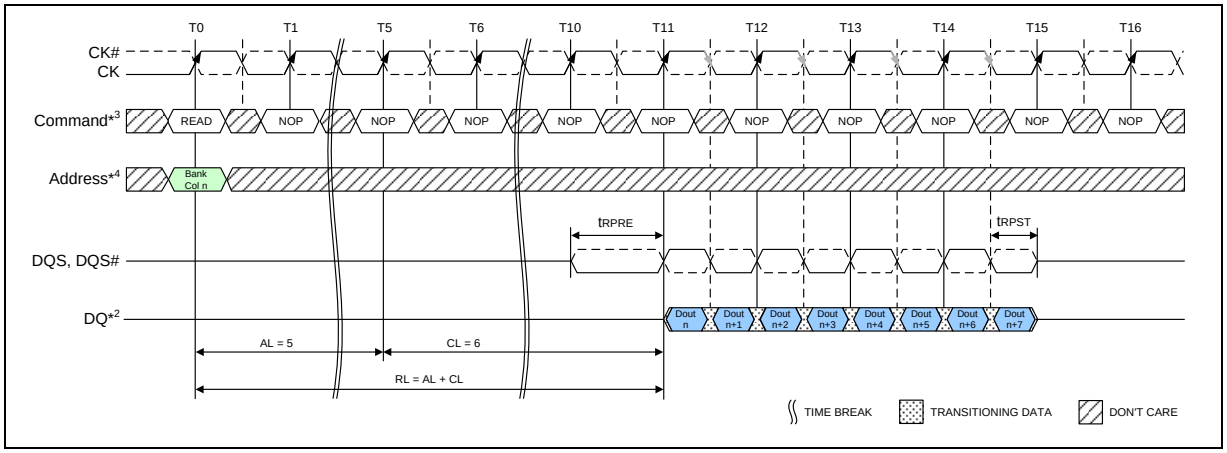
A12 is used only for burst length control, not as a column address.



Notes:

1. BL8, RL = 6, AL = 0, CL = 6.
2. Dout n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0 A[1:0] = 00 or MR0 A[1:0] = 01 and A12 = 1 during READ command at T0.

Figure 21 – READ Burst Operation RL = 6 (AL = 0, CL = 6, BL8)



Notes:

1. BL8, RL = 11, AL = (CL - 1), CL = 6.
2. Dout n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0 A[1:0] = 00 or MR0 A[1:0] = 01 and A12 = 1 during READ command at T0.

Figure 22 – READ Burst Operation RL = 11 (AL = 5, CL = 6, BL8)

8.13.2 READ Timing Definitions

Read timing is shown in Figure 23 and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

- t_{DQSCK} min/max describes the allowed range for a rising data strobe edge relative to CK, CK#.
- t_{DQSCK} is the actual position of a rising strobe edge relative to CK, CK#.
- t_{QSH} describes the DQS, DQS# differential output high time.
- t_{DQSQ} describes the latest valid transition of the associated DQ pins.
- t_{QH} describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- t_{QSL} describes the DQS, DQS# differential output low time.
- t_{DQSQ} describes the latest valid transition of the associated DQ pins.
- t_{QH} describes the earliest invalid transition of the associated DQ pins.

t_{DQSQ}; both rising/falling edges of DQS, no t_{AC} defined.

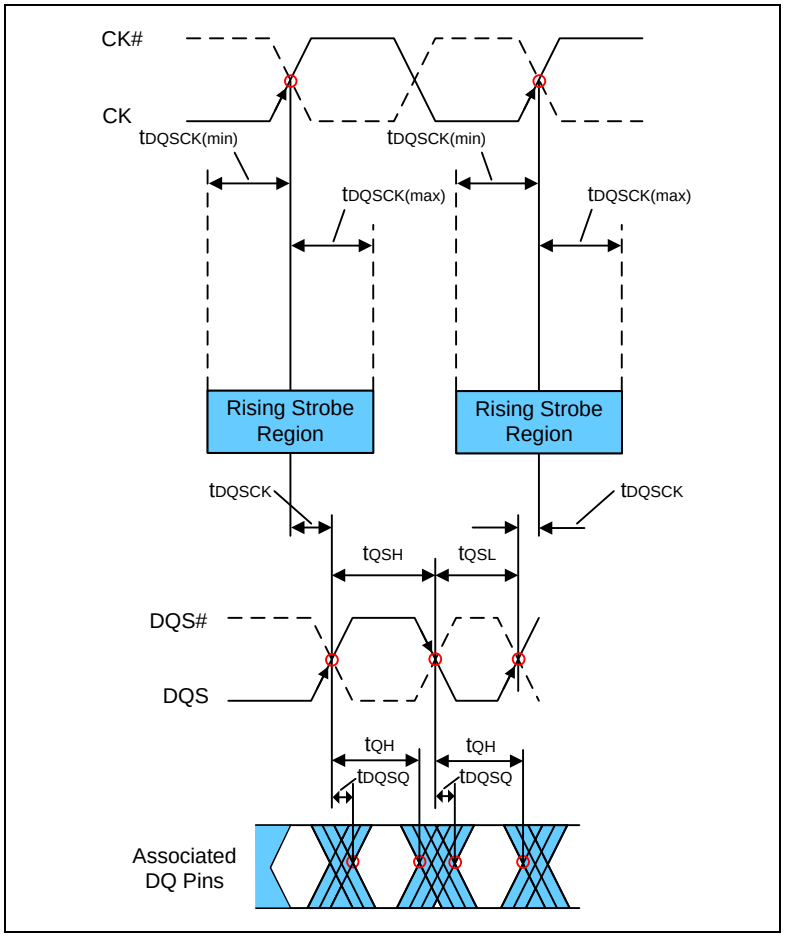


Figure 23 – READ Timing Definition

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8.13.2.1 READ Timing; Clock to Data Strobe relationship

Clock to Data Strobe relationship is shown in Figure 24 and is applied when the DLL is enabled and locked.

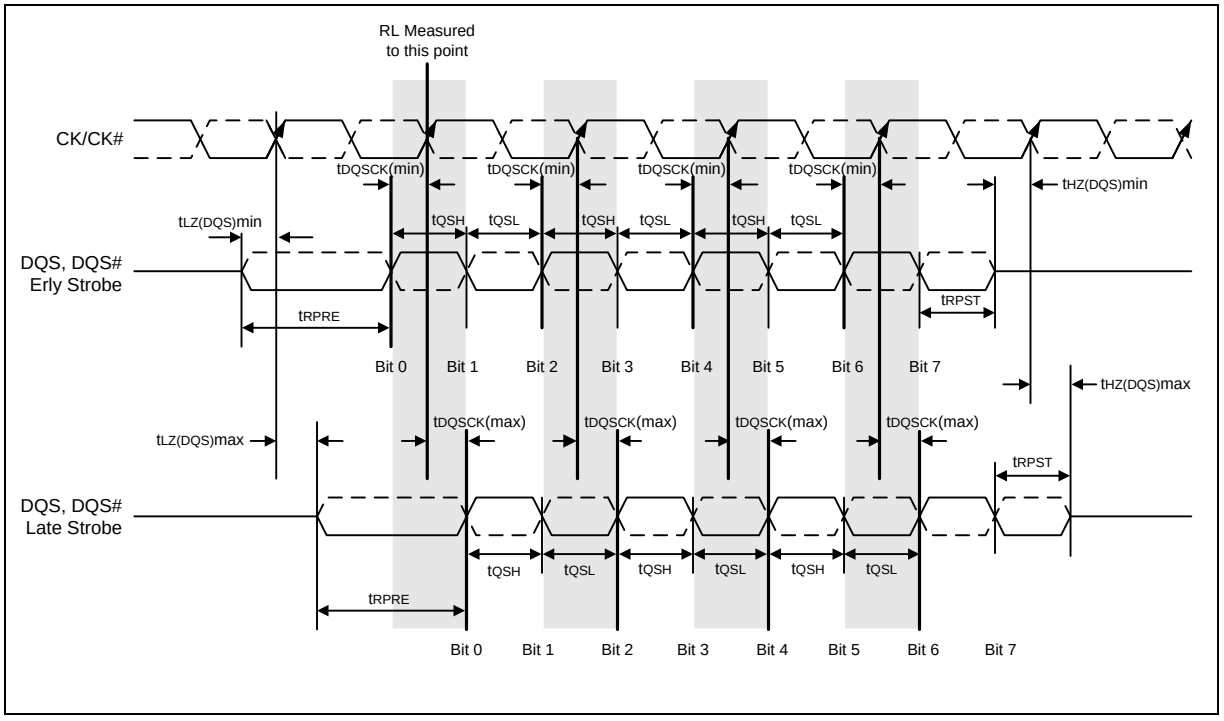
Rising data strobe edge parameters:

- tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK, CK#.
- tDQSCK is the actual position of a rising strobe edge relative to CK, CK#.
- tQSH describes the data strobe high pulse width.

Falling data strobe edge parameters:

- tQSL describes the data strobe low pulse width.

tLZ(DQS), tHZ(DQS) for preamble/postamble (see section 8.13.2.3 and Figure 26).



Notes:

1. Within a burst, rising strobe edge is not necessarily fixed to be always at tDQSCK(min) or tDQSCK(max). Instead, rising strobe edge can vary between tDQSCK(min) and tDQSCK(max).
2. Not with standing note 1, a rising strobe edge with tDQSCK(max) at T(n) can not be immediately followed by a rising strobe edge with tDQSCK(min) at T(n+1). This is because other timing relationships (tQSH, tQSL) exist:

   if tDQSCK(n+1) < 0:

   tDQSCK(n) < 1.0 tCK - (tQSHmin + tQSLmin) - | tDQSCK(n+1) |
3. The DQS, DQS# differential output high time is defined by tQSH and the DQS, DQS# differential output low time is defined by tQSL.
4. Likewise, tLZ(DQS)min and tHZ(DQS)min are not tied to tDQSCK,min (early strobe case) and tLZ(DQS)max and tHZ(DQS)max are not tied to tDQSCK,max (late strobe case).
5. The minimum pulse width of read preamble is defined by tRPRE(min).
6. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZDSQ(max) on the right side.
7. The minimum pulse width of read postamble is defined by tRPST(min).
8. The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side.

Figure 24 – Clock to Data Strobe Relationship

8.13.2.2 READ Timing; Data Strobe to Data relationship

The Data Strobe to Data relationship is shown in Figure 25 and is applied when the DLL is enabled and locked.

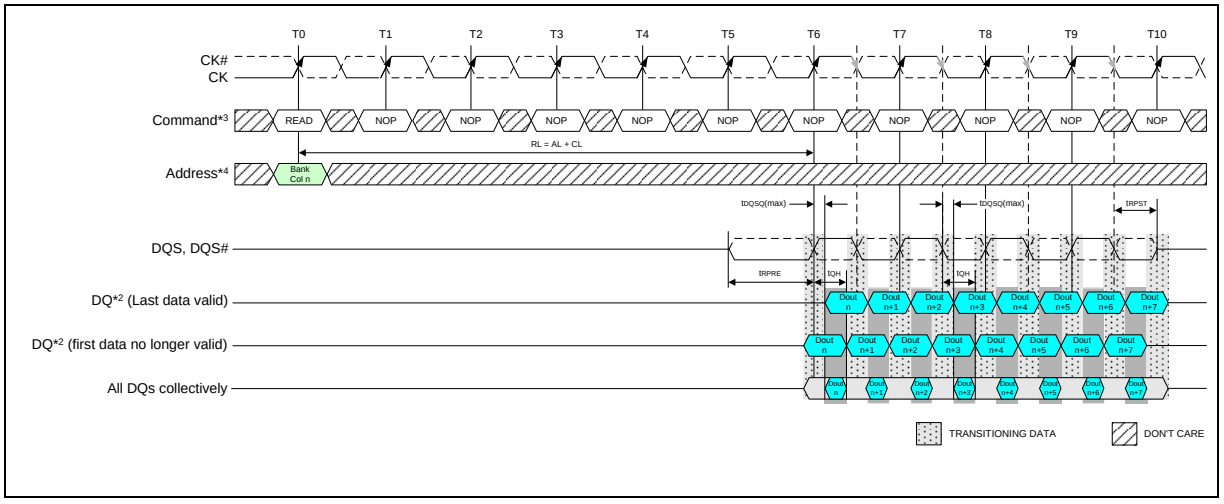
Rising data strobe edge parameters:

- t_{DQSQ} describes the latest valid transition of the associated DQ pins.
- t_{QH} describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- t_{DQSQ} describes the latest valid transition of the associated DQ pins.
- t_{QH} describes the earliest invalid transition of the associated DQ pins.

t_{DQSQ}; both rising/falling edges of DQS, no t_{AC} defined.



Notes:

1. BL = 8, RL = 6 (AL = 0, CL = 6).
2. Dout n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0 A[1:0] = 00 or MR0 A[1:0] = 01 and A12 = 1 during READ command at T0.
5. Output timings are referenced to $V_{DDQ}/2$, and DLL on for locking.
6. t_{DQSQ} defines the skew between DQS, DQS# to Data and does not define DQS, DQS# to Clock.
7. Early Data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

Figure 25 – Data Strobe to Data Relationship

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8.13.2.3 $t_{LZ(DQS)}$, $t_{LZ(DQ)}$, $t_{HZ(DQS)}$, $t_{HZ(DQ)}$ Calculation

t_{HZ} and t_{LZ} transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving $t_{HZ(DQS)}$ and $t_{HZ(DQ)}$, or begins driving $t_{LZ(DQS)}$, $t_{LZ(DQ)}$. Figure 26 shows a method to calculate the point when the device is no longer driving $t_{HZ(DQS)}$ and $t_{HZ(DQ)}$, or begins driving $t_{LZ(DQS)}$, $t_{LZ(DQ)}$, by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters $t_{LZ(DQS)}$, $t_{LZ(DQ)}$, $t_{HZ(DQS)}$, and $t_{HZ(DQ)}$ are defined as singled ended.

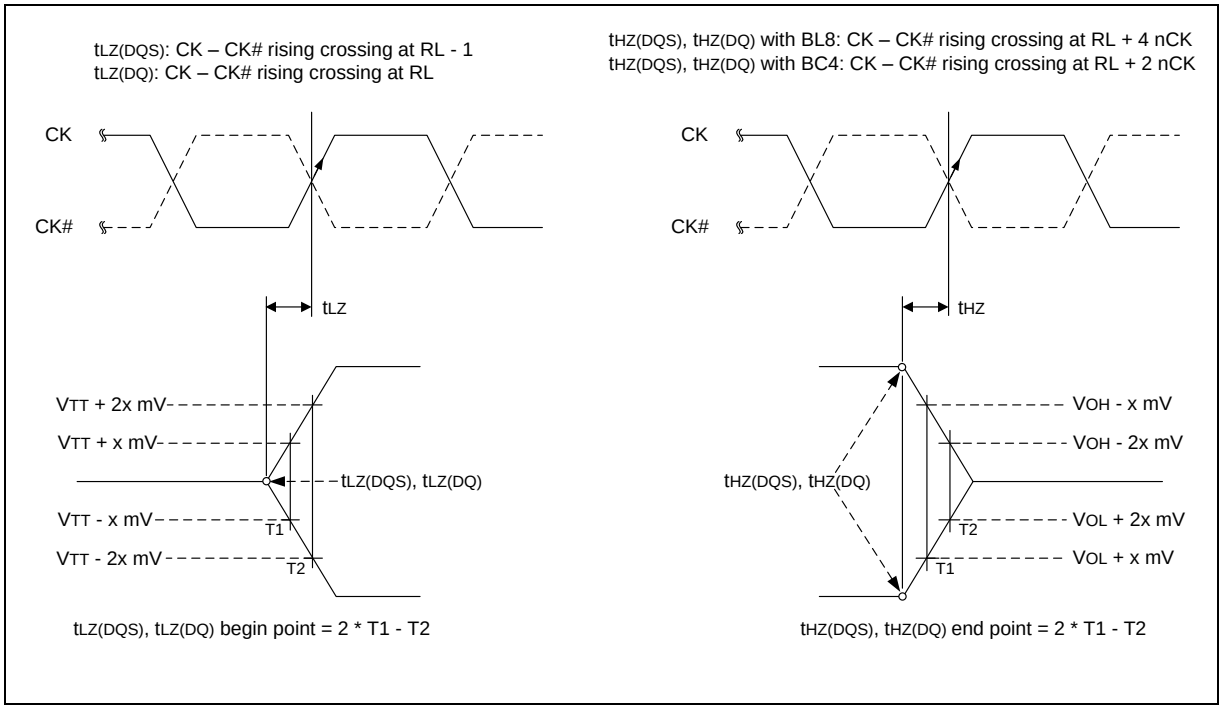


Figure 26 – t_{LZ} and t_{HZ} method for calculating transitions and endpoints

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8.13.2.4 tRPRE Calculation

The method for calculating differential pulse widths for tRPRE is shown in Figure 27.

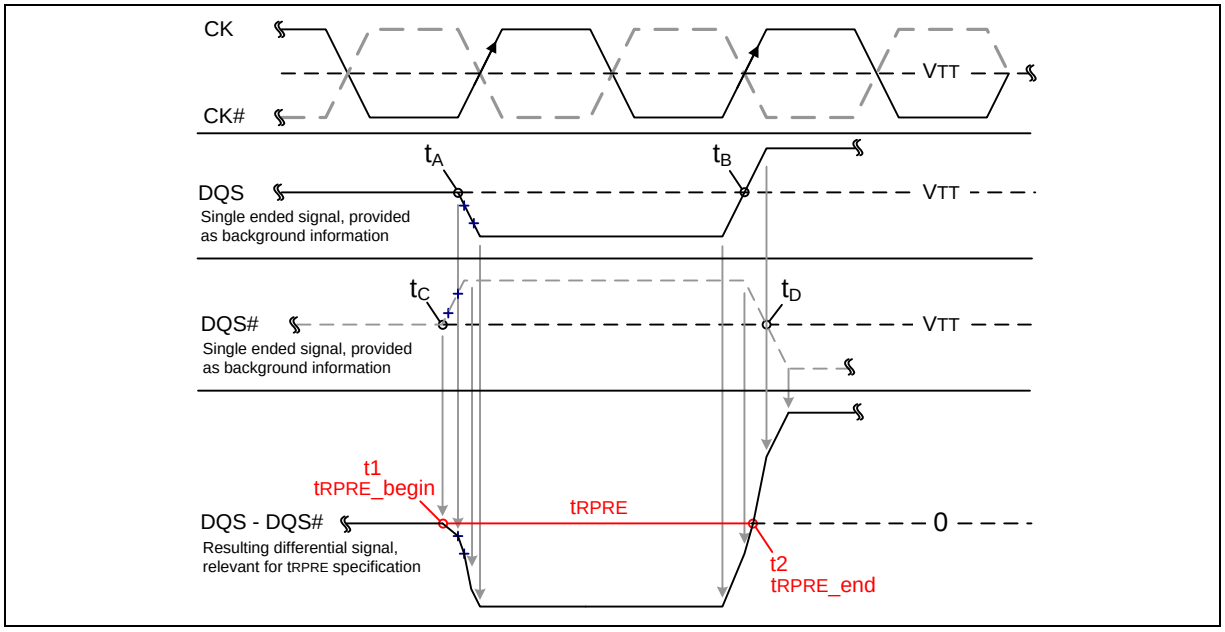


Figure 27 – Method for calculating tRPRE transitions and endpoints

8.13.2.5 tRPST Calculation

The method for calculating differential pulse widths for tRPST is shown in Figure 28.

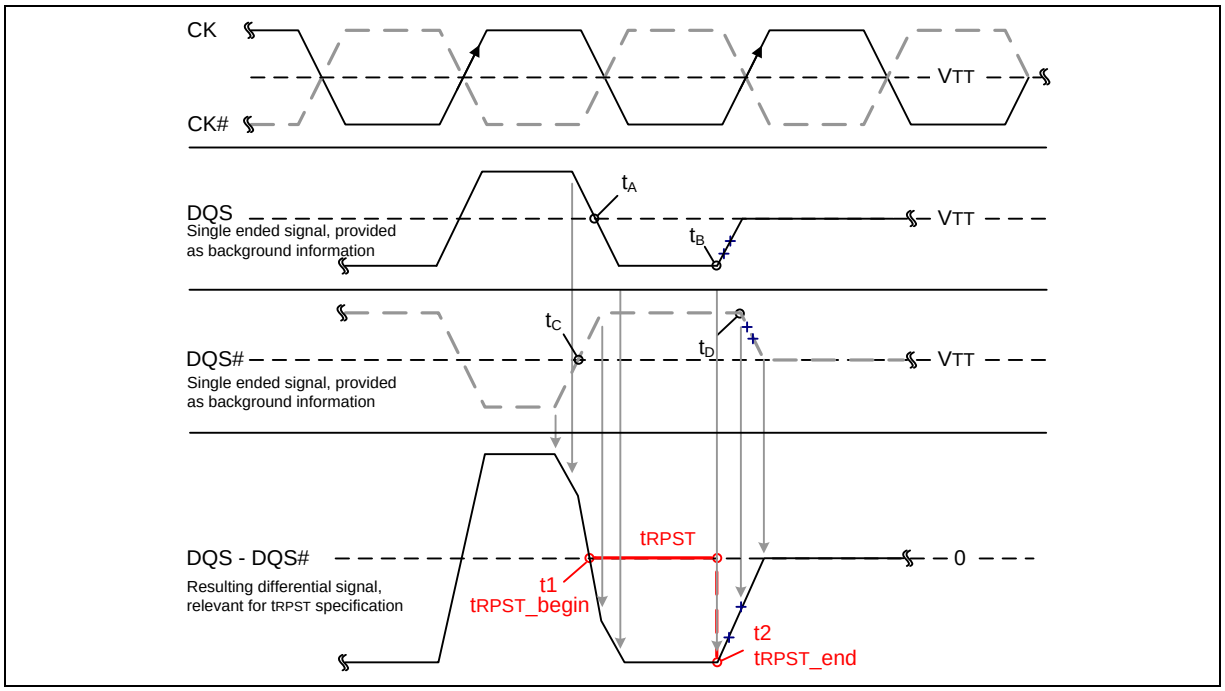


Figure 28 – Method for calculating tRPST transitions and endpoints

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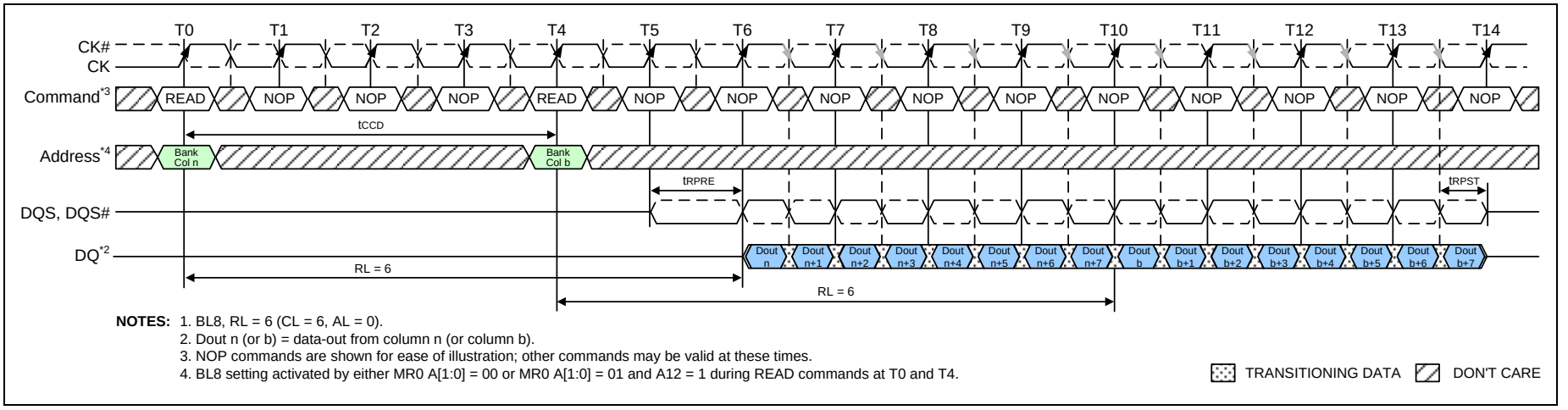


Figure 29 – READ (BL8) to READ (BL8)

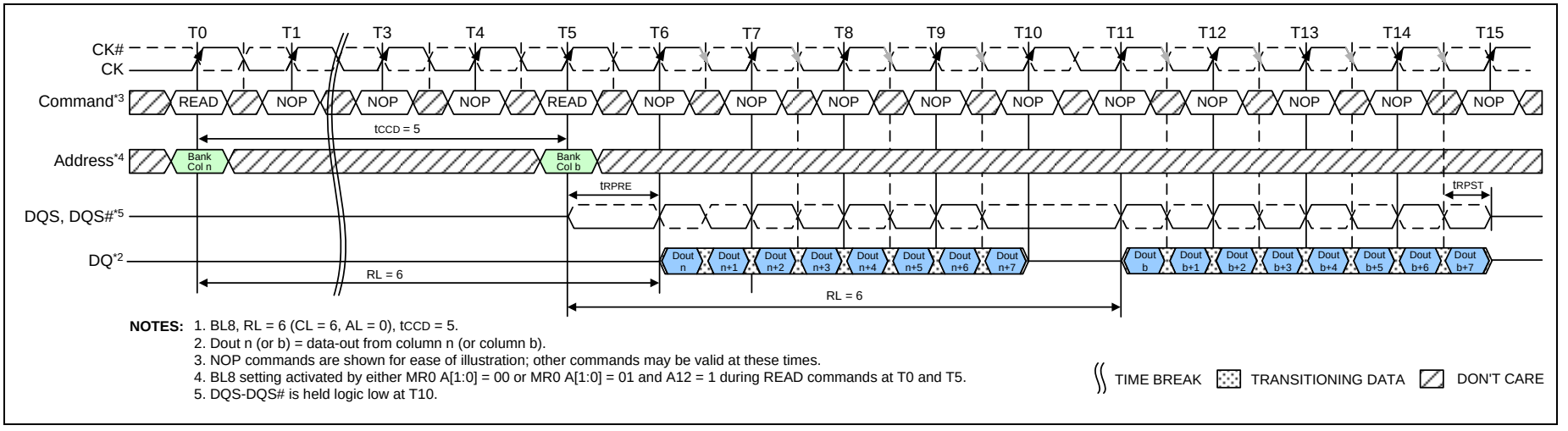


Figure 30 – Nonconsecutive READ (BL8) to READ (BL8), tCCD=5

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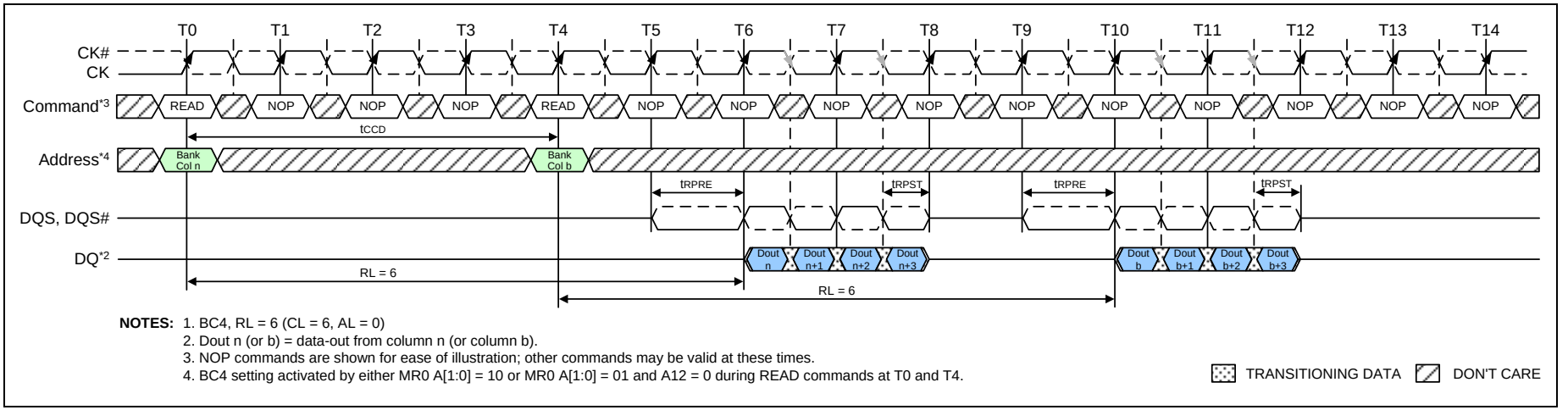


Figure 31 – READ (BC4) to READ (BC4)

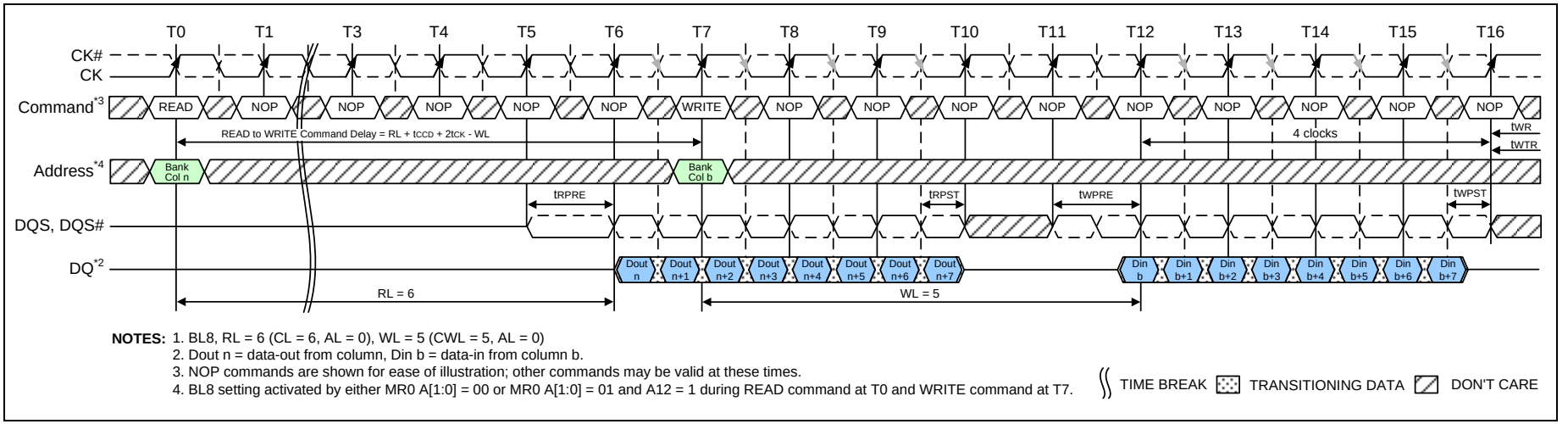


Figure 32 – READ (BL8) to WRITE (BL8)

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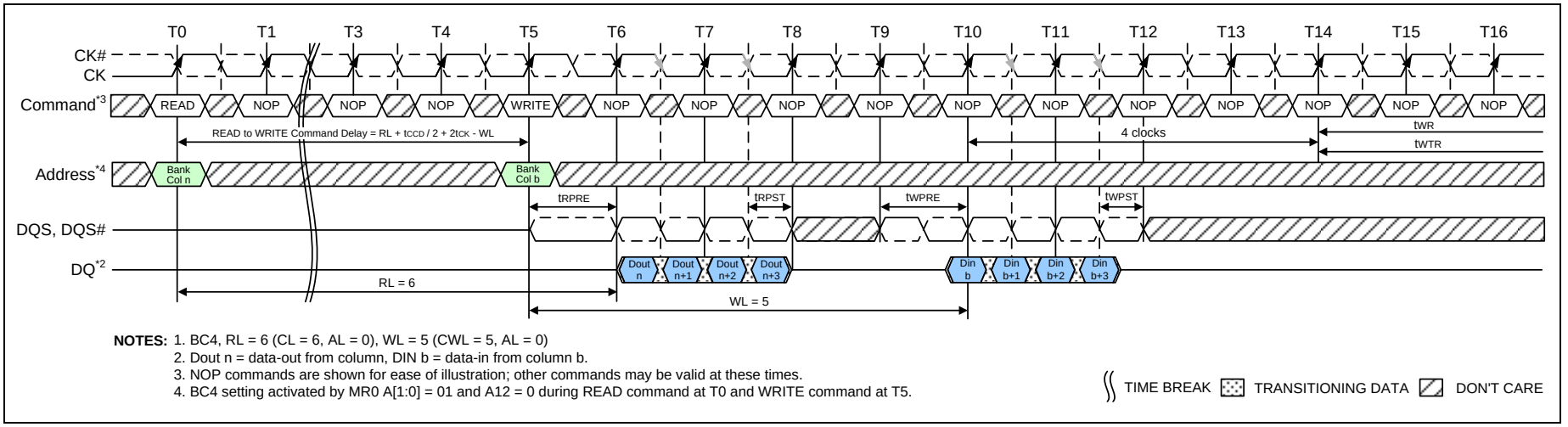


Figure 33 – READ (BC4) to WRITE (BC4) OTF

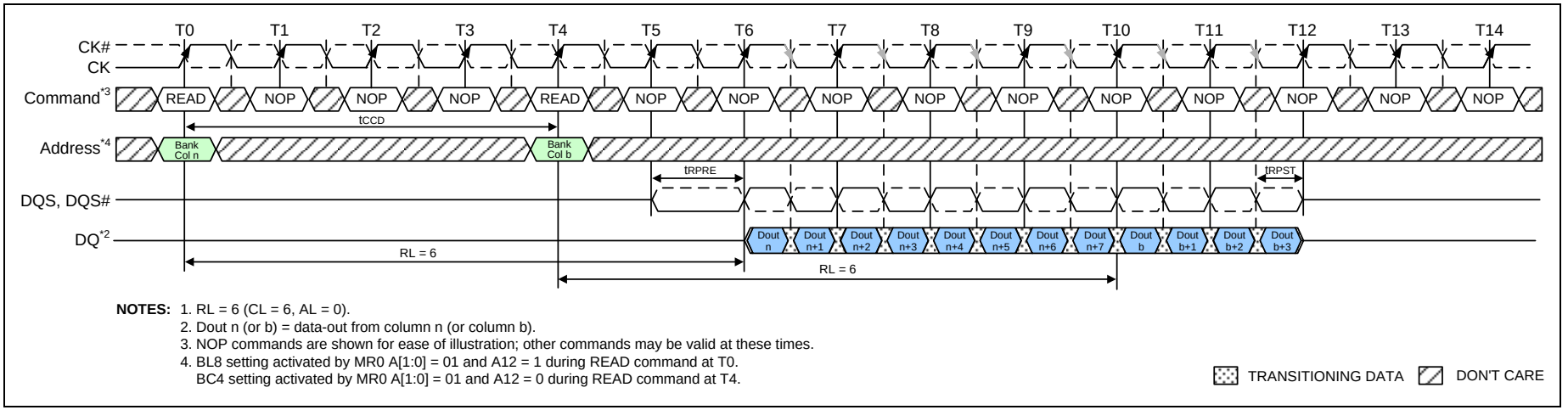


Figure 34 – READ (BL8) to READ (BC4) OTF

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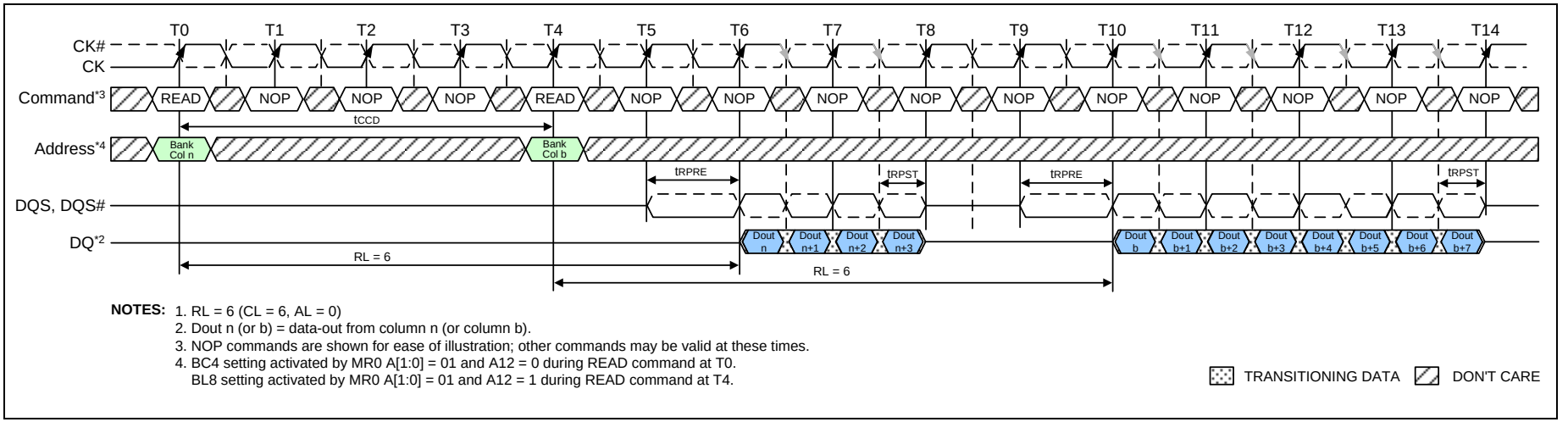


Figure 35 – READ (BC4) to READ (BL8) OTF

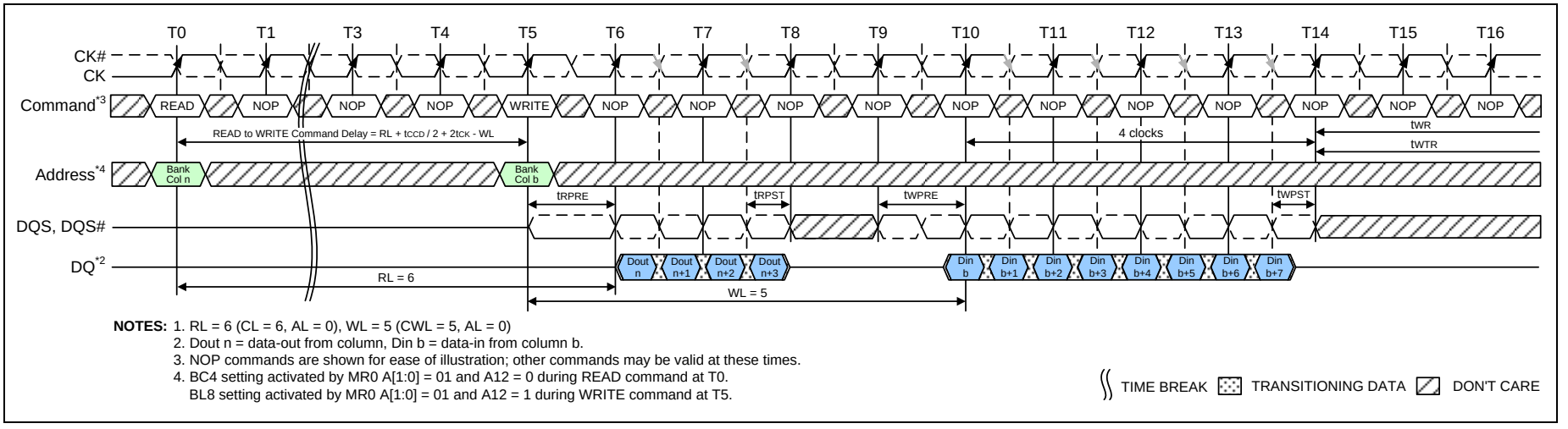


Figure 36 – READ (BC4) to WRITE (BL8) OTF

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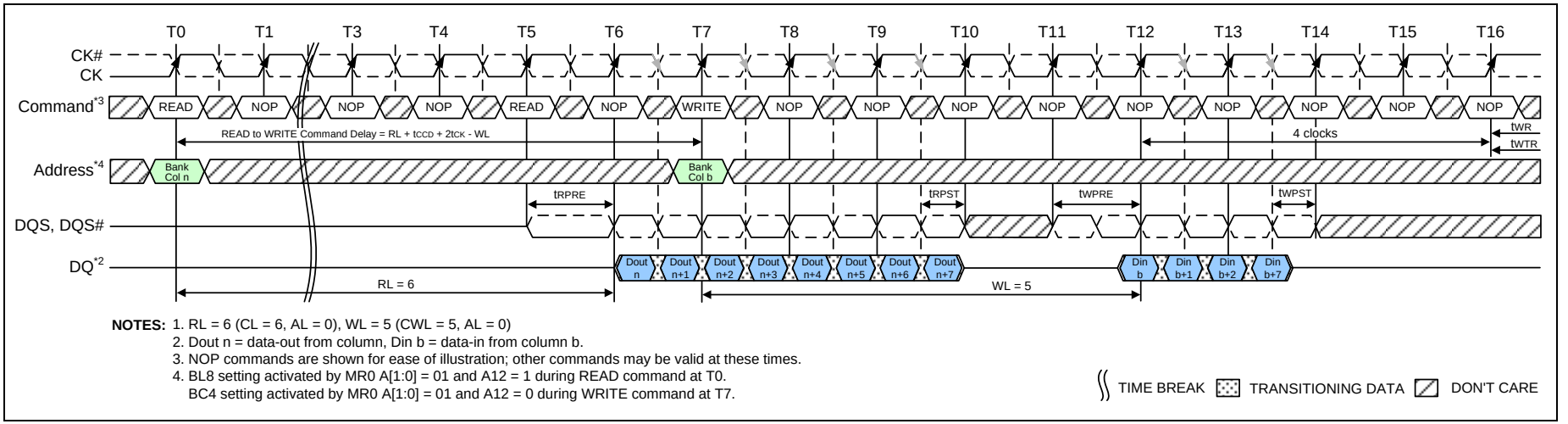


Figure 37 – READ (BL8) to WRITE (BC4) OTF

8.13.2.6 Burst Read Operation followed by a Precharge

The minimum external Read command to Precharge command spacing to the same bank is equal to AL + t_{RTP} with t_{RTP} being the Internal Read Command to Precharge Command Delay. Note that the minimum ACT to PRE timing, $t_{RAS.MIN}$ must be satisfied as well. The minimum value for the Internal Read Command to Precharge Command Delay is given by $t_{RTP.MIN}$ = max(4 × nCK, 7.5 nS). A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

1. The minimum RAS precharge time ($t_{RP.MIN}$) has been satisfied from the clock at which the precharge begins.
2. The minimum RAS cycle time ($t_{RC.MIN}$) from the previous bank activation has been satisfied.

Examples of Read commands followed by Precharge are show in Figure 38 and Figure 39.

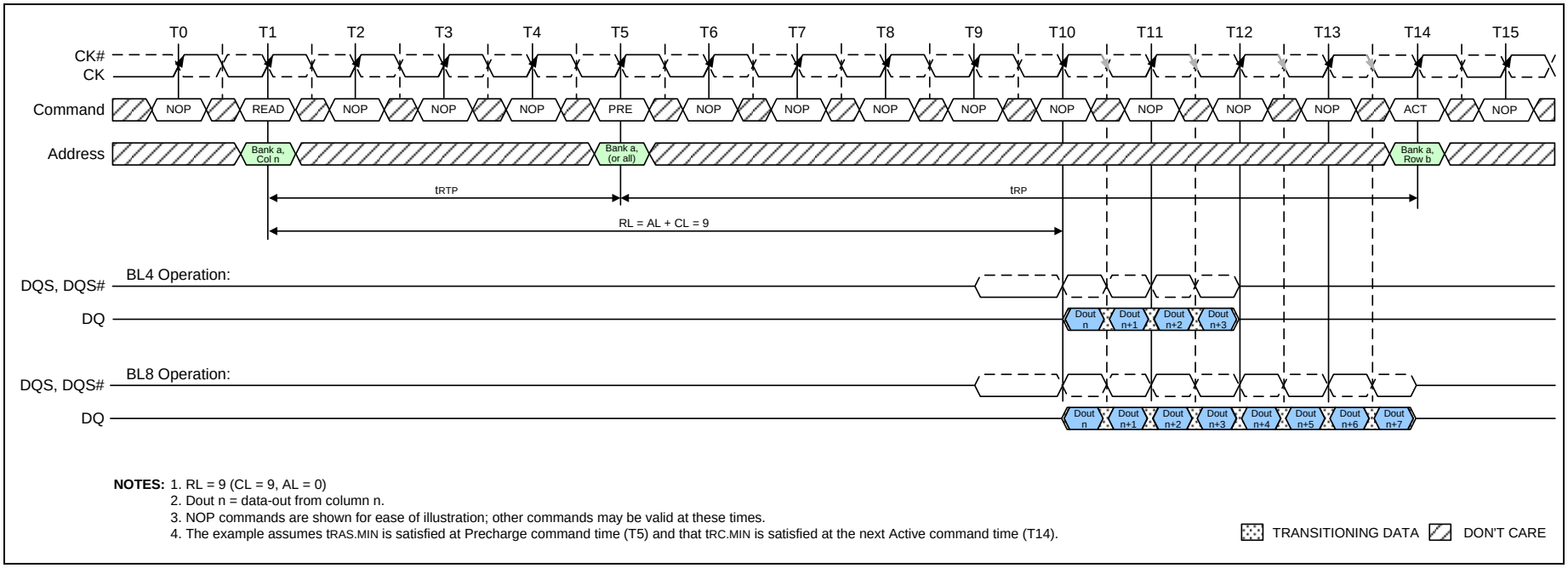


Figure 38 – READ to PRECHARGE (RL = 9, AL = 0, CL = 9, t_{RTP} = 4, t_{RP} = 9)

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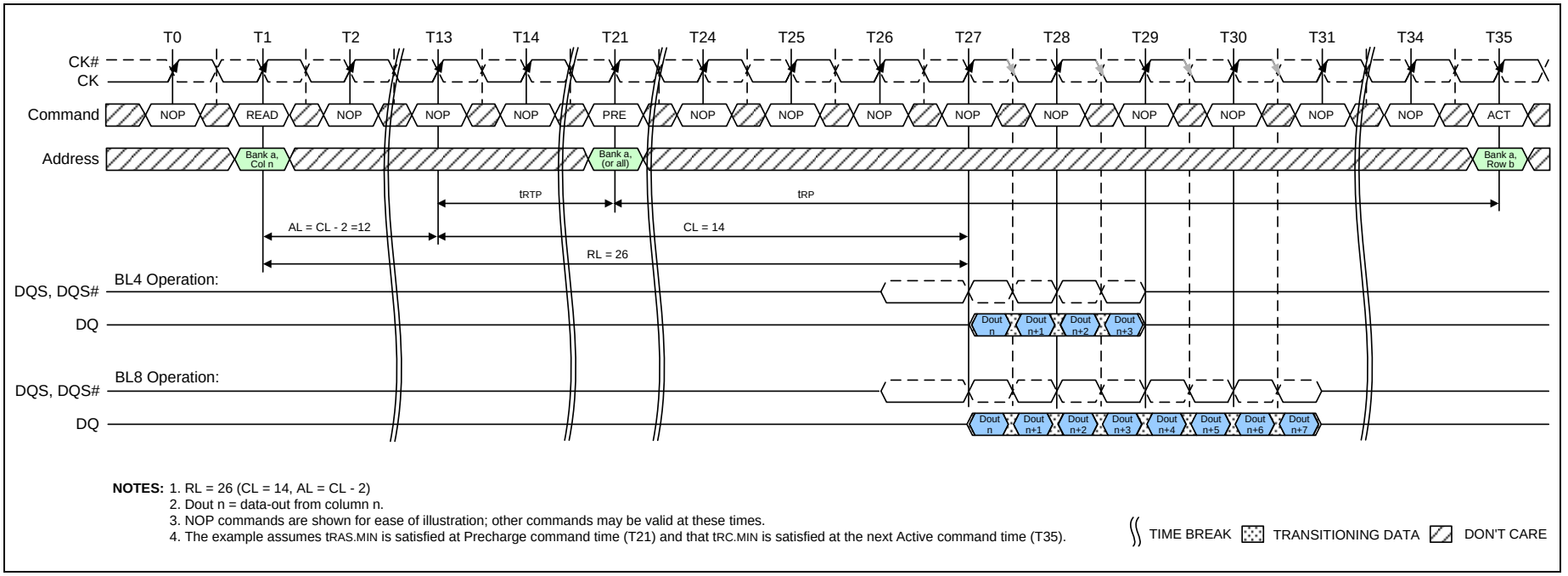


Figure 39 – READ to PRECHARGE (RL = 26, AL = CL-2, CL = 14, t_{RTP} = 8, t_{RP} = 14)

8.14 WRITE Operation

8.14.1 DDR3 Burst Operation

During a READ or WRITE command, DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).

A12 = 0, BC4 (BC4 = burst chop, t_{CCD} = 4)

A12 = 1, BL8

A12 is used only for burst length control, not as a column address.

8.14.2 WRITE Timing Violations

8.14.2.1 Motivation

Generally, if timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure that the DRAM works properly. However, it is desirable; for certain minor violations, that the DRAM is guaranteed not to “hang up”, and that errors are limited to that particular operation.

For the following, it will be assumed that there are no timing violations with regards to the Write command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

8.14.2.2 Data Setup and Hold Violations

Should the data to strobe timing requirements (t_{DS}, t_{DH}) be violated, for any of the strobe edges associated with a write burst, and then wrong data might be written to the memory location addressed with this WRITE command.

In the example (Figure 40 on page 57), the relevant strobe edges for write burst A are associated with the clock edges: T5, T5.5, T6, T6.5, T7, T7.5, T8, T8.5.

Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

8.14.2.3 Strobe to Strobe and Strobe to Clock Violations

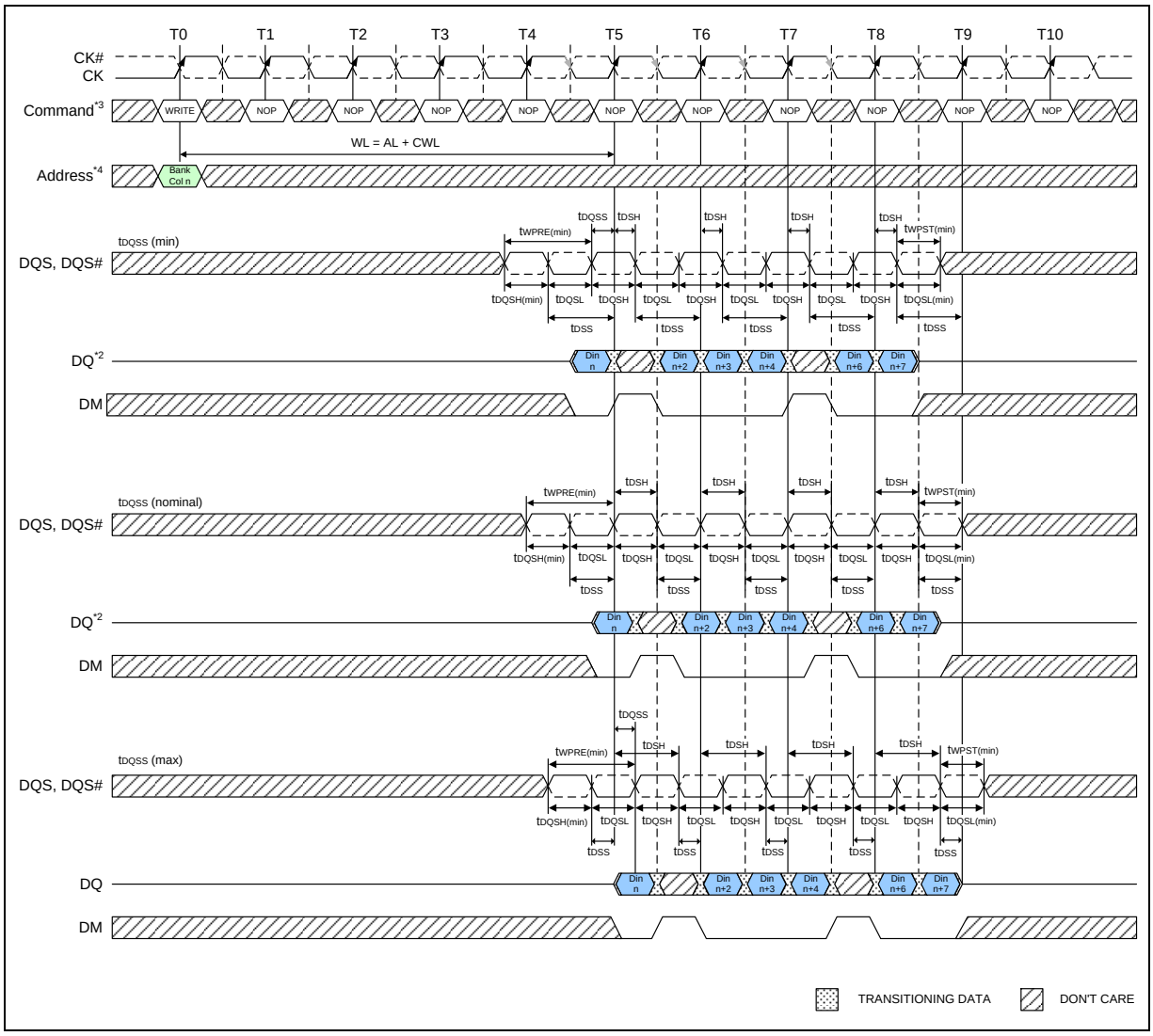
Should the strobe timing requirements (t_{DQSH}, t_{DQSL}, t_{WPRE}, t_{WPST}) or the strobe to clock timing requirements (t_{DSS}, t_{DSH}, t_{DQSS}) be violated, for any of the strobe edges associated with a Write burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

In the example (Figure 48 on page 61) the relevant strobe edges for Write burst *n* are associated with the clock edges: T4, T4.5, T5, T5.5, T6, T6.5, T7, T7.5, T8, T8.5 and T9. Any timing requirements starting or ending on one of these strobe edges need to be fulfilled for a valid burst. For Write burst b the relevant edges are T8, T8.5, T9, T9.5, T10, T10.5, T11, T11.5, T12, T12.5 and T13. Some edges are associated with both bursts.

8.14.2.4 Write Timing Parameters

This drawing is for example only to enumerate the strobe edges that “belong” to a Write burst. No actual timing violations are shown here. For a valid burst all timing parameters for each edge of a burst need to be satisfied (not only for one edge - as shown).

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Notes:

1. BL8, WL = 5 (AL = 0, CWL = 5)
2. Din n = data-in from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0 A[1:0] = 00 or MR0 A[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. tDQSS must be met at each rising clock edge.

Figure 40 – Write Timing Definition and Parameters

8.14.3 Write Data Mask

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR3 SDRAMs, consistent with the implementation on DDR2 SDRAMs. It has identical timings on write operations as the data bits as shown in Figure 40, and though used in a unidirectional manner, is internally loaded identically to data bits to ensure matched system timing. DM is not used during read cycles, however, DM can be used as TDQS during write cycles if enabled by the MR1[A11] setting. See section 8.3.2.7 **"TDQS, TDQS#"** on page 21 for more details on TDQS vs. DM operations.

8.14.4 tWPRE Calculation

The method for calculating differential pulse widths for tWPRE is shown in Figure 41.

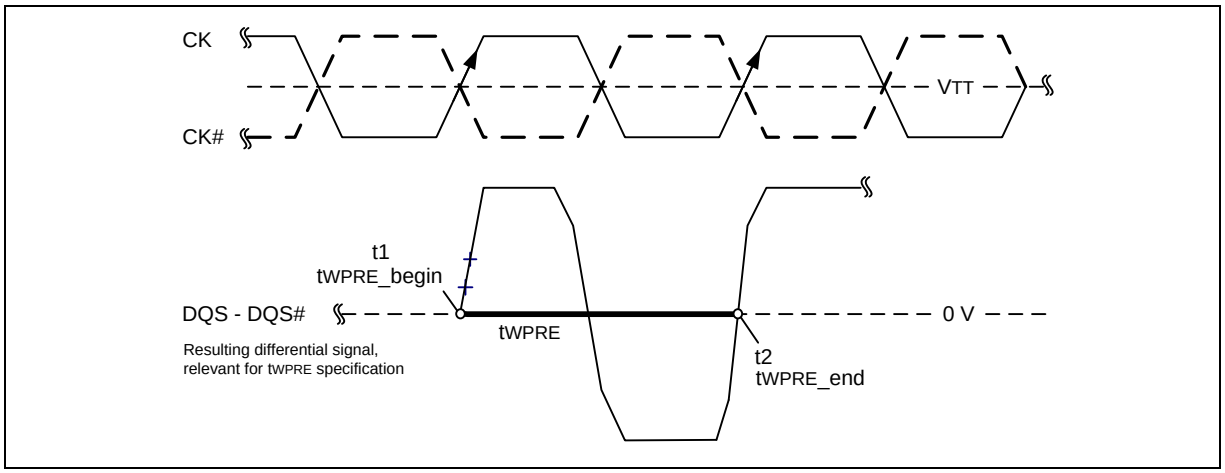


Figure 41 – Method for calculating tWPRE transitions and endpoints

8.14.5 tWPST Calculation

The method for calculating differential pulse widths for tWPST is shown in Figure 42.

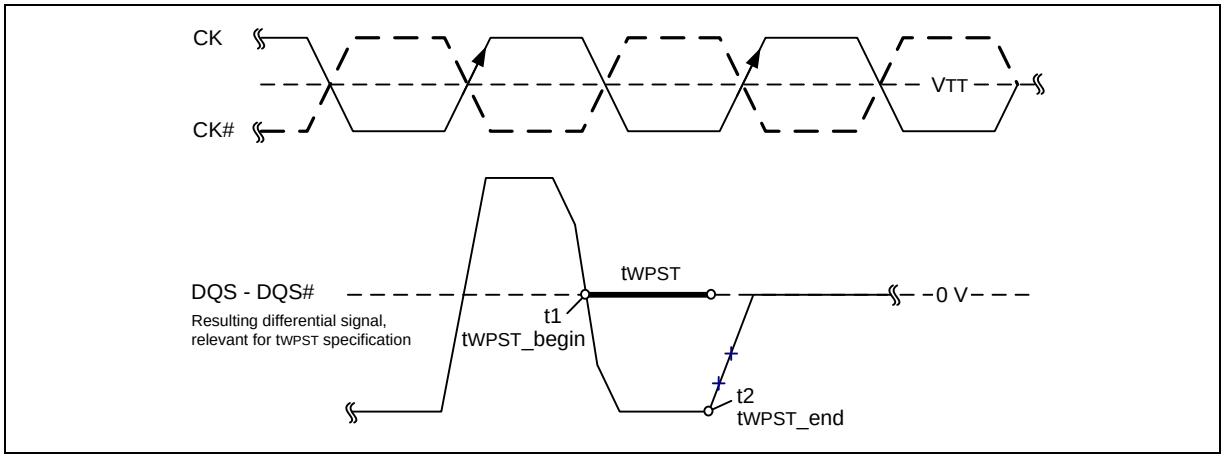
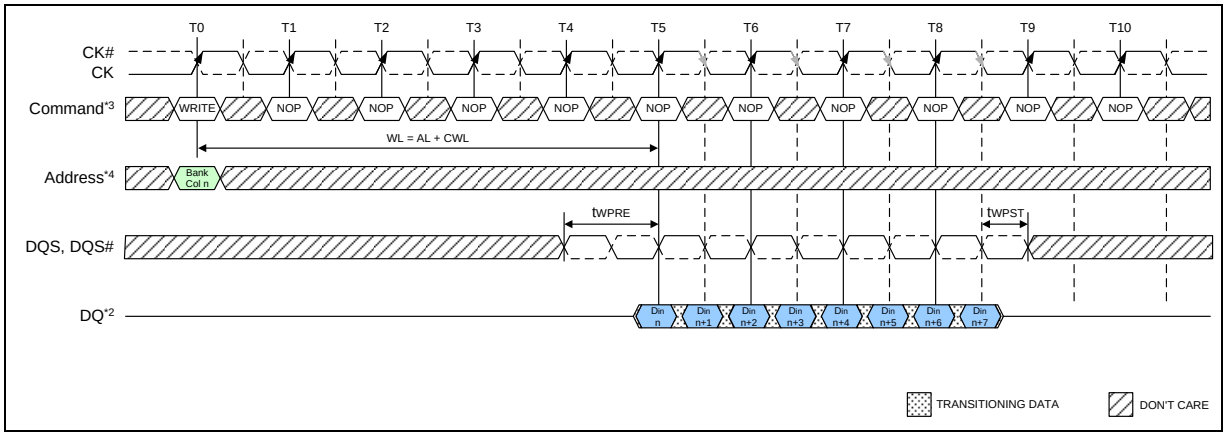


Figure 42 – Method for calculating tWPST transitions and endpoints

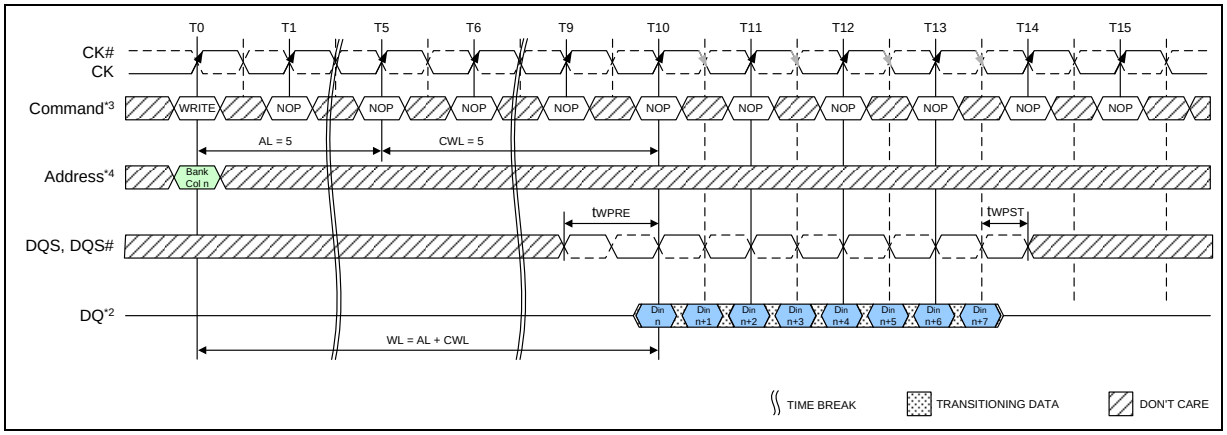
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Notes:

1. BL8, WL = 5; AL = 0, CWL = 5.
2. Din n = data-in from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0 A[1:0] = 00 or MR0 A[1:0] = 01 and A12 = 1 during WRITE command at T0.

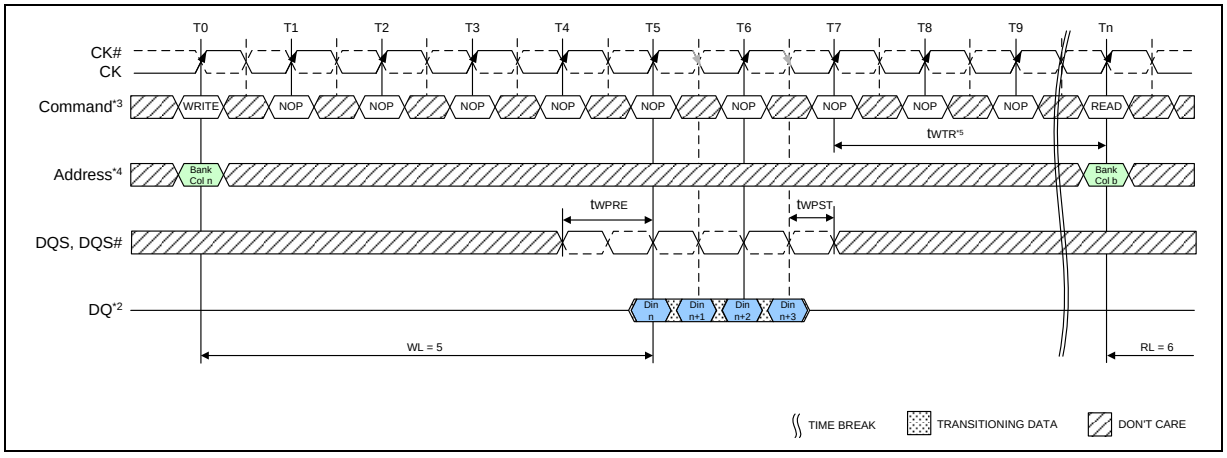
Figure 43 – WRITE Burst Operation WL = 5 (AL = 0, CWL = 5, BL8)



Notes:

1. BL8, WL = 10; AL = CL - 1, CL = 6, CWL = 5.
2. Din n = data-in from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0 A[1:0] = 00 or MR0 A[1:0] = 01 and A12 = 1 during WRITE command at T0.

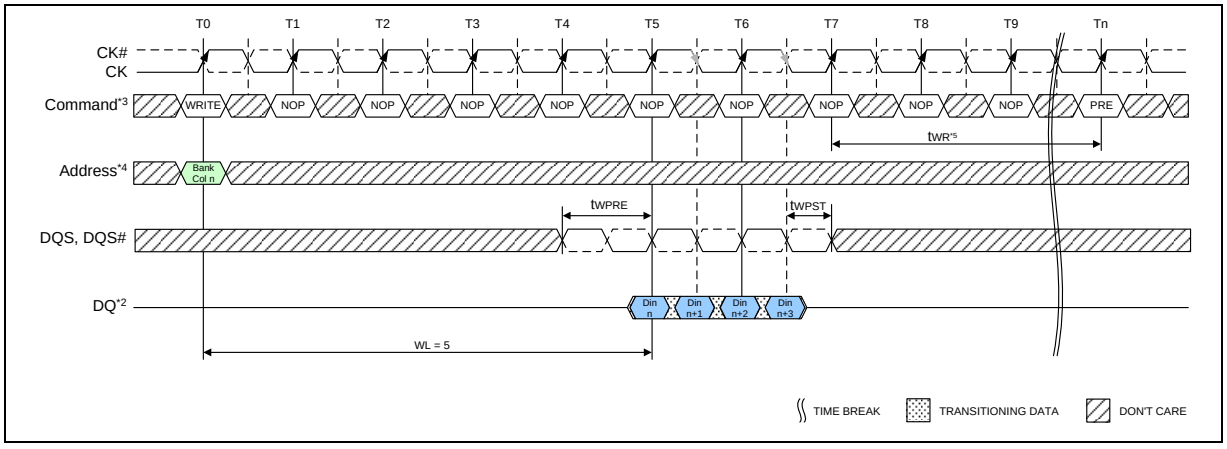
Figure 44 – WRITE Burst Operation WL = 10 (AL = CL-1, CWL = 5, BL8)



Notes:

1. BC4, WL = 5, RL = 6.
2. Din n = data-in from column n; Dout b = data-out from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0 A[1:0] = 10 during WRITE command at T0 and READ command at Tn.
5. tWTR controls the write to read delay to the same device and starts with the first rising clock edge after the last write data shown at T7.

Figure 45 – WRITE (BC4) to READ (BC4) Operation



Notes:

1. BC4, WL = 5, RL = 6.
2. Din n = data-in from column n; Dout b = data-out from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0 A[1:0] = 10 during WRITE command at T0.
5. The write recovery time (tWR) referenced from the first rising clock edge after the last write data shown at T7. tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

Figure 46 – WRITE (BC4) to PRECHARGE Operation

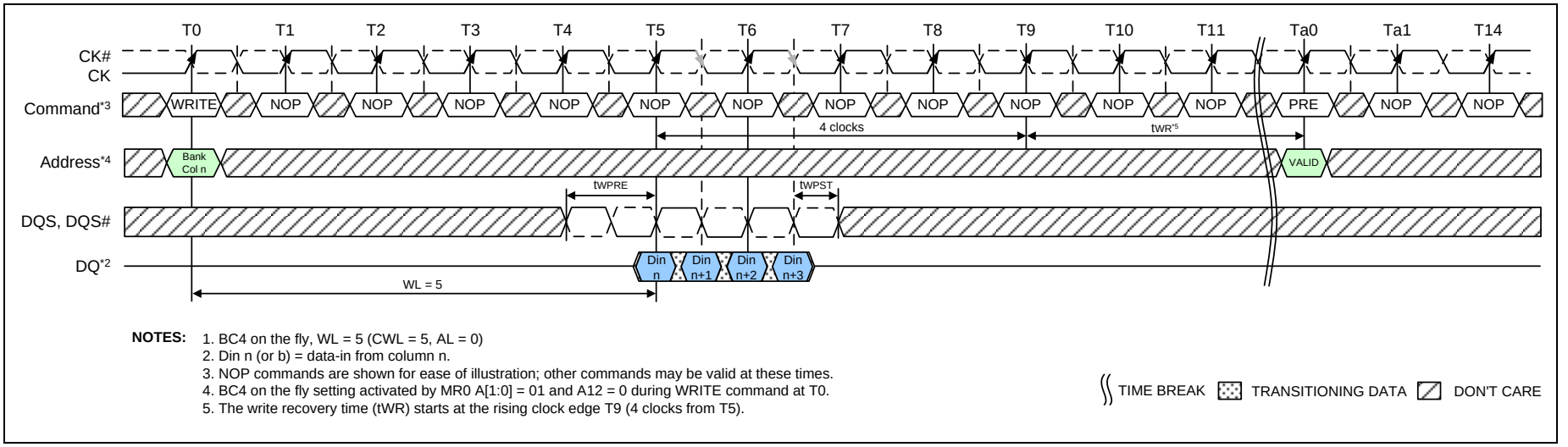


Figure 47 – WRITE (BC4) OTF to PRECHARGE Operation

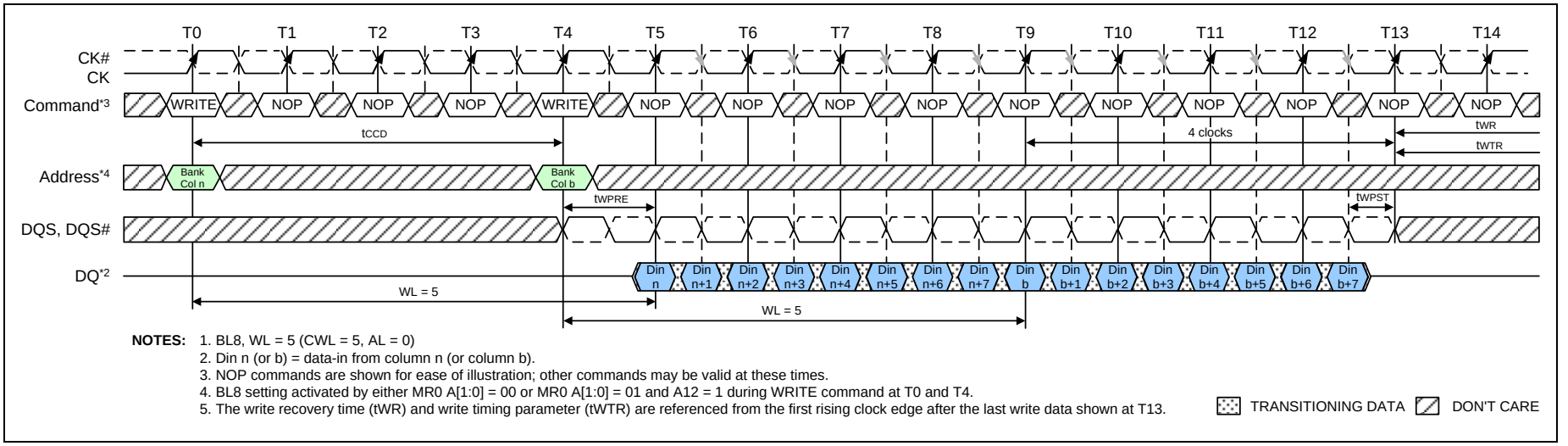


Figure 48 – WRITE (BL8) to WRITE (BL8)

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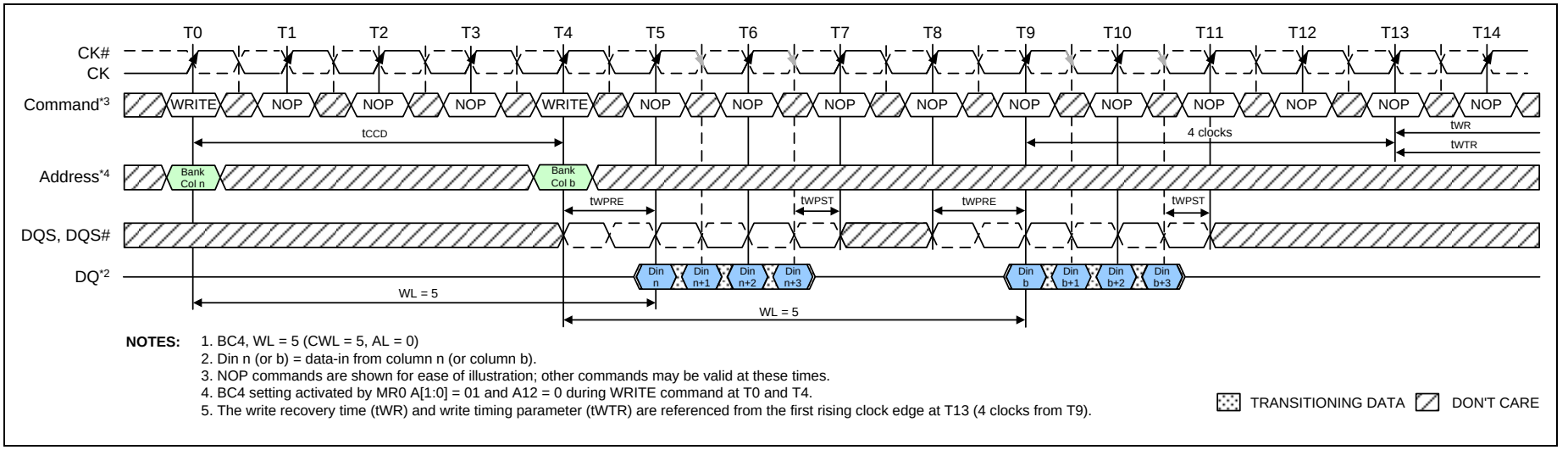


Figure 49 – WRITE (BC4) to WRITE (BC4) OTF

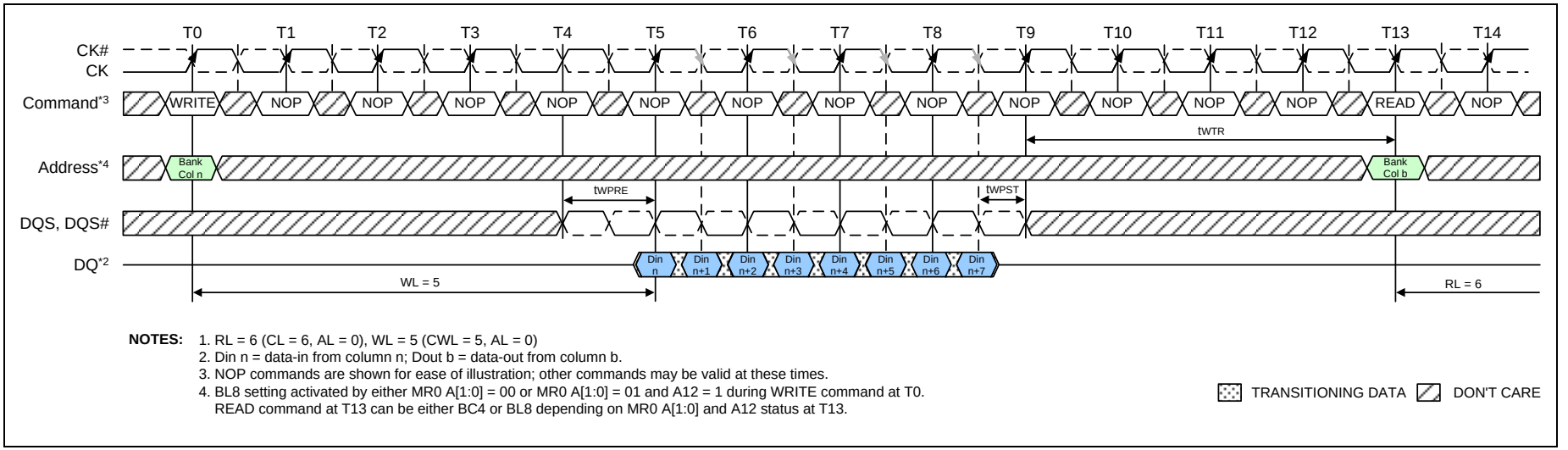


Figure 50 – WRITE (BL8) to READ (BC4/BL8) OTF

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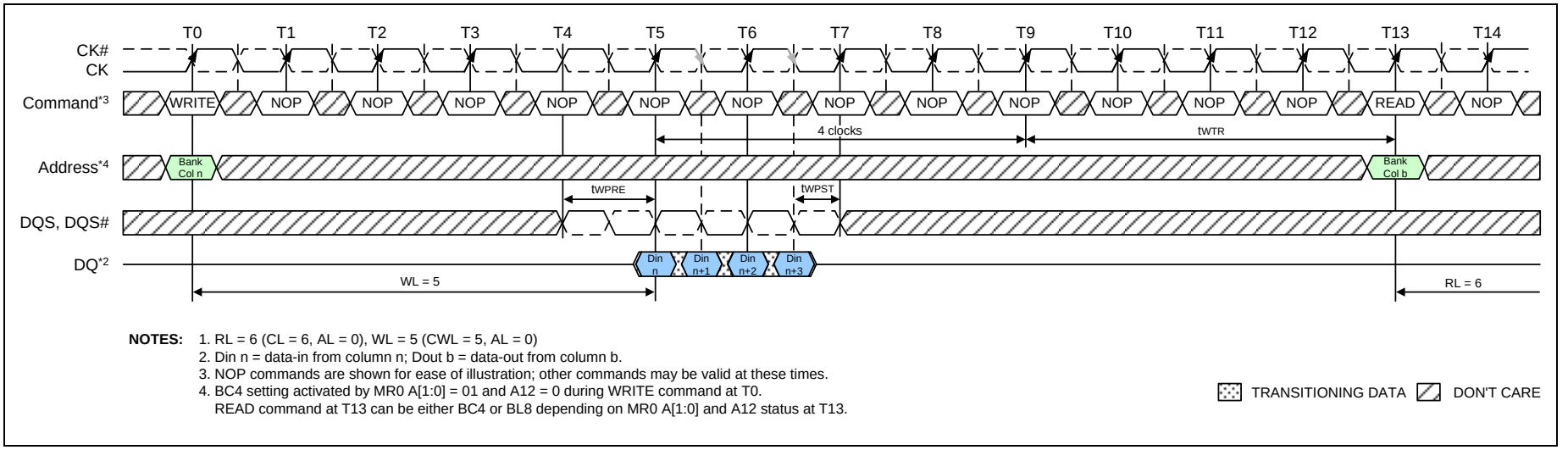


Figure 51 – WRITE (BC4) to READ (BC4/BL8) OTF

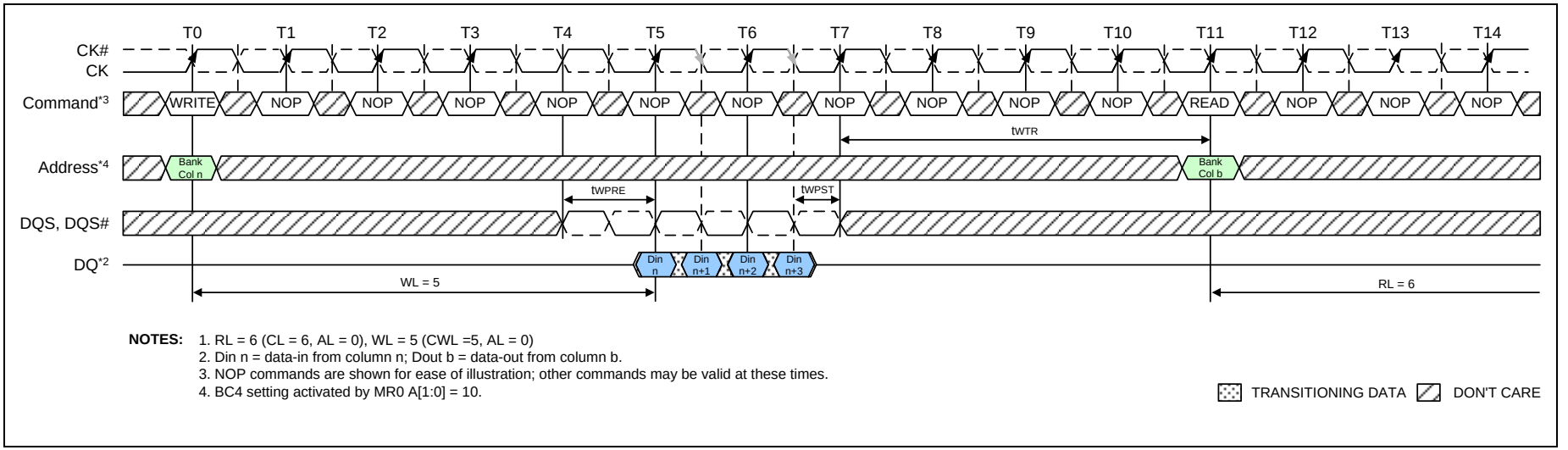


Figure 52 – WRITE (BC4) to READ (BC4)

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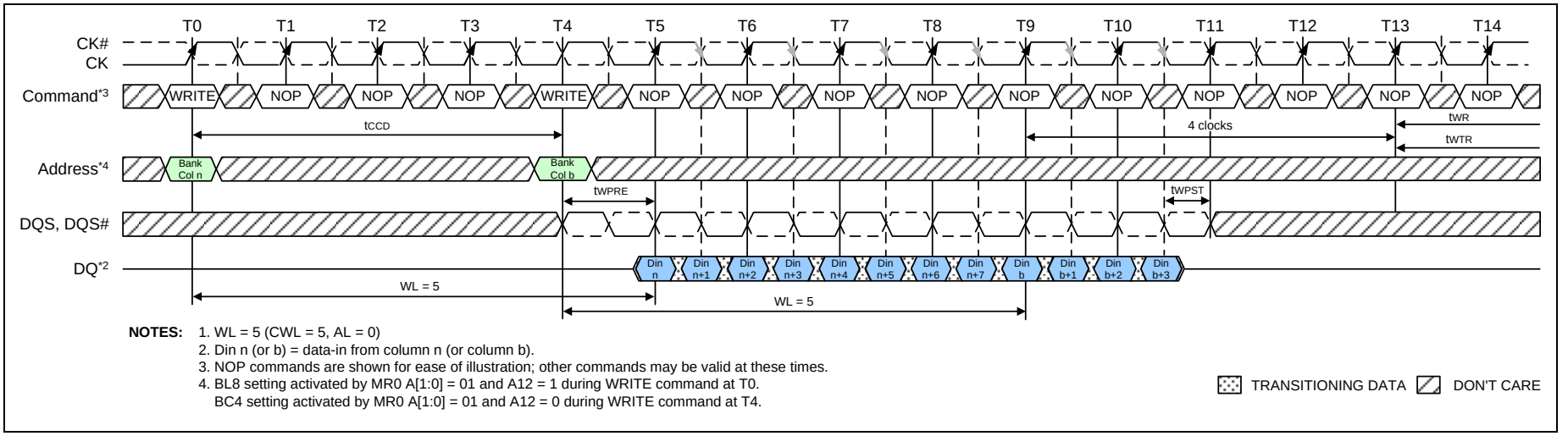


Figure 53 – WRITE (BL8) to WRITE (BC4) OTF

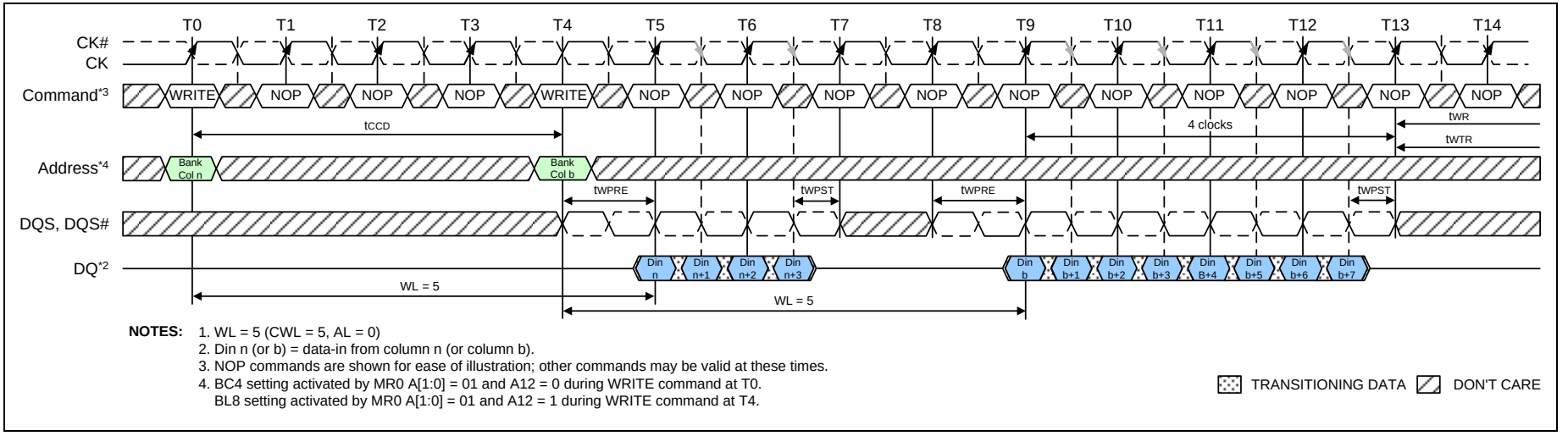


Figure 54 – WRITE (BC4) to WRITE (BL8) OTF

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8.15 Refresh Command

The Refresh command (REF) is used during normal operation of the DDR3 SDRAMs. This command is non persistent, so it must be issued each time a refresh is required. The DDR3 SDRAM requires Refresh cycles at an average periodic interval of t_{REFI}. When CS#, RAS# and CAS# are held Low and WE# High at the rising edge of the clock, the chip enters a Refresh cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time t_{RP}(min) before the Refresh Command can be applied. The refresh addressing is generated by the internal refresh controller. This makes the address bits “Don't Care” during a Refresh command. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started. When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Refresh Command and the next valid command, except NOP or DES, must be greater than or equal to the minimum Refresh cycle time t_{RFC}(min) as shown in Figure 55. Note that the t_{RFC} timing parameter depends on memory density.

In general, a Refresh command needs to be issued to the DDR3 SDRAM regularly every t_{REFI} interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands can be postponed during operation of the DDR3 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 × t_{REFI} (see Figure 56). A maximum of 8 additional Refresh commands can be issued in advance (“pulled in”), with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 9 × t_{REFI} (see Figure 57). At any given time, a maximum of 16 REF commands can be issued within 2 x t_{REFI}. Self-Refresh Mode may be entered with a maximum of eight Refresh commands being postponed. After exiting Self-Refresh Mode with one or more Refresh commands postponed, additional Refresh commands may be postponed to the extent that the total number of postponed Refresh commands (before and after the Self-Refresh) will never exceed eight. During Self-Refresh Mode, the number of postponed or pulled-in REF commands does not change.

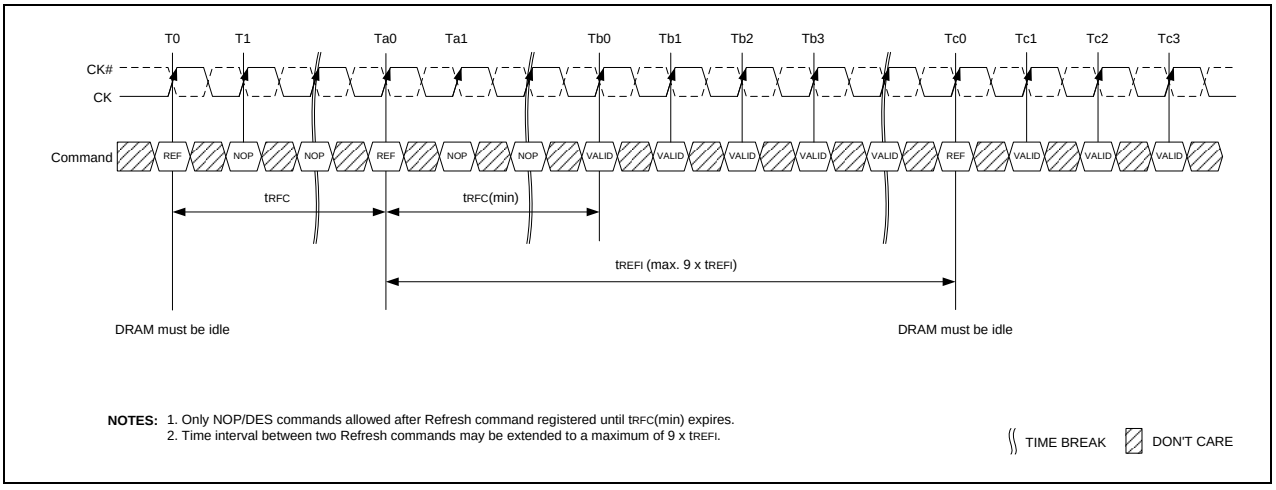


Figure 55 – Refresh Command Timing

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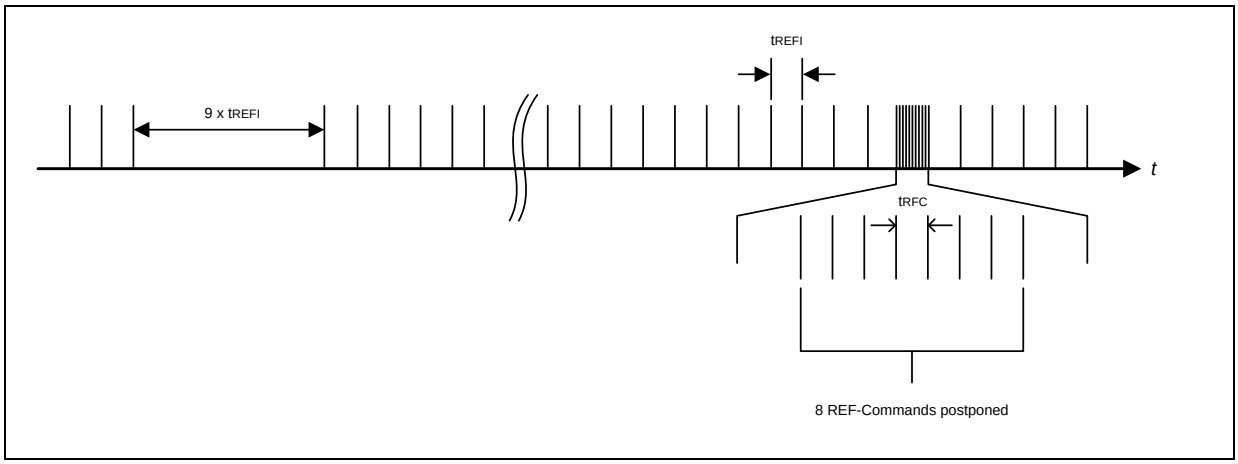


Figure 56 – Postponing Refresh Commands (Example)

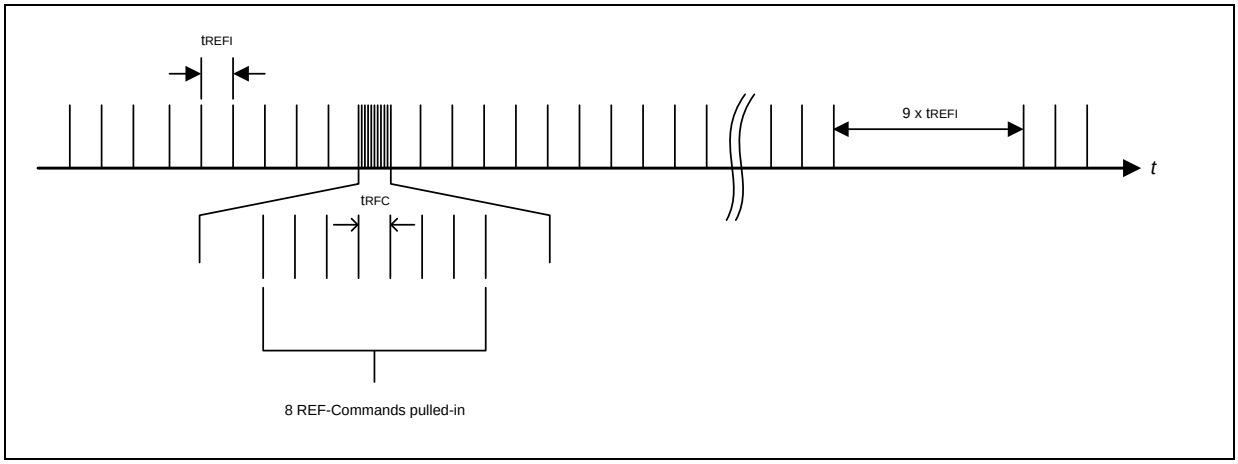


Figure 57 – Pulling-in Refresh Commands (Example)

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8.16 Self-Refresh Operation

The Self-Refresh command can be used to retain data in the DDR3 SDRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR3 SDRAM retains data without external clocking. The DDR3 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh-Entry (SRE) Command is defined by having CS#, RAS#, CAS#, and CKE held low with WE# high at the rising edge of the clock.

Before issuing the Self-Refresh-Entry command, the DDR3 SDRAM must be idle with all bank precharge state with t_{RP} satisfied. 'Idle state' is defined as all banks are closed (t_{RP}, t_{DAL}, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (t_{MRD}, t_{MOD}, t_{RFC}, t_{ZQ}init, t_{ZQ}oper, t_{ZQCS}, etc.) Also, on-die termination must be turned off before issuing Self-Refresh-Entry command, by either registering ODT pin low "ODTL + 0.5t_{CK}" prior to the Self-Refresh Entry command or using MRS to MR1 command. Once the Self-Refresh Entry command is registered, CKE must be held low to keep the device in Self-Refresh mode. During normal operation (DLL on), MR1 (A0 = 0), the DLL is automatically disabled upon entering Self-Refresh and is automatically enabled (including a DLL-Reset) upon exiting Self-Refresh.

When the DDR3 SDRAM has entered Self-Refresh mode, all of the external control signals, except CKE and RESET#, are "don't care." For proper Self-Refresh operation, all power supply and reference pins (V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ}, V_{REFCA} and V_{REFDQ}) must be at valid levels. V_{REFDQ} supply may be turned OFF and V_{REFDQ} may take any value between V_{SS} and V_{DD} during Self Refresh operation, provided that V_{REFDQ} is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh. The DRAM initiates a minimum of one Refresh command internally within t_{CKE} period once it enters Self-Refresh mode.

The clock is internally disabled during Self-Refresh Operation to save power. The minimum time that the DDR3 SDRAM must remain in Self-Refresh mode is t_{CKESR}. The user may change the external clock frequency or halt the external clock t_{CKSRE} after Self-Refresh entry is registered, however, the clock must be restarted and stable t_{CKSRX} before the device can exit Self-Refresh operation.

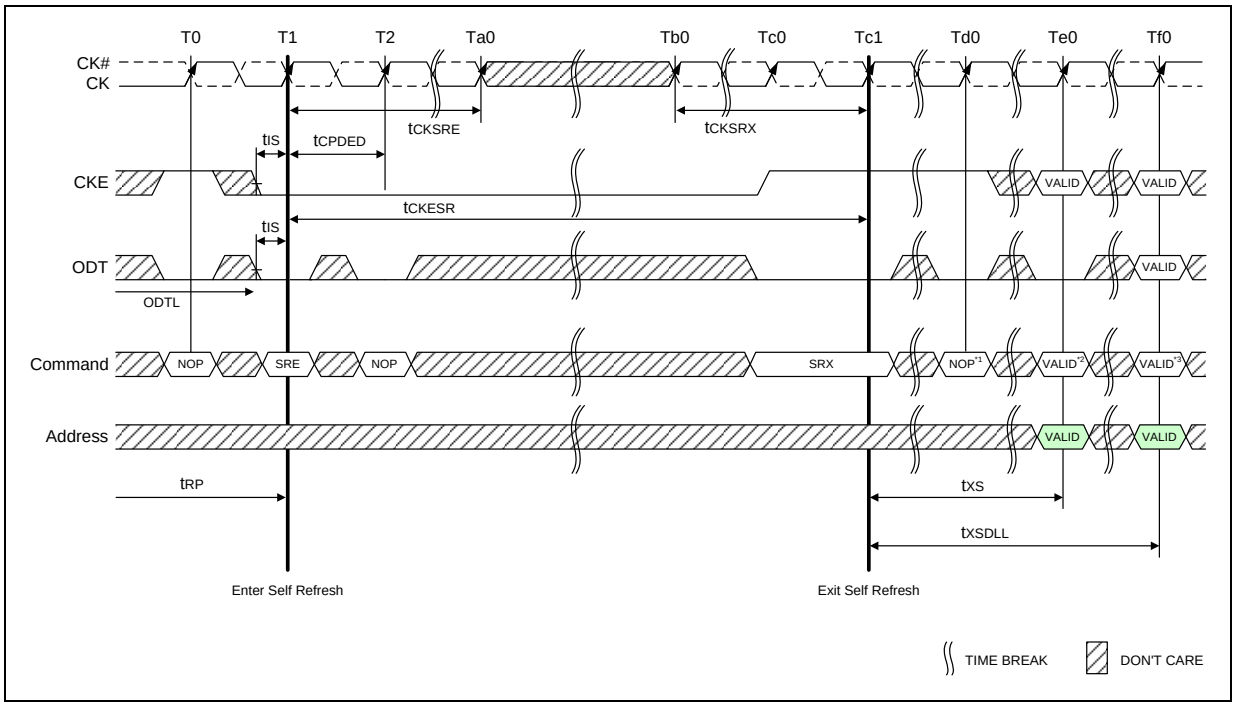
The procedure for exiting Self-Refresh requires a sequence of events. First, the clock must be stable prior to CKE going back HIGH. Once a Self-Refresh Exit command (SRX, combination of CKE going high and either NOP or Deselect on command bus) is registered, a delay of at least t_{XS} must be satisfied before a valid command not requiring a locked DLL can be issued to the device to allow for any internal refresh in progress. Before a command that requires a locked DLL can be applied, a delay of at least t_{XSDLL} must be satisfied.

Depending on the system environment and the amount of time spent in Self-Refresh, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in section 8.18 **"ZQ Calibration Commands"** on page 77. To issue ZQ calibration commands, applicable timing requirements must be satisfied (See Figure 72 - **"ZQ Calibration Timing"** on page 78).

CKE must remain HIGH for the entire Self-Refresh exit period t_{XSDLL} for proper operation except for Self-Refresh re-entry. Upon exit from Self-Refresh, the DDR3 SDRAM can be put back into Self-Refresh mode after waiting at least t_{XS} period and issuing one refresh command (refresh period of t_{RFC}). NOP or deselect commands must be registered on each positive clock edge during the Self-Refresh exit interval t_{XS}. ODT must be turned off during t_{XSDLL}.

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The use of Self-Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self-Refresh mode. Upon exit from Self-Refresh, the DDR3 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode.



Notes:

1. Only NOP or DES command.
2. Valid commands not requiring a locked DLL.
3. Valid commands requiring a locked DLL.

Figure 58 – Self-Refresh Entry/Exit Timing

8.17 Power-Down Modes

8.17.1 Power-Down Entry and Exit

Power-down is synchronously entered when CKE is registered low (along with NOP or Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read / write operation are in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto-precharge and refresh are in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in Figure 59 through Figure 71 with details for entry and exit of Power-Down.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well as proper DLL operation with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

During Power-Down, if all banks are closed after any in-progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in-progress commands are completed, the device will be in active Power-Down mode.

Entering power-down deactivates the input and output buffers, excluding CK, CK#, ODT, CKE and RESET#. To protect DRAM internal delay on CKE line to block the input signals, multiple NOP or Deselect commands are needed during the CKE switch off and cycle(s) after, this timing period are defined as tCPDED. CKE_low will result in deactivation of command and address receivers after tCPDED has expired.

Table 8 – Power-Down Entry Definitions

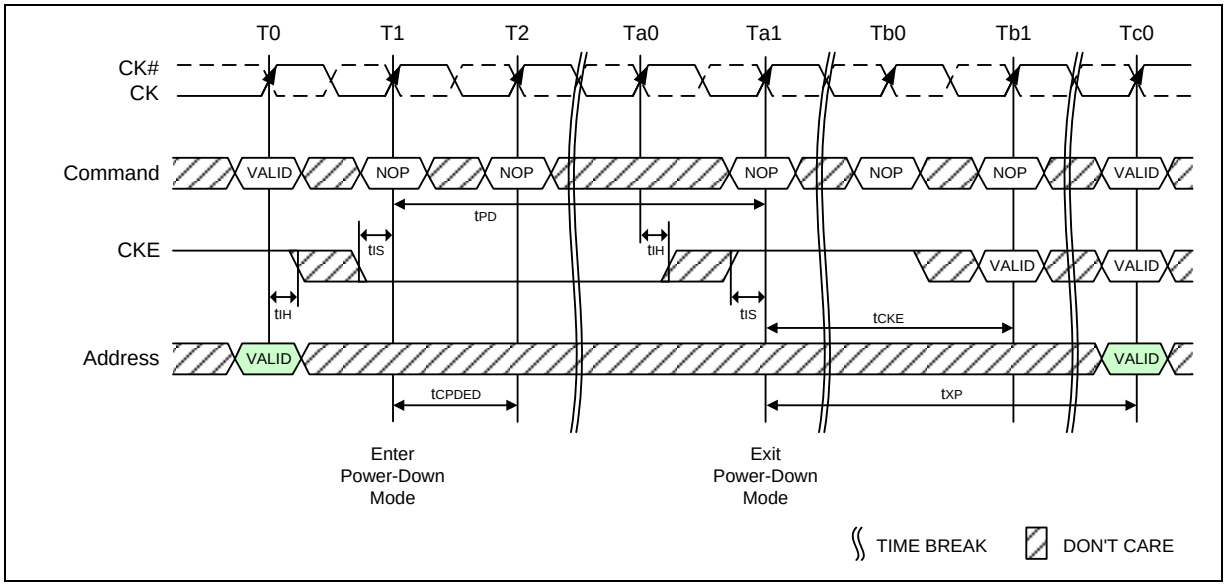
Status of DRAM	MRS bit A12	DLL	PD Exit	Relevant Parameters
Active (A bank or more Open)	Don't Care	On	Fast	**tXP** to any valid command
Precharged (All banks Precharged)	0	Off	Slow	**tXP** to any valid command. Since it is in precharge state, commands here will be ACT, REF, MRS, PRE or PREA. **tXPDLL** to commands that need the DLL to operate, such as RD, RDA or ODT control line.
Precharged (All banks Precharged)	1	On	Fast	**tXP** to any valid command

Also, the DLL is disabled upon entering precharge power-down (Slow Exit Mode), but the DLL is kept enabled during precharge power-down (Fast Exit Mode) or active power-down. In power-down mode, CKE low, RESET# high, and a stable clock signal must be maintained at the inputs of the DDR3 SDRAM, and ODT should be in a valid state, but all other input signals are “Don't Care.” (If RESET# goes low during Power-Down, the DRAM will be out of PD mode and into reset state.) CKE low must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or Deselect command). CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP and/or tXPDLL after CKE goes high. Power-down exit latency is defined in section 10.16 **“AC Characteristics”** on page 139.

Active Power Down Entry and Exit timing diagram example is shown in Figure 59. Timing Diagrams for CKE with PD Entry, PD Exit with Read and Read with Auto Precharge, Write, Write with Auto Precharge, Activate, Precharge, Refresh, and MRS are shown in Figure 60 through Figure 68. Additional clarifications are shown in Figure 69 through Figure 71.

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Note:

1. VALID command at T0 is ACT, NOP, DES or PRE with still one bank remaining open after completion of the precharge command.

Figure 59 – Active Power-Down Entry and Exit Timing Diagram

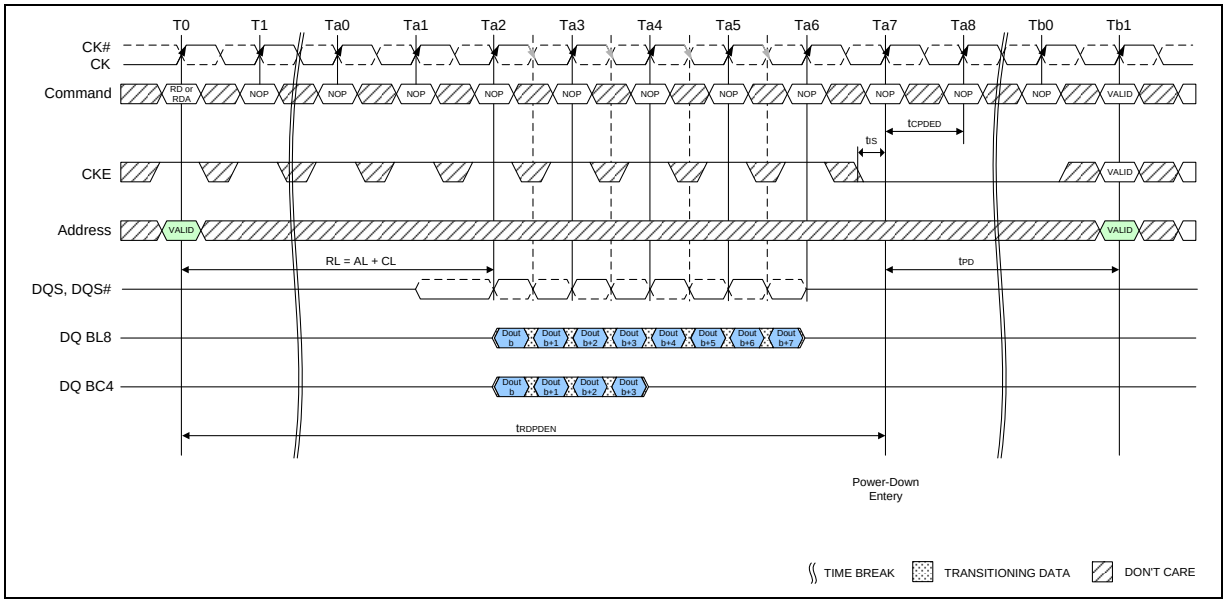
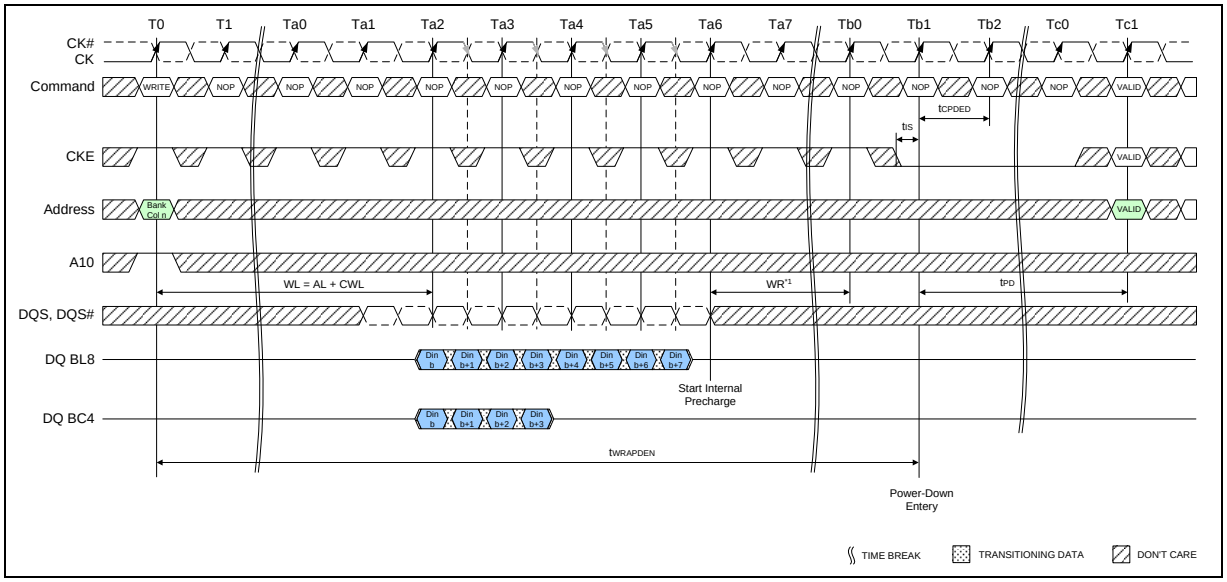


Figure 60 – Power-Down Entry after Read and Read with Auto Precharge

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Note:

1. tWR is programmed through MR0.

Figure 61 – Power-Down Entry after Write with Auto Precharge

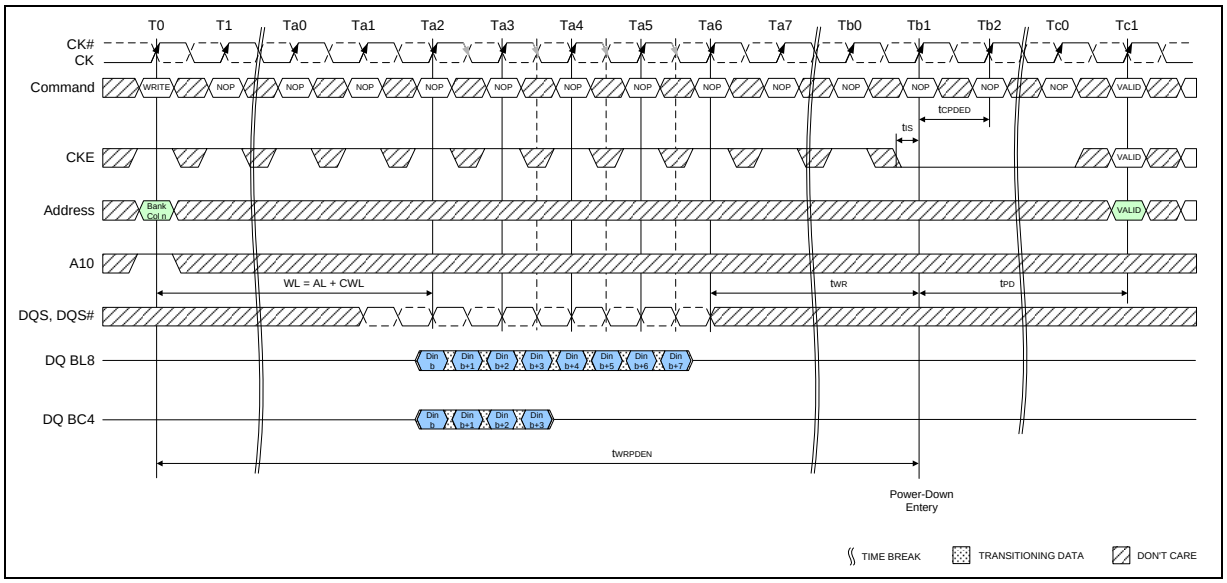


Figure 62 – Power-Down Entry after Write

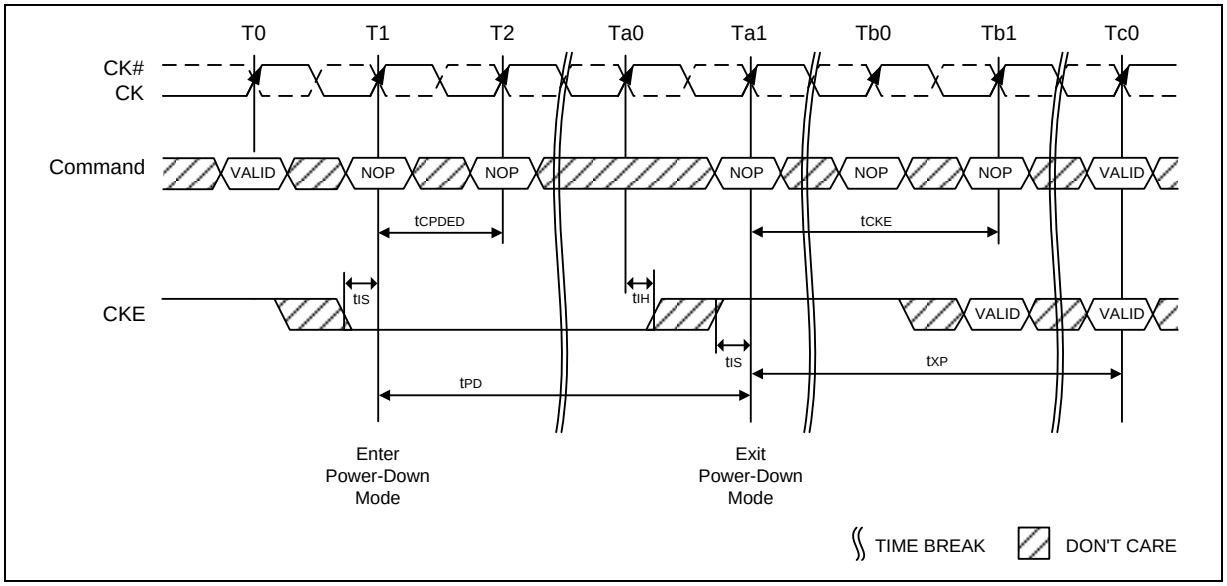


Figure 63 – Precharge Power-Down (Fast Exit Mode) Entry and Exit

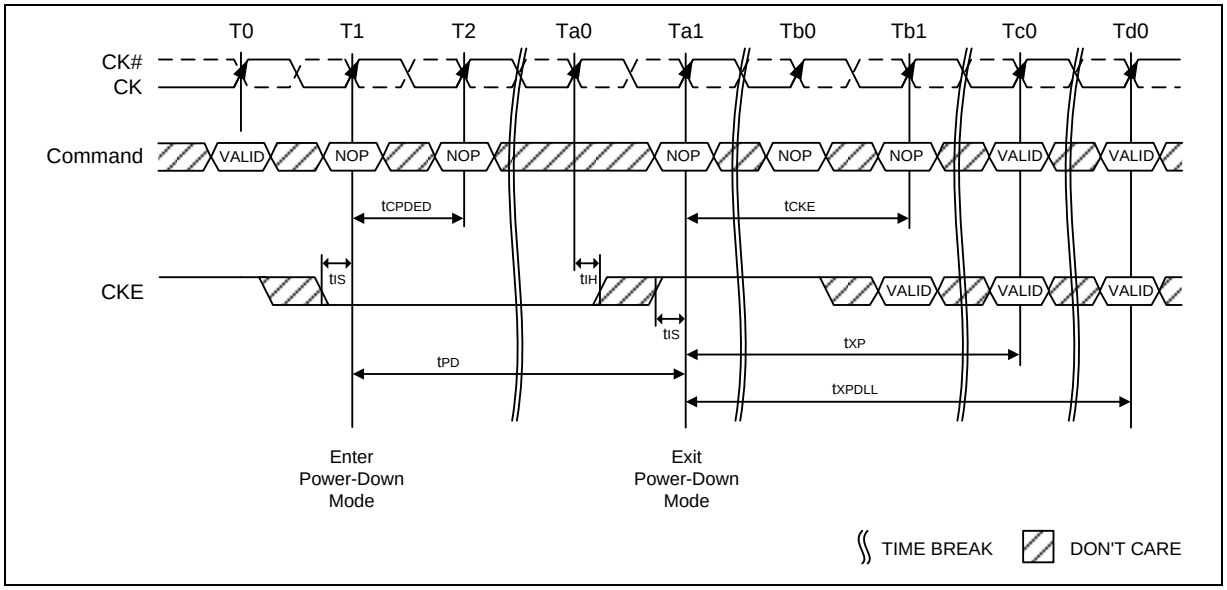


Figure 64 – Precharge Power-Down (Slow Exit Mode) Entry and Exit

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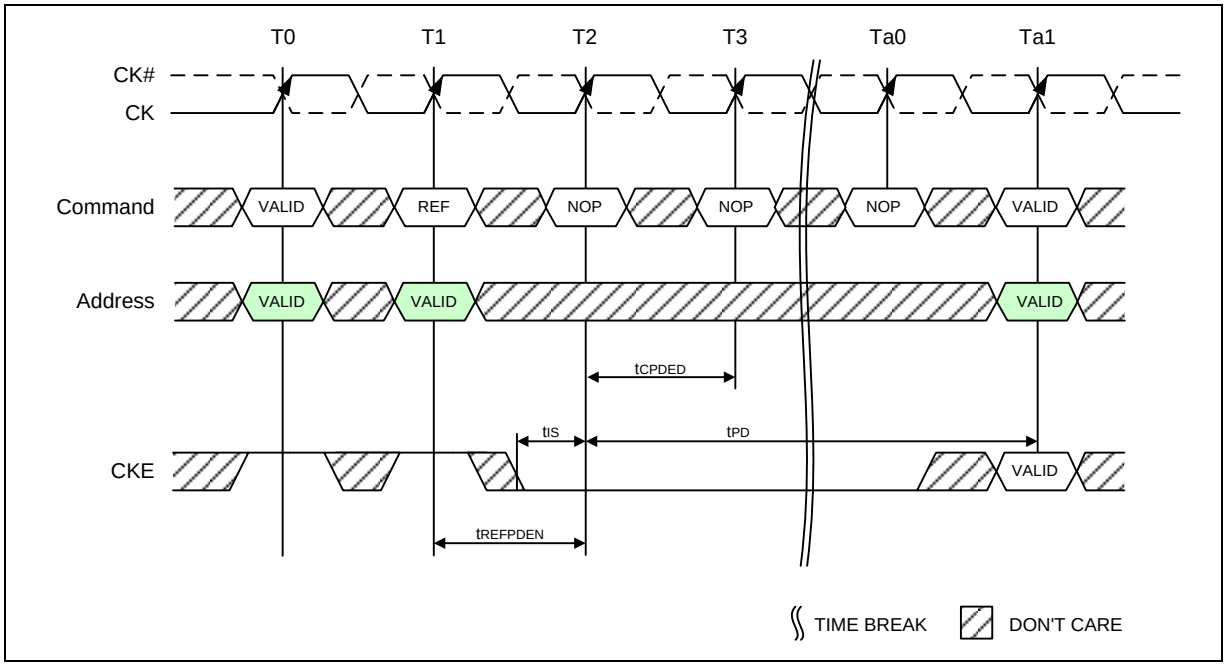


Figure 65 – Refresh Command to Power-Down Entry

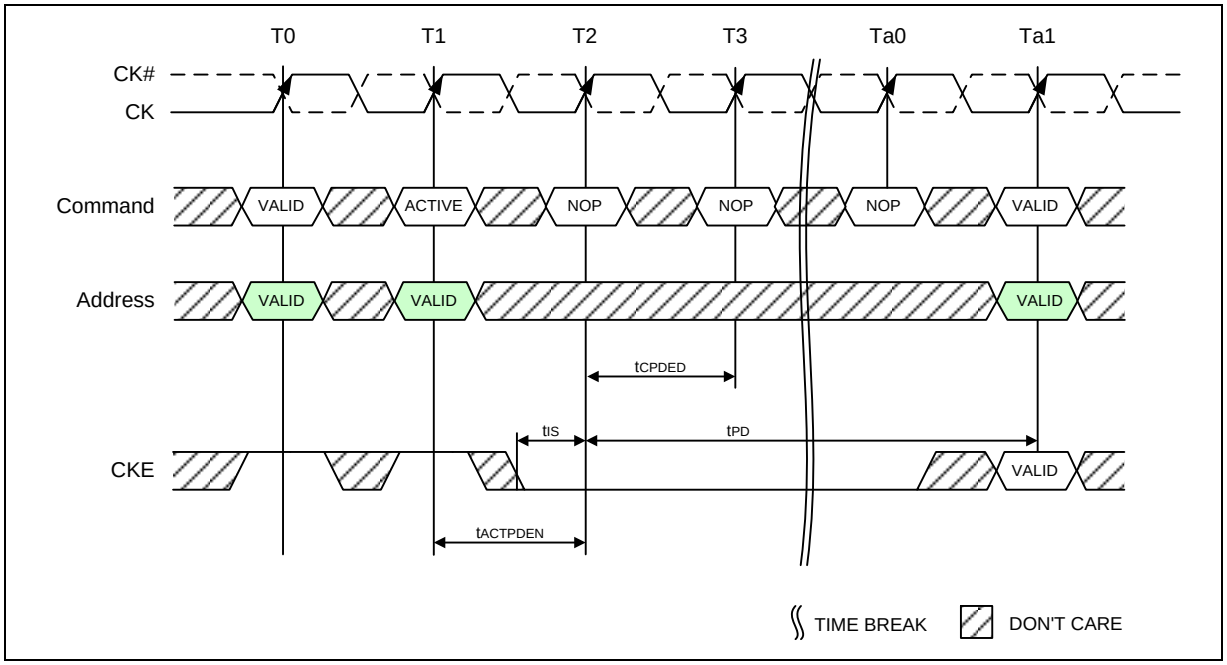


Figure 66 – Active Command to Power-Down Entry

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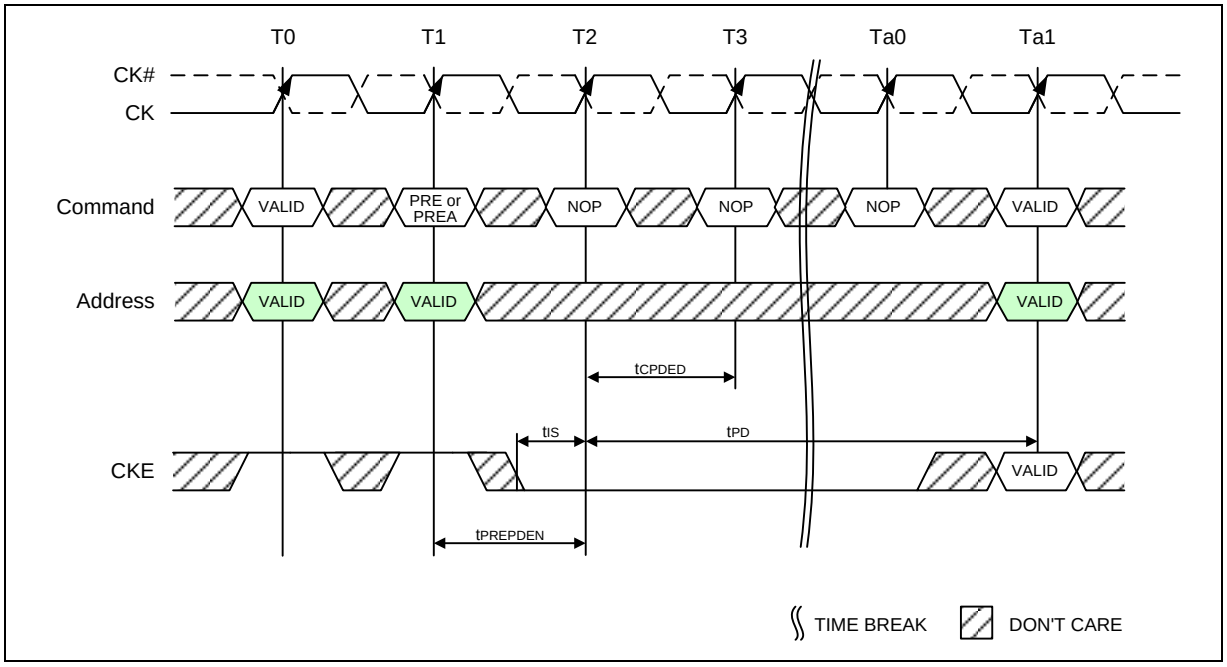


Figure 67 – Precharge / Precharge all Command to Power-Down Entry

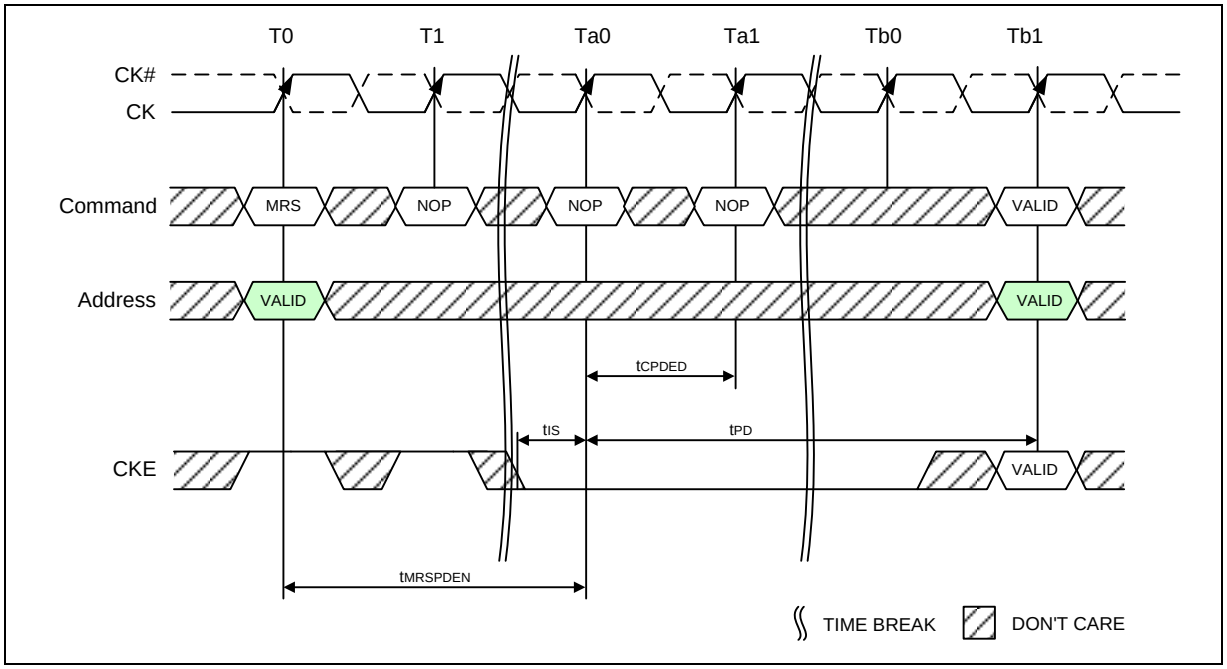


Figure 68 – MRS Command to Power-Down Entry

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8.17.2 Power-Down clarifications - Case 1

When CKE is registered low for power-down entry, tPD(min) must be satisfied before CKE can be registered high for power-down exit. The minimum value of parameter tPD(min) is equal to the minimum value of parameter tCKE(min) as shown in section 10.16 **"AC Characteristics"** on page 139. A detailed example of Case 1 is shown in Figure 69.

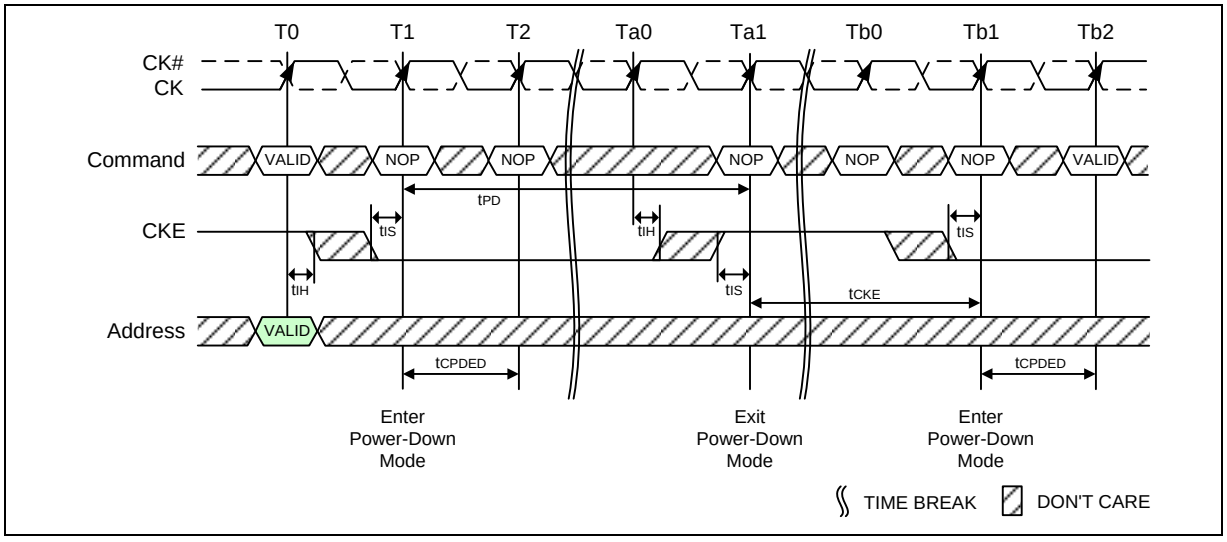


Figure 69 – Power-Down Entry/Exit Clarifications - Case 1

8.17.3 Power-Down clarifications - Case 2

For certain CKE intensive operations, for example, repeated 'PD Exit - Refresh - PD Entry' sequences, the number of clock cycles between PD Exit and PD Entry may be insufficient to keep the DLL updated. Therefore, the following conditions must be met in addition to tCKE in order to maintain proper DRAM operation when the Refresh command is issued between PD Exit and PD Entry. Power-down mode can be used in conjunction with the Refresh command if the following conditions are met:

1) tXP must be satisfied before issuing the command.

2) tXPDLL must be satisfied (referenced to the registration of PD Exit) before the next power-down can be entered. A detailed example of Case 2 is shown in Figure 70.

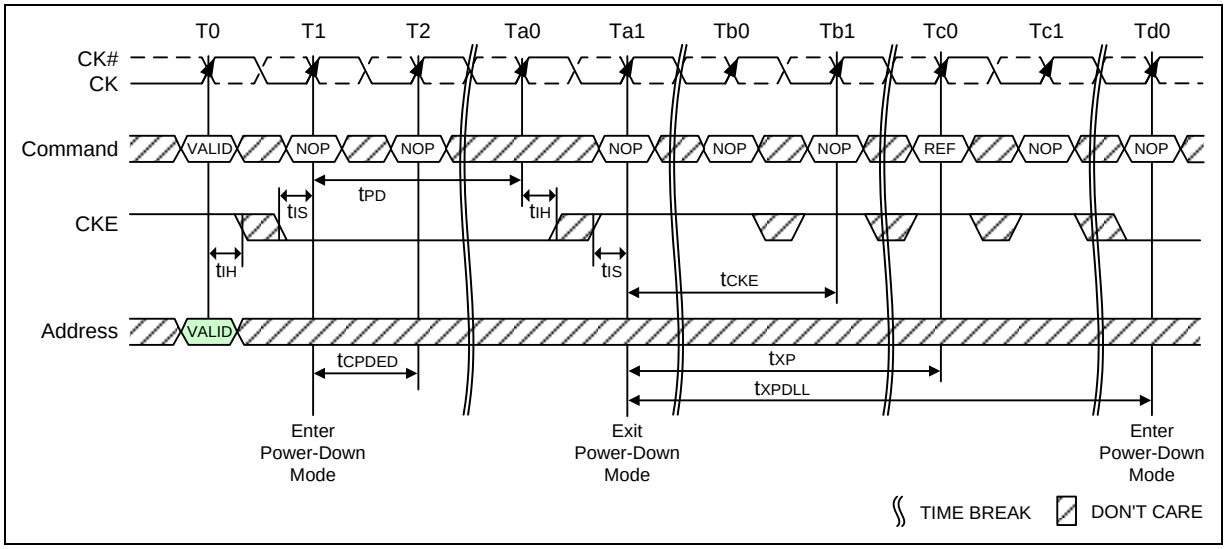


Figure 70 – Power-Down Entry/Exit Clarifications - Case 2

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8.17.4 Power-Down clarifications - Case 3

If an early PD Entry is issued after a Refresh command, once PD Exit is issued, NOP or DES with CKE High must be issued until tRFC(min) from the Refresh command is satisfied. This means CKE can not be registered low twice within a tRFC(min) window. A detailed example of Case 3 is shown in Figure 71.

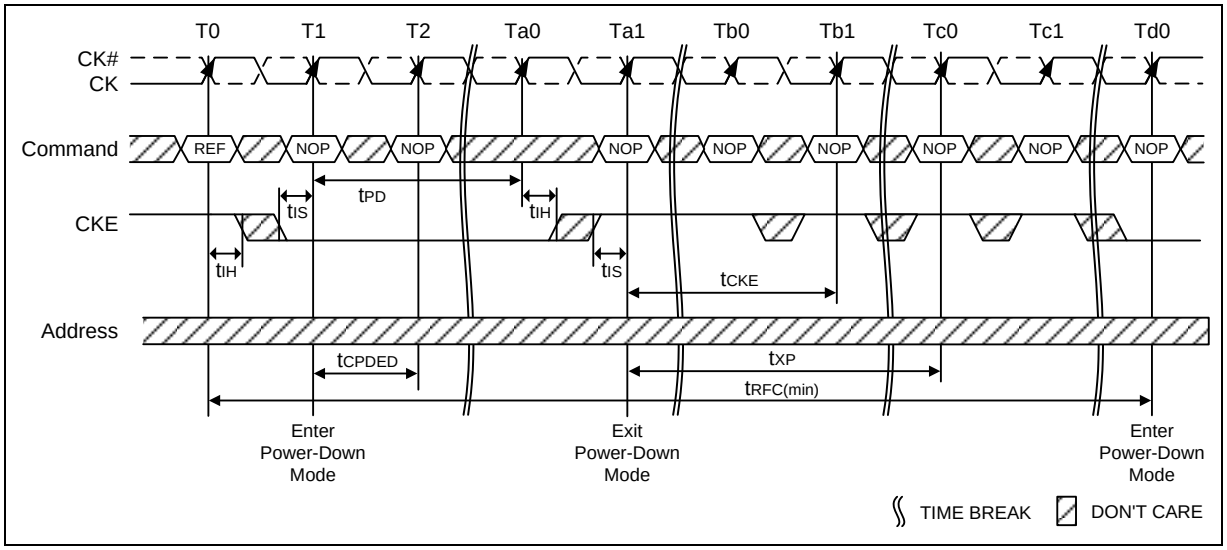


Figure 71 – Power-Down Entry/Exit Clarifications - Case 3

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8.18 ZQ Calibration Commands

8.18.1 ZQ Calibration Description

ZQ Calibration command is used to calibrate DRAM RON & ODT values over PVT (process, voltage and temperature). An external resistor (RZQ) between the DRAM ZQ pin and ground is used as a calibration reference. DDR3 SDRAM needs longer time to calibrate output driver and on-die termination circuits after power-up and/or any reset, medium time for a full calibration during normal operation (e.g. after self-refresh exit) and relatively smaller time to perform periodic update calibrations.

ZQCL (ZQ Calibration Long) command is used to perform the initial calibration during power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. ZQCL command triggers the calibration engine inside the DRAM and, once calibration is achieved, the calibrated values are transferred from the calibration engine to DRAM IO, which gets reflected as updated output driver and on-die termination values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET are allowed a timing period of tZQoper.

ZQCS (ZQ Calibration Short) command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS. One ZQCS command can effectively correct a minimum of 0.5 % (ZQ Correction) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the **'Output Driver Voltage and Temperature Sensitivity'** and **'ODT Voltage and Temperature Sensitivity'** tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{Vdriftrate})}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5 %/°C, VSens = 0.15%/mV, Tdriftrate = 1 °C/sec and Vdriftrate = 15 mV/sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{mS}$$

No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper, or tZQCS. The quiet time on the DRAM channel allows accurate calibration of output driver and on-die termination values. Once DRAM calibration is achieved, the DRAM should disable ZQ current consumption path to reduce power.

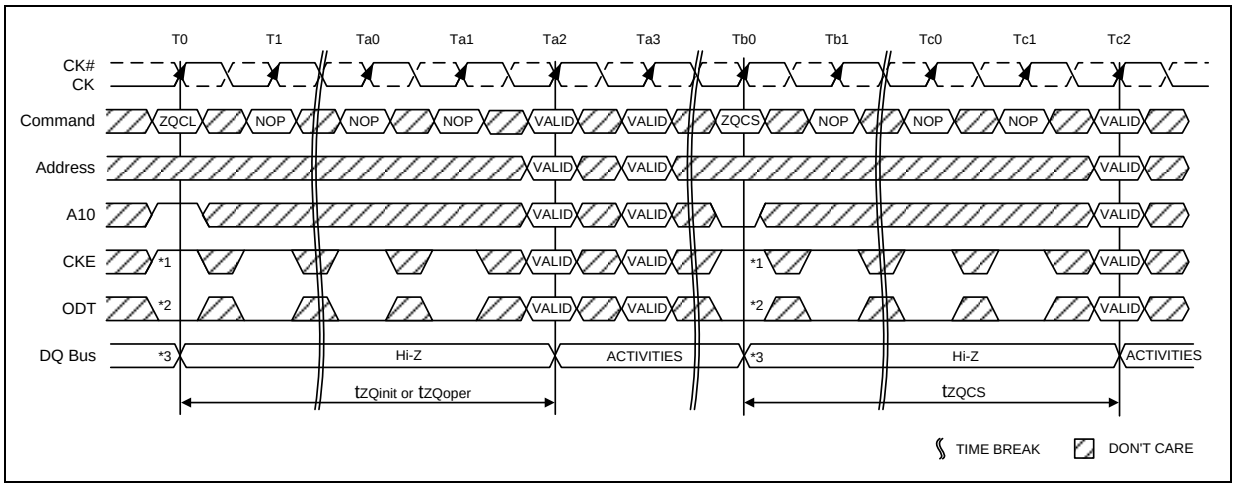
All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller. See section 9.1 **"Command Truth Table"** on page 94 for a description of the ZQCL and ZQCS commands.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon Self-Refresh exit, DDR3 SDRAM will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for ZQ Calibration command (ZQCS or ZQCL) after self refresh exit is tXS.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper, tZQinit, or tZQCS between the devices.

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8.18.2 ZQ Calibration Timing



Notes:

1. CKE must be continuously registered high during the calibration procedure.
2. On-die termination must be disabled via the ODT signal or MRS during the calibration procedure.
3. All devices connected to the DQ bus should be high impedance during the calibration procedure.

Figure 72 – ZQ Calibration Timing

8.18.3 ZQ External Resistor Value, Tolerance, and Capacitive loading

In order to use the ZQ Calibration function, a 240 ohm ± 1% tolerance external resistor must be connected between the ZQ pin and ground. The single resistor can be used for each SDRAM or one resistor can be shared between two SDRAMs if the ZQ calibration timings for each SDRAM do not overlap. The total capacitive loading on the ZQ pin must be limited (See section 10.11 **"Input/Output Capacitance"** on page 120).

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8.19 On-Die Termination (ODT)

ODT (On-Die Termination) is a feature of the DDR3 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, DQS# and DM (and TDQS, TDQS#, when enabled via A11=1 in MR1) signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices. More details about ODT control modes and ODT timing modes can be found further down in this document:

- The ODT control modes are described in section 8.19.1
- The ODT synchronous mode is described in section 8.19.2
- The dynamic ODT feature is described in section 8.19.3
- The ODT asynchronous mode is described in section 8.19.4
- The transitions between ODT synchronous and asynchronous are described in section 8.19.4.1 through section 8.19.4.4

The ODT feature is turned off and not supported in Self-Refresh mode.

A simple functional representation of the DRAM ODT feature is shown in Figure 73.

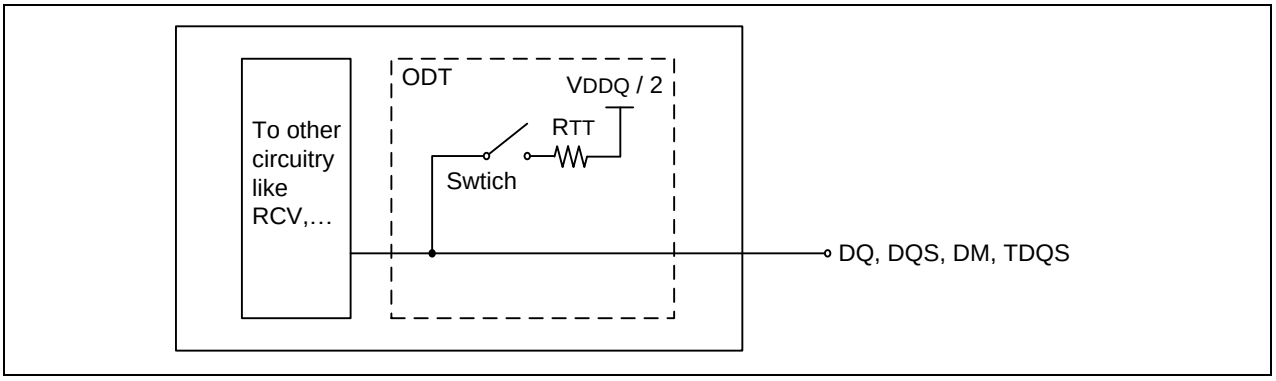


Figure 73 – Functional Representation of ODT

The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information, see below. The value of RTT is determined by the settings of Mode Register bits (see Figure 6 - MR1 Definition on page 19 and Figure 7 - MR2 Definition on page 22). The ODT pin will be ignored if the Mode Registers MR1 and MR2 are programmed to disable ODT, and in self-refresh mode.

8.19.1 ODT Mode Register and ODT Truth Table

The ODT Mode is enabled if any of MR1 {A9, A6, A2} or MR2 {A10, A9} are non zero. In this case, the value of RTT is determined by the settings of those bits (see Figure 6 - MR1 Definition on page 19).

Application: Controller sends WR command together with ODT asserted.

- One possible application: The rank that is being written to provides termination.
- DRAM turns ON termination if it sees ODT asserted (unless ODT is disabled by MR).
- DRAM does not use any write or read command decode information.
- The Termination Truth Table is shown in Table 9.

Table 9 – Termination Truth Table

ODT pin	DRAM Termination State
0	OFF
1	ON, (OFF, if disabled by MR1 {A9, A6, A2} and MR2 {A10, A9} in general)

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8.19.2 Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:

- Any bank active with CKE high
- Refresh with CKE high
- Idle mode with CKE high
- Active power down mode (regardless of MR0 bit A12)
- Precharge power down mode if DLL is enabled during precharge power down by MR0 bit A12.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the Rtt_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

In synchronous ODT mode, RTT will be turned on ODTLon clock cycles after ODT is sampled high by a rising clock edge and turned off ODTLoff clock cycles after ODT is registered low by a rising clock edge. The ODT latency is tied to the write latency (WL) by: ODTLon = WL - 2; ODTLoff = WL - 2.

8.19.2.1 ODT Latency and Posted ODT

In Synchronous ODT Mode, the Additive Latency (AL) programmed into the Mode Register (MR1) also applies to the ODT signal. The DRAM internal ODT signal is delayed for a number of clock cycles defined by the Additive Latency (AL) relative to the external ODT signal. ODTLon = CWL + AL - 2; ODTLoff = CWL + AL - 2. For more details refer to the ODT timing parameters in section 10.16 **"AC Characteristics"** on page 139.

Table 10 – ODT Latency

Symbol	Parameter	DDR3-1333/1600/1866/2133	Unit
ODTLon	ODT turn on Latency	WL - 2 = CWL + AL - 2	nCK
ODTLoff	ODT turn off Latency	WL - 2 = CWL + AL - 2	

8.19.2.2 Timing Parameters

In synchronous ODT mode, the following timing parameters apply (see also Figures 74):

ODTLon, ODTLoff, t_{AON},min,max, t_{AOF},min,max.

Minimum RTT turn-on time (t_{AON}min) is the point in time when the device leaves high impedance and ODT resistance begins to turn on. Maximum RTT turn on time (t_{AON}max) is the point in time when the ODT resistance is fully on. Both are measured from ODTLon.

Minimum RTT turn-off time (t_{AOF}min) is the point in time when the device starts to turn off the ODT resistance. Maximum RTT turn off time (t_{AOF}max) is the point in time when the on-die termination has reached high impedance. Both are measured from ODTLoff.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL = 4) or ODTH8 (BL = 8) after the Write command (see Figure 75). ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of a Write command until ODT is registered low.

ODT must be held high for at least ODTH4 after assertion (T1); ODT must be kept high ODTH4 (BL = 4) or ODTH8 (BL = 8) after Write command (T7). ODTH is measured from ODT first registered high to ODT first registered low, or from registration of Write command with ODT high to ODT registered low. Note that although ODTH4 is satisfied from ODT registered high at T6, ODT must not go low before T11 as ODTH4 must also be satisfied from the registration of the Write command at T7.

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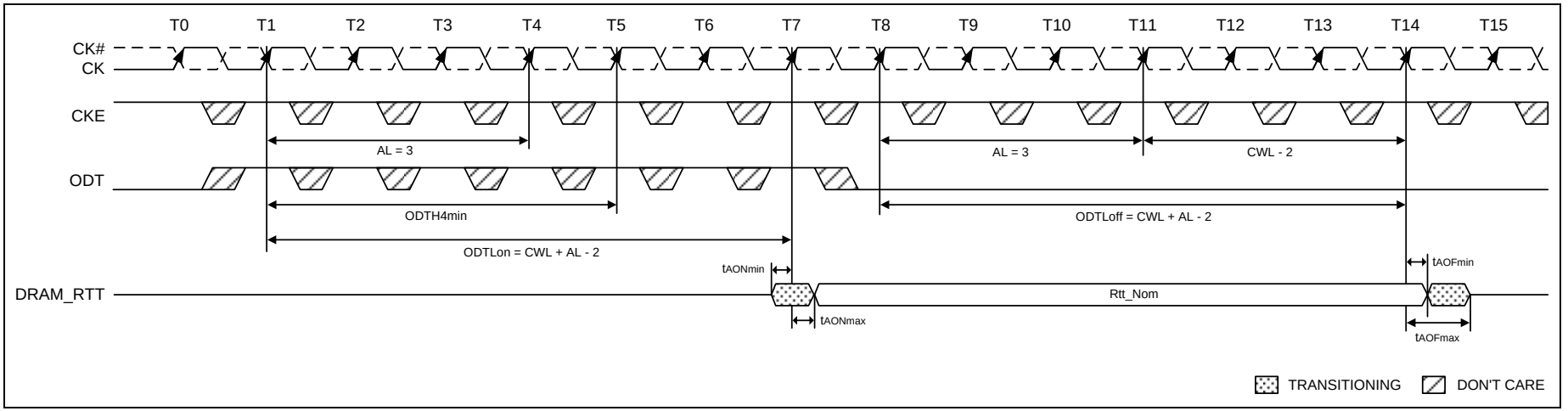


Figure 74 – Synchronous ODT Timing (AL = 3; CWL = 5; ODTLon = AL + CWL - 2 = 6; ODTLoff = AL + CWL - 2 = 6)

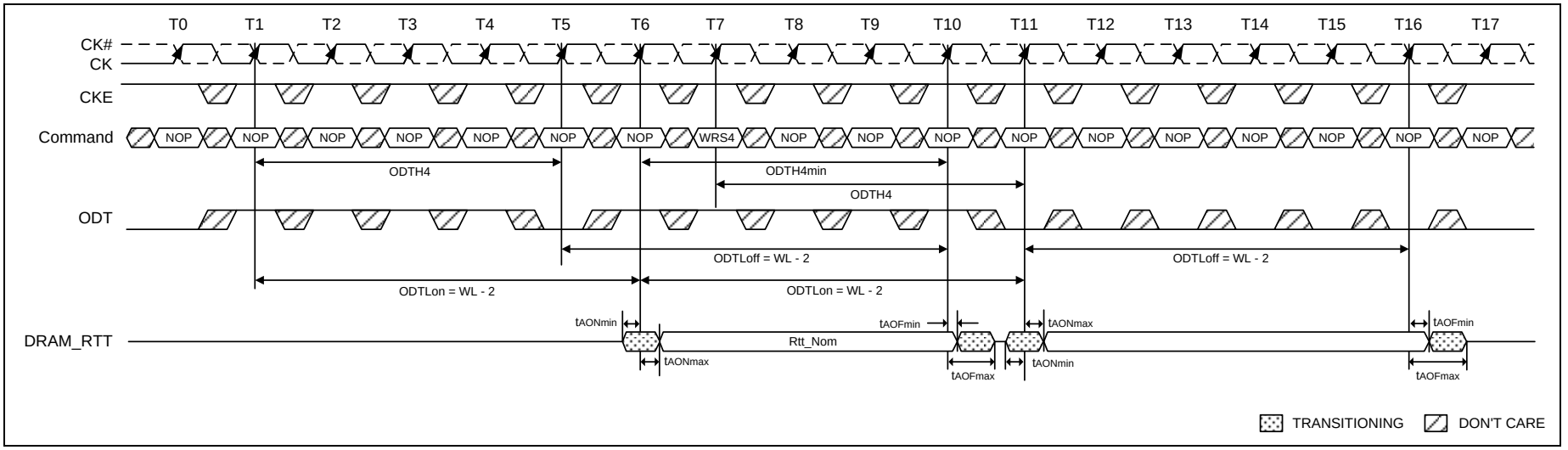


Figure 75 – Synchronous ODT (BL = 4, WL = 7)

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8.19.2.3 ODT during Reads

As the DDR3 SDRAM can not terminate and drive at the same time, RTT must be disabled at least half a clock cycle before the read preamble by driving the ODT pin low appropriately. RTT may not be enabled until the end of the post-amble as shown in the example below. As shown in Figure 76 below, at cycle T15, DRAM turns on the termination when it stops driving, which is determined by tHZ. If DRAM stops driving early (i.e., tHZ is early), then tAONmin timing may apply. If DRAM stops driving late (i.e., tHZ is late), then DRAM complies with tAONmax timing. Note that ODT may be disabled earlier before the Read and enabled later after the Read than shown in this example in Figure 76.

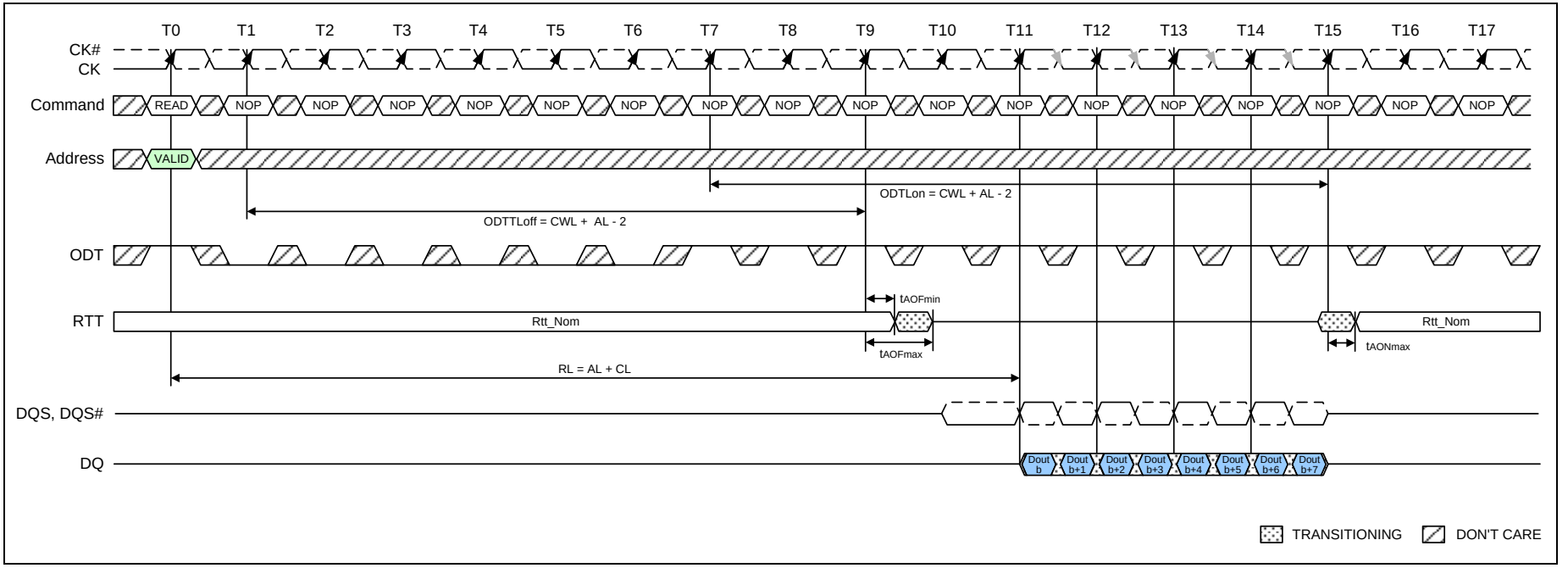


Figure 76 – ODT must be disabled externally during Reads by driving ODT low.
(CL = 6; AL = CL - 1 = 5; RL = AL + CL = 11; CWL = 5; ODTLon = CWL + AL - 2 = 8; ODTLoff = CWL + AL - 2 = 8)

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8.19.3 Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. This requirement is supported by the “Dynamic ODT” feature as described as follows:

8.19.3.1 Functional Description:

The Dynamic ODT Mode is enabled if bit (A9) or (A10) of MR2 is set to ‘1’. The function is described as follows:

- Two RTT values are available: Rtt_Nom and Rtt_WR.
  - The value for Rtt_Nom is preselected via bits A[9,6,2] in MR1.
  - The value for Rtt_WR is preselected via bits A[10,9] in MR2.
- During operation without write commands, the termination is controlled as follows:
  - Nominal termination strength Rtt_Nom is selected.
  - Termination on/off timing is controlled via ODT pin and latencies ODTLon and ODTLoff.
- When a write command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:
  - A latency ODTLcnw after the write command, termination strength Rtt_WR is selected.
  - A latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the write command, termination strength Rtt_Nom is selected.
  - Termination on/off timing is controlled via ODT pin and ODTLon, ODTLoff.

Table 11 shows latencies and timing parameters which are relevant for the on-die termination control in Dynamic ODT mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set

Rtt_WR, MR2{A10, A9}={0,0}, to disable Dynamic ODT externally.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL = 4) or ODTH8 (BL = 8) after the Write command (see Figure 77). ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of a Write command until ODT is registered low.

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Table 11 – Latencies and timing parameters relevant for Dynamic ODT

Name and Description	Abbr.	Defined from	Defined to	Definition for all DDR3 speed bins	Unit
ODT turn-on Latency	ODTLon	Registering external ODT signal high	Turning termination on	ODTLon = WL - 2	tCK
ODT turn-off Latency	ODTLoff	Registering external ODT signal low	Turning termination off	ODTLoff = WL - 2	tCK
ODT Latency for changing from Rtt_Nom to Rtt_WR	ODTLcnw	Registering external write command	Change RTT strength from Rtt_Nom to Rtt_WR	ODTLcnw = WL - 2	tCK
ODT Latency for change from Rtt_WR to Rtt_Nom (BL = 4)	ODTLcwn4	Registering external write command	Change RTT strength from Rtt_WR to Rtt_Nom	ODTLcwn4 = 4 + ODTLoff	tCK
ODT Latency for change from Rtt_WR to Rtt_Nom (BL = 8)	ODTLcwn8	Registering external write command	Change RTT strength from Rtt_WR to Rtt_Nom	ODTLcwn8 = 6 + ODTLoff	tCK(avg)
Minimum ODT high time after ODT assertion	ODTH4	Registering ODT high	ODT registered low	ODTH4 = 4	tCK(avg)
Minimum ODT high time after Write (BL = 4)	ODTH4	Registering Write with ODT high	ODT registered low	ODTH4 = 4	tCK(avg)
Minimum ODT high time after Write (BL =8)	ODTH8	Registering Write with ODT high	ODT registered low	ODTH4 = 6	tCK(avg)
RTT change skew	tADC	ODTLcnw ODTLcwn	RTT valid	tADC(min) = 0.3 * tCK(avg) tADC(max) = 0.7 * tCK(avg)	tCK(avg)

Note: tAOFnom and tADCnom are 0.5 tCK (effectively adding half a clock cycle to ODTLoff, ODTcnw and ODTLcwn)

8.19.3.2 ODT Timing Diagrams

The following pages provide exemplary timing diagrams as described in Table 12:

Table 12 – Timing Diagrams for "Dynamic ODT"

Figure and Page	Description
Figure 77 on page 85	Figure 77, Dynamic ODT: Behavior with ODT being asserted before and after the write
Figure 78 on page 86	Figure 78, Dynamic ODT: Behavior without write command, AL = 0, CWL = 5
Figure 79 on page 86	Figure 79, Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles
Figure 80 on page 87	Figure 80, Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles, example for BC4 (via MRS or OTF), AL = 0, CWL = 5
Figure 81 on page 87	Figure 81, Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 4 clock cycles

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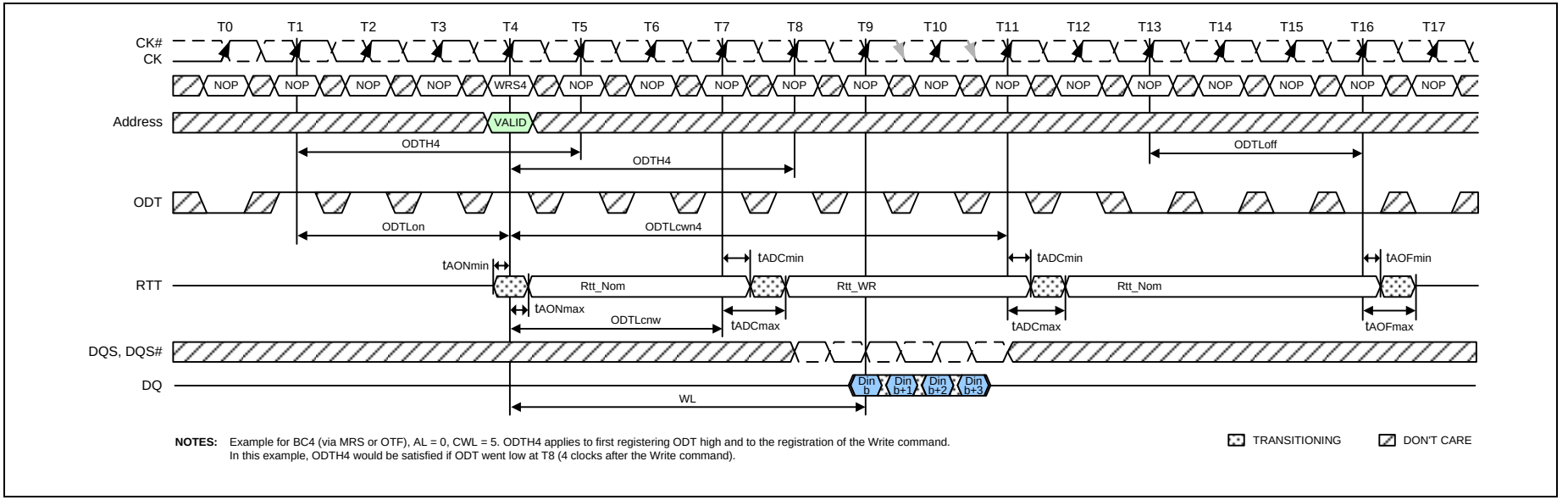
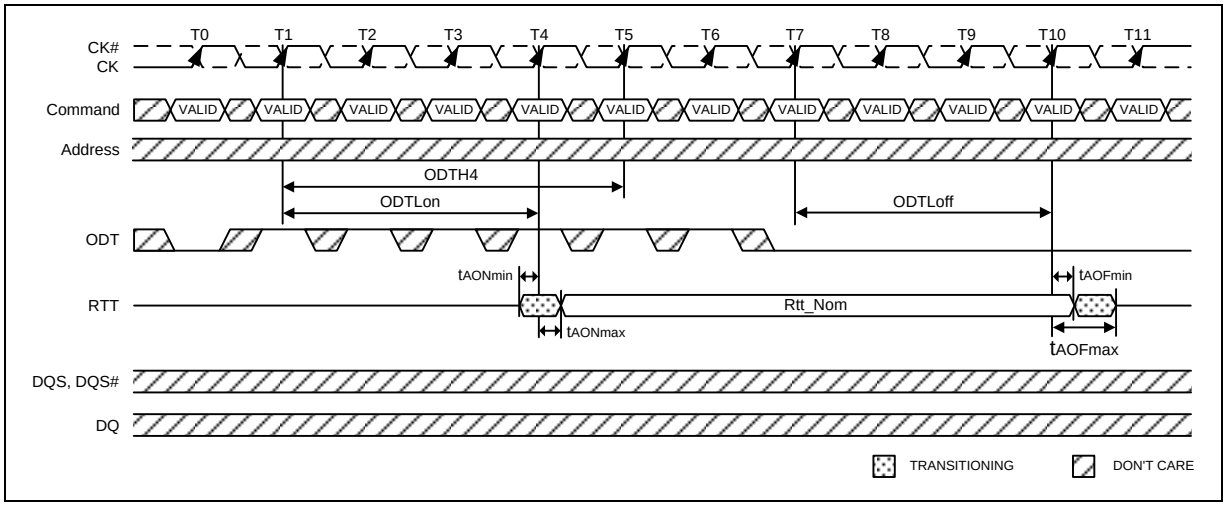


Figure 77 – Dynamic ODT: Behavior with ODT being asserted before and after the write

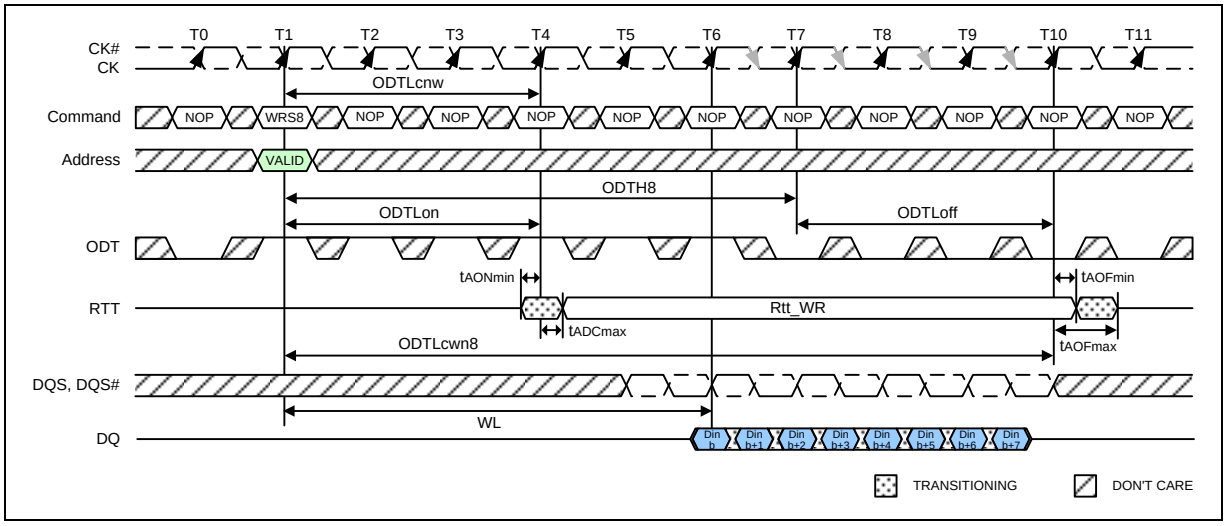
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Notes:

1. ODTH4 is defined from ODT registered high to ODT registered low, so in this example, ODTH4 is satisfied.
2. ODT registered low at T5 would also be legal.

Figure 78 – Dynamic ODT: Behavior without write command, AL = 0, CWL = 5

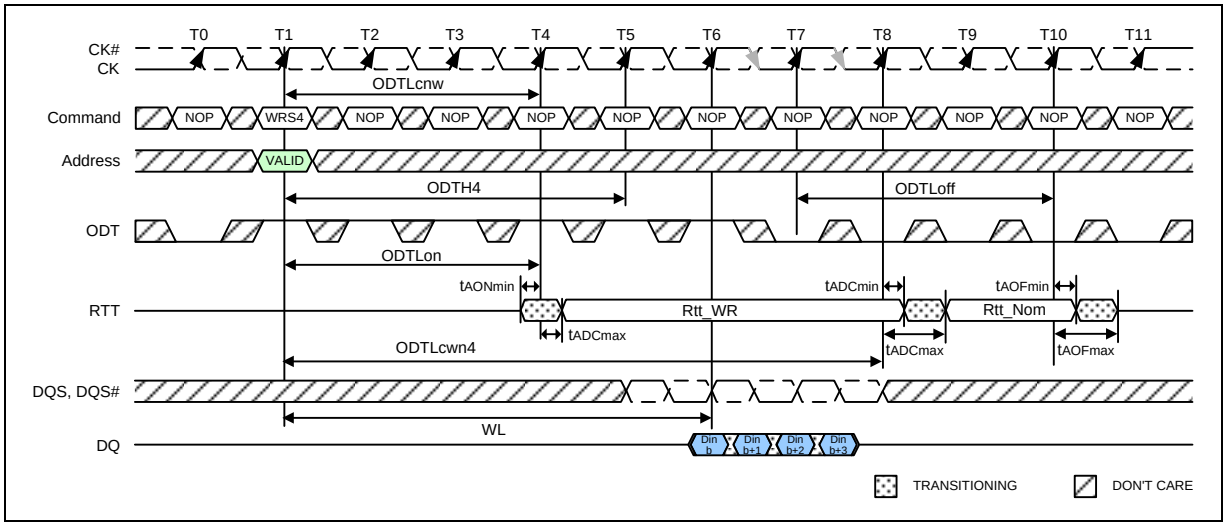


Note:

1. Example for BL8 (via MRS or OTF), AL = 0, CWL = 5. In this example, ODTH8 = 6 is exactly satisfied.

Figure 79 – Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles

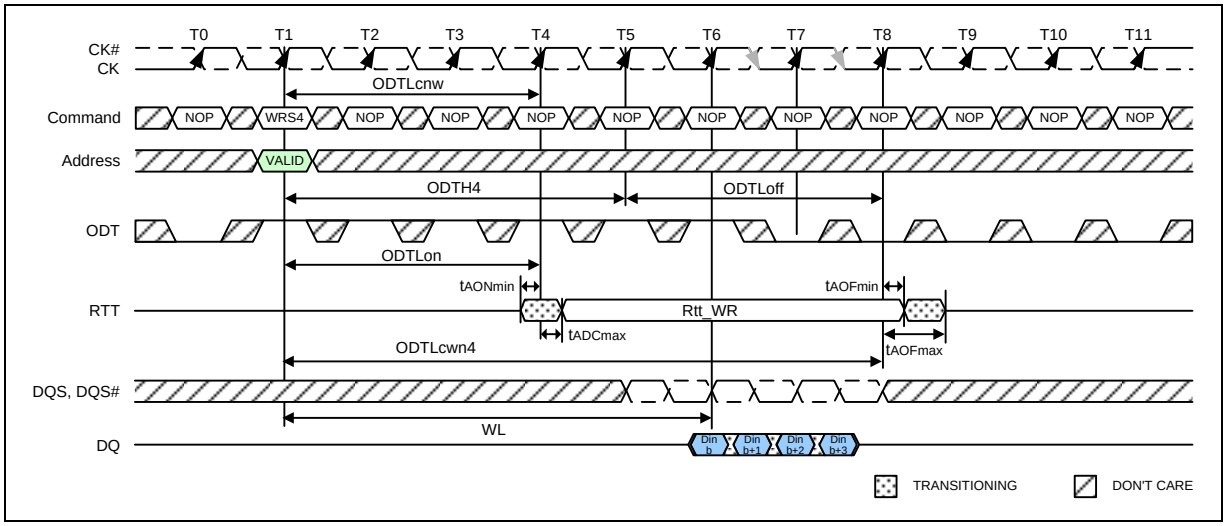
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Notes:

1. ODTH4 is defined from ODT registered high to ODT registered low, so in this example, ODTH4 is satisfied.
2. ODT registered low at T5 would also be legal.

Figure 80 – Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles, example for BC4 (via MRS or OTF), AL = 0, CWL = 5



Note:

1. Example for BC4 (via MRS or OTF), AL = 0, CWL = 5. In this example, ODTH4 = 4 is exactly satisfied.

Figure 81 – Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 4 clock cycles

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8.19.4 Asynchronous ODT Mode

Asynchronous ODT mode is selected when DRAM runs in DLLon mode, but DLL is temporarily disabled (i.e. frozen) in precharge power-down (by MR0 bit A12). Based on the power down mode definitions, this is currently Precharge power down mode if DLL is disabled during precharge power down by MR0 bit A12.

In asynchronous ODT timing mode, internal ODT command is NOT delayed by Additive Latency (AL) relative to the external ODT command.

In asynchronous ODT mode, the following timing parameters apply (see Figure 82): tAONPD,min,max, tAOFPD,min,max.

Minimum RTT turn-on time (tAONPDmin) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on. Maximum RTT turn on time (tAONPDmax) is the point in time when the ODT resistance is fully on.

tAONPDmin and tAONPDmax are measured from ODT being sampled high.

Minimum RTT turn-off time (tAOFPDmin) is the point in time when the devices termination circuit starts to turn off the ODT resistance. Maximum ODT turn off time (tAOFPDmax) is the point in time when the on-die termination has reached high impedance. tAOFPDmin and tAOFPDmax are measured from ODT being sampled low.

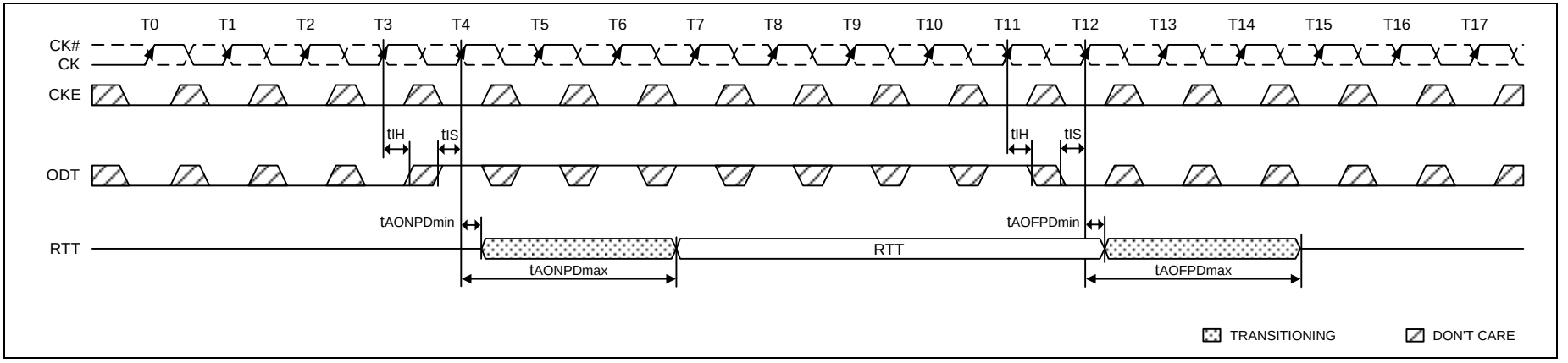


Figure 82 – Asynchronous ODT Timings on DDR3 SDRAM with fast ODT transition: AL is ignored

In Precharge Power Down, ODT receiver remains active, however no Read or Write command can be issued, as the respective ADD/CMD receivers may be disabled.

Table 13 – Asynchronous ODT Timing Parameters for all Speed Bins

Symbol	Description	Min.	Max.	Unit
tAONPD	Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	2	8.5	nS
tAOFPD	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	2	8.5	nS

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8.19.4.1 Synchronous to Asynchronous ODT Mode Transitions

Table 14 – ODT timing parameters for Power Down (with DLL frozen) entry and exit transition period

Description	Min.	Max.
ODT to RTT turn-on delay	min{ ODTLon * tCK(avg) + tAONmin; tAONPDmin }	max{ ODTLon * tCK(avg) + tAONmax; tAONPDmax }
	min{ (WL - 2) * tCK(avg) + tAONmin; tAONPDmin }	max{ (WL - 2) * tCK(avg) + tAONmax; tAONPDmax }
ODT to RTT turn-off delay	min{ ODTLoff * tCK(avg) +tAOFmin; tAOFPDmin }	max{ ODTLoff * tCK(avg) + tAOFmax; tAOFPDmax }
	min{ (WL - 2) * tCK(avg) +tAOFmin; tAOFPDmin }	max{ (WL - 2) * tCK(avg) + tAOFmax; tAOFPDmax }
tANPD	WL -1	

8.19.4.2 Synchronous to Asynchronous ODT Mode Transition during Power-Down Entry

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to “0”, there is a transition period around power down entry, where the DDR3 SDRAM may show either synchronous or asynchronous ODT behavior.

The transition period is defined by the parameters tANPD and tCPDED(min). tANPD is equal to (WL -1) and is counted backwards in time from the clock cycle where CKE is first registered low. tCPDED(min) starts with the clock cycle where CKE is first registered low. The transition period begins with the starting point of tANPD and terminates at the end point of tCPDED(min), as shown in Figure 83. If there is a Refresh command in progress while CKE goes low, then the transition period ends at the later one of tRFC(min) after the Refresh command and the end point of tCPDED(min), as shown in Figure 84. Please note that the actual starting point at tANPD is excluded from the transition period, and the actual end points at tCPDED(min) and tRFC(min), respectively, are included in the transition period.

ODT assertion during the transition period may result in an RTT change as early as the smaller of tAONPDmin and (ODTLon*tCK(avg) + tAONmin) and as late as the larger of tAONPDmax and (ODTLon* tCK(avg) + tAONmax). ODT de-assertion during the transition period may result in an RTT change as early as the smaller of tAOFPDmin and (ODTLoff* tCK(avg) + tAOFmin) and as late as the larger of tAOFPDmax and (ODTLoff* tCK(avg) + tAOFmax). See Table 14.

Note that, if AL has a large value, the range where RTT is uncertain becomes quite large. Figure 83 shows the three different cases: ODT_A, synchronous behavior before tANPD; ODT_B has a state change during the transition period; ODT_C shows a state change after the transition period.

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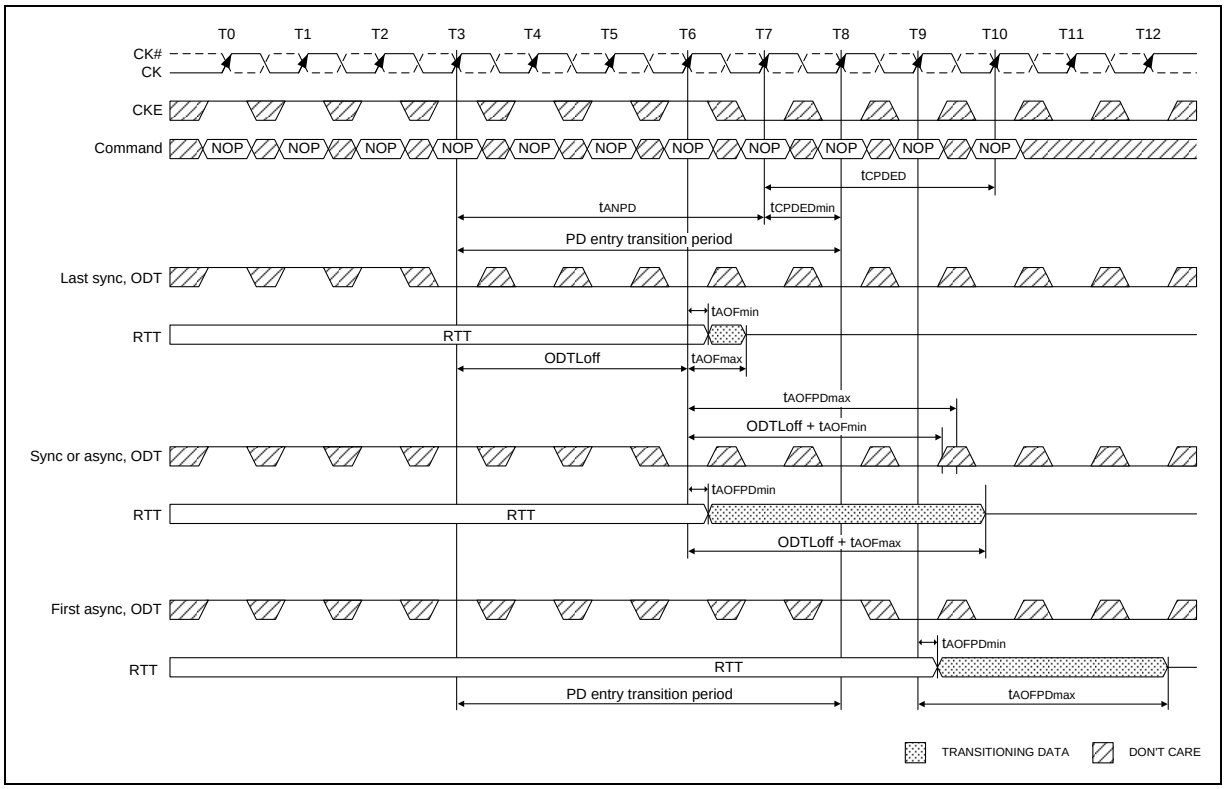


Figure 83 – Synchronous to asynchronous transition during Precharge Power Down (with DLL frozen) entry (AL = 0; CWL = 5; t_{ANPD} = WL - 1 = 4)

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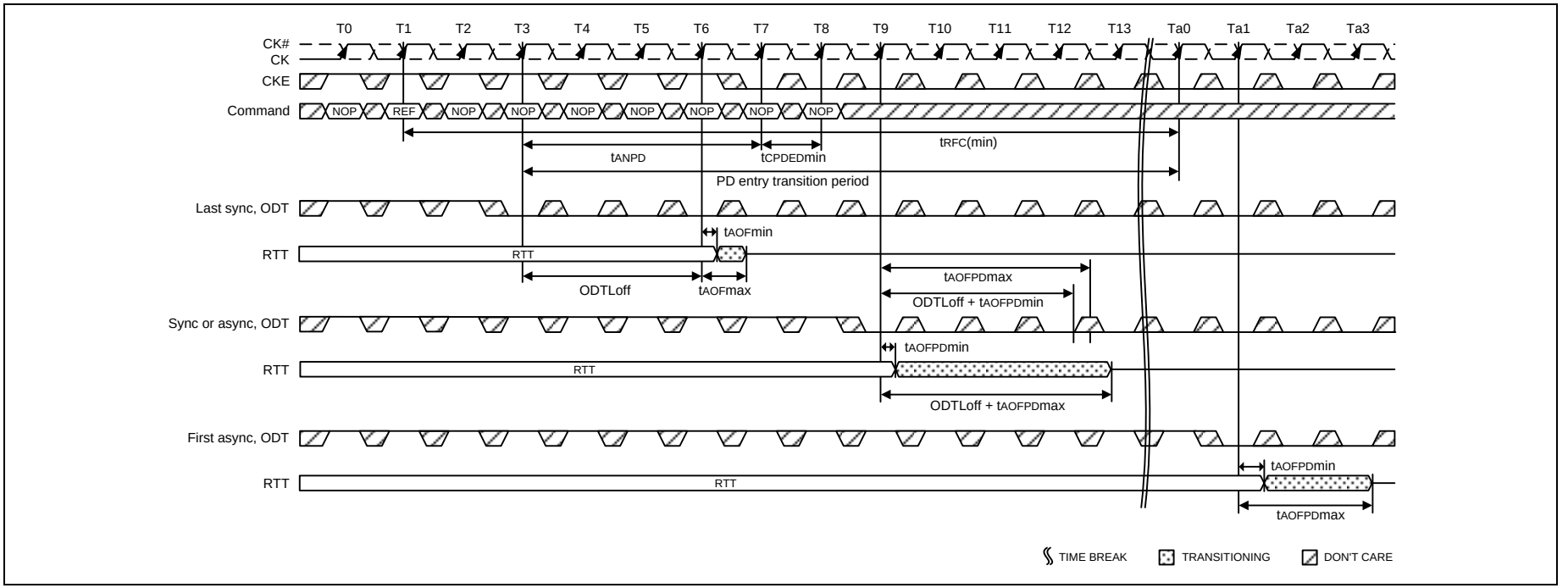


Figure 84 – Synchronous to asynchronous transition after Refresh command (AL = 0; CWL = 5; tANPD = WL - 1 = 4)

8.19.4.3 Asynchronous to Synchronous ODT Mode Transition during Power-Down Exit

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to “0”, there is also a transition period around power down exit, where either synchronous or asynchronous response to a change in ODT must be expected from the DDR3 SDRAM.

This transition period starts t_{ANPD} before CKE is first registered high, and ends t_{XPDLL} after CKE is first registered high. t_{ANPD} is equal to (WL - 1) and is counted (backwards) from the clock cycle where CKE is first registered high.

ODT assertion during the transition period may result in an RTT change as early as the smaller of $t_{AONPD}min$ and ($ODTLon*t_{CK(avg)} + t_{AON}min$) and as late as the larger of $t_{AONPD}max$ and ($ODTLon*t_{CK(avg)} + t_{AON}max$). ODT de-assertion during the transition period may result in an RTT change as early as the smaller of $t_{AOFPD}min$ and ($ODTLoff*t_{CK(avg)} + t_{AOF}min$) and as late as the larger of $t_{AOFPD}max$ and ($ODTLoff*t_{CK(avg)} + t_{AOF}max$). See Table 14.

Note that, if AL has a large value, the range where RTT is uncertain becomes quite large. Figure 85 shows the three different cases: ODT_C, asynchronous response before t_{ANPD}; ODT_B has a state change of ODT during the transition period; ODT_A shows a state change of ODT after the transition period with synchronous response.

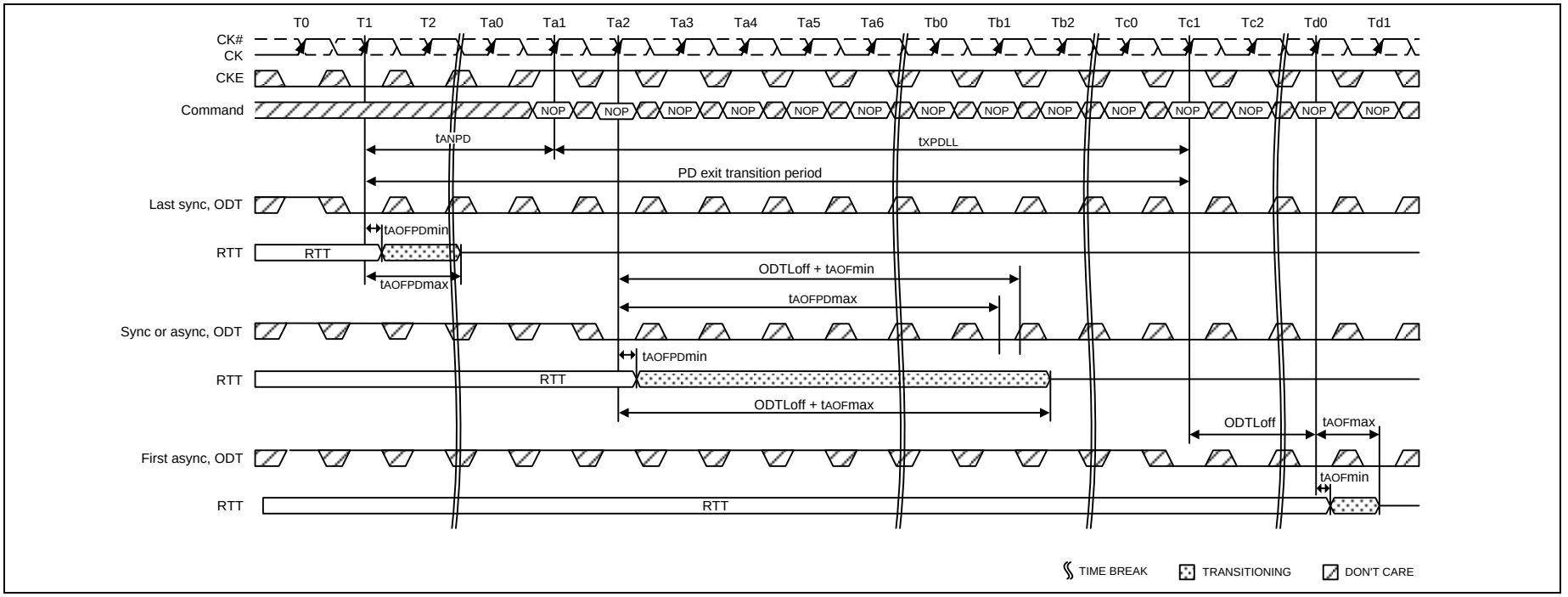


Figure 85 – Asynchronous to synchronous transition during Precharge Power Down (with DLL frozen) exit (CL = 6; AL = CL - 1; CWL = 5; t_{ANPD} = WL - 1 = 9)

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8.19.4.4 Asynchronous to Synchronous ODT Mode during short CKE high and short CKE low periods

If the total time in Precharge Power Down state or Idle state is very short, the transition periods for PD entry and PD exit may overlap (see Figure 86). In this case, the response of the DDR3 SDRAMs RTT to a change in ODT state at the input may be synchronous OR asynchronous from the start of the PD entry transition period to the end of the PD exit transition period (even if the entry period ends later than the exit period).

If the total time in Idle state is very short, the transition periods for PD exit and PD entry may overlap. In this case the response of the DDR3 SDRAMs RTT to a change in ODT state at the input may be synchronous OR asynchronous from the start of the PD exit transition period to the end of the PD entry transition period. Note that in the bottom part of Figure 86 it is assumed that there was no Refresh command in progress when Idle state was entered.

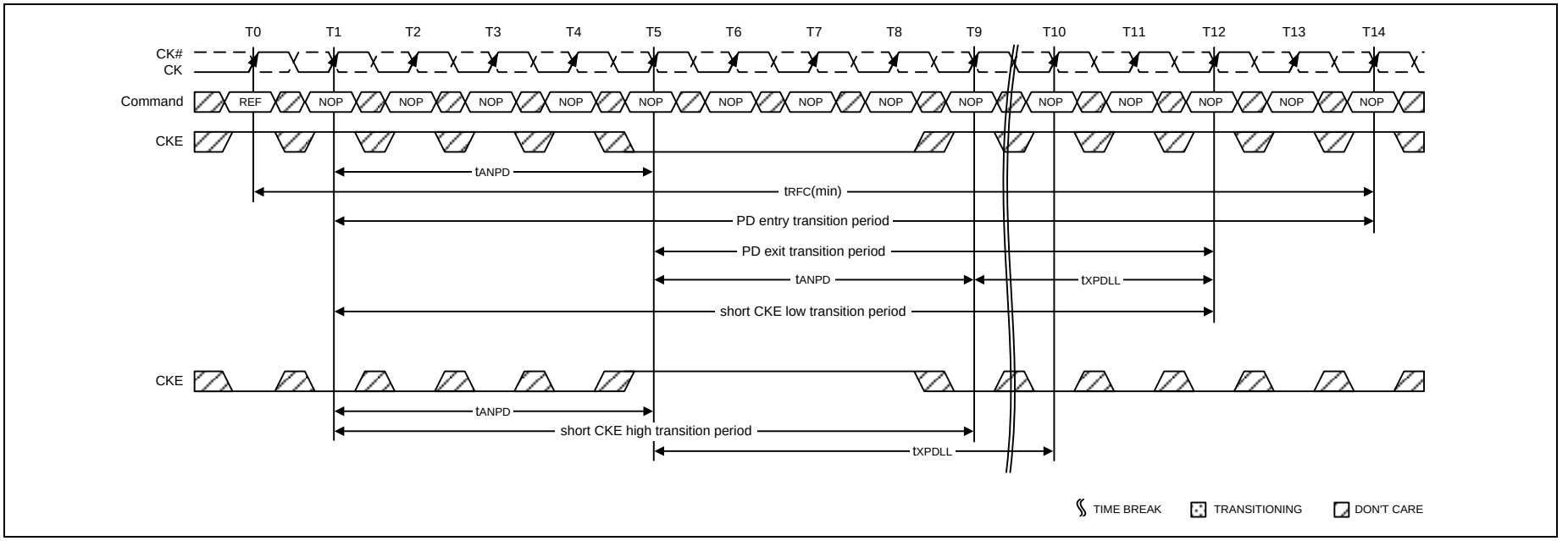


Figure 86 – Transition period for short CKE cycles, entry and exit period overlapping (AL = 0, WL = 5, tANPD = WL - 1 = 4)

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9. OPERATION MODE

9.1 Command Truth Table

Notes 1, 2, 3 and 4 apply to the entire Command Truth Table.

Note 5 Applies to all Read/Write commands.

[BA=Bank Address, RA=Row Address, CA=Column Address, BC#=Burst Chop, X=Don't Care, V=Valid]

Table 15 – Command Truth Table

COMMAND	Abbr.	CKE		CS#	RAS#	CAS#	WE#	BA0-BA2	A13	A12/BC#	A10/AP	A0-A9, A11	NOTES
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9,12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	5
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	5
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	5
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	5
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	5
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	5
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	5
Read (BC4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	5
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	5
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	5
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	5
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	5
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

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Notes:

1. All DDR3 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependent.
2. RESET# is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-fly BL will be defined by MRS.
6. The Power Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Self Refresh Exit is asynchronous.
9. V_{REF} (Both V_{REFDQ} and V_{REFCA}) must be maintained during Self Refresh operation. V_{REFDQ} supply may be turned OFF and V_{REFDQ} may take any value between V_{SS} and V_{DD} during Self Refresh operation, provided that V_{REFDQ} is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.
10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a pervious operation that is still executing, such as a burst read or write cycle.
11. The Deselect command performs the same function as No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition.

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9.2 CKE Truth Table

Notes 1-7 apply to the entire CKE Truth Table.

For Power-down entry and exit parameters See 8.17 **"Power-Down Modes"** on page 69.

CKE low is allowed only if tMRD and tMOD are satisfied.

Table 16 – CKE Truth Table

CURRENT STATE[2]	CKE		COMMAND (N)[3] RAS#, CAS#, WE#, CS#	ACTION (N)[3]	NOTES
	Previous Cycle [1] (N-1)	Current Cycle [1] (N)			
Power Down	L	L	X	Maintain Power Down	14,15
	L	H	DESELECT or NOP	Power Down Exit	11,14
Self Refresh	L	L	X	Maintain Self Refresh	15,16
	L	H	DESELECT or NOP	Self Refresh Exit	8,12,16
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	11,13,14
Reading	H	L	DESELECT or NOP	Power Down Entry	11,13,14,17
Writing	H	L	DESELECT or NOP	Power Down Entry	11,13,14,17
Precharging	H	L	DESELECT or NOP	Power Down Entry	11,13,14,17
Refreshing	H	L	DESELECT or NOP	Precharge Power Down Entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge Power Down Entry	11,13,14,18
	H	L	REFRESH	Self Refresh	9,13,18
Any other state	Refer to section 9.1 **"Command Truth Table"** on page 94 for more detail with all command signals				10

Notes:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
6. During any CKE transition (registration of CKE H->L or CKE L->H) the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).
7. DESELECT and NOP are defined in the Command Truth Table.
8. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.
9. Self Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power Down Entry and Exit are NOP and DESELECT only.
12. Valid commands for Self Refresh Exit are NOP and DESELECT only.
13. Self Refresh can not be entered during Read or Write operations. For a detailed list of restrictions See section 8.16 **"Self-Refresh Operation"** on page 67 and See section 8.17 **"Power-Down Modes"** on page 69.
14. The Power Down does not perform any refresh operations.
15. "X" means "don't care" (including floating around VREF) in Self Refresh and Power Down. It also applies to Address pins.
16. VREF (Both VREFDQ and VREFCA) must be maintained during Self Refresh operation. VREFDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh operation, provided that VREFDQ is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power Down is entered, otherwise Active Power Down is entered.
18. 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self Refresh exit and Power Down Exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

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9.3 Simplified State Diagram

This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

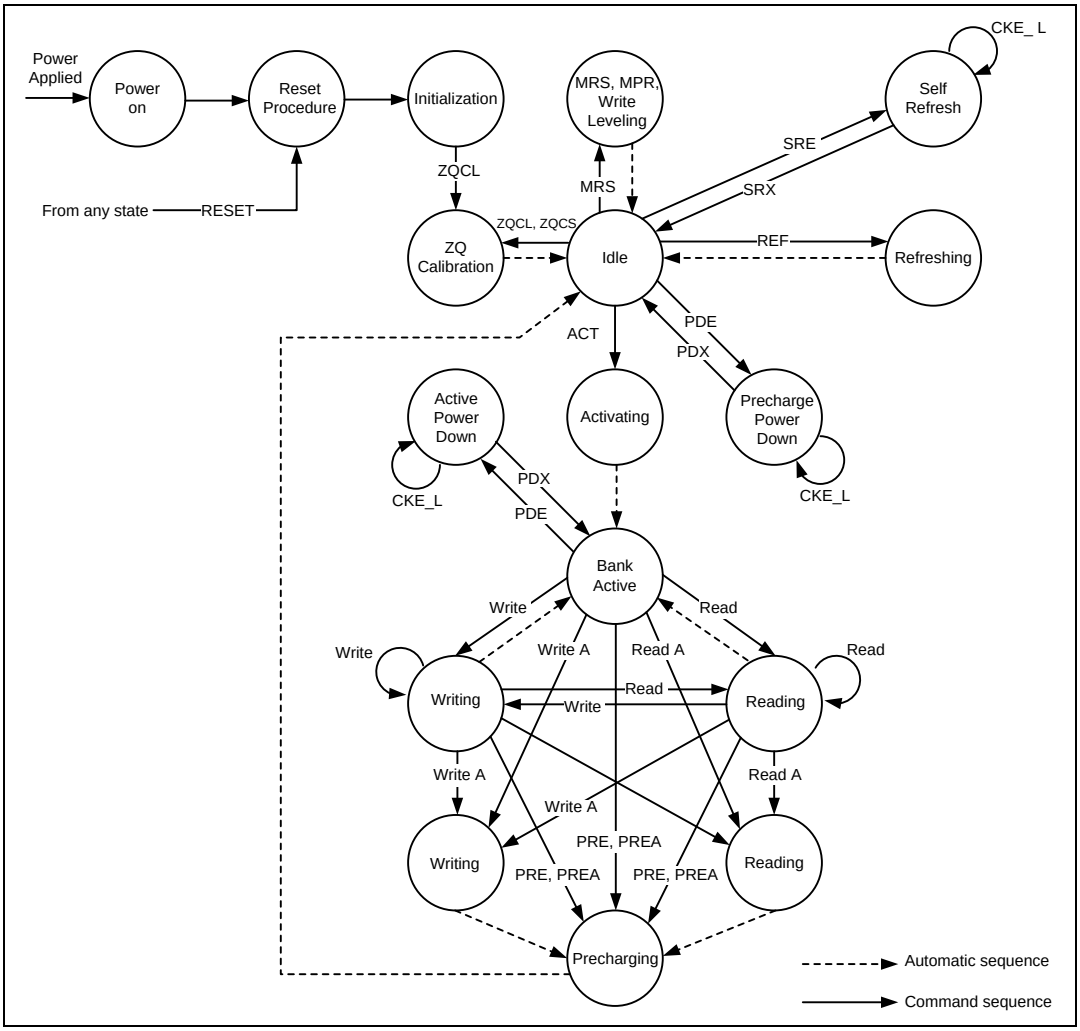


Figure 87 – Simplified State Diagram

Table 17 – State Diagram Command Definitions

Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Active	Read	RD, RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	Precharge All	Write	WR, WRS4, WRS8	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA, WRAS4, WRAS8	SRX	Self-Refresh exit
REF	Refresh	RESET	Start RESET Procedure	MPR	Multi-Purpose Register
ZQCL	ZQ Calibration Long	ZQCS	ZQ Calibration Short	-	-
NOTE: See **"Command Truth Table"** on page 94 for more details					

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10. ELECTRICAL CHARACTERISTICS

10.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT	NOTES
Voltage on VDD pin relative to VSS	VDD	-0.4 ~ 1.975	V	1, 3
Voltage on VDDQ pin relative to VSS	VDDQ	-0.4 ~ 1.975	V	1, 3
Voltage on any pin relative to VSS	VIN, VOUT	-0.4 ~ 1.975	V	1
Storage Temperature	TSTG	-55 ~ 150	°C	1, 2

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times. VREFDQ and VREFCA must not greater than 0.6 x VDDQ. When VDD and VDDQ are less than 500 mV, VREFDQ and VREFCA may be equal to or less than 300 mV.

10.2 Operating Temperature Condition

PARAMETER	SYMBOL	RATING	UNIT	NOTES
Commercial operating temperature range (for -09/-11/-12/-15)	TOPER	0 ~ 85	°C	1, 2
		0 ~95	°C	1, 2, 4
Industrial operating temperature range (for 09I/11I/12I/15I)	TOPER	-40 ~ 85	°C	1, 3
		-40 ~ 95	°C	1, 3, 4
Industrial Plus operating temperature range (for 09J/11J/12J/15J)	TOPER	-40 ~ 85	°C	1, 3
		-40 ~ 105	°C	1, 3, 4

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. During operation, the DRAM case temperature must be maintained between 0 to 95°C for Commercial parts under all specification parameters.
3. During operation, the DRAM case temperature must be maintained between -40 to 95°C for Industrial parts and -40 to 105°C for Industrial Plus parts under all specification parameters.
4. Some applications require operation of the 85°C < TCASE ≤ 95°C operating temperature. Full specifications are provided in this range, but the following additional conditions apply:
   (a) Refresh commands have to be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µS.
   (b) If Self-Refresh operation is required in 85°C < TCASE ≤ 105°C operating temperature range, than it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0_b and MR2 A7 = 1_b) or enable the Auto Self-Refresh mode (ASR) (MR2 A6 = 1_b, MR2 A7 is don't care).

10.3 DC & AC Operating Conditions

10.3.1 Recommended DC Operating Conditions

SYM.	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
VDD	Supply Voltage	1.425	1.5	1.575	V	1, 2
VDDQ	Supply Voltage for Output	1.425	1.5	1.575	V	1, 2
RZQ	External Calibration Resistor connected from ZQ ball to ground	237.6	240.0	242.4	Ω	3

Notes:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. The external calibration resistor RZQ can be time-shared among DRAMs in special applications.

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10.4 Input and Output Leakage Currents

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
I_{IL}	Input Leakage Current ($0V \le V_{IN} \le V_{DD}$)	-2	2	µA	1
I_{OL}	Output Leakage Current (Output disabled, $0V \le V_{OUT} \le V_{DDQ}$)	-5	5	µA	2

Notes:

1. All other balls not under test = 0 V.
2. All DQ, DQS and DQS# are in high-impedance mode.

10.5 Interface Test Conditions

Figure 88 represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

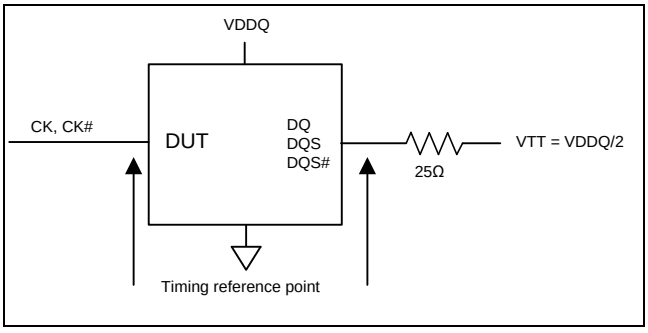


Figure 88 – Reference Load for AC Timings and Output Slew Rates

The Timing Reference Points are the idealized input and output nodes / terminals on the outside of the packaged SDRAM device as they would appear in a schematic or an IBIS model.

The output timing reference voltage level for single ended signals is the cross point with V_{TT}.

The output timing reference voltage level for differential signals is the cross point of the true (e.g. DQS) and the complement (e.g. DQS#) signal.

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10.6 DC and AC Input Measurement Levels

10.6.1 DC and AC Input Levels for Single-Ended Command and Address Signals

Table 18 – Single-Ended DC and AC Input Levels for Command and Address

PARAMETER	SYMBOL	DDR3-1333, DDR3-1600		DDR3-1866/2133		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
DC input logic high	$V_{IH.CA(DC100)}$	V_{REF} + 0.100	V_{DD}	V_{REF} + 0.100	V_{DD}	V	1, 5
DC input logic low	$V_{IL.CA(DC100)}$	V_{SS}	V_{REF} - 0.100	V_{SS}	V_{REF} - 0.100	V	1, 6
AC input logic high	$V_{IH.CA(AC175)}$	V_{REF} + 0.175	Note 2	-	-	V	1, 2, 7
AC input logic low	$V_{IL.CA(AC175)}$	Note 2	V_{REF} - 0.175	-	-	V	1, 2, 8
AC input logic high	$V_{IH.CA(AC150)}$	V_{REF} + 0.150	Note 2	-	-	V	1, 2, 7
AC input logic low	$V_{IL.CA(AC150)}$	Note 2	V_{REF} - 0.150	-	-	V	1, 2, 8
AC input logic high	$V_{IH.CA(AC135)}$	-	-	V_{REF} + 0.135	Note 2	V	1, 2, 7
AC input logic low	$V_{IL.CA(AC135)}$	-	-	Note 2	V_{REF} - 0.135	V	1, 2, 8
AC input logic high	$V_{IH.CA(AC125)}$	-	-	V_{REF} + 0.125	Note 2	V	1, 2, 7
AC input logic low	$V_{IL.CA(AC125)}$	-	-	Note 2	V_{REF} - 0.125	V	1, 2, 8
Reference Voltage for ADD, CMD inputs	$V_{REFCA(DC)}$	0.49 x V_{DD}	0.51 x V_{DD}	0.49 x V_{DD}	0.51 x V_{DD}	V	3, 4, 9

Notes:

1. For input only pins except RESET#. V_{REF} = $V_{REFCA(DC)}$.
2. See section 10.12 **"Overshoot and Undershoot Specifications"** on page 121.
3. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REFCA(DC)}$ by more than ± 1% V_{DD} (for reference: approx. ± 15 mV).
4. For reference: approx. $V_{DD}/2$ ± 15 mV.
5. $V_{IH(DC)}$ is used as a simplified symbol for $V_{IH.CA(DC100)}$.
6. $V_{IL(DC)}$ is used as a simplified symbol for $V_{IL.CA(DC100)}$.
7. $V_{IH(AC)}$ is used as a simplified symbol for $V_{IH.CA(AC175)}$, $V_{IH.CA(AC150)}$, $V_{IH.CA(AC135)}$, and $V_{IH.CA(AC125)}$; $V_{IH.CA(AC175)}$ value is used when V_{REF} + 0.175V is referenced, $V_{IH.CA(AC150)}$ value is used when V_{REF} + 0.15V is referenced, $V_{IH.CA(AC135)}$ value is used when V_{REF} + 0.135V is referenced, and $V_{IH.CA(AC125)}$ value is used when V_{REF} + 0.125V is referenced.
8. $V_{IL(AC)}$ is used as a simplified symbol for $V_{IL.CA(AC175)}$, $V_{IL.CA(AC150)}$, $V_{IL.CA(AC135)}$ and $V_{IL.CA(AC125)}$; $V_{IL.CA(AC175)}$ value is used when V_{REF} - 0.175V is referenced, $V_{IL.CA(AC150)}$ value is used when V_{REF} - 0.15V is referenced, $V_{IL.CA(AC135)}$ value is used when V_{REF} - 0.135V is referenced, and $V_{IL.CA(AC125)}$ value is used when V_{REF} - 0.125V is referenced.
9. $V_{REFCA(DC)}$ is measured relative to VDD at the same point in time on the same device.

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10.6.2 DC and AC Input Levels for Single-Ended Data Signals

Table 19 – Single-Ended DC and AC Input Levels for DQ and DM

PARAMETER	SYMBOL	DDR3-1333, DDR3-1600		DDR3-1866/2133		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
DC input logic high	$V_{IH.DQ(DC100)}$	V_{REF} + 0.100	V_{DD}	V_{REF} + 0.100	V_{DD}	V	1, 5
DC input logic low	$V_{IL.DQ(DC100)}$	V_{SS}	V_{REF} - 0.100	V_{SS}	V_{REF} - 0.100	V	1, 6
AC input logic high	$V_{IH.DQ(AC150)}$	V_{REF} + 0.150	Note 2	-	-	V	1, 2, 7
AC input logic low	$V_{IL.DQ(AC150)}$	Note 2	V_{REF} - 0.150	-	-	V	1, 2, 8
AC input logic high	$V_{IH.DQ(AC135)}$	-	-	V_{REF} + 0.135	Note 2	V	1, 2, 7
AC input logic low	$V_{IL.DQ(AC135)}$	-	-	Note 2	V_{REF} - 0.135	V	1, 2, 8
Reference Voltage for DQ, DM inputs	$V_{REFDQ(DC)}$	0.49 x V_{DD}	0.51 x V_{DD}	0.49 x V_{DD}	0.51 x V_{DD}	V	3, 4, 9

Notes:

1. V_{REF} = $V_{REFDQ(DC)}$.
2. See section 10.12 **"Overshoot and Undershoot Specifications"** on page 121.
3. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REFDQ(DC)}$ by more than ± 1% V_{DD} (for reference: approx. ± 15 mV).
4. For reference: approx. $V_{DD}/2$ ± 15 mV.
5. $V_{IH(DC)}$ is used as a simplified symbol for $V_{IH.DQ(DC100)}$.
6. $V_{IL(DC)}$ is used as a simplified symbol for $V_{IL.DQ(DC100)}$.
7. $V_{IH(AC)}$ is used as a simplified symbol for $V_{IH.DQ(AC150)}$, and $V_{IH.DQ(AC135)}$; $V_{IH.DQ(AC150)}$ value is used when V_{REF} + 0.15V is referenced, and $V_{IH.DQ(AC135)}$ value is used when V_{REF} + 0.135V is referenced.
8. $V_{IL(AC)}$ is used as a simplified symbol for $V_{IL.DQ(AC150)}$, and $V_{IL.DQ(AC135)}$; $V_{IL.DQ(AC150)}$ value is used when V_{REF} - 0.15V is referenced, and $V_{IL.DQ(AC135)}$ value is used when V_{REF} - 0.135V is referenced.
9. $V_{REFDQ(DC)}$ is measured relative to VDD at the same point in time on the same device.

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The DC-tolerance limits and AC-noise limits for the reference voltages V_{REFCA} and V_{REFDQ} are illustrated in Figure 89. It shows a valid reference voltage $V_{REF}(t)$ as a function of time. (V_{REF} stands for V_{REFCA} and V_{REFDQ} likewise).

$V_{REF(DC)}$ is the linear average of $V_{REF}(t)$ over a very long period of time (e.g., 1 sec). This average has to meet the min/max requirements in Table 18. Furthermore $V_{REF}(t)$ may temporarily deviate from $V_{REF(DC)}$ by no more than ± 1% V_{DD}.

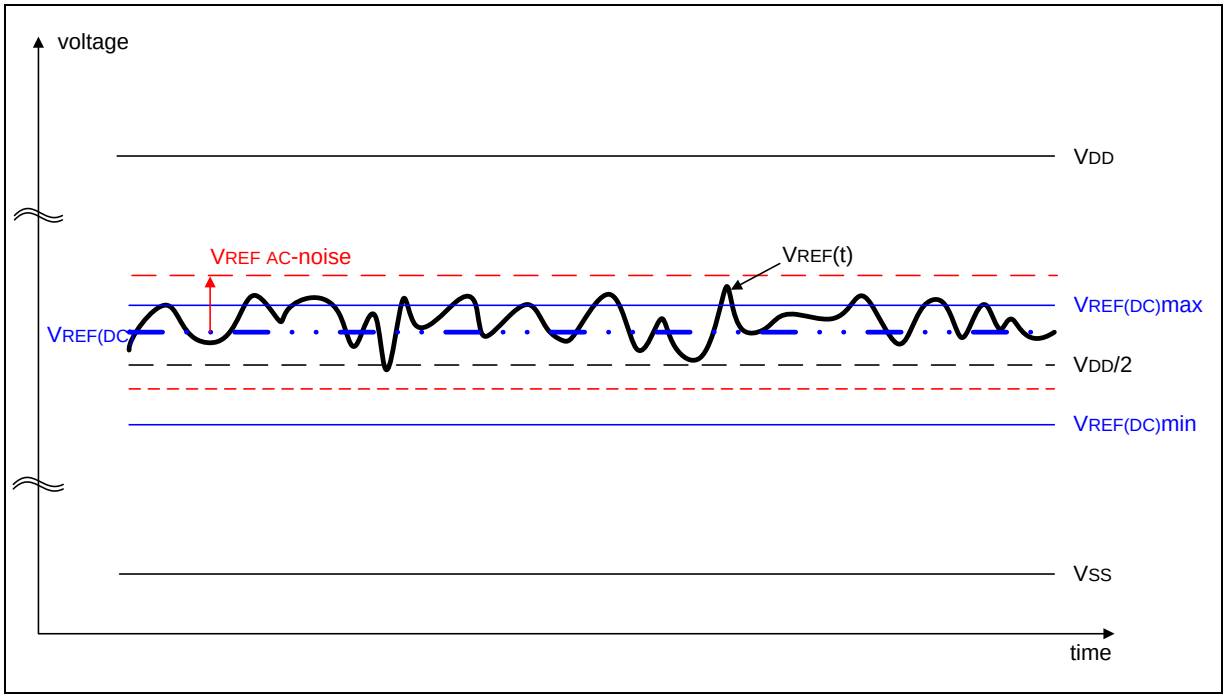


Figure 89 – Illustration of $V_{REF(DC)}$ tolerance and V_{REF} AC-noise limits

The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$, and $V_{IL(DC)}$ are dependent on V_{REF}.

"V_{REF}" shall be understood as $V_{REF(DC)}$, as defined in Figure 89.

This clarifies that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF(DC)}$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (± 1% of V_{DD}) are included in DRAM timings and their associated deratings.

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10.6.3 Differential swing requirements for clock (CK - CK#) and strobe (DQS - DQS#)

Table 20 – Differential DC and AC Input Level

PARAMETER	SYMBOL	DDR3-1333/1600/1866/2133		UNIT	NOTES
		MIN.	MAX.		
Differential input high	$V_{IH.DIFF}$	+0.200	Note 3	V	1
Differential input low	$V_{IL.DIFF}$	Note 3	-0.200	V	1
Differential input high AC	$V_{IH.DIFF(AC)}$	2 x ($V_{IH(AC)}$ - V_{REF})	Note 3	V	2
Differential input low AC	$V_{IL.DIFF(AC)}$	Note 3	2 x ($V_{IL(AC)}$ - V_{REF})	V	2

Notes:

1. Used to define a differential signal slew-rate.
2. For CK - CK# use $V_{IH.CA(AC)}$/$V_{IL.CA(AC)}$ of ADD/CMD and V_{REFCA}; for DQS, DQS# use $V_{IH.DQ(AC)}$/$V_{IL.DQ(AC)}$ of DQs and V_{REFDQ}; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined; however, the single-ended signals CK, CK#, DQS, DQS# need to be within the respective limits ($V_{IH(DC)}$ max, $V_{IL(DC)min}$) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 10.12 **"Overshoot and Undershoot Specifications"** on page 121.

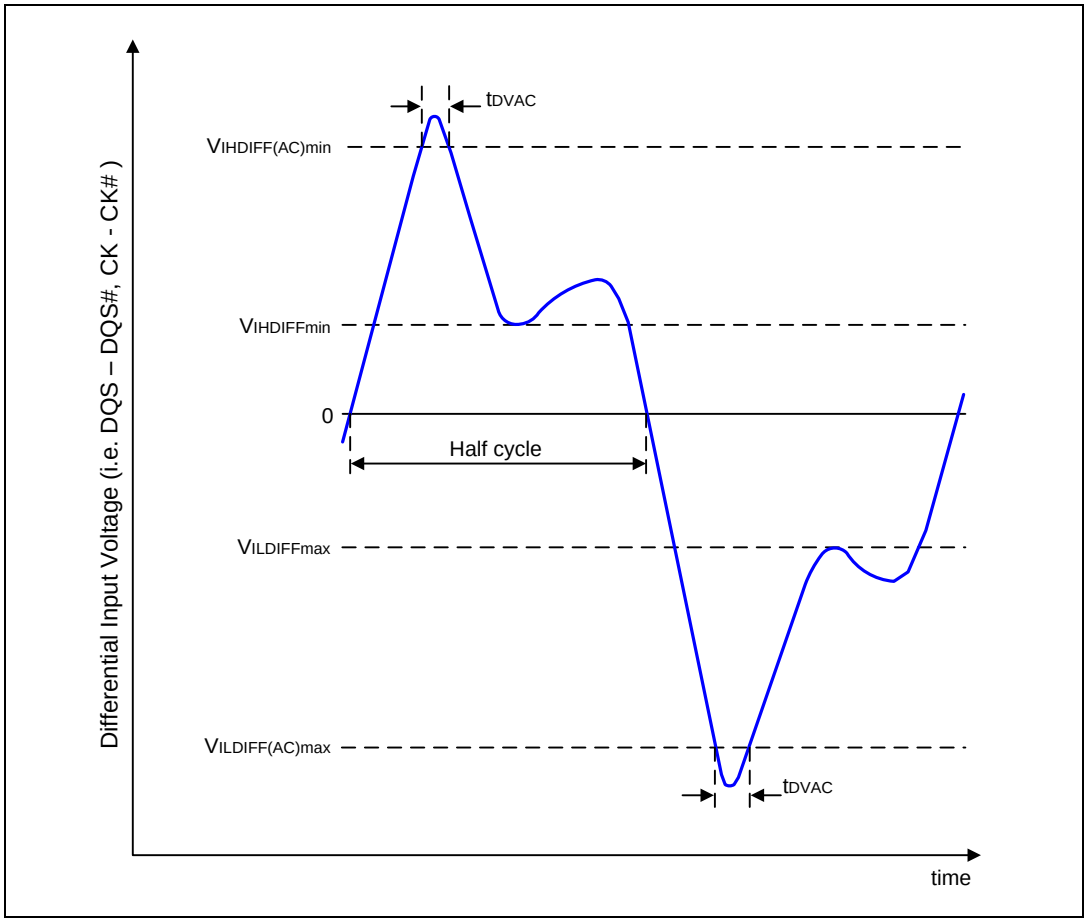


Figure 90 – Definition of differential ac-swing and "time above AC-level" t_{DVAC}

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Table 21 – Allowed time before ringback (tDVAC) for CK - CK# and DQS - DQS#

Slew Rate [V/nS]	DDR3-1333/1600				DDR3-1866/2133			
	tDVAC [pS] @ VIH/LDIFF(AC) = 350mV		tDVAC [pS] @ VIH/LDIFF(AC) = 300mV		tDVAC [pS] @ VIH/LDIFF(AC) = 300mV		tDVAC [pS] @ VIH/LDIFF(AC) = (CK - CK#) only	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
> 4.0	75	-	175	-	134	-	139	-
4.0	57	-	170	-	134	-	139	-
3.0	50	-	167	-	112	-	118	-
2.0	38	-	119	-	67	-	77	-
1.8	34	-	102	-	52	-	63	-
1.6	29	-	81	-	33	-	45	-
1.4	22	-	54	-	9	-	23	-
1.2	Note	-	19	-	Note	-	Note	-
1.0	Note	-	Note	-	Note	-	Note	-
< 1.0	Note	-	Note		Note	-	Note	-

Note:

Rising input differential signal shall become equal to or greater than VIHDIFF(AC) level and Falling input differential signal shall become equal to or less than VILDIFF(AC) level.

10.6.4 Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, CK#, DQS#) has also to comply with certain requirements for single-ended signals.

CK and CK# have to approximately reach VSEHmin / VSELmax (approximately equal to the AC-levels (VIH.CA(AC) / VIL.CA(AC)) for ADD/CMD signals) in every half-cycle.

DQS, DQS # have to reach VSEHmin / VSELmax (approximately the AC-levels (VIH.DQ(AC) / VIL.DQ(AC)) for DQ signals) in every half-cycle preceding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g., if VIH.CA(AC150)/VIL.CA(AC150) is used for ADD/CMD signals, then these AC-levels apply also for the single-ended signals CK and CK#.

Table 22 – Single-ended levels for CK, DQS, CK#, DQS#

PARAMETER	SYM.	DDR3-1333/1600/1866/2133		UNIT	NOTES
		MIN.	MAX.		
Single-ended high level for strobes	VSEH	(VDD/2) + 0.175	Note 3	V	1, 2
Single-ended high level for CK, CK#		(VDD/2) + 0.175	Note 3	V	1, 2
Single-ended low level for strobes	VSEL	Note 3	(VDD/2) - 0.175	V	1, 2
Single-ended low level for CK, CK#		Note 3	(VDD/2) - 0.175	V	1, 2

Notes:

1. For CK, CK# use VIH.CA(AC) / VIL..CA(AC) of ADD/CMD; for strobes (DQS, DQS#) use VIH.DQ(AC) / VIL.DQ(AC) of DQs.
2. VIH.DQ(AC) / VIL.DQ(AC) for DQs is based on VREFDQ; VIH.CA(AC) / VIL.CA(AC) for ADD/CMD is based on VREFCA; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined; however, the single-ended signals CK, CK#, DQS, DQS# need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 10.12 **"Overshoot and Undershoot Specifications"** on page 121.

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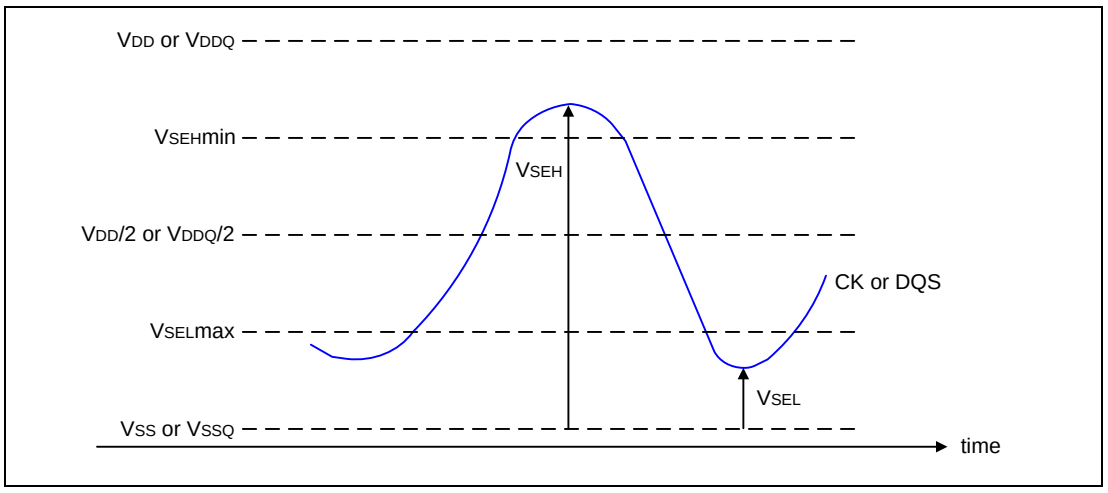


Figure 91 – Single-ended requirement for differential signals

Note that, while ADD/CMD and DQ signal requirements are with respect to V_{REF}, the single-ended components of differential signals have a requirement with respect to $V_{DD}/2$; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach V_{SELmax}, V_{SEHmin} has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

10.6.5 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, CK# and DQS, DQS#) must meet the requirements in Table 23. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the midlevel between of V_{DD} and V_{SS}.

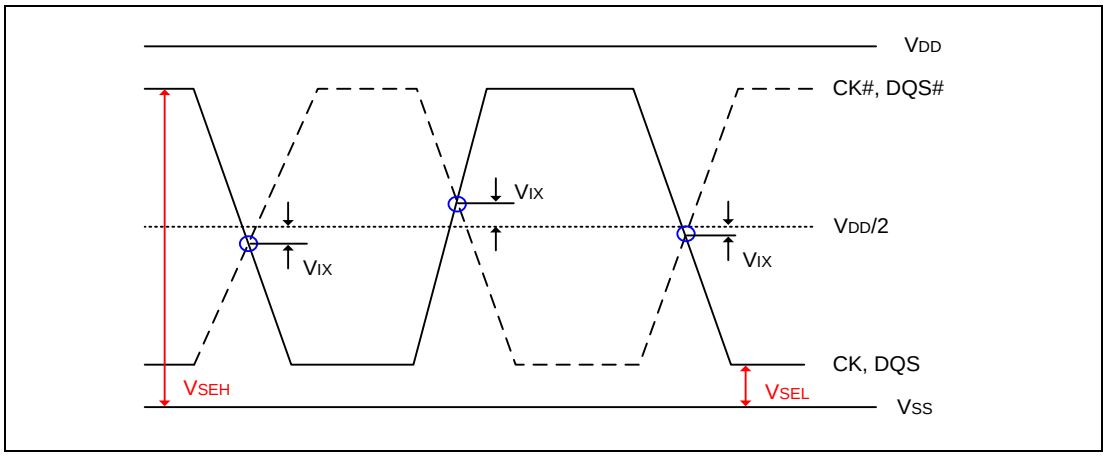


Figure 92 – V_{IX} Definition

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Table 23 – Cross point voltage for differential input signals (CK, DQS)

PARAMETER	SYMBOL	DDR3-1333/1600/1866/2133		UNIT	NOTES
		MIN.	MAX.		
Differential Input Cross Point Voltage relative to VDD/2 for CK, CK#	VIX(CK)	- 150	150	mV	2
		- 175	175	mV	1
Differential Input Cross Point Voltage relative to VDD/2 for DQS, DQS#	VIX(DQS)	-150	150	mV	2

Note:

1. Extended range for VIX is only allowed for clock and if single-ended clock input signals CK and CK# are monotonic with a single-ended swing VSEL/VSEH of at least VDD/2 ± 250 mV, and when the differential slew rate of CK - CK# is larger than 3 V/nS. Refer to Table 22 for VSEL and VSEH standard values.
2. The relation between VIX Min/Max and VSEL/VSEH should satisfy following.
   (VDD/2) + VIX (Min) - VSEL ≥ 25mV
   VSEH - ((VDD/2) + VIX (Max)) ≥ 25mV

10.6.6 Slew Rate Definitions for Single-Ended Input Signals

See section 10.16.4 **"Address / Command Setup, Hold and Derating"** on page 150 for single-ended slew rate definitions for address and command signals.

See section 10.16.5 **"Data Setup, Hold and Slew Rate Derating"** on page 157 for single-ended slew rate definitions for data signals.

10.6.7 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, CK# and DQS, DQS#) are defined and measured as shown in Table 24 and Figure 93.

Table 24 – Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK - CK# and DQS - DQS#)	VIL.DIFFmax	VIH.DIFFmin	[VIH.DIFFmin - VIL.DIFFmax] / ΔTR.DIFF
Differential input slew rate for falling edge (CK - CK# and DQS - DQS#)	VIH.DIFFmin	VIL.DIFFmax	[VIH.DIFFmin - VIL.DIFFmax] / ΔTF.DIFF

Note: The differential signal (i.e., CK - CK# and DQS - DQS#) must be linear between these thresholds

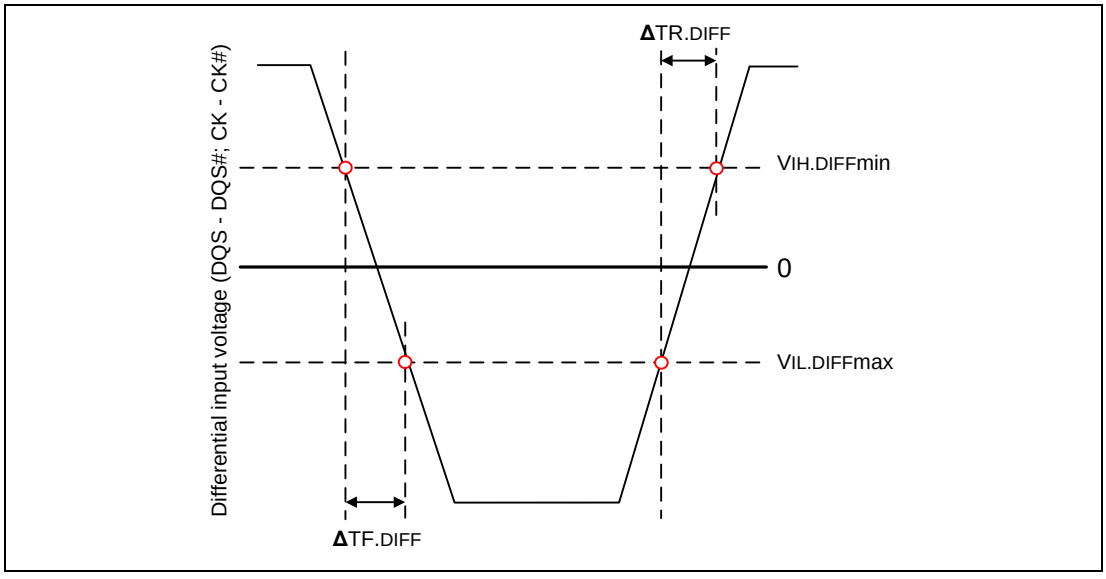


Figure 93 – Differential Input Slew Rate Definition for DQS, DQS# and CK, CK#

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10.7 DC and AC Output Measurement Levels

Table 25 – Single-ended DC and AC Output Levels

PARAMETER	SYMBOL	VALUE	UNIT	NOTES
DC output high measurement level (for IV curve linearity)	$V_{OH(DC)}$	0.8 x V_{DDQ}	V	
DC output mid measurement level (for IV curve linearity)	$V_{OM(DC)}$	0.5 x V_{DDQ}	V	
DC output low measurement level (for IV curve linearity)	$V_{OL(DC)}$	0.2 x V_{DDQ}	V	
AC output high measurement level (for output slew rate)	$V_{OH(AC)}$	V_{TT} + 0.1 x V_{DDQ}	V	1
AC output low measurement level (for output slew rate)	$V_{OL(AC)}$	V_{TT} - 0.1 x V_{DDQ}	V	1

Note:

1. The swing of ± 0.1 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 34 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2.

Table 26 – Differential DC and AC Output Levels

PARAMETER	SYMBOL	VALUE		UNIT	NOTES
		MIN.	MAX.		
AC differential output high measurement level (for output slew rate)	$V_{OH.DIFF(AC)}$	+0.2 x V_{DDQ}		V	1
AC differential output low measurement level (for output slew rate)	$V_{OL.DIFF(AC)}$	-0.2 x V_{DDQ}		V	1

Note:

1. The swing of ± 0.2 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 34 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2 at each of the differential outputs.

10.7.1 Output Slew Rate Definition and Requirements

The slew rate definition depends if the signal is single-ended or differential. For the relevant AC output reference levels see above Table 25 and Table 26.

Table 27 – Output Slew Rate

PARAMETER	SYMBOL	DDR3-1333/1600		DDR3-1866/2133		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
Single-ended Output Slew Rate	SRQse	2.5	5	2.5	5*[1]	V/nS	1, 2, 3
Differential Output Slew Rate	SRQdiff	5	10	5	12	V/nS	2, 3

Notes:

1. In two cases, a maximum slew rate of 6 V/nS applies for a single DQ signal within a byte lane.
   - **Case 1** is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e they stay at either high or low).
   - **Case 2** is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5 V/nS applies.
2. Background for Symbol Nomenclature: SR: Slew Rate; Q: Query Output (like in DQ, which stands for Data-in, Query-Output); se: Single-ended Signals; diff: Differential Signals.
3. For R_{ON} = RZQ/7 settings only.

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10.7.1.1 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 28 and Figure 94.

Table 28 – Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	[$V_{OH(AC)}$ - $V_{OL(AC)}$] / ΔTRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	[$V_{OH(AC)}$ - $V_{OL(AC)}$] / ΔTFse

Note: Output slew rate is verified by design and characterization, and may not be subject to production test.

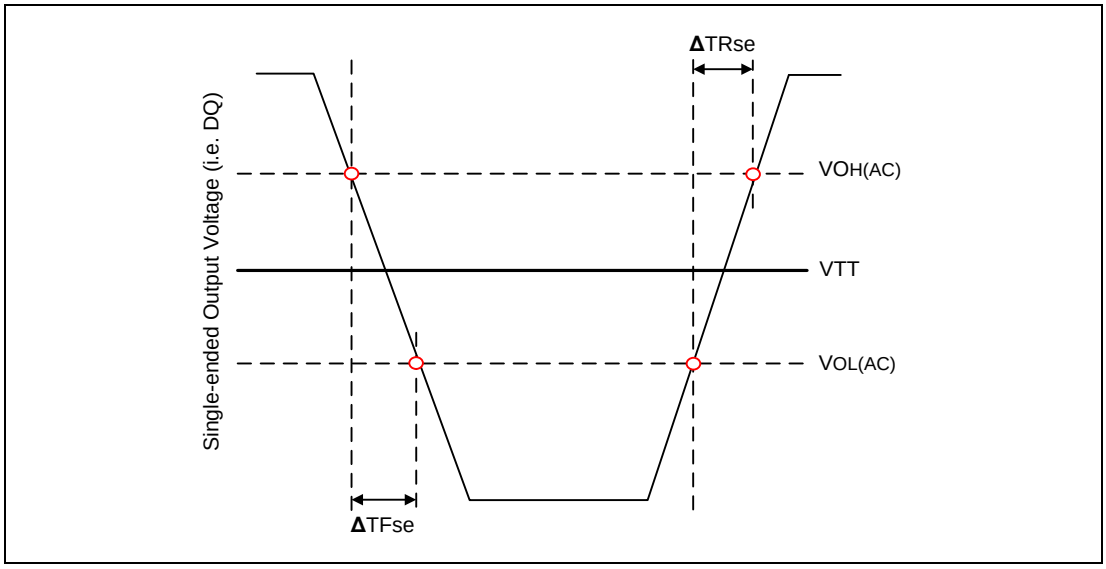


Figure 94 –Single-ended Output Slew Rate Definition

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10.7.1.2 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL.DIFFAC) and VOH.DIFF(AC) for differential signals as shown in Table 29 and Figure 95.

Table 29 – Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	VOL.DIFF(AC)	VOH.DIFF(AC)	[VOH.DIFF(AC) - VOL.DIFF(AC)] / ΔTRdiff
Differential output slew rate for falling edge	VOH.DIFF(AC)	VOL.DIFF(AC)	[VOH.DIFF(AC) - VOL.DIFF(AC)] / ΔTFdiff

Note: Output slew rate is verified by design and characterization, and may not be subject to production test.

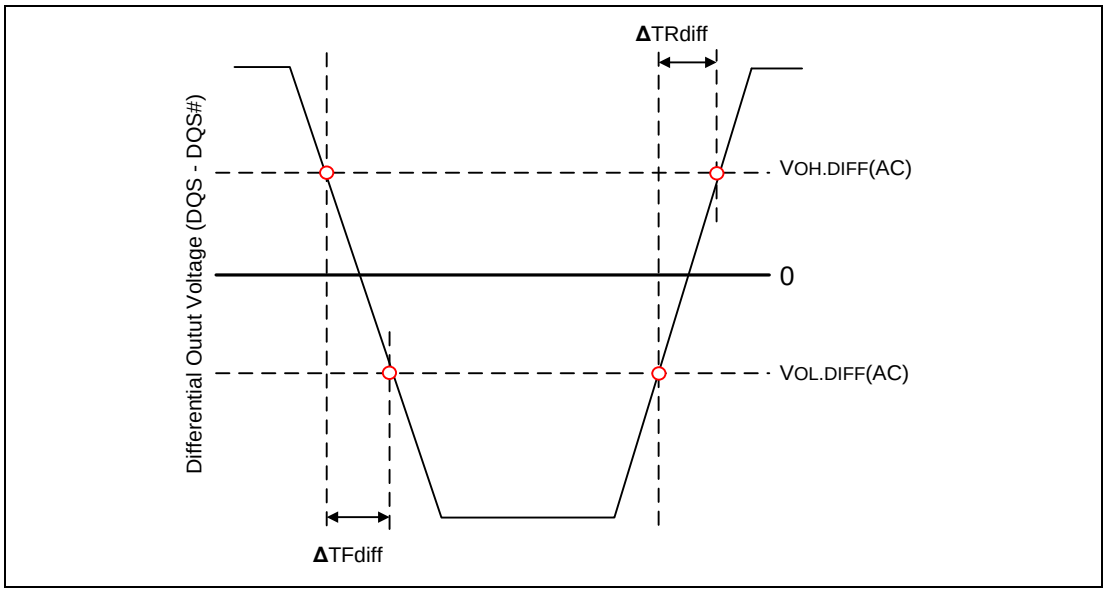


Figure 95 – Differential Output Slew Rate Definition

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10.8 34 ohm Output Driver DC Electrical Characteristics

A functional representation of the output buffer is shown in Figure 96. Output driver impedance *RON* is selected by bits “D.I.C” A1 and A5 in the MR1 Register. Two different values can be selected via MR1 settings:

RON_{34} = R_{ZQ} / 7 (nominal 34.3 Ω ±10% with nominal R_{ZQ} = 240 Ω)
RON_{40} = R_{ZQ} / 6 (nominal 40.0 Ω ±10% with nominal R_{ZQ} = 240 Ω)

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$RON_{Pu} = \frac{V_{DDQ} - V_{Out}}{|I_{Out}|}$ under the condition that RON_{Pd} is turned off

$RON_{Pd} = \frac{V_{Out}}{|I_{Out}|}$ under the condition that RON_{Pu} is turned off

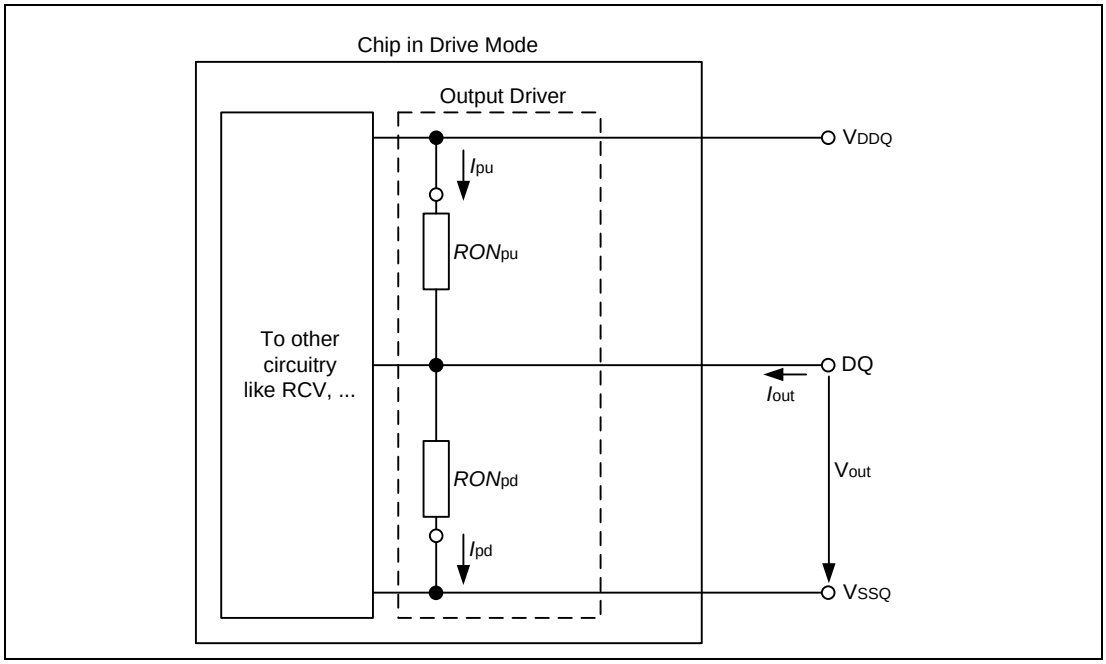


Figure 96 – Output Driver: Definition of Voltages and Currents

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Table 30 – Output Driver DC Electrical Characteristics, assuming RZQ = 240 Ω; entire operating temperature range; after proper ZQ calibration

*RON*Nom	Resistor	VOUT	MIN.	NOM.	MAX.	UNIT	NOTES
34 Ω	*RON*34Pd	V_{OLDC} = 0.2 × V_{DDQ}	0.6	1.0	1.1	*RZQ*/7	1, 2, 3
		V_{OMDC} = 0.5 × V_{DDQ}	0.9	1.0	1.1	*RZQ*/7	1, 2, 3
		V_{OHDC} = 0.8 × V_{DDQ}	0.9	1.0	1.4	*RZQ*/7	1, 2, 3
	*RON*34Pu	V_{OLDC} = 0.2 × V_{DDQ}	0.9	1.0	1.4	*RZQ*/7	1, 2, 3
		V_{OMDC} = 0.5 × V_{DDQ}	0.9	1.0	1.1	*RZQ*/7	1, 2, 3
		V_{OHDC} = 0.8 × V_{DDQ}	0.6	1.0	1.1	*RZQ*/7	1, 2, 3
40 Ω	*RON*40Pd	V_{OLDC} = 0.2 × V_{DDQ}	0.6	1.0	1.1	*RZQ*/6	1, 2, 3
		V_{OMDC} = 0.5 × V_{DDQ}	0.9	1.0	1.1	*RZQ*/6	1, 2, 3
		V_{OHDC} = 0.8 × V_{DDQ}	0.9	1.0	1.4	*RZQ*/6	1, 2, 3
	*RON*40Pu	V_{OLDC} = 0.2 × V_{DDQ}	0.9	1.0	1.4	*RZQ*/6	1, 2, 3
		V_{OMDC} = 0.5 × V_{DDQ}	0.9	1.0	1.1	*RZQ*/6	1, 2, 3
		V_{OHDC} = 0.8 × V_{DDQ}	0.6	1.0	1.1	*RZQ*/6	1, 2, 3
Mismatch between pull-up and pull-down, *MM*PuPd		V_{OMDC} = 0.5 × V_{DDQ}	-10		+10	%	1, 2, 4

Notes:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that V_{DDQ} = V_{DD} and that V_{SSQ} = V_{SS}.
3. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 × V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 × V_{DDQ} and 0.8 × V_{DDQ}.
4. Measurement definition for mismatch between pull-up and pull-down, *MM*PuPd:

   Measure *RON*Pu and *RON*Pd, both at 0.5 * V_{DDQ}:

$$MM_{PuPd} = \frac{RON_{Pu} - RON_{Pd}}{RON_{Nom}} \times 100\%$$

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10.8.1 Output Driver Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 31 and Table 32.

$\Delta T = T - T(@calibration)$; $\Delta V = V_{DDQ} - V_{DDQ}(@calibration)$; $V_{DD} = V_{DDQ}$

Note: dR_{ONdT} and dR_{ONdV} are not subject to production test but are verified by design and characterization.

Table 31 – Output Driver Sensitivity Definition

	MIN.	MAX.	UNIT
RON_{PU}@ V_{OHDC}	0.6 - dR_{ONdTH}*|ΔT| - dR_{ONdVH}*|ΔV|	1.1 + dR_{ONdTH}*|ΔT| + dR_{ONdVH}*|ΔV|	*RZQ*/7
RON@ V_{OMDC}	0.9 - dR_{ONdTM}*|ΔT| - dR_{ONdVM}*|ΔV|	1.1 + dR_{ONdTM}*|ΔT| + dR_{ONdVM}*|ΔV|	*RZQ*/7
RON_{PD}@ V_{OLDC}	0.6 - dR_{ONdTL}*|ΔT| - dR_{ONdVL}*|ΔV|	1.1 + dR_{ONdTL}*|ΔT| + dR_{ONdVL}*|ΔV|	*RZQ*/7

Table 32 – Output Driver Voltage and Temperature Sensitivity

Speed Bin	DDR3-1333		DDR3-1600/1866/2133		UNIT
	MIN.	MAX.	MIN.	MAX.	
dR_{ONdTM}	0	1.5	0	1.5	%/°C
dR_{ONdVM}	0	0.15	0	0.13	%/mV
dR_{ONdTL}	0	1.5	0	1.5	%/°C
dR_{ONdVL}	0	0.15	0	0.13	%/mV
dR_{ONdTH}	0	1.5	0	1.5	%/°C
dR_{ONdVH}	0	0.15	0	0.13	%/mV

Note: These parameters may not be subject to production test. They are verified by design and characterization.

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10.9 On-Die Termination (ODT) Levels and Characteristics

10.9.1 ODT Levels and I-V Characteristics

On-Die Termination effective resistance RTT is defined by bits A9, A6 and A2 of the MR1 Register.

ODT is applied to the DQ, DM and DQS/DQS# pins.

A functional representation of the on-die termination is shown in Figure 97. The individual pull-up and pull-down resistors (RTT_{Pu} and RTT_{Pd}) are defined as follows:

$RTT_{Pu} = \frac{V_{DDQ} - V_{Out}}{|I_{Out}|}$ under the condition that RTT_{Pd} is turned off

$RTT_{Pd} = \frac{V_{Out}}{|I_{Out}|}$ under the condition that RTT_{Pu} is turned off

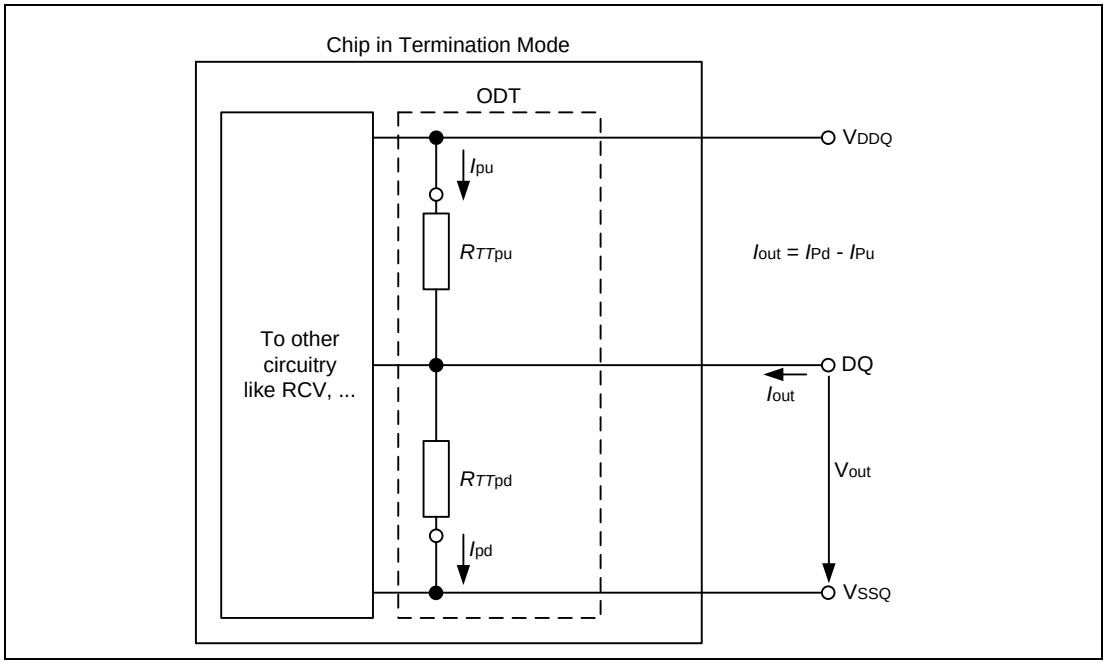


Figure 97 – On-Die Termination: Definition of Voltages and Currents

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10.9.2 ODT DC Electrical Characteristics

An overview about the specification requirements for R_{TT} and ΔV_M is provided in Table 33.

Table 33 – ODT DC Impedance and Mid-Level Requirements

MR1 A9, A6, A2	RTT	Resistor	Vout	Min.	Nom.	Max.	Unit	Notes
0, 1, 0	120 Ω	R_{TT120}	$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.0	1.6	RZQ/2	1, 2, 3, 4
0, 0, 1	60 Ω	R_{TT60}		0.9	1.0	1.6	RZQ/4	1, 2, 3, 4
0, 1, 1	40 Ω	R_{TT40}		0.9	1.0	1.6	RZQ/6	1, 2, 3, 4
1, 0, 1	30 Ω	R_{TT30}		0.9	1.0	1.6	RZQ/8	1, 2, 3, 4
1, 0, 0	20 Ω	R_{TT20}		0.9	1.0	1.6	RZQ/12	1, 2, 3, 4
Deviation of V_M with respect to $V_{DDQ}/2$, ΔV_M				-5		+5	%	1, 2, 3, 4, 5

Notes:

1. With RZQ = 240 Ω.
2. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see the following section ODT temperature and voltage sensitivity.
3. The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$.
4. Measurement definition for R_{TT} :
   Apply $V_{IH(AC)}$ to pin under test and measure current $I(V_{IH(AC)})$, then apply $V_{IL(AC)}$ to pin under test and measure current $I(V_{IL(AC)})$ respectively. Calculate R_{TT} as follows:
   $R_{TT} = [V_{IH(AC)} - V_{IL(AC)}] / [I(V_{IH(AC)}) - I(V_{IL(AC)})]$
5. Measurement definition for V_M and ΔV_M:
   Measure voltage (V_M) at test pin (midpoint) with no load. Calculate ΔV_M as follows:
   $\Delta V_M = (2 \times V_M / V_{DDQ} - 1) \times 100\%$.

10.9.3 ODT Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 34 and Table 35. The following definitions are used:

$\Delta T = T - T$ (@calibration); $\Delta V = V_{DDQ} - V_{DDQ}$ (@calibration); $V_{DD} = V_{DDQ}$

Table 34 – ODT Sensitivity Definition

SYMBOL	MIN.	MAX.	UNIT
R_{TT}	$0.9 - dR_{TT}dT \times \lvert\Delta T\rvert - dR_{TT}dV \times \lvert\Delta V\rvert$	$1.6 + dR_{TT}dT \times \lvert\Delta T\rvert + dR_{TT}dV \times \lvert\Delta V\rvert$	RZQ/2,4,6,8,12

Table 35 – ODT Voltage and Temperature Sensitivity

SYMBOL	MIN.	MAX.	UNIT
$dR_{TT}dT$	0	1.5	%/°C
$dR_{TT}dV$	0	0.15	%/mV

Note: These parameters may not be subject to production test. They are verified by design and characterization

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10.9.4 Design guide lines for RTT_{PU} and RTT_{PD}

Table 36 provides an overview of the ODT DC electrical pull-up and pull-down characteristics. The values are not specification requirements, but can be used as design guide lines.

Table 36 – ODT DC Electrical Pull-Down and Pull-Up Characteristics, assuming R_{ZQ} = 240 Ω ± 1% entire operating temperature range; after proper ZQ calibration

MR1 A9, A6, A2	RTT	Resistor	Vout	Min.	Nom.	Max.	Unit	Notes
0, 1, 0	120 Ω,	$RTT_{120PD240}$,	V_{OLDC} = 0.2 × V_{DDQ}	0.6	1.0	1.1	$R_{ZQ}/TISF_{PUPD}$	1, 2, 3, 4, 5
0, 0, 1	60 Ω,	$RTT_{60PD120}$,	V_{OMDC} = 0.5 × V_{DDQ}	0.9	1.0	1.1	$R_{ZQ}/TISF_{PUPD}$	1, 2, 3, 4, 5
0, 1, 1	40 Ω,	RTT_{40PD80},	V_{OHDC} = 0.8 × V_{DDQ}	0.9	1.0	1.4	$R_{ZQ}/TISF_{PUPD}$	1, 2, 3, 4, 5
1, 0, 1	30 Ω,	RTT_{30PD60},						
1, 0, 0	20 Ω	RTT_{20PD40}						
		$RTT_{120PU240}$,	V_{OLDC} = 0.2 × V_{DDQ}	0.9	1.0	1.4	$R_{ZQ}/TISF_{PUPD}$	1, 2, 3, 4, 5
		$RTT_{60PU120}$,	V_{OMDC} = 0.5 × V_{DDQ}	0.9	1.0	1.1	$R_{ZQ}/TISF_{PUPD}$	1, 2, 3, 4, 5
		RTT_{40PU80},	V_{OHDC} = 0.8 × V_{DDQ}	0.6	1.0	1.1	$R_{ZQ}/TISF_{PUPD}$	1, 2, 3, 4, 5
		RTT_{30PU60},						
		RTT_{20PU40}						

Notes:

1. $TISF_{PUPD}$: Termination Impedance Scaling Factor for Pull-Up and Pull-Down path:
   $TISF_{PUPD}$ = 1 for $RTT_{120PU/PD240}$
   $TISF_{PUPD}$ = 2 for $RTT_{60PU/PD120}$
   $TISF_{PUPD}$ = 3 for $RTT_{40PU/PD80}$
   $TISF_{PUPD}$ = 4 for $RTT_{30PU/PD60}$
   $TISF_{PUPD}$ = 6 for $RTT_{20PU/PD40}$
2. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see the above section ODT temperature and voltage sensitivity.
3. The tolerance limits are specified under the condition that V_{DDQ} = V_{DD} and that V_{SSQ} = V_{SS}.
4. Pull-down and pull-up ODT resistors are recommended to be calibrated at 0.5 × V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 × V_{DDQ} and 0.8 × V_{DDQ}.
5. Not a specification requirement, but a design guide line.

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10.10 ODT Timing Definitions

10.10.1 Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in Figure 98.

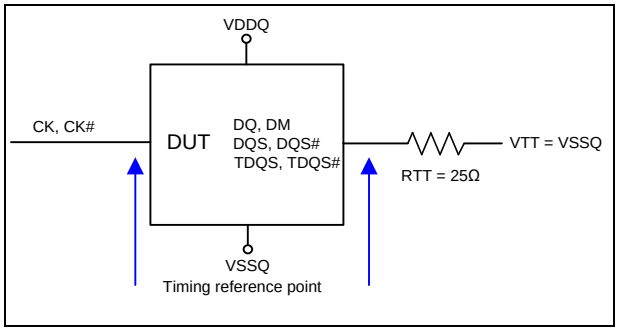


Figure 98 – ODT Timing Reference Load

10.10.2 ODT Timing Definitions

Definitions for t_{AON}, t_{AONPD}, t_{AOF}, t_{AOFPD} and t_{ADC} are provided in Table 37 and subsequent figures. Measurement reference settings are provided in Table 38.

Table 37 – ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition	Figure
t_{AON}	Rising edge of CK - CK# defined by the end point of ODTLon	Extrapolated point at V_{SSQ}	Figure 99
t_{AONPD}	Rising edge of CK - CK# with ODT being first registered high	Extrapolated point at V_{SSQ}	Figure 100
t_{AOF}	Rising edge of CK - CK# defined by the end point of ODTLoff	End point: Extrapolated point at VRtt_Nom	Figure 101
t_{AOFPD}	Rising edge of CK - CK# with ODT being first registered low	End point: Extrapolated point at VRtt_Nom	Figure 102
t_{ADC}	Rising edge of CK - CK# defined by the end point of ODTLcnw, ODTLcwn4 or ODTLcwn8	End point: Extrapolated point at VRtt_WR and VRtt_Nom respectively	Figure 103

Table 38 – Reference Settings for ODT Timing Measurements

Measured Parameter	Rtt_Nom Setting	Rtt_WR Setting	VSW1 [V]	VSW2 [V]
t_{AON}	$R_{ZQ}/4$	NA	0.05	0.10
	$R_{ZQ}/12$	NA	0.10	0.20
t_{AONPD}	$R_{ZQ}/4$	NA	0.05	0.10
	$R_{ZQ}/12$	NA	0.10	0.20
t_{AOF}	$R_{ZQ}/4$	NA	0.05	0.10
	$R_{ZQ}/12$	NA	0.10	0.20
t_{AOFPD}	$R_{ZQ}/4$	NA	0.05	0.10
	$R_{ZQ}/12$	NA	0.10	0.20
t_{ADC}	$R_{ZQ}/12$	RZQ/2	0.20	0.30

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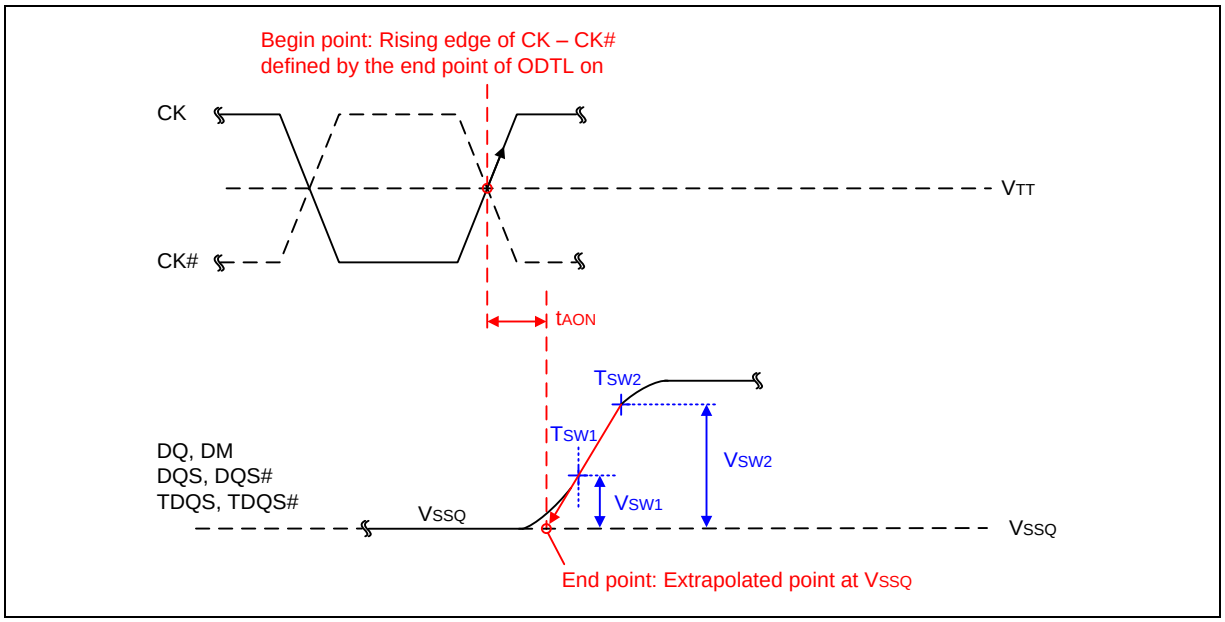


Figure 99 – Definition of tAON

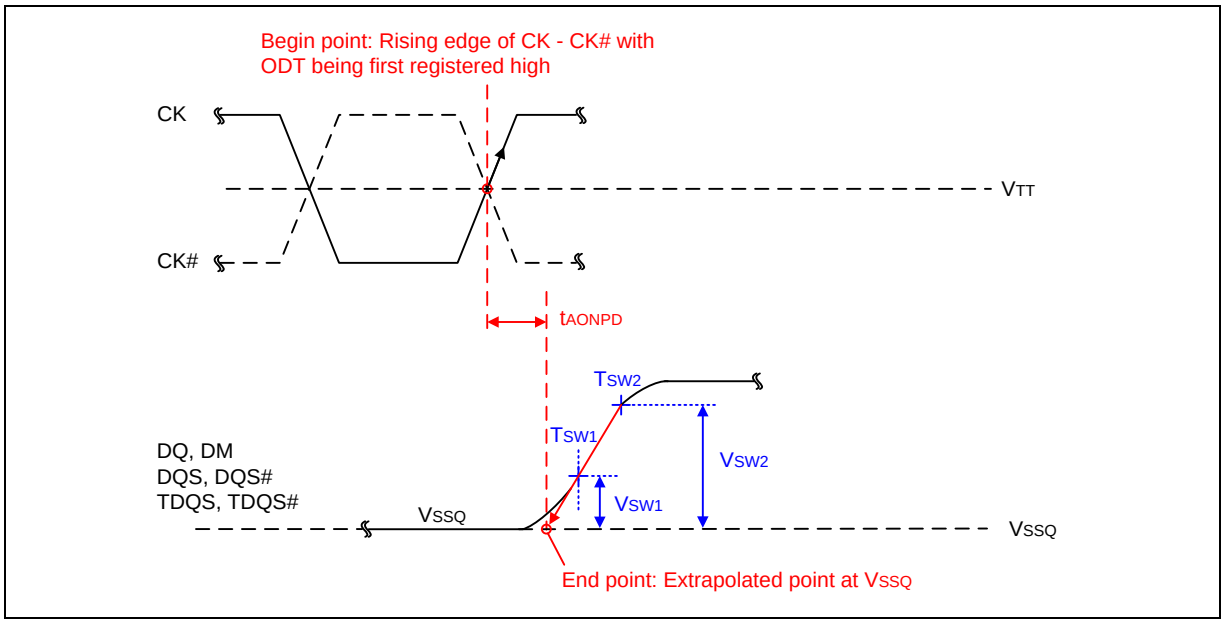


Figure 100 – Definition of tAONPD

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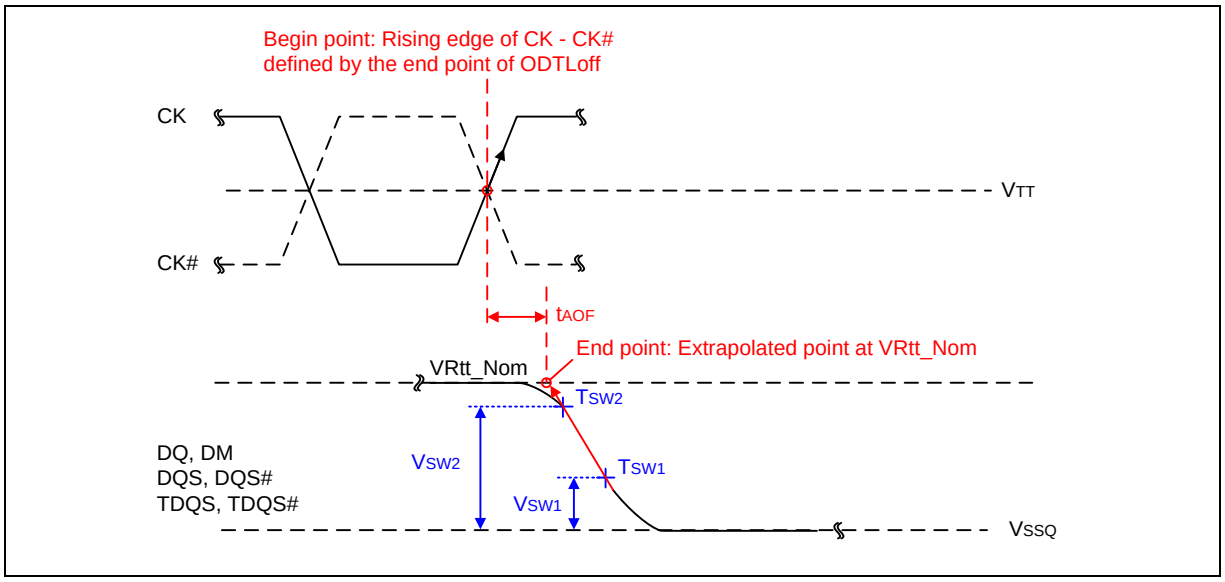


Figure 101 – Definition of t_{AOF}

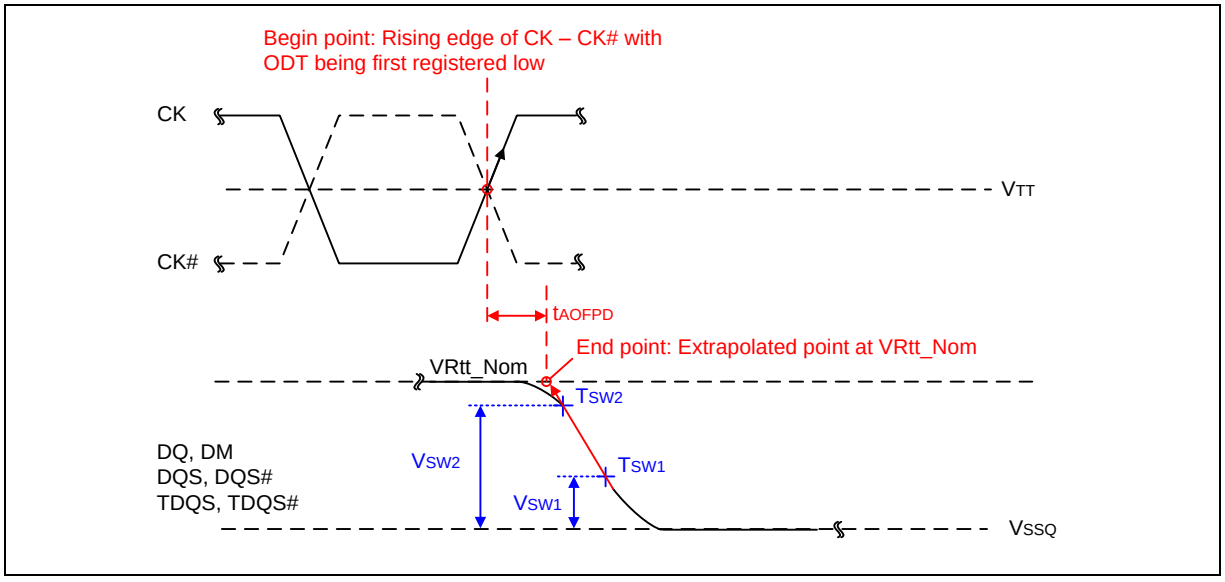


Figure 102 – Definition of t_{AOFPD}

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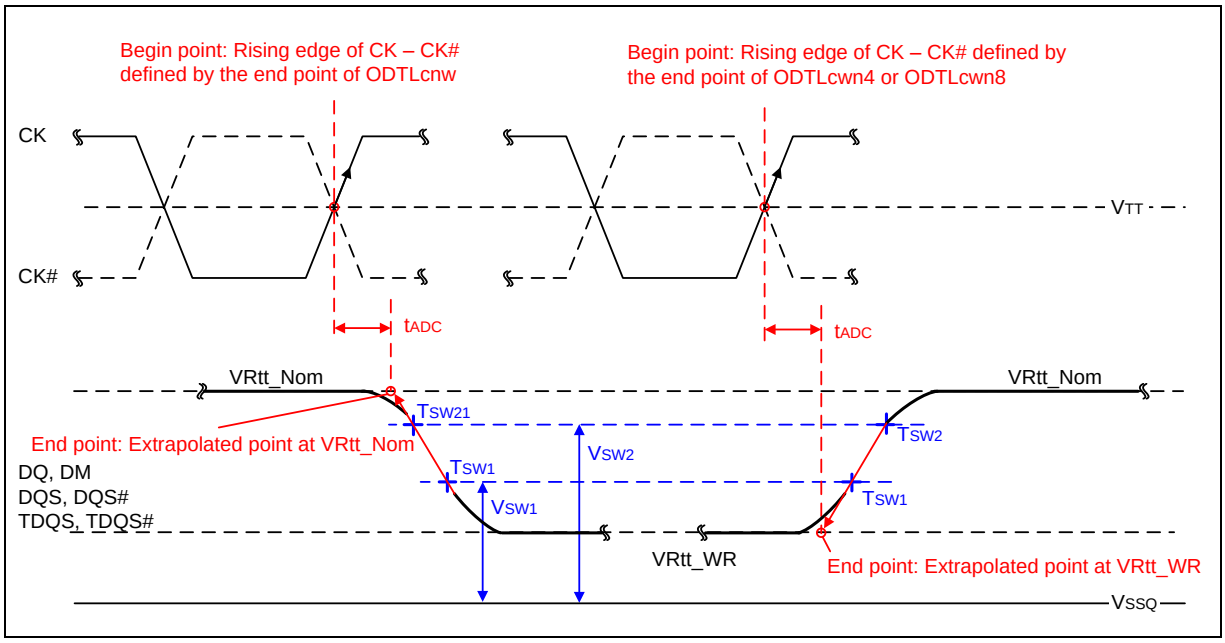


Figure 103 – Definition of t_{ADC}

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10.11 Input/Output Capacitance

PARAMETER	SYMBOL	DDR3-1333		DDR3-1600		DDR3-1866		DDR3-2133		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Input/output capacitance (DQ, DM, DQS, DQS#, TDQS, TDQS#)	C_{IO}	1.4	2.5	1.4	2.3	1.4	2.2	1.4	2.1	pF	1, 2, 3
Input capacitance (CK and CK#)	C_{CK}	0.8	1.4	0.8	1.4	0.8	1.3	0.8	1.3	pF	2, 3
Delta of input capacitance (CK and CK#)	C_{DCK}	0	0.15	0	0.15	0	0.15	0	0.15	pF	2, 3, 4
Delta of Input/Output capacitance (DQS and DQS#)	C_{DDQS}	0	0.15	0	0.15	0	0.15	0	0.15	pF	2, 3, 5
Input capacitance (CTRL, ADD, CMD input-only pins)	C_I	0.75	1.3	0.75	1.3	0.75	1.2	0.75	1.2	pF	2, 3, 6
Delta of input capacitance (All CTRL input-only pins)	C_{DI_CTRL}	-0.4	0.2	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	2, 3, 7, 8
Delta of input capacitance (All ADD/CMD input-only pins)	$C_{DI_ADD_CMD}$	-0.4	0.4	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	2, 3, 9, 10
Delta of Input/output capacitance (DQ, DM, DQS, DQS#, TDQS, TDQS#)	C_{DIO}	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2, 3, 11
Input/output capacitance of ZQ signal	C_{ZQ}	–	3	–	3	–	3	–	3	pF	2, 3, 12

Notes:

1. Although the DM, TDQS and TDQS# pins have different functions, the loading matches DQ and DQS.
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} applied and all other pins floating (except the ball under test, CKE, RESET# and ODT as necessary). $V_{DD}=V_{DDQ}=1.5V$, $V_{BIAS}=V_{DD}/2$ and on-die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
4. Absolute value of C_{CK}-$C_{CK\#}$.
5. Absolute value of $C_{IO(DQS)}$-$C_{IO(DQS\#)}$.
6. C_I applies to ODT, CS#, CKE, A0-A13, BA0-BA2, RAS#, CAS#, WE#.
7. C_{DI_CTRL} applies to ODT, CS# and CKE.
8. $C_{DI_CTRL}=C_I(CTRL)-0.5*(C_I(CLK)+C_I(CLK\#))$.
9. $C_{DI_ADD_CMD}$ applies to A0-A13, BA0-BA2, RAS#, CAS# and WE#.
10. $C_{DI_ADD_CMD}=C_I(ADD_CMD) - 0.5*(C_I(CLK)+C_I(CLK\#))$.
11. $C_{DIO}=C_{IO(DQ,DM)} - 0.5*(C_{IO(DQS)}+C_{IO(DQS\#)})$.
12. Maximum external load capacitance on ZQ signal: 5 pF.

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10.12 Overshoot and Undershoot Specifications

10.12.1 AC Overshoot /Undershoot Specification for Address and Control Pins:

Applies to A0-A13, BA0-BA2, CS#, RAS#, CAS#, WE#, CKE, ODT

PARAMETER	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	UNIT
Maximum peak amplitude allowed for overshoot area	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDD	0.4	0.33	0.28	0.25	V-nS
Maximum undershoot area below VSS	0.4	0.33	0.28	0.25	V-nS

Notes:

1. The sum of applied voltage (VDD) and peak amplitude overshoot voltage is not to exceed absolute maximum DC ratings.
2. The sum of applied voltage (VDD) and peak amplitude undershoot voltage is not to exceed absolute maximum DC ratings.

10.12.2 AC Overshoot /Undershoot Specification for Clock, Data, Strobe and Mask pins:

Applies to CK, CK#, DQ, DQS, DQS#, DM

PARAMETER	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	UNIT
Maximum peak amplitude allowed for overshoot area	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDDQ	0.15	0.13	0.11	0.10	V-nS
Maximum undershoot area below VSSQ	0.15	0.13	0.11	0.10	V-nS

Notes:

1. The sum of applied voltage (VDD) and peak amplitude overshoot voltage is not to exceed absolute maximum DC ratings.
2. The sum of applied voltage (VDD) and peak amplitude undershoot voltage is not to exceed absolute maximum DC ratings.

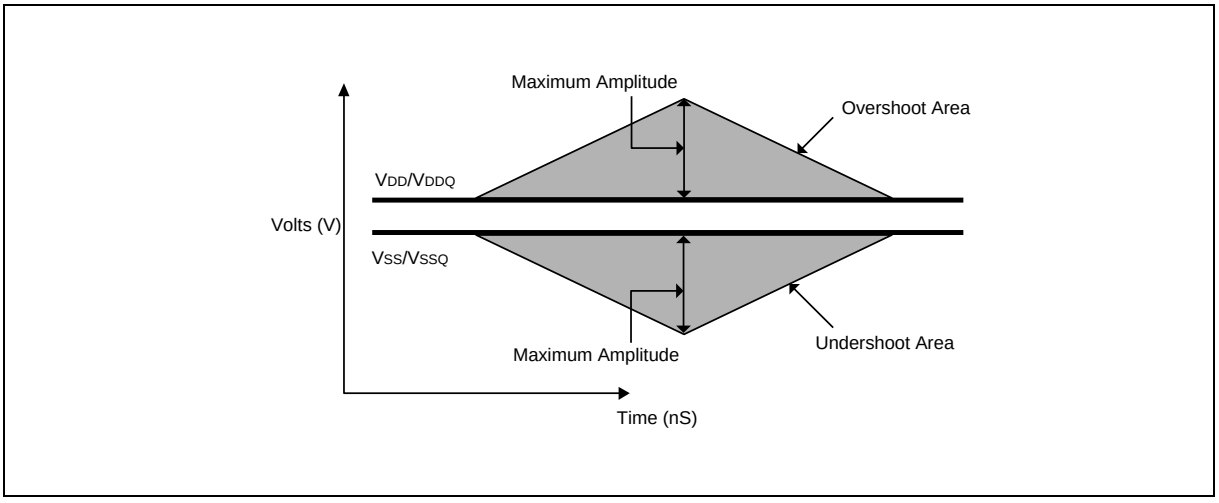


Figure 104 – AC Overshoot and Undershoot Definition

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10.13 IDD and IDDQ Specification Parameters and Test Conditions

10.13.1 IDD and IDDQ Measurement Conditions

In this section, IDD and IDDQ measurement conditions such as test load and patterns are defined. Figure 105 shows the setup and test load for IDD and IDDQ measurements.

- **IDD currents** (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- **IDDQ currents** (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

  Attention: IDDQ values cannot be directly used to calculate IO power of the DDR3 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 106. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply:

- "0" and "LOW" is defined as $V_{IN} \leq V_{ILAC(max)}$.
- "1" and "HIGH" is defined as $V_{IN} \geq V_{IHAC(min)}$.
- "MID-LEVEL" is defined as inputs are $V_{REF} = V_{DD} / 2$.
- Timings used for IDD and IDDQ Measurement-Loop Patterns are provided in Table 39.
- Basic IDD and IDDQ Measurement Conditions are described in Table 40.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 41 through Table 48.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting

  RON = RZQ/7 (34 Ohm in MR1);

  Qoff = 0_b (Output Buffer enabled in MR1);

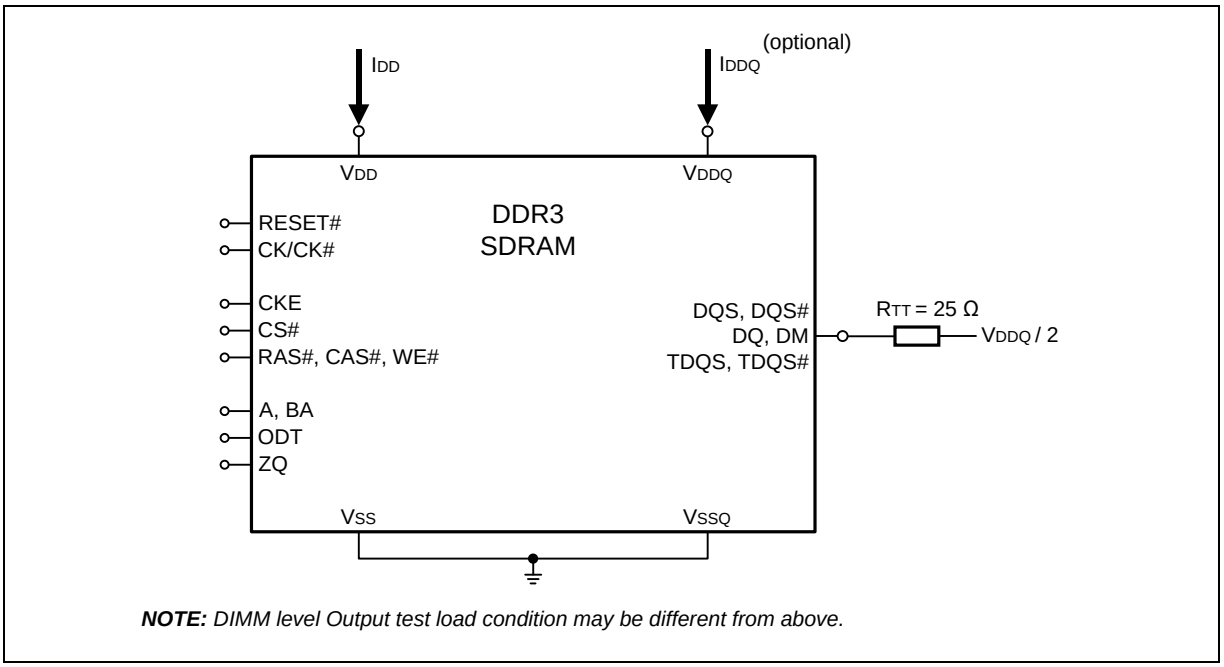
  Rtt_Nom = RZQ/6 (40 Ohm in MR1);

  Rtt_WR = RZQ/2 (120 Ohm in MR2);
- **Attention:** The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {CS#, RAS#, CAS#, WE# } := {HIGH, LOW, LOW, LOW}
- Define D# = {CS#, RAS#, CAS#, WE# } := {HIGH, HIGH, HIGH, HIGH}

Table 39 – Timings used for IDD and IDDQ Measurement-Loop Patterns

Speed Bin	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Unit
CL-nRCD-nRP	9-9-9	11-11-11	13-13-13	14-14-14	
Part Number Extension	-15/15I/15J	-12/12I/12J	-11/11I/11J	-09/09I/09J	
tCK	1.5	1.25	1.07	0.938	nS
CL	9	11	13	14	nCK
nRCD	9	11	13	14	nCK
nRC	33	39	45	50	nCK
nRAS	24	28	32	36	nCK
nRP	9	11	13	14	nCK
nFAW	20	24	26	27	nCK
nRRD	4	5	5	6	nCK
nRFC 1 Gb	74	88	103	118	nCK

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NOTE: *DIMM level Output test load condition may be different from above.*

Figure 105 – Measurement Setup and Test Load for IDD and IDDQ (optional) Measurements

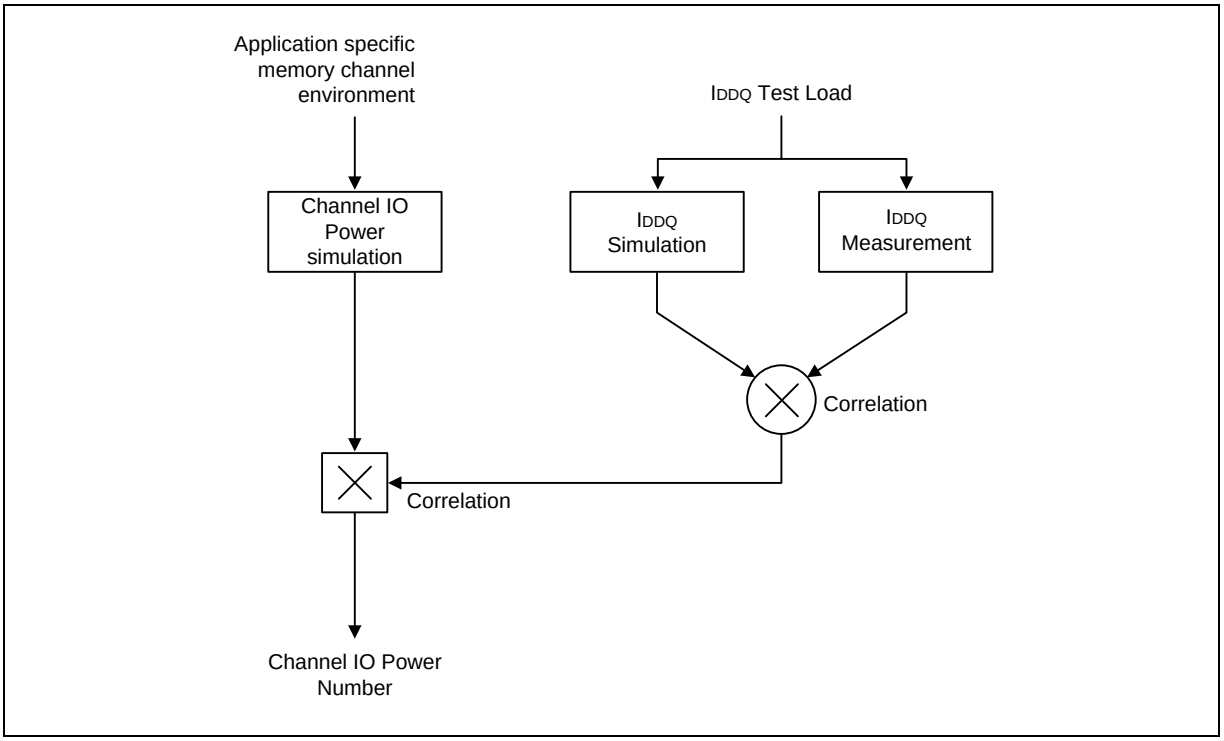


Figure 106 – Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement

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Table 40 – Basic IDD and IDDQ Measurement Conditions

SYM.	DESCRIPTION
IDD0	**Operating One Bank Active-Precharge Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL:** see Table 39; **BL:** 8(1); **AL:** 0; **CS#:** High between ACT and PRE; **Command, Address, Bank Address Inputs:** partially toggling according to Table 41; **Data IO:** MID-LEVEL; **DM:** stable at 0; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 41); **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Pattern Details:** see Table 41
IDD1	**Operating One Bank Active-Read-Precharge Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL:** see Table 39; **BL:** 8(1,6); **AL:** 0; **CS#:** High between ACT, RD and PRE; **Command, Address, Bank Address Inputs, Data IO:** partially toggling according to Table 42; **DM:** stable at 0; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 42); **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Pattern Details:** see Table 42
IDD2N	**Precharge Standby Current** **CKE:** High; **External clock:** On; **tCK, CL:** see Table 39; **BL:** 8(1); **AL:** 0; **CS#:** stable at 1; **Command, Address, Bank Address Inputs:** partially toggling according to Table 43; **Data IO:** MID-LEVEL; **DM:** stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Pattern Details:** see Table 43
IDD2NT	**Precharge Standby ODT Current** **CKE:** High; **External clock:** On; **tCK, CL:** see Table 39; **BL:** 8(1); **AL:** 0; **CS#:** stable at 1; **Command, Address, Bank Address Inputs:** partially toggling according to Table 44; **Data IO:** MID-LEVEL; **DM:** stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** toggling according to Table 44; **Pattern Details:** see Table 44
IDDQ2NT	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2P0	**Precharge Power-Down Current Slow Exit** **CKE:** Low; **External clock:** On; **tCK, CL:** see Table 39; **BL:** 8(1); **AL:** 0; **CS#:** stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM:** stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Precharge Power Down Mode:** Slow Exit(3)
IDD2P1	**Precharge Power-Down Current Fast Exit** **CKE:** Low; **External clock:** On; **tCK, CL:** see Table 39; **BL:** 8(1); **AL:** 0; **CS#:** stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM:** stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Precharge Power Down Mode:** Fast Exit(3)
IDD2Q	**Precharge Quiet Standby Current** **CKE:** High; **External clock:** On; **tCK, CL:** see Table 39; **BL:** 8(1); **AL:** 0; **CS#:** stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM:** stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0
IDD3N	**Active Standby Current** **CKE:** High; **External clock:** On; **tCK, CL:** see Table 39; **BL:** 8(1); **AL:** 0; **CS#:** stable at 1; **Command, Address, Bank Address Inputs:** partially toggling according to Table 43; **Data IO:** MID-LEVEL; **DM:** stable at 0; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Pattern Details:** see Table 43
IDD3P	**Active Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL:** see Table 39; **BL:** 8(1); **AL:** 0; **CS#:** stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM:** stable at 0; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0

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Basic IDD and IDDQ Measurement Conditions, continued

SYM.	DESCRIPTION
IDD4R	**Operating Burst Read Current** **CKE:** High; **External clock:** On; **tCK, CL:** see Table 39; **BL:** 8(1,6); **AL:** 0; **CS#:** High between RD; **Command, Address, Bank Address Inputs:** partially toggling according to Table 45; **Data IO:** seamless read data burst with different data between one burst and the next one according to Table 45; **DM:** stable at 0; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 45); **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Pattern Details:** see Table 45
IDDQ4R	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDD4W	**Operating Burst Write Current** **CKE:** High; **External clock:** On; **tCK, CL:** see Table 39; **BL:** 8(1); **AL:** 0; **CS#:** High between WR; **Command, Address, Bank Address Inputs:** partially toggling according to Table 46; **Data IO:** seamless write data burst with different data between one burst and the next one according to Table 46; **DM:** stable at 0; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 46); **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at HIGH; **Pattern Details:** see Table 46
IDD5B	**Burst Refresh Current** **CKE:** High; **External clock:** On; **tCK, CL, nRFC:** see Table 39; **BL:** 8(1); **AL:** 0; **CS#:** High between REF; **Command, Address, Bank Address Inputs:** partially toggling according to Table 47; **Data IO:** MID-LEVEL; **DM:** stable at 0; **Bank Activity:** REF command every nRFC (see Table 47); **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Pattern Details:** see Table 47
IDD6	**Self Refresh Current: Normal Temperature Range** **Auto Self-Refresh (ASR):** Disabled(4); **Self-Refresh Temperature Range (SRT):** Normal(5); **CKE:** Low; **External clock:** Off; **CK and CK#:** LOW; **CL:** see Table 39; **BL:** 8(1); **AL:** 0; **CS#, Command, Address, Bank Address, Data IO:** MID-LEVEL; **DM:** stable at 0; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** MID-LEVEL
IDD6ET	**Self-Refresh Current: Extended Temperature Range** **Auto Self-Refresh (ASR):** Disabled(4); **Self-Refresh Temperature Range (SRT):** Extended(5); **CKE:** Low; **External clock:** Off; **CK and CK#:** LOW; **CL:** see Table 39; **BL:** 8(1); **AL:** 0; **CS#, Command, Address, Bank Address, Data IO:** MID-LEVEL; **DM:** stable at 0; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** MID-LEVEL
IDD7	**Operating Bank Interleave Read Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL:** see Table 39; **BL:** 8(1,6); **AL:** CL-1; **CS#:** High between ACT and RDA; **Command, Address, Bank Address Inputs:** partially toggling according to Table 48; **Data IO:** read data bursts with different data between one burst and the next one according to Table 48; **DM:** stable at 0; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 48; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Pattern Details:** see Table 48
IDD8	**RESET# Low Current** **RESET#:** Low; **External clock:** Off; **CK and CK#:** Low; **CKE:** FLOATING; **CS#, Command, Address, Bank Address, Data IO:** FLOATING; **ODT Signal:** FLOATING RESET# Low current reading is valid once power is stable and RESET has been Low for at least 1mS

Notes:

1. Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00b.
2. Output Buffer Enable: set MR1 A[12] = 0b; set MR1 A[5,1] = 01b; Rtt_Nom enable: set MR1 A[9,6,2] = 011b; Rtt_WR enable: set MR2 A[10,9] = 10b.
3. Precharge Power Down Mode: set MR0 A12=0b for Slow Exit or MR0 A12=1b for Fast Exit.
4. Auto Self-Refresh (ASR): set MR2 A6 = 0b to disable or 1b to enable feature.
5. Self-Refresh Temperature Range (SRT): set MR2 A7=0b for normal or 1b for extended temperature range.
6. Read Burst Type: Nibble Sequential, set MR0 A[3] = 0b.

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Table 41 – IDD0 Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[13:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	**ACT**	0	0	1	1	0	**0**	0	0	0	**0**	0	-
			1, 2	D, D	1	0	0	0	0	**0**	0	0	0	**0**	0	-
			3, 4	D#, D#	1	1	1	1	0	**0**	0	0	0	**0**	0	-
			...	Repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	**PRE**	0	0	1	0	0	0	0	0	0	**0**	0	-
			...	Repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	**ACT**	0	0	1	1	0	**0**	0	0	0	**F**	0	-
			1*nRC+1, 2	D, D	1	0	0	0	0	**0**	0	0	0	**F**	0	-
			1*nRC+3, 4	D#, D#	1	1	1	1	0	**0**	0	0	0	**F**	0	-
			...	Repeat pattern nRC + 1,...,4 until nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	**PRE**	0	0	1	0	0	0	0	0	0	**F**	0	-
			...	Repeat pattern nRC + 1,...,4 until 2*nRC - 1, truncate if necessary												
		1	2*nRC	Repeat Sub-Loop 0, use **BA[2:0] = 1** instead												
		2	4*nRC	Repeat Sub-Loop 0, use **BA[2:0] = 2** instead												
		3	6*nRC	Repeat Sub-Loop 0, use **BA[2:0] = 3** instead												
		4	8*nRC	Repeat Sub-Loop 0, use **BA[2:0] = 4** instead												
		5	10*nRC	Repeat Sub-Loop 0, use **BA[2:0] = 5** instead												
		6	12*nRC	Repeat Sub-Loop 0, use **BA[2:0] = 6** instead												
		7	14*nRC	Repeat Sub-Loop 0, use **BA[2:0] = 7** instead												

Notes:

1. DM must be driven LOW all the time. DQS, DQS# are MID-LEVEL.
2. DQ signals are MID-LEVEL.

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Table 42 – IDD1 Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[13:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	**ACT**	0	0	1	1	0	**0**	0	0	0	**0**	0	-
			1, 2	D, D	1	0	0	0	0	**0**	0	0	0	**0**	0	-
			3, 4	D#, D#	1	1	1	1	0	**0**	0	0	0	**0**	0	-
			...	Repeat pattern 1...4 until nRCD - 1, truncate if necessary												
			nRCD	**RD**	0	1	0	1	0	**0**	0	0	0	**0**	0	**00000000**
			...	Repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	**PRE**	0	0	1	0	0	0	0	0	0	**0**	0	-
			...	Repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	**ACT**	0	0	1	1	0	**0**	0	0	0	**F**	0	-
			1*nRC+1, 2	D, D	1	0	0	0	0	**0**	0	0	0	**F**	0	-
			1*nRC+3, 4	D#, D#	1	1	1	1	0	**0**	0	0	0	**F**	0	-
			...	Repeat pattern nRC + 1,...,4 until nRC + nRCD - 1, truncate if necessary												
			1*nRC+nRCD	**RD**	0	1	0	1	0	**0**	0	0	0	**F**	0	**00110011**
			...	Repeat pattern nRC + 1,...,4 until nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	**PRE**	0	0	1	0	0	**0**	0	0	0	**F**	0	-
			...	Repeat pattern nRC + 1,...,4 until 2*nRC - 1, truncate if necessary												
		1	2*nRC	Repeat Sub-Loop 0, use **BA[2:0] = 1** instead												
		2	4*nRC	Repeat Sub-Loop 0, use **BA[2:0] = 2** instead												
		3	6*nRC	Repeat Sub-Loop 0, use **BA[2:0] = 3** instead												
		4	8*nRC	Repeat Sub-Loop 0, use **BA[2:0] = 4** instead												
		5	10*nRC	Repeat Sub-Loop 0, use **BA[2:0] = 5** instead												
		6	12*nRC	Repeat Sub-Loop 0, use **BA[2:0] = 6** instead												
		7	14*nRC	Repeat Sub-Loop 0, use **BA[2:0] = 7** instead												

Notes:

1. DM must be driven LOW all the time. DQS, DQS# are used according to RD Commands, otherwise MID-LEVEL.
2. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

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Table 43 – IDD2N and IDD3N Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[13:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	D	1	0	0	0	0	**0**	0	0	0	**0**	0	-
			1	D	1	0	0	0	0	**0**	0	0	0	**0**	0	-
			2	D#	1	1	1	1	0	**0**	0	0	0	**F**	0	-
			3	D#	1	1	1	1	0	**0**	0	0	0	**F**	0	-
		1	4-7	Repeat Sub-Loop 0, use **BA[2:0] = 1** instead												
		2	8-11	Repeat Sub-Loop 0, use **BA[2:0] = 2** instead												
		3	12-15	Repeat Sub-Loop 0, use **BA[2:0] = 3** instead												
		4	16-19	Repeat Sub-Loop 0, use **BA[2:0] = 4** instead												
		5	20-23	Repeat Sub-Loop 0, use **BA[2:0] = 5** instead												
		6	24-27	Repeat Sub-Loop 0, use **BA[2:0] = 6** instead												
		7	28-31	Repeat Sub-Loop 0, use **BA[2:0] = 7** instead												

Notes:

1. DM must be driven LOW all the time. DQS, DQS# are MID-LEVEL.
2. DQ signals are MID-LEVEL.

Table 44 – IDD2NT and IDDQ2NT Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[13:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	D	1	0	0	0	0	**0**	0	0	0	**0**	0	-
			1	D	1	0	0	0	0	**0**	0	0	0	**0**	0	-
			2	D#	1	1	1	1	0	**0**	0	0	0	**F**	0	-
			3	D#	1	1	1	1	0	**0**	0	0	0	**F**	0	-
		1	4-7	Repeat Sub-Loop 0, but **ODT = 0 and BA[2:0] = 1**												
		2	8-11	Repeat Sub-Loop 0, but **ODT = 1 and BA[2:0] = 2**												
		3	12-15	Repeat Sub-Loop 0, but **ODT = 1 and BA[2:0] = 3**												
		4	16-19	Repeat Sub-Loop 0, but **ODT = 0 and BA[2:0] = 4**												
		5	20-23	Repeat Sub-Loop 0, but **ODT = 0 and BA[2:0] = 5**												
		6	24-27	Repeat Sub-Loop 0, but **ODT = 1 and BA[2:0] = 6**												
		7	28-31	Repeat Sub-Loop 0, but **ODT = 1 and BA[2:0] = 7**												

Notes:

1. DM must be driven LOW all the time. DQS, DQS# are MID-LEVEL.
2. DQ signals are MID-LEVEL.

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Table 45 – IDD4R and IDDQ4R Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[13:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2, 3	D#, D#	1	1	1	1	0	0	0	0	0	0	0	-
			4	RD	0	1	0	1	0	0	0	0	0	F	0	**00110011**
			5	D	1	0	0	0	0	0	0	0	0	F	0	-
			6, 7	D#, D#	1	1	1	1	0	0	0	0	0	F	0	-
		1	8-15	Repeat Sub-Loop 0, but **BA[2:0] = 1**												
		2	16-23	Repeat Sub-Loop 0, but **BA[2:0] = 2**												
		3	24-31	Repeat Sub-Loop 0, but **BA[2:0] = 3**												
		4	32-39	Repeat Sub-Loop 0, but **BA[2:0] = 4**												
		5	40-47	Repeat Sub-Loop 0, but **BA[2:0] = 5**												
		6	48-55	Repeat Sub-Loop 0, but **BA[2:0] = 6**												
		7	56-63	Repeat Sub-Loop 0, but **BA[2:0] = 7**												

Notes:

1. DM must be driven LOW all the time. DQS, DQS# are used according to RD Commands, otherwise MID-LEVEL.
2. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

Table 46 – IDD4W Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[13:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	WR	0	1	0	0	1	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	0	0	0	0	0	-
			2, 3	D#, D#	1	1	1	1	1	0	0	0	0	0	0	-
			4	WR	0	1	0	0	1	0	0	0	0	F	0	**00110011**
			5	D	1	0	0	0	1	0	0	0	0	F	0	-
			6, 7	D#, D#	1	1	1	1	1	0	0	0	0	F	0	-
		1	8-15	Repeat Sub-Loop 0, but **BA[2:0] = 1**												
		2	16-23	Repeat Sub-Loop 0, but **BA[2:0] = 2**												
		3	24-31	Repeat Sub-Loop 0, but **BA[2:0] = 3**												
		4	32-39	Repeat Sub-Loop 0, but **BA[2:0] = 4**												
		5	40-47	Repeat Sub-Loop 0, but **BA[2:0] = 5**												
		6	48-55	Repeat Sub-Loop 0, but **BA[2:0] = 6**												
		7	56-63	Repeat Sub-Loop 0, but **BA[2:0] = 7**												

Notes:

1. DM must be driven LOW all the time. DQS, DQS# are used according to WR Commands, otherwise MID-LEVEL.
2. Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are MID-LEVEL.

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Table 47 – IDD5B Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[13:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	**REF**	0	0	0	1	0	0	0	0	0	0	0	-
		1	1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	-
			3, 4	D#, D#	1	1	1	1	0	0	0	0	0	F	0	-
			5...8	Repeat cycles 1...4, but **BA[2:0] = 1**												
			9...12	Repeat cycles 1...4, but **BA[2:0] = 2**												
			13...16	Repeat cycles 1...4, but **BA[2:0] = 3**												
			17...20	Repeat cycles 1...4, but **BA[2:0] = 4**												
			21...24	Repeat cycles 1...4, but **BA[2:0] = 5**												
			25...28	Repeat cycles 1...4, but **BA[2:0] = 6**												
			29...32	Repeat cycles 1...4, but **BA[2:0] = 7**												
		2	33...nRFC - 1	**Repeat Sub-Loop 1, until nRFC - 1**. Truncate, if necessary												

Notes:

1. DM must be driven LOW all the time. DQS, DQS# are MID-LEVEL.
2. DQ signals are MID-LEVEL.

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Table 48 – IDD7 Measurement-Loop Pattern[1]

ATTENTION: Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[13:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	0	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	0	0	0	0	0	-
			...	Repeat above D Command until nRRD - 1												
		1	nRRD	ACT	0	0	1	1	0	1	0	0	0	F	0	-
			nRRD+1	RDA	0	1	0	1	0	1	0	1	0	F	0	**00110011**
			nRRD+2	D	1	0	0	0	0	1	0	0	0	F	0	-
			...	Repeat above D Command until 2 * nRRD -1												
		2	2*nRRD	Repeat Sub-Loop 0, but **BA[2:0] = 2**												
		3	3*nRRD	Repeat Sub-Loop 1, but **BA[2:0] = 3**												
		4	4*nRRD	D	1	0	0	0	0	3	0	0	0	F	0	-
				Assert and repeat above D Command until nFAW - 1, if necessary												
		5	nFAW	Repeat Sub-Loop 0, but **BA[2:0] = 4**												
		6	nFAW+nRRD	Repeat Sub-Loop 1, but **BA[2:0] = 5**												
		7	nFAW+2*nRRD	Repeat Sub-Loop 0, but **BA[2:0] = 6**												
		8	nFAW+3*nRRD	Repeat Sub-Loop 1, but **BA[2:0] = 7**												
		9	nFAW+4*nRRD	D	1	0	0	0	0	7	0	0	0	F	0	-
				Assert and repeat above D Command until 2 * nFAW - 1, if necessary												
		10	2*nFAW+0	ACT	0	0	1	1	0	0	0	0	0	F	0	-
			2*nFAW+1	RDA	0	1	0	1	0	0	0	1	0	F	0	**00110011**
			2*nFAW+2	D	1	0	0	0	0	0	0	0	0	F	0	-
				Repeat above D Command until 2 * nFAW + nRRD - 1												
		11	2*nFAW+nRRD	ACT	0	0	1	1	0	1	0	0	0	0	0	-
			2*nFAW+nRRD+1	RDA	0	1	0	1	0	1	0	1	0	0	0	00000000
			2*nFAW+nRRD+2	D	1	0	0	0	0	1	0	0	0	0	0	-
				Repeat above D Command until 2 * nFAW + 2 * nRRD -1												
		12	2*nFAW+2*nRRD	Repeat Sub-Loop 10, but **BA[2:0] = 2**												
		13	2*nFAW+3*nRRD	Repeat Sub-Loop 11, but **BA[2:0] = 3**												
		14	2*nFAW+4*nRRD	D	1	0	0	0	0	3	0	0	0	0	0	-
				Assert and repeat above D Command until 3 * nFAW - 1, if necessary												
		15	3*nFAW	Repeat Sub-Loop 10, but **BA[2:0] = 4**												
		16	3*nFAW+nRRD	Repeat Sub-Loop 11, but **BA[2:0] = 5**												
		17	3*nFAW+2*nRRD	Repeat Sub-Loop 10, but **BA[2:0] = 6**												
		18	3*nFAW+3*nRRD	Repeat Sub-Loop 11, but **BA[2:0] = 7**												
		19	3*nFAW+4*nRRD	D	1	0	0	0	0	7	0	0	0	0	0	-
				Assert and repeat above D Command until 4 * nFAW - 1, if necessary												

Notes:

1. DM must be driven LOW all the time. DQS, DQS# are used according to RD Commands, otherwise MID-LEVEL.
2. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

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10.13.2 IDD Current Specifications

SYM.	Speed Bin	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	UNIT
	Part Number Extension	-15/15I/15J	-12/12I/12J	-11/11I/11J	-09/09I/09J	
	DEFINITION	MAX.	MAX.	MAX.	MAX.	
IDD0	Operating One Bank Active-Precharge Current	95	105	115	130	mA
IDD1	Operating One Bank Active-Read-Precharge Current	115	130	140	160	mA
IDD2N	Precharge Standby Current	70	75	80	90	mA
IDD2NT	Precharge Standby ODT Current	65	80	90	100	mA
IDD2P0	Precharge Power Down Current Slow Exit	14	14	14	14	mA
IDD2P1	Precharge Power Down Current Fast Exit	40	45	50	55	mA
IDD2Q	Precharge Quiet Standby Current	70	75	80	90	mA
IDD3N	Active Standby Current	75	85	95	100	mA
IDD3P	Active Power Down Current	50	55	55	60	mA
IDD4R	Operating Burst Read Current	120	140	150	170	mA
IDD4W	Operating Burst Write Current	130	150	170	190	mA
IDD5B	Burst Refresh Current	140	150	160	170	mA
IDD6*3	Normal Temperature Self-Refresh Current	10	10	10	10	mA
IDD6ET*4	Extended Temperature Self-Refresh Current	12	12	12	12	mA
IDD7	Operating Bank Interleave Read Current	175	195	215	245	mA
IDD8	RESET# Low Current	8	8	8	8	mA

Notes:

1. Max. values for IDD currents consider worst case conditions of process, temperature and voltage.
2. The IDD values must be derated (increased) when operated outside the range 0°C ≤ TCASE ≤ 85°C:
   (a) When TCASE < 0°C: IDD2P0, IDD2P1 and IDD3P must be derated by 4%; IDD4R and IDD5W must be derated by 2%; and IDD6, IDD6ET and IDD7 must be derated by 7%.
   (b) When TCASE > 85°C: IDD0, IDD1, IDD2N, IDD2NT, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, and IDD5B must be derated by 2%; and IDD2P0, IDD2P1 must be derated by 30%.
3. Set MR2 A[6] = 0b, Auto Self-Refresh (ASR) disable; Set MR2 A[7] = 0b, Self-Refresh Temperature Range (SRT) disable for normal temperature range.
4. Set MR2 A[6] = 0b, ASR disable; Set MR2 A[7] = 1b, SRT enable for extended temperature range.

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10.14 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR3 SDRAM device.

Definition for tCK(avg)

$t_{CK(avg)}$ is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left[\sum_{j=1}^{N} tCK_j\right] / N$$

$$where \qquad N = 200$$

Definition for tCK(abs)

$t_{CK(abs)}$ is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. $t_{CK(abs)}$ is not subject to production test.

Definition for tCH(avg) and tCL(avg)

$t_{CH(avg)}$ is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left[\sum_{j=1}^{N} tCH_j\right] / (N \times tCK(avg))$$

$$where \qquad N = 200$$

$t_{CL(avg)}$ is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left[\sum_{j=1}^{N} tCL_j\right] / (N \times tCK(avg))$$

$$where \qquad N = 200$$

Definition for tJIT(per) and tJIT(per,lck)

$t_{JIT(per)}$ is defined as the largest deviation of any signal t_{CK} from $t_{CK(avg)}$.

$t_{JIT(per)}$ = Min/max of {$t_{CK}i$ - $t_{CK(avg)}$ where i = 1 to 200}.

$t_{JIT(per)}$ defines the single period jitter when the DLL is already locked.

$t_{JIT(per,lck)}$ uses the same definition for single period jitter, during the DLL locking period only.

$t_{JIT(per)}$ and $t_{JIT(per,lck)}$ are not subject to production test.

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Definition for tJIT(cc) and tJIT(cc,lck)

$t_{JIT(cc)}$ is defined as the absolute difference in clock period between two consecutive clock cycles.

$t_{JIT(cc)}$ = Max of $|\{t_{CK_{i+1}} - t_{CK_i}\}|$.

$t_{JIT(cc)}$ defines the cycle to cycle jitter when the DLL is already locked.

$t_{JIT(cc,lck)}$ uses the same definition for cycle to cycle jitter, during the DLL locking period only.

$t_{JIT(cc)}$ and $t_{JIT(cc,lck)}$ are not subject to production test.

Definition for tERR(nper)

t_{ERR} is defined as the cumulative error across n multiple consecutive cycles from $t_{CK(avg)}$. t_{ERR} is not subject to production test.

10.15 Speed Bins

DDR3 SDRAM Speed Bins include t_{CK}, t_{RCD}, t_{RP}, t_{RC} and t_{RAS} for each corresponding bin.

10.15.1 DDR3-1333 Speed Bin and Operating Conditions

Speed Bin			DDR3-1333		UNIT	NOTES
CL-nRCD-nRP			9-9-9			
Part Number Extension			-15/15I/15J			
Parameter		Symbol	Min.	Max.		
Maximum operating frequency using maximum allowed settings for Sup_CL and Sup_CWL		f_{CKMAX}	–	667	MHz	
Internal read command to first data		t_{AA}	13.5 (13.125)*10	20	nS	
ACT to internal read or write delay time		t_{RCD}	13.5 (13.125)*10	–	nS	
PRE command period		t_{RP}	13.5 (13.125)*10	–	nS	
ACT to ACT or REF command period		t_{RC}	49.5 (49.125)*10	–	nS	
ACT to PRE command period		t_{RAS}	36	9 * t_{REFI}	nS	
CL = 5	CWL = 5	$t_{CK(AVG)}$	3.0	3.3	nS	1, 2, 3, 4, 6
	CWL = 6, 7	$t_{CK(AVG)}$	Reserved		nS	5
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	nS	1, 2, 3, 4, 6
	CWL = 6, 7	$t_{CK(AVG)}$	Reserved		nS	5
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		nS	5
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	nS	1, 2, 3, 4, 6
			(Optional)*10		nS	
	CWL = 7	$t_{CK(AVG)}$	Reserved		nS	5
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		nS	5
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	nS	1, 2, 3, 4, 6
	CWL = 7	$t_{CK(AVG)}$	Reserved		nS	5
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		nS	5
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	nS	1, 2, 3, 4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		nS	5
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	nS	1, 2, 3, 4
Supported CL Settings		Sup_CL	5, 6, (7), 8, 9, 10		nCK	
Supported CWL Settings		Sup_CWL	5, 6, 7		nCK	

Note:

Field value contents in blue font or parentheses are optional AC parameter and CL setting. Detail descriptions refer to note 10.

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10.15.2 DDR3-1600 Speed Bin and Operating Conditions

Speed Bin			DDR3-1600		UNIT	NOTES
CL-nRCD-nRP			11-11-11			
Part Number Extension			-12/12I/12J			
Parameter		Symbol	Min.	Max.		
Maximum operating frequency using maximum allowed settings for Sup_CL and Sup_CWL		f_{CKMAX}	–	800	MHz	
Internal read command to first data		t_{AA}	13.75 (13.125)*10	20	nS	
ACT to internal read or write delay time		t_{RCD}	13.75 (13.125)*10	–	nS	
PRE command period		t_{RP}	13.75 (13.125)*10	–	nS	
ACT to ACT or REF command period		t_{RC}	48.75 (48.125)*10	–	nS	
ACT to PRE command period		t_{RAS}	35	9 * t_{REFI}	nS	
CL = 5	CWL = 5	$t_{CK(AVG)}$	3.0	3.3	nS	1, 2, 3, 4, 7
	CWL = 6, 7, 8	$t_{CK(AVG)}$	Reserved		nS	5
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	nS	1, 2, 3, 4, 7
	CWL = 6, 7, 8	$t_{CK(AVG)}$	Reserved		nS	5
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		nS	5
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	nS	1, 2, 3, 4, 7
			(Optional)*10		nS	5
	CWL = 7, 8	$t_{CK(AVG)}$	Reserved		nS	5
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		nS	5
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	nS	1, 2, 3, 4, 7
	CWL = 7, 8	$t_{CK(AVG)}$	Reserved		nS	5
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		nS	5
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	nS	5
			(Optional)*10		nS	1, 2, 3, 4, 7
	CWL = 8	$t_{CK(AVG)}$	Reserved		nS	5
CL =10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		nS	5
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	nS	1, 2, 3, 4, 7
	CWL = 8	$t_{CK(AVG)}$	Reserved		nS	5
CL =11	CWL = 5, 6, 7	$t_{CK(AVG)}$	Reserved		nS	5
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	nS	1, 2, 3, 4
Supported CL Settings		Sup_CL	5, 6, (7), 8, (9), 10, 11		nCK	
Supported CWL Settings		Sup_CWL	5, 6, 7, 8		nCK	

Note:
Field value contents in blue font or parentheses are optional AC parameter and CL setting. Detail descriptions refer to note 10.

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10.15.3 DDR3-1866 Speed Bin and Operating Conditions

Speed Bin			DDR3-1866		UNIT	NOTES
CL-nRCD-nRP			13-13-13			
Part Number Extension			-11/11I/11J			
Parameter		Symbol	Min.	Max.		
Maximum operating frequency using maximum allowed settings for Sup_CL and Sup_CWL		f_{CKMAX}	–	933	MHz	
Internal read command to first data		t_{AA}	13.91	20	nS	
ACT to internal read or write delay time		t_{RCD}	13.91	–	nS	
PRE command period		t_{RP}	13.91	–	nS	
ACT to ACT or REF command period		t_{RC}	47.91	–	nS	
ACT to PRE command period		t_{RAS}	34	9 * t_{REFI}	nS	
CL = 5	CWL = 5	$t_{CK(AVG)}$	3.0	3.3	nS	1, 2, 3, 4, 8
	CWL = 6, 7, 8, 9	$t_{CK(AVG)}$	Reserved		nS	5
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	nS	1, 2, 3, 4, 8
	CWL = 6, 7, 8, 9	$t_{CK(AVG)}$	Reserved		nS	5
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		nS	5
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	nS	1, 2, 3, 4, 8
	CWL = 7, 8, 9	$t_{CK(AVG)}$	Reserved		nS	5
CL =10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		nS	5
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	nS	1, 2, 3, 4, 8
	CWL = 8, 9	$t_{CK(AVG)}$	Reserved		nS	5
CL =13	CWL = 5, 6, 7, 8	$t_{CK(AVG)}$	Reserved		nS	5
	CWL = 9	$t_{CK(AVG)}$	1.07	< 1.25	nS	1, 2, 3, 4
Supported CL Settings		Sup_CL	5, 6, 8, 10, 13		nCK	
Supported CWL Settings		Sup_CWL	5, 6, 7, 9		nCK	

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10.15.4 DDR3-2133 Speed Bin and Operating Conditions

Speed Bin			DDR3-2133		UNIT	NOTES
CL-nRCD-nRP			14-14-14			
Part Number Extension			-09/09I/09J			
Parameter		Symbol	Min.	Max.		
Maximum operating frequency using maximum allowed settings for Sup_CL and Sup_CWL		f_{CKMAX}	–	1067	MHz	
Internal read command to first data		t_{AA}	13.09	20	nS	
ACT to internal read or write delay time		t_{RCD}	13.09	-	nS	
PRE command period		t_{RP}	13.09	-	nS	
ACT to ACT or REF command period		t_{RC}	46.09	-	nS	
ACT to PRE command period		t_{RAS}	33	9 * t_{REFI}	nS	
CL = 5	CWL = 5	$t_{CK(AVG)}$	3.0	3.3	nS	1, 2, 3, 4, 9
	CWL = 6, 7, 8, 9, 10	$t_{CK(AVG)}$	Reserved		nS	5
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	nS	1, 2, 3, 4, 9
	CWL = 6, 7, 8, 9, 10	$t_{CK(AVG)}$	Reserved		nS	5
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		nS	5
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	nS	1, 2, 3, 4, 9
	CWL = 7, 8, 9, 10	$t_{CK(AVG)}$	Reserved		nS	5
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		nS	5
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	nS	1, 2, 3, 4, 9
	CWL = 7, 8, 9, 10	$t_{CK(AVG)}$	Reserved		nS	5
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		nS	5
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	nS	1, 2, 3, 4, 9
	CWL = 8, 9, 10	$t_{CK(AVG)}$	Reserved		nS	5
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		nS	5
	CWL = 7	$t_{CK(AVG)}$	1.5	< 1.875	nS	1, 2, 3, 4, 9
	CWL = 8, 9, 10	$t_{CK(AVG)}$	Reserved		nS	5
CL = 11	CWL = 5, 6, 7	$t_{CK(AVG)}$	Reserved		nS	5
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	nS	1, 2, 3, 4, 9
	CWL = 9, 10	$t_{CK(AVG)}$	Reserved		nS	5
CL = 13	CWL = 5, 6, 7, 8	$t_{CK(AVG)}$	Reserved		nS	5
	CWL = 9	$t_{CK(AVG)}$	1.07	< 1.25	nS	1, 2, 3, 4, 9
	CWL = 10	$t_{CK(AVG)}$	Reserved		nS	5
CL = 14	CWL = 5, 6, 7, 8, 9	$t_{CK(AVG)}$	Reserved		nS	5
	CWL = 10	$t_{CK(AVG)}$	0.938	< 1.07	nS	1, 2, 3, 4
Supported CL Settings		Sup_CL	5, 6, 7, 8, 9, 10, 11, 13, 14		nCK	
Supported CWL Settings		Sup_CWL	5, 6, 7, 8, 9, 10		nCK	

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10.15.5 Speed Bin General Notes

The absolute specification for all speed bins is T_{OPER} and V_{DD} = V_{DDQ} = 1.5V ± 0.075V. In addition the following general notes apply.

1. Max. limits are exclusive. E.g. if $t_{CK(AVG).MAX}$ value is 2.5 nS, $t_{CK(AVG)}$ needs to be < 2.5 nS.
2. The CL setting and CWL setting result in $t_{CK(AVG).MIN}$ and $t_{CK(AVG).MAX}$ requirements. When making a selection of $t_{CK(AVG)}$, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
3. $t_{CK(AVG).MIN}$ limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller standard $t_{CK(AVG)}$ value (2.5, 1.875, 1.5, 1.25, 1.07, or 0.938 nS) when calculating CL [nCK] = t_{AA} [nS] / $t_{CK(AVG)}$ [nS], rounding up to the next 'Supported CL'.
4. $t_{CK(AVG).MAX}$ limits: Calculate $t_{CK(AVG)}$ = $t_{AA.MAX}$ / CL SELECTED and round the resulting $t_{CK(AVG)}$ down to the next valid speed bin (i.e. 3.3nS or 2.5nS or 1.875 nS or 1.25 nS or 1.07 nS). This result is $t_{CK(AVG).MAX}$ corresponding to CL SELECTED.
5. 'Reserved' settings are not allowed. User must program a different value.
6. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR3-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization
10. For devices supporting optional down binning to CL=7 and CL=9, t_{AA}/t_{RCD}/t_{RP} min must be 13.125 nS or lower. SPD settings must be programmed to match. For example, DDR3-1333 (9-9-9) devices supporting down binning to DDR3-1066 (7-7-7) should program 13.125 nS in SPD bytes for t_{AA}min (Byte 16), t_{RCD}min (Byte 18), and t_{RP}min (Byte 20). DDR3-1600 (11-11-11) devices supporting down binning to DDR3-1333 (9-9-9) or DDR3-1066 (7-7-7) should program 13.125 nS in SPD bytes for t_{AA}min (Byte16), t_{RCD}min (Byte 18), and t_{RP}min (Byte 20). Once t_{RP} (Byte 20) is programmed to 13.125 nS, t_{RC}min (Byte 21, 23) also should be programmed accordingly. For example, 49.125nS (t_{RAS}min + t_{RP}min = 36 nS + 13.125 nS) for DDR3-1333 (9-9-9) and 48.125 nS (t_{RAS}min + t_{RP}min = 35 nS + 13.125 nS) for DDR3-1600 (11-11-11).

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10.16 AC Characteristics

10.16.1 AC Timing and Operating Condition for -09/09I/09J/-11/11I/11J speed grades

SYMBOL	SPEED GRADE	DDR3-2133 (-09/09I/09J)		DDR3-1866 (-11/11I/11J)		UNITS	NOTES
	PARAMETER	MIN.	MAX.	MIN.	MAX.		
Common Notes							1, 2, 3, 4
Clock Input Timing							
tCK(DLL-off)	Minimum clock cycle time (DLL-off mode)	8	–	8	–	nS	45
tCK(avg)	Average Clock Period	See "Speed Bin" on page 137		See "Speed Bin" on page 136		pS	
tCH(avg)	Average CK/CK# high pulse width	0.47	0.53	0.47	0.53	tCK(avg)	
tCL(avg)	Average CK/CK# low pulse width	0.47	0.53	0.47	0.53	tCK(avg)	
tCK(abs)	Absolute Clock Period	Min.: tCK(avg)min + tJIT(per)min Max.: tCK(avg)max + tJIT(per)max				pS	37
tCH(abs)	Absolute CK/CK# high pulse width	0.43	–	0.43	–	tCK(avg)	38
tCL(abs)	Absolute CK/CK# low pulse width	0.43	–	0.43	–	tCK(avg)	39
tJIT(per)	Clock Period Jitter	-50	50	-60	60	pS	
tJIT(per,lck)	Clock Period Jitter during DLL locking period	-40	40	-50	50	pS	
tJIT(cc)	Cycle to Cycle Period Jitter	100		120		pS	
tJIT(cc,lck)	Cycle to Cycle Period Jitter during DLL locking period	80		100		pS	
tJIT(duty)	Clock Duty Cycle Jitter	Already included in tCH(abs) and tCL(abs)				pS	
tERR(2per)	Cumulative error across 2 cycles	-74	74	-88	88	pS	
tERR(3per)	Cumulative error across 3 cycles	-87	87	-105	105	pS	
tERR(4per)	Cumulative error across 4 cycles	-97	97	-117	117	pS	
tERR(5per)	Cumulative error across 5 cycles	-105	105	-126	126	pS	
tERR(6per)	Cumulative error across 6 cycles	-111	111	-133	133	pS	
tERR(7per)	Cumulative error across 7 cycles	-116	116	-139	139	pS	
tERR(8per)	Cumulative error across 8 cycles	-121	121	-145	145	pS	
tERR(9per)	Cumulative error across 9 cycles	-125	125	-150	150	pS	
tERR(10per)	Cumulative error across 10 cycles	-128	128	-154	154	pS	
tERR(11per)	Cumulative error across 11 cycles	-132	132	-158	158	pS	
tERR(12per)	Cumulative error across 12 cycles	-134	134	-161	161	pS	
tERR(nper)	Cumulative error across n = 13, 14...49, 50 cycles	Min.: tJIT(per)min * (1 + 0.68 * ln(n)) Max.: tJIT(per)max * (1 + 0.68 * ln(n))				pS	7

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AC Timing and Operating Condition for -09/09I/09J/-11/11I/11J speed grades, continued

SYMBOL	SPEED GRADE / PARAMETER		DDR3-2133 (-09/09I/09J) MIN.	DDR3-2133 (-09/09I/09J) MAX.	DDR3-1866 (-11/11I/11J) MIN.	DDR3-1866 (-11/11I/11J) MAX.	UNITS	NOTES
Data Timing								
tDQSQ	DQS, DQS# to DQ skew, per group, per access		–	75	–	85	pS	23
tQH	DQ output hold time from DQS, DQS#		0.38	–	0.38	–	tCK(avg)	18, 23
tLZ(DQ)	DQ low impedance time from CK, CK#		-360	180	-390	195	pS	17, 23, 24
tHZ(DQ)	DQ high impedance time from CK, CK#		–	180	–	195	pS	17, 23, 24
tDS(AC135)	Data setup time to DQS, DQS#	Base specification @ 2V/nS	53		68		pS	11, 40
		VREF @ 2 V/nS	120.5		135.5		pS	11, 40, 42
tDH(DC100)	Data hold time from DQS, DQS#	Base specification @ 2V/nS	55		70		pS	11, 40
		VREF @ 2 V/nS	105		120		pS	11, 40, 42
tDIPW	DQ and DM input pulse width for each input		280	–	320	–	pS	10
Data Strobe Timing								
tRPRE	DQS,DQS# differential READ Preamble		0.9	Note 21	0.9	Note 21	tCK(avg)	18, 21, 23
tRPST	DQS,DQS# differential READ Postamble		0.3	Note 22	0.3	Note 22	tCK(avg)	18, 22, 23
tQSH	DQS,DQS# differential output high time		0.4	–	0.4	–	tCK(avg)	18, 23
tQSL	DQS,DQS# differential output low time		0.4	–	0.4	–	tCK(avg)	18, 23
tWPRE	DQS,DQS# differential WRITE Preamble		0.9	–	0.9	–	tCK(avg)	46
tWPST	DQS,DQS# differential WRITE Postamble		0.3	–	0.3	–	tCK(avg)	46
tDQSCK	DQS,DQS# rising edge output access time from rising CK, CK#		-180	180	-195	195	pS	17, 23
tLZ(DQS)	DQS and DQS# low-impedance time from CK, CK# (Referenced from RL - 1)		-360	180	-390	195	pS	17, 23, 24
tHZ(DQS)	DQS and DQS# high-impedance time from CK, CK# (Referenced from RL + BL/2)		–	180	–	195	pS	17, 23, 24
tDQSL	DQS,DQS# differential input low pulse width		0.45	0.55	0.45	0.55	tCK(avg)	12, 14
tDQSH	DQS,DQS# differential input high pulse width		0.45	0.55	0.45	0.55	tCK(avg)	13, 14
tDQSS	DQS,DQS# rising edge to CK,CK# rising edge		-0.27	0.27	-0.27	0.27	tCK(avg)	16
tDSS	DQS,DQS# falling edge setup time to CK,CK# rising edge		0.18	–	0.18	–	tCK(avg)	15, 16
tDSH	DQS,DQS# falling edge hold time from CK,CK# rising edge		0.18	–	0.18	–	tCK(avg)	15, 16
Command and Address Timing								
tAA	Internal read command to first data		See “Speed Bin” on page 137		See “Speed Bin” on page 136		nS	8
tRCD	ACT to internal read or write delay time						nS	8
tRP	PRE command period						nS	8
tRC	ACT to ACT or REF command period						nS	8
tRAS	ACT to PRE command period						nS	8
tDLLK	DLL locking time		512	–	512	–	nCK	
tRTP	Internal READ Command to PRECHARGE Command delay		max(4nCK, 7.5nS)	–	max(4nCK, 7.5nS)	–		8
tWTR	Delay from start of internal write transaction to internal read command		max(4nCK, 7.5nS)	–	max(4nCK, 7.5nS)	–		8, 26

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AC Timing and Operating Condition for -09/09I/09J/-11/11I/11J speed grades, continued

SYMBOL	SPEED GRADE / PARAMETER		DDR3-2133 (-09/09I/09J) MIN.	DDR3-2133 (-09/09I/09J) MAX.	DDR3-1866 (-11/11I/11J) MIN.	DDR3-1866 (-11/11I/11J) MAX.	UNITS	NOTES
Command and Address Timing								
tWR	WRITE recovery time		15	–	15	–	nS	8, 26
tMRD	Mode Register Set command cycle time		4	–	4	–	nCK	
tMOD	Mode Register Set command update delay		max(12nCK, 15nS)	–	max(12nCK, 15nS)	–		
tCCD	CAS# to CAS# command delay		4	–	4	–	nCK	
tDAL(min)	Auto precharge write recovery + precharge time		WR + roundup(tRP(min)/ tCK(avg))				nCK	6
tMPRR	Multi-Purpose Register Recovery Time		1	–	1	–	nCK	29
tRRD	ACTIVE to ACTIVE command period for 1KB page size		max(4nCK, 5nS)	–	max(4nCK, 5nS)	–		8
tFAW	Four activate window for 1KB page size		25	–	27	–	nS	8
tIS(AC135)	Command and Address setup time to CK, CK#	Base specification	60		65		pS	9, 41
		VREF @ 1 V/nS	195		200		pS	9, 41, 42
tIS(AC125)	Command and Address setup time to CK, CK#	Base specification	135		150		pS	9, 41
		VREF @ 1 V/nS	260		275		pS	9, 41, 42
tIH(DC100)	Command and Address hold time from CK, CK#	Base specification	95		100		pS	9, 41
		VREF @ 1 V/nS	195		200		pS	9, 41, 42
tIPW	Control, address and control input pulse width for each input		470	–	535	–	pS	10
Calibration Timing								
tZQinit	Power-up and RESET calibration time		max(512nCK, 640nS)	–	max(512nCK, 640nS)	–		
tZQoper	Normal operation Full calibration time		max(256nCK, 320nS)	–	max(256nCK, 320nS)	–		
tZQCS	Normal operation Short calibration time		max(64nCK, 80nS)	–	max(64nCK, 80nS)	–		33
Reset Timing								
tXPR	Exit Reset from CKE HIGH to a valid command		max(5nCK, 120nS)	–	max(5nCK, 120nS)	–		
Self Refresh Timing								
tXS	Exit Self Refresh to commands not requiring a locked DLL		max(5nCK, 120nS)	–	max(5nCK, 120nS)	–		34
tXSDLL	Exit Self Refresh to commands requiring a locked DLL		tDLLK(min)	–	tDLLK(min)	–	nCK	35
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing		tCKE(min) + 1nCK	–	tCKE(min) + 1nCK	–		
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE)		max(5 nCK, 10nS)	–	max(5 nCK, 10nS)	–		
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX)		max(5 nCK, 10nS)	–	max(5 nCK, 10nS)	–		
Refresh Timing								
tRFC	REF command to ACT or REF command time		110	–	110	–	nS	36
tREFI	Average periodic refresh Interval	-40°C ≤ TCASE ≤ 85°C*	–	7.8	–	7.8	µS	
		0°C ≤ TCASE ≤ 85°C	–	7.8	–	7.8	µS	
		85°C < TCASE ≤ 95°C	–	3.9	–	3.9	µS	
		95°C < TCASE ≤ 105°C*	–	3.9	–	3.9	µS	

* -40°C ≤ TCASE ≤ 85°C is available for 09I, 09J, 11I and 11J grade parts only. 95°C < TCASE ≤ 105°C is available for 09J and 11J grade parts only.

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AC Timing and Operating Condition for -09/09I/09J/-11/11I/11J speed grades, continued

SYMBOL	SPEED GRADE	DDR3-2133 (-09/09I/09J)		DDR3-1866 (-11/11I/11J)		UNITS	NOTES
	PARAMETER	MIN.	MAX.	MIN.	MAX.		
Power Down Timing							
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nCK, 6nS)	–	max(3nCK, 6nS)	–		34
tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	max(10nCK, 24nS)	–	max(10nCK, 24nS)	–		35
tCKE	CKE minimum pulse width	max(3nCK, 5nS)	–	max(3nCK, 5nS)	–		
tCPDED	Command pass disable delay	2	–	2	–	nCK	
tPD	Power Down Entry to Exit Timing	tCKE(min)	9 * tREFI	tCKE(min)	9 * tREFI		25
tACTPDEN	Timing of ACT command to Power Down entry	2	–	1	–	nCK	27
tPRPDEN	Timing of PRE or PREA command to Power Down entry	2	–	1	–	nCK	27
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL + 4 + 1	–	RL + 4 + 1	–	nCK	
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	Min.: WL + 4 + roundup (tWR(min)/ tCK(avg)) Max.: –				nCK	20
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	Min.: WL + 4 + WR + 1 Max.: –				nCK	19
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	Min.: WL + 2 + roundup (tWR(min)/ tCK(avg)) Max.: –				nCK	20
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	Min.: WL + 2 + WR + 1 Max.: –				nCK	19
tREFPDEN	Timing of REF command to Power Down entry	2	–	1	–	nCK	27, 28
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(min)	–	tMOD(min)	–		
ODT Timing							
ODTH4	ODT high time without write command or with write command and burst chop 4	4	–	4	–	nCK	30
ODTH8	ODT high time with Write command and burst length 8	6	–	6	–	nCK	31
tAONPD	Asynchronous RTT turn-on delay (Power Down with DLL frozen)	2	8.5	2	8.5	nS	32
tAOFPD	Asynchronous RTT turn-off delay (Power Down with DLL frozen)	2	8.5	2	8.5	nS	32
tAON	RTT turn-on	-180	180	-195	195	pS	17, 43
tAOF	Rtt_Nom and Rtt_WR turn-off time from ODTLoff reference	0.3	0.7	0.3	0.7	tCK(avg)	17, 44
tADC	RTT dynamic change skew	0.3	0.7	0.3	0.7	tCK(avg)	17
Write Leveling Timing							
tWLMRD	First DQS/DQS# rising edge after write leveling mode is programmed	40	–	40	–	nCK	5
tWLDQSEN	DQS/DQS# delay after write leveling mode is programmed	25	–	25	–	nCK	5
tWLS	Write leveling setup time from (CK, CK#) zero crossing to rising (DQS, DQS#) zero crossing	125	–	140	–	pS	
tWLH	Write leveling hold time from rising (DQS, DQS#) zero crossing to (CK, CK#) zero crossing	125	–	140	–	pS	
tWLO	Write leveling output delay	0	7.5	0	7.5	nS	
tWLOE	Write leveling output error	0	2	0	2	nS	

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10.16.2 AC Timing and Operating Condition for -12/12I/12J/-15/15I/15J speed grades

SYMBOL	SPEED GRADE	DDR3-1600 (-12/12I/12J)		DDR3-1333 (-15/15I/15J)		UNITS	NOTES
	PARAMETER	MIN.	MAX.	MIN.	MAX.		
Common Notes							1, 2, 3, 4
Clock Input Timing							
tCK(DLL-off)	Minimum clock cycle time (DLL-off mode)	8	–	8	–	nS	45
tCK(avg)	Average Clock Period	See "Speed Bin" on page 135		See "Speed Bin" on page 134		pS	
tCH(avg)	Average CK/CK# high pulse width	0.47	0.53	0.47	0.53	tCK(avg)	
tCL(avg)	Average CK/CK# low pulse width	0.47	0.53	0.47	0.53	tCK(avg)	
tCK(abs)	Absolute Clock Period	Min.: tCK(avg)min + tJIT(per)min Max.: tCK(avg)max + tJIT(per)max				pS	37
tCH(abs)	Absolute CK/CK# high pulse width	0.43	–	0.43	–	tCK(avg)	38
tCL(abs)	Absolute CK/CK# low pulse width	0.43	–	0.43	–	tCK(avg)	39
tJIT(per)	Clock Period Jitter	-70	70	-80	80	pS	
tJIT(per,lck)	Clock Period Jitter during DLL locking period	-60	60	-70	70	pS	
tJIT(cc)	Cycle to Cycle Period Jitter	140		160		pS	
tJIT(cc,lck)	Cycle to Cycle Period Jitter during DLL locking period	120		140		pS	
tJIT(duty)	Clock Duty Cycle Jitter	Already included in tCH(abs) and tCL(abs)				pS	
tERR(2per)	Cumulative error across 2 cycles	-103	103	-118	118	pS	
tERR(3per)	Cumulative error across 3 cycles	-122	122	-140	140	pS	
tERR(4per)	Cumulative error across 4 cycles	-136	136	-155	155	pS	
tERR(5per)	Cumulative error across 5 cycles	-147	147	-168	168	pS	
tERR(6per)	Cumulative error across 6 cycles	-155	155	-177	177	pS	
tERR(7per)	Cumulative error across 7 cycles	-163	163	-186	186	pS	
tERR(8per)	Cumulative error across 8 cycles	-169	169	-193	193	pS	
tERR(9per)	Cumulative error across 9 cycles	-175	175	-200	200	pS	
tERR(10per)	Cumulative error across 10 cycles	-180	180	-205	205	pS	
tERR(11per)	Cumulative error across 11 cycles	-184	184	-210	210	pS	
tERR(12per)	Cumulative error across 12 cycles	-188	188	-215	215	pS	
tERR(nper)	Cumulative error across n = 13, 14...49, 50 cycles	Min.: tJIT(per)min * (1 + 0.68 * ln(n)) Max.: tJIT(per)max * (1 + 0.68 * ln(n))				pS	7

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AC Timing and Operating Condition for -12/12I/12J/-15/15I/15J speed grades, continued

SYMBOL	SPEED GRADE		DDR3-1600 (-12/12I/12J)		DDR3-1333 (-15/15I/15J)		UNITS	NOTES
	PARAMETER		MIN.	MAX.	MIN.	MAX.		
Data Timing								
tDQSQ	DQS, DQS# to DQ skew, per group, per access		–	100	–	125	pS	23
tQH	DQ output hold time from DQS, DQS#		0.38	–	0.38	–	tCK(avg)	18, 23
tLZ(DQ)	DQ low impedance time from CK, CK#		-450	225	-500	250	pS	17, 23, 24
tHZ(DQ)	DQ high impedance time from CK, CK#		–	225	–	250	pS	17, 23, 24
tDS(AC150)	Data setup time to DQS, DQS#	Base specification	10		30		pS	11, 40
		VREF @ 1 V/nS	160		180			11, 40, 42
tDH(DC100)	Data hold time from DQS, DQS#	Base specification	45		65		pS	11, 40
		VREF @ 1 V/nS	145		165			11, 40, 42
tDIPW	DQ and DM input pulse width for each input		360	–	400	–	pS	10
Data Strobe Timing								
tRPRE	DQS,DQS# differential READ Preamble		0.9	Note 21	0.9	Note 21	tCK(avg)	18, 21, 23
tRPST	DQS,DQS# differential READ Postamble		0.3	Note 22	0.3	Note 22	tCK(avg)	18, 22, 23
tQSH	DQS,DQS# differential output high time		0.4	–	0.4	–	tCK(avg)	18, 23
tQSL	DQS,DQS# differential output low time		0.4	–	0.4	–	tCK(avg)	18, 23
tWPRE	DQS,DQS# differential WRITE Preamble		0.9	–	0.9	–	tCK(avg)	46
tWPST	DQS,DQS# differential WRITE Postamble		0.3	–	0.3	–	tCK(avg)	46
tDQSCK	DQS,DQS# rising edge output access time from rising CK, CK#		-225	225	-255	255	pS	17, 23
tLZ(DQS)	DQS and DQS# low-impedance time from CK, CK# (Referenced from RL - 1)		-450	225	-500	250	pS	17, 23, 24
tHZ(DQS)	DQS and DQS# high-impedance time from CK, CK# (Referenced from RL + BL/2)		–	225	–	250	pS	17, 23, 24
tDQSL	DQS,DQS# differential input low pulse width		0.45	0.55	0.45	0.55	tCK(avg)	12, 14
tDQSH	DQS,DQS# differential input high pulse width		0.45	0.55	0.45	0.55	tCK(avg)	13, 14
tDQSS	DQS,DQS# rising edge to CK,CK# rising edge		-0.27	0.27	-0.25	0.25	tCK(avg)	16
tDSS	DQS,DQS# falling edge setup time to CK,CK# rising edge		0.18	–	0.2	–	tCK(avg)	15, 16
tDSH	DQS,DQS# falling edge hold time from CK,CK# rising edge		0.18	–	0.2	–	tCK(avg)	15, 16
Command and Address Timing								
tAA	Internal read command to first data		See “Speed Bin” on page 135		See “Speed Bin” on page 134		nS	8
tRCD	ACT to internal read or write delay time						nS	8
tRP	PRE command period						nS	8
tRC	ACT to ACT or REF command period						nS	8
tRAS	ACT to PRE command period						nS	8
tDLLK	DLL locking time		512	–	512	–	nCK	
tRTP	Internal READ Command to PRECHARGE Command delay		max(4nCK, 7.5nS)	–	max(4nCK, 7.5nS)	–		8
tWTR	Delay from start of internal write transaction to internal read command		max(4nCK, 7.5nS)	–	max(4nCK, 7.5nS)	–		8, 26

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AC Timing and Operating Condition for -12/12I/12J/-15/15I/15J speed grades, continued

SYMBOL	SPEED GRADE / PARAMETER		DDR3-1600 (-12/12I/12J) MIN.	DDR3-1600 (-12/12I/12J) MAX.	DDR3-1333 (-15/15I/15J) MIN.	DDR3-1333 (-15/15I/15J) MAX.	UNITS	NOTES
Command and Address Timing								
tWR	WRITE recovery time		15	–	15	–	nS	8, 26
tMRD	Mode Register Set command cycle time		4	–	4	–	nCK	
tMOD	Mode Register Set command update delay		max(12nCK, 15nS)	–	max(12nCK, 15nS)	–		
tCCD	CAS# to CAS# command delay		4	–	4	–	nCK	
tDAL(min)	Auto precharge write recovery + precharge time		WR + roundup(tRP(min)/ tCK(avg))				nCK	6
tMPRR	Multi-Purpose Register Recovery Time		1	–	1	–	nCK	29
tRRD	ACTIVE to ACTIVE command period for 1KB page size		max(4nCK, 6nS)	–	max(4nCK, 6nS)	–		8
tFAW	Four activate window for 1KB page size		30	–	30	–	nS	8
tIS(AC175)	Command and Address setup time to CK, CK#	Base specification	45		65		pS	9, 41
		VREF @ 1 V/nS	220		240		pS	9, 41, 42
tIS(AC150)	Command and Address setup time to CK, CK#	Base specification	170		190		pS	9, 41
		VREF @ 1 V/nS	320		340		pS	9, 41, 42
tIH(DC100)	Command and Address hold time from CK, CK#	Base specification	120		140		pS	9, 41
		VREF @ 1 V/nS	220		240		pS	9, 41, 42
tIPW	Control, address and control input pulse width for each input		560	–	620	–	pS	10
Calibration Timing								
tZQinit	Power-up and RESET calibration time		max(512nCK, 640nS)	–	max(512nCK, 640nS)	–		
tZQoper	Normal operation Full calibration time		max(256nCK, 320nS)	–	max(256nCK, 320nS)	–		
tZQCS	Normal operation Short calibration time		max(64nCK, 80nS)	–	max(64nCK, 80nS)	–		33
Reset Timing								
tXPR	Exit Reset from CKE HIGH to a valid command		max(5nCK, 120nS)	–	max(5nCK, 120nS)	–		
Self Refresh Timing								
tXS	Exit Self Refresh to commands not requiring a locked DLL		max(5nCK, 120nS)	–	max(5nCK, 120nS)	–		34
tXSDLL	Exit Self Refresh to commands requiring a locked DLL		tDLLK(min)	–	tDLLK(min)	–	nCK	35
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing		tCKE(min) + 1nCK	–	tCKE(min) + 1nCK	–		
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE)		max(5 nCK, 10nS)	–	max(5 nCK, 10nS)	–		
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX)		max(5 nCK, 10nS)	–	max(5 nCK, 10nS)	–		
Refresh Timing								
tRFC	REF command to ACT or REF command time		110	–	110	–	nS	36
tREFI	Average periodic refresh Interval	-40°C ≤ TCASE ≤ 85°C*	–	7.8	–	7.8	µS	
		0°C ≤ TCASE ≤ 85°C	–	7.8	–	7.8	µS	
		85°C < TCASE ≤ 95°C	–	3.9	–	3.9	µS	
		95°C < TCASE ≤ 105°C*	–	3.9	–	3.9	µS	

* -40°C ≤ TCASE ≤ 85°C is available for 12I, 12J, 15I and 15J grade parts only. 95°C < TCASE ≤ 105°C is available for 12J and 15J grade parts only.

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AC Timing and Operating Condition for -12/12I/-15/15I speed grades, continued

SYMBOL	SPEED GRADE	DDR3-1600 (-12/12I)		DDR3-1333 (-15/15I)		UNITS	NOTES
	PARAMETER	MIN.	MAX.	MIN.	MAX.		
Power Down Timing							
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nCK, 6nS)	–	max(3nCK, 6nS)	–		34
tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	max(10nCK, 24nS)	–	max(10nCK, 24nS)	–		35
tCKE	CKE minimum pulse width	max(3nCK, 5nS)	–	max(3nCK, 5.625nS)	–		
tCPDED	Command pass disable delay	1	–	1	–	nCK	
tPD	Power Down Entry to Exit Timing	tCKE(min)	9 * tREFI	tCKE(min)	9 * tREFI		25
tACTPDEN	Timing of ACT command to Power Down entry	1	–	1	–	nCK	27
tPRPDEN	Timing of PRE or PREA command to Power Down entry	1	–	1	–	nCK	27
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL + 4 + 1	–	RL + 4 + 1	–	nCK	
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	Min.: WL + 4 + roundup (tWR(min)/ tCK(avg)) Max.: –				nCK	20
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	Min.: WL + 4 + WR + 1 Max.: –				nCK	19
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	Min.: WL + 2 + roundup (tWR(min)/ tCK(avg)) Max.: –				nCK	20
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	Min.: WL + 2 + WR + 1 Max.: –				nCK	19
tREFPDEN	Timing of REF command to Power Down entry	1	–	1	–	nCK	27, 28
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(min)	–	tMOD(min)	–		
ODT Timing							
ODTH4	ODT high time without write command or with write command and burst chop 4	4	–	4	–	nCK	30
ODTH8	ODT high time with Write command and burst length 8	6	–	6	–	nCK	31
tAONPD	Asynchronous RTT turn-on delay (Power Down with DLL frozen)	2	8.5	2	8.5	nS	32
tAOFPD	Asynchronous RTT turn-off delay (Power Down with DLL frozen)	2	8.5	2	8.5	nS	32
tAON	RTT turn-on	-225	225	-250	250	pS	17, 43
tAOF	Rtt_Nom and Rtt_WR turn-off time from ODTLoff reference	0.3	0.7	0.3	0.7	tCK(avg)	17, 44
tADC	RTT dynamic change skew	0.3	0.7	0.3	0.7	tCK(avg)	17
Write Leveling Timing							
tWLMRD	First DQS/DQS# rising edge after write leveling mode is programmed	40	–	40	–	nCK	5
tWLDQSEN	DQS/DQS# delay after write leveling mode is programmed	25	–	25	–	nCK	5
tWLS	Write leveling setup time from (CK, CK#) zero crossing to rising (DQS, DQS#) zero crossing	165	–	195	–	pS	
tWLH	Write leveling hold time from rising (DQS, DQS#) zero crossing to (CK, CK#) zero crossing	165	–	195	–	pS	
tWLO	Write leveling output delay	0	7.5	0	9	nS	
tWLOE	Write leveling output error	0	2	0	2	nS	

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10.16.3 Timing Parameter Notes

1. Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.

   For example, tMRD = 4 [nCK] means; if one Mode Register Set command is registered at Tm, another Mode Register Set command may be registered at Tm+4, even if (Tm+4 - Tm) is 4 x tCK(avg) + tERR(4per),min (which is smaller than 4 x tCK(avg)).
2. Timing that is not specified is illegal and after such an event, in order to provide proper operation, the DRAM must be resetted or powered down and then restarted through the specified initialization sequence before normal operation can continue.
3. The CK/CK# input reference level (for timing reference to CK / CK#) is the point at which CK and CK# cross.

   The DQS/DQS# input reference level is the point at which DQS and DQS# cross;

   The input reference level for signals other than CK/CK#, DQS/DQS# and RESET# is VREFCA and VREFDQ respectively.
4. Inputs are not recognized as valid until VREFCA stabilizes within specified limits.
5. The max values are system dependent.
6. tCK(avg) refers to the actual application clock period. WR refers to the WR parameter stored in mode register MR0.
7. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
8. For these parameters, the DDR3 SDRAM device supports tnPARAM [nCK] = RU{ tPARAM [nS] / tCK(avg) [nS] }, which is in clock cycles, assuming all input clock jitter specifications are satisfied.

   For example, the device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-1333 (9-9-9), of which tRP = 13.5nS, the device will support tnRP = RU{tRP / tCK(avg)} = 9, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+9 is valid even if (Tm+9 - Tm) is less than 13.5nS due to input clock jitter.
9. These parameters are measured from a command/address signal (CKE, CS#, RAS#, CAS#, WE#, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
10. Pulse width of a input signal is defined as the width between the first crossing of VREF(DC) and the consecutive crossing of VREF(DC).
11. These parameters are measured from a data signal (DM, DQ0, DQ1, etc.) transition edge to its respective data strobe signal (DQS, DQS#) crossing.
12. tDQSL describes the instantaneous differential input low pulse width on DQS - DQS#, as measured from one falling edge to the next consecutive rising edge.
13. tDQSH describes the instantaneous differential input high pulse width on DQS - DQS#, as measured from one rising edge to the next consecutive falling edge.
14. tDQSH,act + tDQSL,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
15. tDSH,act + tDSS,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
16. These parameters are measured from a data strobe signal (DQS, DQS#) crossing to its respective clock signal (CK, CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

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17. When the device is operated with input clock jitter, this parameter needs to be derated by the actual t_{ERR}(mper),act of the input clock, where 2 <= m <= 12. (output deratings are relative to the actual SDRAM input clock.)

    For example, if the measured jitter into a DDR3-1333 SDRAM has t_{ERR}(mper),act,min = - 138 pS and t_{ERR}(mper),act,max = + 155 pS, then

    t_{DQSCK},min(derated) = t_{DQSCK},min - t_{ERR}(mper),act,max = - 255 pS - 155 pS = - 410 pS and t_{DQSCK},max(derated) = t_{DQSCK},max - t_{ERR}(mper),act,min = 255 pS + 138 pS = + 393 pS.

    Similarly, $t_{LZ(DQ)}$ for DDR3-1333 derates to $t_{LZ(DQ)}$,min(derated) = - 500 pS - 155 pS = - 655 pS and $t_{LZ(DQ)}$,max(derated) = 250 pS + 138 pS = + 388 pS. (Caution on the min/max usage!)

    Note that t_{ERR}(mper),act,min is the minimum measured value of t_{ERR}(nper) where 2 <= n <= 12, and t_{ERR}(mper),act,max is the maximum measured value of t_{ERR}(nper) where 2 <= n <= 12.

18. When the device is operated with input clock jitter, this parameter needs to be derated by the actual t_{JIT}(per),act of the input clock. (output deratings are relative to the SDRAM input clock.)

    For example, if the measured jitter into a DDR3-1333 SDRAM has t_{CK}(avg),act = 1500 pS, t_{JIT}(per),act,min = - 58 pS and t_{JIT}(per),act,max = + 74 pS, then

    t_{RPRE},min(derated) = t_{RPRE},min + t_{JIT}(per),act,min = 0.9 x t_{CK}(avg),act + t_{JIT}(per),act,min = 0.9 x 1500 pS - 58 pS = + 1292 pS.

    Similarly, t_{QH},min(derated) = t_{QH},min + t_{JIT}(per),act,min = 0.38 x t_{CK}(avg),act + t_{JIT}(per),act,min = 0.38 x 1500 pS - 58 pS = + 512 pS. (Caution on the min/max usage!).

19. WR in clock cycles as programmed in mode register MR0.

20. t_{WR}(min) is defined in nS, for calculation of t_{WRPDEN} it is necessary to round up t_{WR}(min)/t_{CK}(avg) to the next integer value.

21. The maximum read preamble is bound by $t_{LZ(DQS)}$min on the left side and t_{DQSCK}(max) on the right side. See Figure 24 - **"READ Timing; Clock to Data Strobe relationship"** on page 45.

22. The maximum read postamble is bound by t_{DQSCK}(min) plus t_{QSH}(min) on the left side and $t_{HZ(DQS)}$max on the right side. See Figure 24 - **"READ Timing; Clock to Data Strobe relationship"** on page 45.

23. Value is only valid for RON34.

24. Single ended signal parameter.

25. t_{REFI} depends on T_{OPER}.

26. Start of internal write transaction is defined as follows:

    For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.

    For BC4 (on- the- fly): Rising clock edge 4 clock cycles after WL.

    For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.

27. CKE is allowed to be registered low while operations such as row activation, precharge, auto-precharge or refresh are in progress, but power down I_{DD} spec will not be applied until finishing those operations.

28. Although CKE is allowed to be registered LOW after a REFRESH command once $t_{REFPDEN}$(min) is satisfied, there are cases where additional time such as t_{XPDLL}(min) is also required. See section 8.17.3 **"Power-Down clarifications - Case 2"** on page 75.

29. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.

30. ODTH4 is measured from ODT first registered high (without a Write command) to ODT first registered low, or from ODT registered high together with a Write command with burst length 4 to ODT registered low.

31. ODTH8 is measured from ODT registered high together with a Write command with burst length 8 to ODT registered low.

32. This parameter applies upon entry and during precharge power down mode with DLL frozen.

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33. One ZQCS command can effectively correct a minimum of 0.5 % (ZQ Correction) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.

    One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

    where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

    For example, if TSens = 1.5% / °C, VSens = 0.15% / mV, Tdriftrate = 1 °C / sec and Vdriftrate = 15 mV/sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128mS$$

34. Commands not requiring a locked DLL are all commands except Read, Read with Auto-Precharge and Synchronous ODT.
35. Commands requiring a locked DLL are Read, Read with Auto-Precharge and Synchronous ODT.
36. A maximum of one regular plus eight posted refresh commands can be issued to any given DDR3 SDRAM device meaning that the maximum absolute interval between any refresh command and the next refresh command is 9 ×t_{REFI}.
37. Parameter t_{CK}(avg) is specified per its average value. However, it is understood that the relationship between the average timing t_{CK}(avg) and the respective absolute instantaneous timing t_{CK}(abs) holds all times.
38. t_{CH}(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
39. t_{CL}(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
40. t_{DS}(base) and t_{DH}(base) values are for a single-ended 1V/nS slew rate DQs (DQs are at 2V/nS for DDR3-1866 and DDR3-2133) and 2V/nS DQS, DQS# differential slew rate. Note for DQ and DM signals, $V_{REF(DC)}$ = $V_{REFDQ(DC)}$. For input only pins except RESET#, $V_{REF(DC)}$ = $V_{REFCA(DC)}$. See section 10.16.5 **"Data Setup, Hold and Slew Rate Derating"** on page 157.
41. t_{IS}(base) and t_{IH}(base) values are for 1V/nS CMD/ADD single-ended slew rate and 2V/nS CK, CK# differential slew rate. Note for DQ and DM signals, $V_{REF(DC)}$ = $V_{REFDQ(DC)}$. For input only pins except RESET#, $V_{REF(DC)}$ = $V_{REFCA(DC)}$. See section 10.16.4 **"Address / Command Setup, Hold and Derating"** on page 150.
42. The setup and hold times are listed converting the base specification values (to which derating tables apply) to V_{REF} when the slew rate is 1 V/nS (DQs are at 2V/nS for DDR3-1866 and DDR3-2133). These values, with a slew rate of 1 V/nS (DQs are at 2V/nS for DDR3-1866 and DDR3-2133), are for reference only.
43. For definition of RTT turn-on time t_{AON} See 8.19.2.2 **"Timing Parameters"** on page 80.
44. For definition of RTT turn-off time t_{AOF} See 8.19.2.2 **"Timing Parameters"** on page 80.
45. There is no maximum cycle time limit besides the need to satisfy the refresh interval, t_{REFI}.
46. Actual value dependent upon measurement level definitions See Figure 41 - **"Method for calculating t_{WPRE} transitions and endpoints"** on page 58 and See Figure 42 - **"Method for calculating t_{WPST} transitions and endpoints"** on page 58.

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10.16.4 Address / Command Setup, Hold and Derating

For all input signals the total t_{IS} (setup time) and t_{IH} (hold time) required is calculated by adding the datasheet $t_{IS(base)}$ and $t_{IH(base)}$ value (see Table 49) to the Δt_{IS} and Δt_{IH} derating value (see Table 50 to Table 53) respectively. Example: t_{IS} (total setup time) = $t_{IS(base)}$ + Δt_{IS}

Setup (t_{IS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)}$min. Setup (t_{IS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)}$max. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(DC)}$ to AC region', use nominal slew rate for derating value (see Figure 107). If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(DC)}$ to AC region', the slew rate of a tangent line to the actual signal from the AC level to $V_{REF(DC)}$ level is used for derating value (see Figure 109).

Hold (t_{IH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)}$max and the first crossing of $V_{REF(DC)}$. Hold (t_{IH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)}$min and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between shaded 'DC to $V_{REF(DC)}$ region', use nominal slew rate for derating value (see Figure 108). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'DC to $V_{REF(DC)}$ region', the slew rate of a tangent line to the actual signal from the DC level to $V_{REF(DC)}$ level is used for derating value (see Figure 110).

For a valid transition the input signal has to remain above/below $V_{IH/IL(AC)}$ for some time t_{VAC} (see Table 54).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(AC)}$ at the time of the rising clock transition, a valid input signal is still required to complete the transition and reach $V_{IH/IL(AC)}$.

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table 49 – ADD/CMD Setup and Hold Base-Values for 1V/nS

Symbol	Reference	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Unit
$t_{IS(base)}$ AC175	$V_{IH/L(AC)}$	65	45	-	-	pS
$t_{IS(base)}$ AC150	$V_{IH/L(AC)}$	190	170	-	-	pS
$t_{IS(base)}$ AC135	$V_{IH/L(AC)}$	-	-	65	60	pS
$t_{IS(base)}$ AC125	$V_{IH/L(AC)}$	-	-	150	135	pS
$t_{IH(base)}$ DC100	$V_{IH/L(DC)}$	140	120	100	95	pS

Notes:

1. (AC/DC referenced for 1V/nS Address/Command slew rate and 2 V/nS differential CK-CK# slew rate)
2. The $t_{IS(base)\ AC150}$ specifications are adjusted from the $t_{IS(base)\ AC175}$ specification by adding an additional 100pS for DDR3-1333/1600 of derating to accommodate for the lower alternate threshold of 150 mV and another 25 pS to account for the earlier reference point [(175 mV - 150 mV) / 1 V/nS].
3. The $t_{IS(base)\ AC125}$ specifications are adjusted from the $t_{IS(base)\ AC135}$ specification by adding an additional 75pS for DDR3-1866 or 65pS for DDR3-2133 of derating to accommodate for the lower alternate threshold of 125 mV and another 10 pS to account for the earlier reference point [(135 mV - 125 mV) / 1 V/nS].

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Table 50 – Derating values DDR3-1333/1600 tIS/tIH - AC/DC based AC175 Threshold

CMD/ ADD Slew rate (V/nS)	ΔtIS, ΔtIH derating in [pS] AC/DC based AC175 Threshold -> VIH(AC)=VREF(DC)+175mV, VIL(AC)=VREF(DC)-175mV															
	CK, CK# Differential Slew Rate															
	4.0 V/nS		3.0 V/nS		2.0 V/nS		1.8 V/nS		1.6 V/nS		1.4 V/nS		1.2 V/nS		1.0 V/nS	
	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
2.0	88	50	88	50	88	50	96	58	104	66	112	74	120	84	128	100
1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	84
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	-2	-4	-2	-4	-2	-4	6	4	14	12	22	20	30	30	38	46
0.8	-6	-10	-6	-10	-6	-10	2	-2	10	6	18	14	26	24	34	40
0.7	-11	-16	-11	-16	-11	-16	-3	-8	5	0	13	8	21	18	29	34
0.6	-17	-26	-17	-26	-17	-26	-9	-18	-1	-10	7	-2	15	8	23	24
0.5	-35	-40	-35	-40	-35	-40	-27	-32	-19	-24	-11	-16	-2	-6	5	10
0.4	-62	-60	-62	-60	-62	-60	-54	-52	-46	-44	-38	-36	-30	-26	-22	-10

Table 51 – Derating values DDR3-1333/1600 tIS/tIH - AC/DC based - Alternate AC150 Threshold

CMD/ ADD Slew rate (V/nS)	ΔtIS, ΔtIH derating in [pS] AC/DC based Alternate AC150 Threshold -> VIH(AC)=VREF(DC)+150mV, VIL(AC)=VREF(DC)-150mV															
	CK, CK# Differential Slew Rate															
	4.0 V/nS		3.0 V/nS		2.0 V/nS		1.8 V/nS		1.6 V/nS		1.4 V/nS		1.2 V/nS		1.0 V/nS	
	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
2.0	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	0	-4	0	-4	0	-4	8	4	16	12	24	20	32	30	40	46
0.8	0	-10	0	-10	0	-10	8	-2	16	6	24	14	32	24	40	40
0.7	0	-16	0	-16	0	-16	8	-8	16	0	24	8	32	18	40	34
0.6	-1	-26	-1	-26	-1	-26	7	-18	15	-10	23	-2	31	8	39	24
0.5	-10	-40	-10	-40	-10	-40	-2	-32	6	-24	14	-16	22	-6	30	10
0.4	-25	-60	-25	-60	-25	-60	-17	-52	-9	-44	-1	-36	7	-26	15	-10

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Table 52 – Derating values DDR3-1866/2133 tIS/tIH - AC/DC based Alternate AC135 Threshold

CMD/ ADD Slew rate (V/nS)	ΔtIS, ΔtIH derating in [pS] AC/DC based Alternate AC135 Threshold -> VIH(AC)=VREF(DC)+135mV, VIL(AC)=VREF(DC)-135mV															
	CK, CK# Differential Slew Rate															
	4.0 V/nS		3.0 V/nS		2.0 V/nS		1.8 V/nS		1.6 V/nS		1.4 V/nS		1.2 V/nS		1.0 V/nS	
	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
2.0	68	50	68	50	68	50	76	58	84	66	92	74	100	84	108	100
1.5	45	34	45	34	45	34	53	42	61	50	69	58	77	68	85	84
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	2	-4	2	-4	2	-4	10	4	18	12	26	20	34	30	42	46
0.8	3	-10	3	-10	3	-10	11	-2	19	6	27	14	35	24	43	40
0.7	6	-16	6	-16	6	-16	14	-8	22	0	30	8	38	18	46	34
0.6	9	-26	9	-26	9	-26	17	-18	25	-10	33	-2	41	8	49	24
0.5	5	-40	5	-40	5	-40	13	-32	21	-24	29	-16	37	-6	45	10
0.4	-3	-60	-3	-60	-3	-60	6	-52	14	-44	22	-36	30	-26	38	-10

Table 53 – Derating values DDR3-1866/2133 tIS/tIH - AC/DC based Alternate AC125 Threshold

CMD/ ADD Slew rate (V/nS)	ΔtIS, ΔtIH derating in [pS] AC/DC based Alternate AC125 Threshold -> VIH(AC)=VREF(DC)+125mV, VIL(AC)=VREF(DC)-125mV															
	CK, CK# Differential Slew Rate															
	4.0 V/nS		3.0 V/nS		2.0 V/nS		1.8 V/nS		1.6 V/nS		1.4 V/nS		1.2 V/nS		1.0 V/nS	
	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
2.0	63	50	63	50	63	50	71	58	79	66	87	74	95	84	103	100
1.5	42	34	42	34	42	34	50	42	58	50	66	58	74	68	82	84
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	4	-4	4	-4	4	-4	12	4	20	12	28	20	36	30	44	46
0.8	6	-10	6	-10	6	-10	14	-2	22	6	30	14	38	24	46	40
0.7	11	-16	11	-16	11	-16	19	-8	27	0	35	8	43	18	51	34
0.6	16	-26	16	-26	16	-26	24	-18	32	-10	40	-2	48	8	56	24
0.5	15	-40	15	-40	15	-40	23	-32	31	-24	39	-16	47	-6	55	10
0.4	13	-60	13	-60	13	-60	21	-52	29	-44	37	-36	45	-26	53	-10

Table 54 – Required time tVAC above VIH(AC) {below VIL(AC)} for valid ADD/CMD transition

Slew Rate [V/nS]	DDR3-1333/1600				DDR3-1866/2133			
	tVAC @ 175mV [pS]		tVAC @ 150mV [pS]		tVAC @ 135mV [pS]		tVAC @ 125mV [pS]	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
> 2.0	75	-	175	-	168	-	173	-
2.0	57	-	170	-	168	-	173	-
1.5	50	-	167	-	145	-	152	-
1.0	38	-	130	-	100	-	110	-
0.9	34	-	113	-	85	-	96	-
0.8	29	-	93	-	66	-	79	-
0.7	22	-	66	-	42	-	56	-
0.6	Note	-	30	-	10	-	27	-
0.5	Note	-	Note	-	Note	-	Note	-
< 0.5	Note	-	Note		Note	-	Note	-

Note: Rising input signal shall become equal to or greater than VIH(AC) level and Falling input signal shall become equal to or less than VIL(AC) level.

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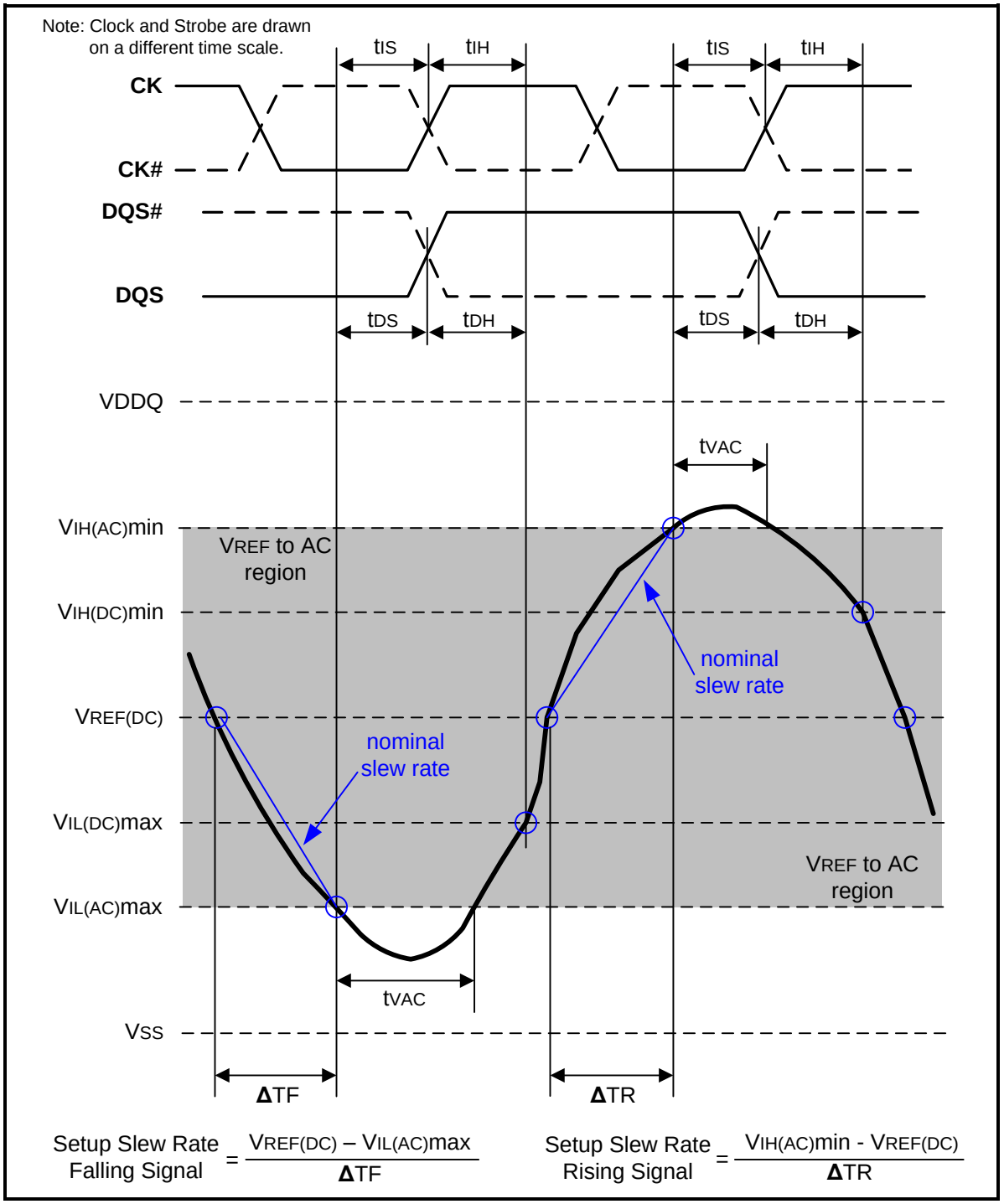


Figure 107 – Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

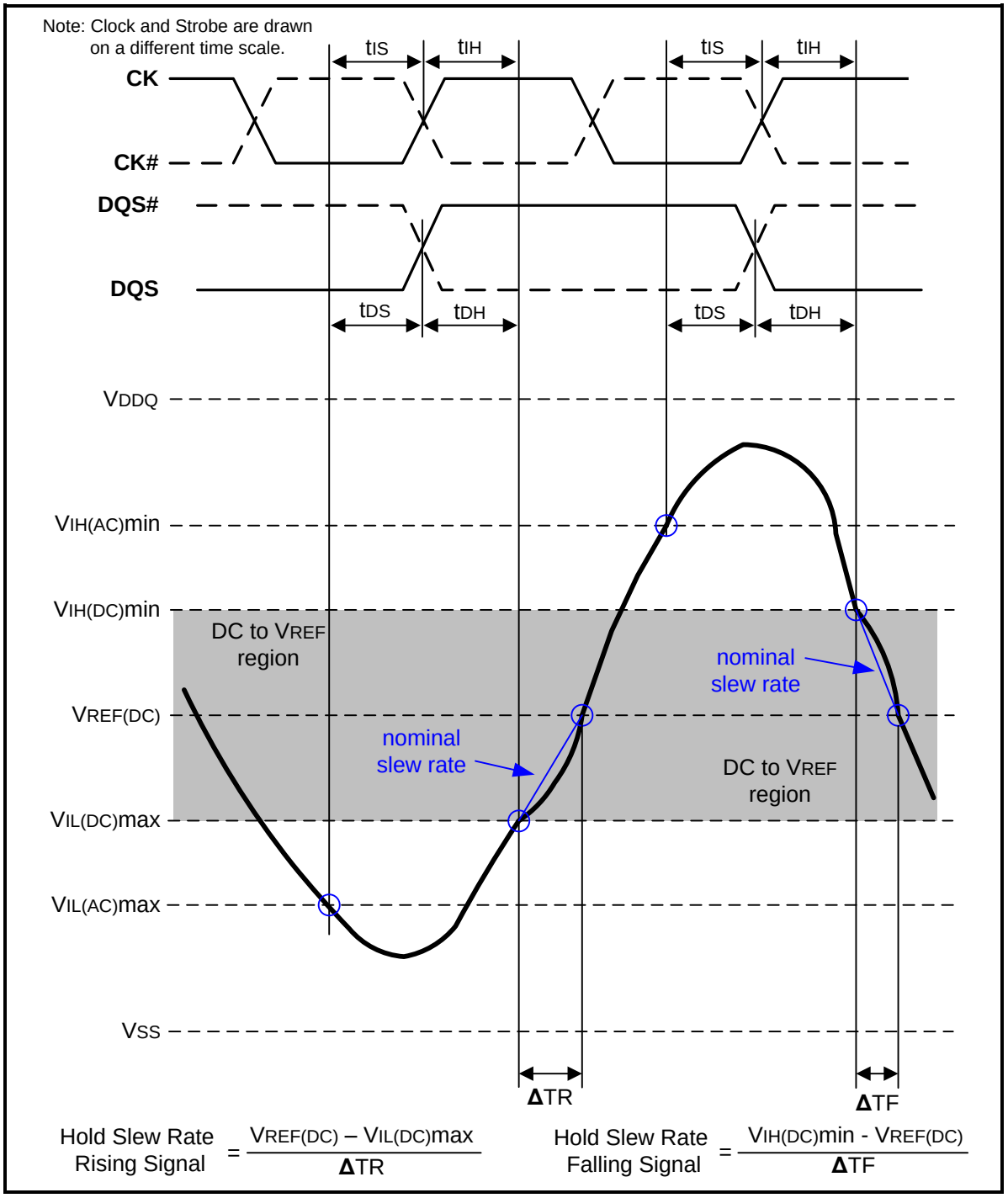


Figure 108 – Illustration of nominal slew rate for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock)

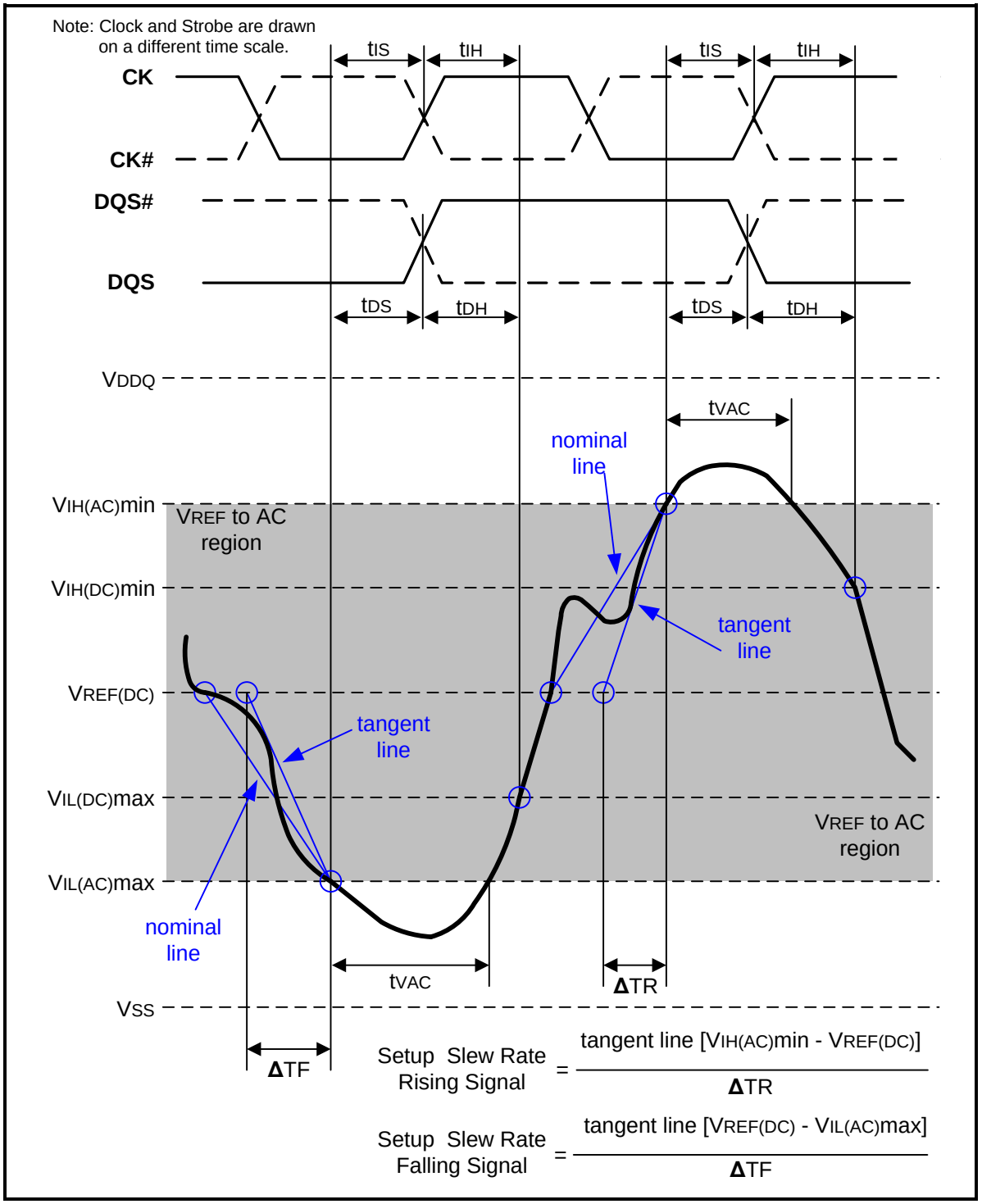


Figure 109 – Illustration of tangent line for setup time tDS (for DQ with respect to strobe) and tIS (for ADD/CMD with respect to clock)

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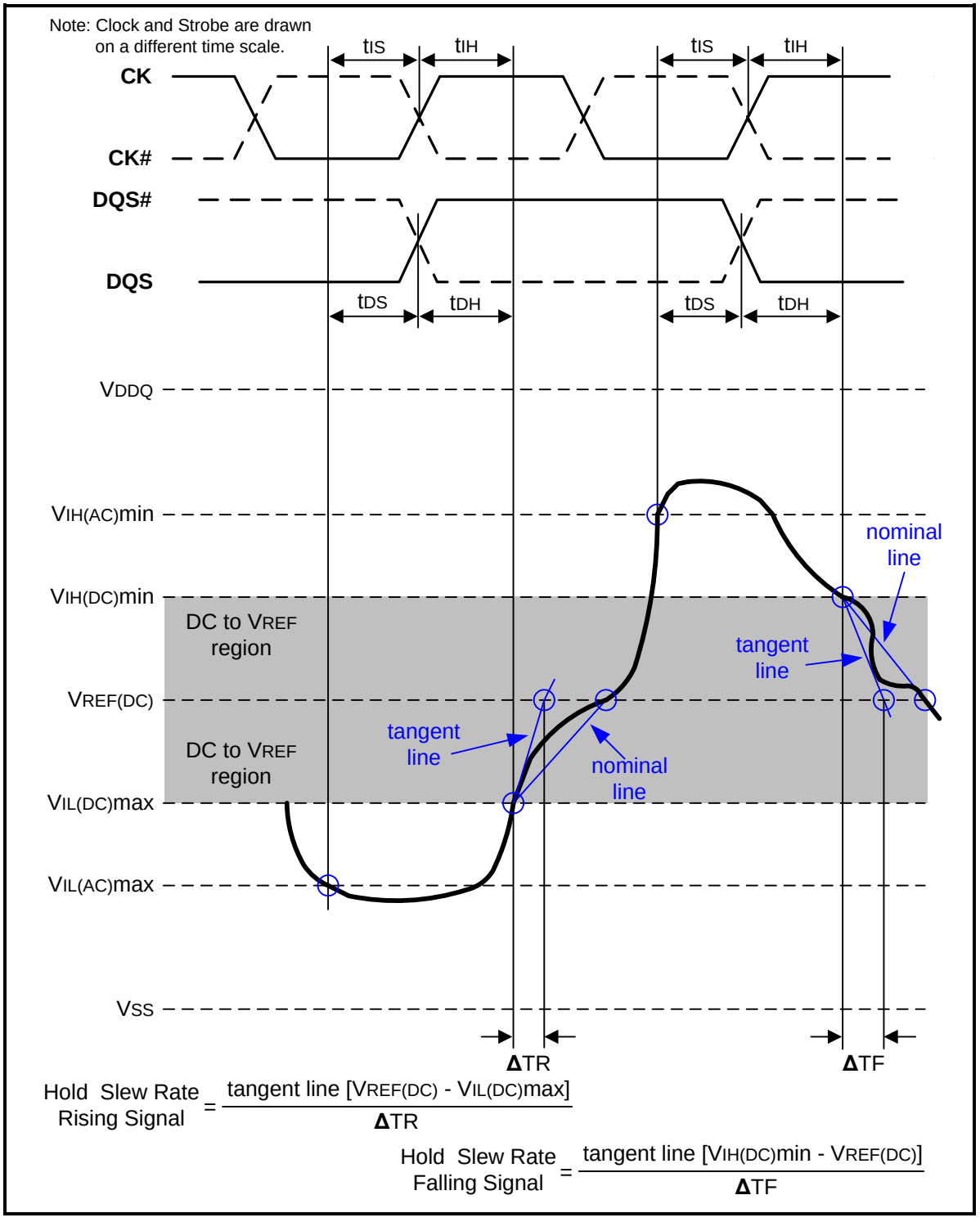


Figure 110 – Illustration of tangent line for hold time tDH (for DQ with respect to strobe) and tIH (for ADD/CMD with respect to clock)

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10.16.5 Data Setup, Hold and Slew Rate Derating

For all input signals the total t_{DS} (setup time) and t_{DH} (hold time) required is calculated by adding the data sheet $t_{DS(base)}$ and $t_{DH(base)}$ value (see Table 55) to the Δt_{DS} and Δt_{DH} (see Table 56 and Table 57) derating value respectively. Example: t_{DS} (total setup time) = $t_{DS(base)}$ + Δt_{DS}.

Setup (t_{DS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IH(AC)}$min. Setup (t_{DS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)}$max (see Figure 107). If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(DC)}$ to AC region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(DC)}$ to AC region', the slew rate of a tangent line to the actual signal from the AC level to $V_{REF(DC)}$ level is used for derating value (see Figure 109).

Hold (t_{DH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)}$max and the first crossing of $V_{REF(DC)}$. Hold (t_{DH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)}$min and the first crossing of $V_{REF(DC)}$ (see Figure 108). If the actual signal is always later than the nominal slew rate line between shaded 'DC level to $V_{REF(DC)}$ region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'DC to $V_{REF(DC)}$ region', the slew rate of a tangent line to the actual signal from the DC level to $V_{REF(DC)}$ level is used for derating value (see Figure 110).

For a valid transition the input signal has to remain above/below $V_{IH/IL(AC)}$ for some time t_{VAC} (see Table 58).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(AC)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(AC)}$.

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table 55 – Data Setup and Hold Base-Values

Symbol	Reference	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Unit	Notes
tDS(base) AC150	VIH/L(AC) SR=1V/nS	30	10	-	-	pS	2
tDS(base) AC135	VIH/L(AC) SR=2V/nS	-	-	68	53	pS	1
tDH(base) DC100	VIH/L(DC) SR=1V/nS	65	45	-	-	pS	2
tDH(base) DC100	VIH/L(DC) SR=2V/nS	-	-	70	55	pS	1

Notes:

1. (AC/DC referenced for 2V/nS DQ-slew rate and 4 V/nS DQS slew rate).
2. (AC/DC referenced for 1V/nS DQ-slew rate and 2 V/nS DQS slew rate).

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Table 56 – Derating values for DDR3-1333/1600 tDS/tDH - (AC150)

DQ Slew rate (V/nS)	ΔtDS, ΔtDH derating in [pS] AC/DC based* DQS, DQS# Differential Slew Rate															
	4.0 V/nS		3.0 V/nS		2.0 V/nS		1.8 V/nS		1.6 V/nS		1.4 V/nS		1.2 V/nS		1.0 V/nS	
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
2.0	75	50	75	50	75	50	-	-	-	-	-	-	-	-	-	-
1.5	50	34	50	34	50	34	58	42	-	-	-	-	-	-	-	-
1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
0.9	-	-	0	-4	0	-4	8	4	16	12	24	20	-	-	-	-
0.8	-	-	-	-	0	-10	8	-2	16	6	24	14	32	24	-	-
0.7	-	-	-	-	-	-	8	-8	16	0	24	8	32	18	40	34
0.6	-	-	-	-	-	-	-	-	15	-10	23	-2	31	8	39	24
0.5	-	-	-	-	-	-	-	-	-	-	14	-16	22	-6	30	10
0.4	-	-	-	-	-	-	-	-	-	-	-	-	7	-26	15	-10

Note: Cell contents '-' are defined as not supported.

Table 57 – Derating values for DDR3-1866/2133 tDS/tDH - (AC135)

DQ Slew rate (V/nS)	ΔtDS, ΔtDH derating in [pS] AC/DC based* Alternate AC135 Threshold -> VIH(AC)=VREF(DC)+135mV, VIL(AC)=VREF(DC)-135mV Alternate DC100 Threshold -> VIH(DC)=VREF(DC)+100mV, VIL(DC)=VREF(DC)-100mV DQS, DQS# Differential Slew Rate																							
	8.0 V/nS		7.0 V/nS		6.0 V/nS		5.0 V/nS		4.0 V/nS		3.0 V/nS		2.0 V/nS		1.8 V/nS		1.6 V/nS		1.4 V/nS		1.2 V/nS		1.0 V/nS	
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
4.0	34	25	34	25	34	25	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
3.5	29	21	29	21	29	21	29	21	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
3.0	23	17	23	17	23	17	23	17	23	17	-	-	-	-	-	-	-	-	-	-	-	-	-	-
2.5	-	-	14	10	14	10	14	10	14	10	14	10	-	-	-	-	-	-	-	-	-	-	-	-
2.0	-	-	-	-	0	0	0	0	**0**	**0**	0	0	0	0	-	-	-	-	-	-	-	-	-	-
1.5	-	-	-	-	-	-	-23	-17	-23	-17	-23	-17	-23	-17	-15	-9	-	-	-	-	-	-	-	-
1.0	-	-	-	-	-	-	-	-	-68	-50	-68	-50	-68	-50	-60	-42	-52	-34	-	-	-	-	-	-
0.9	-	-	-	-	-	-	-	-	-	-	-66	-54	-66	-54	-58	-46	-50	-38	-42	-30	-	-	-	-
0.8	-	-	-	-	-	-	-	-	-	-	-	-	-64	-60	-56	-52	-48	-44	-40	-36	-32	-26	-	-
0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-53	-59	-45	-51	-37	-43	-29	-33	-21	-17
0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-43	-61	-35	-53	-27	-43	-19	-27
0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-39	-66	-31	-56	-23	-40
0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-38	-76	-30	-60

Note: Cell contents '-' are defined as not supported.

Table 58 – Required time tVAC above VIH(AC) {below VIL(AC)} for valid DQ transition

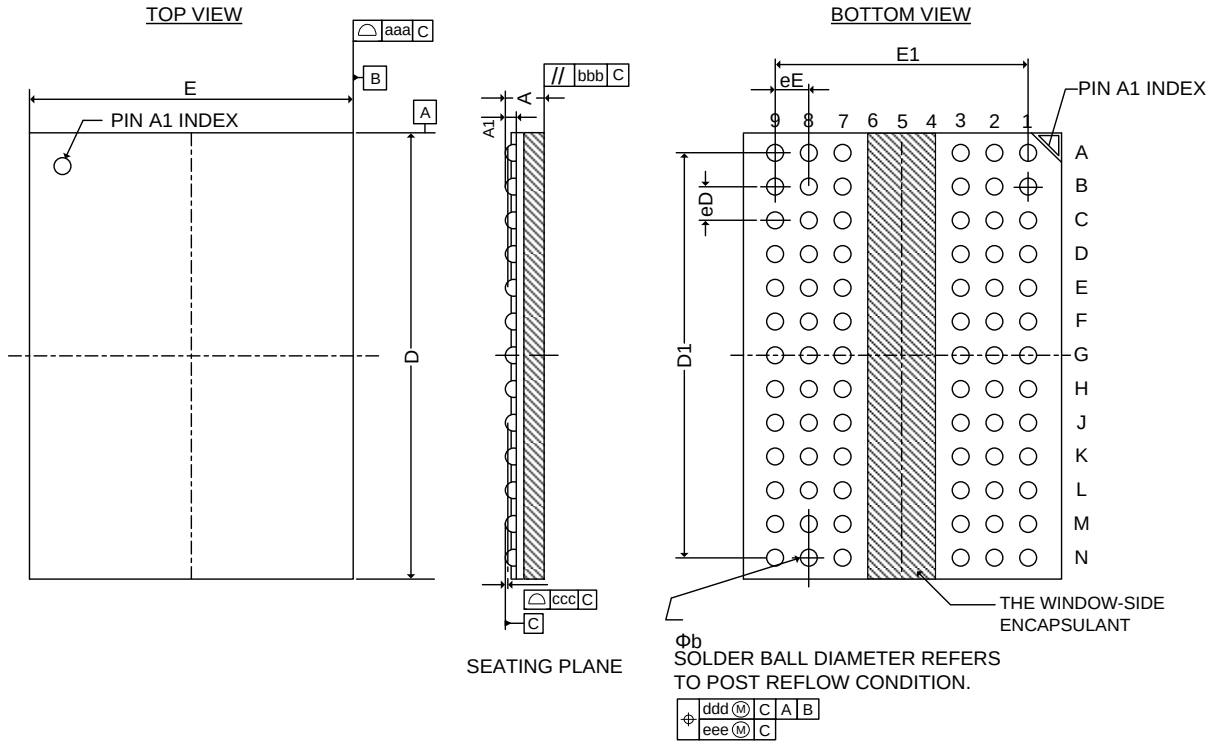
Slew Rate [V/nS]	DDR3-1333/1600 (AC150)		DDR3-1866 (AC135)		DDR3-2133 (AC135)	
	tVAC [pS]		tVAC [pS]		tVAC [pS]	
	Min.	Max.	Min.	Max.	Min.	Max.
> 2.0	105	-	93	-	73	-
2.0	105	-	93	-	73	-
1.5	80	-	70	-	50	-
1.0	30	-	25	-	5	-
0.9	13	-	Note	-	Note	-
0.8	Note	-	Note	-	Note	-
0.7	Note	-	-	-	-	-
0.6	Note	-	-	-	-	-
0.5	Note	-	-	-	-	-
< 0.5	Note	-	-	-	-	-

Note: Rising input signal shall become equal to or greater than VIH(AC) level and Falling input signal shall become equal to or less than VIL(AC) level.

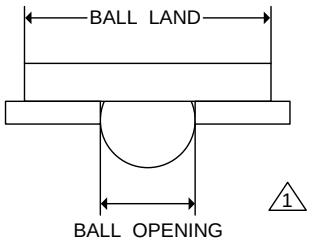
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11. PACKAGE SPECIFICATION

Package Outline VFBGA78 Ball (8x10.5 mm², ball pitch: 0.8mm) (Window BGA Type)



SYMBOL	Dimension in mm			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.00	---	---	0.0394
A1	0.25	---	0.40	0.0098	---	0.0157
b	0.40	---	0.50	0.0157	---	0.0197
D	10.40	10.50	10.60	0.4094	0.4134	0.4173
E	7.90	8.00	8.10	0.3110	0.3150	0.3189
D1	9.60 BSC.			0.3780 BSC.		
E1	6.40 BSC.			0.2519 BSC.		
eE	0.80 BSC.			0.0315 BSC.		
eD	0.80 BSC.			0.0315 BSC.		
aaa	---	---	0.15	---	---	0.0059
bbb	---	---	0.20	---	---	0.0780
ccc	---	---	0.10	---	---	0.0039
ddd	---	---	0.15	---	---	0.0059
eee	---	---	0.08	---	---	0.0031



Note:
1. Ball land: 0.5mm, Ball opening: 0.4mm,
PCB Ball land suggested ≤ 0.4mm

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12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01	Jun. 26, 2017	All	Initial formally datasheet
A02	Nov. 23, 2017	5, 7, 17, 134~138	Add CL = 5 setting
		125, 132	Refine IDD6 and IDD6ET parameters definition
		132	Add note 3 & 4 measured condition for IDD6 and IDD6ET parameters

Please note that all data and specifications are subject to change without notice.
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