*2 CHIP STACKED 8G-BIT*

# W29N08GW/ZxxBA
# 8G-BIT 1.8V
# NAND FLASH MEMORY

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# 1. GENERAL DESCRIPTION

The W29N08GW/Z (8G-bit) NAND Flash memory provides a storage solution for embedded systems with limited space, pins and power. It is ideal for code shadowing to RAM, solid state applications and storing media data such as, voice, video, text and photos. The device operates on a single 1.7V to 1.95V power supply with active current consumption as low as 13mA at 1.8V and 20uA for CMOS standby current.

The memory array totals 1,107,296,256 bytes, and organized into 8,192 erasable blocks of 135,168 bytes (67,584 words). Each block consists of 64 programmable pages of 2,112-bytes (1056 words) each. Each page consists of 2,048-bytes (1024 words) for the main data storage area and 64-bytes (32words) for the spare data area (The spare area is typically used for error management functions).

The W29N08GW/Z supports the standard NAND flash memory interface using the multiplexed 8-bit (16-bit) bus to transfer data, addresses, and command instructions. The five control signals, CLE, ALE, #CE, #RE and #WE handle the bus interface protocol. Also, the device has two other signal pins, the #WP (Write Protect) and the RY/#BY (Ready/Busy) for monitoring the device status.

# 2. FEATURES

- **Basic Features**
  - – Density : 8Gbit (2 chip stacked solution)
  - – Vcc : 1.7V to 1.95V
  - – Bus width : x8/x16
  - – Operating temperature
    - ▪ Industrial: -40°C to 85°C
    - ▪ Industrial Plus: -40°C to 105°C
- **Single-Level Cell (SLC) technology.**
- **Organization**
  - – Density: 8G-bit/1G-byte
  - – Page size
    - ▪ 2,112 bytes (2048 + 64 bytes)
    - ▪ 1,056 words (1024 + 32 words)
  - – Block size
    - ▪ 64 pages (128K + 4K bytes)
    - ▪ 64 pages (64K + 2K words)
- **Highest Performance**
  - – Read performance (Max.)
    - ▪ Random read: 25us
    - ▪ Sequential read cycle: 35ns
  - – Write Erase performance
    - ▪ Page program time: 250us(typ.)
    - ▪ Block erase time: 2ms(typ.)
  - – Endurance 100,000 Erase/Program Cycles(1)
  - – 10-years data retention
- **Command set**
  - – Standard NAND command set
  - – Additional command support
    - ▪ Copy Back
    - ▪ Two-plane operation
  - – Contact Winbond for OTP feature
  - – Contact Winbond for Block Lock feature
- **Lowest power consumption**
  - – Read: 13mA(typ.)
  - – Program/Erase: 13mA(typ.)
  - – CMOS standby: 20uA(typ.)
- **Space Efficient Packaging**
  - – 48-pin standard TSOP1
  - – 63-ball VFBGA

**Note:**

1. **Endurance specification is based on 1bit/528 byte ECC (Error Correcting Code).**


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# 3. PACKAGE TYPES AND PIN CONFIGURATIONS

W29N08GW/Z is offered in a 48-pin TSOP1 package (code S), 63-ball VFBGA package (Code B) as shown in Figure 3-1 and 3-3, respectively. Package diagrams and dimensions are illustrated in Section: Package Dimensions.

## 3.1 Pin Assignment 48 pin TSOP1

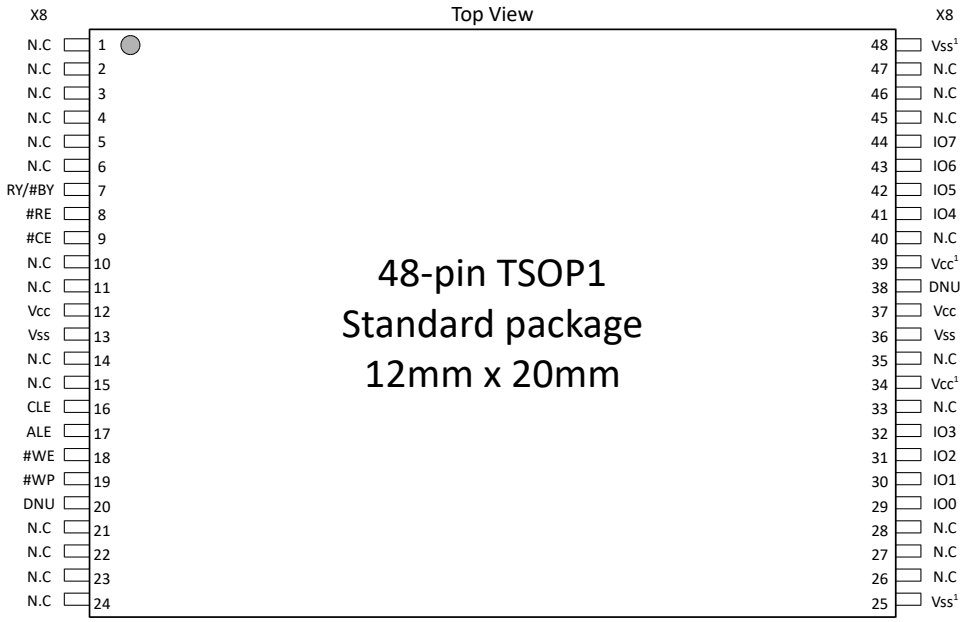



Figure 3-1 Pin Assignment 48-pin TSOP1 (Package code S)

**Note:**

1. **These pins might not be connected in the package. Winbond recommends connecting these pins to the designed external sources for ONFI compatibility.**


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## 3.2 Pin Assignment 63 ball VFBGA (x8)

Top View, ball down

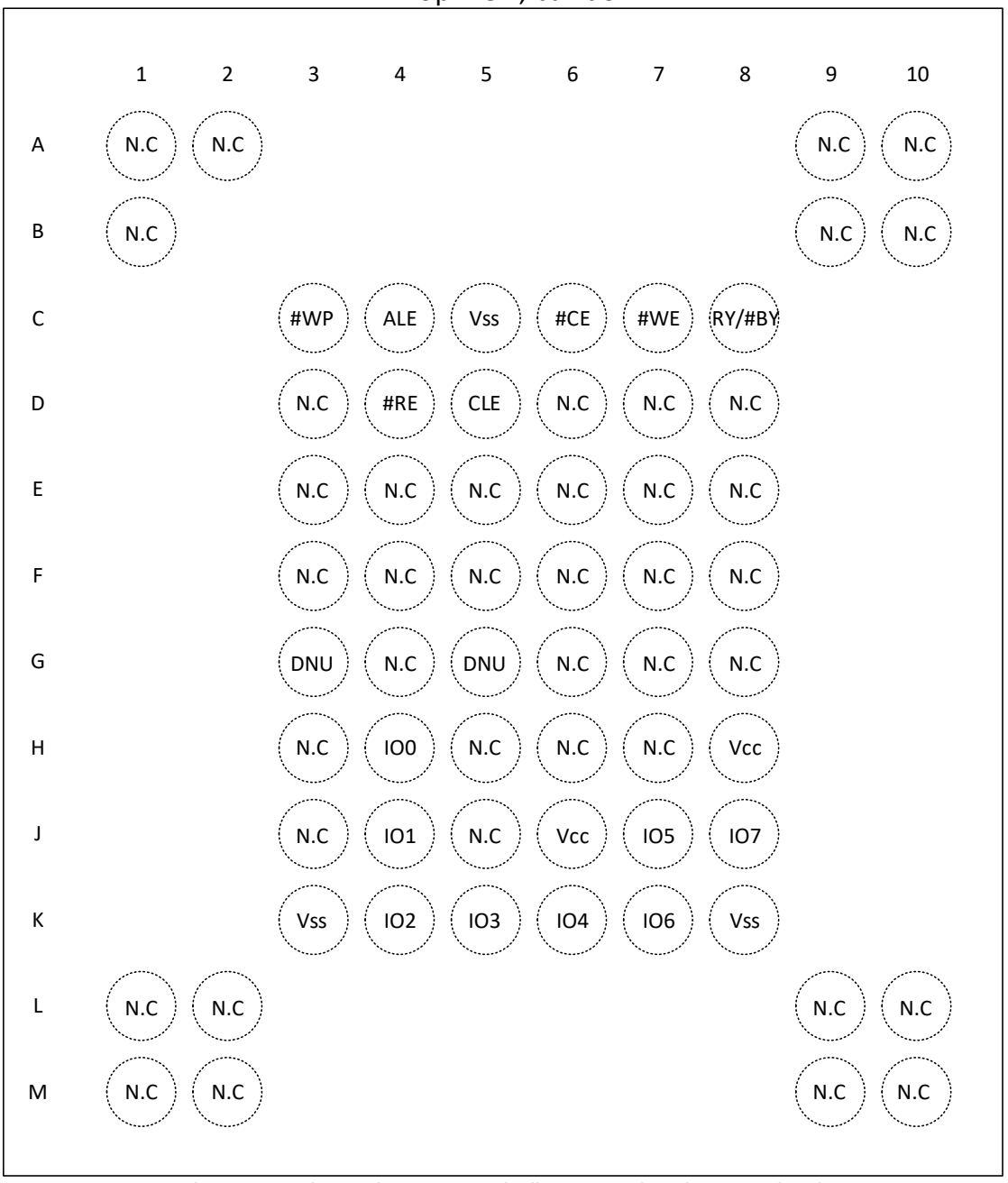



Figure 3-2 Pin Assignment 63-ball VFBGA (Package code B)


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## 3.3 Pin Assignment 63 ball VFBGA (x16)

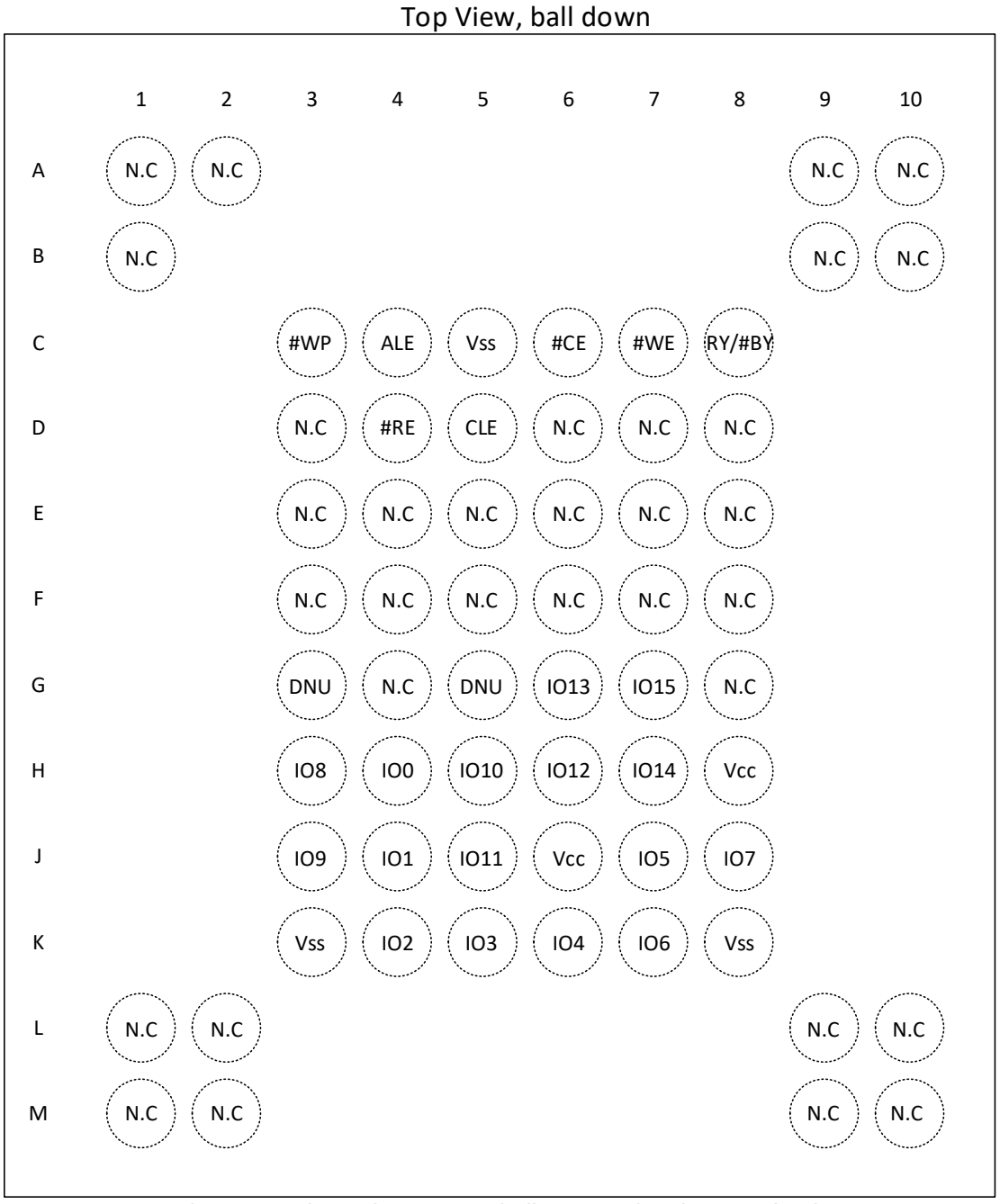



Figure 3-3 Pin Assignment 63-ball VFBGA (Package code B)


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## 3.4 Pin Descriptions

| PIN NAME | I/O | FUNCTION |
|---|---|---|
| #WP | I | Write Protect |
| ALE | I | Address Latch Enable |
| #CE | I | Chip Enable |
| #WE | I | Write Enable |
| RY/#BY | O | Ready/Busy |
| #RE | I | Read Enable |
| CLE | I | Command Latch Enable |
| I/O[0-7]<br>I/O[0-15] | I/O | Data Input/Output (x8, x16) |
| Vcc | Supply | Power supply |
| Vss | Supply | Ground |
| DNU | - | Do Not Use: DNUs must be left unconnected. |
| N.C | - | No Connect: NCs are not internally connected. They can be driven or left unconnected. |

Table 3-1 Pin Descriptions

**Note:**

1. **Connect all Vcc and Vss pins to power supply or ground. Do not leave Vcc or Vss disconnected.**


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# 4. PIN DESCRITPIONS

## 4.1 Chip Enable (#CE)

#CE pin enables and disables device operation. When #CE is high the device is disabled and the I/O pins are set to high impedance and enters into standby mode if not busy. When #CE is set low the device will be enabled, power consumption will increase to active levels and the device is ready for Read and Write operations.

## 4.2 Write Enable (#WE)

#WE pin enables the device to control write operations to input pins of the device. Such as, command instructions, addresses and data that are latched on the rising edge of #WE.

## 4.3 Read Enable (#RE)

#RE pin controls serial data output from the pre-loaded Data Register. Valid data is present on the I/O bus after the tREA period from the falling edge of #RE. Column addresses are incremented for each #RE pulse.

## 4.4 Address Latch Enable (ALE)

ALE pin controls address input to the address register of the device. When ALE is active high, addresses are latched via the I/O pins on the rising edge of #WE.

## 4.5 Command Latch Enable (CLE)

CLE pin controls command input to the command register of the device. When CLE is active high, commands are latched into the command register via I/O pins on the rising edge of #WE.

## 4.6 Write Protect (#WP)

#WP pin can be used to prevent the inadvertent program/erase to the device. When #WP pin is active low, all program/erase operations are disabled.

## 4.7 Ready/Busy (RY/#BY)

RY/#BY pin indicates the device status. When RY/#BY output is low, it indicates that the device is processing either a program, erase or read operations. When it returns to high, those operations have completed. RY/#BY pin is an open drain.

## 4.8 Input and Output (I/Ox)

I/Ox bi-directional pins are used for the following; command, address and data operations.


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## 5. SINGLE DIE BLOCK DIAGRAM

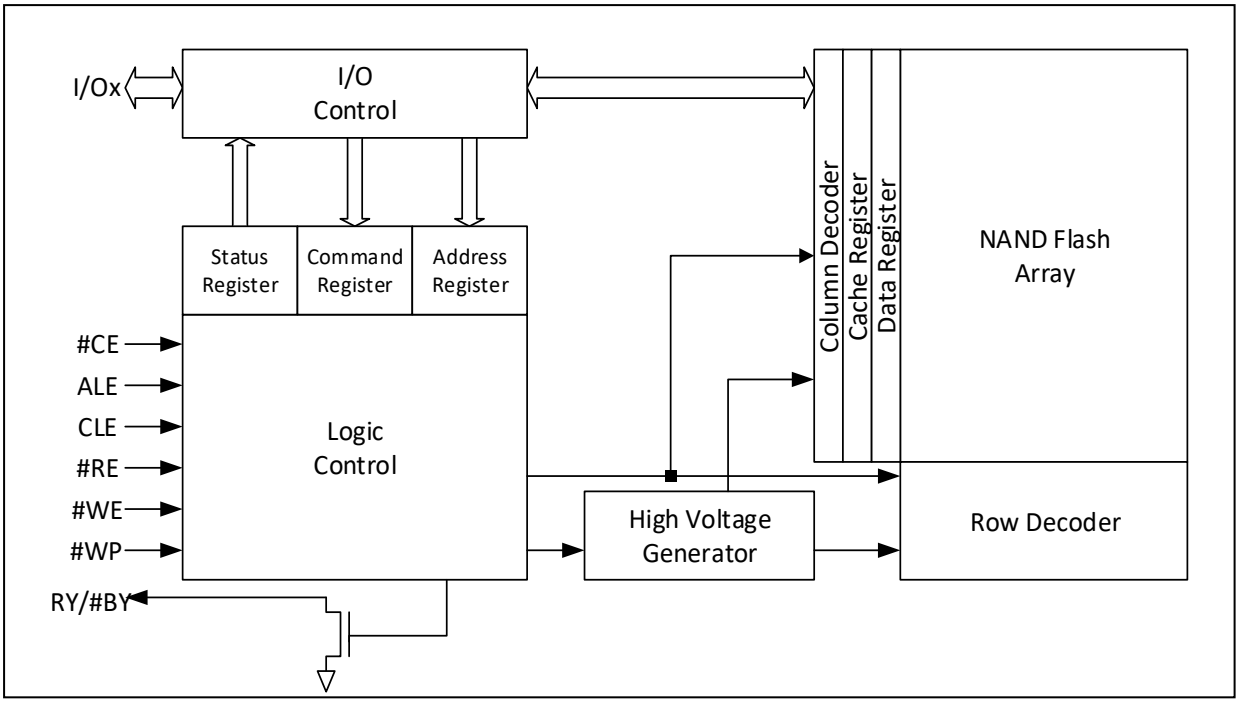



Figure 5-1 Single Die NAND Flash Memory Block Diagram


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# 6. MEMORY ARRAY ORGANIZATION

## 6.1 Single Die Array Organization (x8)

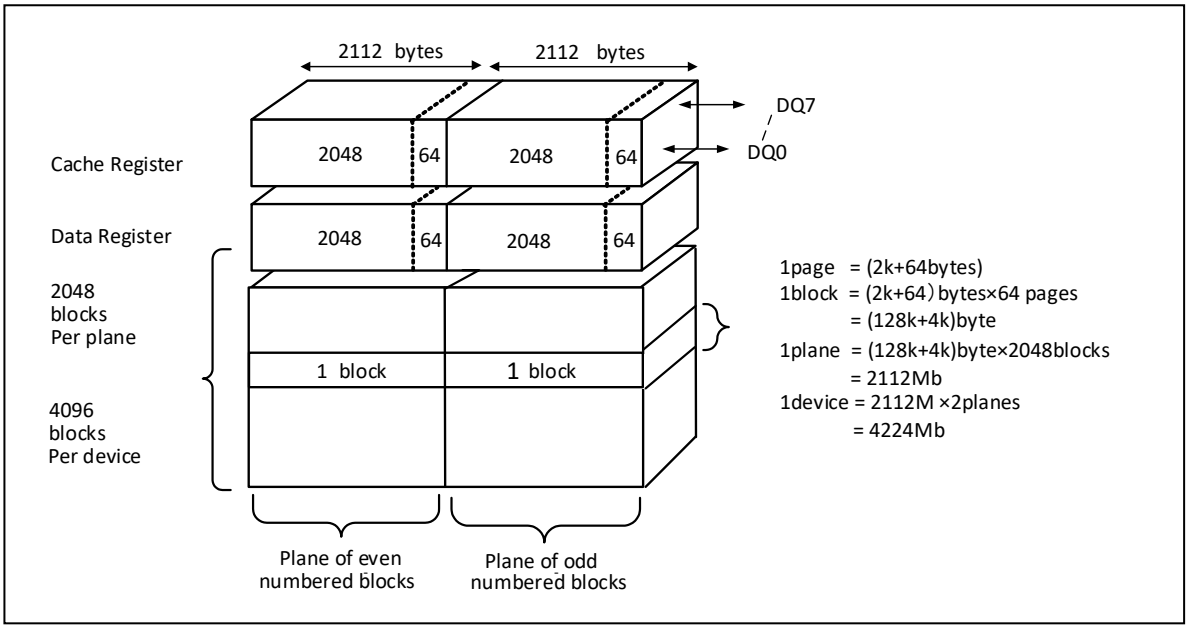



Figure 6-1 Single Die Array Organization (x8)

| | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | I/O0 |
|---|---|---|---|---|---|---|---|---|
| 1st cycle | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| 2nd cycle | L | L | L | L | A11 | A10 | A9 | A8 |
| 3rd cycle | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 |
| 4th cycle | A27 | A26 | A25 | A24 | A23 | A22 | A21 | A20 |
| 5th cycle | L | L | L | L | L | A30 | A29 | A28 |

Table 6-1 Addressing

**Notes:**

1. **"L" indicates a low condition, which must be held during the address cycle to insure correct processing.**
2. **A0 to A11 during the 1st and 2nd cycles are column addresses. A12 to A30 during the 3rd, 4th and 5th cycles are row addresses.**
3. **A18 is plane address**
4. **The device ignores any additional address inputs that exceed the device's requirement.**
5. **Do not input commands except RESET and Read Status over die address boundaries before previous operation is completed.**


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## 6.2 Single Die Array Organization (x16)

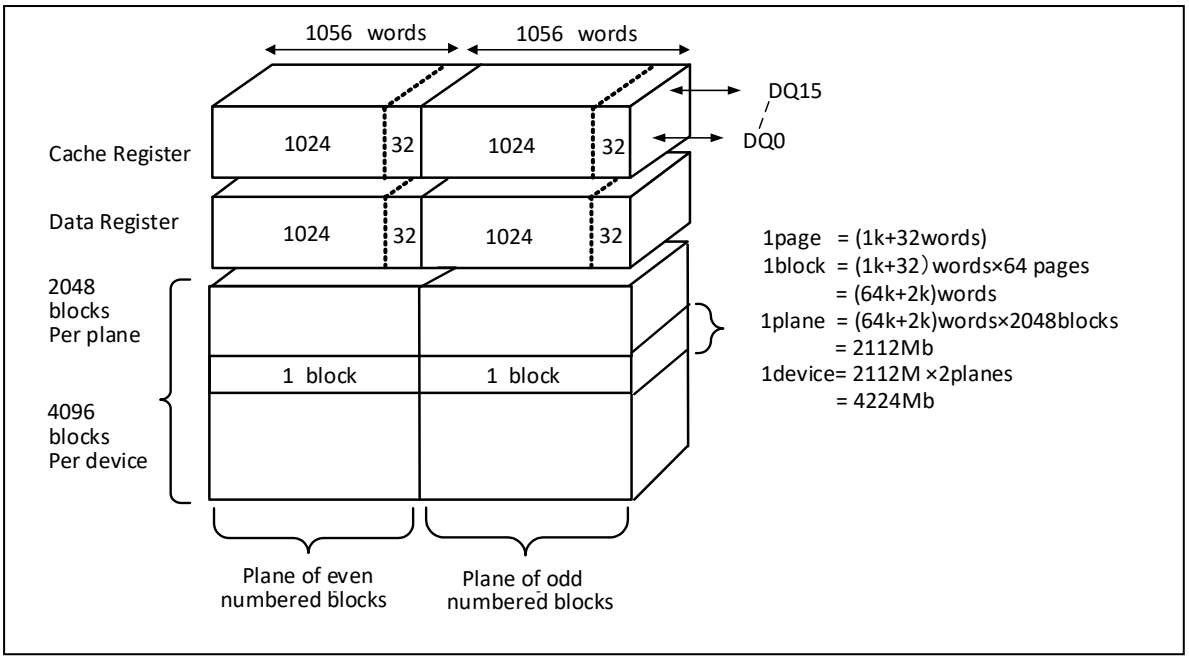



Figure 6-2 Single Die Array Organization (x16)

| | I/O[15:8] | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | I/O0 |
|---|---|---|---|---|---|---|---|---|---|
| 1st cycle | L | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| 2ndcycle | L | L | L | L | L | L | A10 | A9 | A8 |
| 3rd cycle | L | A18 | A17 | A16 | A15 | A14 | A13 | A12 | A11 |
| 4th cycle | L | A26 | A25 | A24 | A23 | A22 | A21 | A20 | A19 |
| 5th cycle | L | L | L | L | L | L | A29 | A28 | A27 |

Table 6-2 Addressing

**Notes:**

1. **"L" indicates a low condition, which must be held during the address cycle to insure correct processing.**
2. **A0 to A10 during the 1st and 2nd cycles are column addresses. A11 to A29 during the 3rd, 4th and 5th cycles are row addresses.**
3. **A17 is plane address**
4. **The device ignores any additional address inputs that exceed the device's requirement.**
5. **Do not input commands except RESET and Read Status over die address boundaries before previous operation is completed.**


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## 7. MODE SELECTION TABLE

| MODE | | CLE | ALE | #CE | #WE | #RE | #WP |
|---|---|---|---|---|---|---|---|
| Read mode | Command input | H | L | L |  | H | X |
| | Address input | L | H | L |  | H | X |
| Program Erase mode | Command input | H | L | L |  | H | H |
| | Address input | L | H | L |  | H | H |
| Data input | | L | L | L |  | H | H |
| Sequential Read and Data output | | L | L | L | H |  | X |
| During read (busy) | | X | X | X | X | H | X |
| During program (busy) | | X | X | X | X | X | H |
| During erase (busy) | | X | X | X | X | X | H |
| Write protect | | X | X | X | X | X | L |
| Standby | | X | X | H | X | X | 0V/Vcc |

Table 7-1 Mode Selection

**Notes:**

1. **"H" indicates a HIGH input level, "L" indicates a LOW input level, and "X" indicates a Don't Care Level.**
2. **#WP should be biased to CMOS HIGH or LOW for standby.**


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## 8. COMMAND TABLE

| COMMAND | 1ST CYCLE | 2ND CYCLE | 3rd CYCLE | 4th CYCLE | Acceptable during busy |
|---|---|---|---|---|---|
| PAGE READ | 00h | 30h | | | |
| READ for COPY BACK | 00h | 35h | | | |
| READ ID | 90h | | | | |
| READ STATUS | 70h | | | | Yes |
| RESET | FFh | | | | Yes |
| PAGE PROGRAM | 80h | 10h | | | |
| PROGRAM for COPY BACK | 85h | 10h | | | |
| BLOCK ERASE | 60h | D0h | | | |
| RANDOM DATA INPUT*1 | 85h | | | | |
| RANDOM DATA OUTPUT*1 | 05h | E0h | | | |
| READ PARAMETER PAGE | ECh | | | | |
| READ UNIQUE ID | EDh | | | | |
| GET FEATURES | EEh | | | | |
| SET FEATURES | EFh | | | | |
| READ STATUS ENHANCED | 78h | | | | Yes |
| TWO PLANE READ PAGE | 00h | 00h | 30h | | |
| TWO PLANE READ FOR COPY BACK | 00h | 00h | 35h | | |
| TWO PLANE RANDOM DATA READ | 06h | E0h | | | |
| TWO PLANE PROGRAM(TRADITIONAL) | 80h | 11h | 81h | 10h | |
| TWO PLANE PROGRAM(ONFI) | 80h | 11h | 80h | 10h | |
| TWO PLANE PROGRAM FOR COPY BACK(TRADITIONAL) | 85h | 11h | 81h | 10h | |
| TWO PLANE PROGRAM FOR COPY BACK(ONFI) | 85h | 11h | 85h | 10h | |
| TWO PLANE BLOCK ERASE(TRADITIONAL) | 60h | 60h | D0h | | |
| TWO PLANE BLOCK ERASE(ONFI) | 60h | D1h | 60h | D0h | |

Table 8-1 Command Table

**Notes:**

1. **RANDOM DATA INPUT and RANDOM DATA OUTPUT command is only to be used within a page.**
2. **Any commands that are not in the above table are considered as undefined and are prohibited as inputs.**
3. **Do not cross plane address boundaries when using Copy Back Read and Program for copy back.**


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# 9. DEVICE OPERATIONS

## 9.1 READ operation

### 9.1.1 PAGE READ (00h-30h)

When the device powers on, 00h command is latched to command register. Therefore, system only issues five address cycles and 30h command for initial read from the device. This operation can also be entered by writing 00h command to the command register, and then write five address cycles, followed by writing 30h command. After writing 30h command, the data is transferred from NAND array to Data Register during tR. Data transfer progress can be done by monitoring the status of the RY/#BY signal output. RY/#BY signal will be LOW during data transfer. Also, there is an alternate method by using the READ STATUS (70h) command. If the READ STATUS command is issued during read operation, the Read (00h) command must be re-issued to read out the data from Data Register. When the data transfer is complete, RY/#BY signal goes HIGH, and the data can be read from Data Register by toggling #RE. Read is sequential from initial column address to the end of the page. (See Figure 9-1)

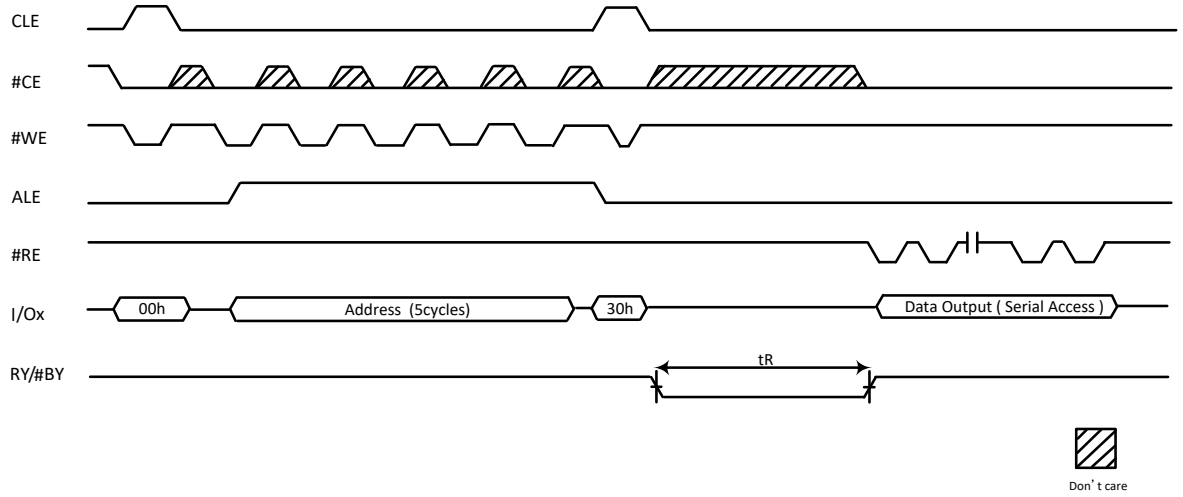



Figure 9-1 Page Read Operations

### 9.1.2 TWO PLANE READ (00h-00h-30h)

TWO PLANE READ (00h-00h-30h) transfers two pages data from the NAND array to the data registers. Each page address have to be indicated different plane address.

To set the TWO PLANE READ mode, write the 00h command to the command register, and then write five address cycles for plane 0. Secondly, write the 00h command to the command register, and five address cycles for plane 1. Finally, the 30h command is issued. The first-plane and second-plane addresses must be identical for all of issued address except plane address.

After the 30h command is written, page data is transferred from both planes to their respective data registers in tR. RY/#BY goes LOW While these are transfered,. When the transfers are complete, RY/#BY goes HIGH. To read out the data, at first, system writes TWO PLANE RAMDOM DATA READ (06h-E0h) command to select a plane, next, repeatedly pulse #RE to read out the data from selected plane. To change the plane address, issues TWO PLANE RANDOM DATA READ (06h-E0h)


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command to select the another plane address, then repeatedly pulse #RE to read out the data from the selected plane data register.

Alternatively, data transfers can be monitored by the READ STATUS (70h). When the transfers are complete, status register bit 6 is set to 1. To read data from the first of the two planes even when READ STATUS ENHANCED (78h) command is used, the system must issue the TWO PLANE RANDOM DATA READ (06h-E0h) command at first and pulse #RE repeatedly.

Write a TWO PLANE RANDOM DATA READ (06h-E0h) command to select the other plane ,after the data cycle is complete. pulse #RE repeatedly to output the data beginning at the specified column address. During TWO PLANE READ operation,the READ STATUS ENHANCED (78h) command is prohibited .

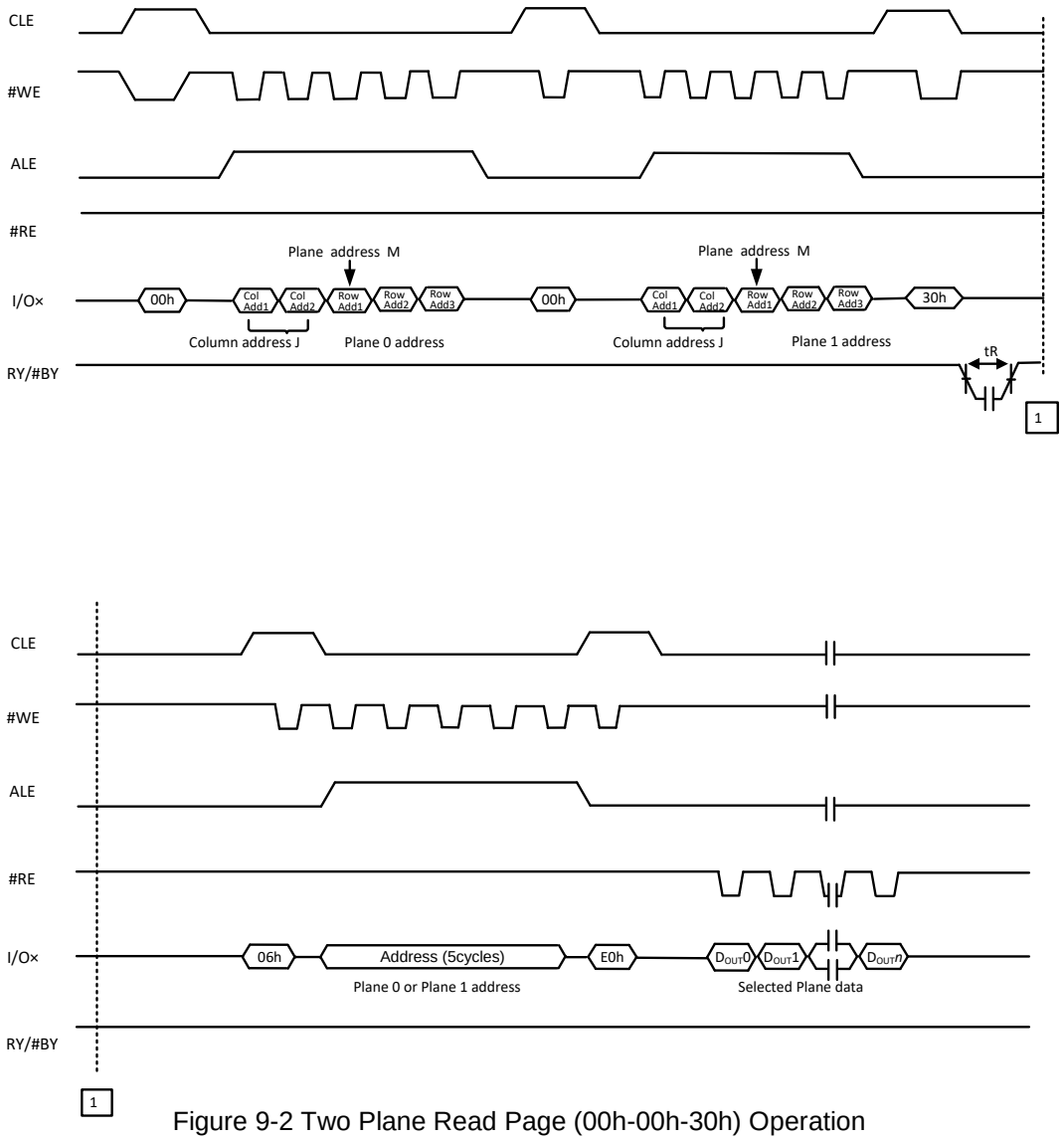



Figure 9-2 Two Plane Read Page (00h-00h-30h) Operation


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### 9.1.3 RANDOM DATA OUTPUT (05h-E0h)

The RANDOM DATA OUTPUT allows the selection of random column addresses to read out data from a single or multiple of addresses. The use of the RANDOM DATA OUTPUT command is available after the PAGE READ (00h-30h) sequence by writing the 05h command following by the two cycle column address and then the E0h command. Toggling #RE will output data sequentially. The RANDOM DATA OUTPUT command can be issued multiple times, but limited to the current loaded page.

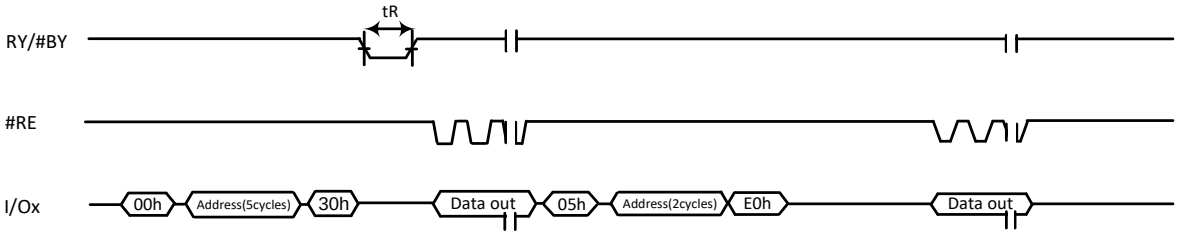



Figure 9-3 Random Data Output

#### 9.1.3.1. TWO PLANE RANDOM DATA OUTPUT (06h-E0h)

TWO PLANE RANDOM DATA READ (06h-E0h) command can indicate to specified plane and column address on data register . This command is accepted by a device when it is ready.

Issuing 06h to the command register, two column address cycles, three row address cycles, E0h are followed, this enables data output mode on the address device's data register at the specified column address. After the E0h command , the host have to wait at least tWHR before requesting data output. The selected device is in data output mode until another valid command is issued.

The TWO PLANE RANDOM DATA READ (06h-E0h) command is used to select the data register to be enabled for data output. When the data output is complete on the selected plane, the command can be issued again to start data output on another plane.

If there is a need to update the column address without selecting a new data register, the RANDOM DATA READ (05h-E0h) command can be used instead.

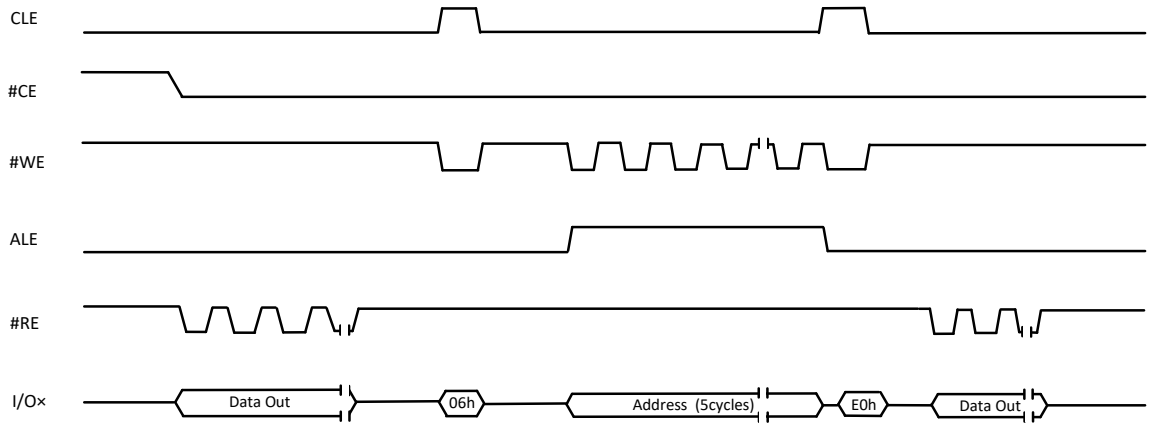



Figure 9-4 Two Plane Random Data Read (06h-E0h) Operation


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### 9.1.4 READ ID (90h)

READ ID command is comprised of two modes determined by the input address, device (00h) or ONFI (20h) identification information. To enter the READ ID mode, write 90h to the Command Register followed by a 00h address cycle, then toggle #RE for 5 single byte cycles, W29N08GW/Z. The pre-programmed code includes the Manufacturer ID, Device ID, and Product-Specific Information (see Table 9.1). If the READ ID command is followed by 20h address, the output code includes 4 single byte cycles of ONFI identifying information (See Table 9.2). The device remains in the READ ID Mode until the next valid command is issued.

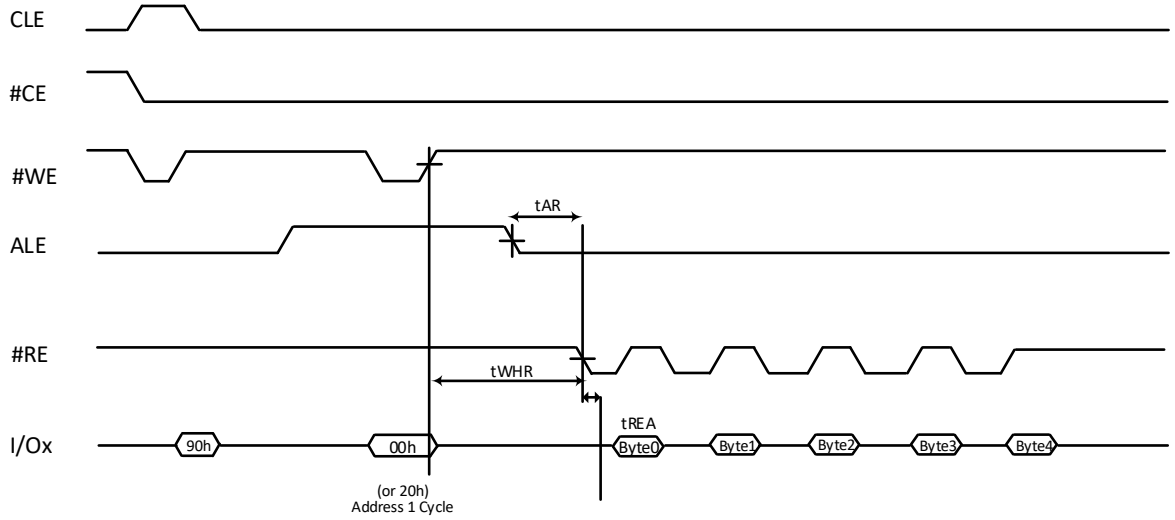



Figure 9-5 Read ID

| # of Byte/Cycles | 1st Byte/Cycle | 2nd Byte/Cycle | 3rd Byte/Cycle | 4th Byte/Cycle | 5th Byte/Cycle |
|---|---|---|---|---|---|
| W29N08GZ | EFh | A3h | 91h | 15h | 58h |
| W29N08GW | EFh | B3h | 91h | 55h | 58h |
| Description | MFR ID | Device ID | Cache Programming not Supported | Page Size:2KB<br>Spare Area Size:64B<br>BLK Size w/o Spare:128KB<br>Organized:x8 or x16<br>Serial Access:25ns | |

x16 device : the ID is outputted at word units, and defined lower-byte (IO0-7). ID table shows only lower-byte ID.

Table 9-1 Device ID and Configuration Codes for Address 00h

| # of Byte/Cycles | 1st Byte/Cycle | 2nd Byte/Cycle | 3rd Byte/Cycle | 4th Byte/Cycle |
|---|---|---|---|---|
| Code | 4Fh | 4Eh | 46h | 49h |

Table 9-2 ONFI Identifying Codes for Address 20h


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### 9.1.5 READ PARAMETER PAGE (ECh)

READ PARAMETER PAGE can read out the device's parameter data structure, such as, manufacturer information, device organization, timing parameters, key features, and other pertinent device parameters. The data structure is stored with at least three copies in the device's parameter page. Figure 9-9 shows the READ PARAMETER PAGE timing. The RANDOM DATA OUTPUT (05h-E0h) command is supported during data output.

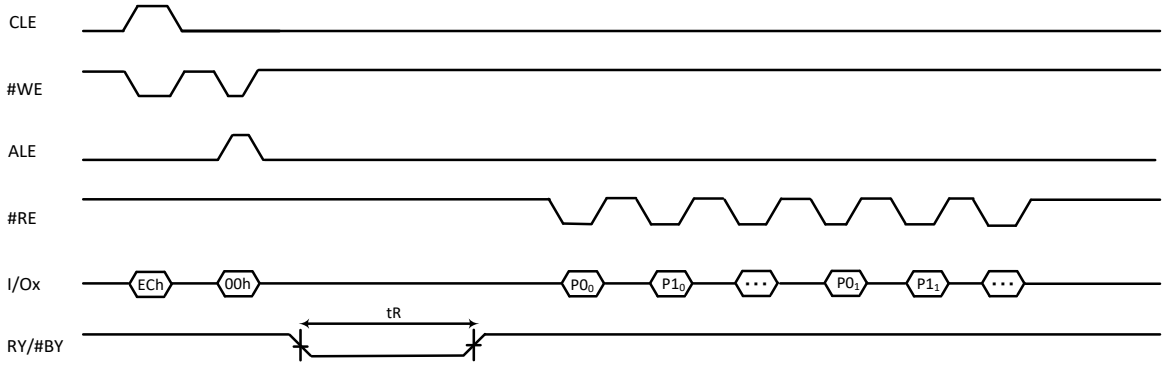



Figure 9-6 Read Parameter Page

| Byte | Description | | Value |
|---|---|---|---|
| 0-3 | Parameter page signature | | 4Fh, 4Eh, 46h, 49h |
| 4-5 | Revision number | | 02h, 00h |
| 6-7 | Features supported | W29N08GZ | 18h,00h |
| | | W29N08GW | 19h,00h |
| 8-9 | Optional commands supported | | 3Ch,00h |
| 10-31 | Reserved | | 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h |
| 32-43 | Device manufacturer | | 57h, 49h, 4Eh, 42h, 4Fh, 4Eh, 44h, 20h, 20h, 20h, 20h, 20h |
| 44-63 | Device model | W29N08GZ | 57h,32h,39h,4Eh,30h,38h,47h,5Ah,20h,20h,20h,20h, 20h,20h,20h,20h,20h,20h,20h,20h,20h |
| | | W29N08GW | 57h,32h,39h,4Eh,30h,38h,47h,57h,20h,20h,20h,20h, 20h,20h,20h,20h,20h,20h,20h,20h,20h |
| 64 | Manufacturer ID | | EFh |
| 65-66 | Date code | | 00h, 00h |
| 67-79 | Reserved | | 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h |
| 80-83 | # of data bytes per page | | 00h, 08h, 00h, 00h |


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| Byte | Description | | Value |
|---|---|---|---|
| 84-85 | # of spare bytes per page | | 40h, 00h |
| 86-89 | # of data bytes per partial page | | 00h, 02h, 00h, 00h |
| 90-91 | # of spare bytes per partial page | | 10h, 00h |
| 92-95 | # of pages per block | | 40h, 00h, 00h, 00h |
| 96-99 | # of blocks per unit | | 00h, 10h, 00h, 00h |
| 100 | # of logical units | | 02h |
| 101 | # of address cycles | | 23h |
| 102 | # of bits per cell | | 01h |
| 103-104 | Bad blocks maximum per unit | | 50h, 00h |
| 105-106 | Block endurance | | 01h, 05h |
| 107 | Guaranteed valid blocks at beginning of target | | 01h |
| 108-109 | Block endurance for guaranteed valid blocks | | 00h, 00h |
| 110 | # of programs per page | | 04h |
| 111 | Partial programming attributes | | 00h |
| 112 | # of ECC bits | | 01h |
| 113 | # of interleaved address bits | | 01h |
| 114 | Interleaved operation attributes | | 00h |
| 115-127 | Reserved | | 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h |
| 128 | I/O pin capacitance | | 0Ah |
| 129-130 | Timing mode support | | 1Fh, 00h |
| 131-132 | Program cache timing | | 00h, 00h |
| 133-134 | Maximum page program time | | BCh, 02h |
| 135-136 | Maximum block erase time | | 10h, 27h |
| 137-138 | Maximum random read time | | 19h, 00h |
| 139-140 | tCCS minimum | | 46h, 00h |
| 141-163 | Reserved | | 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h |
| 164-165 | Vendor specific revision # | | 01h, 00h |
| 166-253 | Vendor specific | | 00h |
| 254-255 | Integrity CRC | W29N08GZ | EDh, C6h |
| | | W29N08GW | E3h, 7Ch |


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| Byte | Description | Value |
|---|---|---|
| 256-511 | Value of bytes 0-255 | |
| 512-767 | Value of bytes 0-255 | |
| >767 | Additional redundant parameter pages | |

x16 device : the ID is outputted at word units, and defined lower-byte (IO0-7). ID table shows only lower-byte ID.

Table 9-3 Parameter Page Output Value

### 9.1.6 READ STATUS (70h)

The W29N08GW/Z has an 8-bit Status Register which can be read during device operation. Refer to Table 9.4 for specific Status Register definitions. After writing 70h command to the Command Register, read cycles will only read from the Status Register. The status can be read from I/O[7:0] outputs, as long as #CE and #RE are LOW. Note; #RE does not need to be toggled for Status Register read. The Command Register remains in status read mode until another command is issued. To change to normal read mode, issue the PAGE READ (00h) command. After the PAGE READ command is issued, data output starts from the initial column address.

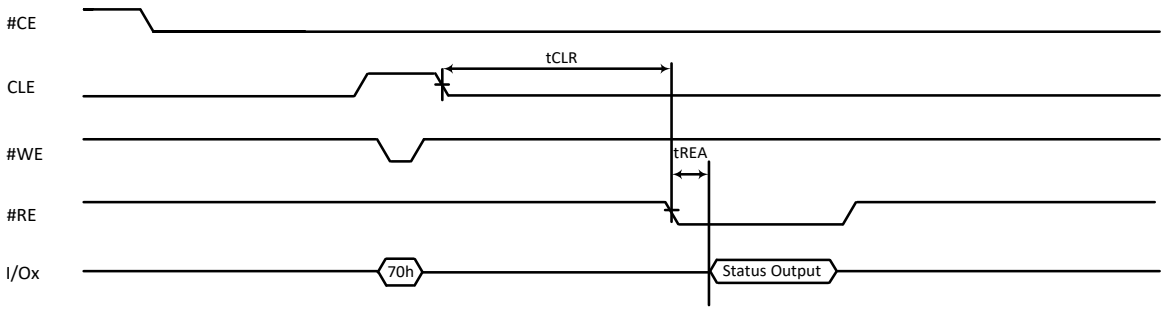



Figure 9-7 Read Status Operation


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| SR bit | Page Read | Page Program | Block Erase | Definition |
|---|---|---|---|---|
| I/O 0 | Not Use | Pass/Fail | Pass/Fail | 0=Successful Program/Erase<br>1=Error in Program/Erase |
| I/O 1 | Not Use | Not Use | Not Use | 0=Successful Program<br>1=Error in Program |
| I/O 2 | Not Use | Not Use | Not Use | 0 |
| I/O 3 | Not Use | Not Use | Not Use | 0 |
| I/O 4 | Not Use | Not Use | Not Use | 0 |
| I/O 5 | Ready/Busy | Ready/Busy | Ready/Busy | Ready = 1<br>Busy = 0 |
| I/O 6 | Ready/Busy | Ready/Busy | Ready/Busy | Ready = 1<br>Busy = 0 |
| I/O 7 | Write Protect | Write Protect | Write Protect | Unprotected = 1<br>Protected = 0 |

Table 9-4 Status Register Bit Definition

### 9.1.7 READ STATUS ENHANCED (78h)

The READ STATUS ENHANCED (78h) command returns the status of the addressed plane on a target even when it is busy (SR BIT 6 = 0).

Writing 78h to the command register, followed by three row address cycles containing the page, plane and block addresses that is same as executed addresses, puts the device into read status mode. The device stays in this mode until another valid command is issued

The device status is returned when the host requests data output. The SR BIT 6 and SR bit 5 bits of the status register are shared for all planes on the device. The SR BIT 1 and SR BIT 0 (SR bit0) bits are specific to the plane specified in the row address.

The READ STATUS ENHANCED (78h) command also enables the device for data output. To begin data output following a READ operation after the device is ready (SR BIT 6 = 1), issue the READ MODE (00h) command, then begin data output. If the host needs to change the data register that will output data, use the TWO PLANE RANDOMDATA READ (06h-E0h) command after the device is ready


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Use of the READ STATUS ENHANCED (78h) command is prohibited when OTP mode is enabled. It is also prohibited following some of the other reset, identification.

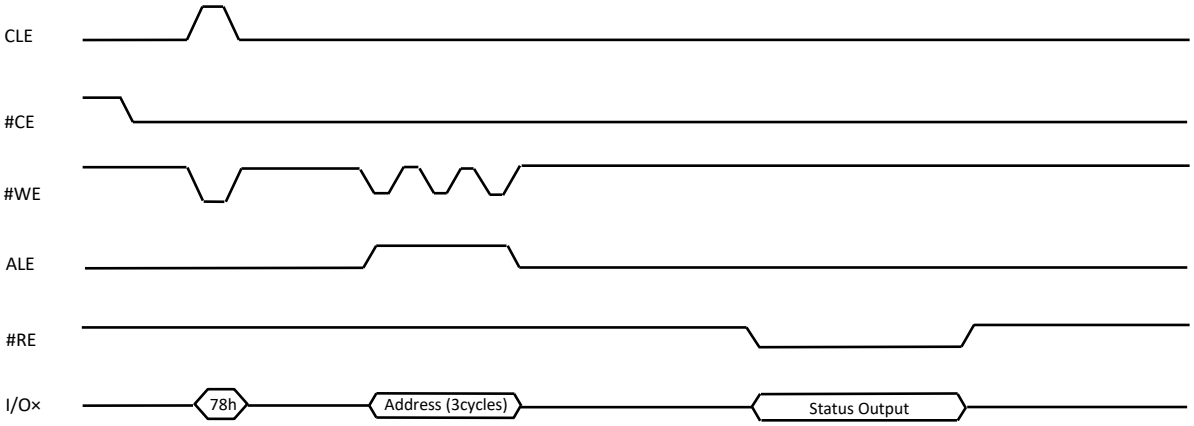



Figure 9-8 Read Status Enhanced (78h) Operation


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### 9.1.8 READ UNIQUE ID (EDh)

The W29N08GW/Z NAND Flash device has a method to uniquely identify each NAND Flash device by using the READ UNIQUE ID command. The format of the ID is limitless, but the ID for every NAND Flash device manufactured, will be guaranteed to be unique.

Numerous NAND controllers typically use proprietary error correction code (ECC) schemes. In these cases Winbond cannot protect unique ID data with factory programmed ECC. However, to ensure data reliability, Winbond will program the NAND Flash devices with 16 bytes of unique ID code, starting at byte 0 on the page, immediately followed by 16 bytes of the complement of that unique ID. The combination of these two actions is then repeated 16 times. This means the final copy of the unique ID will resides at location byte 511. At this point an XOR or exclusive operation can be performed on the first copy of the unique ID and its complement. If the unique ID is good, the results should yield all the bits as 1s. In the event that any of the bits are 0 after the XOR operation, the procedure can be repeated on a subsequent copy of the unique ID data.

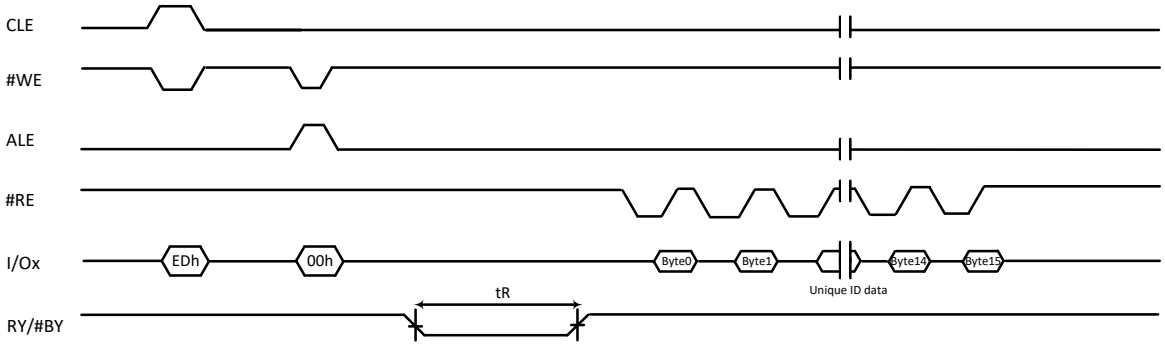



Figure 9-9 Read Unique ID


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## 9.2 PROGRAM operation

### 9.2.1 PAGE PROGRAM (80h-10h)

The W29N08GW/Z Page Program command will program pages sequentially within a block, from the lower order page address to higher order page address. Programming pages out of sequence is prohibited. The W29N08GW/Z supports partial-page programming operations up to 4 times before an erase is required if partitioning a page. Note; programming a single bit more than once without first erasing it is not supported.

### 9.2.2 SERIAL DATA INPUT (80h)

Page Program operation starts with the execution of the Serial Data Input command (80h) to the Command Register, following next by inputting five address cycles and then the data is loaded. Serial data is loaded to Data Register with each #WE cycle. The Program command (10h) is written to the Command Register after the serial data input is finished. At this time the internal write state controller automatically executes the algorithms for program and verifies operations. Once the programming starts, determining the completion of the program process can be done by monitoring the RY/#BY output or the Status Register Bit 6, which will follow the RY/#BY signal. RY/#BY will stay LOW during the internal array programming operation during the period of (tPROG). During page program operation, only two commands are available, READ STATUS (70h) and RESET (FFh). When the device status goes to the ready state, Status Register Bit 0 (I/O0) indicates whether the program operation passed (Bit0=0) or failed (Bit0=1), (see Figure 9-13). The Command Register remains in read status mode until the next command is issued.

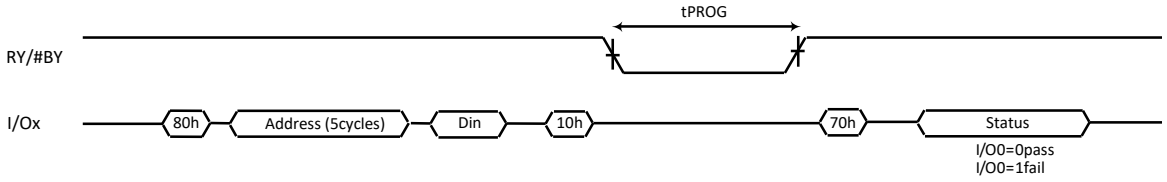



Figure 9-10 Page Program


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### 9.2.3 RANDOM DATA INPUT (85h)

After the Page Program (80h) execution of the initial data has been loaded into the Data Register, if the need for additional writing of data is required, using the RANDOM DATA INPUT (85h) command can perform this function to a new column address prior to the Program (10h) command. The RANDOM DATA INPUT command can be issued multiple times in the same page (See Figure 9-14).

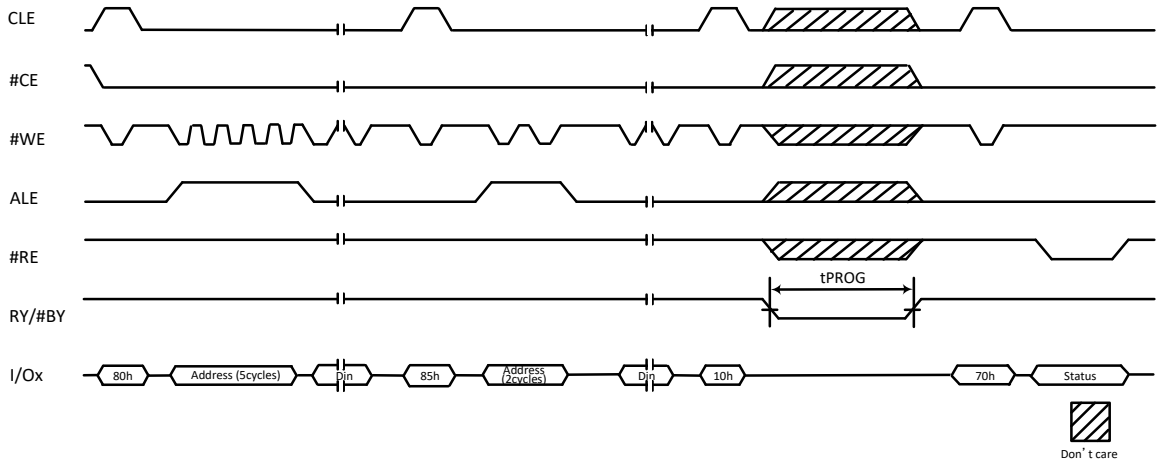



Figure 9-11 Random Data Input

### 9.2.4 TWO PLANE PAGE PROGRAM

TWO PLANE PAGE PROGRAM command make it possible for host to input data to the addressed plane's data register and queue the data register to be moved to the NAND Flash array.

This command can be issued several times. Each time a new plane address is specified that plane is also queued for data transfer. To input data for the final plane and to begin the program operation for all previously queued planes, either the PAGE PROGRAM command has to be issued. All of the queued planes will move the data to the NAND Flash array. when it is ready (SR BIT 6 = 1),this command is accepted.

At the block and page address is specified, input a page to the data register and queue it to be moved to the NAND Flash array ,the 80h is issued to the command register. Unless this command has been preceded by a TWO PLANE PAGE PROGRAM command, issuing the 80h to the command register clears all of the data registers' contents on the selected target. Write five address cycles containing the column address and row address; data input cycles follow. Serial data is input beginning at the column address specified. At any time, while the data input cycle, the RANDOM DATA INPUT (85h) command can be issued. When data input is complete, write 11h to the command register. The device will go busy (SR BIT 6 = 0, SR BIT 5 = 0) for tDBSY.

To ascertain the progress of tDBSY, the host can monitor the target's RY/#BY signal or, the status operations (70h, 78h) can be used alternatively,. When the device status shows that it is ready (SR BIT 6 = 1), additional TWO PLANE PAGE PROGRAM commands can be issued to queue additional planes for data transfer, then, the PAGE PROGRAM commands can be issued.

When the PAGE PROGRAM command is used as the final command of a two plane program operation, data is transferred from the data registers to the NAND Flash array for all of the addressed


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planes during tPROG. When the device is ready (SR BIT 6 = 1, SR BIT 5 = 1), the host should check the status of the SR BIT 0 for each of the planes to verify that programming completed successfully.

When system issues TWO PLANE PAGE PROGRAM, PAGE PROGRAM, READ STATUS (70h) command can confirm whether the operation(s) passed or failed. If the status after READ STATUS (70h) command indicates an error (SR BIT 0 = 1 and/or SR BIT 1 = 1), READ STATUS ENHANCED (78h) command can be determined which plane is failed.

TWO PLANE PROGRAM commands require five-cycle addresses, one address indicates the operational plane. These addresses are subject to the following requirements:

• The column address bits must be valid address for each plane

• The plane select bit, A18, must be set to “L” for 1st address input, and set to “H” for 2nd address input.

• The page address (A17-A12) and block address (A29-A19) of first input are don’t care. It follows secondary inputted page address and block address.

Two plane operations must be same type operation across the planes; for example, it is not possible to perform a PROGRAM operation on one plane with an ERASE operation on another.

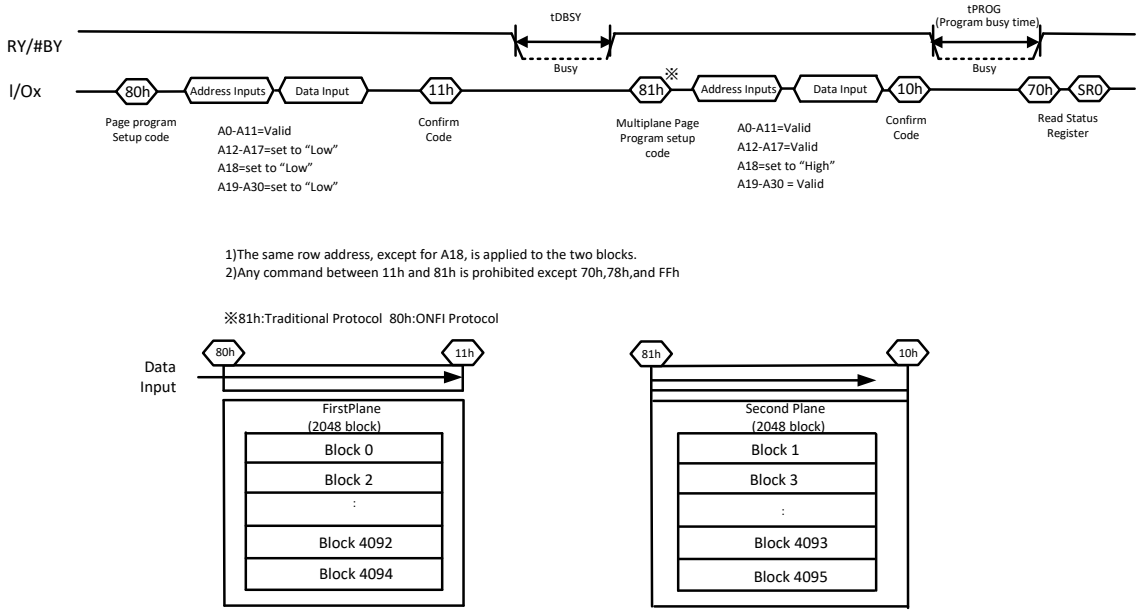



Figure 9-12 Two Plane Page Program


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## 9.3 COPY BACK operation

Copy Back operations require two command sets. Issue a READ for COPY BACK (00h-35h) command first, then the PROGRAM for COPY BACK (85h-10h) command. Copy back operations are only supported within a same plane.

### 9.3.1 READ for COPY BACK (00h-35h)

The READ for COPY BACK command is used together with the PROGRAM for COPY BACK (85h-10h) command. To start execution, READ for COPY BACK (00h) command is written to the Command Register, followed by the five cycles of the source page address. To start the transfer of the selected page data from the memory array to the Data Register, write the 35h command to the Command Register.

After execution of the READ for COPY BACK command sequence and RY/#BY returns to HIGH marking the completion of the operation, the transferred data from the source page into the Data Register may be read out by toggling #RE. Data is output sequentially from the column address that was originally specified with the READ for COPY BACK command. RANDOM DATA OUTPUT (05h-E0h) commands can be issued multiple times without any limitation after READ for COPY BACK command has been executed (see Figures 9-19 and 9-20).

At this point the device is in ready state to accept the PROGRAM for COPY BACK command.

### 9.3.2 PROGRAM for COPY BACK (85h-10h)

After the READ for COPY BACK command operation has been completed and RY/#BY goes HIGH, the PROGRAM for COPY BACK command can be written to the Command Register. The command results in the transfer of data from the Data Register to the Data Register, then internal operations start programming of the new destination page. The sequence would be, write 85h to the Command Register, followed by the five cycle destination page address to the NAND array. Next write the 10h command to the Command Register; this will signal the internal controller to automatically start to program the data to new destination page. During this programming time, RY/#BY will LOW. The READ STATUS command can be used instead of the RY/#BY signal to determine when the program is complete. When Status Register Bit 6 (I/O6) equals to “1”, Status Register Bit 0 (I/O0) will indicate if the operation was successful or not.

The RANDOM DATA INPUT (85h) command can be used during the PROGRAM for COPY BACK command for modifying the original data. Once the data is copied into the Data Register using the READ for COPY BACK (00h-35h) command, follow by writing the RANDOM DATA INPUT (85h) command, along with the address of the data to be changed. The data to be changed is placed on the external data pins. This operation copies the data into the Data Register. Once the 10h command is written to the Command Register, the original data and the modified data are transferred to the Data Register, and programming of the new page commences. The RANDOM DATA INPUT command can be issued numerous times without limitation, as necessary before starting the programming sequence with 10h command.

Since COPY BACK operations do not use external memory and the data of source page might include a bit errors, a competent ECC scheme should be developed to check the data before programming data to a new destination page.


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### 9.3.3 TWO PLANE READ for COPY BACK

To improve read through rate, TWO PLANE READ for COPY BACK operation is copied data concurrently from one or two plane to the specified data registers.

TWO PLANE PROGRAM for COPY BACK command can move the data in two pages from the data registers to different pages. This operation improves system performance than PROGRAM for COPY BACK operation.

### 9.3.4 TWO PLANE PROGRAM for COPY BACK

Function of TWO PLANE PROGRAM for COPY BACK command is equal to TWO-PLANE PAGE PROGRAM command, except that when 85h is written to the command register, then data register contents are not cleared. Refer to TWO-PLANE PAGE PROGRAM for more details features.


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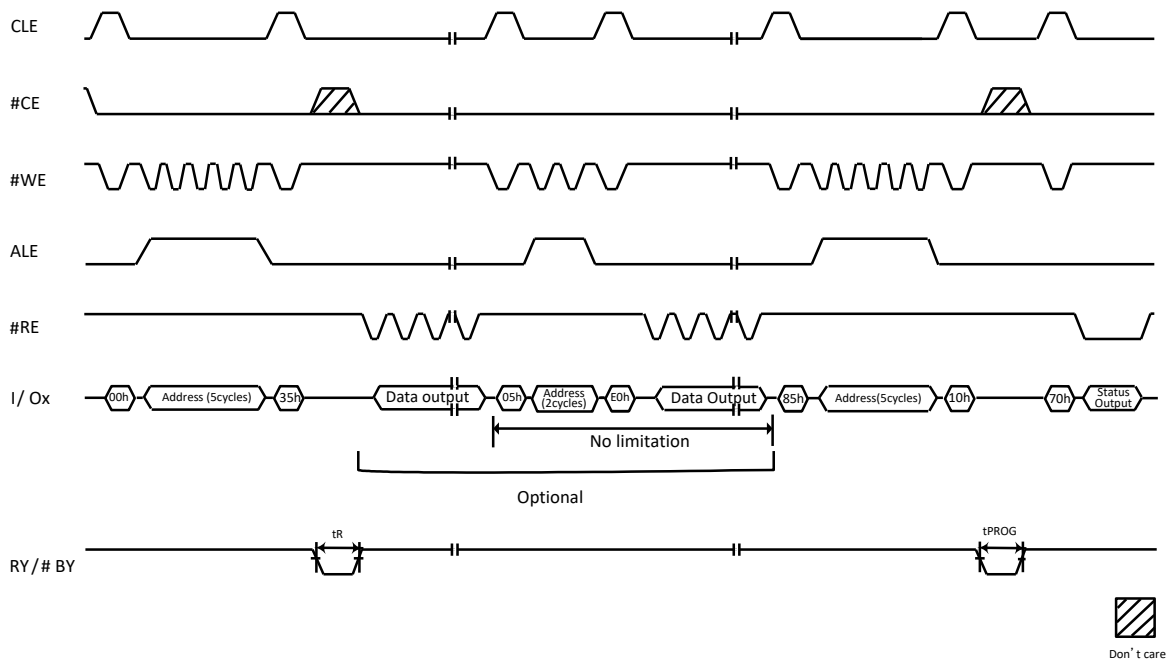



Figure 9-13 Program for Copy Back Operation

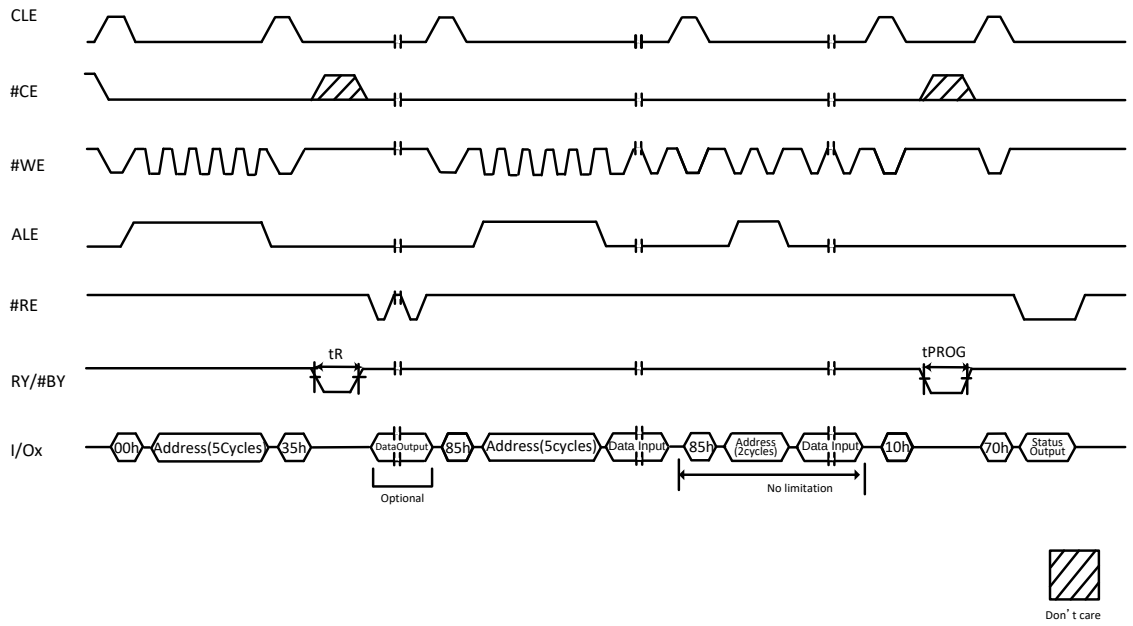



Figure 9-14 Copy Back Operation with Random Data Input


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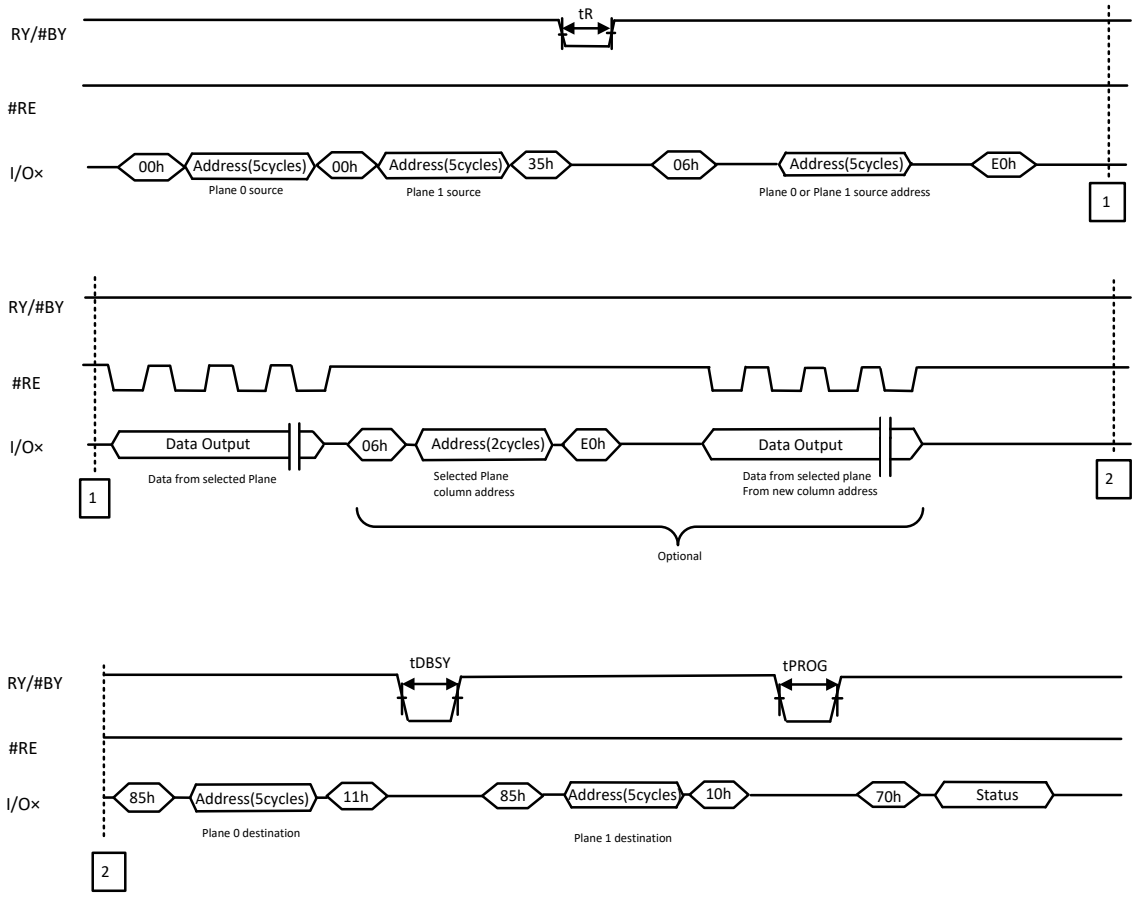



Figure 9-15 Two Plane Copy Back

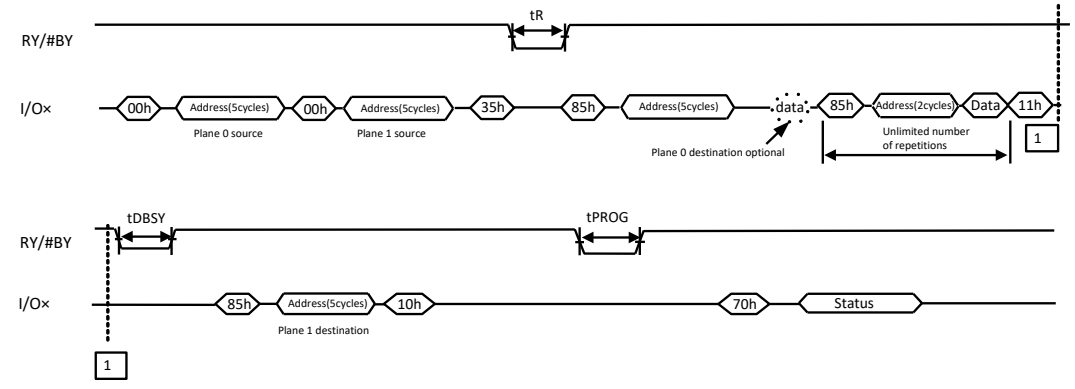
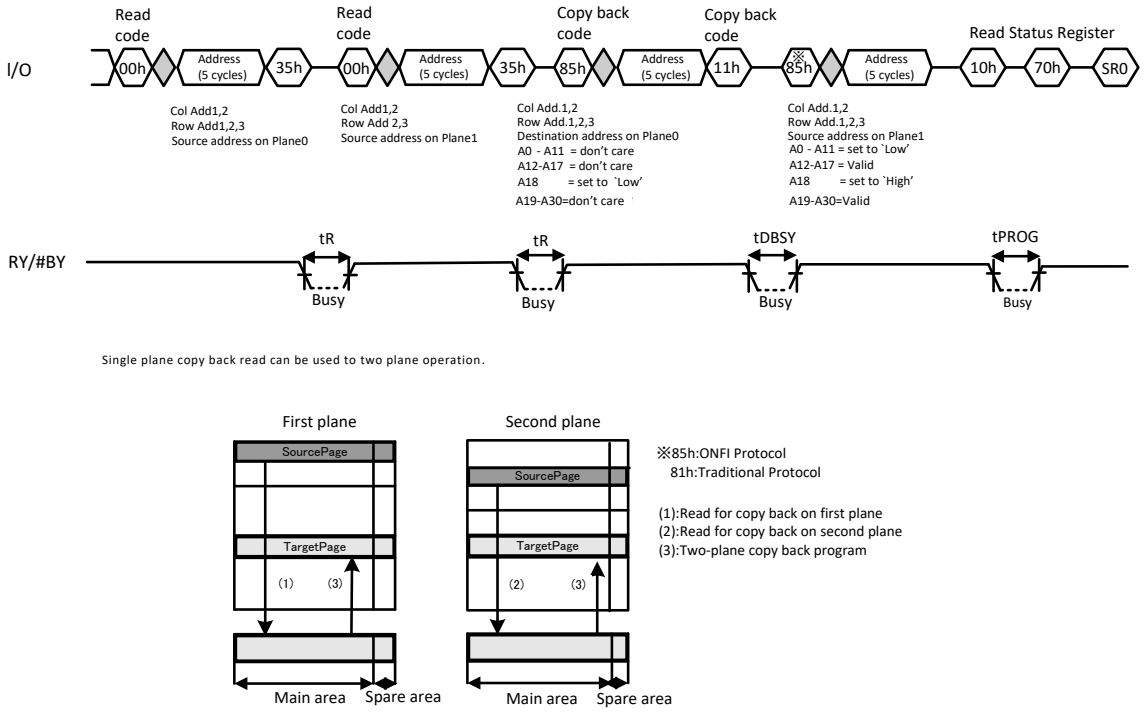



Figure 9-16 Two Plane Copy Back with Random Data Input


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Single plane copy back read can be used to two plane operation.




Figure 9-17 Two Plane Program for Copy Back


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## 9.4 BLOCK ERASE operation

### 9.4.1 BLOCK ERASE (60h-D0h)

Erase operations happen at the architectural block unit. This W29N08GW/Z has 2048 erase blocks. Each block is organized into 64 pages (x8:2112 bytes/page, x16:1056 words/page), 132K bytes (x8:128K + 4K bytes, x16:64 K+ 2Kwords)/block. The BLOCK ERASE command operates on a block by block basis.

Erase Setup command (60h) is written to the Command Register. Next, the three cycle block address is written to the device. The page address bits are loaded during address block address cycle, but are ignored. The Erase Confirm command (D0h) is written to the Command Register at the rising edge of #WE, RY/#BY goes LOW and the internal controller automatically handles the block erase sequence of operation. RY/#BY goes LOW during Block Erase internal operations for a period of tBERS,

The READ STATUS (70h) command can be used for confirm block erase status. When Status Register Bit6 (I/O6) becomes to “1”, block erase operation is finished. Status Register Bit0 (I/O0) will indicate a pass/fail condition (see Figure 9-24).

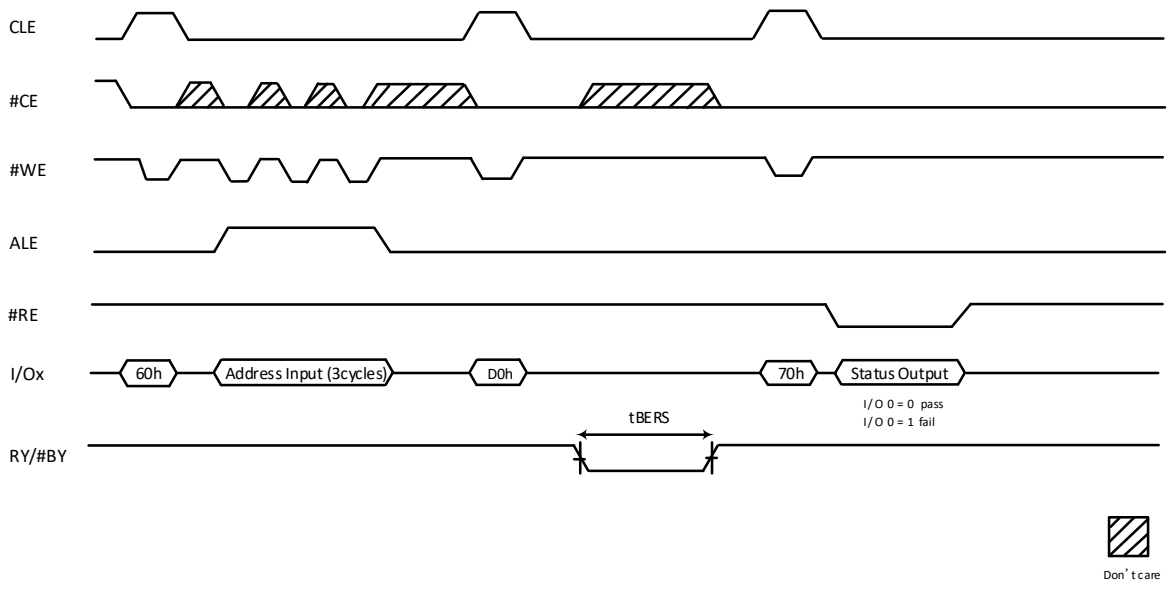



Figure 9-18 Block Erase Operation


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### 9.4.2 TWO PLANE BLOCK ERASE

TWO PLANE BLOCK ERASE (60h-D1h) command indicates two blocks in the specified plane that is to be erased. To start ERASE operation for indicated blocks in the specified plane, write the BLOCK ERASE (60h-D0h) command.

To indicate a block to be erased, writing 60h to the command register, then, write three address cycles containing the row address, the page address is ignored. By writing D1h command to command register, the device will go busy (SR BIT 6 = 0, SR BIT 5 = 0) for tDBSY.

To confirm busy status during tDBSY, the host can monitor RY/#BY signal. Instead, system can use READ STATUS (70h) or READ STATUS ENHANCED (78h) commands. When the status shows ready (SR BIT 6 = 1, SR BIT 5 = 1), additional TWO PLANE BLOCK ERASE commands can be issued for erasing two blocks in a specified plane.

When system issues TWO PLANE BLOCK ERASE (60h-D1h), and BLOCK ERASE (60h-D0h) commands, READ STATUS (70h) command can confirm whether the operation(s) passed or failed. If the status after READ STATUS (70h) command indicates an error (SR BIT 0 = 1), READ STATUS ENHANCED (78h) command can be determined which plane is failed.

TWO PLANE BLOCK ERASE commands require three cycles of row addresses; one address indicates the operational plane. These addresses are subject to the following requirements:

• The plane select bit, A18, must be set to “L” for 1st address input, and set to “H” for 2nd address input.

• The block address (A29-A19) of first address input is don’t care. It follows secondary inputted block address.

Two plane operations must be same type operation across the planes; for example, it is not possible to perform a PROGRAM operation on one plane with an ERASE operation on another.

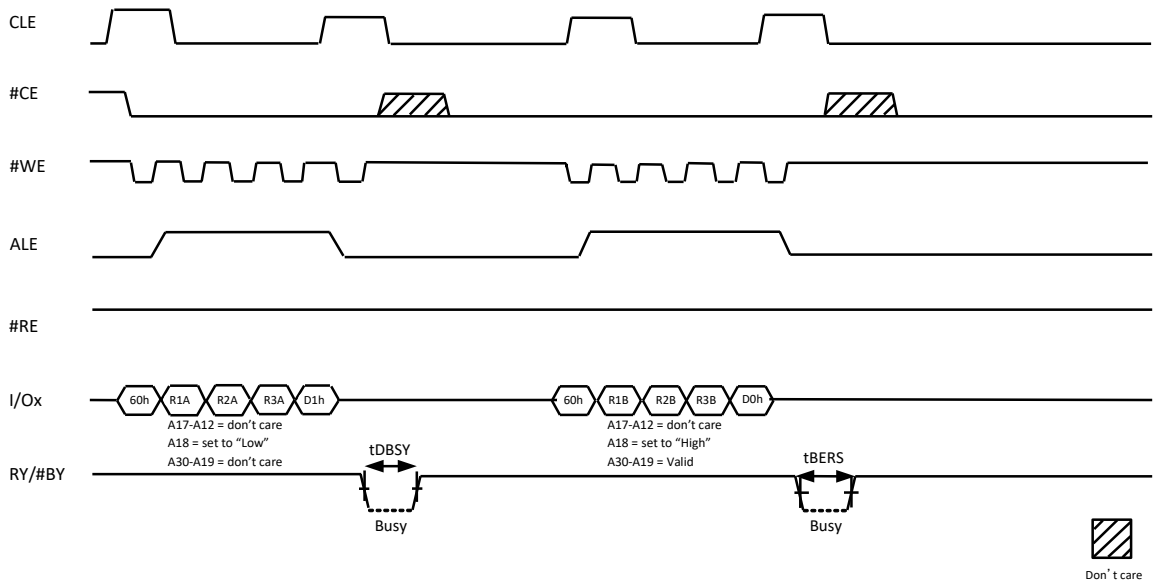



Figure 9-19 Two Plane Block Erase Operation


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## 9.5 RESET operation

### 9.5.1 RESET (FFh)

READ, PROGRAM, and ERASE commands can be aborted by the RESET (FFh) command during the time the W29N08GW/Z is in the busy state. The Reset operation puts the device into known status. The data that is processed in either the programming or erasing operations are no longer valid. This means the data can be partially programmed or erased and therefore data is invalid. The Command Register is cleared and is ready to accept next command. The Data Register contents are marked invalid.

The Status Register indicates a value of E0h when #WP is HIGH; otherwise a value of 60h is written when #WP is LOW. After RESET command is written to the command register, RY/#BY goes LOW for a period of tRST (see Figure 9-26).

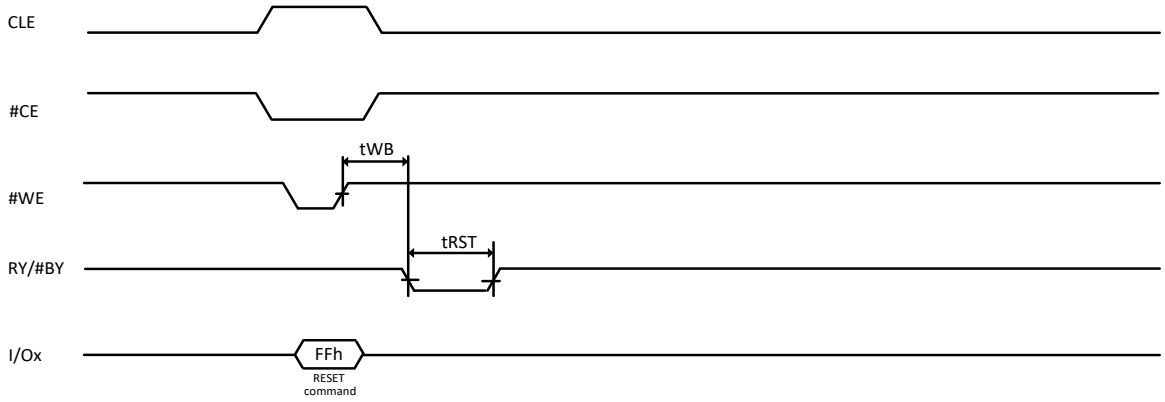



Figure 9-20 Reset Operation


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## 9.6 FEATURE OPERATION

The GET FEATURES (EEh) and SET FEATURES (EFh) commands are used to change the NAND Flash device behavior from the default power on settings. These commands use a one-byte feature address to determine which feature is to be read or modified. A range of 0 to 255 defines all features; each is described in the features table (see Table 9.5 thru 9.7). The GET FEATURES (EEh) command reads 4-Byte parameter in the features table (See GET FEATURES function). The SET FEATURES (EFh) command places the 4-Byte parameter in the features table (See SET FEATURES function).

When a feature is set, meaning it remains active by default until the device is powered off. The set feature remains the set even if a RESET (FFh) command is issued.

| Feature address | Description |
|---|---|
| 00h | N.A |
| 02h-7Fh | Reserved |
| 80h | Vendor specific parameter : Programmable I/O drive strength |
| 81h | Vendor specific parameter : Programmable RY/#BY pull-down strength |
| 82h-FFh | Reserved |

Table 9-5 Features


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**Feature Address 80h: Programmable I/O Drive Strength**

| Sub feature parameter | Options | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | I/O0 | Value | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **P1** | | | | | | | | | | | |
| I/O drive strength | Full (default) | Reserved (0) | | | | | | 0 | 0 | 00h | 1 |
| | Three-quarters | Reserved (0) | | | | | | 0 | 1 | 01h | |
| | One-half | Reserved (0) | | | | | | 1 | 0 | 02h | |
| | One-quarter | Reserved (0) | | | | | | 1 | 1 | 03h | |
| **P2** | | | | | | | | | | | |
| | | Reserved (0) | | | | | | | | 00h | |
| **P3** | | | | | | | | | | | |
| | | Reserved (0) | | | | | | | | 00h | |
| **P4** | | | | | | | | | | | |
| | | Reserved (0) | | | | | | | | 00h | |

Table 9-6 Feature Address 80h

**Note:**

1. **The default drive strength setting is Full strength. The Programmable I/O Drive Strength mode is used to change from the default I/O drive strength. Drive strength should be selected based on expected loading of the memory bus. This table shows the four supported output drive-strength settings. The device returns to the default drive strength mode when a power cycle has occurred. AC timing parameters may need to be relaxed if I/O drive strength is not set to full.**


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**Feature Address 81h: Programmable RY/#BY Pull-down Strength**

| Sub feature parameter | Options | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | I/O0 | Value | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **P1** | | | | | | | | | | | |
| RY/#BY pull-down strength | Full (default) | Reserved (0) | | | | | | 0 | 0 | 00h | 1 |
| | Three-quarters | Reserved (0) | | | | | | 0 | 1 | 01h | |
| | One-half | Reserved (0) | | | | | | 1 | 0 | 02h | |
| | One-quarter | Reserved (0) | | | | | | 1 | 1 | 03h | |
| **P2** | | | | | | | | | | | |
| | | Reserved (0) | | | | | | | | 00h | |
| **P3** | | | | | | | | | | | |
| | | Reserved (0) | | | | | | | | 00h | |
| **P4** | | | | | | | | | | | |
| | | Reserved (0) | | | | | | | | 00h | |

Table 9-7 Feature Address 81h

**Note:**

1. **The default programmable RY/#BY pull-down strength is set to Full strength. The pull-down strength is used to change the RY/#BY pull-down strength. RY/#BY pull-down strength should be selected based on expected loading of RY/#BY. The four supported pull-down strength settings are shown. The device returns to the default pull-down strength when a power cycle has occurred.**


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### 9.6.1 GET FEATURES (EEh)

The GET FEATURES command returns the device feature settings including those previously set by the SET FEATURES command. To use the Get Feature mode write the command (EEh) to the Command Register followed by the single cycle byte Feature Address. RY/#BY will goes LOW for the period of tFEAT. If Read Status (70h) command is issued for monitoring the process completion status, Read Command (00h) has to be executed to re-establish data output mode. Once, RY/#BY goes HIGH, the device feature settings can be read by toggling #RE. The device remains in Feature Mode until another valid command is issued to Command Register. See Figure 9-27.

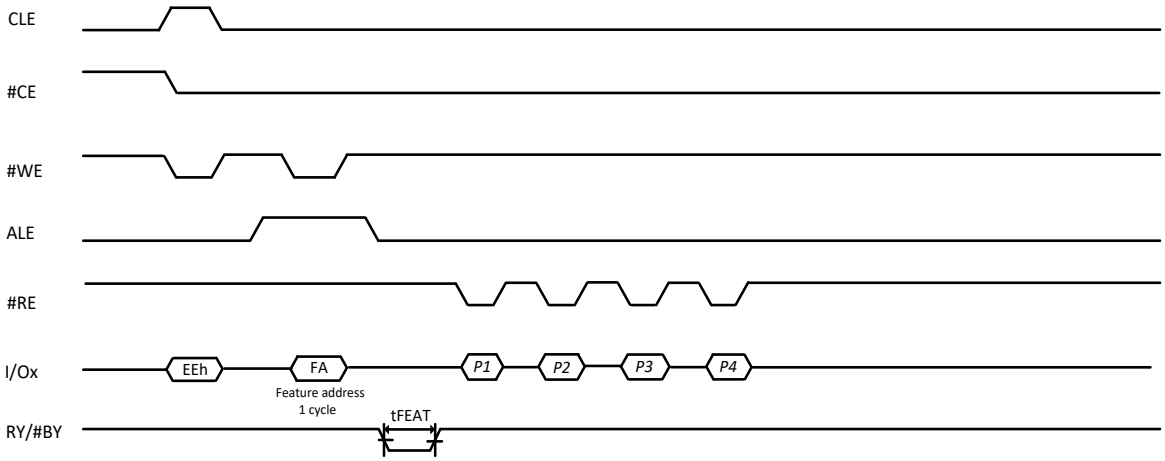



Figure 9-21 Get Feature Operation


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### 9.6.2 SET FEATURES (EFh)

The SET FEATURES command sets the behavior parameters by selecting a specified feature address. To change device behavioral parameters, execute Set Feature command by writing EFh to the Command Register, followed by the single cycle feature address. Each feature parameter (P1-P4) is latched at the rising edge of each #WE. The RY/#BY signal will go LOW during the period of tFEAT while the four feature parameters are stored. The Read Status (70h) command can be issued for monitoring the progress status of this operation. The parameters are stored in device until the device goes through a power on cycle. The device remains in feature mode until another valid command is issued to Command Register.

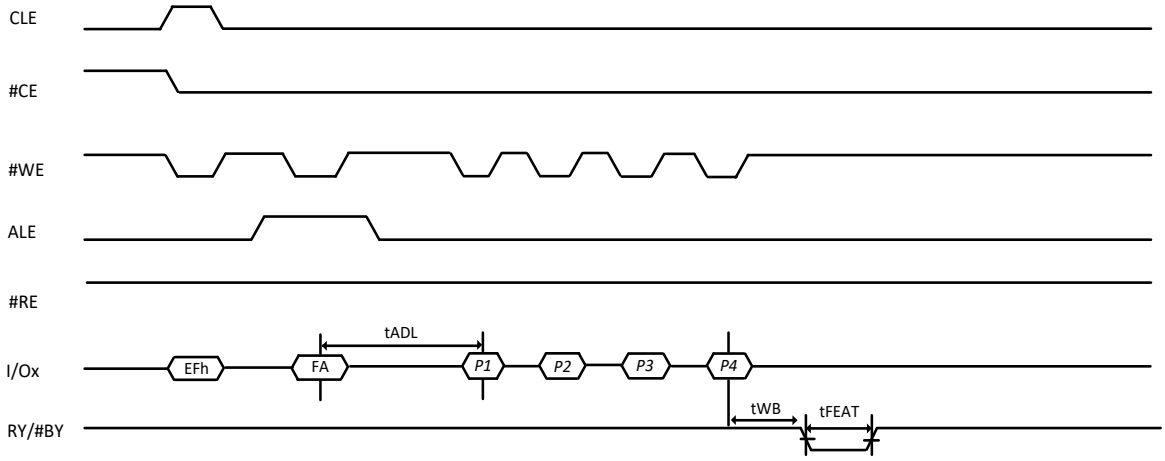



Figure 9-22 Set Feature Operation


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## 9.7 ONE TIME PROGRAMMABLE (OTP) area

The device has One-Time Programmable (OTP) memory area comprised of a number of pages (2112 bytes/page) (1056words/page). This entire range of pages is functionally guaranteed. Only the OTP commands can access the OTP area. When the device ships from Winbond, the OTP area is in an erase state (all bits equal “1”). The OTP area cannot be erased, therefore protecting the area only prevent further programming. Contact to Winbond for using this feature.


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## 9.8 WRITE PROTECT

#WP pin can enable or disable program and erase commands preventing or allowing program and erase operations. Figure 9-29 to 9-34 shows the enabling or disabling timing with #WP setup time (tWW) that is from rising or falling edge of #WP to latch the first commands. After first command is latched, #WP pin must not toggle until the command operation is complete and the device is in the ready state. (Status Register Bit5 (I/O5) equal 1)

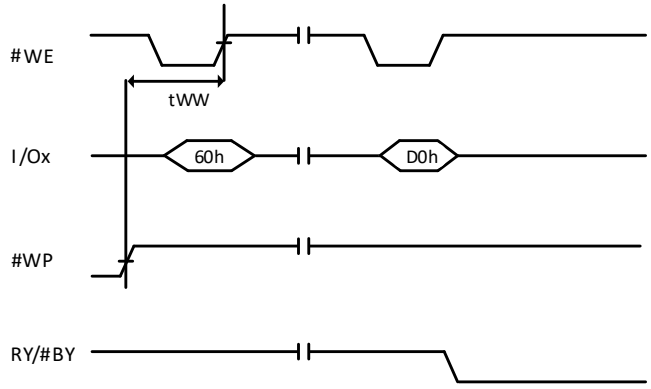



Figure 9-23 Erase Enable

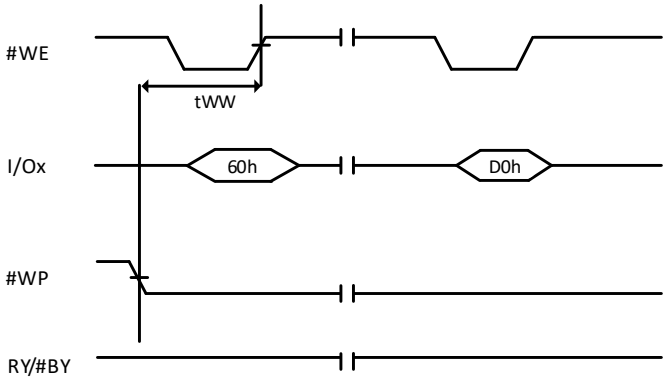



Figure 9-24 Erase Disable


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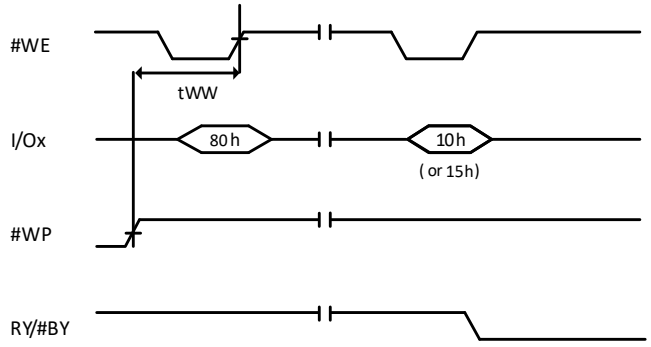



Figure 9-25 Program Enable

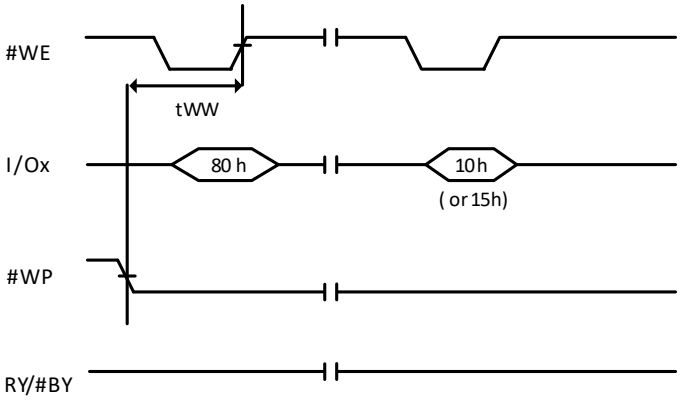



Figure 9-26 Program Disable

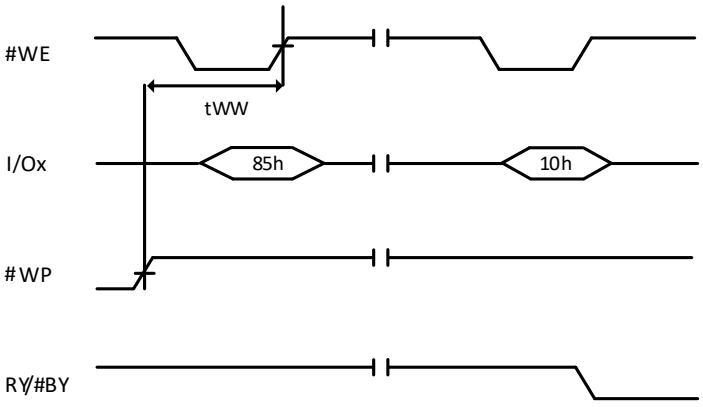



Figure 9-27 Program for Copy Back Enable


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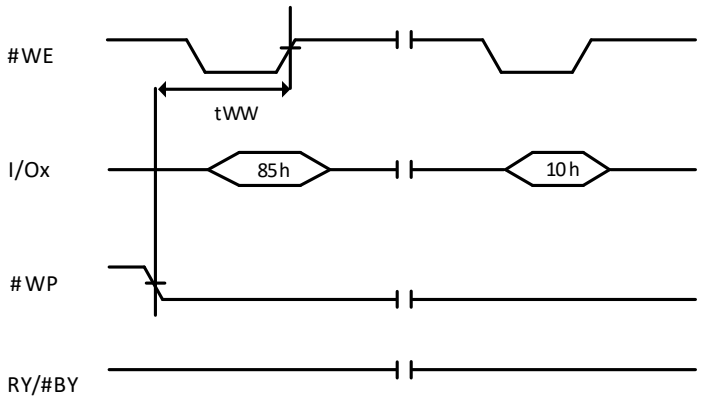



Figure 9-28 Program for Copy Back Disable

## 9.9 BLOCK LOCK

The device has block lock feature that can protect the entire device or user can indicate a ranges of blocks from program and erase operations. Using this feature offers increased functionality and flexibility data protection to prevent unexpected program and erase operations. Contact to Winbond for using this feature.


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# 10. ELECTRICAL CHARACTERISTICS

## 10.1 Absolute Maximum Ratings (1.8V)

| PARAMETERS | SYMBOL | CONDITIONS | RANGE | UNIT |
|---|---|---|---|---|
| Supply Voltage | VCC | | –0.6 to +2.4 | V |
| Voltage Applied to Any Pin | VIN | Relative to Ground | –0.6 to +2.4 | V |
| Storage Temperature | TSTG | | –65 to +150 | °C |
| Short circuit output current, I/Os | | | 5 | mA |

Table 10-1 Absolute Maximum Ratings

**Notes:**

1. **Specification for W29N08GW/Z is preliminary. See preliminary designation at the end of this document.**
2. **Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.**
3. **Maximum DC voltage on input/output pins is Vcc+0.3V which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.**
4. **This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.**

## 10.2 Operating Ranges (1.8V)

| PARAMETER | SYMBOL | CONDITIONS | SPEC | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| Supply Voltage | VCC | | 1.7 | 1.95 | V |
| Ambient Temperature, Operating | TA | Industrial | -40 | +85 | °C |
| | | Industrial Plus | -40 | +105 | |

Table 10-2 Operating Ranges


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## 10.3 Device Power-up Timing

The device is designed to avoid unexpected program/erase operations during power transitions. When the device is powered on, an internal voltage detector disables all functions whenever Vcc is below about 1.1V at 1.8V device. Write Protect (#WP) pin provides hardware protection and is recommended to be kept at VIL during power up and power down. A recovery time of minimum 1ms is required before internal circuit gets ready for any command sequences (See Figure 10-1).

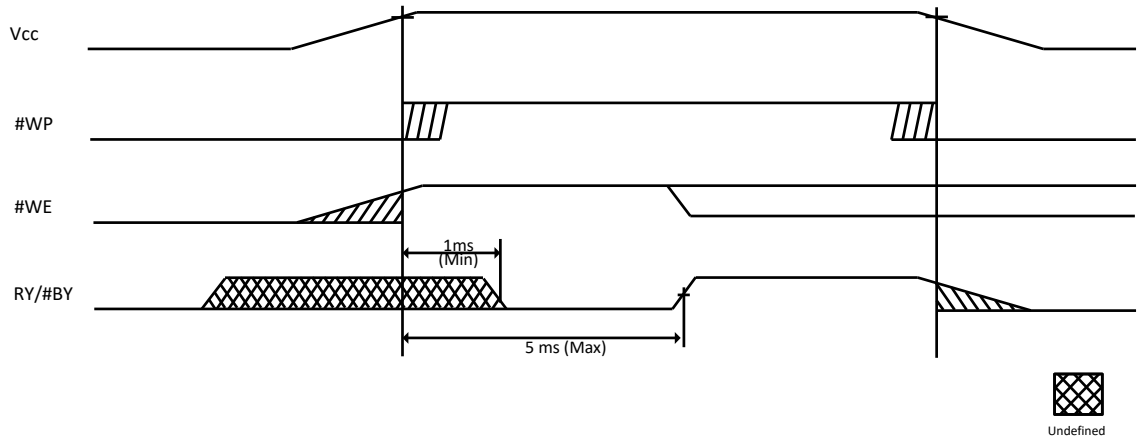



Figure 10-1 Power ON/OFF sequence


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## 10.4 DC Electrical Characteristics (1.8V)

| PARAMETER | SYMBOL | CONDITIONS | SPEC | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Sequential Read current | Icc1 | tRC= tRC MIN<br>#CE=VIL<br>IOUT=0mA | - | 13 | 20 | mA |
| Program current | Icc2 | - | - | 13 | 20 | mA |
| Erase current | Icc3 | - | - | 13 | 20 | mA |
| Standby current (TTL) | ISB1 | #CE=VIH<br>#WP=0V/Vcc | - | - | 1 | mA |
| Standby current (CMOS) Industrial | ISB2 | #CE=Vcc – 0.2V<br>#WP=0V/Vcc | - | 20 | 100 | µA |
| Standby current (CMOS) Industrial Plus | | | - | 20 | 200 | µA |
| Input leakage current | ILI | VIN= 0 V to Vcc | - | - | ±10 | µA |
| Output leakage current | ILO | VOUT=0V to Vcc | - | - | ±10 | µA |
| Input high voltage | VIH | I/O15~0, #CE,#WE,#RE, #WP,CLE,ALE | 0.8 x Vcc | - | Vcc + 0.3 | V |
| Input low voltage | VIL | - | -0.3 | - | 0.2 x Vcc | V |
| Output high voltage(1) | VOH | IOH=-100µA | Vcc -0.1 | - | - | V |
| Output low voltage(1) | VOL | IOL=+100µA | - | - | 0.1 | V |
| Output low current | IOL(RY/#BY) | VOL=0.2V | 3 | 4 | | mA |

Table 10-3 DC Electrical Characteristics

**Note:**

1. **VOH and VOL may need to be relaxed if I/O drive strength is not set to full.**
2. **IOL (RY/#BY) may need to be relaxed if RY/#BY pull-down strength is not set to full**


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## 10.5 AC Measurement Conditions (1.8V)

| PARAMETER | SYMBOL | SPEC | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| Input Capacitance(1), (2) | CIN | - | 10 | pF |
| Input/Output Capacitance(1), (2) | CIO | - | 10 | pF |
| Input Rise and Fall Times | TR/TF | - | 2.5 | ns |
| Input Pulse Voltages | - | 0 to VCC | | V |
| Input/Output timing Voltage | - | Vcc/2 | | V |
| Output load (1) | CL | 1TTL GATE and CL=30pF | | - |

Table 10-4 AC Measurement Conditions

**Notes:**

1. **Verified on device characterization , not 100% tested**
2. **Test conditions TA=25'C, f=1MHz, VIN=0V**


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## 10.6 AC Timing Characteristics for Command, Address and Data Input (1.8V)

| PARAMETER | SYMBOL | SPEC | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| ALE to Data Loading Time | tADL | 70 | - | ns |
| ALE Hold Time | tALH | 5 | - | ns |
| ALE setup Time | tALS | 10 | - | ns |
| #CE Hold Time | tCH | 5 | - | ns |
| CLE Hold Time | tCLH | 5 | - | ns |
| CLE setup Time | tCLS | 10 | - | ns |
| #CE setup Time | tCS | 20 | - | ns |
| Data Hold Time | tDH | 5 | - | ns |
| Data setup Time | tDS | 10 | - | ns |
| Write Cycle Time | tWC | 35 | - | ns |
| #WE High Hold Time | tWH | 10 | - | ns |
| #WE Pulse Width | tWP | 12 | - | ns |
| #WP setup Time | tWW | 100 | - | ns |

Table 10-5 AC Timing Characteristics for Command, Address and Data Input

**Note:**

1. **tADL is the time from the #WE rising edge of final address cycle to the #WE rising edge of first data cycle.**


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## 10.7 AC Timing Characteristics for Operation (1.8V)

| PARAMETER | SYMBOL | SPEC | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| ALE to #RE Delay | tAR | 10 | - | ns |
| #CE Access Time | tCEA | - | 30 | ns |
| #CE HIGH to Output High-Z(1) | tCHZ | - | 50 | ns |
| CLE to #RE Delay | tCLR | 10 | - | ns |
| #CE HIGH to Output Hold | tCOH | 15 | - | ns |
| Output High-Z to #RE LOW | tIR | 0 | - | ns |
| Data Transfer from Cell to Data Register | tR | - | 25 | µs |
| READ Cycle Time | tRC | 35 | - | ns |
| #RE Access Time | tREA | - | 25 | ns |
| #RE HIGH Hold Time | tREH | 10 | - | ns |
| #RE HIGH to Output Hold | tRHOH | 15 | - | ns |
| #RE HIGH to #WE LOW | tRHW | 100 | - | ns |
| #RE HIGH to Output High-Z(1) | tRHZ | - | 100 | ns |
| #RE LOW to output hold | tRLOH | 3 | - | ns |
| #RE Pulse Width | tRP | 12 | - | ns |
| Ready to #RE LOW | tRR | 20 | - | ns |
| Reset Time (READ/PROGRAM/ERASE)(2) | tRST | - | 5/10/500 | µs |
| #WE HIGH to Busy(3) | tWB | - | 100 | ns |
| #WE HIGH to #RE LOW | tWHR | 80 | - | ns |

Table 10-6 AC Timing Characteristics for Operation

**Notes: AC characteristics may need to be relaxed if I/O drive strength is not set to "full."**

1. **Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100 % tested**
2. **Do not issue new command during tWB, even if RY/#BY is ready.**


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## 10.8 Program and Erase Characteristics

| PARAMETER | SYMBOL | SPEC | | UNIT |
|---|---|---|---|---|
| | | TYP | MAX | |
| Number of partial page programs | NoP | - | 4 | cycles |
| Page Program time | tPROG | 250 | 700 | µs |
| Busy Time for SET FEATURES /GET FEATURES | tFEAT | - | 1 | µs |
| Busy Time for program/erase at locked block | tLBSY | - | 3 | µs |
| Busy Time for OTP program when OTP is protected | tOBSY | - | 30 | µs |
| Block Erase Time | tBERS | 2 | 10 | ms |
| Last Page Program time (1) | tLPROG | - | - | - |
| Busy Time for Two Plane page program and Two Plane Block Erase | tDBSY | 0.5 | 1 | µs |

Table 10-7 Program and Erase Characteristics

**Note:**

1. **tLPROG = Last Page program time (tPROG) + Last -1 Page program time (tPROG) – Last page Address, Command and Data load time.**


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## 11. TIMING DIAGRAMS

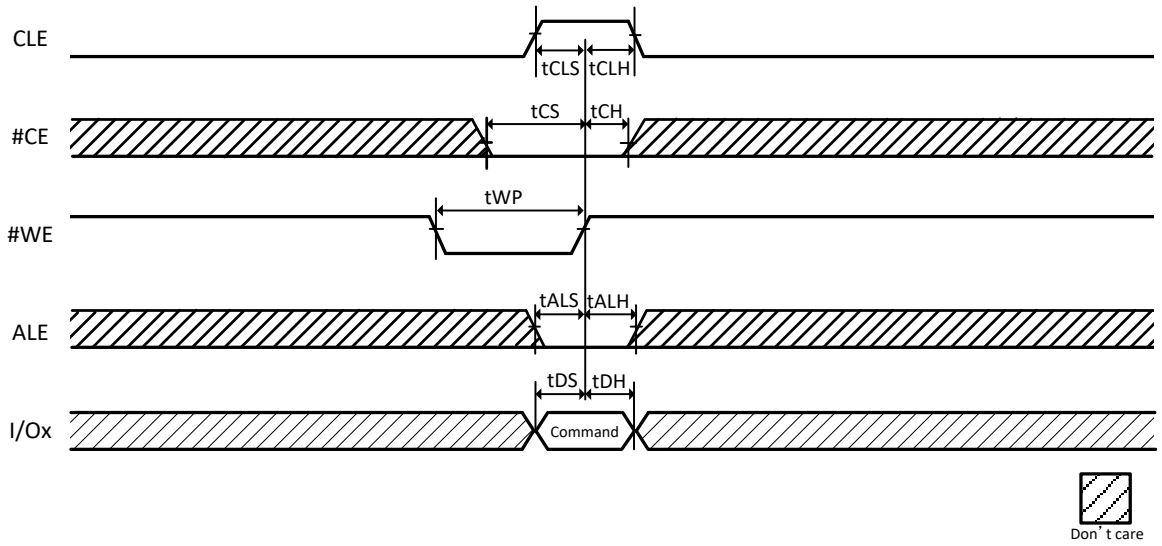



Figure 11-1 Command Latch Cycle

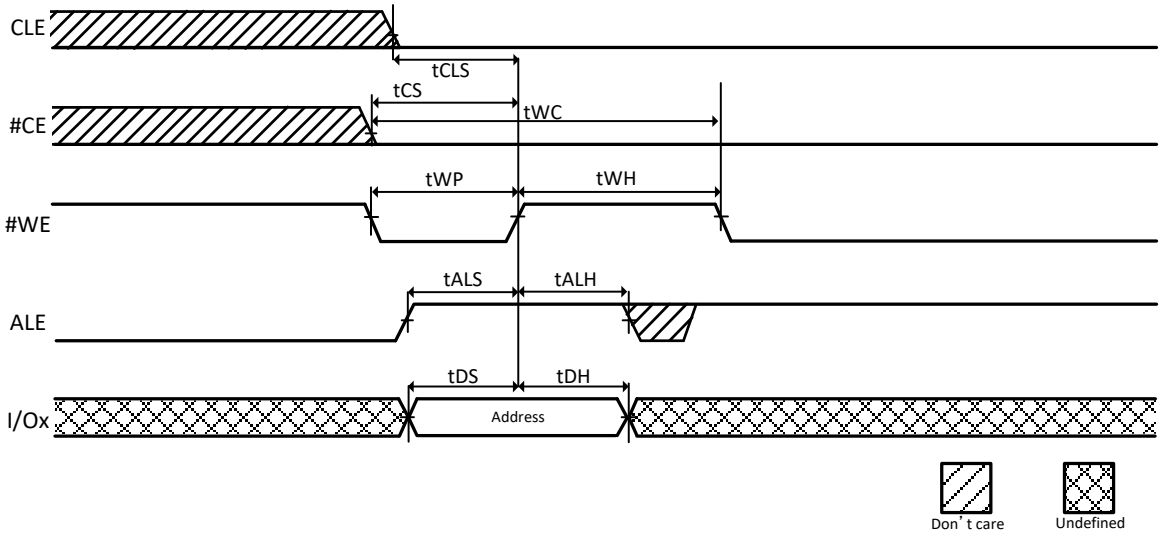



Figure 11-2 Address Latch Cycle


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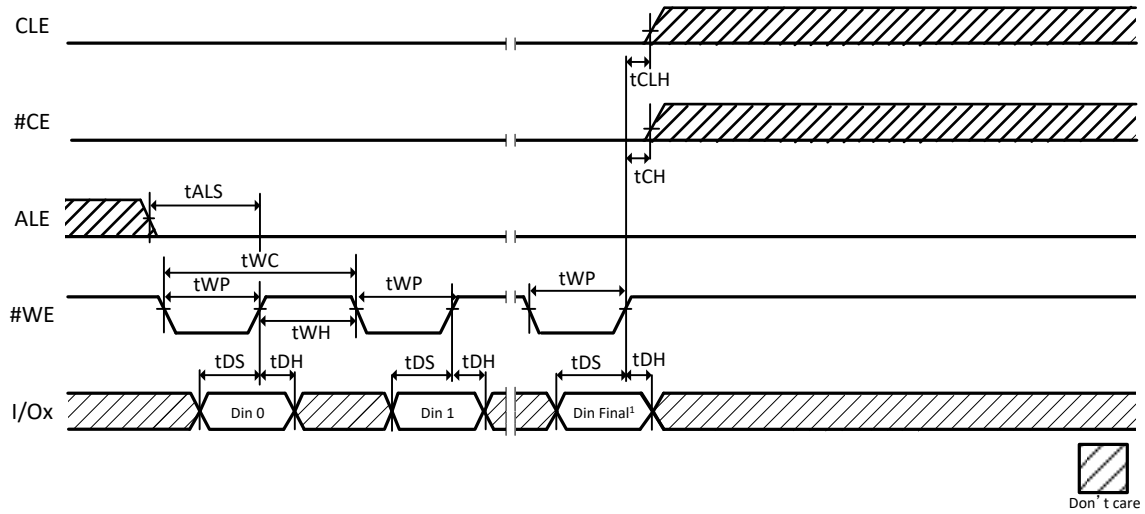



Figure 11-3 Data Latch Cycle

**Note:**

1. **Din Final = 2,111(x8)**

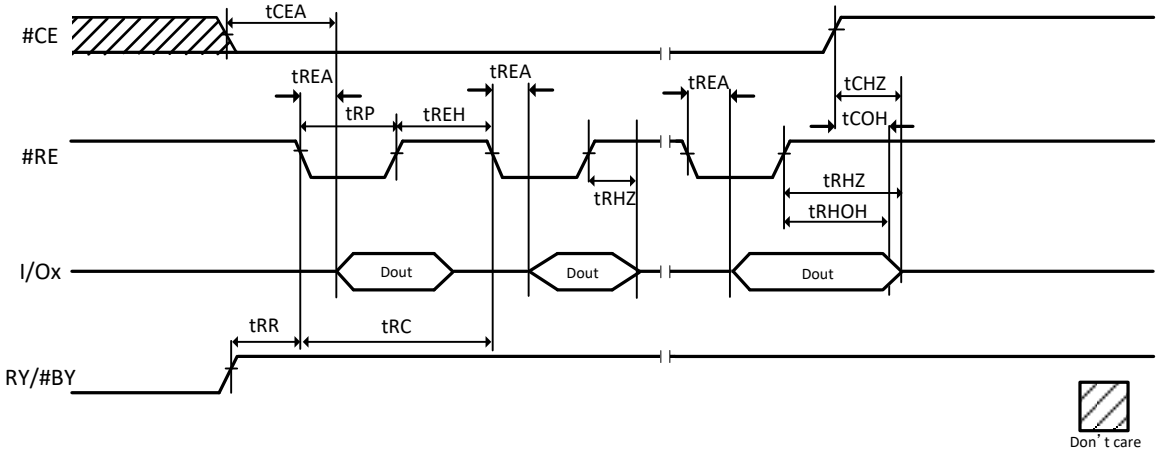



Figure 11-4 Serial Access Cycle after Read


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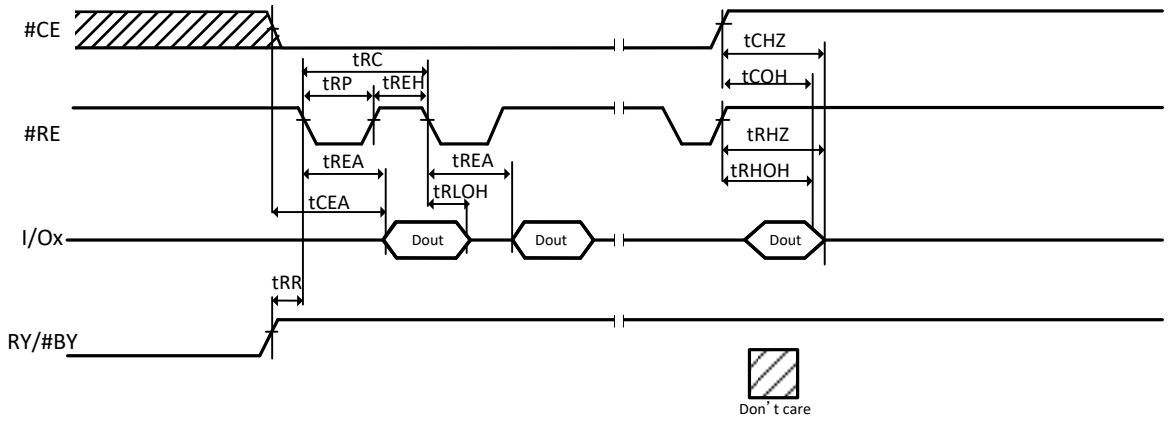



Figure 11-5 Serial Access Cycle after Read (EDO)

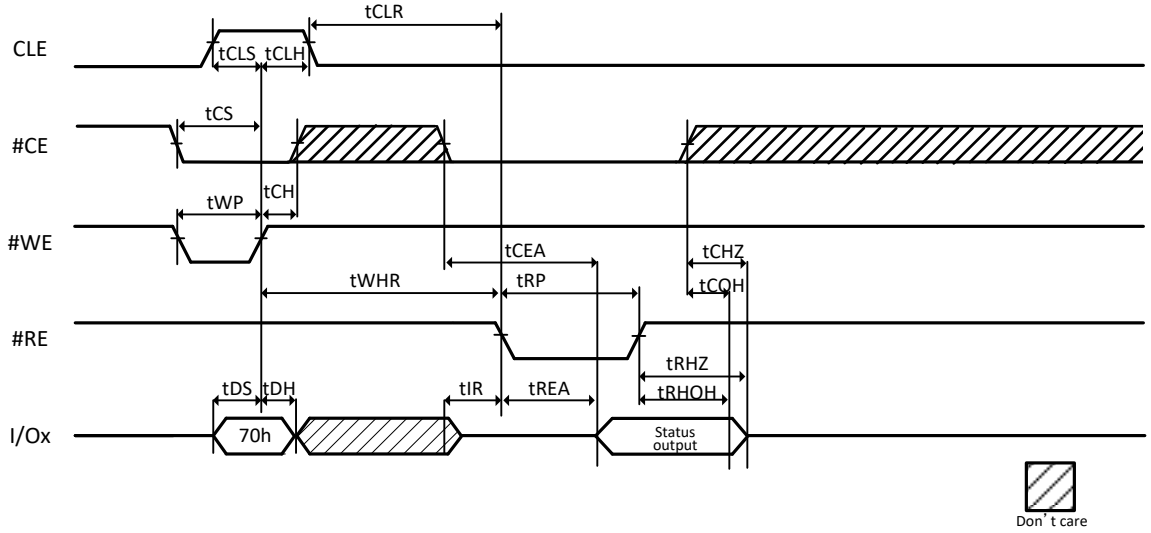



Figure 11-6 Read Status Operation


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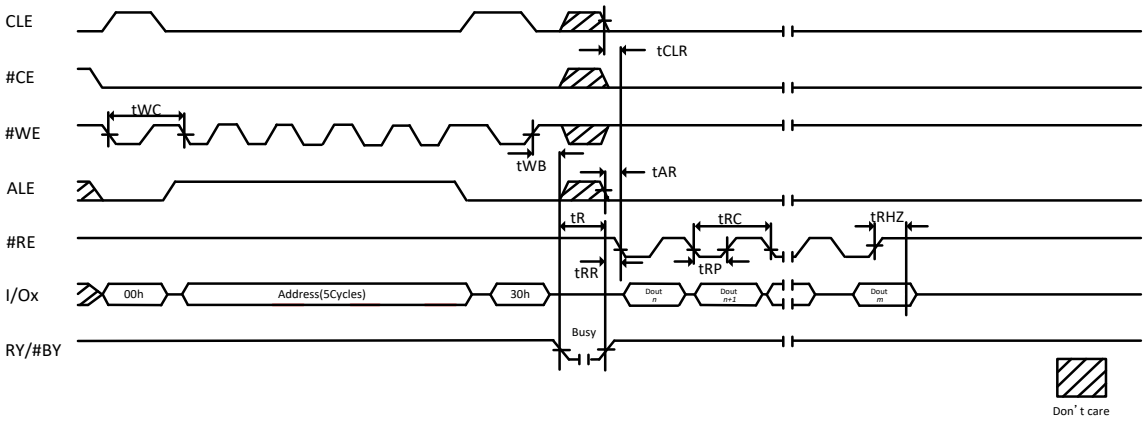



Figure 11-7 Page Read Operation

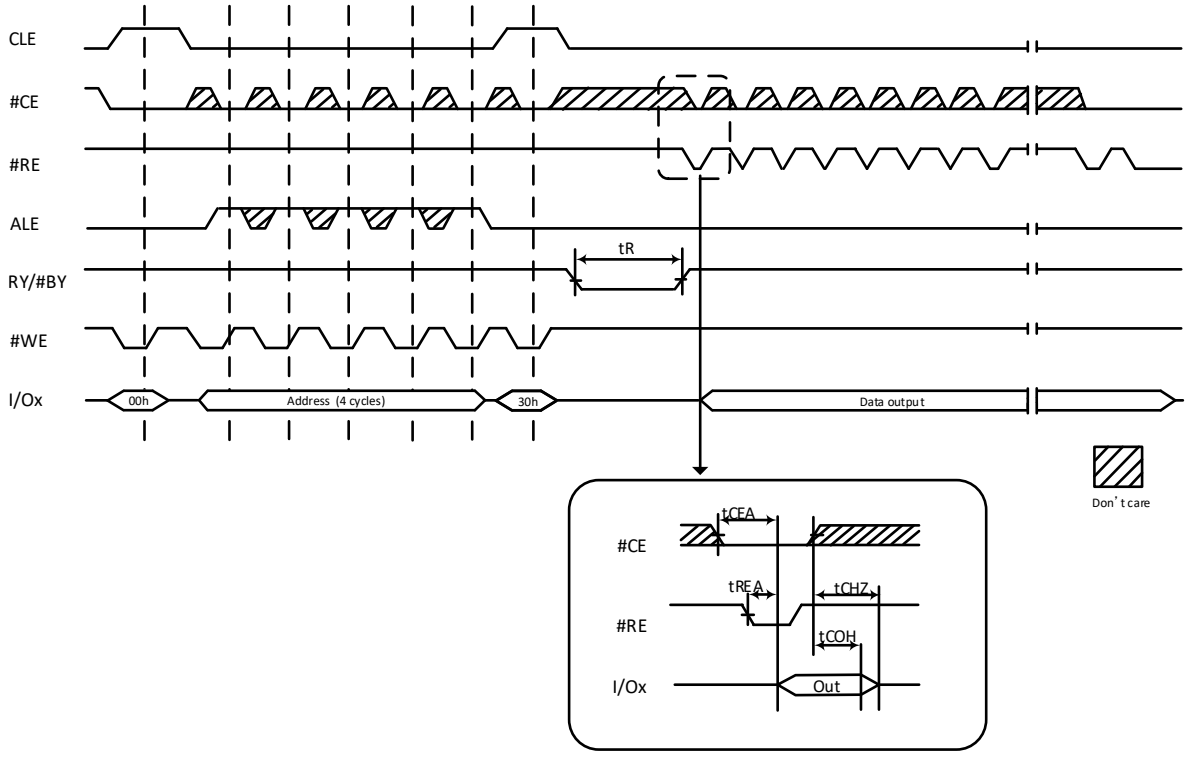



Figure 11-8 #CE Don't Care Read Operation


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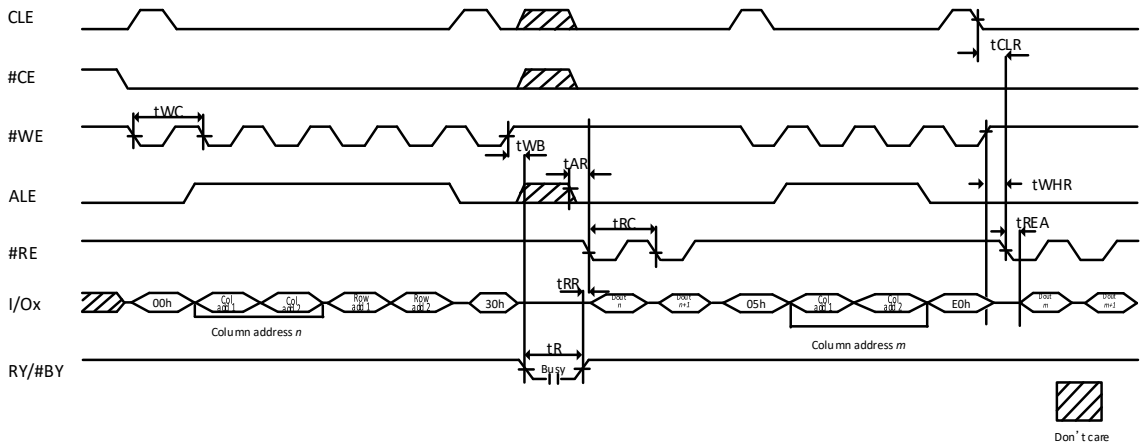



Figure 11-9 Random Data Output Operation

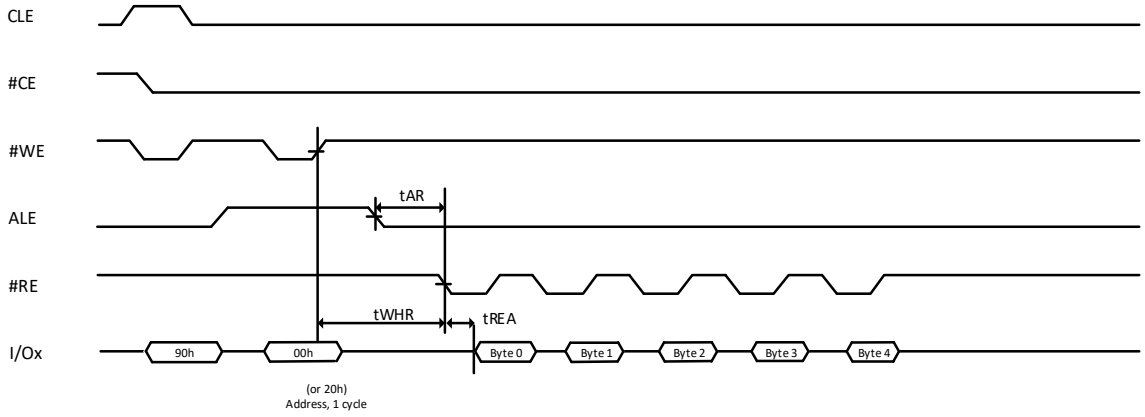



Figure 11-10 Read ID

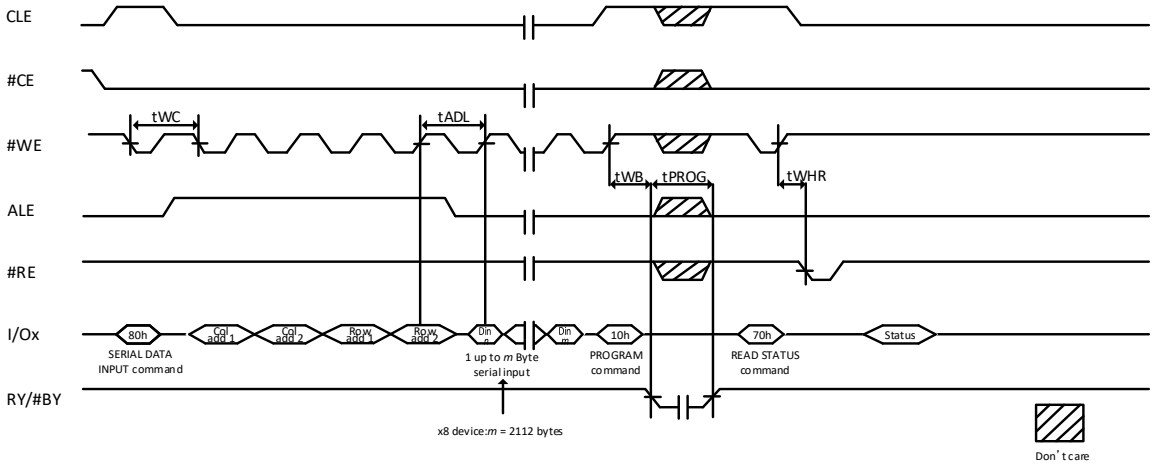



Figure 11-11 Page Program


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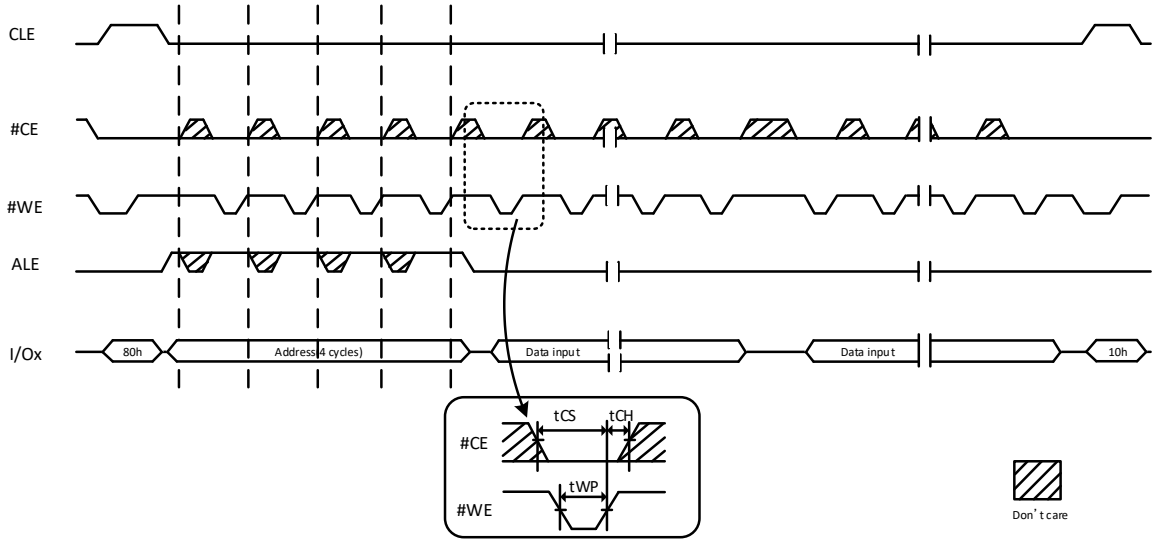



Figure 11-12 #CE Don't Care Page Program Operation


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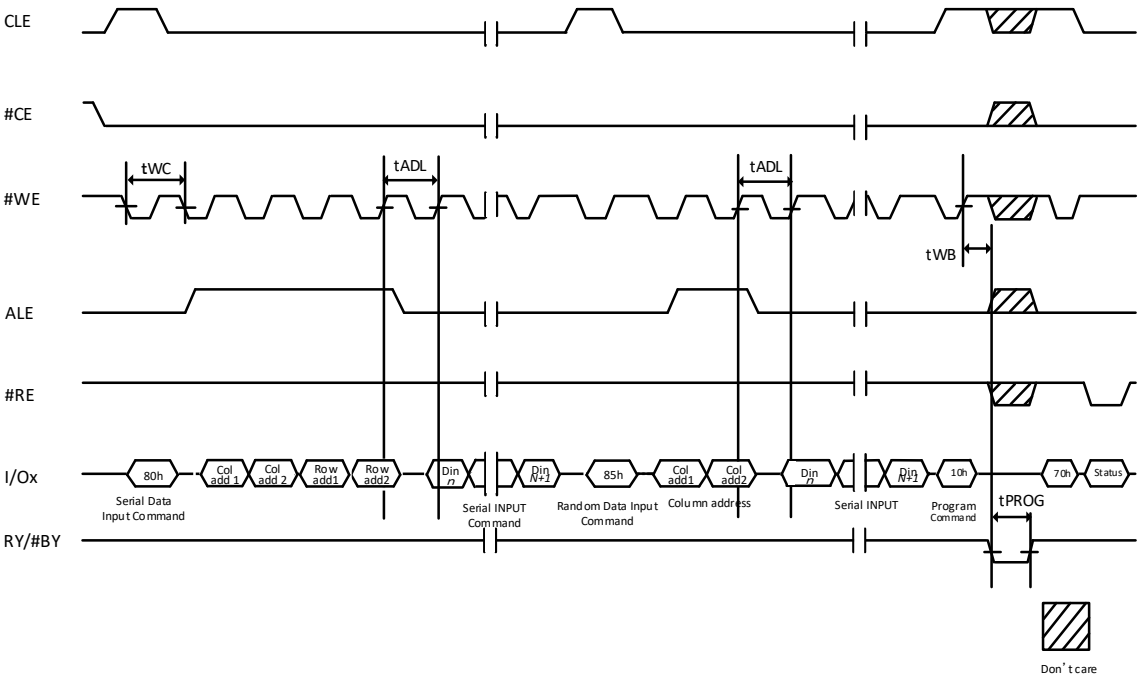



Figure 11-13 Page Program with Random Data Input

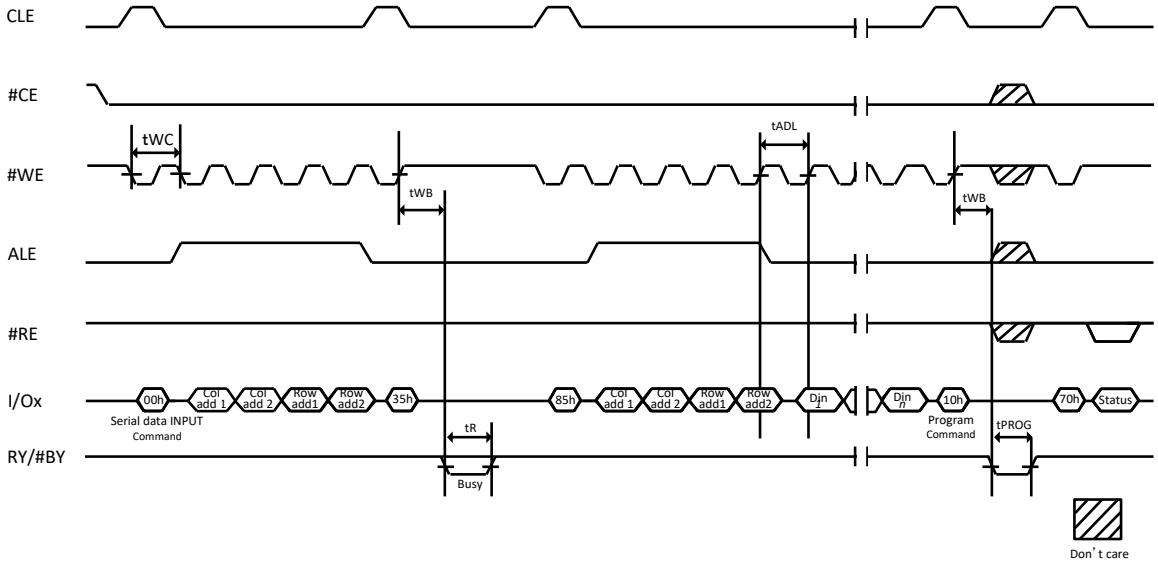



Figure 11-14 Copy Back


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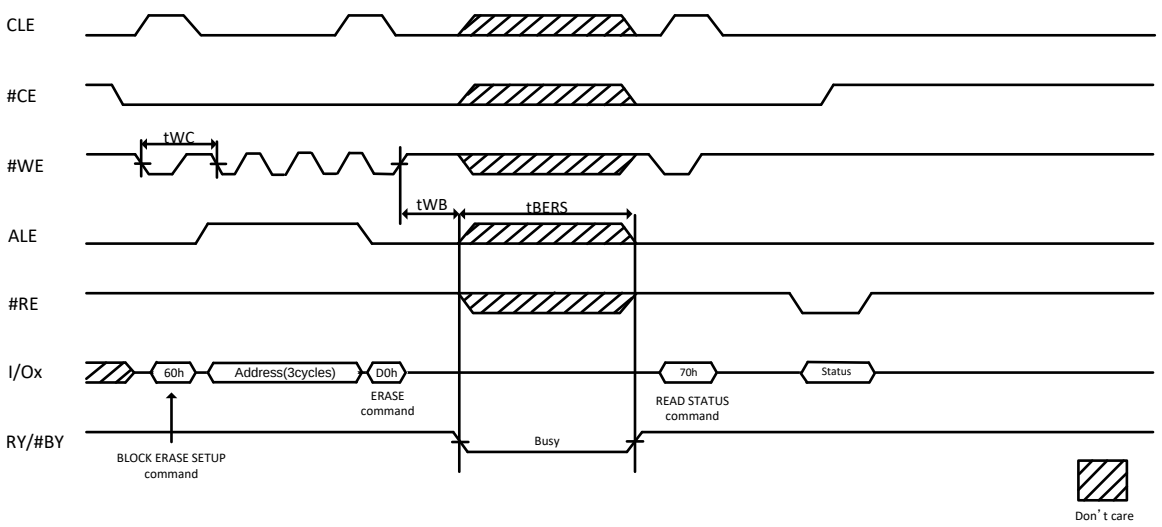



Figure 11-15 Block Erase

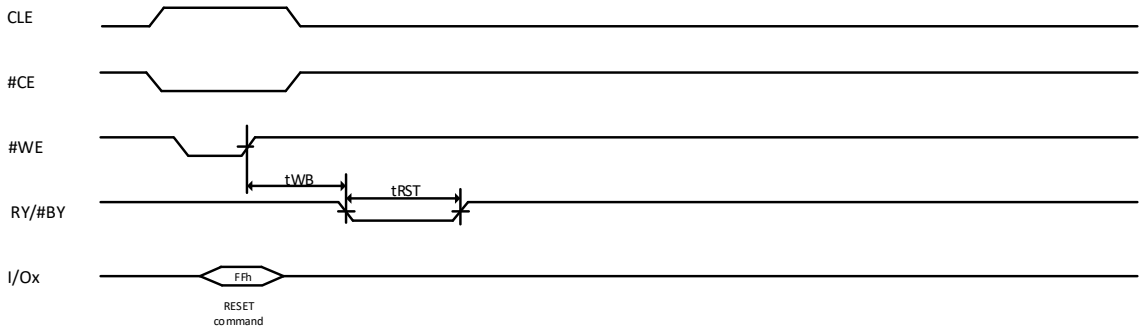



Figure 11-16 Reset


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# 12. INVALID BLOCK MANAGEMENT

## 12.1 Invalid Blocks

The W29N08GW/Z may have initial invalid blocks when it ships from factory. Also, additional invalid blocks may develop during the use of the device. Nvb represents the minimum number of valid blocks in the total number of available blocks (See Table 12.1). An invalid block is defined as blocks that contain one or more bad bits. Block 0, block address 00h is guaranteed to be a valid block at the time of shipment.

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Valid block number | Nvb | 8032 | 8192 | blocks |

Table 12-1 Valid Block Number

## 12.2 Initial Invalid Blocks

Initial invalid blocks are defined as blocks that contain one or more invalid bits when shipped from factory.

Although the device contains initial invalid blocks, a valid block of the device is of the same quality and reliability as all valid blocks in the device with reference to AC and DC specifications. The W29N08GW/Z has internal circuits to isolate each block from other blocks and therefore, the invalid blocks will not affect the performance of the entire device.

Before the device is shipped from the factory, it will be erased and invalid blocks are marked. All initial invalid blocks are marked with non-FFh at the first byte of spare area on the 1st or 2nd page. The initial invalid block information cannot be recovered if inadvertently erased. Therefore, software should be created to initially check for invalid blocks by reading the marked locations before performing any program or erase operation, and create a table of initial invalid blocks as following flow chart


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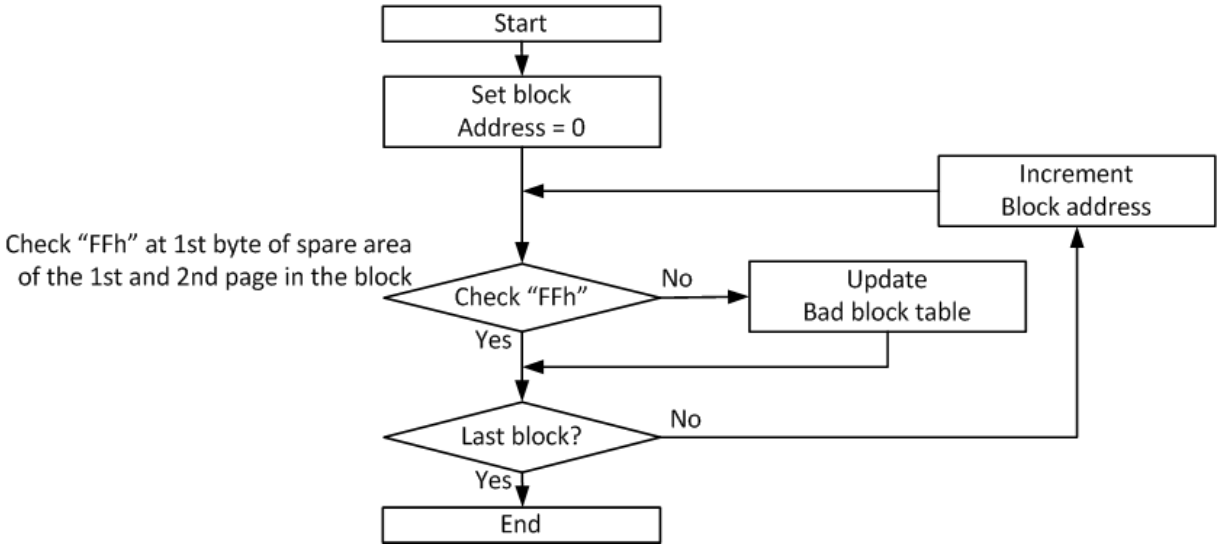



Figure 12-1 Flow Chart of Create Initial Invalid Block Table

## 12.3 Error in Operation

Additional invalid blocks may develop in the device during its life cycle. Following the procedures herein is required to guarantee reliable data in the device.

After each program and erase operation, check the status read to determine if the operation failed. In case of failure, a block replacement should be done with a bad-block management algorithm. The system has to use a minimum 1-bit ECC per 528 bytes of data to ensure data recovery.

| Operation | Detection and recommended procedure |
|---|---|
| Erase | Status read after erase → Block Replacement |
| Program | Status read after program → Block Replacement |
| Read | Verify ECC → ECC correction |

Table 12-2 Block Failure


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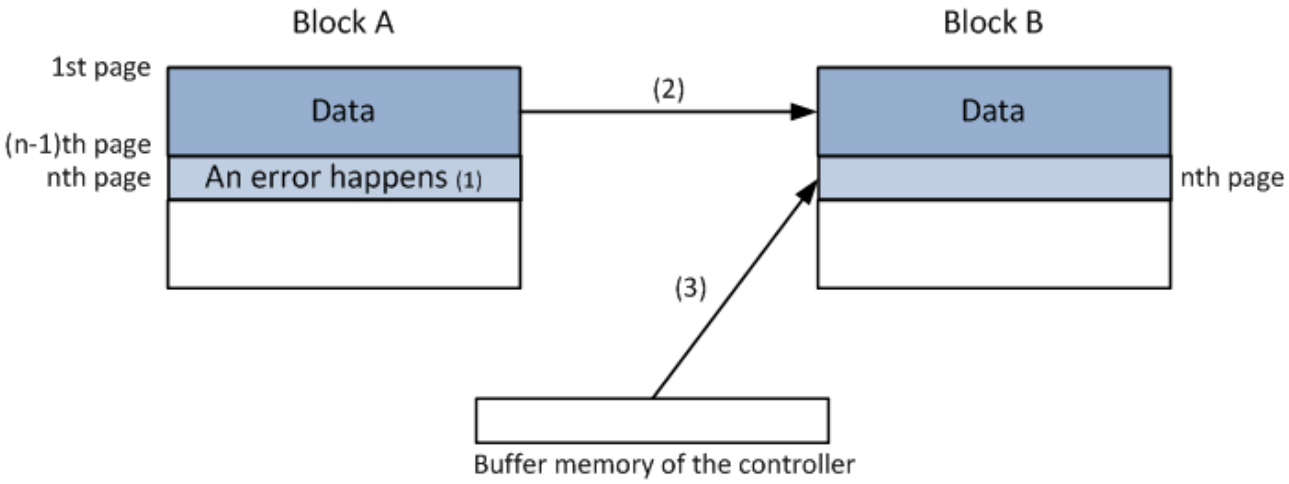



Figure 12-12-2 Bad Block Replacement

**Note:**

1. **An error happens in the nth page of block A during program or erase operation.**
2. **Copy the data in block A to the same location of block B which is valid block.**
3. **Copy the nth page data of block A in the buffer memory to the nth page of block B**
4. **Creating or updating bad block table for preventing further program or erase to block A**

.

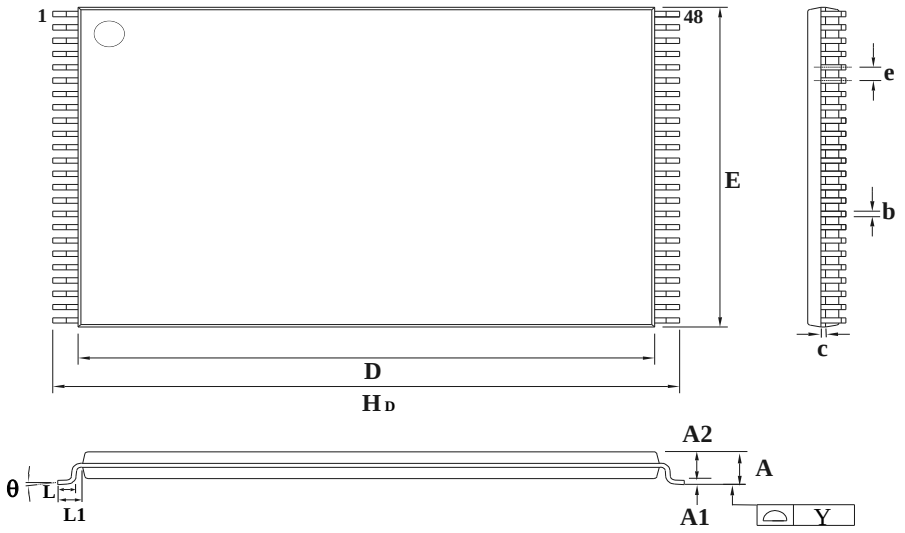
## 12.4 Addressing in Program Operation

The pages within the block have to be programmed sequentially from LSB (least significant bit) page to the MSB (most significant bit) within the block. The LSB is defined as the start page to program, does not need to be page 0 in the block. Random page programming is prohibited.


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# 13. PACKAGE DIMENSIONS

## 13.1 TSOP 48-pin 12x20

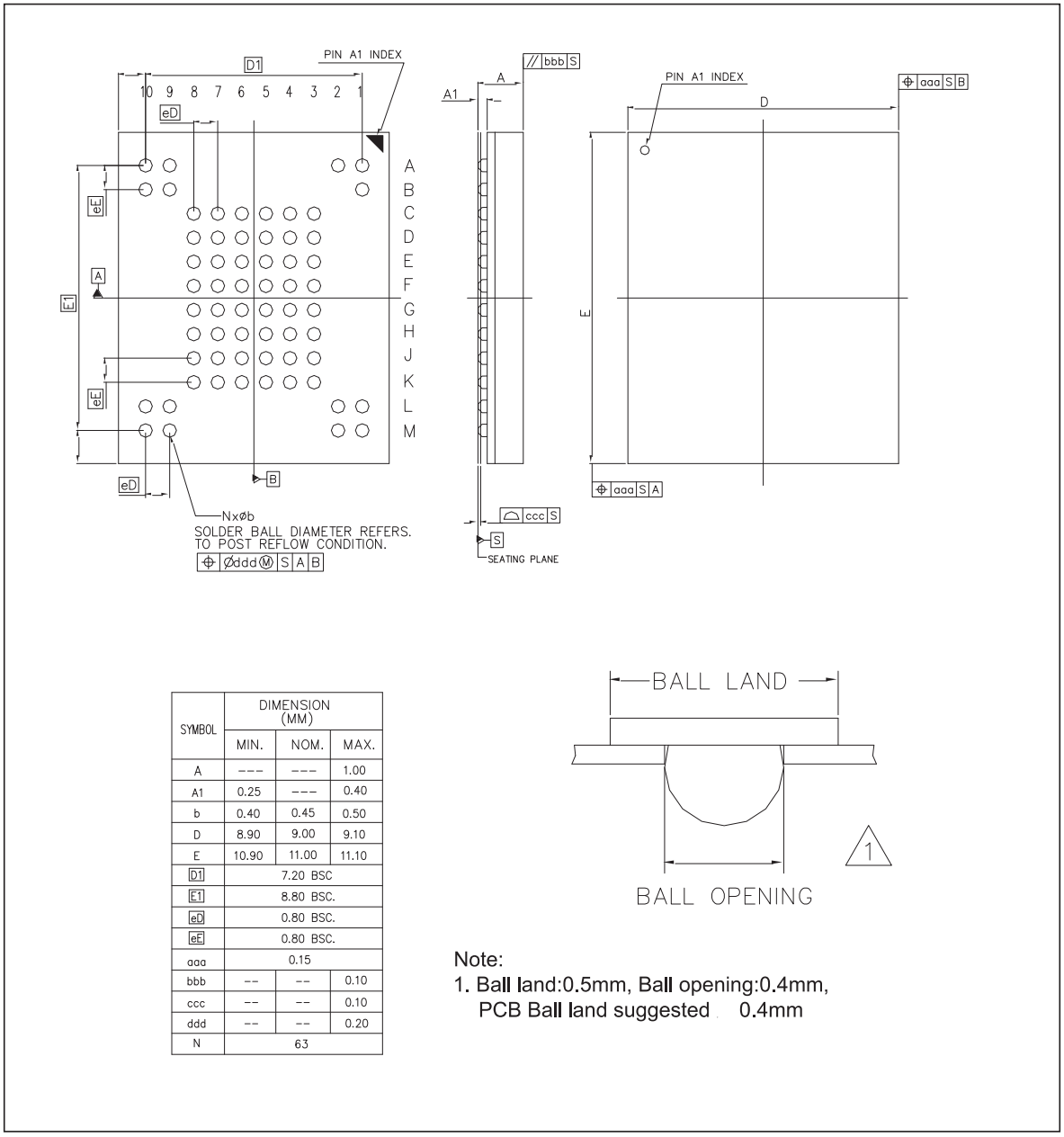



| Symbol | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.20 | — | — | 0.047 |
| A1 | 0.05 | — | — | 0.002 | — | — |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| D | 18.3 | 18.4 | 18.5 | 0.720 | 0.724 | 0.728 |
| $H_D$ | 19.8 | 20.0 | 20.2 | 0.780 | 0.787 | 0.795 |
| E | 11.9 | 12.0 | 12.1 | 0.468 | 0.472 | 0.476 |
| b | 0.17 | 0.22 | 0.27 | 0.007 | 0.009 | 0.011 |
| c | 0.10 | — | 0.21 | 0.004 | — | 0.008 |
| e | — | 0.50 | — | — | 0.020 | — |
| L | 0.50 | 0.60 | 0.70 | 0.020 | 0.024 | 0.028 |
| L1 | — | 0.80 | — | — | 0.031 | — |
| Y | — | — | 0.10 | — | — | 0.004 |
| θ | 0 | — | 5 | 0 | — | 5 |

Figure 13-1 TSOP 48-pin 12x20mm


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## 13.2 Fine-Pitch Ball Grid Array 63-ball




| SYMBOL | DIMENSION (MM) | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | --- | --- | 1.00 |
| A1 | 0.25 | --- | 0.40 |
| b | 0.40 | 0.45 | 0.50 |
| D | 8.90 | 9.00 | 9.10 |
| E | 10.90 | 11.00 | 11.10 |
| D1 | 7.20 BSC | | |
| E1 | 8.80 BSC. | | |
| eD | 0.80 BSC. | | |
| eE | 0.80 BSC. | | |
| aaa | 0.15 | | |
| bbb | -- | -- | 0.10 |
| ccc | -- | -- | 0.10 |
| ddd | -- | -- | 0.20 |
| N | 63 | | |

Note:
1. Ball land:0.5mm, Ball opening:0.4mm,
   PCB Ball land suggested 0.4mm

Figure 13-2 Fine-Pitch Ball Grid Array 63-Ball


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## 14. ORDERING INFORMATION

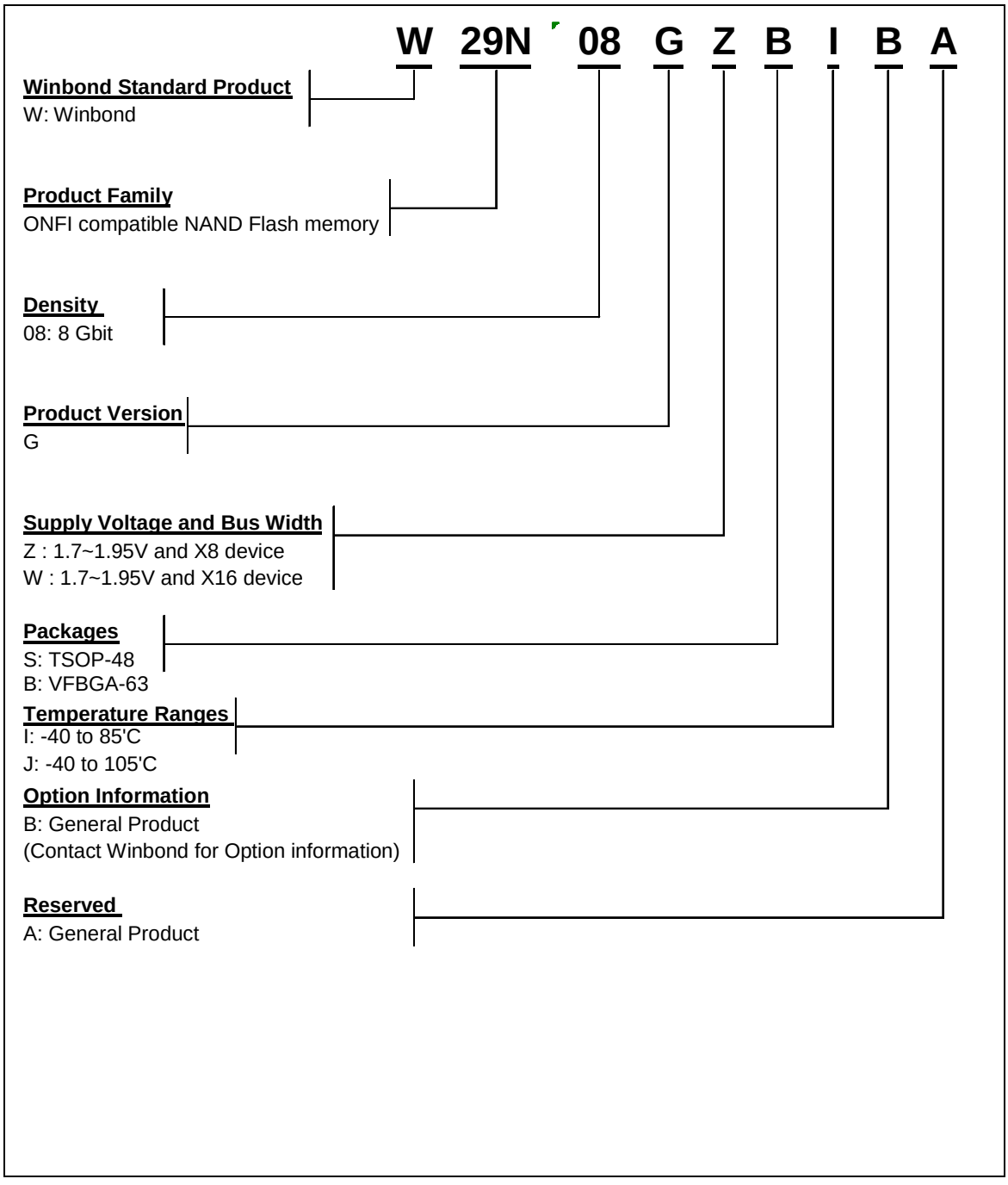



Figure 14-1 Ordering Part Number Description


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## 15. VALID PART NUMBERS

The following table provides the valid part numbers for the W29N08GW/Z NAND Flash Memory. Please contact Winbond for specific availability by density and package type. Winbond NAND Flash memories use a 12-digit Product Number for ordering.

Part Numbers for Industrial Temperature:

| PACKAGE TYPE | DENSITY | VCC | BUS | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|---|---|
| **S** TSOP-48 | 8G-bit | 1.8V | X8 | W29N08GZSIBA | W29N08GZSIBA |
| **B** VFBGA-63 | 8G-bit | 1.8V | X8 | W29N08GZBIBA | W29N08GZBIBA |
| **B** VFBGA-63 | 8G-bit | 1.8V | X16 | W29N08GWBIBA | W29N08GWBIBA |

Table 15-1 Part Numbers for Industrial Temperature

Part Numbers for Industrial Plus Temperature:

| PACKAGE TYPE | DENSITY | VCC | BUS | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|---|---|
| **S** TSOP-48 | 8G-bit | 1.8V | X8 | W29N08GZSJBA | W29N08GZSJBA |
| **B** VFBGA-63 | 8G-bit | 1.8V | X8 | W29N08GZBJBA | W29N08GZBJBA |
| **B** VFBGA-63 | 8G-bit | 1.8V | X16 | W29N08GWBJBA | W29N08GWBJBA |

Table 15-2 Part Numbers for Industrial Plus Temperature


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## 16. REVISION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---|---|---|---|
| 0.1 | 3/20/2018 | | New Create as Preliminary |
| A | 4/25/2018 | 22-23 | Remove Preliminary<br>Update Table 9-3 |
| B | 1/07/2019 | 7 | Update sequential read cycle |
| C | 4/15/2019 | 8, 69 | Remove W29N08GWSIBA |
| D | 10/04/2019 | 24 | Add CRC value |
| E | 12/17/2019 | 7, 48, 68<br>50<br>69 | Added max temperature for Industrial Plus Grade<br>Added ISB2 for Industrial Plus Grade<br>Added valid part numbers for Industrial Plus Grade |

Table 16-1 History Table

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All other marks are the property of their respective owner.

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