256M-BIT
3.0-VOLT PARALLEL FLASH MEMORY WITH PAGE MODE

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GENERAL DESCRIPTION

The W29GL256P Parallel Flash memory provides a storage solution for embedded system applications that require better performance, lower power consumption and higher density. The device has a random access speed of 90ns and a fast page access speed of 25ns, as well as significantly faster program and erase time than the products available on the market today. The W29GL256P also offers special features such as Compatible Manufacturer ID that makes the device industry standard compatible without the need to change firmware.

1 FEATURES

- **64k-Word/128k-Byte uniform sector architecture**
  - Total 256 uniform sectors
- **32-Word/64-Byte write buffer**
  - Reduces total program time for multiple-word updates
- **8-Word/16-Byte page read buffer**
- **Secured Silicon Sector area**
  - Programmed and locked by the customer or during production
  - 128-word/256-byte sector for permanent, safe identification using an 8-word/16-byte random electronic serial number
- **Enhanced Sector Protect using Dynamic and Individual mechanisms**
- **Polling/Toggling methods are used to detect the status of program and erase operation**
- **Suspend and resume commands used for program and erase operations**
- **More than 100,000 erase/program cycles**
- **More than 20-year data retention**
- **Software and Hardware write protection**
  - Write-Protect all or a portion of memory
  - Enable/Disable protection with #WP pin
  - Top or bottom array protection
- **Low power consumption**
- **Deep power down mode**
- **Industrial temperature range**
- **Faster Erase and Program time**
  - Erase is 1.5x faster than industry standard
  - Program is 2x faster than industry standard
  - Allows for improved production throughput and faster field updates
- **CFI (Common Flash Interface) support**
- **Single 3V Read/Program/Erase (2.7 - 3.6V)**
- **Enhanced Variable IO control**
  - All input levels (address, control, and DQ) and output levels are determined by voltage on the E_{VIO} input. E_{VIO} ranges from 1.65 to V_{CC}
- **#WP/ACC Input**
  - Accelerates programming time (when V_{HH} is applied) for greater throughput during system production
  - Protects first or last sector regardless of sector protection settings
- **Hardware reset input (#RESET) resets device**
- **Ready/#Busy output (RY/#BY) detects completion of program or erase cycle**
- **Packages**
  - 56-pin TSOP
  - 64-ball LFBGA

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2 PIN CONFIGURATION

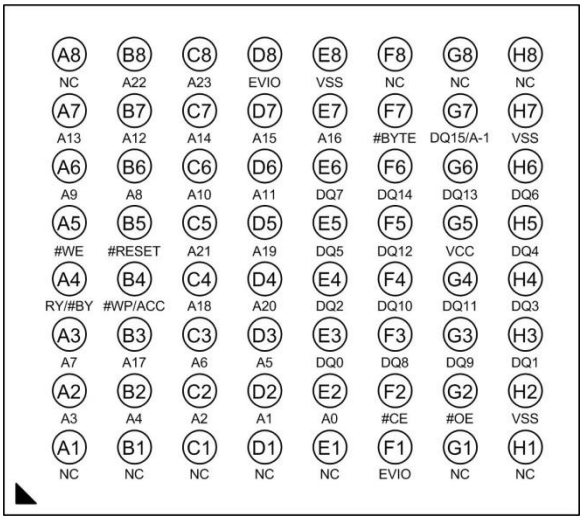


Figure 2-1 LFBGA64 TOP VIEW

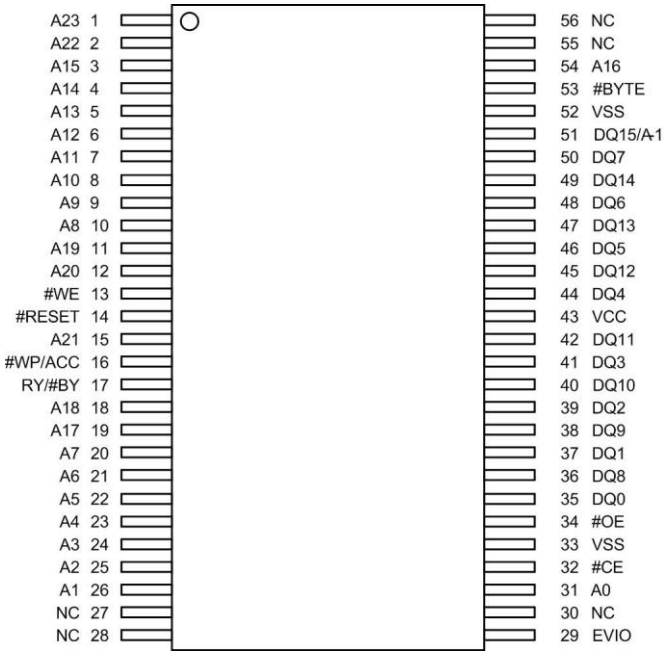


Figure 2-2 56-PIN STANDARD TSOP (TOP VIEW)

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3 BLOCK DIAGRAM

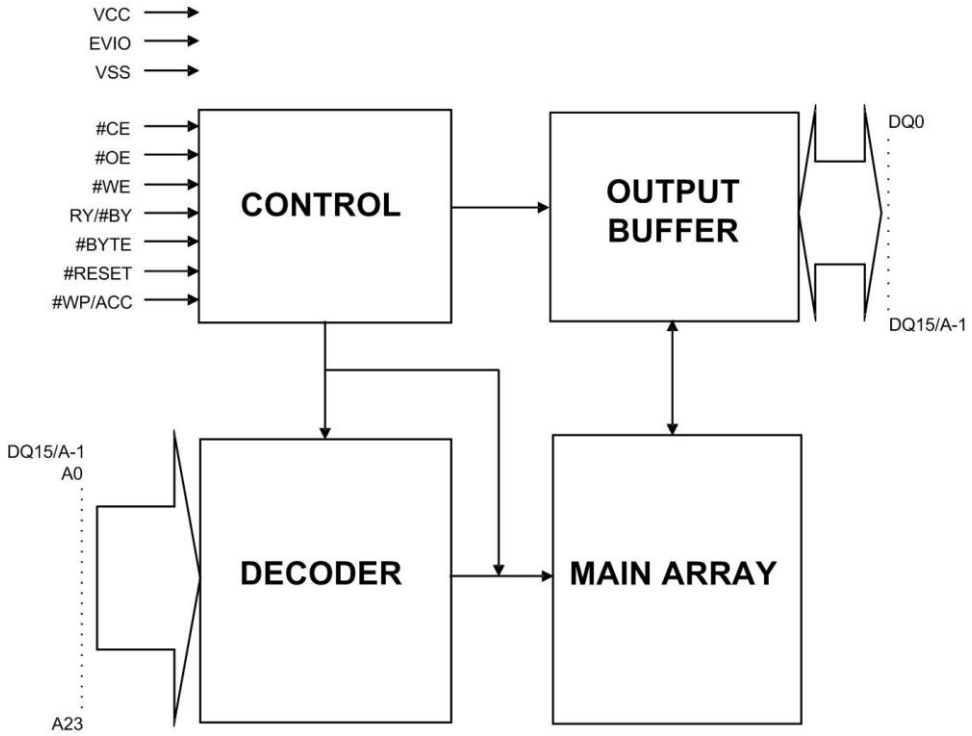


Figure 3-1 Block Diagram

4 PIN DESCRIPTION

SYMBOL	PIN NAME	
A0-A23	Address Inputs	
DQ0-DQ14	Data Inputs/Outputs	
DQ15/A-1	Word mode	DQ15 is Data Input/Output
	Byte mode	A-1 is Address Input
#CE	Chip Enable	
#OE	Output Enable	
#WE	Write Enable	
#WP/ACC	Hardware Write Protect/ Acceleration Pin	
#BYTE	Byte Enable	
#RESET	Hardware Reset	
RY/#BY	Ready/Busy Status	
VCC	Power Supply	
EVIO	Enhanced Variable IO Supply	
VSS	Ground	
NC	No Connection	

Table 4-1 Pin Description

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5 ARRAY ARCHITECTURE

5.1 Sector Address Table

Sector	Sector Address A23-A16	Sector Size (KByte/KWord)	X8 Start / Finish		X16 Start / Finish	
SA00	0000000	128/64	000000h	01FFFFh	000000h	00FFFFh
SA01	0000001	128/64	020000h	03FFFFh	010000h	01FFFFh
. . .	. . .	. . .	. . .	. . .	. . .	. . .
SA254	11111110	128/64	1FC0000h	1FDFFFFh	FE0000h	FEFFFFh
SA255	11111111	128/64	1FE0000h	1FFFFFFh	FF0000h	FFFFFFh

Table 5-1 Sector Address

Note: The address range [A23:A-1] in byte mode (#BYTE = VIL) or [A23:A0] in word mode (#BYTE = VIH)

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6 FUNCTIONAL DESCRIPTION

6.1 Device Bus Operation

Mode Select	#Reset	#CE	#WE	#OE	Address(4)	Data I/O DQ[7:0]	#BYTE VIL Data I/O DQ[15:8]	#BYTE VIH	#WP/ACC
Device Reset	L	X	X	X	X	High-Z	High-Z	High-Z	L/H
Standby Mode	VCC±0.3V	VCC±0.3V	X	X	X	High-Z	High-Z	High-Z	H
Output Disable	H	L	H	H	X	High-Z	High-Z	High-Z	L/H
Read Mode	H	L	H	L	AIN	DOUT	DQ[14:8]=High-Z DQ15=A-1	DOUT	L/H
Write	H	L	L	H	AIN	DIN		DIN	Note(1,2)
Accelerated Program	H	L	L	H	AIN	DIN		DIN	VHH

Table 6-1 Device Bus Operation

Notes:
1. The first or last sector was protected if #WP/ACC=VIL.
2. When #WP/ACC = VIH, the protection conditions of the outmost sector depends on previous protection conditions. Refer to the enhanced protect feature.
3. DQ[15:0] are input (DIN) or output (DOUT) pins according to the requests of instruction sequence, sector protection, or data polling algorithm.
4. In Word Mode (Byte#=VIH), the addresses are A23 to A0. In Byte Mode (Byte#=VIL), the addresses are A23 to A-1 (DQ15),.

Description		Control Inputs #CE	#WE	#OE	A23 ~12	A11 ~10	A9	A8 ~7	A6	A5 ~4	A3 ~2	A1	A0	DQ [7:0]	DQ[15:8] BYTE	WORD
Read Silicon ID Manufacturer Code		L	H	L	X	X	VHH	X	L	X	L	L	L	EF	X	00
Device ID	Cycle 1	L	H	L	X	X	VHH	X	L	X	L	L	H	7E	X	22
	Cycle 2	L	H	L	X	X	VHH	X	L	X	H	H	L	22	X	22
	Cycle 3	L	H	L	X	X	VHH	X	L	X	H	H	H	01	X	22
Sector Lock Status Verification(1)		L	H	L	SA	X	VHH	X	L	X	L	H	L	01/00	X	X
Secure Sector (H) (2)		L	H	L	X	X	VHH	X	L	X	L	H	H	99/19	X	X
Secure Sector (L) (2)		L	H	L	X	X	VHH	X	L	X	L	H	H	89/09	X	X

Table 6-2 Device Bus Operation (continue)

Notes:
1. Sector unprotected code:00h. Sector protected code:01h.
2. Factory locked code: #WP protects high address sector: 99h. #WP protects low address sector: 89h. Factory unlocked code: #WP protects high address sector: 19h. #WP protects low address sector: 09h

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6.2 Instruction Definitions

The device operation can be initiated by writing specific address and data commands or sequences into the instruction register. The device will be reset to reading array data when writing incorrect address and data values or writing them in the improper sequence.

The addresses will be latched on the falling edge of #WE or #CE, whichever happens later; while the data will be latched on the rising edge of #WE or #CE, whichever happens first. Please refer to timing waveforms.

6.2.1 Reading Array Data

The default state after power up or a reset operation is the Read mode.

To execute a read operation, the chip is enabled by setting #CE and #OE active and #WE high. At the same time, the required address or status register location is provided on the address lines. The system reads the addressed location contents on the Data IO pins after the t_{CE} and t_{OE} timing requirements have been met. Output data will not be accessible on the Data IO pins if either the device or it's outputs are not enabled by #CE or #OE being High, and the outputs will remain in a tri-state condition.

When the device completes an embedded memory operation (i.e., Program, automatic Chip Erase or Sector Erase) successfully, it will return to the Read mode and from any address in the memory array the data can be read. However, If the embedded operation fails to complete, by verifying the status register bit DQ5 (exceeds time limit flag) going high during the operations, at this time system should execute a Reset operation causing the device to return to Read mode.

Some operating states require a reset operation to return to Read mode such as:

- Time-out condition during a program or erase failed condition, indicated by the status register bit DQ5 going High during the operation. Failure during either of these states will prevent the device from automatically returning to Read mode.
- During device Auto Select mode or CFI mode, a reset operation is required to terminate their operation.

In the above two situations, the device will not return to the Read mode unless a reset operation is executed (either hardware reset or software reset instruction) or the system will not be able to read array data.

The device will enter Erase-Suspended Read mode if the device receives an Erase Suspend instruction while in the Sector Erase state. The erase operation will pause (after a time delay not exceeding 20µs) prior to entering Erase-Suspend Read mode. At this time data can be programmed or read from any sector that is not being erased. Another way to verify device status is to read the addresses inside the sectors being erased. This will only provide the contents of the status register.

Program operation during Erase-Suspend Read mode of valid sector(s) will automatically return to the Erase-Suspend Read mode upon successful completion of the program operation.

An Erase Resume instruction must be executed to exit the Erase-Suspended Read mode, at which time suspended erase operations will resume. Erase operation will resume where it left off and continue until successful completion unless another Erase Suspend instruction is received.

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6.2.2 Page Mode Read

The Page Mode Read has page sizes of 16 bytes or 8 words. The higher addresses A[23:3] accesses the desired page. To access a particular word or byte in a page, it is selected by A[2:0] for word mode and A[2:0,A-1] for byte mode. Page mode can be turned on by keeping “page-read address” constant and changing the “intra-read page” addresses. The page access time is t_{AA} or t_{CE}, followed by t_{PA} for the page read time. When #CE toggles, access time is t_{AA} or t_{CE}.

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6.2.3 Device Reset Operation

Pulling the #RESET pin Low for a period equal to or greater than tRP will return the device to Read mode. If the device is performing a program or erase operation, the reset operation will take at most a period of tREADY1 before the device returns to Read mode. The RY/#BY pin will remain Low (Busy Status) until the device returns to Read mode.

Note, the device draws larger current if the #RESET pin is held at voltages greater that GND+0.3V and less than or equal to VIL. When the #RESET pin is held a GND±0.3V, the device only consumes Reset (ICC5) current.

It is recommended to tie the system reset signal to the #RESET pin of the flash memory. This allows the device to be reset with the system and puts it in a state where the system can immediately begin reading boot code from it.

Executing the Reset instruction will reset the device back to the Read mode in the following situations:

- During an erase instruction sequence, before the full instruction set is completed.
- Sector erase time-out period
- Erase failed, while DQ5 is High.
- During program instruction sequence, before the full instruction set is completed, including the erase-suspended program instruction.
- Program failed, while DQ5 is High as well as the erase-suspended program failure.
- Auto-select mode
- CFI mode
- The user must issue a reset instruction to reset the device back to the Read mode when the device is in Auto-Select mode or CFI mode, or when there is a program or erase failure (DQ5 is High).
- When the device is performing a Programming (not program fail) or Erasing (Not erase fail) function, the device will ignore reset commands.

6.2.4 Standby Mode

Standby mode is entered when both #RESET and #CE are driven to VCC ±300mV (inactive state). At this time output pins are placed in the high impedance state regardless of the state of the #WE or #OE pins and the device will draw minimal standby current (ICC4). If the device is deselected during erase or program operation, the device will draw active current until the operation is completed.

6.2.5 Output Disable Mode

The #OE pin controls the state of the Data IO pins. If #OE is driven High (VIH), all Data IO pins will remain at high impedance and if driven Low, the Data IO pins will drive data (#OE has no affect on the RY/BY# output pin).

6.2.6 Write Operation

To execute a write operation, Chip Enable (#CE) pin is driven Low and the Output Enable (#OE) is pulled high to disable the Data IO pins to a high impedance state. The desired address and data should be present on the appropriate pins. Addresses are latched on the falling edge of either #WE or #CE and Data is latched on the rising edge or either #CE or #WE. To see an example, please refer to timing diagrams in Figure 8-5 and Figure 8-15. If an invalid write instruction, not defined in this datasheet is written to the device, it may put the device in an undefined state.

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6.2.7 Byte/Word Selection

To choose between the Byte or Word mode, the #BYTE input pin is used to select how the data is input/output on the Data IO pins and the organization of the array data. If the #BYTE pin is driven High, Word mode will be selected and all 16 Data IO pins will be active. If the #BYTE is pulled Low, Byte mode will be active and only Data IO DQ[7:0] will be active. The remaining Data IO pins (DQ[14:8]) will be in a high impedance state and DQ15 becomes the A-1 address input pin.

6.2.8 Automatic Programming of the Memory Array

To program the memory array in Byte or Word mode, refer to the Instruction Definition Tables for correct cycle defined instructions that include the 2 unlocking instruction cycles, the A0h program cycle instruction and subsequent cycles containing the specified address location and the byte or word desired data content, followed by the start of the embedded algorithm to automatically program the array.

Once the program instruction sequence has been executed, the internal state machine commences execution of the algorithms and timing necessary for programming and cell verification. Included in this operation is generating suitable program pulses, checking cell threshold voltage (V_T) margins, and if any cells do not pass verification or have acceptable margins, repetitive program pulse sequence will be cycled again. The internal process mechanisms will protect cells that do pass margin and verification tests from being over-programmed by prohibiting further program pulses to passing cells as failing cells continue to be run through the internal programming sequence until the pass.

This feature allows the user to only perform the auto-programming sequence once and the device state machine takes care of the program and verification process.

Array bits during programming can only change a bit status of “1” (erase state) to a “0” (programmed state). It is not possible to do the reverse with a programming operation. This can only be done by first performing an erase operation. Keep in mind, the internal write verification only checks and detects errors in cases where a “1” is not successfully programmed to “0”.

During the embedded programming algorithm process any commands written to the device will be ignored, except hardware reset or a program suspend instruction. Hardware reset will terminate the program operation after a period of time, not to exceed 10µs. If in the case a Program Suspend was executed, the device will enter the program suspend read mode. When the embedded program algorithm is completed or the program is terminated by a hardware reset, the device will return to Read mode.

The user can check for completion by reading the following bits in the status register, once the embedded program operation has started:

Status	DQ7	DQ6	DQ5	DQ1	RY/#BY[1]
In progress	DQ7#	Toggling	0	0	0
Exceeded time limit	DQ7#	Toggling	1	N/A	0

Table 6-3 Polling During Embedded Program Operation

Note:
1. RY/#BY is an open drain output pin and should be connected to VCC through a high value pull-up resistor.

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6.2.9 Erasing the Memory Array

Sector Erase and Chip Erase are the two possible types of erase operations executed on the memory array. Sector Erase operation erases one or more selected sectors and this can be simultaneous. Chip Erase operation erases the entire memory array, except for any protected sectors.

6.2.9.1 Sector Erase

The sector erase operation returns all selected sectors in memory to the “1” state, effectively clearing all data. This action requires six instruction cycles to commence the erase operation. The unlock sequence is the first two cycles, followed by the configuration cycle, the fourth and fifth are also ”unlock cycles”, and the Sector Erase instruction is the sixth cycle. An internal 50µs time-out counter is started once the sector erase instruction sequence has been completed. During this time, additional sector addresses and Sector Erase commands may be issued, thus allowing for multiple sectors to be selected and erased simultaneously. Once the 50µs time-out counter has reached its limit, no additional command instructions will be accepted and the embedded sector erase algorithm will commence.

Note, that the 50µs time-out counter restarts after every sector erase instruction sequence. The device will abort and return to Read mode, if any instruction other than Sector Erase or Erase Suspend is attempted during the time-out period.

Once the embedded sector erase algorithm begins, all instructions except Erase Suspend or Hardware Reset will be ignored. The hardware reset will abort the erase operation and return the device to the Read mode.

The embedded sector erase algorithm status can be verified by the following:

Status	DQ7	DQ6	DQ5	DQ3[1]	DQ2	RY/#BY[2]
Time-out period	0	Toggling	0	0	Toggling	0
In progress	0	Toggling	0	1	Toggling	0
Exceeded time limit	0	Toggling	1	1	Toggling	0

Table 6-4 Polling During Embedded Sector Erase Operation

Note:

1. The DQ3 status bit is the 50µs time-out indicator. When DQ3=0, the 50µs time-out counter has not yet reached zero and the new Sector Erase instruction maybe issued to specify the address of another sector to be erased. When DQ3=1, the 50µs time-out counter has expired and the Sector Erase operation has already begun. Erase Suspend is the only valid instruction that maybe issued once the embedded erase operation is underway.
2. RY/#BY is an open drain output pin and should be connected to VCC through a high value pull-up resistor.
3. When an attempt is made to erase only protected sector(s), the erase operation will abort thus preventing any data changes in the protected sector(s). DQ7 will output “0” and DQ6 will toggle briefly (100µs or less) before aborting and returning the device to Read mode. If unprotected sectors are also specified, however, they will be erased normally and the protected sector(s) will remain unchanged.
4. DQ2 is a localized indicator showing a specified sector is undergoing erase operation or not. DQ2 toggles when user reads at the addresses where the sectors are actively being erased (in erase mode) or to be erased (in erase suspend mode).

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6.2.9.2 Chip Erase

The Chip Erase operation returns all memory locations containing a bit state of “0” to the “1” state, effectively clearing all data. This action requires six instruction cycles to commence the erase operation. The unlock sequence is the first two cycles, followed by the configuration cycle, the fourth and fifth are also ”unlock cycles”, and the sixth cycle initiates the chip erase operation.

Once the chip erase algorithm begins, no other instruction will be accepted. However, if a hardware reset is executed or the operating voltage is below acceptable levels, the chip erase operation will be terminated and automatically returns to Read mode.

The embedded chip erase algorithm status can be verified by the following:

Status	DQ7	DQ6	DQ5	DQ2	RY/#BY[1]
In progress	0	Toggling	0	Toggling	0
Exceeded time limit	0	Toggling	1	Toggling	0

Table 6-5 Polling During Embedded Chip Erase Operation

Note:
1. RY/#BY is an open drain pin and should be connected to VCC through a high value pull-up resistor.

6.2.10 Erase Suspend/Resume

If there is a sector erase operation in progress, an Erase Suspend instruction is the only valid instruction that may be issued. Once the Erase Suspend instruction is executed during the 50µs time-out period following a Sector Erase instruction, the time-out period will terminate right away and the device will enter Erase-Suspend Read mode. If an Erase Suspend instruction is executed after the sector erase operation has started, the device will not enter Erase-Suspended Read mode until approximately 20µs (5µs typical) time has elapsed. To determine the device has entered the Erase-Suspend Read mode, use DQ6, DQ7 and RY/#BY status to verify the state of the device.

Once the device has entered Erase-Suspended Read mode, it is possible to read or program any sector(s) except those being erased by the erase operation. Only the contents of the status register is present when attempting to read a sector that has been scheduled to erase or be programmed when in the suspend mode. A resume instruction must be executed and recommend checking DQ6 toggle bit status, before issuing another erase instruction.

The status register bits can be verified to determine the current status of the device:

Status	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/#BY
Erase suspend read in erase suspended sector	1	No toggle	0	N/A	Toggle	N/A	1
Erase suspend read in non-erase suspended sector	Data	Data	Data	Data	Data	Data	1
Erase suspend program in non-erase suspended sector	DQ7#	Toggle	0	N/A	N/A	N/A	0

Table 6-6 Polling During Embedded Erase Suspend

Instruction sets such as read silicon ID, sector protect verify, program, CFI query and erase resume can also be executed during Erase-Suspend mode, except sector and chip erase.

6.2.11 Sector Erase Resume

Only in the Erase-Suspended Read mode can the Sector Erase Resume instruction be a valid command. Once erase resumes, another Erase Suspend instruction can be executed, but allow a 400µs interval between Erase Resume and the next Erase Suspend instruction.

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6.2.12 Program Suspend/Resume

Once a program operation is in progress, a Program Suspend is the only valid instruction that maybe executed. Verifying if the device has entered the Program-Suspend Read mode after executing the Program-Suspend instruction, can be done by checking the RY/#BY and DQ6. Programming should halt within 15μs maximum (5μs typical).

Any sector(s) can be read except those being program suspended. Trying to read a sector being program suspended is invalid. Before another program operation can be executed, a Resume instruction must be performed and DQ6 toggling bit status has to be verified. Use the status register bits shown in the following table to determine the current state of the device:

Status	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/#BY
Program suspend read in program suspended sector	Invalid						1
Program suspend read in non-program suspended sector	Data	Data	Data	Data	Data	Data	1

Table 6-7 Polling During Embedded Program Suspend

Instruction sets such as read silicon ID, sector protect verify, program, CFI query can also be executed during Program/Erase-Suspend mode.

6.2.13 Program Resume

The program Resume instruction is valid only when the device is in Program-Suspended mode. Once the program resumes, another Program Suspend instruction can be executed. Insure there is at least a 5μs interval between Program Resume and the next Suspend instruction.

6.2.14 Write Buffer Programming Operation

Write Buffer Programming Operation, programs 64bytes or 32words in a two step programming operation. To begin execution of the Write Buffer Programming, start with the first two unlock cycles, the third cycle writes the programming Sector Address destination followed by the Write Buffer Load Instruction (25h). The fourth cycle repeats the Sector Address, while the write data is the number of intended word locations to be written minus one. (Example, if the number of word locations to be written is 9, then the value would be 8h.) The 5th cycle is the first starting address/data set. This will be the first pair to be programmed and consequentially, sets the “write-buffer-page” address. Repeat Cycle 5 format for each additional address/data sets to be written to the buffer. Keep in mind all sets must remain within the write buffer page address range. If not, operation will ABORT.

The “write-buffer-page” is selected by choosing address A[23:5].

The second step will be to program the contents of the write buffer page. This is done with one cycle, containing the sector address that was used in step one and the “Write to Buffer Program Confirm” instruction (29h).

Standard suspend/resume commands can be used during the operation of the write-buffer. Also, once the write buffer programming operation is finished, it’ll return to the normal READ mode.

Write buffer programming can be conducted in any sequence. However the CFI functions, autoselect, Secured Silicon sector are not functional when program operation is in progress. Multiple write buffer programming operations on the same write buffer address range without intervention erase is accessible. Any bit in a write buffer address range cannot be programmed from 0 back to 1.

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6.2.15 Buffer Write Abort

Write Buffer Programming Sequence will ABORT, if the following condition takes place:

- The word count minus one loaded is bigger than the page buffer size (32) during, “Number of Locations to Program.”
- Sector Address written is not the same as the one specified during the Write-Buffer-Load instruction.
- If the Address/Data set is not inside the Write Buffer Page range which was set during cycle 5’s first initial write-buffer-page select address/data set.
- No “Program Confirm Instruction” after the assigned number of “data load” cycles.

After Write Buffer Abort, the status register will be DQ1=1, DQ7 = DATA# (last address loaded), DQ6=toggle, DQ5=0. This status represents a Write Buffer Programming Operation was ABORTED. A Write-to-Buffer-Abort Reset instruction sequence has to be written to reset the device back to the read array mode.

DQ1 is the bit for Buffer Write Abort. When DQ1=1, the device will abort from buffer write operation and go back to read status register shown in the following table:

Status	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/#BY
Buffer Write Busy	DQ7#	Toggle	0	N/A	N/A	0	0
Buffer Write Abort	DQ7#	Toggle	0	N/A	N/A	1	0
Buffer Write Exceeded Time Limit	DQ7#	Toggle	1	N/A	N/A	0	0

Table 6-8 Polling Buffer Write Abort Flag

6.2.16 Accelerated Programming Operation

The device will enter the Accelerated Programming mode by applying high voltage (V_{HH}) to the #WP/ACC pin. Accelerated Programming mode allows the system to skip the normal unlock sequences instruction and program byte/word locations directly. The current drawn from the #WP/ACC pin during accelerated programming is no more that I_{ACC1}. Important Note: Do not exceed 10 accelerated programs per sector. (#WP/ACC should not be held at VHH for any other function except for programming or damage to the device may occur.)

6.2.17 Automatic Select Bus Operation

There are basically two methods to access Automatic Selection Operations; Automatic Select Instructions through software commands and High Voltage applied to A9. See Automatic Select Instruction Sequence later on in this section for details of equivalent instruction operations that do not require the use of V_{HH}. The following five bus operations require A9 to be raised to V_{HH}.

6.2.17.1 Sector Lock Status Verification

To verify the protected state of any sector using bus operations, execute a Read Operation with V_{HH} applied to A9, the sector address present on address pins A[23:12], address pins A6, A3, A2, and A0 held Low, and address pins A1 held High. If DQ0 is Low, the sector is considered not protected, and if DQ0 is High, the sector is considered to be protected.

6.2.17.2 Read Silicon Manufacturer ID Code

Winbond’s 29GL-P/29GL-S families of Parallel Flash memories feature an Industry Standard compatible Manufacturer ID code of EFh. To verify the Silicon Manufacturer ID code, execute a Read Operation with VHH applied to the A9 pin and address pins A6, A3, A2, A1 and A0 are held Low. The ID code can then be read on data bits DQ[7:0].

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6.2.17.3 Read Silicon Device ID Code

To verify the Silicon Device ID Codes, execute a Read Operation with V_{HH} applied to the A9 pin and address pins A6, A3, A2, A1, and A0 have several bit combinations to return the Winbond Device ID codes of 7Eh, 22h or 01h, which is shown on the data bits DQ[7:0]. See Table 7-2.

6.2.17.4 Read Indicator Bit DQ7 for Security Sector High and Low Address

To verify that the Security Sector has been factory locked, execute a Read Operation with V_{HH} applied to A9, address pins A6, A3, and A2 are held Low, and address pins A1 and A0 are held High. If the Security Sector has been factory locked, the code 99h(Highest Address Sector) or 89h(Lowest Address Sector) will be shown on the data bits DQ[7:0]. Otherwise, the factory unlocked code of 19h(H)/09(L) will be shown.

6.2.18 Automatic Select Operations

The Automatic Select instruction show in Table 7-13 can be executed if the device is in one of the following modes; Read, Program Suspended, Erase-Suspended Read, or CFI. At which time the user can issue (two unlock cycles followed by the Automatic Select instruction 90h) to enter Automatic Select mode. Once in the Automatic Select mode, the user can query the Manufacturer ID, Device ID, Security Sector locked status, or Sector protected status multiple times without executing the unlock cycles and a Automatic Select instruction (90h) again.

Once in Automatic Select mode, executing a Reset instruction (F0h) will return the device back to the valid mode from which it left when the Automatic Select mode was first executed.

Another way previously mentioned to enter Automatic Select mode is to use one of the bus operation shown Table 7-2 in Device Bus Operation. Once the high voltage (V_{HH}) is removed from the A9 pin, the device will return back to the valid mode from which it left when the Automatic Select mode was first executed.

6.2.19 Automatic Select Instruction Sequence

Accessing the manufacturer ID, device ID, and verifying whether or not secured silicon is locked and whether or not a sector protected is the purpose of Automatic Select mode. There are four instruction cycles that comprise the Automatic Select mode. The first two cycles are write unlock commands, followed by the Automatic Select instruction (90h). The fourth cycle is a read cycle, and the user may read at any address any number of times without entering another instruction sequence. To exit the Automatic Select mode and back to read array, the Reset instruction is necessary. No other instructions are allowed except the Reset Instruction once Automatic Select mode has been selected. Refer to the following table for more detailed information.

			Address	Data (hex)	Representation
Manufacturer ID		Word	X00	EF	
		Byte	X00	EF	
Device ID	W29GL256P	Word	X01/0E/0F	227E/2222/2201	
		Byte	X02/1C/1E	7E/22/01	
Secure Silicon		Word	X03	99/19(H)	Factory locked/unlocked
				89//09(L)	
		Byte	X06	99/19(H)	Factory locked/unlocked
				89/09(L)	
Sector Protect Verify		Word	(Sector address) X02	00/01	Unprotected/protected
		Byte	Sector address) X04	00/01	Unprotected/protected

Table 6-9 Auto Select for MFR/Device ID/Secure Silicon/Sector Protect Read

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6.2.20 Enhanced Variable IO (EVIO) Control

The Enhanced Variable IO (EVIO) control allows the host system to set the voltage levels that the device generates and tolerates on all inputs and outputs (address, control, and DQ signals). EVIO range is 1.65 to VCC.

For example, a EVIO of 1.65-3.6 volts allows for I/O at the 1.8 or 3 volt levels, driving and receiving signals to and from other 1.8 or 3 V devices on the same data bus.

6.2.21 Hardware Data Protection Options

Hardware Data Protection is the second of the two main sector protections offered by the W29GL256.

6.2.21.1 #WP/ACC Option

By setting the #WP/ACC pin to VIL, the highest or lowest sector (device specific) is protected from all erase/program operations. If #WP/ACC is set High, the highest and Lowest sector revert back to the previous protected/unprotected state.

Note: The max input load current can increase, if #WP/ACC pin is at VIH when the device is put into standby mode.

6.2.21.2 VCC Write Protect

This device will not accept any write instructions when VCC is less that VWPT (VCC Write Protect Threshold). This prevents data from inadvertently being altered during power-up, power-down, a temporary power loss or to the low level of VCC. If VCC is lower that VWPT, the device automatically resets itself and will ignore write cycles until VCC is greater than VWPT. Once VCC rises above VWPT, insure that the proper signals are on the control pins to avoid unexpected program or erase operations.

6.2.21.3 Write Pulse “Glitch” Protection

Pulses less than 5ns are viewed as glitches for control signals #CE, #WE, and #OE and will not be considered for valid write cycles.

6.2.21.4 Power-up Write Inhibit

The device ignores the first instruction on the rising edge of #WE, if upon powering up the device, #WE and #CE are set at VIL and #OE is set at VIH.

6.2.21.5 Logical Inhibit

A write cycle is ignored when either #CE is at VIH, #WE is at VIH, or #OE is at VIL. A valid write cycle requires both #CE and #WE are at VIL with #OE at VIH.

6.2.22 Inherent Data Protection

The device built-in mechanism will reset to Read mode during power up to avoid accidental erasure or programming.

6.2.22.1 Instruction Completion

Invalid instruction sets will result in the memory returning to read mode. Only upon a successful completion of a valid instruction set will the device begin its erase or program operation..

6.2.22.2 Power-up Sequence

The device is placed in Read mode, during power-up sequence.

6.2.23 Power Supply Decoupling

To reduce noise effects, a 0.1µF capacitor is recommended to be connected between VCC and GND.

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6.3 Enhanced Sector Protect/Un-protect

This device is set from the factory in the Individual Protection mode of the Enhanced Sector Protect scheme. The user can disable or enable the programming or erasing operation to any individual sector or whole chip. The figure below helps describe an overview of these methods.

The device defaults to the Individual mode and all sectors are unprotected when shipped from the factory.

The following flow chart shows the detailed algorithm of Enhanced Sector Protect:

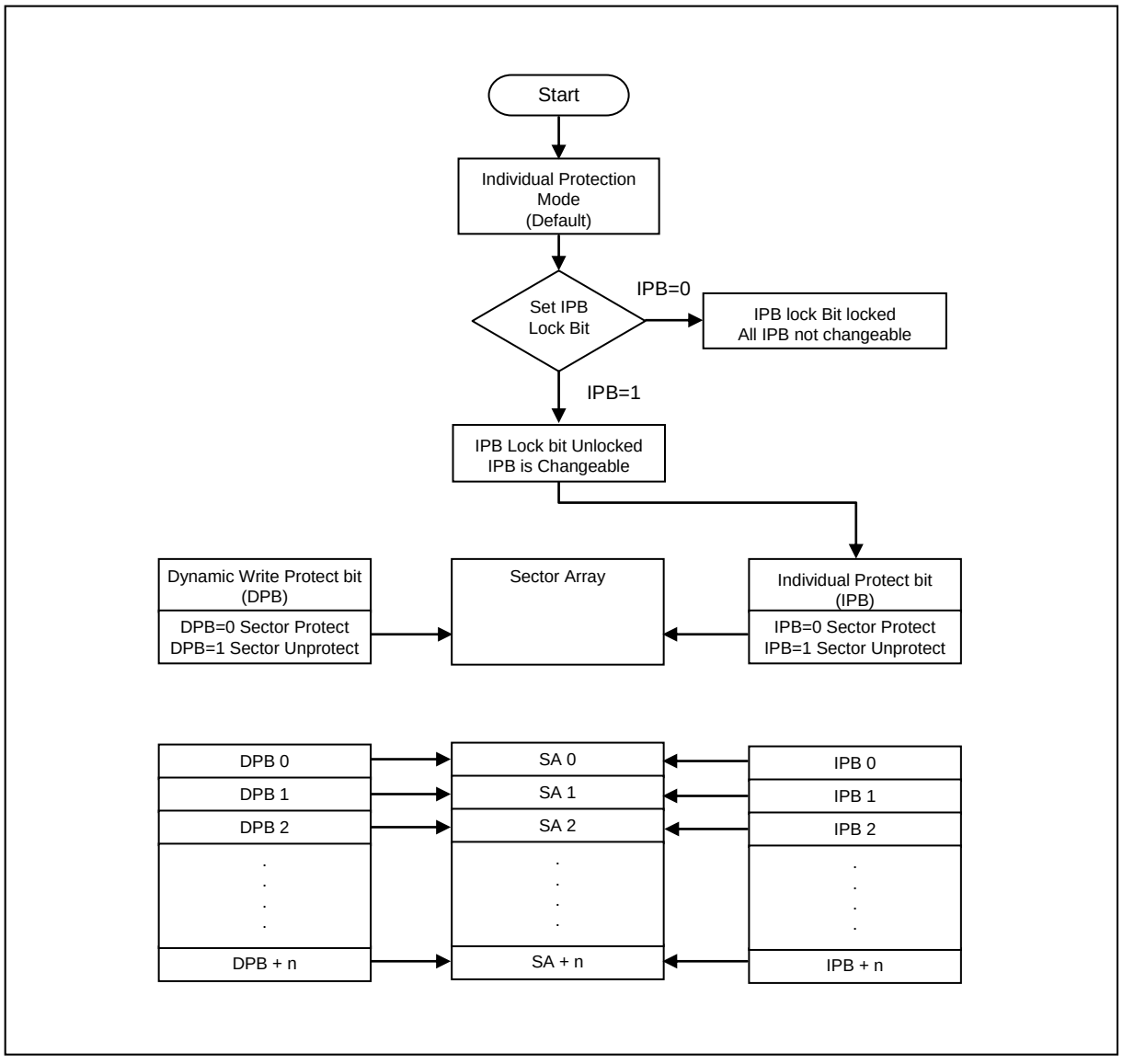


Figure 6-1 Enhanced Sector Protect/Un-protect IPB Program Algorithm

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6.3.1 Lock Register

User can choose Secured Silicon Sector Protection Bit for security sector protection method via setting the Lock Register bit, DQ0. Lock Register is a 16-bit one time programmable register. Once programmed DQ0, will be locked in that mode permanently.

Once the Instruction Set Entry instruction sequence for the Lock Register Bits is issued, all sectors read and write functions are disabled until Lock Register Exit sequence has been executed.

The memory sectors and extended memory sector protection is configured using the Lock Register.

DQ[15:1]	DQ0
Don't Care	Secured Silicon Sector Protection Bit

Table 6-10 Lock Register Bits

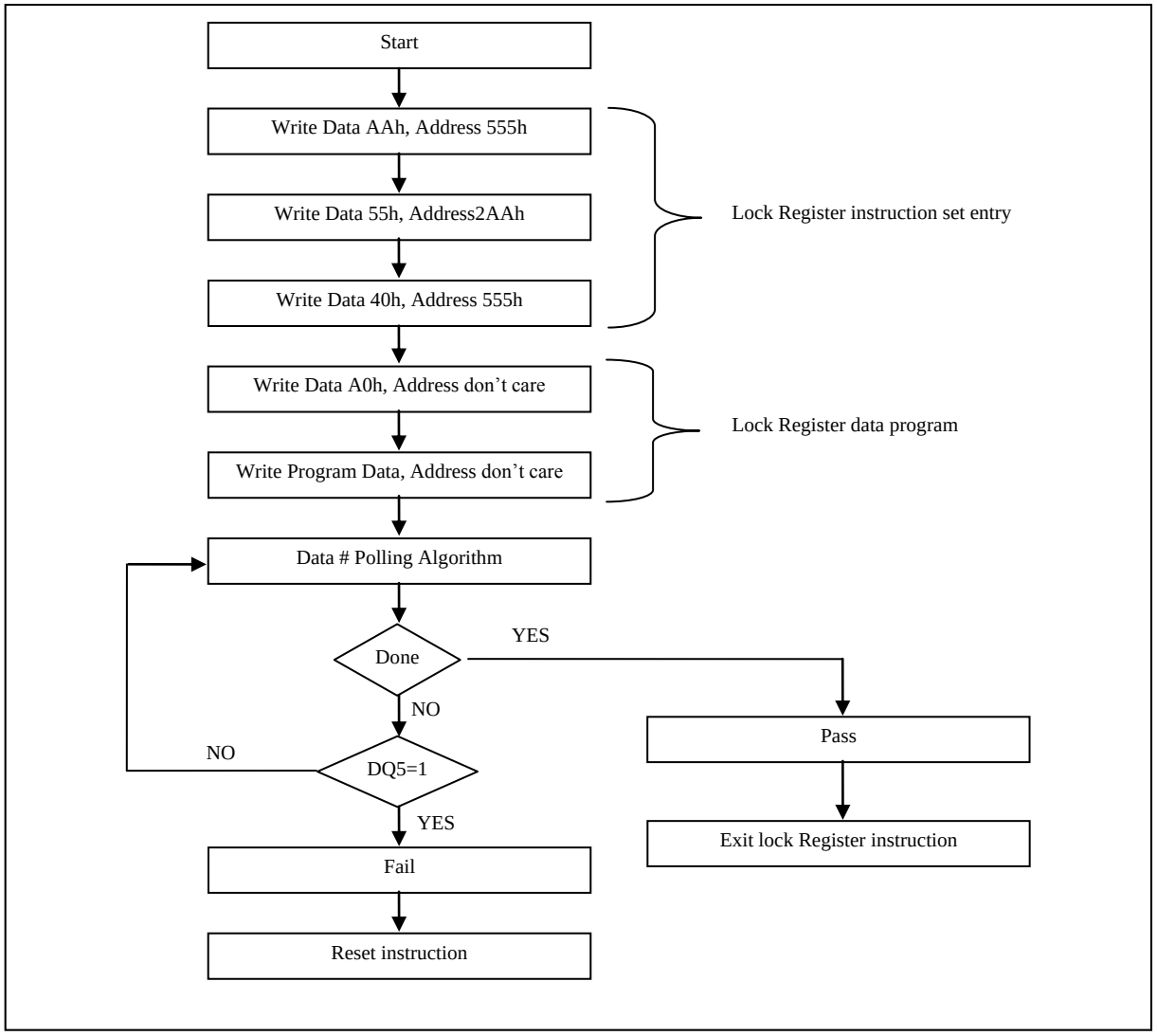


Figure 6-2 Lock Register Program Algorithm

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6.3.2 Individual (Non-Volatile) Protection Mode

6.3.2.1 Individual Protection Bits (IPB)

The Individual Protection Bit (IPB) is a nonvolatile bit, one bit per sector, with endurance equal to that of the Flash memory array. Before erasing, IPB preprogramming and verification is managed by the device, so no monitoring is necessary.

The Individual Protection Bits are set sector by sector by the IPB program instruction. Once a IPB is set to “0”, the linked sector is protected, blocking any program and/or erase functions on that sector. The IPB cannot be erased individually, but executing the “All IPB Erase” instruction will erase all IPB simultaneously. Read and write functions are disabled when IPB programming is going on for all sectors until this mode exits.

In case one of the protected sectors need to be unprotected, first, the IPB Lock Bit must be set to “1” by performing one of the following: power-cycle the device or perform a hardware reset. Second, an “All IPB Erase instruction needs to be performed. Third, Individual Protection Bits need to be set once again to reflect the desired settings and finally, the IPB Lock Bit needs to be set once again which locks the Individual Protection Bits and the device functions normally once again.

Executing an IPB Read instruction to the device is required to verify the programming state of the IPB for any given sector. Refer to the IPB Program Algorithm flow chart below for details.

Note:

- While IPB Lock Bit is set, Program and/or erase instructions will not be executed and times out without programming and/or erasing the IPB.
- For best protection results, it is recommended to execute the IPB Lock Bit Set instruction early on in the boot code. Also, protect the boot code by holding WP#/ACC = V_{IL}. Note that the IPB and DPB bits perform the same when WP#/ACC = V_{HH}, and when WP#/ACC =V_{IH}.
- While in the IPB command mode, read within that sector will bring the IPB status back for that sector. All Read must be executed by the read mode.
- Issuing the IPB Instruction Set Exit will reset the device to normal read mode enabling reads and writes for the array.

6.3.2.2 Dynamic Protection Bits (DPB)

Dynamic Protection allows the software applications to easily protect sectors against unintentional changes, although, the protection can be readily disabled when changes are needed.

All Dynamic Protection Bits (DPB) are individually linked to their associated sectors and these volatile bits can be modified individually (set or cleared). The DPB provide protection schemes for only unprotected sectors that have their associated IPB cleared. To change a DPB, the “DPB Instruction Set Entry” must be executed first and then either the DPB Set (programmed to “0”) or DPB Clear (erased to “1”) commands have to be executed. This places each sector in the protected or unprotected state separately. To exit the DPB mode, execute the “DPB Instruction Set Exit” instruction.

Note:

- When the parts are first shipped, the IPB are cleared (erased to “1”) and upon power up or reset, the DPB can be set or cleared.

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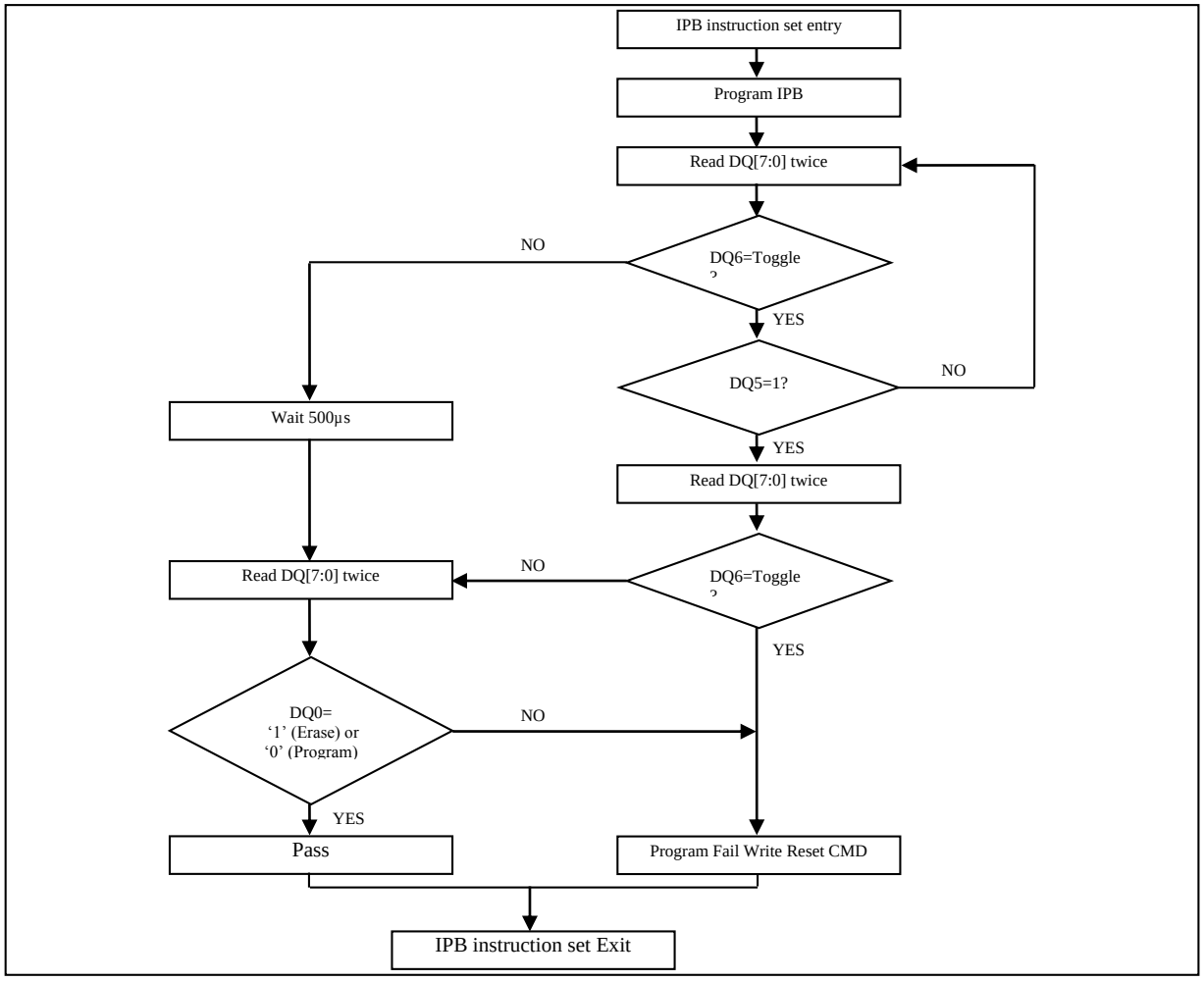


Figure 6-3 IPB Program Algorithm

Note:

1. IPB program/erase status polling flowchart: Check DQ6 toggle, when DQ6 stop toggle, the read status is 00h/01h (00h for program and 01h for erase, otherwise the status is "fail' and "exit".

6.3.2.3 Individual Protection Bit Lock Bit

The Individual Protection Bit Lock Bit (IPBLK) is a global lock bit to control all IPB states. It is a singular volatile bit. If the IPBLK is set ("0"), all IPB are locked and all sectors are protected or unprotected according to their individual IPB. When IPBLK=1 (cleared), all IPB are unlocked and allowed to be set or cleared.

To clear the IPB Lock Bit, a hardware reset or a power-up cycle must be executed.

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Sector Protection Status			Sector Status
DPB	IPBLK	IPB	
clear	clear	clear	Unprotect, DPB and IPB are changeable
clear	clear	set	Protect, DPB and IPB are changeable
clear	set	clear	Unprotect, DPB is changeable
clear	set	set	Protect, DPB is changeable
set	clear	clear	Protect, DPB and IPB are changeable
set	clear	set	Protect, DPB and IPB are changeable
set	set	clear	Protect, DPB is changeable
set	set	set	Protect, DPB is changeable

Table 6-11 Sector Protection Status Table

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6.4 Security Sector Flash Memory Region

An extra memory space length of 128 words is used as the Security Sector Region which can be factory locked or customer lockable. To enquire about the lock status of the device, the customer can issue a Security Sector Protect Verify or Security Sector Factory Protect Verify using Automatic Select Address 03h and DQ7.

The security sector region is unprotected when shipped from factory and the security silicon indicator bit (DQ7) is set to "0" for a customer lockable device. The security sector region is protected when shipped from factory and the security silicon sector indicator bit is set to "1" for a factory-locked device.

6.4.1 Factory Locked: Security Sector Programmed and Protected at factory

In a factory locked device, the Security Sector is permanently locked prior to factory shipment The ESN occupies addresses 00000h to 0000Fh in byte mode or 00000h to 00007h in word mode since the device has a 16-byte (8-word) ESN(Electronic Serial Number) in the security region.

Security Silicon Sector Address Range	Standard Factory Locked	Express Flash Factory Locked	Customer Lockable
000000h-000007h	ESN	ESN or Determined by Customer	Determined by Customer
000008h-00007Fh	Inaccessible	Determined by Customer	

Table 6-12 Factory Locked: Security Sector

6.4.2 Customer Lockable: Security Sector Not Programmed or Protected

Important Notice; Once the security silicon sector is protected (Lock Register OTP DQ0 = “0”, Security Sector indicator DQ7 bit=”0”), there is no way to unprotect the security silicon sector and the contents of the memory region can no longer be programmed.

Once the security silicon is locked and verified, an Exit Security Sector Region instruction must be executed to get back to the Read Array mode. A power cycle, or a hardware reset will also return the device to read array mode.

This region can act as extra memory space when this security feature is not utilized. It is important to note, the security sector region is a One Time Programmable (OTP) region. You can overwrite a WORD, but you cannot change the state of a programmed cell.

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6.5 Instruction Definition Tables

Instruction			1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
			ADD	DATA	ADD	DATA	ADD	DATA	ADD	DATA	ADD	DATA	ADD	DATA
Read Mode		WORD	Add	Data										
		BYTE	Add	Data										
Reset Mode		WORD	XXX	F0										
		BYTE	XXX	F0										
Automatic Select	Silicon ID	WORD	555	AA	2AA	55	555	90	X00	EF				
		BYTE	AAA	AA	555	55	AAA	90	X00	EF				
	Device ID	WORD	555	AA	2AA	55	555	90	X01	ID1	X0E	ID2	X0F	ID3
		BYTE	AAA	AA	555	55	AAA	90	X02	ID1	X1C	ID2	X1E	ID3
	Factory Protect Verify	WORD	555	AA	2AA	55	555	90	X03	99/19(H) 89/09(L)				
		BYTE	AAA	AA	555	55	AAA	90	X06	99/19(H) 89/09(L)				
	Sector Protect Verify	WORD	555	AA	2AA	55	555	90	(SA)X02	00/01				
		BYTE	AAA	AA	555	55	AAA	90	(SA)X04	00/01				
Security Sector Region		WORD	555	AA	2AA	55	555	88						
		BYTE	AAA	AA	555	55	AAA	88						
Exit Security Sector		WORD	555	AA	2AA	55	555	90	XXX	00				
		BYTE	AAA	AA	555	55	AAA	90	XXX	00				

Table 6-13 ID Reads, Sector Verify, and Security Sector Entry/Exit

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Instruction		1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		ADD	DATA	ADD	DATA	ADD	DATA	ADD	DATA	ADD	DATA	ADD	DATA
Program	WORD	555	AA	2AA	55	555	A0	Add	Data				
	BYTE	AAA	AA	555	55	AAA	A0	Add	Data				
Write to Buffer Program	WORD	555	AA	2AA	55	SA	25	SA	N-1	WA	WD	WBL	WD
	BYTE	AAA	AA	555	55	SA	25	SA	N-1	WA	WD	WBL	WD
Write to Buffer Program Abort Reset	WORD	555	AA	2AA	55	555	F0						
	BYTE	AAA	AA	555	55	AAA	F0						
Write to Buffer Program Confirm	WORD	SA	29										
	BYTE	SA	29										
Chip Erase	WORD	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
	BYTE	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Sector Erase	WORD	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
	BYTE	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
CFI Read	WORD	55	98										
	BYTE	AA	98										
Program/Erase Suspend	WORD	XXX	B0										
	BYTE	XXX	B0										
Program/Erase Resume	WORD	XXX	30										
	BYTE	XXX	30										

Table 6-14 Program, Write Buffer, CFI, Erase and Suspend

WA=WRITE ADDRESS, WD=WRITE DATA, SA=SECTOR ADDRESS, N-1=WORD COUNT, WBL=WRITEBUFFER LOCATION, ID1/ID2/ID3: REFER TO Table 7-2 FOR DETAIL ID.

Instruction			1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle	
			ADD	DATA	ADD	DATA	ADD	DATA	ADD	DATA	ADD	DATA
Deep Power Down	ENTER	WORD	555	AA	2AA	55	XXX	B9				
		BYTE	AAA	AA	555	55	XXX	B9				
	EXIT	WORD	XXX	AB								
		BYTE	XXX	AB								

Table 6-15 Deep Power Down

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Instruction			1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle	
			ADD	DATA	ADD	DATA	ADD	DATA	ADD	DATA	ADD	DATA
Lock Register	Lock Register Instruction Set Entry	WORD	555	AA	2AA	55	555	40				
		BYTE	AAA	AA	555	55	AAA	40				
	Program	WORD	XXX	A0	XXX	DATA						
		BYTE	XXX	A0	XXX	DATA						
	Read	WORD	XXX	DATA								
		BYTE	XXX	DATA								
	Lock Register Instruction Exit	WORD	XXX	90	XXX	00						
		BYTE	XXX	90	XXX	00						
Global Non-Volatile	IPB Instruction Set Entry	WORD	555	AA	2AA	55	555	C0				
		BYTE	AAA	AA	555	55	AAA	C0				
	IPB Program	WORD	XXX	A0	SA	00						
		BYTE	XXX	A0	SA	00						
	All IPB Erase	WORD	XXX	80	00	30						
		BYTE	XXX	80	00	30						
	IPB Status Read	WORD	SA	00/01								
		BYTE	SA	00/01								

Table 6-16 Lock Register and Global Non-Volatile

Instruction			1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle	
			ADD	DATA	ADD	DATA	ADD	DATA	ADD	DATA	ADD	DATA
Global Non-Volatile	IPB Instruction Set Exit	WORD	XXX	90	XXX	00						
		BYTE	XXX	90	XXX	00						
Global Volatile Freeze	IPB Instruction Set Entry	WORD	555	AA	2AA	55	555	50				
		BYTE	AAA	AA	555	55	AAA	50				
	IPB Lock Set	WORD	XXX	A0	XXX	00						
		BYTE	XXX	A0	XXX	00						
	IPB Lock Status Read	WORD	XXX	00/01								
		BYTE	XXX	00/01								
	IPB Lock Instruction Set Exit	WORD	XXX	90	XXX	00						
		BYTE	XXX	90	XXX	00						

Table 6-17 IPB Functions

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Instruction			1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle	
			ADD	DATA	ADD	DATA	ADD	DATA	ADD	DATA	ADD	DATA
Volatile	DPB Instruction Set Entry	WORD	555	AA	2AA	55	555	E0				
		BYTE	AAA	AA	555	55	AAA	E0				
	DPB Set	WORD	XXX	A0	SA	00						
		BYTE	XXX	A0	SA	00						
	DPB Clear	WORD	XXX	A0	SA	01						
		BYTE	XXX	A0	SA	01						
	DPB Status READ	WORD	SA	00/01								
		BYTE	SA	00/01								
	DPB Instruction Set Exit	WORD	XXX	90	XXX	00						
		BYTE	XXX	90	XXX	00						

Table 6-18 Volatile DPB Functions

Notes:

1. It is not recommended to use any other code that is not in the instruction definition table which can potentially enter the hidden mode.
2. For the IPB Lock and DPB Status Read "00" represents lock (protect), "01" represents unlock (unprotect).

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6.6 Common Flash Memory Interface (CFI) Mode

6.6.1 Query Instruction and Common Flash memory Interface (CFI) Mode

Through Common Flash Interface (CFI) operations it is possible to access the operating characteristics, structure and vendor specific information, such as identifying information, memory size, byte/word configuration, operating voltages and timing information of this device. From the Read array mode writing CFI Read instruction 98h to the address "55h"/"AAh" (Word/Byte, respectively), the device will gain access to the CFI Query Mode. Once in the CFI mode data can be read using the addresses given in Table 7-19 thru 7-22.

A reset instruction must be executed to exit CFI mode and the device will return to read array mode.

CFI mode: Identification Data Values (All Values in these tables are hexadecimal)

Description	Address (Word Mode)	Address (Byte Mode)	Data
Query-unique ASII string “QRY”	10h	20h	0051h
	11h	22h	0052h
	12h	24h	0059h
Primary vendor instruction set and control interface ID code	13h	26h	0006h
	14h	28h	0000h
Address for primary algorithm extended query table	15h	2Ah	0040h
	16h	2Ch	0000h
Alternate vendor instruction set and control interface ID code	17h	2Eh	0000h
	18h	30h	0000h
Address for alternate algorithm extended query table	19h	32h	0000h
	1Ah	34h	0000h

Table 6-19 CFI Mode: ID Data Values

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CFI mode: System Interface Data Values

Description	Address (Word Mode)	Address (Byte Mode)	Data
VCC supply minimum program/erase voltage	1Bh	36h	0027h
VCC supply maximum program/erase voltage	1Ch	38h	0036h
VPP supply minimum program/erase voltage	1Dh	3Ah	0000h
VPP supply maximum program/erase voltage	1Eh	3Ch	0000h
Typical timeout per single word/byte write, 2^n µs	1Fh	3Eh	0003h
Typical timeout for maximum-size buffer write, 2^n µs (00h, not support)	20h	40h	0004h
Typical timeout per individual block erase, 2^n ms	21h	42h	0009h
Typical timeout for full chip erase, 2^n ms (00h, not support)	22h	44h	0011h
Maximum timeout for word/byte write, 2^n times typical	23h	46h	0003h
Maximum timeout for buffer write, 2^n times typical	24h	48h	0005h
Maximum timeout per individual block erase, 2^n times typical	25h	4Ah	0003h
Maximum timeout for chip erase, 2^n times typical (00h, not support)	26h	4Ch	0002h

Table 6-20 CFI Mode: System Interface Data Values

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CFI mode: Device Geometry Data Values

Description	Address (Word Mode)	Address (Byte Mode)	Data
Device size = 2^n in number of bytes	27h	4Eh	0019h
Flash device interface description (02=asynchronous x8/x16)	28h	50h	0002h
	29h	52h	0000h
Maximum number of bytes in buffer write = 2^n (00h, not support)	2Ah	54h	0006h
	2Bh	56h	0000h
Number of erase regions within device (01h:uniform, 02h:boot)	2Ch	58h	0001h
Index for Erase Bank Area 1: [2E,2D] = # of same-size sectors in region 1-1 [30, 2F] = sector size in multiples of 256K-bytes	2Dh	5Ah	00FFh
	2Eh	5Ch	0000h
	2Fh	5Eh	0000h
	30h	60h	0002h
Index for Erase Bank Area 2	31h	62h	0000h
	32h	64h	0000h
	33h	66h	0000h
	34h	68h	0000h
Index for Erase Bank Area 3	35h	6Ah	0000h
	36h	6Ch	0000h
	37h	6Eh	0000h
	38h	70h	0000h
Index for Erase Bank Area 4	39h	72h	0000h
	3Ah	74h	0000h
	3Bh	76h	0000h
	3Ch	78h	0000h

Table 6-21 CFI Mode: Device Geometry Data Values

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CFI mode: Primary Vendor-Specific Extended Query Data Values

Description	Address (Word Mode)	Address (Byte Mode)	Data
Query - Primary extended table, unique ASCII string, PRI	40h	80h	0050h
	41h	82h	0052h
	42h	84h	0049h
Major version number, ASCII	43h	86h	0031h
Minor version number, ASCII	44h	88h	0033h
Unlock recognizes address (0= recognize, 1= don't recognize)	45h	8Ah	001Ch
Erase suspend (2= to both read and program)	46h	8Ch	0002h
Sector protect (N= # of sectors/group)	47h	8Eh	0001h
Temporary sector unprotect (1=supported)	48h	90h	0000h
Sector protect/Chip unprotect scheme	49h	92h	0008h
Simultaneous R/W operation (0=not supported)	4Ah	94h	0000h
Burst mode (0=not supported)	4Bh	96h	0000h
Page mode (0=not supported, 01 = 4 word page, 02 = 8 word page)	4Ch	98h	0002h
Minimum ACC(acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4Dh	9Ah	0095h
Maximum ACC(acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4Eh	9Ch	00A5h
WP# Protection 04=Uniform sectors bottom WP# protect 05=Uniform sectors top WP# protect	4Fh	9Eh	00xxh
Program Suspend (0=not supported, 1=supported)	50h	A0h	0001h

Table 6-22 CFI mode: Primary Vendor-Specific Extended Query Data Values

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7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Stress Ratings

Surrounding Temperature with Bias	-65°C to +125°C
Storage Temperature	-65°C to +150°C
VCC Voltage Range	-0.5V to +4.0V
EVIO Voltage Range	-0.5V to +4.0V
A9, #WP/ACC Voltage Range	-0.5V to +10.5V
Other Pins Voltage Range	-0.5V to VCC +0.5V
Output Short Circuit Current (less than one second)	200 mA

Table 7-1 Absolute Maximum Stress Ratings

7.2 Operating Temperature and Voltage

Industrial Grade Surrounding Temperature (TA)	-40°C to +85°C
Full VCC Range Supply Voltage	+2.7V to 3.6V
EVIO Range Supply Voltage(1)	1.65V to VCC

Table 7-2 Operating Temperature and Voltage

NOTE:
1. The EVIO feature was designed to support voltages from 1.65V to VCC. Device testing is conducted at EVIO=VCC.
2. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
3. Specifications contained within the following tables are subject to change.
4. During voltage transitions, all pins may overshoot VSS to -2.0V and VCC to +2.0V for periods up to 20ns, see below Figure.
5. Specification for the W29GL256P is preliminary. See preliminary designation at the end of this document.

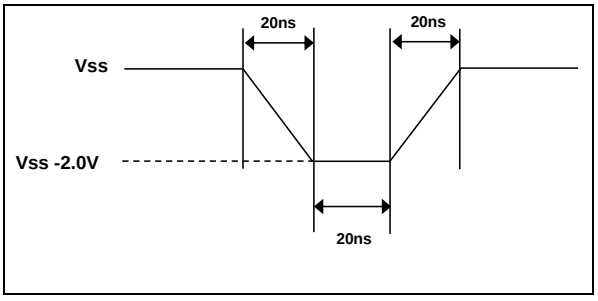


Figure 7-1 Maximum Negative Overshoot

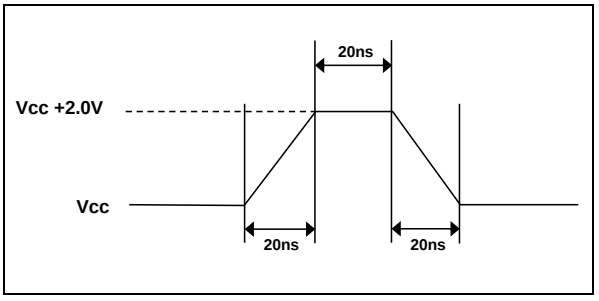


Figure 7-2 Maximum Positive Overshoot

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7.3 DC Characteristics

DESCRIPTION	SYMBOL	Conditions	MIN	TYP.	MAX	Unit
Input Leak	I_{LI}	Others			±2.0	µA
		WP#/ACC			±5.0	µA
A9 Leak	I_{LIT}	A9=10.5V			35	µA
Output Leak	I_{LO}				±1.0	µA
Read Current	I_{CC1}	#CE=V_{IL}, #OE=V_{IH}, Vcc=Vccmax:f=1MHz		6+	20	mA
		#CE=V_{IL}, #OE=V_{IH}, Vcc=Vccmax:f=5MHz		20	30	mA
		#CE=V_{IL}, #OE=V_{IH}, Vcc=Vccmax:f=10MHz		45	55	mA
Vcc Page Read Current	I_{CC2}	#CE=V_{IL}, #OE=V_{IH}, Vcc=Vccmax:f=10MHz		7	15	mA
		#CE=V_{IL}, #OE=V_{IH}, Vcc=Vccmax:f=33MHz		15	25	mA
Write Current	I_{CC3}	#CE=V_{IL}, #OE=V_{IH}, Vcc=Vccmax		20	30	mA
Standby Current	I_{CC4}	#CE, #RESET=VCC ±0.3V, #OE=V_{IH}, Vcc=Vccmax, VIL=Vss + 0.3V/-0.1V		70	100	µA
Reset Current	I_{CC5}	Vcc=Vccmax, #RESET enabled, other pins disabled		70	100	µA
Sleep Mode Current(1)	I_{CC6}	Vcc=Vccmax, V_{IH}=Vcc ±0.3, V_{IL}=Vss +(0.3v/-0.1v), #WP/ACC=V_{IH}		70	100	µA
Vcc deep power down current	I_{DPD}			1	5	µA
Accelerated Pgm Current, WP#/ACC, pin(Word/Byte)	I_{ACC1}	#CE=V_{IL}, #OE=V_{IH}		10	20	mA
Accelerated Pgm Current, Vcc pin, (Word/Byte)	I_{ACC2}	#CE=V_{IL}, #OE=V_{IH}		20	30	mA
Input Low Voltage	V_{IL}		-0.1		0.3xE_{VIO}	V
Input High Voltage	V_{IH}		0.7xE_{VIO}		E_{VIO}+0.3	V
Very High Voltage for Auto Select/ Accelerated Program	V_{HH}		9.5		10.5	
Output Low Voltage	V_{OL}	I_{OL}=100µA			0.45	V
Output High Voltage	V_{OH}	I_{OH}=-100µA	0.85xE_{VIO}			V
VCC Write Protect Threshold	V_{WPT}		2.3		2.5	V

Table 7-3 DC Characteristics

Note:
1. Sleep mode enable the lower power when address remain stable for tAA+30ns.

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7.4 Switching Test Circuits

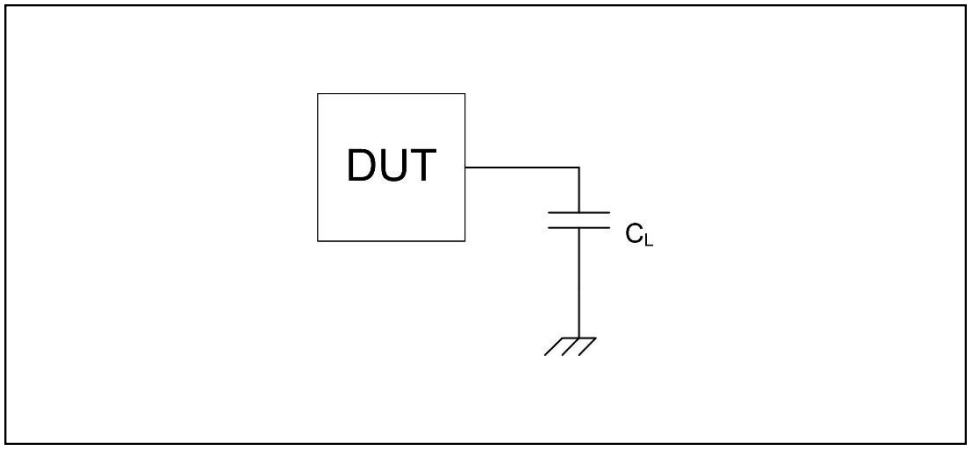


Figure 7-3 Switch Test Circuit

Test Condition	All Speeds	Unit
Output Load	1TTL gate	
Output Load Capacitance	30	pF
Rise/Fall Times	5	ns
Input Pulse levels	0.0 - EVIO	V
Input timing measurement reference level (If EVIO<VCC, the reference level is 0.5 EVIO)	0.5EVIO	V
Output timing measurement reference levels	0.5EVIO	V

Table 7-4 Test Specification

7.4.1 Switching Test Waveform

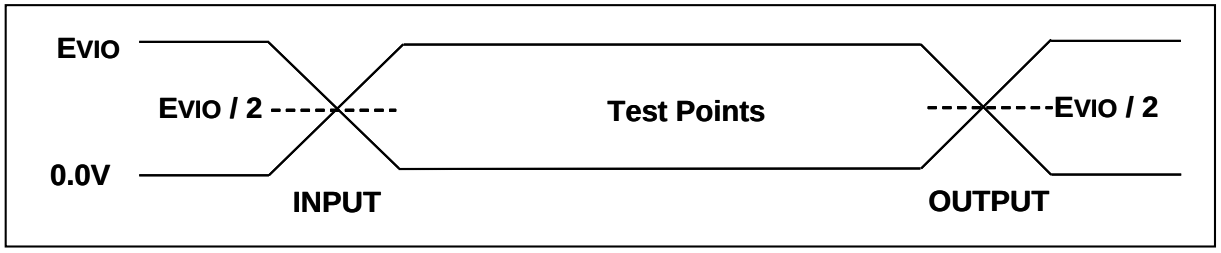


Figure 7-4 Switching Test Waveform

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7.5 AC Characteristics

Description		Symbol		Vcc=2.7V~3.6V			
		ALT	STD	Min	Typ	Max	Units
Valid Data Output after Address	E_{VIO} = V_{CC} ≥ 3V	t_{ACC}	t_{AA}			90	ns
	E_{VIO}=1.65V to V_{CC}(1)					100	ns
Page Access Time	E_{VIO}=V_{CC}	t_{PACC}	t_{PA}			25	ns
	E_{VIO}=1.65V to V_{CC}(1)					35	ns
Valid data output after #CE low	E_{VIO} = V_{CC} ≥ 3V		t_{CE}			90	ns
	E_{VIO}=1.65V to V_{CC}(1)					100	ns
Valid data output after #OE low	E_{VIO}=V_{CC}		t_{OE}			25	ns
	E_{VIO}=1.65V to V_{CC}(1)					35	ns
Read Period Time	E_{VIO} = V_{CC} ≥ 3V		t_{RC}	90			ns
	E_{VIO}=1.65V to V_{CC}(1)			100			ns
Data Output High Impedance after #OE high			t_{DF}			20	ns
Data Output High Impedance after #CE high			t_{DF}			20	ns
Output Hold Time from the earliest rising edge of address, #CE, #OE			t_{OH}	0			ns
Write Period Time			t_{WC}	90			ns
Command write period time			t_{CWC}	90			ns
Address Setup Time			t_{AS}	0			ns
Address Setup Time to #OE low during Toggle Bit Polling			t_{ASO}	15			ns
Address Hold Time			t_{AH}	45			ns
Address Hold Time from #CE or #OE High during Toggle Bit Polling			t_{AHT}	0			ns
Data Setup Time			t_{DS}	30			ns
Data Hold Time			t_{DH}	0			ns
V_{CC} Setup Time			t_{VCS}	35			µs
Chip enable Setup Time			t_{CS}	0			ns
Chip enable Hold Time			t_{CH}	0			ns
Output enable Setup Time			t_{OES}	0			ns
Output enable Hold Time	Read		t_{OEH}	0			ns
	Toggle & Data# Polling			10			ns
#WE Setup Time			t_{WS}	0			ns
#WE Hold Time			t_{WH}	0			ns
#CE Pulse Width		t_{CP}	t_{CEPW}	35			ns
#CE Pulse With High		t_{CPH}	t_{CEPWH}	30			ns
#WE Pulse Width			t_{WP}	35			ns
#WE Pulse Width High			t_{WPH}	30			ns
Program/Erase active time by RY/#BY	E_{VIO} = V_{CC} ≥ 3V		t_{BUSY}			90	ns
	E_{VIO}=1.65V to V_{CC}					100	ns
Read Recover Time before Write (#OE High to #WE Low)			t_{GHWL}	0			ns
Read Recover Time before Write (#OE High to #CE Low)			t_{GHEL}	0			ns
32-Word Write Buffer Program Operation			t_{WHWH1}		100		µs
Effective Write Buffer Program Operation	Word		t_{WHWH1}		6		µs

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Description		Symbol		Vcc=2.7V~3.6V			
		ALT	STD	Min	Typ	Max	Units
Accelerated Effective Write Buffer Operation	Per Word		tWHWH1		4.8		µs
Program Operation	Byte		tWHWH1		6	200	µs
Program Operation	Word		tWHWH1		10	200	µs
ACC 32-Word Program Operation			tWHWH1		100		µs
Sector Erase Operation			tWHWH2		0.3	2	Sec
Sector Erase Timeout			tSEA			50	µs
Release from Deep Power Down mode			tRDP	100		200	µs

Table 7-5 AC Characteristics

Note:

1. The EVIO feature was designed to support voltages from 1.65V to VCC. Device testing is conducted at EVIO=VCC.

7.5.1 Instruction Write Operation

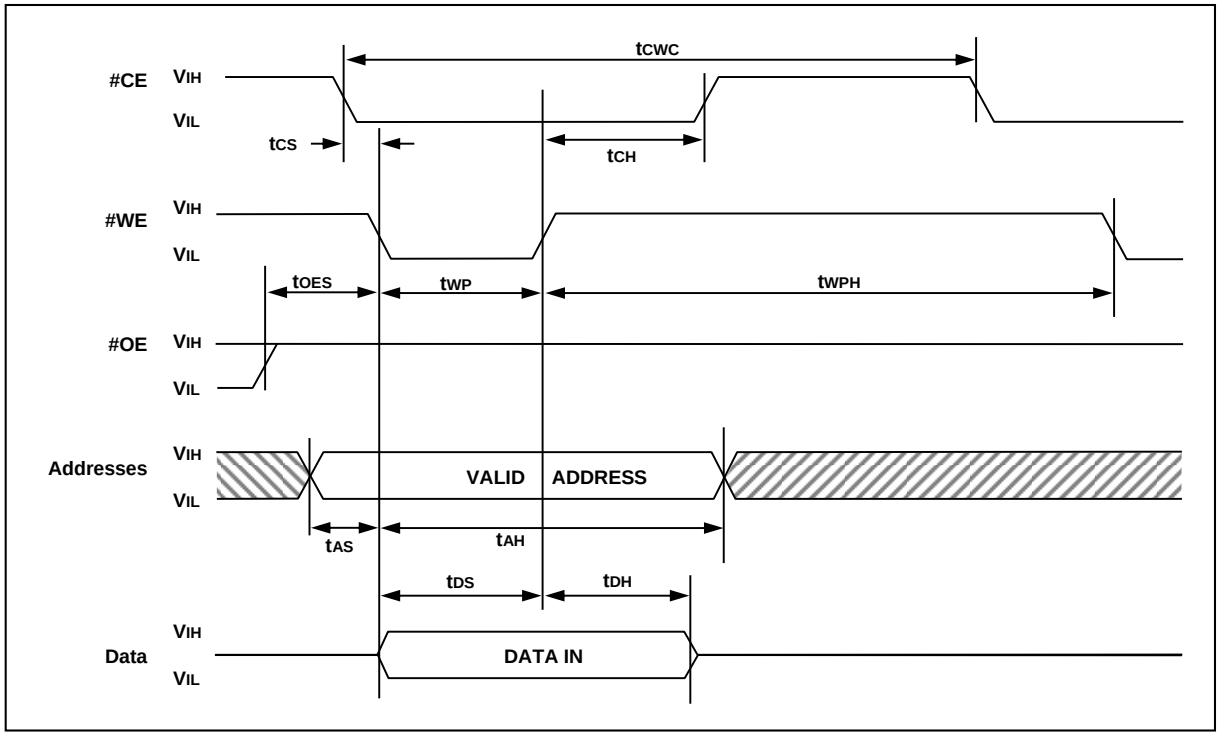


Figure 7-5 Instruction Write Operation Waveform

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7.5.2 Read / Reset Operation

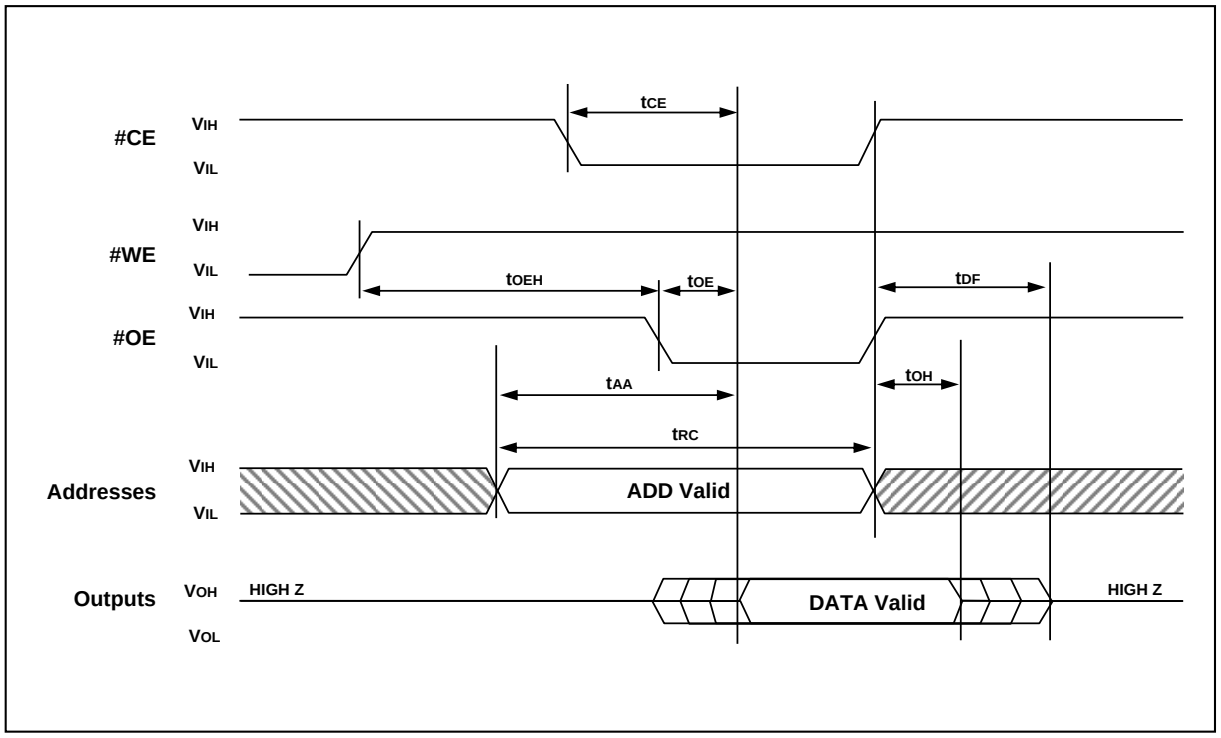


Figure 7-6 Read Timing Waveform

7.5.2.1 AC Characteristics

Description	Symbol		Setup	Speed	Unit
	ALT	STD			
#RESET Pulse Width (During Automatic Algorithm)	tRP	tRP1	MIN	10	µs
#RESET Pulse Width (NOT During Automatic Algorithm)	tRP	tRP2	MIN	500	ns
#RESET High Time Before Read		tRH	MIN	200	ns
RY/#BY Recovery Time (to #CE, #OE goes low)	tRB	tRB1	MIN	0	ns
RY/#BY Recovery Time (to #WE goes low)	tRB	tRB2	MIN	50	ns
#RESET Low (During Automatic Algorithm) to Read or Write	tREADY	tREADY1	MAX	20	µs
#RESET Low (Not During Automatic Algorithm) to Read or Write	tREADY	tREADY2	MAX	500	ns

Table 7-6 AC Characteristics #RESET and RY/#BY

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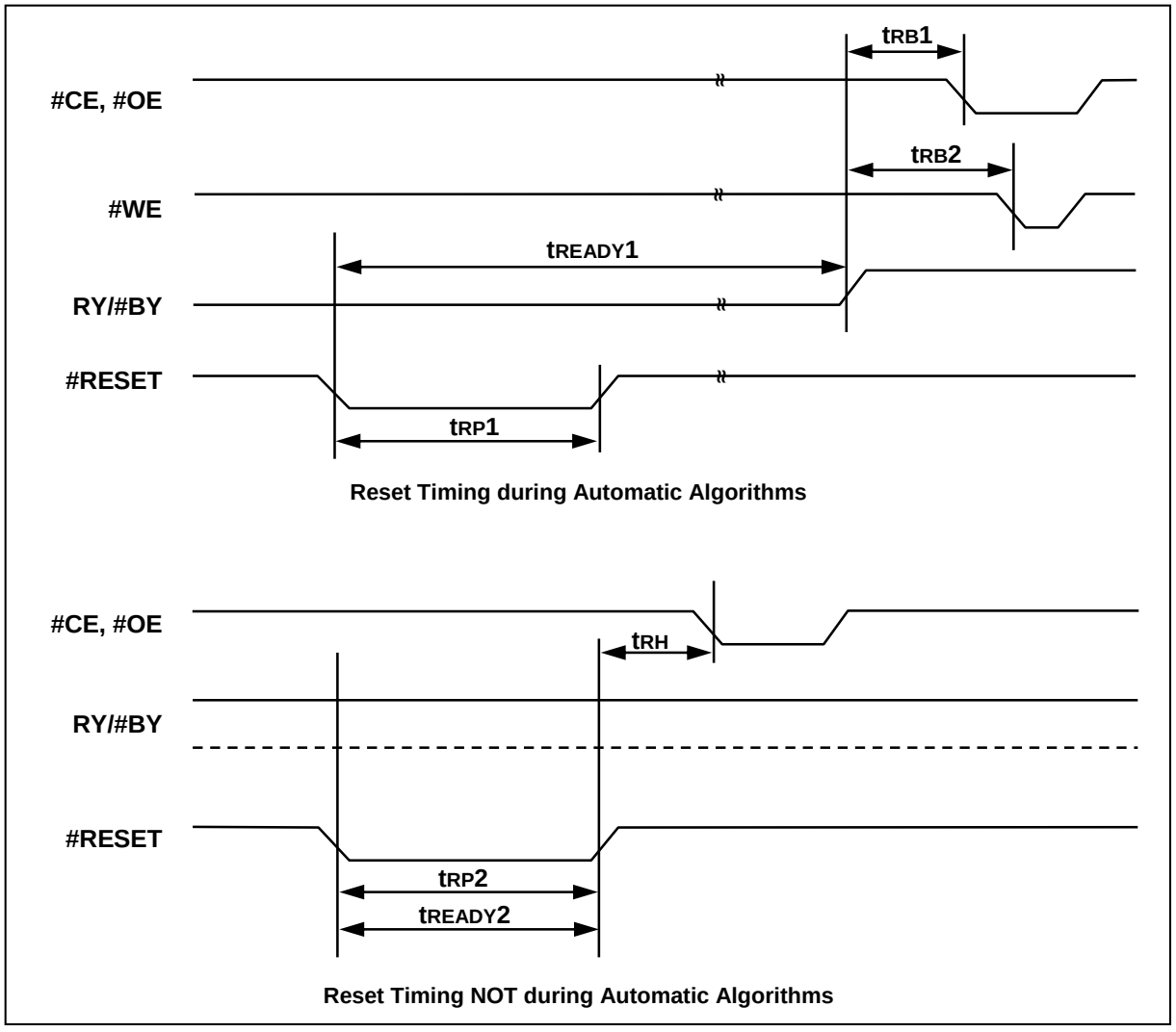


Figure 7-7 #RESET Timing Waveform

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7.5.3 Erase/Program Operation

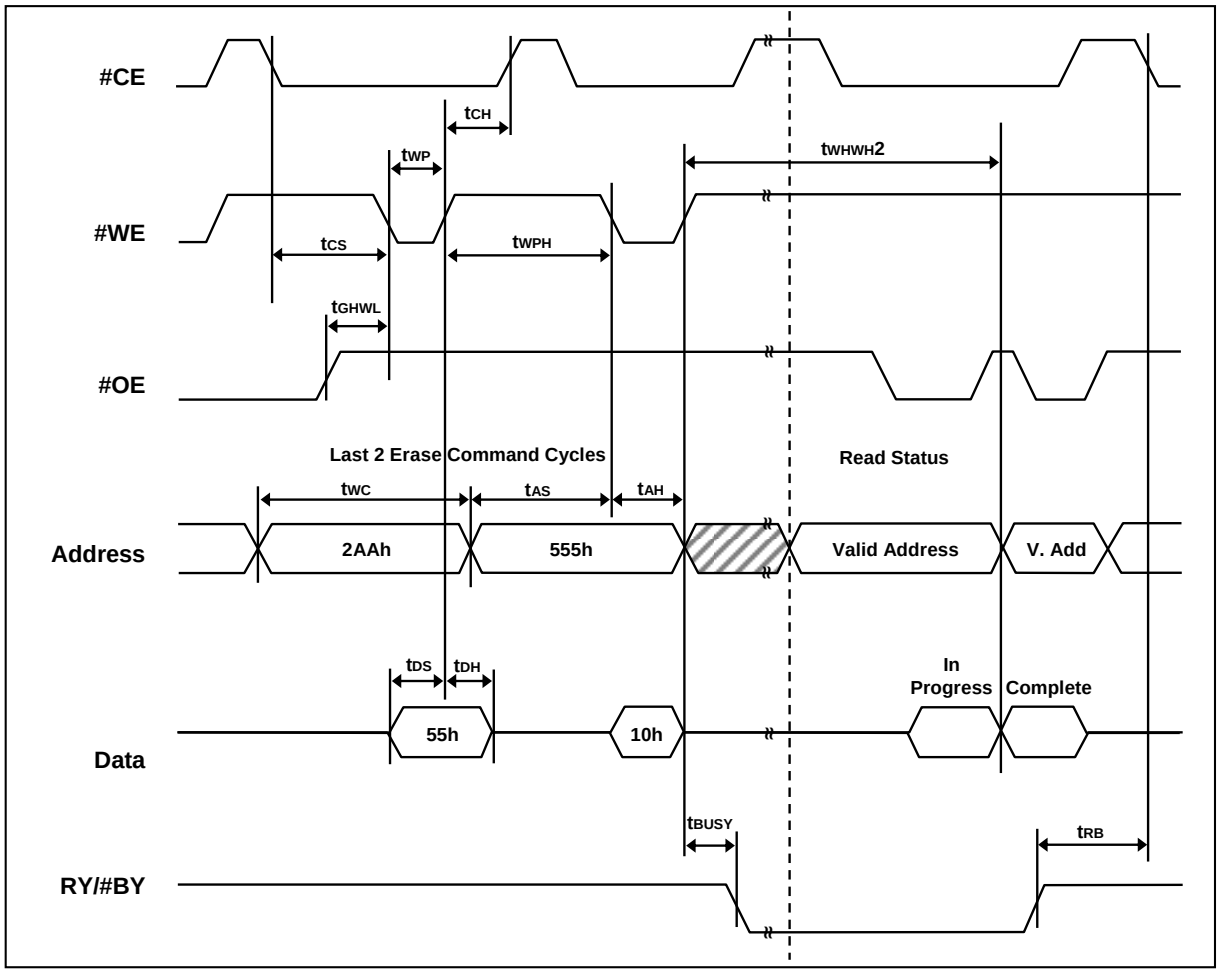


Figure 7-8 Automatic Chip Erase Timing Waveform

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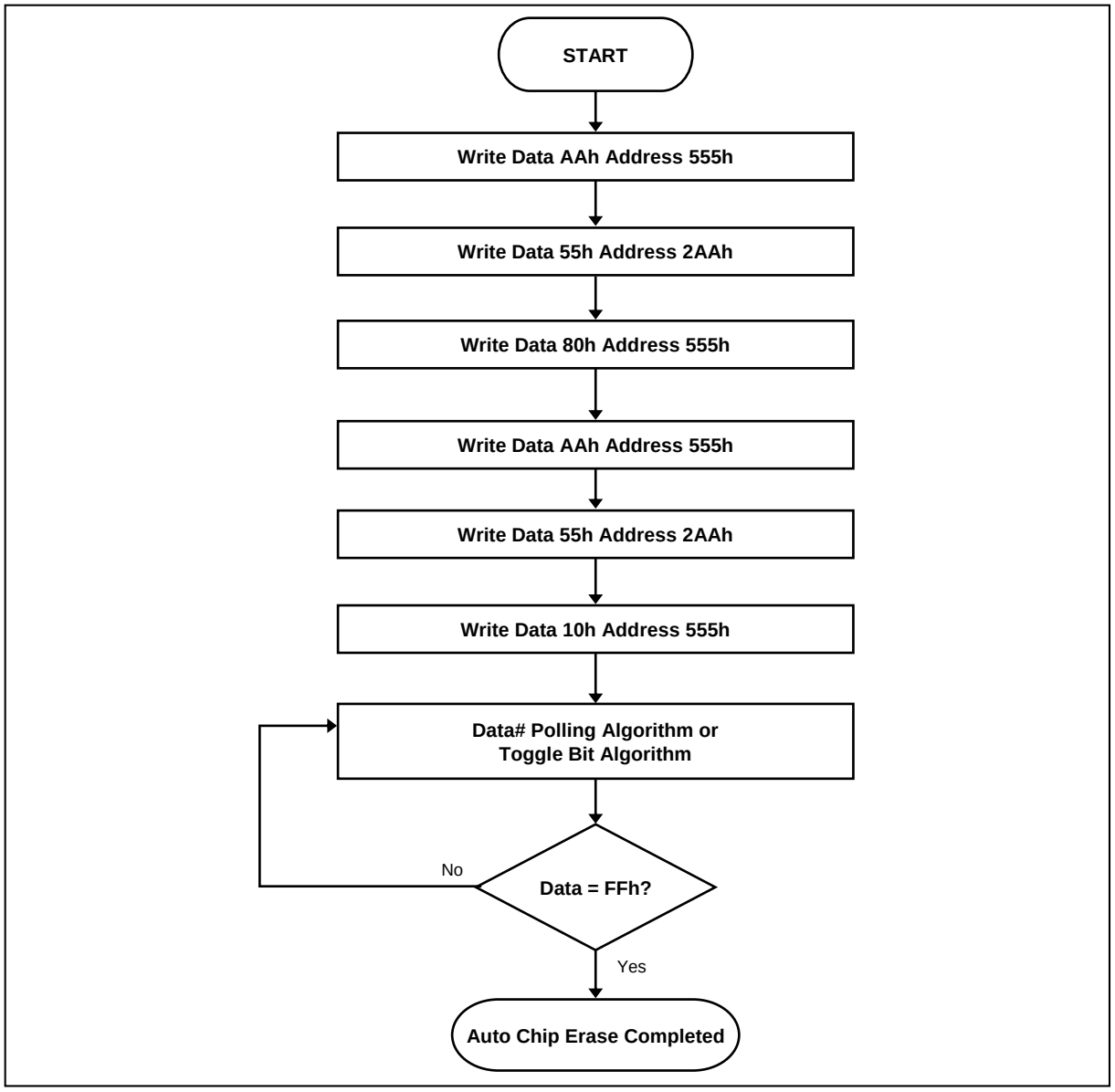


Figure 7-9 Automatic Chip Erase Algorithm Flowchart

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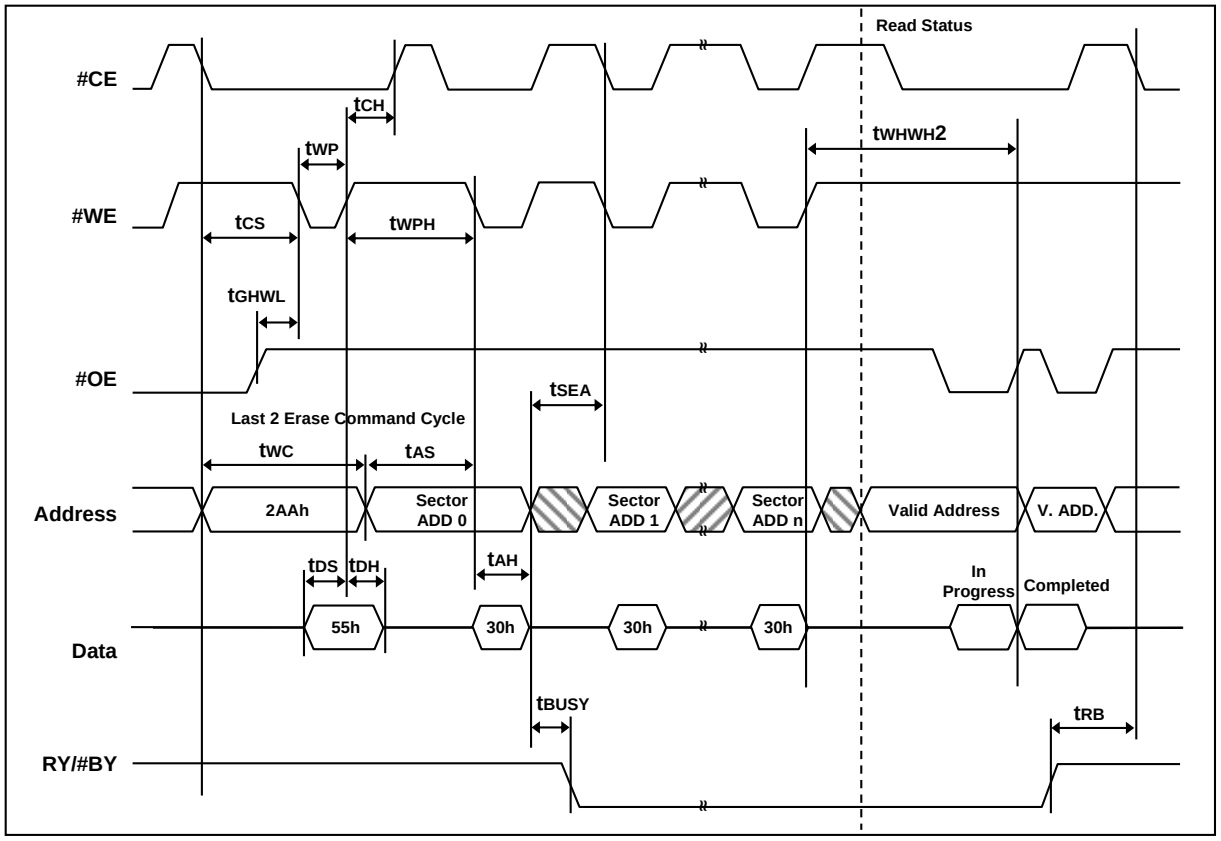


Figure 7-10 Automatic Sector Erase Timing Waveform

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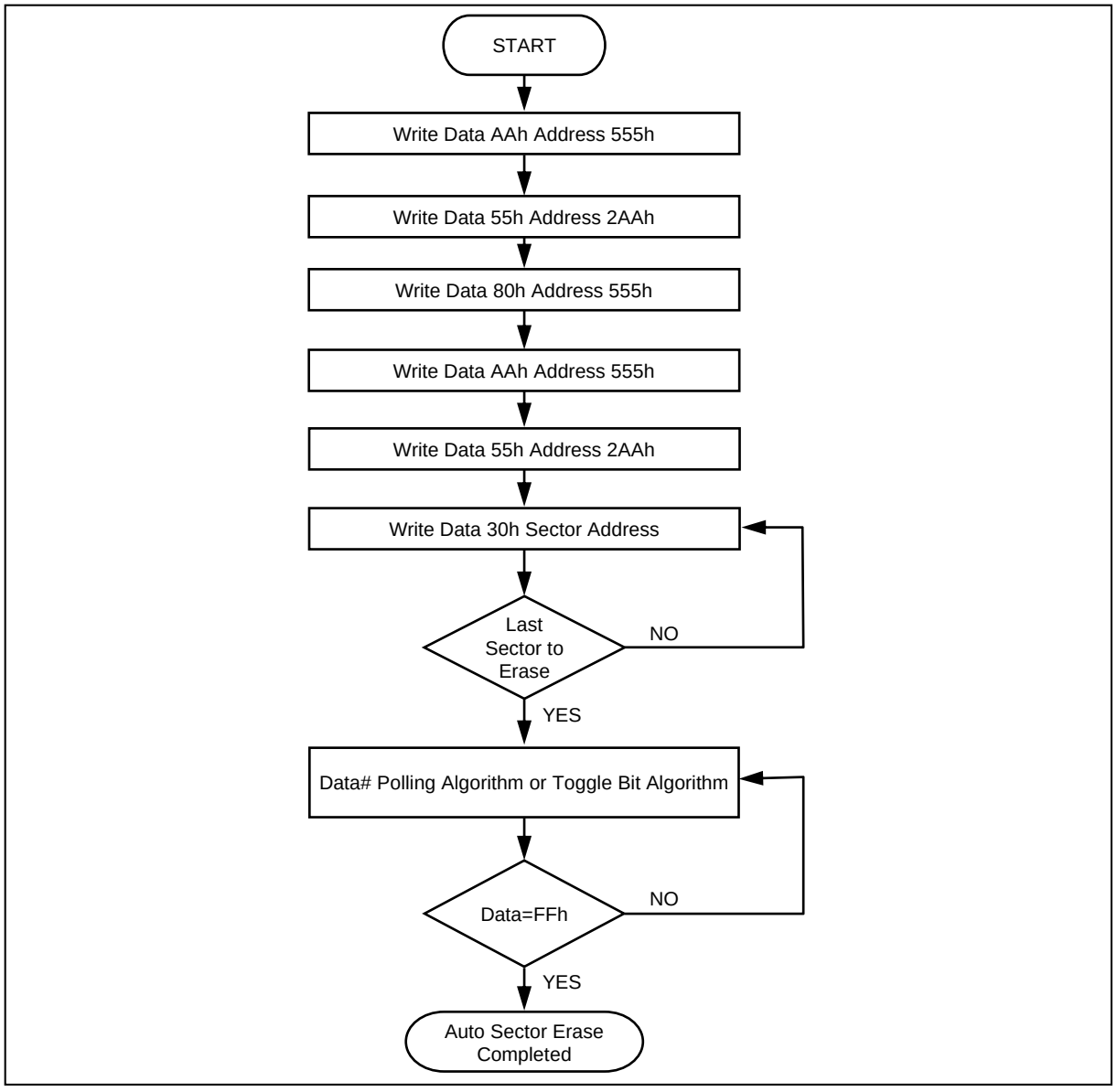


Figure 7-11 Automatic Sector Erase Algorithm Flowchart

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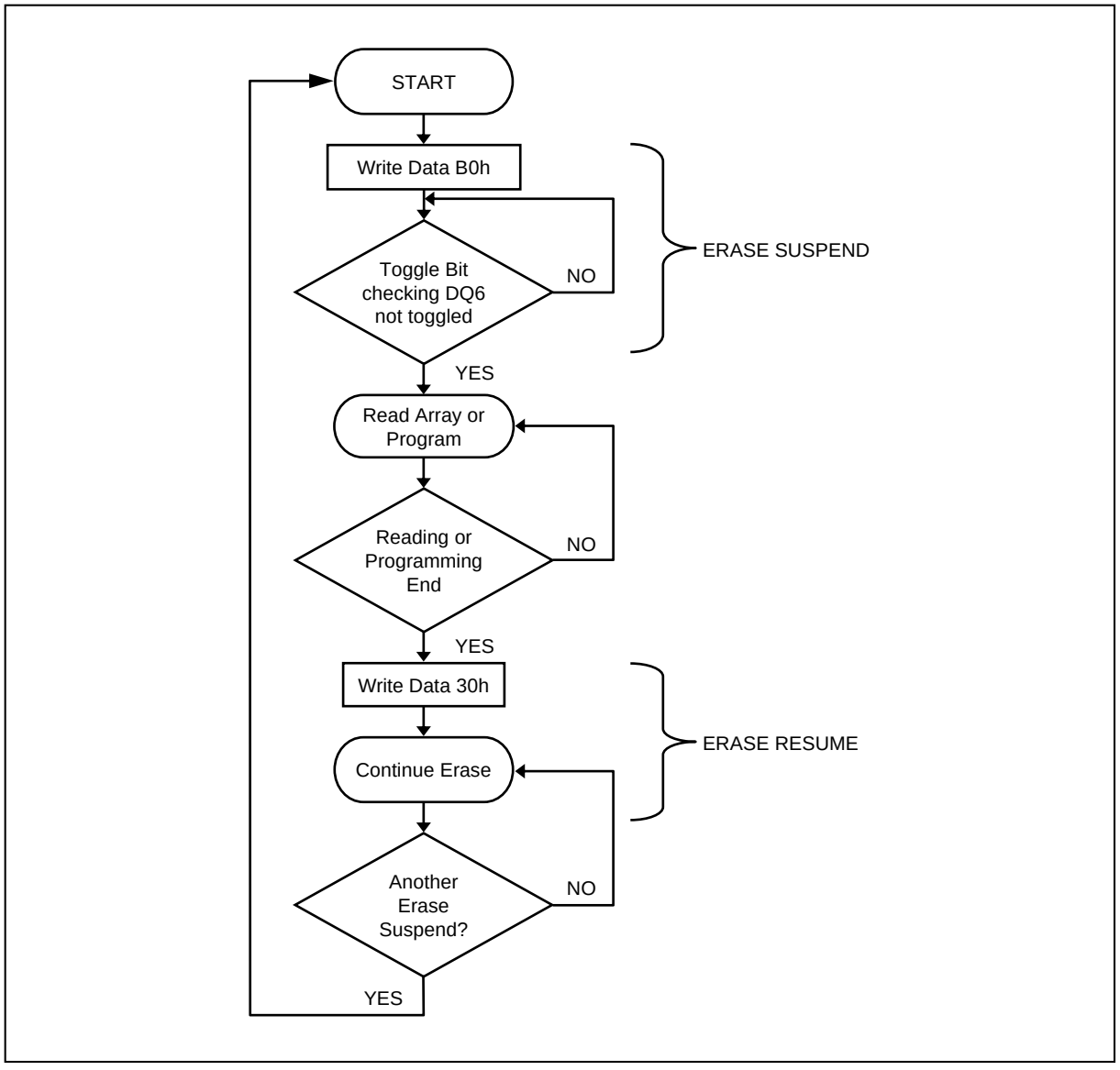


Figure 7-12 Erase Suspend/Resume Flowchart

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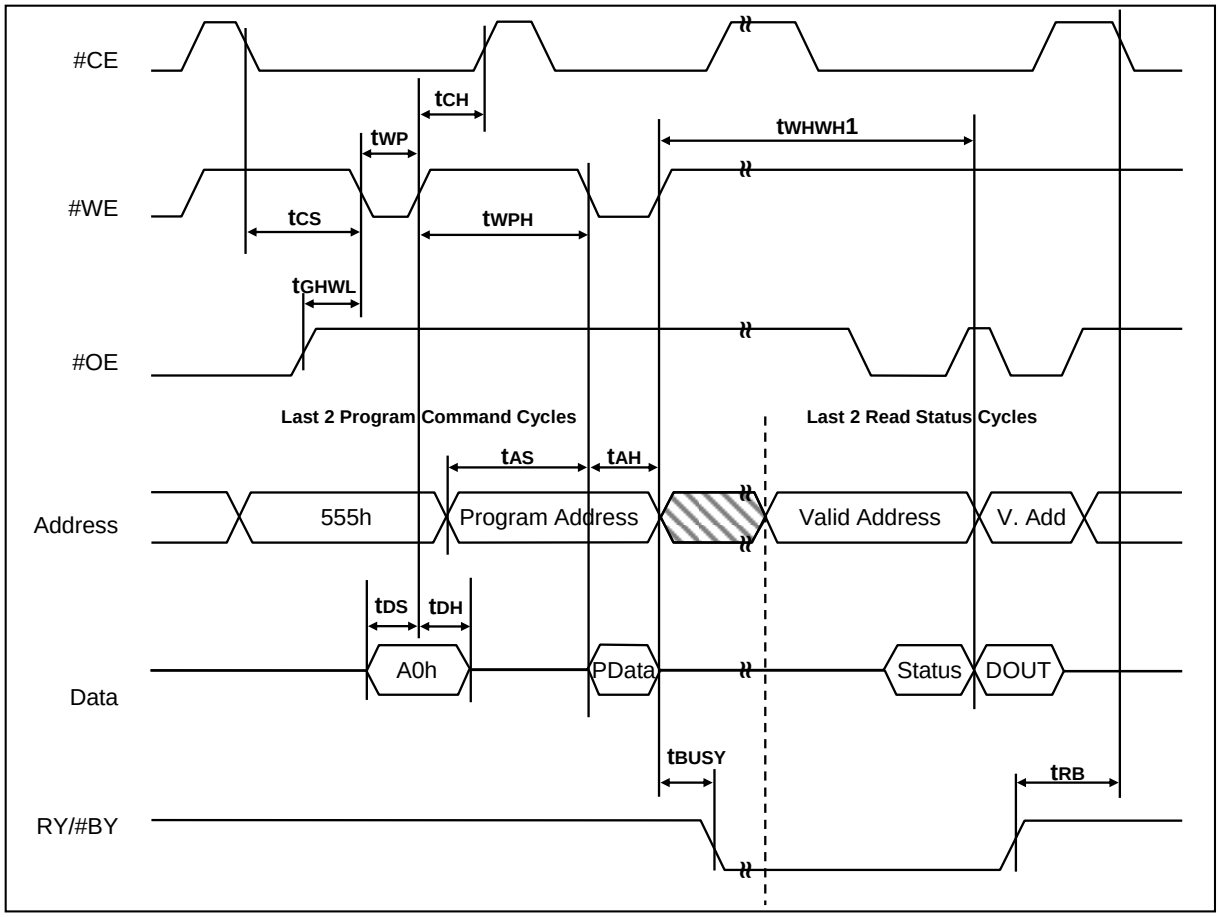


Figure 7-13 Automatic Program Timing Waveform

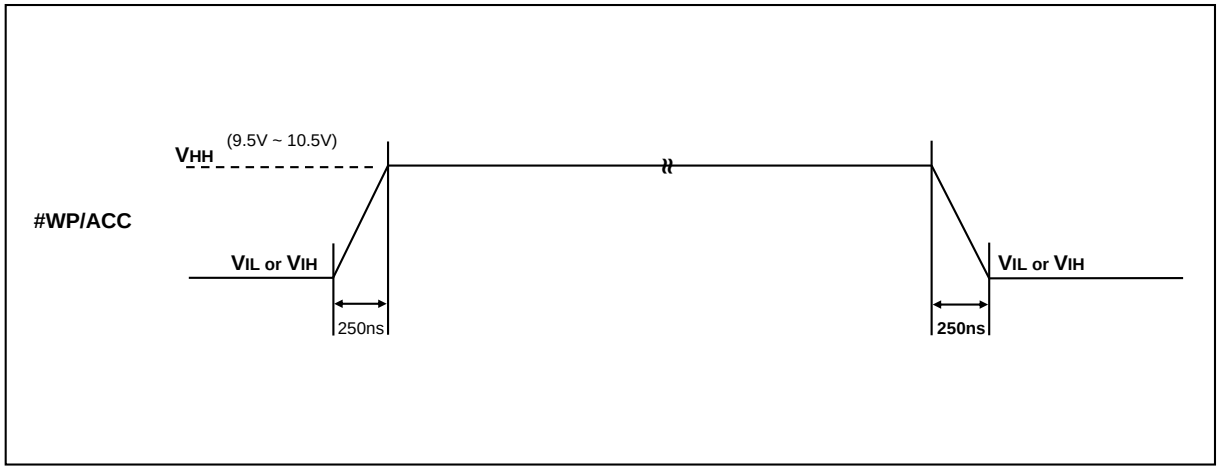


Figure 7-14 Accelerated Program Timing Waveform

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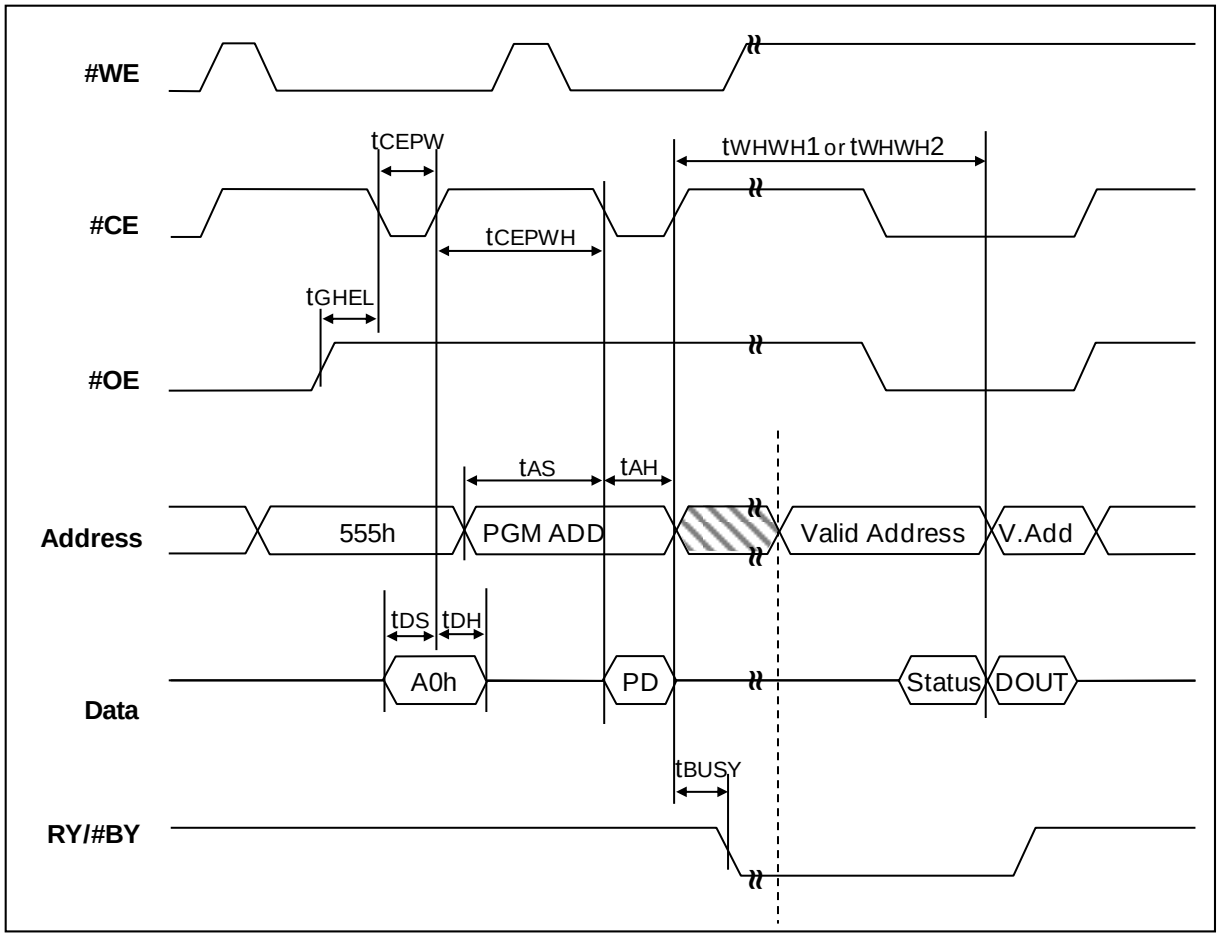


Figure 7-15 CE# Controlled Write Timing Waveform

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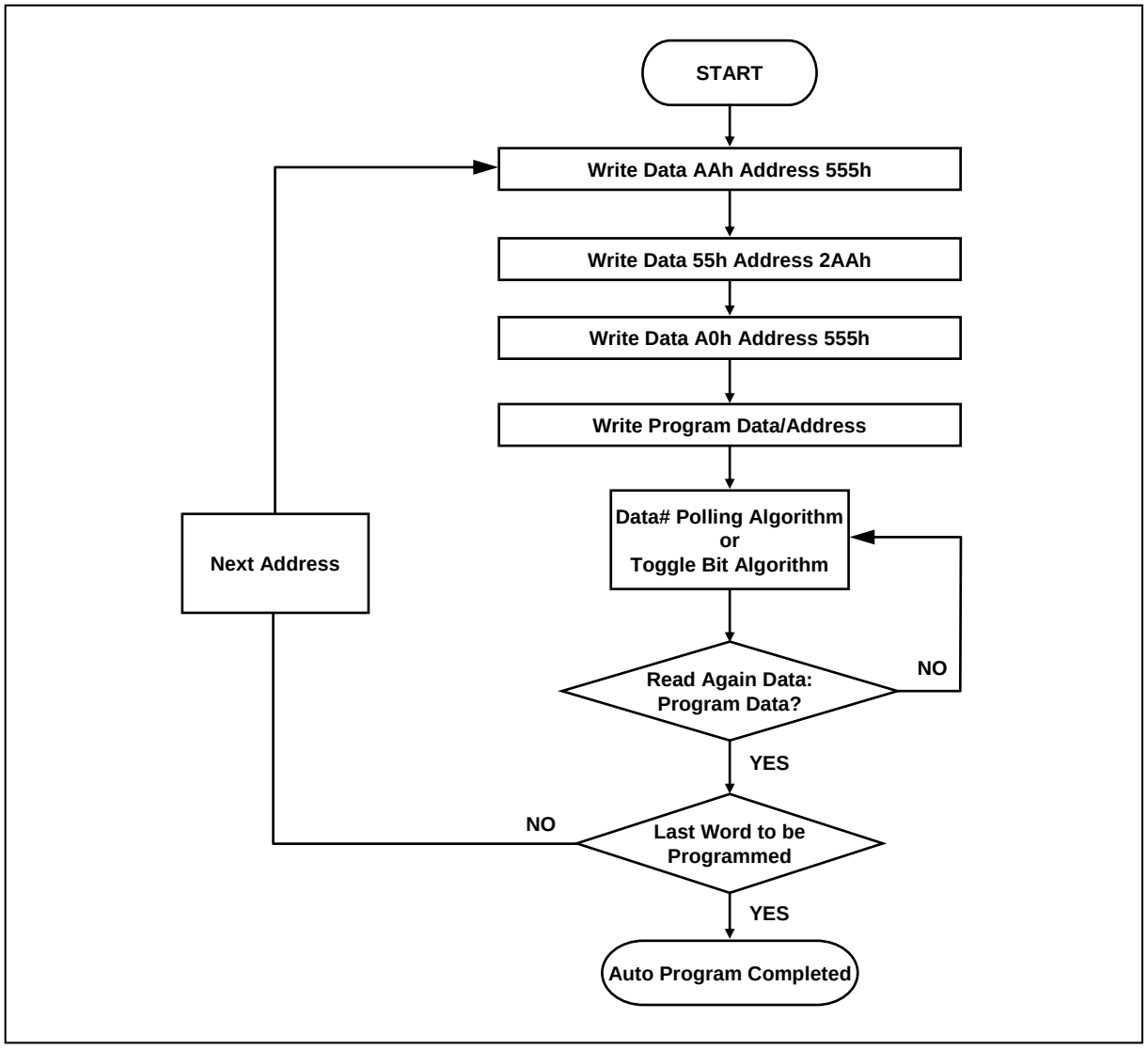


Figure 7-16 Automatic Programming Algorithm Flowchart

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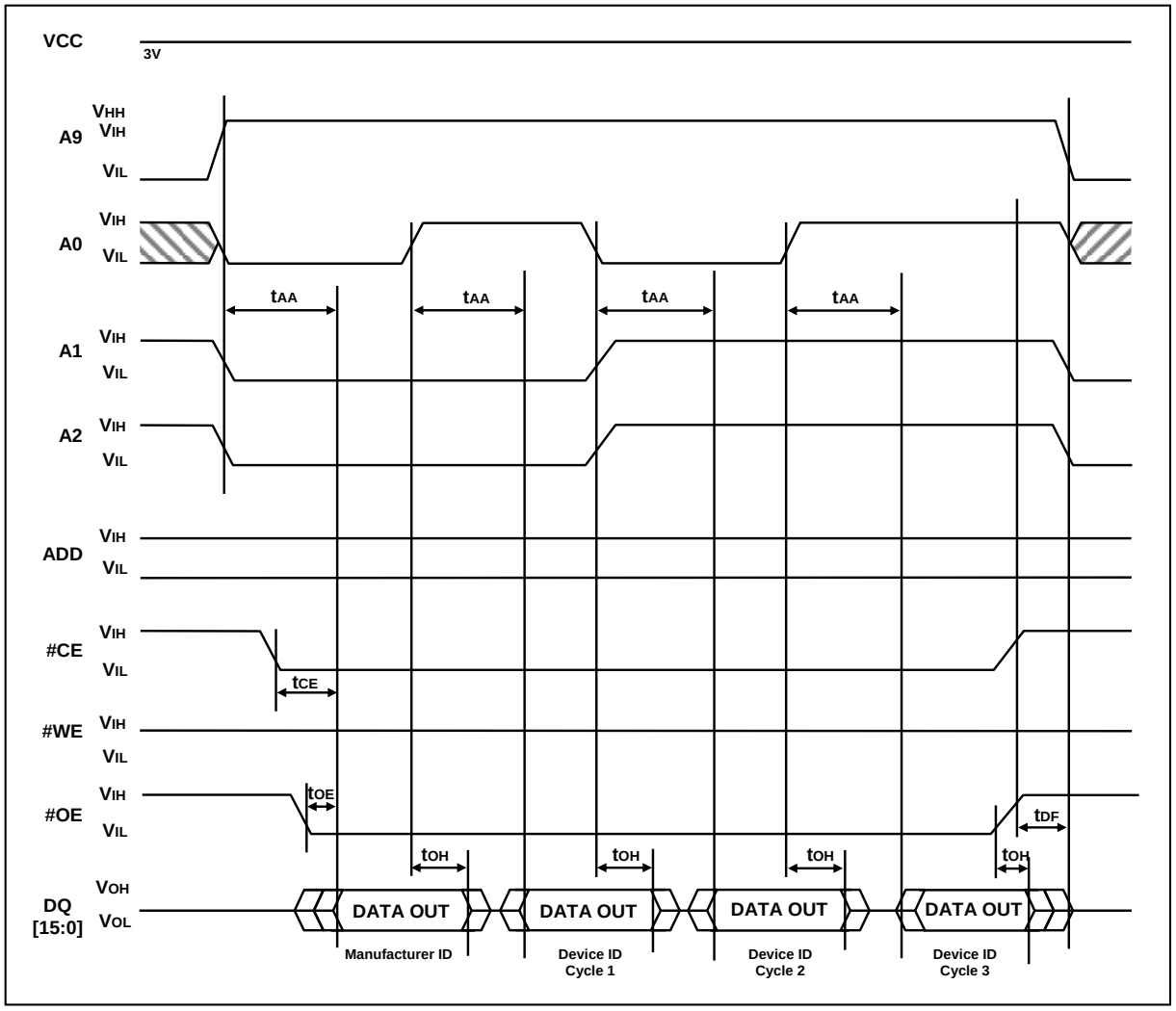


Figure 7-17 Silicon ID Read Timing Waveform

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7.5.4 Write Operation Status

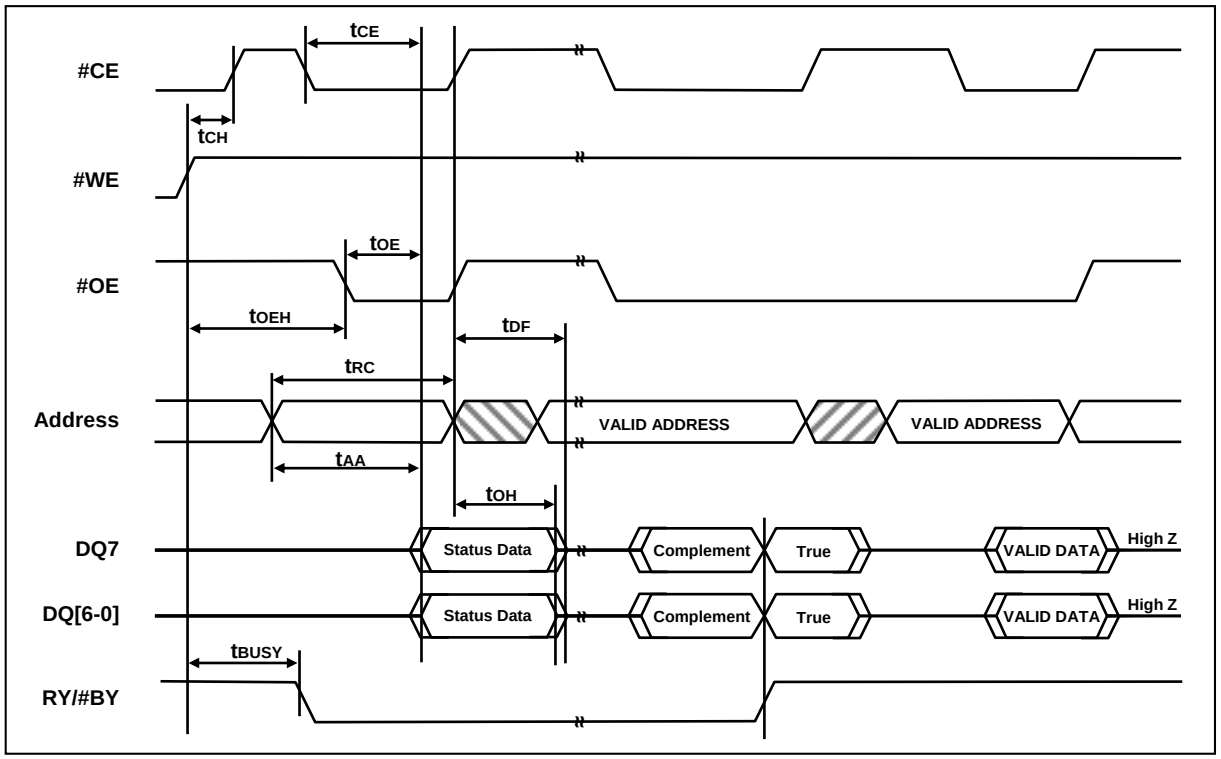


Figure 7-18 Data# Polling Timing Waveform (During Automatic Algorithms)

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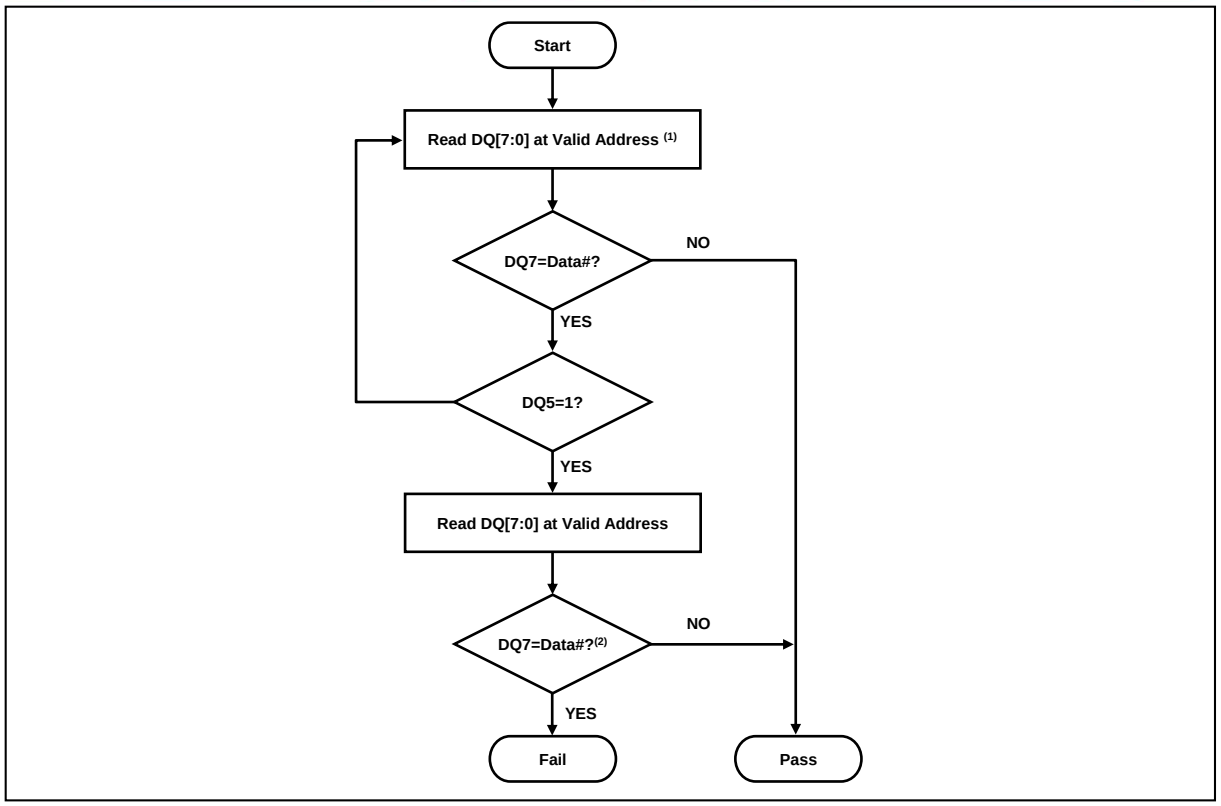


Figure 7-19 Status Polling for Word Programming/Erase

Notes:
1. For programming, valid address means program address. For erasing, valid address means erase sectors address.
2. DQ7 should be rechecked even DQ5="1" because DQ7 may change simultaneously with DQ5.

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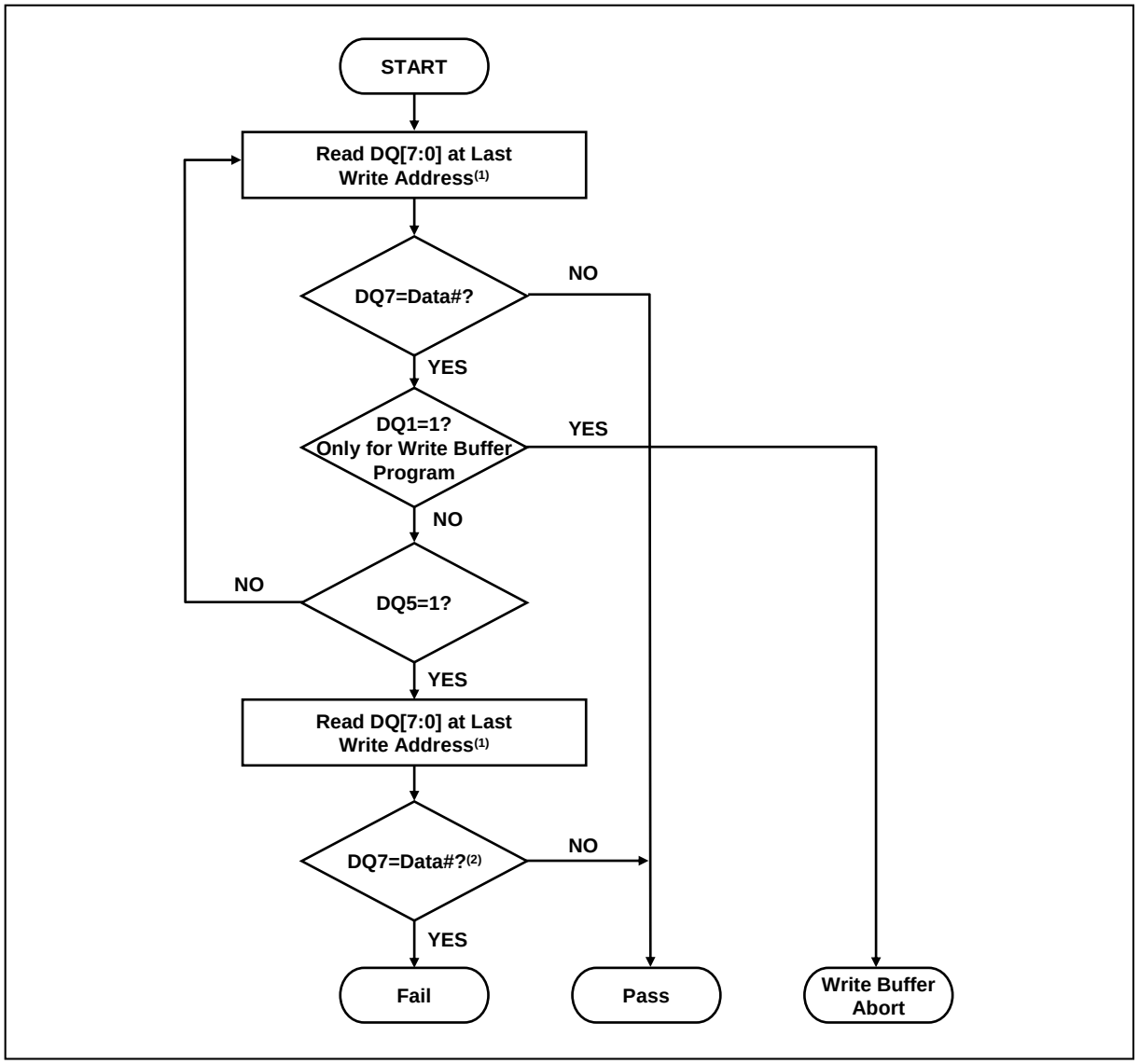


Figure 7-20 Status Polling for Write Buffer Program Flowchart

Notes:
1. For programming, valid address means program address.
2. For erasing, valid address means erase sectors address.
3. DQ7 should be rechecked even DQ5="1" because DQ7 may change simultaneously with DQ5.

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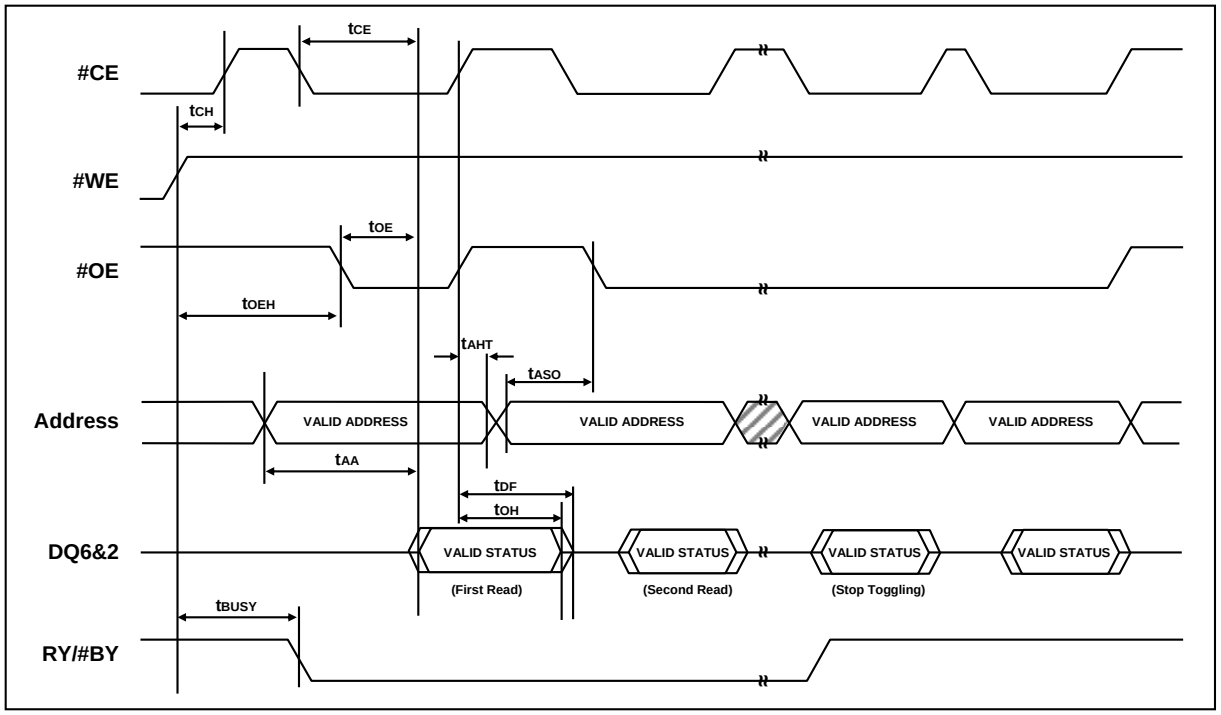


Figure 7-21 Toggling Bit Timing Waveform (During Automatic Algorithms)

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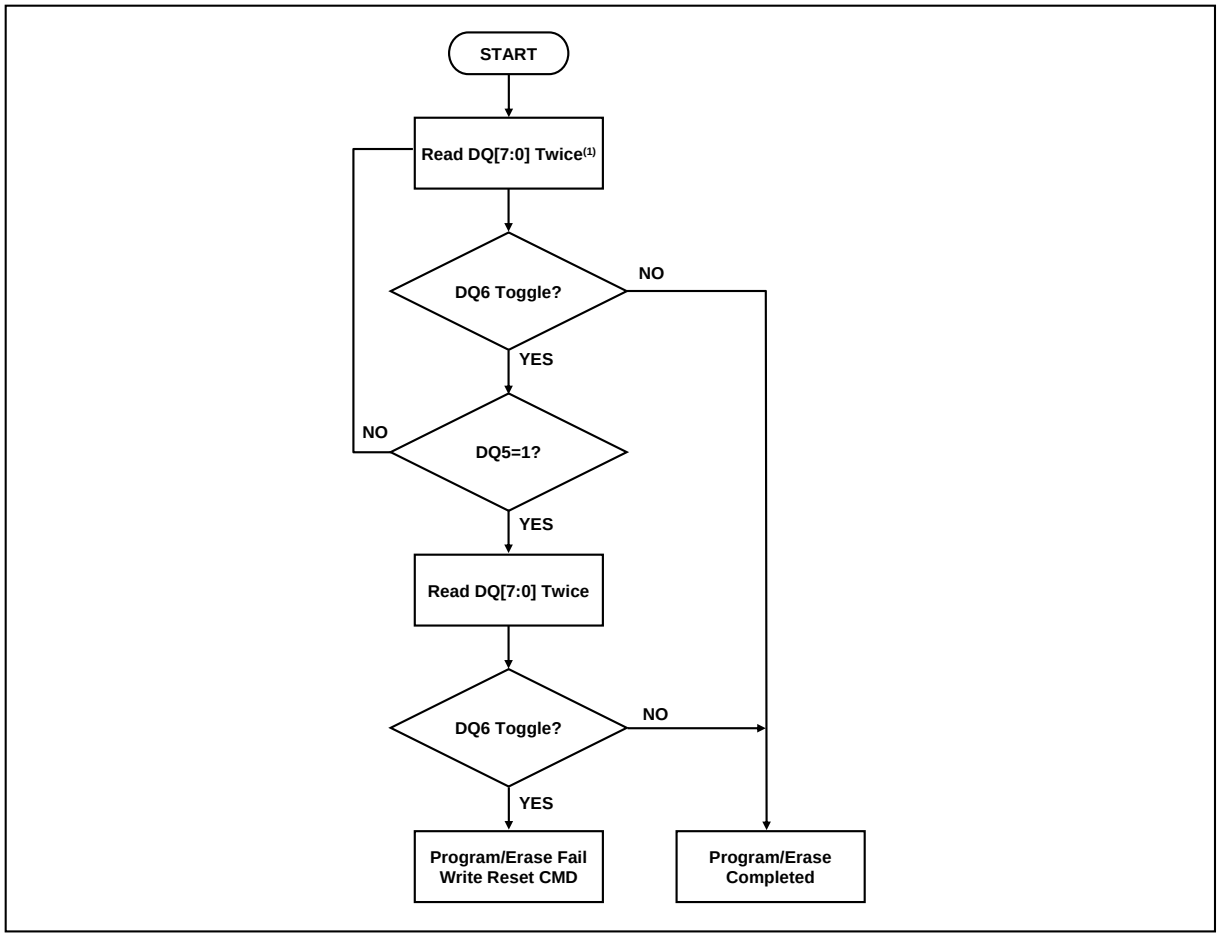


Figure 7-22 Toggle Bit Algorithm

Notes:
1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as DQ5 changes to "1".

7.5.5 WORD/BYTE CONFIGURATION (#BYTE)

Description	Symbol	Test Setup	All Speed options	Unit
#CE to #BYTE from L/H	t_{ELFL}/t_{ELFH}	MAX.	5	ns
#BYTE from L to Output Hiz	t_{FLQZ}	Max.	30	ns
#BYTE from H to Output Active	t_{FHQV}	Min.	90	ns

Table 7-7 AC Characteristics Word/Byte Configuration (#BYTE)

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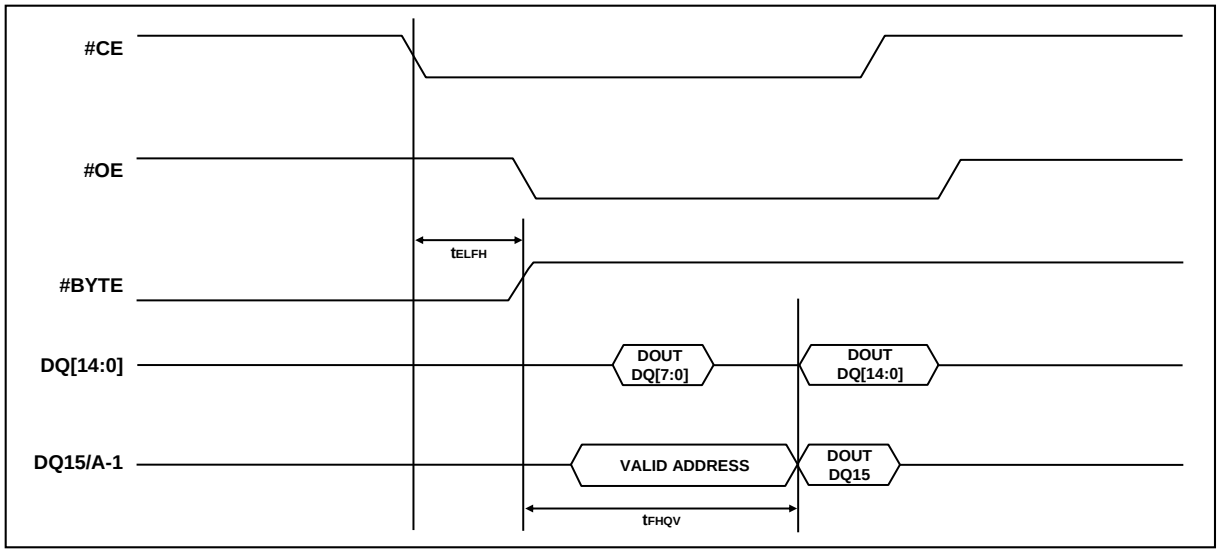


Figure 7-23 #BYTE Timing Waveform For Read operations

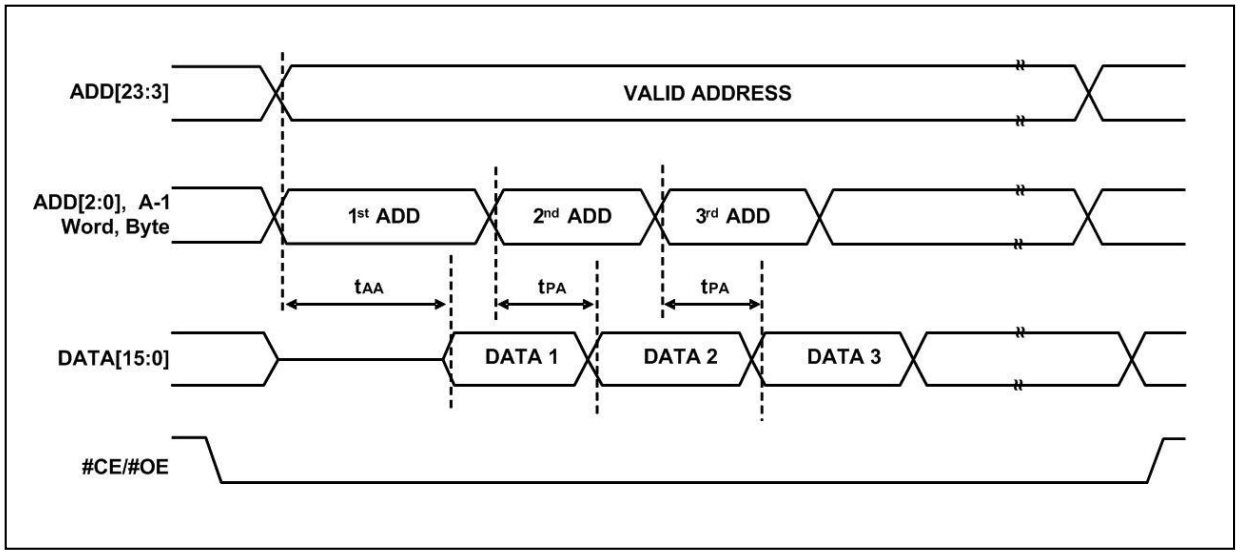


Figure 7-24 Page Read Timing Waveform

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7.5.6 DEEP POWER DOWN MODE

Description	SYMBOL	TYP.	MAX
#WE High to release from Deep Power Down Mode	tRDP	100µs	200µs
#WE High to Deep Power Down Mode	tDP	10µs	20µs

Table 7-8 AC Characteristics for Deep Power Down

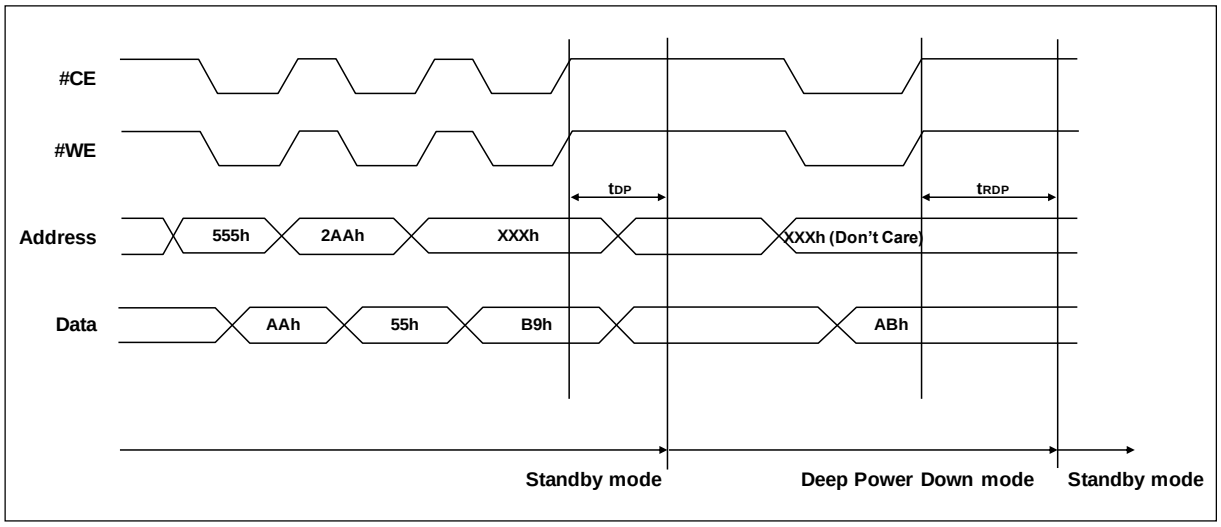


Figure 7-25 Deep Power Down mode Waveform

7.5.7 WRITE BUFFER PROGRAM

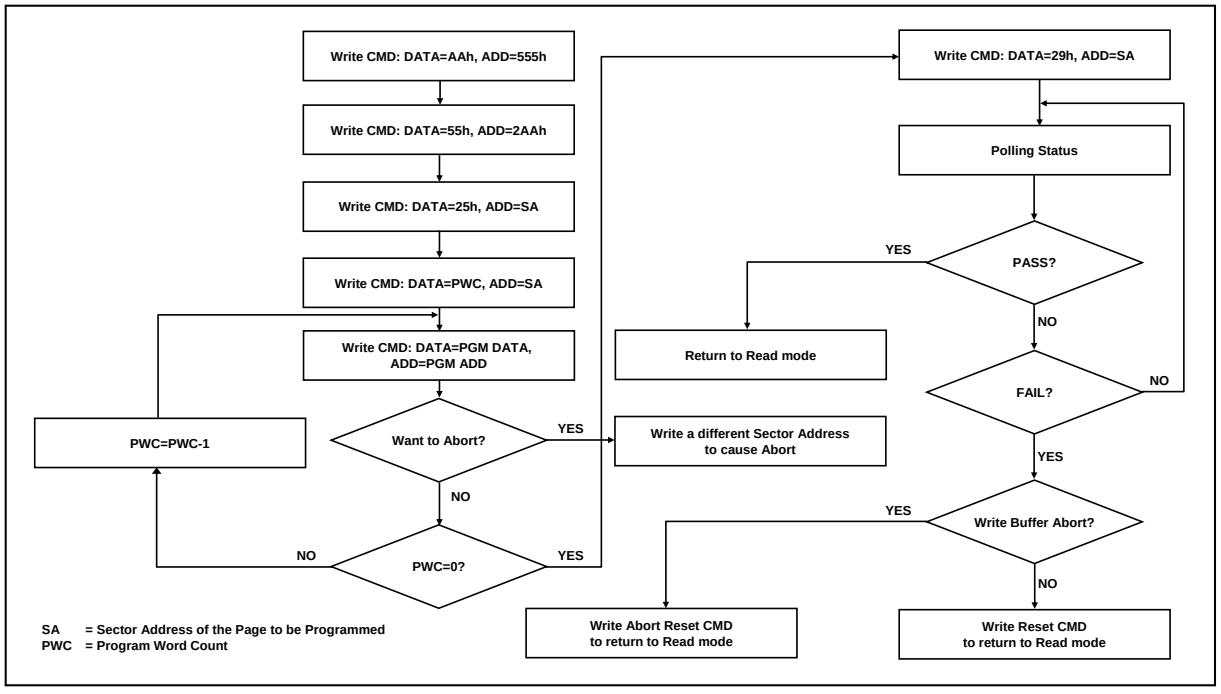


Figure 7-26 Write Buffer Program Flowchart

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7.6 Recommended Operating Conditions

7.6.1 At Device Power-up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

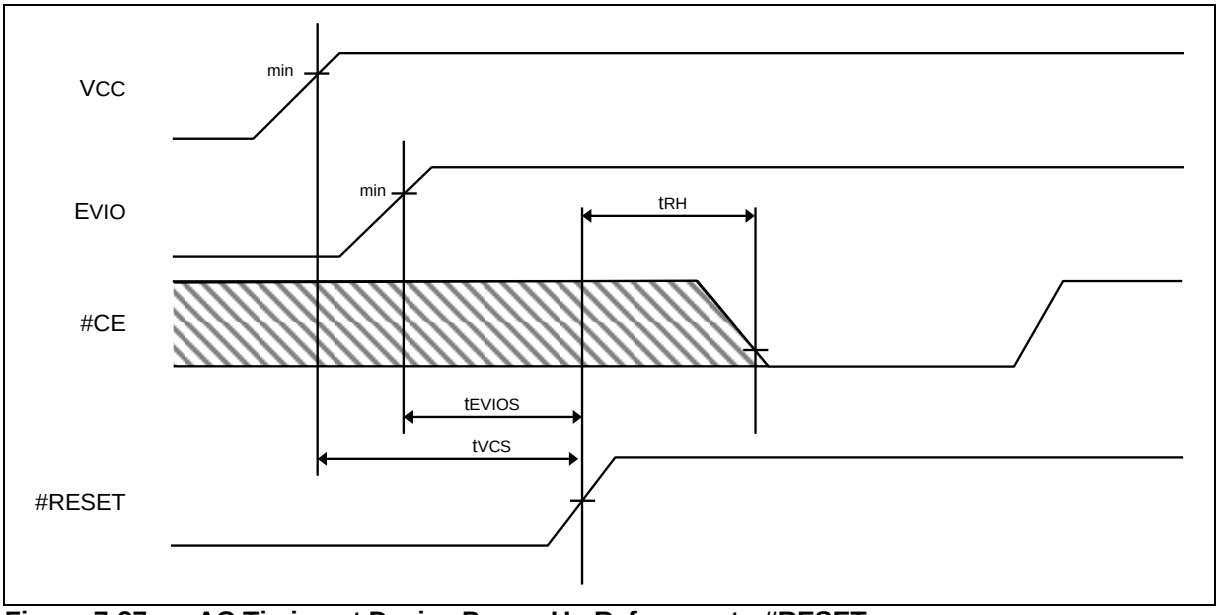


Figure 7-27 AC Timing at Device Power-Up Reference to #RESET

Description	SYMBOL		MIN	MAX	UNIT
	ALT	STD			
Reset Low Time from rising edge of VCC	t_{VCS}		35		µs
Reset Low time from rising edge of EVIO	t_{VIOS}	t_{EVIOS}	35		µs
Reset High Time before Read	t_{RH}		200		ns

Table 7-9 AC Characteristics at Device Power Up

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7.7 Erase and Programming Performance

PARAMETER	LIMITS			UNITS
	MIN	TYP(1)	MAX(2)	
Chip Erase Time		80	500	Sec
Sector Erase Time		0.3	2	Sec
Chip Programming Time		48	224	Sec
Word Programming Time		10	200	µs
Total Write Buffer Time		100		µs
ACC Total Write Buffer Time		100		µs
Erase/Program Cycles	100,000			Cycles

Table 7-10 AC Characteristics for Erase and Programming Performance

Notes:
1. Typical program and erase times assume the following conditions: 25°C, 3.0V VCC. Programming specifications assume checkerboard data pattern.
2. Maximum values are measured at VCC = 3.0 V, worst case temperature. Maximum values are valid up to and including 100,000 program/erase cycles.
3. Erase/Program cycles comply with JEDEC JESD-47E & A117A standard.
4. Exclude 00h program before erase operation.

7.8 Data Retention

PARAMETER	CONDITION	MIN	MAX	UNIT
Data Retention	55°C	20		Years

Table 7-11 Data Retention

7.9 Latch-up Characteristics

PARAMETER	MIN	MAX
Input Voltage different with GND on #WP/ACC and A9 pins	-1.0V	10.5V
Input Voltage difference with GND on all normal input pins	-1.0V	1.5xVCC
VCC Current	-100mA	+100mA
All pins included except VCC. Test condition is VCC=3.0V, one pin per test.		

Table 7-12 Latch-up Characteristics

7.10 Pin Capacitance

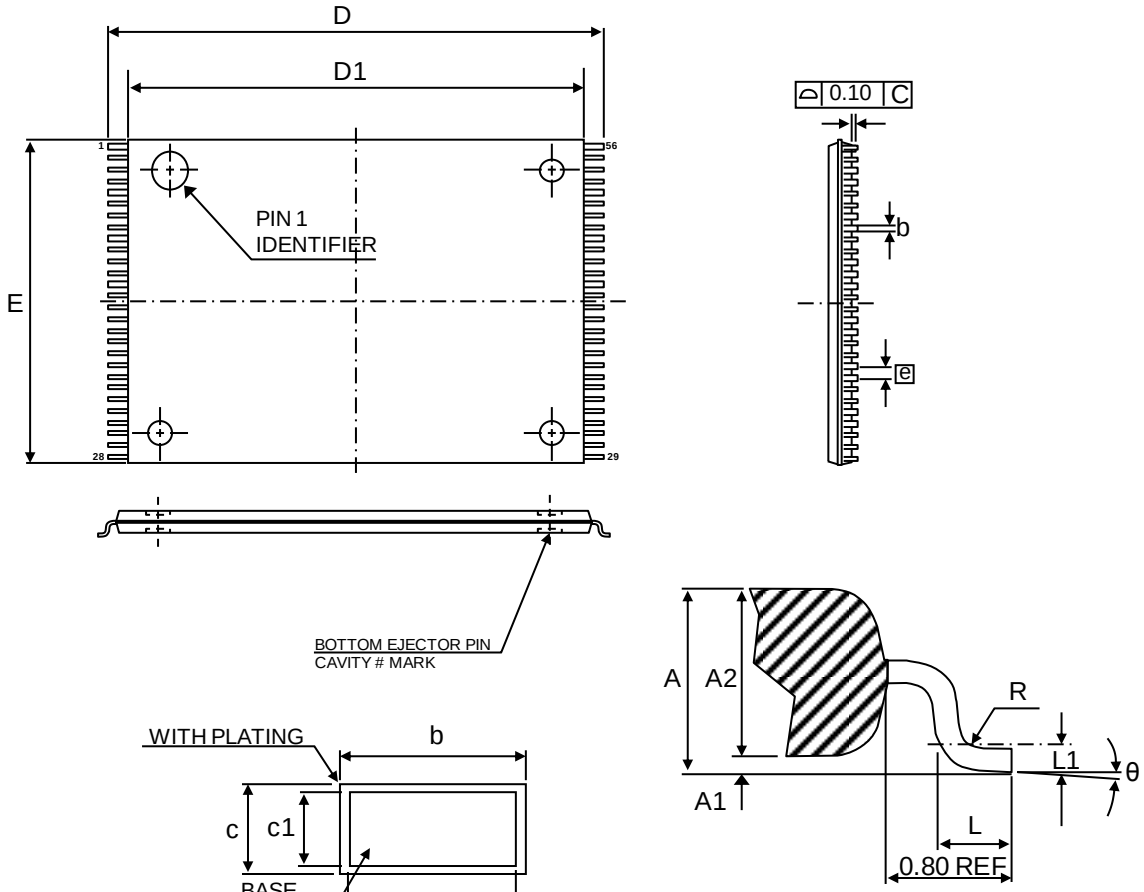
DESCRIPTION	PARAMETER	TEST SET	TYP.	MAX	UNIT
Control Pin Capacitance	CIN2	VIN=0	7.5	9	pF
Output Capacitance	COUT	VOUT=0	8.5	12	pF
Input Capacitance	CIN	VIN=0	6	7.5	pF

Table 7-13 Pin Capacitance

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8 PACKAGE DIMENSIONS

8.1 TSOP 56-pin 14x20mm

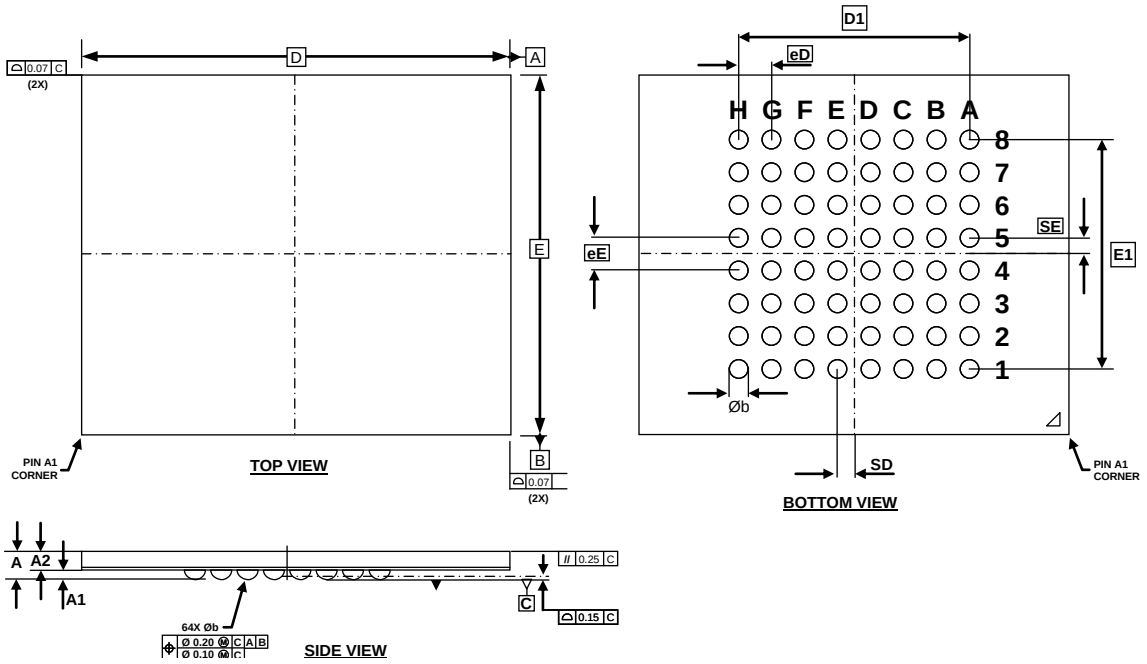


Symbol	Dimension in MM			Dimension Inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.2	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.10	-	0.21	0.004	-	0.008
c1	0.10	0.13	0.16	0.004	0.005	0.006
D	20.00 BSC			0.787 BSC		
D1	18.40 BSC			0.724 BSC		
E	14.00 BSC			0.551 BSC		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	0.25 BSC			0.010 BSC		
e	0.5 BSC			0.020 BSC		
R	0.08	-	0.35	0.003	-	0.008
θ	0°	-	8°	0°	-	8°

Figure 8-1 TSOP 56-pin 14x20mm

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8.2 Low-Profile Fine-Pitch Ball Grid Array, 64-ball 11x13mm (LFBA64)



SYMBOL	DIMENSION (MM)			NOTE
	MIN	NOM	MAX	
A	-	-	1.40	PROFILE
A1	0.40		-	BALL HEIGHT
A2	0.60		-	BODY THICKNESS
D	13.00 BSC			BODY SIZE
E	11.00 BSC			BODY SIZE
D1	7.00 BSC			MATRIX FOOTPRINT
E1	7.00 BSC			MATRIX FOOTPRINT
n	64			BALL COUNT
Øb	0.5	0.6	0.7	BALL DIAMETER
eE	1.00 BSC			BALL PITCH
eD	1.00 BSC			BALL PITCH
SD/SE	0.50 BSC			SOLDER BALL PLACEMENT
	NONE			DEPOPULATED SOLDER BALLS

Figure 8-2 LFBGA 64-ball 11x13mm

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9 ORDERING INFORMATION

9.1 Ordering Part Number Definitions

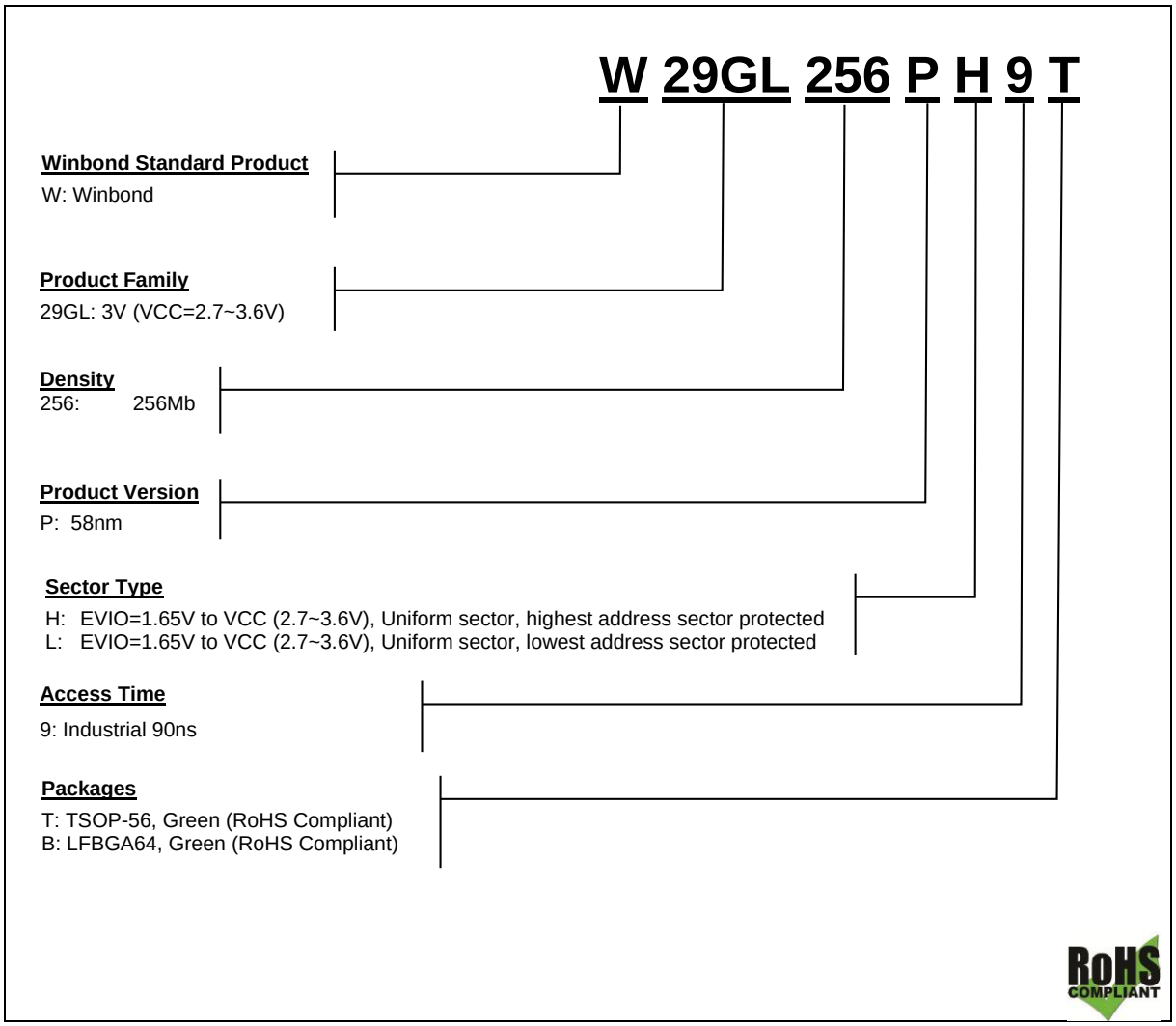


Figure 9-1 Ordering Part Numbering

Notes:
1. Winbond reserves the right to make changes to its products without prior notice.
2. Contact Winbond Sales for Secured Sector Lock Options.

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9.2 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the W29GL256P Parallel Flash Memory. Please contact Winbond for specific availability by density and package type. Winbond Parallel memories use a 12-digit Product Number for ordering.

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
TSOP-56	256Mb	W29GL256PH9T	W29GL256PH9T
TSOP-56	256Mb	W29GL256PL9T	W29GL256PL9T
LFBGA64	256Mb	W29GL256PH9B	W29GL256PH9B
LFBGA64	256Mb	W29GL256PL9B	W29GL256PL9B

Table 9-1 Valid Part Numbers and Markings

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10 HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	07-02-2014	-	First Release

Table 10-1 Revision History

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