# 3.0V 32, 64, 128, 256, 512M-BIT, 1G-BIT, 2G-BIT SERIAL FLASH MEMORY WITH DUAL/QUAD SPI, QPI & DTR

*Industrial Plus Grade*

**Preliminary Designation**

The data for W25Q25RV is currently in a preliminary state.

The “Preliminary” designation on a *Winbond* datasheet indicates that the product is not fully characterized. The specifications are subject to change and are not guaranteed. *Winbond* or an authorized sales representative should be consulted for current information before using this product.

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# 1 FEATURE DESCRIPTIONS

- **New Family of SpiFlash Memories**
  - –The W25QxxRV includes the following products:
    W25Q33RV:32M-bit
    W25Q64RV:64M-bit
    W25Q12RV:128M-bit
    W25Q25RV:256M-bit
    W25Q51RV:512M-bit
    W25Q01RV:1G-bit
    W25Q02RV: 2G-bit
  - – Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - – Dual SPI: CLK, /CS, $IO_0$, $IO_1$, /WP, /Hold
  - – Quad SPI: CLK, /CS, $IO_0$, $IO_1$, $IO_2$, $IO_3$
  - – SPI/QPI DTR (Double Transfer Rate) Read(1)
  - – 3 or 4-Byte Addressing Mode
  - – Factory Mode
  - – Software & Hardware Reset(2)-
- **Highest Performance Serial Flash**
  - – 133MHz Standard/Dual/Quad SPI clocks
  - – 266/532MHz equivalent Dual/Quad SPI
  - – 66MB/S continuous data transfer rate
  - – Min. 100K Program-Erase cycles
  - – More than 20-year data retention
- **Low Power, Wide Temperature Range**
  - – Single 2.7V to 3.6V supply
  - – <0.1µA Power-down (typ.)
  - – -40°C to 105°C operating range
- **Flexible Architecture with 4KB sectors**
  - – Uniform Sector/Block Erase (4K/32K/64K-Byte)
  - – Program 1 to 256 byte per programmable page
  - – Erase/Program Suspend & Resume
- **Advanced Security Features**
  - – Software and Hardware Write-Protect
  - – Power Supply Lock-Down
  - – Special OTP protection
  - – Top/Bottom, Complement array protection
  - – Flex Block/Sector array protection
  - – 64-Bit Unique ID for each device
  - – Discoverable Parameters (SFDP) Register
  - – 3X256-Bytes Security Registers with OTP locks
  - – Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging**
  - – 8-pin SOP 150-mil / 208-mil
  - – 8-pad XSON 4x4x0.45mm
  - – 8-pad USON 4x3mm
  - – 8-pad WSON 6x5-mm
  - – 8-pad WSON/VSON 8x6-mm
  - – 16-pin SOP 300-mil (additional /RESET pin)
  - – 24-ball TFBGA 8x6-mm(5x5 ball array)
  - – Contact Winbond for KGD and other options
- **Preliminary AC/DC Characteristics**
  - – W25Q25RV

**Note:**
1. The SPI DTR and QPI DTR instructions are only supported with Part Number Suffix “M”
2. Hardware /RESET pin is only available on TFBGA or SOP16 packages
3. Please contact Winbond for other packages.



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# 2 PACKAGE TYPES AND PIN CONFIGURATIONS

## 2.1 Pin Configuration SOP 150/208-mil

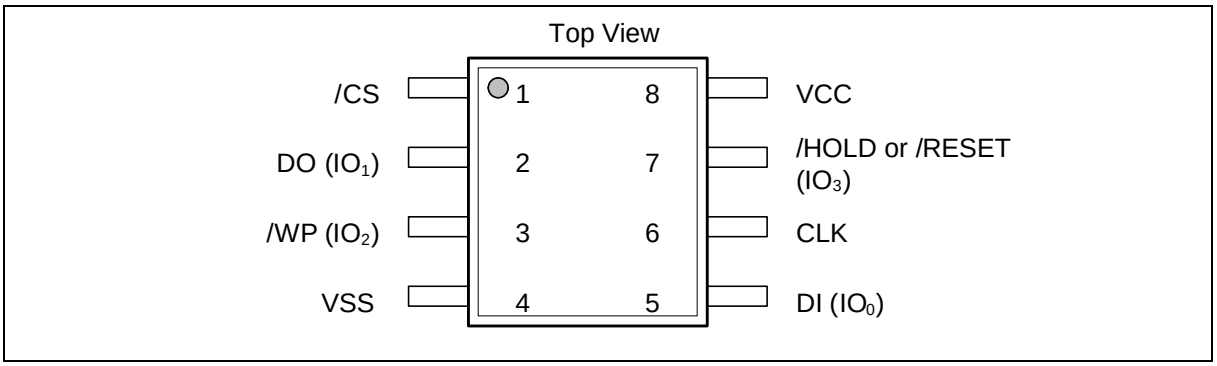



Figure 2.1. Pin Assignments, 8-pin SOP 150,208-mil (Package Code SN/CN, SS/CS)

## 2.2 Pad Configuration XSON 4x4-mm, USON 4X3mm, WSON 6x5-mm, 8x6-mm,VSON 8x6mm

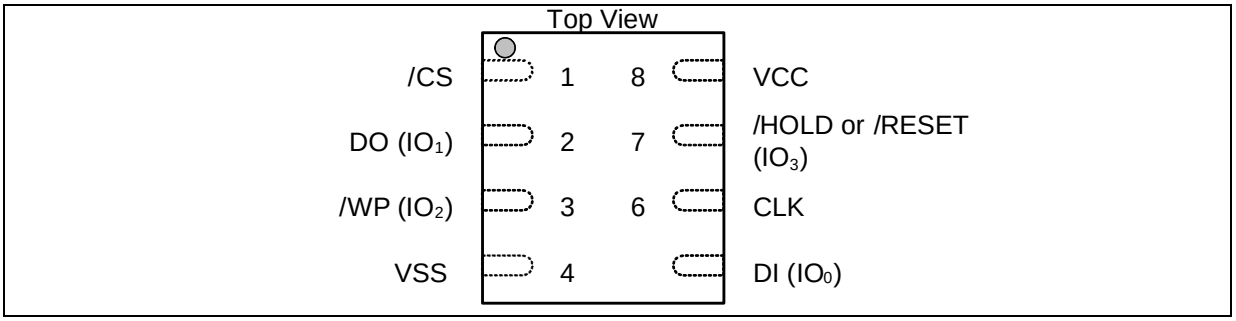



Figure 2.2. Pad Assignments, XSON 4x4-mm, USON 4X3mm, WSON 6x5(Package Code XG,UU,ZP/CP, ZH) Pad Assignments, WSON 8x6-mm (Package ZE/CE)

## 2.3 Pad Description for Package Code: SN, CN, SS, CS, XG, UU, ZP, CP, ZE, CE

| PAD NO. | PAD NAME | I/O | FUNCTION |
|---|---|---|---|
| 1 | /CS | I | Chip Select Input |
| 2 | DO (IO1) | I/O | Data Output (Data Input Output 1)(1) |
| 3 | /WP (IO2) | I/O | Write Protect Input ( Data Input Output 2)(2) |
| 4 | GND | | Ground |
| 5 | DI (IO0) | I/O | Data Input (Data Input Output 0)(1) |
| 6 | CLK | I | Serial Clock Input |
| 7 | /HOLD or /RESET (IO3) | I/O | Hold or Reset Input (Data Input Output 3)(2) |
| 8 | VCC | | Power Supply |

**Note:**

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /HOLD (or /RESET) functions are only available for Standard/Dual SPI..



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## 2.4 Pin Configuration SOP 300-mil

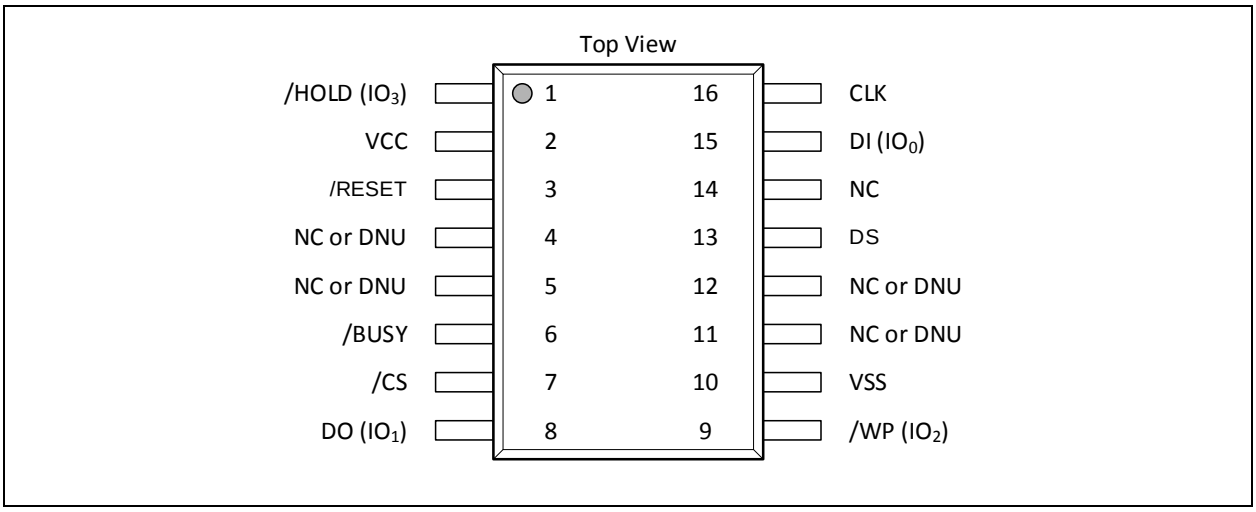



Figure 2.4. Pin Assignments, 16-pin SOP 300-mil (Package Code SF/CF)

## 2.5 Pin Description for Package Code SF, CF

| PIN NO. | PIN NAME | I/O | FUNCTION | |
|---|---|---|---|---|
| 1 | /HOLD or (IO3) | I/O | Hold (Data Input Output 3)(2) | |
| 2 | VCC | | Power Supply | |
| 3 | /RESET | I | Reset Input(3) | |
| 4 | N/C, DNU | | No Connect(4) | Don't Use(5) |
| 5 | N/C, DNU | | No Connect(4) | Don't Use(5) |
| 6 | /BUSY | O | Reset Output | |
| 7 | /CS | I | Chip Select Input | |
| 8 | DO (IO1) | I/O | Data Output (Data Input Output 1)(1) | |
| 9 | /WP (IO2) | I/O | Write Protect Input (Data Input Output 2)(2) | |
| 10 | VSS | | Ground | |
| 11 | DNU | | Don't Use | |
| 12 | N/C, DNU | | No Connect(4) | Don't Use(5) |
| 13 | DS | O | Data Strobe | |
| 14 | N/C | | No Connect | |
| 15 | DI (IO0) | I/O | Data Input (Data Input Output 0)(1) | |
| 16 | CLK | I | Serial Clock Input | |

**Note:**

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /HOLD (or /RESET) functions are only available for Standard/Dual SPI.
3. The /RESET pin on SOP-16 package is a dedicated hardware reset pin regardless of device settings. If the reset function is not used, this pin can be left floating in the system.
4. For W25Q12RV, W25Q25RV.
5. For W25Q51RV, W25Q01RV and W25Q02RV



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## 2.6 Ball Configuration TFBGA 8x6-mm (5x5 Ball Array)

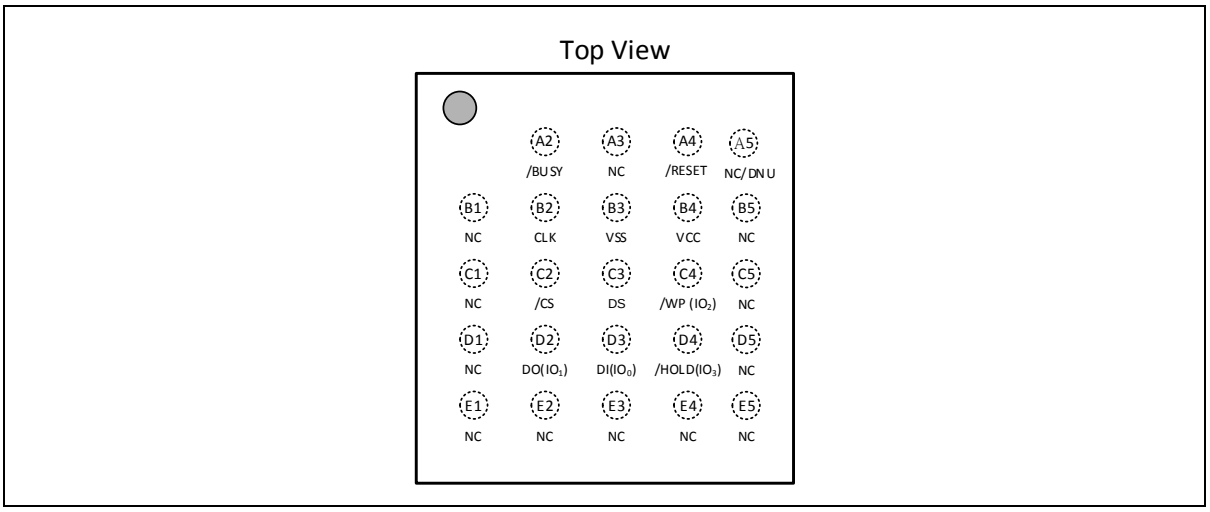



Figure 2.6. W25Q51RV/01RV/02RV Ball Assignments, 24-ball TFBGA 8x6-mm (Package Code TB/CB)

## 2.7 Ball Description for Package Code TB, CB

| BALL NO. | PIN NAME | I/O | FUNCTION |
|---|---|---|---|
| A2 | /BUSY | O | Reset Output |
| A4 | /RESET | I | Reset Input(3) |
| A5 | DNU | | Don't Use |
| B2 | CLK | I | Serial Clock Input |
| B3 | VSS | | Ground |
| B4 | VCC | | Power Supply |
| C2 | /CS | I | Chip Select Input |
| C3 | DS | O | Data Strobe Output |
| C4 | /WP (IO2) | I/O | Write Protect Input (Data Input Output 2)(2) |
| D2 | DO (IO1) | I/O | Data Output (Data Input Output 1)(1) |
| D3 | DI (IO0) | I/O | Data Input (Data Input Output 0)(1) |
| D4 | /HOLD (IO3)<br>/RESET | I/O | Hold or Reset Input (Data Input Output 3)(2) |
| Multiple | NC | | No Connect |

**Note:**
1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions (factory default for Quad Enabled part numbers with ordering option "IQ").
3. The /RESET pin is a dedicated hardware reset pin regardless of device settings or operation states. If the hardware reset function is not used, this pin can be left floating or connected to VCC in the system.



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# 3 PIN DESCRIPTIONS

## 3.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low, the device will be selected, power consumption will increase to active levels, and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see “Write Protection” and Figure 58). If needed, a pull-up resistor on the /CS pin can be used to accomplish this.

## 3.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25QxxRV supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /HOLD pin becomes IO3.

## 3.3 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (CMP, TB, BP3, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /WP pin function is not available since this pin is used for IO2. See Figure 2.x for the pin configuration of Quad I/O operation.

## 3.4 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /HOLD pin function is not available since this pin is used for IO3. See Figure 2.x for the pin configuration of Quad I/O operation.

## 3.5 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")



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## 3.6 Reset (/RESET)

The /RESET pin allows the device to be reset by the controller. For 8-pin packages, when QE=0, the IO3 pin can be configured either as a /HOLD pin or as a /RESET pin depending on Status Register setting. When QE=1, the /HOLD or /RESET function is not available for 8-pin configuration.

A dedicated hardware /RESET pin is available on SOP-16 and TFBGA packages. When it's driven low for a minimum period of ~1µS, this device will terminate any external or internal operations and return to its power-on state.

## 3.7 BUSY (/BUSY)

The /BUSY pin is provided to the system hardware designers to determine if the flash device is busy performing device initialization or internal reset. The /BUSY pin will be pulled low through the Open-Drain connection during the device power-on-reset (POR) period, as well as the device reset period (tRST) triggered by either software reset command or the hardware /RESET pin. While the /BUSY pin is pulled low internally, no command will be accepted by the device.

## 3.8 Data Strobe (DS)

The Data Strobe (DS) pin is required to support DDR clock speeds higher than 84MHz. It is an output signal that aids in validating and synchronizing data output for the host at higher clock speeds. The DS pin is used during read operations, and it is not used during program, erase, or write operations.

When the DS pin is enabled, the device drives the DS output pin low from a high impedance state after /CS pin is asserted and the first input clock is shifted in. As the read instruction sequence continues, the IO pins transition from input to data output sequence At the same time, the DS pin toggles simultaneously to synchronize every data output transition on either the falling edge of the clock during extended SPI or both edges of the clock during DDR. Once /CS pin is driven high after a read sequence, the DS pin goes back to the high impedance state.

The DS pin is not driven and is in the high impedance when it is enable/disabled by the DSEN bit in Status Register-3.

This functionality is applicable across SPI, QPI, and DDR modes and provides robust support for high-speed data read operations.



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# 4 BLOCK DIAGRAM

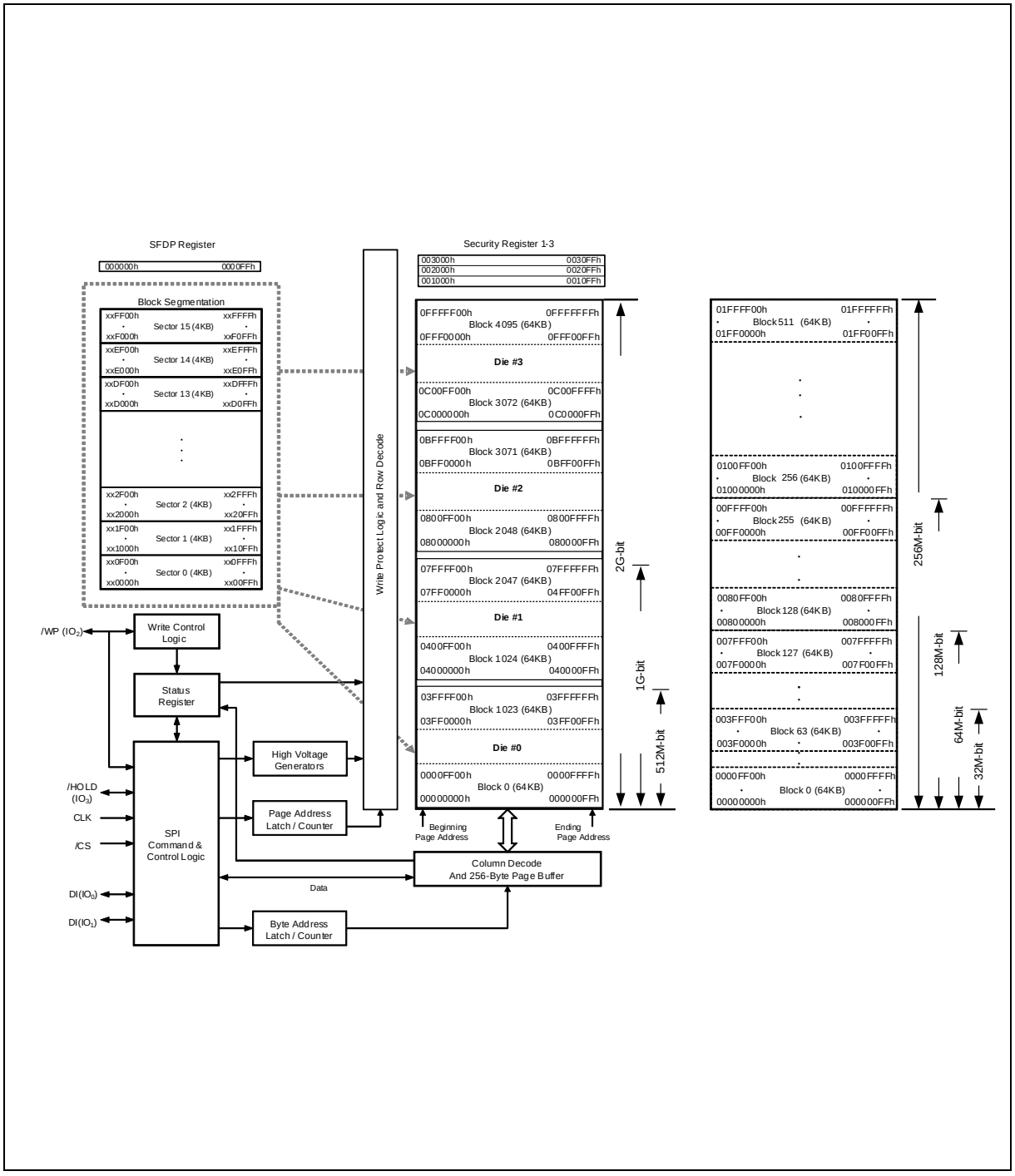



Figure 4 W25QxxRV Serial Flash Memory Block Diagram



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# 5 FUNCTIONAL DESCRIPTIONS

## 5.1 SPI / QPI Operations

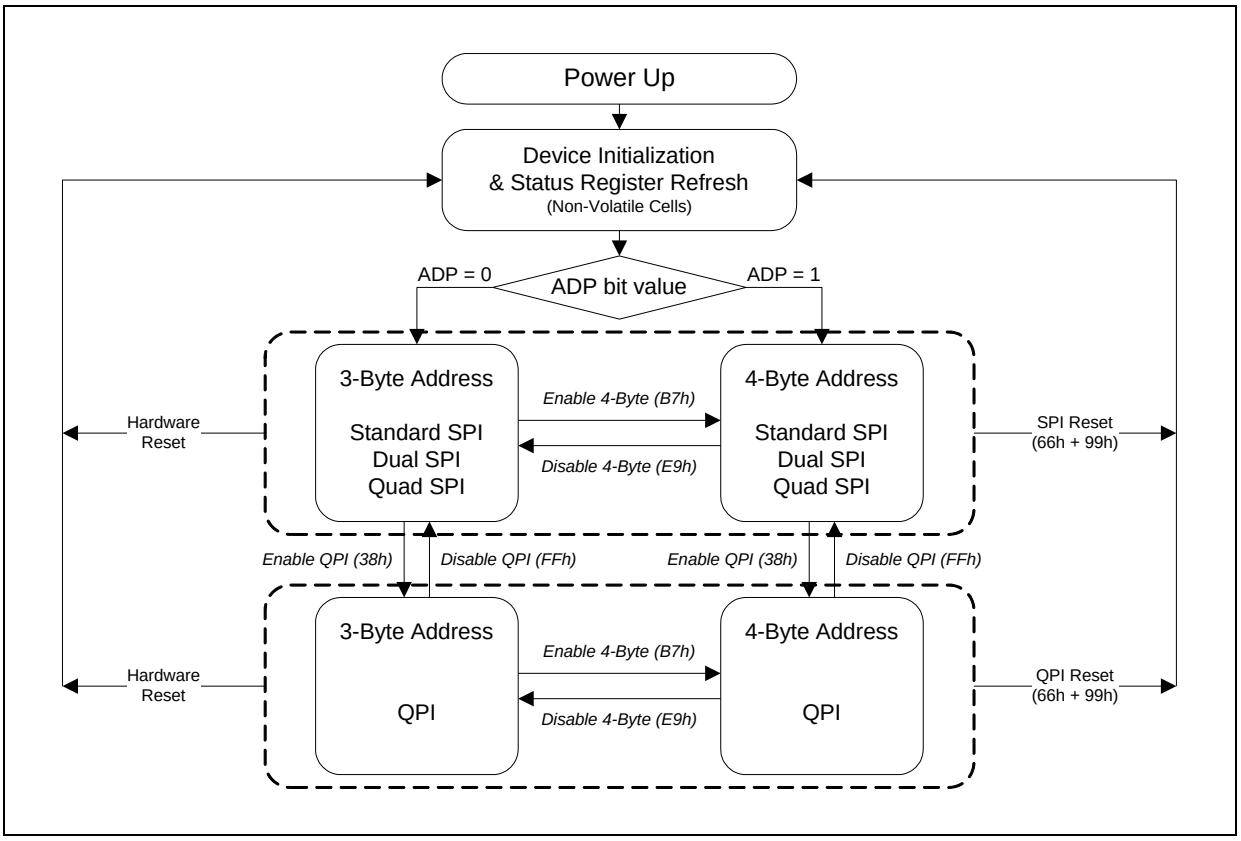



Figure 5.1 W25QxxRV Serial Flash Memory Operation Diagram

### 5.1.1 Standard SPI Instructions

The W25QxxRV is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 is the normal state of the CLK signal when the SPI bus master is in standby, and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

### 5.1.2 Dual SPI Instructions

The W25QxxRV supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

### 5.1.3 Quad SPI Instructions

The W25QxxRV supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, and “Fast Read Quad I/O (EBh)”. These instructions allow data to be transferred to or from the



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device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions, the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

### 5.1.4 QPI Instructions

The W25QxxRV supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enter QPI (38h)” instruction. The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via DI pin in eight serial clocks. The QPI mode utilizes all four IO pins to input the instruction code, thus only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. “Enter QPI (38h)” and “Exit QPI (FFh)” instructions are used to switch between these two modes. Upon power-up or after a software reset using “Reset (99h)” instruction, the default state of the device is Standard/Dual/Quad SPI mode. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI instructions, the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. See Figure 4 for the device operation modes.

### 5.1.5 SPI / QPI DTR Read Instructions

To effectively improve the read operation throughput without increasing the serial clock frequency, the W25QxxRV introduces multiple DTR (Double Transfer Rate) Read instructions that support Standard/Dual/Quad SPI and QPI modes. The byte-long instruction code is still latched into the device on the rising edge of the serial clock similar to all other SPI/QPI instructions. Once a DTR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

The SPI DTR and QPI DTR instructions are only supported with Part Number Suffix “M”



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### 5.1.6 3-Byte / 4-Byte Address Modes

The W25QxxRV provide two Address Modes that can be used to specify any byte of data in the memory array. The 3-Byte Address Mode is backward compatible to older generations of serial flash memory that only support up to 128M-bit data. To address the 256/512M-bit in 3-Byte Address Mode, Extended Address Register must be used in addition to the 3-Byte addresses.

4-Byte Address Mode is designed to support Serial Flash Memory devices from 256M-bit to 2G-bit. The extended Address Register is not necessary when the 4-Byte Address Mode is enabled.

Upon power up, the W25QxxRV can operate in either 3-Byte Address Mode or 4-Byte Address Mode, depending on the Non-Volatile Status Register Bit ADP (S17) setting. If ADP=0, the device will operate in 3-Byte Address Mode; if ADP=1, the device will operate in 4-Byte Address Mode. The factory default value for ADP is 0.

To switch between the 3-Byte or 4-Byte Address Modes, “Enter 4-Byte Mode (B7h)” or “Exit 4-Byte Mode (E9h)” instructions must be used. The current address mode is indicated by the Status Register Bit ADS (S16).

The W25QxxRV also supports a set of basic SPI instructions which requires dedicated 4-Byte address regardless of the device Address Mode setting. Please refer to the Instruction Set Tables for details.

### 5.1.7 Hold Function

For Standard SPI and Dual SPI operations, the /HOLD signal allows the W25QxxRV operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt required use of the SPI bus. In this case, the /HOLD function can save the state of the instruction and the data in the buffer, so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI. The Quad Enable Bit QE in Status Register-2 is used to determine if the pin is used as /HOLD pin or data I/O pin. When QE=0 (factory default), the pin is /HOLD. When QE=1, the pin will become an I/O pin, and the /HOLD function is no longer available.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low, the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low, the /HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.



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### 5.1.8 Software Reset & Hardware /RESET pin

The W25QxxRV can be reset to the initial power-on state by a software Reset sequence, either in SPI mode or QPI mode. This sequence must include two consecutive commands: Enable Reset (66h) & Reset (99h). If the command sequence is successfully accepted, the device will take approximately 30uS ($t_{RST}$) to reset. No command will be accepted during the reset period.

For the WSON-8 package types, W25QxxRV can also be configured to utilize a hardware /RESET pin. The HOLD/RST bit in the Status Register-3 is the configuration bit for /HOLD pin function or /RESET pin function. When HOLD/RST=0 (factory default), the pin acts as a /HOLD pin as described above; when HOLD/RST=1, the pin acts as a /RESET pin. Driving the /RESET pin low for a minimum period of ~1µs (tRESET*) will reset the device to its initial power-on state. Any on-going Program/Erase operation will be interrupted, and data corruption may happen. While /RESET is low, the device will not accept any command inputs.

If QE bit is set to 1, the /HOLD or /RESET function will be disabled, and the pin will become one of the four data I/O pins.

For the SOP-16 & TFBGA package, W25QxxRV provides a dedicated /RESET pin in addition to the /HOLD ($IO_3$) pin as illustrated in Figure 2.4. Driving the /RESET pin low for a minimum period of ~1µs (tRESET*) will reset the device to its initial power-on state. The HOLD/RST bit or the QE bit in the Status Register will not affect the function of this dedicated /RESET pin.

The Hardware /RESET pin has the highest priority among all the input signals. Driving /RESET low for a minimum period of ~1us (tRESET*) will interrupt any on-going external/internal operations, regardless the status of other SPI signals (/CS, CLK, IOs, /WP and/or /HOLD).

**Note:**

1. While a faster /RESET pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum pulse is recommended to ensure reliable operation.
2. There is an internal pull-up resistor for the dedicated /RESET pin on the SOP-16 & TFBGA package. If the reset function is not used, this pin can be left floating in the system.



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### 5.1.9 Reset Signaling Protocol

The W25QxxRV provides additional Hardware Reset by a signaling protocol. The key points for the Reset Signaling Protocol are CLK remains stable in either High or Low state. Toggle /CS instead of CLK. This prevents any confusion with a command, as no command bits are transferred (clocked). W25QxxRV captures the state of DI(IO0) on the rising edge of /CS. DI(IO0) have to be low on the first /CS, high on the second, low on the third, high on the fourth. This 05h pattern (=0b0101) is for differentiate from random noise. The hardware reset by signaling protocol release the deep power down state.

Once the Reset Signaling Protocol is accepted, any on-going internal operations will be terminated and will reset the device to its initial power-on state. It takes same busy time with power-on (tVSL and tPUW) because Hardware Reset goes into the same state of after power-on. No command will be accepted during the tVSL period. Please refer to “7.2.1 Device Reset (FFh), Enable Reset (66h) and Reset Device (99h)” for detail information about the value of each Status Registers after reset. If there is an on-going internal Erase or Program operation when Reset command sequence is accepted by the device, data corruption may happen at only the address that is the target of the on-going operation. It is recommended to check the BUSY bit in Status Register before issuing the Reset command.

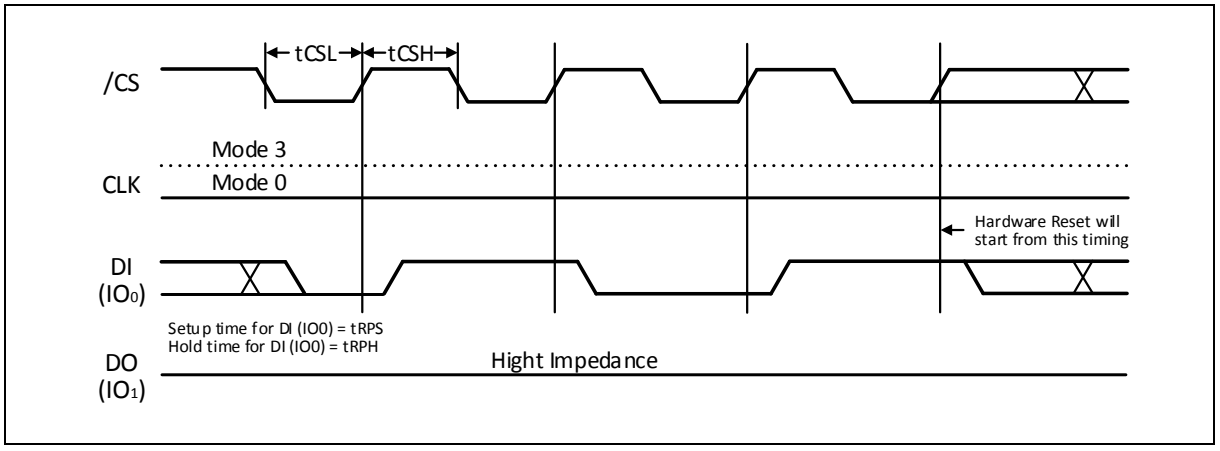



Figure 5.1.9. Reset Signaling Protocol



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## 5.2 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25QxxRV provides several means to protect the data from inadvertent writes.

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Status Registers
- Additional Flex Block/Sector Locks for array protection
- Write Protection using Power-down instruction
- Lock Down write protection for Status Register until the next power-up
- One Time Program (OTP) write protection for array and Security Registers using Status Register*

*** Note: This OTP feature is available upon special flow. Please contact Winbond for details**.

Upon power-up or at power-down, the W25QxxRV will maintain a reset condition while VCC is below the threshold value of $V_{WI}$, (7.3 Power-Up Power-Down Timing and Requirements). While reset, all operations are disabled, and no instructions are recognized. During power-up and after the VCC voltage exceeds $V_{WI}$, all program and erase related instructions are further disabled for a time delay of $t_{PUW}$. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and $t_{VSL}$ time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse command sequence. If needed, a pull-up resistor on /CS pin can be used to accomplish this.

After power-up, the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction, the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP, SRL) and Block Protect (CMP, TB, BP[3:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See the Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

The W25Q also provides an additional Write Protect method through the use of Flex Block/Sector Locks. Each 64KB block and each 4KB sector within the top and bottom blocks (totaling 32 sectors) is equipped with a Flex Block/Sector Lock bit. When the lock bit is set to 0, the corresponding sector or block can be erased or programmed; when the lock bit is set to 1, any Erase or Program command issued to that sector or block will be ignored. Upon power-up, software reset and hardware reset, if the WPS bit in status register 3 value is set to 0, all Flex Block/Sector Lock bits are initialized to 0. Upon power-up, software reset and hardware reset, if the WPS bit in status register 3 value is set to 1, all Flex Block/Sector Lock bits are initialized to 1, thereby protecting the entire memory array from Erase/Program operations. To unlock a specific sector or block, the “Flex Block/Sector Unlock (39h)” instruction must be issued.

When WPS bit is set to 0, the Flex block lock settings are active. This configuration is referred to as Flex Protection, which combines Flex Block/Sector Lock with Block Protect mechanisms (CMP, TB, BP[3:0]) to enable more flexible and fine-grained control overwrite protection.

When WPS bit is set to 1, only the Block Lock setting is active.



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Please refer to the table below for the number of lockable blocks and sectors available in each device model:

| Part No. | Density | Flex Block/Sector Locks |
|---|---|---|
| W25Q33RV | 32M-bit | 62 blocks (64KB each) + 32 sectors (4KB each) |
| W25Q64RV | 64M-bit | 126 blocks (64KB each) + 32 sectors (4KB each) |
| W25Q12RV | 128M-bit | 254 blocks (64KB each) + 32 sectors (4KB each) |
| W25Q25RV | 256M-bit | 510 blocks (64KB each) + 32 sectors (4KB each) |
| W25Q51RV | 512M-bit | 1022 blocks (64KB each) + 32 sectors (4KB each) |
| W25Q01RV | 1G-bit | [1022 blocks (64KB each) + 32 sectors (4KB each)] x 2 |
| W25Q02RV | 2G-bit | [1022 blocks (64KB each) + 32 sectors (4KB each)] x 4 |



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## 5.3 Status and Configuration Registers

Three Status and Configuration Registers are provided for the W25QxxRV series. The Read Status Register-1/2/3 instructions can be used to provide status on the availability of the flash memory array, whether the device is written enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, Erase/Program Suspend status, output driver strength, power-up and current Address Mode. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Security Register OTP locks, Hold/Reset functions, DSEN, output driver strength and power-up Address Mode. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP, SRL), the Write Enable instruction, and during Standard/Dual SPI operations, the /WP pin. The Extended Address Register stores the 4th Byte Address (most significant byte) in 3-Byte Address mode operation to access the full 256Mb address range.

### 5.3.1 Status Registers

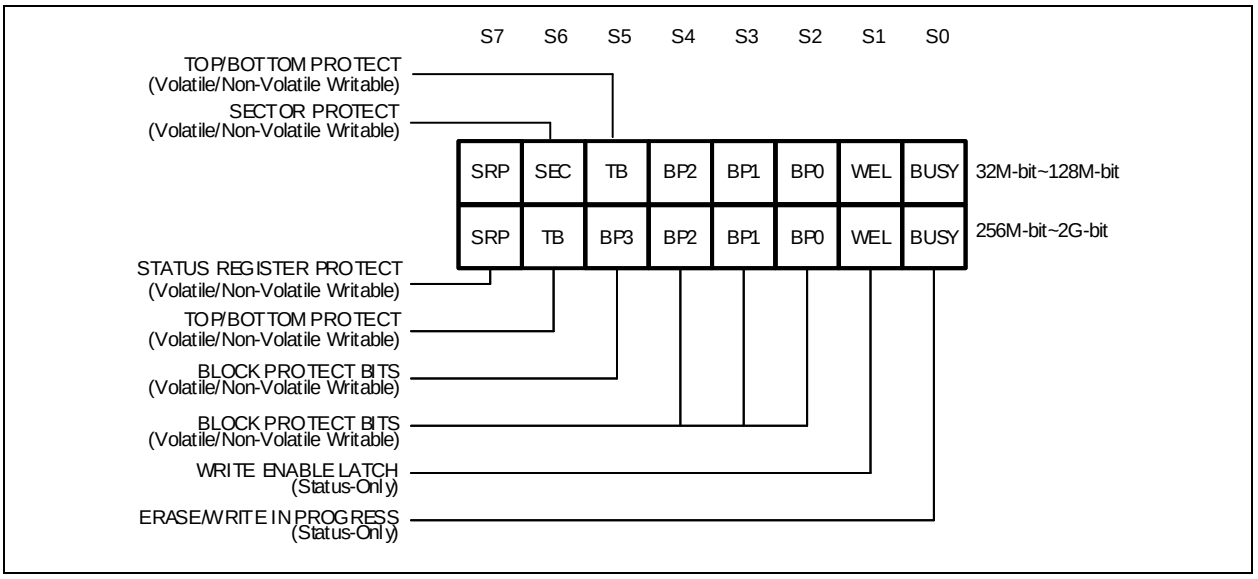



Figure 5.4.1. Status Register-1

### 5.3.2 Program/Erase/Write In Progress (BUSY) – *Status Only*

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction. During this time, the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions. Read Status Register instruction can always be used to poll the BUSY status during internal operations to determine if the operation has finished.

### 5.3.3 Write Enable Latch (WEL) – *Status Only*

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.

### 5.3.4 Block Protect Bits (BP3, BP2, BP1, BP0) – *Volatile/Non-Volatile Writable*

The Block Protect Bits (BP3, BP2, BP1, BP0) are non-volatile read/write bits in the status register (S5, S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write



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Status Register Instruction (see tw in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

### 5.3.5 Top/Bottom Block Protect (TB) – *Volatile/Non-Volatile Writable*

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP3, BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP, SRL and WEL bits.

### 5.3.6 Complement Protect (CMP) – Volatile/Non-Volatile Writable

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with TB, BP3, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by TB, BP3, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 64KB block can be protected while the rest of the array is not; when CMP=1, the top 64KB block will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.

### 5.3.7 Sector/Block Protect Bit (SEC) – *Volatile/Non-Volatile Writable*

The non-volatile Sector/Block Protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The default setting is SEC=0.



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### 5.3.8 Status Register Protect (SRP, SRL) – *Volatile/Non-Volatile Writable*

The Status Register Protect bits (SRP) are non-volatile read/write bits in the status register (S7). The SRP bit controls the method of write protection: software protection or hardware protection. The Status Register Lock bits (SRL) are non-volatile/volatile read/write bits in the status register (S8). The SRL bit controls the method of write protection: temporary lock-down or permanently one time program.

| SRL | SRP | /WP | Status Register | Description |
|---|---|---|---|---|
| 0 | 0 | X | Software Protection | /WP pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. [Factory Default] |
| 0 | 1 | 0 | Hardware Protected | When /WP pin is low the Status Register locked and cannot be written to. |
| 0 | 1 | 1 | Hardware Unprotected | When /WP pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1. |
| 1 | X | X | Power Supply Lock-Down | Status Register is protected and cannot be written to again until the next power-down, power-up cycle.(1) |
| 1 | X | X | One Time Program(2) | Status Register is permanently protected and cannot be written to. (**enabled by adding prefix command AAh, 55h)** |

**Note:**
1. When SRL =1, a power-down, power-up cycle will change SRL =0 state.
2. Please contact Winbond for details regarding the special instruction sequence.

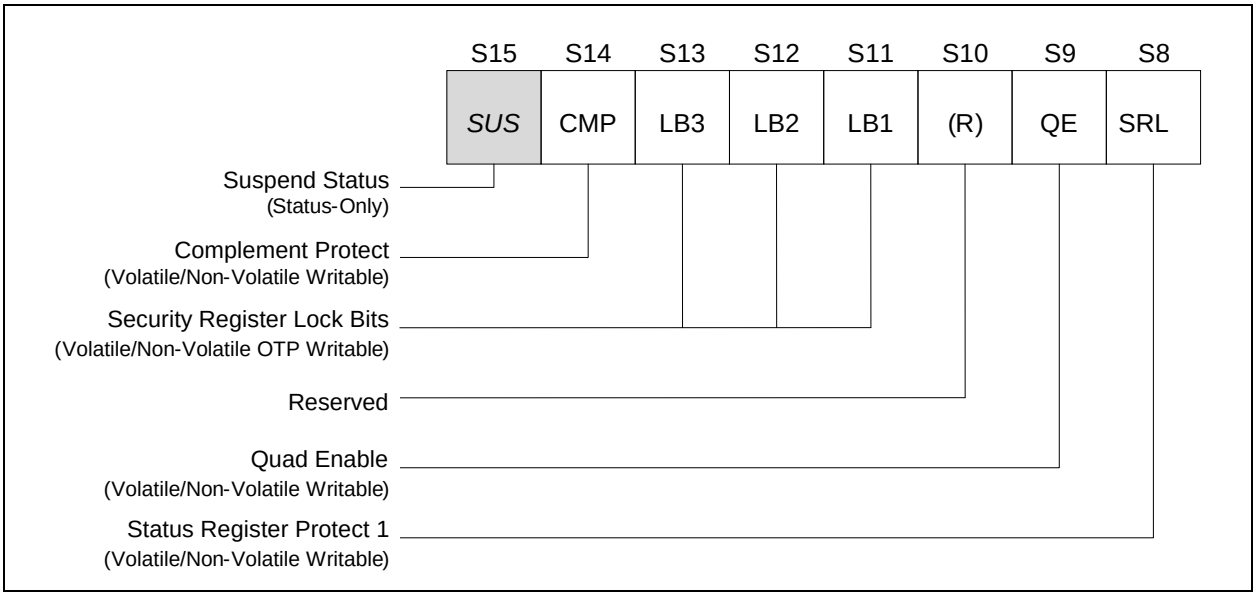



Figure 5.3.9. Status Register-2



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### 5.3.9 Erase/Program Suspend Status (SUS) – *Status Only*

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by the Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

### 5.3.10 Security Register Lock Bits (LB3, LB2, LB1, SFDP Lock) –*Non-Volatile OTP Writable*

The Security Register Lock Bits (LB3, LB2, LB1, SFDP Lock Bit) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11,S10) that provide the write protect control and status to the Security Registers. The default state of LB [3:1] is 0, Security Registers are unlocked. LB [3:1] can be set to 1 individually using the Write Status Register instruction. LB [3:1] are One Time Programmable (OTP). Once it's set to 1, the corresponding 256-Byte Security Register will become read-only permanently.

### 5.3.11 Quad Enable (QE) – Volatile/Non-Volatile Writable

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that enables Quad SPI operation. When the QE bit is set to a 0 state (factory default for part numbers with ordering options"-M"), the /WP pin and /HOLD are enabled, and the device operates in Standard/Dual SPI modes. When the QE bit is set to a 1((factory default for part numbers with ordering options"-Q"), the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled, the device operates in Standard/Dual/Quad SPI modes.

The QE bit is required to be set to a 1 before issuing an "Enter QPI (38h)" to switch the device from Standard/Dual/Quad SPI to QPI, otherwise the command will be ignored. When the device is in QPI mode, QE bit will remain a 1. A "Write Status Register" command in QPI mode cannot change the QE bit from a "1" to a "0".

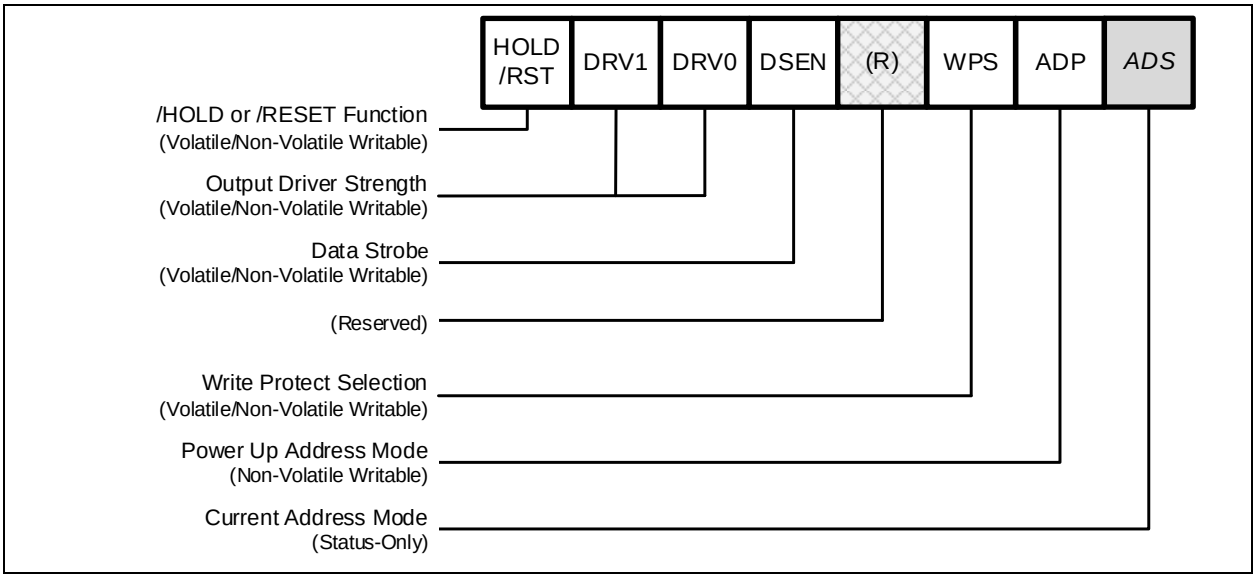



Figure 5.3.12. Status Register-3

### 5.3.12 Current Address Mode (ADS) – *Status Only*

The Current Address Mode bit is a read only bit in the Status Register-3 that indicates which address mode the device is currently operating in. When ADS=0, the device is in the 3-Byte Address Mode. When ADS=1, the device is in the 4-Byte Address Mode.



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### 5.3.13 Power-Up Address Mode (ADP) – Non-Volatile Writable

The ADP bit is a non-volatile bit that determines the initial address mode when the device is powered on or reset. This bit is only used during the power on or device reset initialization period, and it is only writable by the non-volatile Write Status sequence (06h + 11h). When ADP=0 (factory default). The device will power up into 3-Byte Address Mode. The Extended Address Register must be used to access memory regions beyond 128Mb. When ADP=1, the device will power up into 4-Byte Address Mode directly.

### 5.3.14 Write Protect Selection (WPS) – Volatile/Non-Volatile Writable

The WPS bit is used to select which Write Protect scheme should be used. When WPS=0, the device uses the combination of CMP, TB, BP [3:0] bits and Block Lock bits to protect a specific area of the memory array. When WPS=1, the device utilizes the Individual Block Locks to protect any individual sector or blocks. The CMP, TB and BP setting is ignored.

Upon power-up, software reset and hardware reset, If the WPS bit in status register 3 value is set to 0, all Flex Block/Sector Lock bits are initialized to 0; if the WPS bit in status register 3 value is set to 1, all Flex Block/Sector Lock bits are initialized to 1. Thereby protecting the entire memory array from Erase/Program operations. To unlock a specific sector or block, the “Flex Block/Sector Unlock (39h)” instruction must be issued.

Issuing the Write Status Register 3 instruction to change the WPS bit value will not change the Flex Block/Sector Lock bit setting.



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### 5.3.15 Data Strobe Function (DSEN)- *Volatile/Non-Volatile Writable*

On W25QxxRV, the Data Strobe (DS) bit is used during read operations and is not used during program, erase, or write operations. These bits are non-volatile read/write bits in the status register. DSEN = 0 (Disable); DSEN = 1 (Enable).

### 5.3.16 Output Driver Strength (DRV1, DRV0) – *Volatile/Non-Volatile Writable*

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

| DRV1, DRV0 | Resistance | Default value of Part Number and Suffix |
|---|---|---|
| 0, 0 | 25-ohm | W25Q02RV-Q/M |
| 0, 1 | 33-ohm | W25Q01RV-Q/M<br>W25Q33/64/12/25/51RV-N |
| 1, 0 | 50-ohm | W25Q33/64/12/25/51RV-Q/M |
| 1, 1 | 100-ohm | |

### 5.3.17 /HOLD or /RESET Pin Function (HOLD/RST) – *Volatile/Non-Volatile Writable*

The HOLD/RST bit is used to determine whether the /HOLD or /RESET function should be implemented on the hardware pin. When HOLD/RST=0 (factory default), the pin acts as /HOLD; when HOLD/RST=1, the pin acts as /RESET. However, the /HOLD or /RESET functions are only available when QE=0. If QE is set to 1, the /HOLD and /RESET functions are disabled, the pin acts as a dedicated data I/O pin.

### 5.3.18 Reserved Bits – *Non-Functional*

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of these bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effect.



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## 5.4 Status Register Memory Protection (WPS = 0)

### 5.4.1 W25Q33RV Status Register Memory Protection (WPS = 0, CMP = 0)

| STATUS REGISTER[1] | | | | | W25Q33RV (32M-BIT/ 4M-BYTE) MEMORY PROTECTION[3] | | | |
|---|---|---|---|---|---|---|---|---|
| SEC | TB | BP2 | BP1 | BP0 | PROTECTED BLOCK(S) | PROTECTED ADDRESSES | PROTECTED DENSITY | PROTECTED PORTION[2] |
| X | X | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 0 | 0 | 0 | 1 | 63 | 3F0000h – 3FFFFFh | 64KB | Upper 1/64 |
| 0 | 0 | 0 | 1 | 0 | 62 and 63 | 3E0000h – 3FFFFFh | 128KB | Upper 1/32 |
| 0 | 0 | 0 | 1 | 1 | 60 thru 63 | 3C0000h – 3FFFFFh | 256KB | Upper 1/16 |
| 0 | 0 | 1 | 0 | 0 | 56 thru 63 | 380000h – 3FFFFFh | 512KB | Upper 1/8 |
| 0 | 0 | 1 | 0 | 1 | 48 thru 63 | 300000h – 3FFFFFh | 1MB | Upper 1/4 |
| 0 | 0 | 1 | 1 | 0 | 32 thru 63 | 200000h – 3FFFFFh | 2MB | Upper 1/2 |
| 0 | 1 | 0 | 0 | 1 | 0 | 000000h – 00FFFFh | 64KB | Lower 1/64 |
| 0 | 1 | 0 | 1 | 0 | 0 and 1 | 000000h – 01FFFFh | 128KB | Lower 1/32 |
| 0 | 1 | 0 | 1 | 1 | 0 thru 3 | 000000h – 03FFFFh | 256KB | Lower 1/16 |
| 0 | 1 | 1 | 0 | 0 | 0 thru 7 | 000000h – 07FFFFh | 512KB | Lower 1/8 |
| 0 | 1 | 1 | 0 | 1 | 0 thru 15 | 000000h – 0FFFFFh | 1MB | Lower 1/4 |
| 0 | 1 | 1 | 1 | 0 | 0 thru 31 | 000000h – 1FFFFFh | 2MB | Lower 1/2 |
| X | X | 1 | 1 | 1 | 0 thru 63 | 000000h – 3FFFFFh | 4MB | ALL |
| 1 | 0 | 0 | 0 | 1 | 63 | 3FF000h – 3FFFFFh | 4KB | U - 1/1024 |
| 1 | 0 | 0 | 1 | 0 | 63 | 3FE000h – 3FFFFFh | 8KB | U - 1/512 |
| 1 | 0 | 0 | 1 | 1 | 63 | 3FC000h – 3FFFFFh | 16KB | U - 1/256 |
| 1 | 0 | 1 | 0 | X | 63 | 3F8000h – 3FFFFFh | 32KB | U - 1/128 |
| 1 | 0 | 1 | 1 | 0 | 63 | 3F8000h – 3FFFFFh | 32KB | U - 1/128 |
| 1 | 1 | 0 | 0 | 1 | 0 | 000000h – 000FFFh | 4KB | L - 1/1024 |
| 1 | 1 | 0 | 1 | 0 | 0 | 000000h – 001FFFh | 8KB | L - 1/512 |
| 1 | 1 | 0 | 1 | 1 | 0 | 000000h – 003FFFh | 16KB | L - 1/256 |
| 1 | 1 | 1 | 0 | X | 0 | 000000h – 007FFFh | 32KB | L - 1/128 |
| 1 | 1 | 1 | 1 | 0 | 0 | 000000h – 007FFFh | 32KB | L - 1/128 |

**Notes:**

1. X = don't care
2. L = Lower; U = Upper.
3. If any Erase or Program command specifies a memory region that contains a protected data portion, this command will be ignored.



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### 5.4.2 W25Q33RV Status Register Memory Protection ( WPS = 0, CMP = 1)

| STATUS REGISTER(1) | | | | | W25Q33RV (32M-BIT/ 4M-BYTE) MEMORY PROTECTION(3) | | | |
|---|---|---|---|---|---|---|---|---|
| SEC | TB | BP2 | BP1 | BP0 | PROTECTED BLOCK(S) | PROTECTED ADDRESSES | PROTECTED DENSITY | PROTECTED PORTION(2) |
| X | X | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 0 | 0 | 0 | 1 | 63 | 3F0000h – 3FFFFFh | 64KB | Upper 1/64 |
| 0 | 0 | 0 | 1 | 0 | 62 and 63 | 3E0000h – 3FFFFFh | 128KB | Upper 1/32 |
| 0 | 0 | 0 | 1 | 1 | 60 thru 63 | 3C0000h – 3FFFFFh | 256KB | Upper 1/16 |
| 0 | 0 | 1 | 0 | 0 | 56 thru 63 | 380000h – 3FFFFFh | 512KB | Upper 1/8 |
| 0 | 0 | 1 | 0 | 1 | 48 thru 63 | 300000h – 3FFFFFh | 1MB | Upper 1/4 |
| 0 | 0 | 1 | 1 | 0 | 32 thru 63 | 200000h – 3FFFFFh | 2MB | Upper 1/2 |
| 0 | 1 | 0 | 0 | 1 | 0 | 000000h – 00FFFFh | 64KB | Lower 1/64 |
| 0 | 1 | 0 | 1 | 0 | 0 and 1 | 000000h – 01FFFFh | 128KB | Lower 1/32 |
| 0 | 1 | 0 | 1 | 1 | 0 thru 3 | 000000h – 03FFFFh | 256KB | Lower 1/16 |
| 0 | 1 | 1 | 0 | 0 | 0 thru 7 | 000000h – 07FFFFh | 512KB | Lower 1/8 |
| 0 | 1 | 1 | 0 | 1 | 0 thru 15 | 000000h – 0FFFFFh | 1MB | Lower 1/4 |
| 0 | 1 | 1 | 1 | 0 | 0 thru 31 | 000000h – 1FFFFFh | 2MB | Lower 1/2 |
| X | X | 1 | 1 | 1 | 0 thru 63 | 000000h – 3FFFFFh | 4MB | ALL |
| 1 | 0 | 0 | 0 | 1 | 63 | 3FF000h – 3FFFFFh | 4KB | U - 1/1024 |
| 1 | 0 | 0 | 1 | 0 | 63 | 3FE000h – 3FFFFFh | 8KB | U - 1/512 |
| 1 | 0 | 0 | 1 | 1 | 63 | 3FC000h – 3FFFFFh | 16KB | U - 1/256 |
| 1 | 0 | 1 | 0 | X | 63 | 3F8000h – 3FFFFFh | 32KB | U - 1/128 |
| 1 | 0 | 1 | 1 | 0 | 63 | 3F8000h – 3FFFFFh | 32KB | U - 1/128 |
| 1 | 1 | 0 | 0 | 1 | 0 | 000000h – 000FFFh | 4KB | L - 1/1024 |
| 1 | 1 | 0 | 1 | 0 | 0 | 000000h – 001FFFh | 8KB | L - 1/512 |
| 1 | 1 | 0 | 1 | 1 | 0 | 000000h – 003FFFh | 16KB | L - 1/256 |
| 1 | 1 | 1 | 0 | X | 0 | 000000h – 007FFFh | 32KB | L - 1/128 |
| 1 | 1 | 1 | 1 | 0 | 0 | 000000h – 007FFFh | 32KB | L - 1/128 |

**Notes:**
1. X = don't care
2. L = Lower; U = Upper.
3. If any Erase or Program command specifies a memory region that contains a protected data portion, this command will be ignored.



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### 5.4.3 W25Q64RV Status Register Memory Protection (WPS = 0, CMP = 0)

| Status Register[1] | | | | | W25Q64RV (64M-bit/ 8M-Byte) Memory Protection[3] | | | |
|---|---|---|---|---|---|---|---|---|
| SEC | TB | BP2 | BP1 | BP0 | PROTECTED BLOCK(S) | PROTECTED ADDRESSES | PROTECTED DENSITY | PROTECTED PORTION[2] |
| X | X | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 0 | 0 | 0 | 1 | 126 and 127 | 7E0000h – 7FFFFFh | 128KB | Upper 1/64 |
| 0 | 0 | 0 | 1 | 0 | 124 thru 127 | 7C0000h – 7FFFFFh | 256KB | Upper 1/32 |
| 0 | 0 | 0 | 1 | 1 | 120 thru 127 | 780000h – 7FFFFFh | 512KB | Upper 1/16 |
| 0 | 0 | 1 | 0 | 0 | 112 thru 127 | 700000h – 7FFFFFh | 1MB | Upper 1/8 |
| 0 | 0 | 1 | 0 | 1 | 96 thru 127 | 600000h – 7FFFFFh | 2MB | Upper 1/4 |
| 0 | 0 | 1 | 1 | 0 | 64 thru 127 | 400000h – 7FFFFFh | 4MB | Upper 1/2 |
| 0 | 1 | 0 | 0 | 1 | 0 and 1 | 000000h – 01FFFFh | 128KB | Lower 1/64 |
| 0 | 1 | 0 | 1 | 0 | 0 thru 3 | 000000h – 03FFFFh | 256KB | Lower 1/32 |
| 0 | 1 | 0 | 1 | 1 | 0 thru 7 | 000000h – 07FFFFh | 512KB | Lower 1/16 |
| 0 | 1 | 1 | 0 | 0 | 0 thru 15 | 000000h – 0FFFFFh | 1MB | Lower 1/8 |
| 0 | 1 | 1 | 0 | 1 | 0 thru 31 | 000000h – 1FFFFFh | 2MB | Lower 1/4 |
| 0 | 1 | 1 | 1 | 0 | 0 thru 63 | 000000h – 3FFFFFh | 4MB | Lower 1/2 |
| X | X | 1 | 1 | 1 | 0 thru 127 | 000000h – 7FFFFFh | 8MB | ALL |
| 1 | 0 | 0 | 0 | 1 | 127 | 7FF000h – 7FFFFFh | 4KB | U – 1/2048 |
| 1 | 0 | 0 | 1 | 0 | 127 | 7FE000h – 7FFFFFh | 8KB | U – 1/1024 |
| 1 | 0 | 0 | 1 | 1 | 127 | 7FC000h – 7FFFFFh | 16KB | U – 1/512 |
| 1 | 0 | 1 | 0 | X | 127 | 7F8000h – 7FFFFFh | 32KB | U – 1/256 |
| 1 | 1 | 0 | 0 | 1 | 0 | 000000h – 000FFFh | 4KB | L – 1/2048 |
| 1 | 1 | 0 | 1 | 0 | 0 | 000000h – 001FFFh | 8KB | L – 1/1024 |
| 1 | 1 | 0 | 1 | 1 | 0 | 000000h – 003FFFh | 16KB | L – 1/512 |
| 1 | 1 | 1 | 0 | X | 0 | 000000h – 007FFFh | 32KB | L – 1/256 |

**Notes:**
1. X = don't care
2. L = Lower; U = Upper.
3. If any Erase or Program command specifies a memory region that contains a protected data portion, this command will be ignored.



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### 5.4.4 W25Q64RV Status Register Memory Protection (WPS = 0, CMP = 1)

| Status Register[1] | | | | | W25Q64RV (64M-bit/ 8M-Byte) Memory Protection[3] | | | |
|---|---|---|---|---|---|---|---|---|
| SEC | TB | SEC | TB | SEC | PROTECTED BLOCK(S) | PROTECTED ADDRESSES | PROTECTED DENSITY | PROTECTED PORTION[2] |
| X | X | 0 | 0 | 0 | 0 thru 127 | 000000h – 7FFFFFh | 8MB | ALL |
| 0 | 0 | 0 | 0 | 1 | 0 thru 125 | 000000h – 7DFFFFh | 8,064KB | Lower 63/64 |
| 0 | 0 | 0 | 1 | 0 | 0 thru 123 | 000000h – 7BFFFFh | 7,936KB | Lower 31/32 |
| 0 | 0 | 0 | 1 | 1 | 0 thru 119 | 000000h – 77FFFFh | 7,680KB | Lower 15/16 |
| 0 | 0 | 1 | 0 | 0 | 0 thru 111 | 000000h – 6FFFFFh | 7MB | Lower 7/8 |
| 0 | 0 | 1 | 0 | 1 | 0 thru 95 | 000000h – 5FFFFFh | 5MB | Lower 3/4 |
| 0 | 0 | 1 | 1 | 0 | 0 thru 63 | 000000h – 3FFFFFh | 4MB | Lower 1/2 |
| 0 | 1 | 0 | 0 | 1 | 2 thru 127 | 020000h – 7FFFFFh | 8,064KB | Upper 63/64 |
| 0 | 1 | 0 | 1 | 0 | 4 thru 127 | 040000h – 7FFFFFh | 7,936KB | Upper 31/32 |
| 0 | 1 | 0 | 1 | 1 | 8 thru 127 | 080000h – 7FFFFFh | 7,680KB | Upper 15/16 |
| 0 | 1 | 1 | 0 | 0 | 16 thru 127 | 100000h – 7FFFFFh | 7MB | Upper 7/8 |
| 0 | 1 | 1 | 0 | 1 | 32 thru 127 | 200000h – 7FFFFFh | 5MB | Upper 3/4 |
| 0 | 1 | 1 | 1 | 0 | 64 thru 127 | 400000h – 7FFFFFh | 4MB | Upper 1/2 |
| X | X | 1 | 1 | 1 | NONE | NONE | NONE | NONE |
| 1 | 0 | 0 | 0 | 1 | 0 thru 127 | 000000h – 7FEFFFh | 8,188KB | L – 2047/2048 |
| 1 | 0 | 0 | 1 | 0 | 0 thru 127 | 000000h – 7FDFFFh | 8,184KB | L – 1023/1024 |
| 1 | 0 | 0 | 1 | 1 | 0 thru 127 | 000000h – 7FBFFFh | 8,176KB | L – 511/512 |
| 1 | 0 | 1 | 0 | X | 0 thru 127 | 000000h – 7F7FFFh | 8,160KB | L – 255/256 |
| 1 | 1 | 0 | 0 | 1 | 0 thru 127 | 001000h – 7FFFFFh | 8,188KB | L – 2047/2048 |
| 1 | 1 | 0 | 1 | 0 | 0 thru 127 | 002000h – 7FFFFFh | 8,184KB | L – 1023/1024 |
| 1 | 1 | 0 | 1 | 1 | 0 thru 127 | 004000h – 7FFFFFh | 8,176KB | L – 511/512 |
| 1 | 1 | 1 | 0 | X | 0 thru 127 | 008000h – 7FFFFFh | 8,160KB | L – 255/256 |

**Notes:**
1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains a protected data portion, this command will be ignored.



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### 5.4.5 W25Q12RV Status Register Memory Protection (WPS = 0, CMP = 0)

| STATUS REGISTER[1] | | | | | W25Q12RV (128M-BIT/ 16M-BYTE) MEMORY PROTECTION[3] | | | |
|---|---|---|---|---|---|---|---|---|
| SEC | TB | BP2 | BP1 | BP0 | PROTECTED BLOCK(S) | PROTECTED ADDRESSES | PROTECTED DENSITY | PROTECTED PORTION[2] |
| X | X | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 0 | 0 | 0 | 1 | 252 thru 255 | FC0000h – FFFFFFh | 256KB | Upper 1/64 |
| 0 | 0 | 0 | 1 | 0 | 248 thru 255 | F80000h – FFFFFFh | 512KB | Upper 1/32 |
| 0 | 0 | 0 | 1 | 1 | 240 thru 255 | F00000h – FFFFFFh | 1MB | Upper 1/16 |
| 0 | 0 | 1 | 0 | 0 | 224 thru 255 | E00000h – FFFFFFh | 2MB | Upper 1/8 |
| 0 | 0 | 1 | 0 | 1 | 192 thru 255 | C00000h – FFFFFFh | 4MB | Upper 1/4 |
| 0 | 0 | 1 | 1 | 0 | 128 thru 255 | 800000h – FFFFFFh | 8MB | Upper 1/2 |
| 0 | 1 | 0 | 0 | 1 | 0 thru 3 | 000000h – 03FFFFh | 256KB | Lower 1/64 |
| 0 | 1 | 0 | 1 | 0 | 0 thru 7 | 000000h – 07FFFFh | 512KB | Lower 1/32 |
| 0 | 1 | 0 | 1 | 1 | 0 thru 15 | 000000h – 0FFFFFh | 1MB | Lower 1/16 |
| 0 | 1 | 1 | 0 | 0 | 0 thru 31 | 000000h – 1FFFFFh | 2MB | Lower 1/8 |
| 0 | 1 | 1 | 0 | 1 | 0 thru 63 | 000000h – 3FFFFFh | 4MB | Lower 1/4 |
| 0 | 1 | 1 | 1 | 0 | 0 thru 127 | 000000h – 7FFFFFh | 8MB | Lower 1/2 |
| X | X | 1 | 1 | 1 | 0 thru 255 | 000000h – FFFFFFh | 16MB | ALL |
| 1 | 0 | 0 | 0 | 1 | 255 | FFF000h – FFFFFFh | 4KB | U - 1/4096 |
| 1 | 0 | 0 | 1 | 0 | 255 | FFE000h – FFFFFFh | 8KB | U - 1/2048 |
| 1 | 0 | 0 | 1 | 1 | 255 | FFC000h – FFFFFFh | 16KB | U - 1/1024 |
| 1 | 0 | 1 | 0 | X | 255 | FF8000h – FFFFFFh | 32KB | U - 1/512 |
| 1 | 1 | 0 | 0 | 1 | 0 | 000000h – 000FFFh | 4KB | L - 1/4096 |
| 1 | 1 | 0 | 1 | 0 | 0 | 000000h – 001FFFh | 8KB | L - 1/2048 |
| 1 | 1 | 0 | 1 | 1 | 0 | 000000h – 003FFFh | 16KB | L - 1/1024 |
| 1 | 1 | 1 | 0 | X | 0 | 000000h – 007FFFh | 32KB | L - 1/512 |

**Notes:**
1. X = don't care
2. L = Lower; U = Upper.
3. If any Erase or Program command specifies a memory region that contains a protected data portion, this command will be ignored.



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### 5.4.6 W25Q12RV Status Register Memory Protection (WPS = 0, CMP = 1)

| STATUS REGISTER[1] | | | | | W25Q12RV (128M-BIT/ 16M-BYTE) MEMORY PROTECTION[3] | | | |
|---|---|---|---|---|---|---|---|---|
| SEC | TB | BP2 | BP1 | BP0 | PROTECTED BLOCK(S) | PROTECTED ADDRESSES | PROTECTED DENSITY | PROTECTED PORTION[2] |
| X | X | 0 | 0 | 0 | 0 thru 255 | 000000h - FFFFFFh | 16MB | ALL |
| 0 | 0 | 0 | 0 | 1 | 0 thru 251 | 000000h - FBFFFFh | 16,128KB | Lower 63/64 |
| 0 | 0 | 0 | 1 | 0 | 0 thru 247 | 000000h – F7FFFFh | 15,872KB | Lower 31/32 |
| 0 | 0 | 0 | 1 | 1 | 0 thru 239 | 000000h - EFFFFFh | 15MB | Lower 15/16 |
| 0 | 0 | 1 | 0 | 0 | 0 thru 223 | 000000h - DFFFFFh | 14MB | Lower 7/8 |
| 0 | 0 | 1 | 0 | 1 | 0 thru 191 | 000000h - BFFFFFh | 12MB | Lower 3/4 |
| 0 | 0 | 1 | 1 | 0 | 0 thru 127 | 000000h - 7FFFFFh | 8MB | Lower 1/2 |
| 0 | 1 | 0 | 0 | 1 | 4 thru 255 | 040000h - FFFFFFh | 16,128KB | Upper 63/64 |
| 0 | 1 | 0 | 1 | 0 | 8 thru 255 | 080000h - FFFFFFh | 15,872KB | Upper 31/32 |
| 0 | 1 | 0 | 1 | 1 | 16 thru 255 | 100000h - FFFFFFh | 15MB | Upper 15/16 |
| 0 | 1 | 1 | 0 | 0 | 32 thru 255 | 200000h - FFFFFFh | 14MB | Upper 7/8 |
| 0 | 1 | 1 | 0 | 1 | 64 thru 255 | 400000h - FFFFFFh | 12MB | Upper 3/4 |
| 0 | 1 | 1 | 1 | 0 | 128 thru 255 | 800000h - FFFFFFh | 8MB | Upper 1/2 |
| X | X | 1 | 1 | 1 | NONE | NONE | NONE | NONE |
| 1 | 0 | 0 | 0 | 1 | 0 thru 255 | 000000h – FFEFFFh | 16,380KB | L - 4095/4096 |
| 1 | 0 | 0 | 1 | 0 | 0 thru 255 | 000000h – FFDFFFh | 16,376KB | L - 2047/2048 |
| 1 | 0 | 0 | 1 | 1 | 0 thru 255 | 000000h – FFBFFFh | 16,368KB | L - 1023/1024 |
| 1 | 0 | 1 | 0 | X | 0 thru 255 | 000000h – FF7FFFh | 16,352KB | L - 511/512 |
| 1 | 1 | 0 | 0 | 1 | 0 thru 255 | 001000h – FFFFFFh | 16,380KB | U - 4095/4096 |
| 1 | 1 | 0 | 1 | 0 | 0 thru 255 | 002000h – FFFFFFh | 16,376KB | U - 2047/2048 |
| 1 | 1 | 0 | 1 | 1 | 0 thru 255 | 004000h – FFFFFFh | 16,368KB | U -1023/1024 |
| 1 | 1 | 1 | 0 | X | 0 thru 255 | 008000h – FFFFFFh | 16,352KB | U - 511/512 |

**Notes:**
1. X = don't care
2. L = Lower; U = Upper.
3. If any Erase or Program command specifies a memory region that contains a protected data portion, this command will be ignored.



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### 5.4.7 W25Q25RV Status Register Memory Protection (WPS = 0, CMP = 0)

| STATUS REGISTER(1) | | | | | W25Q25RV (256M-BIT / 32M-BYTE) MEMORY PROTECTION(2) | | | |
|---|---|---|---|---|---|---|---|---|
| TB | BP3 | BP2 | BP1 | BP0 | PROTECTED BLOCK(S) | PROTECTED ADDRESSES | PROTECTED DENSITY | PROTECTED PORTION |
| X | 0 | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 0 | 0 | 0 | 1 | 511 | 01FF0000h - 01FFFFFFh | 64KB | Upper 1/512 |
| 0 | 0 | 0 | 1 | 0 | 510 thru 511 | 01FE0000h - 01FFFFFFh | 128KB | Upper 1/256 |
| 0 | 0 | 0 | 1 | 1 | 508 thru 511 | 01FC0000h - 01FFFFFFh | 256KB | Upper 1/128 |
| 0 | 0 | 1 | 0 | 0 | 504 thru 511 | 01F80000h - 01FFFFFFh | 512KB | Upper 1/64 |
| 0 | 0 | 1 | 0 | 1 | 496 thru 511 | 01F00000h - 01FFFFFFh | 1MB | Upper 1/32 |
| 0 | 0 | 1 | 1 | 0 | 480 thru 511 | 01E00000h - 01FFFFFFh | 2MB | Upper 1/16 |
| 0 | 0 | 1 | 1 | 1 | 448 thru 511 | 01C00000h - 01FFFFFFh | 4MB | Upper 1/8 |
| 0 | 1 | 0 | 0 | 0 | 384 thru 511 | 01800000h - 01FFFFFFh | 8MB | Upper 1/4 |
| 0 | 1 | 0 | 0 | 1 | 256 thru 511 | 01000000h - 01FFFFFFh | 16MB | Upper 1/2 |
| 1 | 0 | 0 | 0 | 1 | 0 | 00000000h - 0000FFFFh | 64KB | Lower 1/512 |
| 1 | 0 | 0 | 1 | 0 | 0 thru 1 | 00000000h - 0001FFFFh | 128KB | Lower 1/256 |
| 1 | 0 | 0 | 1 | 1 | 0 thru 3 | 00000000h - 0003FFFFh | 256KB | Lower 1/128 |
| 1 | 0 | 1 | 0 | 0 | 0 thru 7 | 00000000h - 0007FFFFh | 512KB | Lower 1/64 |
| 1 | 0 | 1 | 0 | 1 | 0 thru 15 | 00000000h - 000FFFFFh | 1MB | Lower 1/32 |
| 1 | 0 | 1 | 1 | 0 | 0 thru 31 | 00000000h - 001FFFFFh | 2MB | Lower 1/16 |
| 1 | 0 | 1 | 1 | 1 | 0 thru 63 | 00000000h - 003FFFFFh | 4MB | Lower 1/8 |
| 1 | 1 | 0 | 0 | 0 | 0 thru 127 | 00000000h - 007FFFFFh | 8MB | Lower 1/4 |
| 1 | 1 | 0 | 0 | 1 | 0 thru 255 | 00000000h - 00FFFFFFh | 16MB | Lower 1/2 |
| X | 1 | 1 | 0 | X | 0 thru 511 | 00000000h - 01FFFFFFh | 32MB | ALL |
| X | 1 | X | 1 | X | 0 thru 511 | 00000000h - 01FFFFFFh | 32MB | ALL |

**Notes:**
1. X = don't care
2. If any Erase or Program command specifies a memory region that contains a protected data portion, this command will be ignored.



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### 5.4.8 W25Q25RV Status Register Memory Protection (WPS = 0, CMP = 1)

| STATUS REGISTER[1] | | | | | W25Q25RV (256M-BIT / 32M-BYTE) MEMORY PROTECTION[2] | | | |
|---|---|---|---|---|---|---|---|---|
| TB | BP3 | BP2 | BP1 | BP0 | PROTECTED BLOCK(S) | PROTECTED ADDRESSES | PROTECTED DENSITY | PROTECTED PORTION |
| X | 0 | 0 | 0 | 0 | ALL | 00000000h - 01FFFFFFh | ALL | ALL |
| 0 | 0 | 0 | 0 | 1 | 0 thru 510 | 00000000h - 01FEFFFFh | 32,704KB | Lower 511/512 |
| 0 | 0 | 0 | 1 | 0 | 0 thru 509 | 00000000h - 01FDFFFFh | 32,640KB | Lower 255/256 |
| 0 | 0 | 0 | 1 | 1 | 0 thru 507 | 00000000h - 01FBFFFFh | 32,512KB | Lower 127/128 |
| 0 | 0 | 1 | 0 | 0 | 0 thru 503 | 00000000h - 01F7FFFFh | 32,256KB | Lower 63/64 |
| 0 | 0 | 1 | 0 | 1 | 0 thru 495 | 00000000h - 01EFFFFFh | 31MB | Lower 31/32 |
| 0 | 0 | 1 | 1 | 0 | 0 thru 479 | 00000000h - 01DFFFFFh | 30MB | Lower 15/16 |
| 0 | 0 | 1 | 1 | 1 | 0 thru 447 | 00000000h - 01BFFFFFh | 28MB | Lower 7/8 |
| 0 | 1 | 0 | 0 | 0 | 0 thru 383 | 00000000h - 017FFFFFh | 24MB | Lower 3/4 |
| 0 | 1 | 0 | 0 | 1 | 0 thru 255 | 00000000h - 00FFFFFFh | 16MB | Lower 1/2 |
| 1 | 0 | 0 | 0 | 1 | 1 thru 511 | 00010000h - 01FFFFFFh | 32,704KB | Upper 511/512 |
| 1 | 0 | 0 | 1 | 0 | 2 thru 511 | 00020000h - 01FFFFFFh | 32,640KB | Upper 255/256 |
| 1 | 0 | 0 | 1 | 1 | 4 thru 511 | 00040000h - 01FFFFFFh | 32,512KB | Upper 127/128 |
| 1 | 0 | 1 | 0 | 0 | 8 thru 511 | 00080000h - 01FFFFFFh | 32,256KB | Upper 63/64 |
| 1 | 0 | 1 | 0 | 1 | 16 thru 511 | 00100000h - 01FFFFFFh | 31MB | Upper 31/32 |
| 1 | 0 | 1 | 1 | 0 | 32 thru 511 | 00200000h - 01FFFFFFh | 30MB | Upper 15/16 |
| 1 | 0 | 1 | 1 | 1 | 64 thru 511 | 00400000h - 01FFFFFFh | 28MB | Upper 7/8 |
| 1 | 1 | 0 | 0 | 0 | 128 thru 511 | 00800000h - 01FFFFFFh | 24MB | Upper 3/4 |
| 1 | 1 | 0 | 0 | 1 | 256 thru 511 | 01000000h - 01FFFFFFh | 16MB | Upper 1/2 |
| X | 1 | 1 | 0 | X | NONE | NONE | NONE | NONE |
| X | 1 | X | 1 | X | NONE | NONE | NONE | NONE |

**Notes:**
1. X = don't care
2. If any Erase or Program command specifies a memory region that contains a protected data portion, this command will be ignored.



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### 5.4.9 W25Q51RV Status Register Memory Protection (WPS = 0, CMP = 0)

| STATUS REGISTER(1) | | | | | W25Q51RV (512M-BIT / 64M-BYTE) MEMORY PROTECTION(2) | | | |
|---|---|---|---|---|---|---|---|---|
| TB | BP3 | BP2 | BP1 | BP0 | PROTECTED BLOCK(S) | PROTECTED ADDRESSES | PROTECTED DENSITY | PROTECTED PORTION |
| 0 | 0 | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 0 | 0 | 0 | 1 | 1023 | 03FF0000h - 03FFFFFFh | 64KB | Upper 1/1024 |
| 0 | 0 | 0 | 1 | 0 | 1022 thru 1023 | 03FE0000h - 03FFFFFFh | 128KB | Upper 1/512 |
| 0 | 0 | 0 | 1 | 1 | 1020 thru 1023 | 03FC0000h - 03FFFFFFh | 256KB | Upper 1/256 |
| 0 | 0 | 1 | 0 | 0 | 1016 thru 1023 | 03F80000h - 03FFFFFFh | 512KB | Upper 1/128 |
| 0 | 0 | 1 | 0 | 1 | 1008 thru 1023 | 03F00000h - 03FFFFFFh | 1MB | Upper 1/64 |
| 0 | 0 | 1 | 1 | 0 | 992 thru 1023 | 03E00000h - 03FFFFFFh | 2MB | Upper 1/32 |
| 0 | 0 | 1 | 1 | 1 | 960 thru 1023 | 03C00000h - 03FFFFFFh | 4MB | Upper 1/16 |
| 0 | 1 | 0 | 0 | 0 | 896 thru 1023 | 03800000h - 03FFFFFFh | 8MB | Upper 1/8 |
| 0 | 1 | 0 | 0 | 1 | 768 thru 1023 | 03000000h - 03FFFFFFh | 16MB | Upper 1/4 |
| 0 | 1 | 0 | 1 | 0 | 512 thru 1023 | 02000000h - 03FFFFFFh | 32MB | Upper 1/2 |
| 0 | 1 | 0 | 1 | 1 | 0 thru 1023 | 00000000h - 03FFFFFFh | 64MB | ALL |
| 0 | 1 | 1 | 0 | 0 | 0 thru 1023 | 00000000h - 03FFFFFFh | 64MB | ALL |
| 0 | 1 | 1 | 0 | 1 | 0 thru 1023 | 00000000h - 03FFFFFFh | 64MB | ALL |
| 0 | 1 | 1 | 1 | 0 | 0 thru 1023 | 00000000h - 03FFFFFFh | 64MB | ALL |
| 0 | 1 | 1 | 1 | 1 | 0 thru 1023 | 00000000h - 03FFFFFFh | 64MB | ALL |
| 1 | 0 | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 1 | 0 | 0 | 0 | 1 | 0 | 00000000h - 0000FFFFh | 64KB | Lower 1/1024 |
| 1 | 0 | 0 | 1 | 0 | 0 thru 1 | 00000000h - 0001FFFFh | 128KB | Lower 1/512 |
| 1 | 0 | 0 | 1 | 1 | 0 thru 3 | 00000000h - 0003FFFFh | 256KB | Lower 1/256 |
| 1 | 0 | 1 | 0 | 0 | 0 thru 7 | 00000000h - 0007FFFFh | 512KB | Lower 1/128 |
| 1 | 0 | 1 | 0 | 1 | 0 thru 15 | 00000000h - 000FFFFFh | 1MB | Lower 1/64 |
| 1 | 0 | 1 | 1 | 0 | 0 thru 31 | 00000000h - 001FFFFFh | 2MB | Lower 1/32 |
| 1 | 0 | 1 | 1 | 1 | 0 thru 63 | 00000000h - 003FFFFFh | 4MB | Lower 1/16 |
| 1 | 1 | 0 | 0 | 0 | 0 thru 127 | 00000000h - 007FFFFFh | 8MB | Lower 1/8 |
| 1 | 1 | 0 | 0 | 1 | 0 thru 255 | 00000000h - 00FFFFFFh | 16MB | Lower 1/4 |
| 1 | 1 | 0 | 1 | 0 | 0 thru 511 | 00000000h - 01FFFFFFh | 32MB | Lower 1/2 |
| 1 | 1 | 0 | 1 | 1 | 0 thru 1023 | 00000000h - 03FFFFFFh | 64MB | ALL |
| 1 | 1 | 1 | X | X | 0 thru 1023 | 00000000h - 03FFFFFFh | 64MB | ALL |

**Notes:**

1. X = don't care
2. If any Erase or Program command specifies a memory region that contains a protected data portion, this command will be ignored.



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### 5.4.10 W25Q51RV Status Register Memory Protection (WPS = 0, CMP = 1)

| STATUS REGISTER(1) | | | | | W25Q51RV (512M-BIT / 64M-BYTE) MEMORY PROTECTION(2) | | | |
|---|---|---|---|---|---|---|---|---|
| TB | BP3 | BP2 | BP1 | BP0 | PROTECTED BLOCK(S) | PROTECTED ADDRESSES | PROTECTED DENSITY | PROTECTED PORTION |
| 0 | 0 | 0 | 0 | 0 | ALL | 00000000h - 03FFFFFFh | ALL | ALL |
| 0 | 0 | 0 | 0 | 1 | 0 thru 1022 | 00000000h - 03FEFFFFh | 65,472KB | Lower 1023/1024 |
| 0 | 0 | 0 | 1 | 0 | 0 thru 1021 | 00000000h - 03FDFFFFh | 65,408KB | Lower 511/512 |
| 0 | 0 | 0 | 1 | 1 | 0 thru 1019 | 00000000h - 03FBFFFFh | 65,280KB | Lower 255/256 |
| 0 | 0 | 1 | 0 | 0 | 0 thru 1015 | 00000000h - 03F7FFFFh | 65,024KB | Lower 127/128 |
| 0 | 0 | 1 | 0 | 1 | 0 thru 1007 | 00000000h - 03EFFFFFh | 63MB | Lower 63/64 |
| 0 | 0 | 1 | 1 | 0 | 0 thru 991 | 00000000h - 03DFFFFFh | 62MB | Lower 31/32 |
| 0 | 0 | 1 | 1 | 1 | 0 thru 959 | 00000000h - 03BFFFFFh | 60MB | Lower 15/16 |
| 0 | 1 | 0 | 0 | 0 | 0 thru 895 | 00000000h - 037FFFFFh | 56MB | Lower 7/8 |
| 0 | 1 | 0 | 0 | 1 | 0 thru 767 | 00000000h - 02FFFFFFh | 48MB | Lower 3/4 |
| 0 | 1 | 0 | 1 | 0 | 0 thru 511 | 00000000h - 01FFFFFFh | 32MB | Lower 1/2 |
| 0 | 1 | 0 | 1 | 1 | NONE | NONE | NONE | NONE |
| 0 | 1 | 1 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 1 | 1 | 0 | 1 | NONE | NONE | NONE | NONE |
| 0 | 1 | 1 | 1 | 0 | NONE | NONE | NONE | NONE |
| 0 | 1 | 1 | 1 | 1 | NONE | NONE | NONE | NONE |
| 1 | 0 | 0 | 0 | 0 | ALL | 00000000h - 03FFFFFFh | ALL | ALL |
| 1 | 0 | 0 | 0 | 1 | 1 thru 1023 | 00010000h - 03FFFFFFh | 65,472KB | Upper 1023/1024 |
| 1 | 0 | 0 | 1 | 0 | 2 thru 1023 | 00020000h - 03FFFFFFh | 65,408KB | Upper 511/512 |
| 1 | 0 | 0 | 1 | 1 | 4 thru 1023 | 00040000h - 03FFFFFFh | 65,280KB | Upper 255/256 |
| 1 | 0 | 1 | 0 | 0 | 8 thru 1023 | 00080000h - 03FFFFFFh | 65,024KB | Upper 127/128 |
| 1 | 0 | 1 | 0 | 1 | 16 thru 1023 | 00100000h - 03FFFFFFh | 63MB | Upper 63/64 |
| 1 | 0 | 1 | 1 | 0 | 32 thru 1023 | 00200000h - 03FFFFFFh | 62MB | Upper 31/32 |
| 1 | 0 | 1 | 1 | 1 | 64 thru 1023 | 00400000h - 03FFFFFFh | 60MB | Upper 15/16 |
| 1 | 1 | 0 | 0 | 0 | 128 thru 1023 | 00800000h - 03FFFFFFh | 56MB | Upper 7/8 |
| 1 | 1 | 0 | 0 | 1 | 256 thru 1023 | 01000000h - 03FFFFFFh | 48MB | Upper 3/4 |
| 1 | 1 | 0 | 1 | 0 | 512 thru 1023 | 02000000h - 03FFFFFFh | 32MB | Upper 1/2 |
| 1 | 1 | 0 | 1 | 1 | NONE | NONE | NONE | NONE |
| 1 | 1 | 1 | X | X | NONE | NONE | NONE | NONE |

**Notes:**
1. X = don't care
2. If any Erase or Program command specifies a memory region that contains a protected data portion, this command will be ignored.



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### 5.4.11 W25Q01RV Status Register Memory Protection (WPS = 0, CMP = 0)

| STATUS REGISTER[1] | | | | | W25Q01RV (1G-BIT / 128M-BYTE) MEMORY PROTECTION[2] | | | |
|---|---|---|---|---|---|---|---|---|
| TB | BP3 | BP2 | BP1 | BP0 | PROTECTED BLOCK(S) | PROTECTED ADDRESSES | PROTECTED DENSITY | PROTECTED PORTION |
| 0 | 0 | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 0 | 0 | 0 | 1 | 2047 | 07FF0000h - 07FFFFFFh | 64KB | Upper 1/2048 |
| 0 | 0 | 0 | 1 | 0 | 2046 thru 2047 | 07FE0000h - 07FFFFFFh | 128KB | Upper 1/1024 |
| 0 | 0 | 0 | 1 | 1 | 2044 thru 2047 | 07FC0000h - 07FFFFFFh | 256KB | Upper 1/512 |
| 0 | 0 | 1 | 0 | 0 | 2040 thru 2047 | 07F80000h - 07FFFFFFh | 512KB | Upper 1/256 |
| 0 | 0 | 1 | 0 | 1 | 2032 thru 2047 | 07F00000h - 07FFFFFFh | 1MB | Upper 1/128 |
| 0 | 0 | 1 | 1 | 0 | 2016 thru 2047 | 07E00000h - 07FFFFFFh | 2MB | Upper 1/64 |
| 0 | 0 | 1 | 1 | 1 | 1984 thru 2047 | 07C00000h - 07FFFFFFh | 4MB | Upper 1/32 |
| 0 | 1 | 0 | 0 | 0 | 1920 thru 2047 | 07800000h - 07FFFFFFh | 8MB | Upper 1/16 |
| 0 | 1 | 0 | 0 | 1 | 1792 thru 2047 | 07000000h - 07FFFFFFh | 16MB | Upper 1/8 |
| 0 | 1 | 0 | 1 | 0 | 1536 thru 2047 | 06000000h - 07FFFFFFh | 32MB | Upper 1/4 |
| 0 | 1 | 0 | 1 | 1 | 1024 thru 2047 | 04000000h - 07FFFFFFh | 64MB | Upper 1/2 |
| 0 | 1 | 1 | 0 | 0 | 0 thru 2047 | 00000000h - 07FFFFFFh | 128MB | ALL |
| 0 | 1 | 1 | 0 | 1 | 0 thru 2047 | 00000000h - 07FFFFFFh | 128MB | ALL |
| 0 | 1 | 1 | 1 | 0 | 0 thru 2047 | 00000000h - 07FFFFFFh | 128MB | ALL |
| 0 | 1 | 1 | 1 | 1 | 0 thru 2047 | 00000000h - 07FFFFFFh | 128MB | ALL |
| 1 | 0 | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 1 | 0 | 0 | 0 | 1 | 0 | 00000000h - 0000FFFFh | 64KB | Lower 1/2048 |
| 1 | 0 | 0 | 1 | 0 | 0 thru 1 | 00000000h - 0001FFFFh | 128KB | Lower 1/1024 |
| 1 | 0 | 0 | 1 | 1 | 0 thru 3 | 00000000h - 0003FFFFh | 256KB | Lower 1/512 |
| 1 | 0 | 1 | 0 | 0 | 0 thru 7 | 00000000h - 0007FFFFh | 512KB | Lower 1/256 |
| 1 | 0 | 1 | 0 | 1 | 0 thru 15 | 00000000h - 000FFFFFh | 1MB | Lower 1/128 |
| 1 | 0 | 1 | 1 | 0 | 0 thru 31 | 00000000h - 001FFFFFh | 2MB | Lower 1/64 |
| 1 | 0 | 1 | 1 | 1 | 0 thru 63 | 00000000h - 003FFFFFh | 4MB | Lower 1/32 |
| 1 | 1 | 0 | 0 | 0 | 0 thru 127 | 00000000h - 007FFFFFh | 8MB | Lower 1/16 |
| 1 | 1 | 0 | 0 | 1 | 0 thru 255 | 00000000h - 00FFFFFFh | 16MB | Lower 1/8 |
| 1 | 1 | 0 | 1 | 0 | 0 thru 511 | 00000000h - 01FFFFFFh | 32MB | Lower 1/4 |
| 1 | 1 | 0 | 1 | 1 | 0 thru 1023 | 00000000h - 03FFFFFFh | 64MB | Lower 1/2 |
| 1 | 1 | 1 | X | X | 0 thru 2047 | 00000000h - 07FFFFFFh | 128MB | ALL |

**Notes:**
1. X = don't care
2. If any Erase or Program command specifies a memory region that contains a protected data portion, this command will be ignored.



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### 5.4.12 W25Q01RV Status Register Memory Protection (WPS = 0, CMP = 1)

| STATUS REGISTER[1] | | | | | W25Q01RV (1G-BIT / 128M-BYTE) MEMORY PROTECTION[2] | | | |
|---|---|---|---|---|---|---|---|---|
| TB | BP3 | BP2 | BP1 | BP0 | PROTECTED BLOCK(S) | PROTECTED ADDRESSES | PROTECTED DENSITY | PROTECTED PORTION |
| 0 | 0 | 0 | 0 | 0 | ALL | 00000000h - 07FFFFFFh | ALL | ALL |
| 0 | 0 | 0 | 0 | 1 | 0 thru 2046 | 00000000h - 07FEFFFFh | 131,008KB | Lower 2047/2048 |
| 0 | 0 | 0 | 1 | 0 | 0 thru 2045 | 00000000h - 07FDFFFFh | 130,944KB | Lower 1023/1024 |
| 0 | 0 | 0 | 1 | 1 | 0 thru 2043 | 00000000h - 07FBFFFFh | 130,816KB | Lower 511/512 |
| 0 | 0 | 1 | 0 | 0 | 0 thru 2039 | 00000000h - 07F7FFFFh | 130,560KB | Lower 255/256 |
| 0 | 0 | 1 | 0 | 1 | 0 thru 2031 | 00000000h - 07EFFFFFh | 127MB | Lower 127/128 |
| 0 | 0 | 1 | 1 | 0 | 0 thru 2015 | 00000000h - 07DFFFFFh | 126MB | Lower 63/64 |
| 0 | 0 | 1 | 1 | 1 | 0 thru 1983 | 00000000h - 07BFFFFFh | 124MB | Lower 31/32 |
| 0 | 1 | 0 | 0 | 0 | 0 thru 1919 | 00000000h - 077FFFFFh | 120MB | Lower 15/16 |
| 0 | 1 | 0 | 0 | 1 | 0 thru 1791 | 00000000h - 06FFFFFFh | 112MB | Lower 7/8 |
| 0 | 1 | 0 | 1 | 0 | 0 thru 1535 | 00000000h - 05FFFFFFh | 96MB | Lower 3/4 |
| 0 | 1 | 0 | 1 | 1 | 0 thru 1023 | 00000000h - 03FFFFFFh | 64MB | Lower 1/2 |
| 0 | 1 | 1 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 1 | 1 | 0 | 1 | NONE | NONE | NONE | NONE |
| 0 | 1 | 1 | 1 | 0 | NONE | NONE | NONE | NONE |
| 0 | 1 | 1 | 1 | 1 | NONE | NONE | NONE | NONE |
| 1 | 0 | 0 | 0 | 0 | ALL | 00000000h - 07FFFFFFh | ALL | ALL |
| 1 | 0 | 0 | 0 | 1 | 1 thru 2047 | 00010000h - 07FFFFFFh | 131,008KB | Upper 2047/2048 |
| 1 | 0 | 0 | 1 | 0 | 2 thru 2047 | 00020000h - 07FFFFFFh | 130,944KB | Upper 1023/1024 |
| 1 | 0 | 0 | 1 | 1 | 4 thru 2047 | 00040000h - 07FFFFFFh | 130,816KB | Upper 511/512 |
| 1 | 0 | 1 | 0 | 0 | 8 thru 2047 | 00080000h - 07FFFFFFh | 130,560KB | Upper 255/256 |
| 1 | 0 | 1 | 0 | 1 | 16 thru 2047 | 00100000h - 07FFFFFFh | 127MB | Upper 127/128 |
| 1 | 0 | 1 | 1 | 0 | 32 thru 2047 | 00200000h - 07FFFFFFh | 126MB | Upper 63/64 |
| 1 | 0 | 1 | 1 | 1 | 64 thru 2047 | 00400000h - 07FFFFFFh | 124MB | Upper 31/32 |
| 1 | 1 | 0 | 0 | 0 | 128 thru 2047 | 00800000h - 07FFFFFFh | 120MB | Upper 15/16 |
| 1 | 1 | 0 | 0 | 1 | 256 thru 2047 | 01000000h - 07FFFFFFh | 112MB | Upper 7/8 |
| 1 | 1 | 0 | 1 | 0 | 512 thru 2047 | 02000000h - 07FFFFFFh | 96MB | Upper 3/4 |
| 1 | 1 | 0 | 1 | 1 | 1024 thru 2047 | 04000000h - 07FFFFFFh | 64MB | Upper 1/2 |
| 1 | 1 | 1 | X | X | NONE | NONE | NONE | NONE |

**Notes:**
1. X = don't care
2. If any Erase or Program command specifies a memory region that contains a protected data portion, this command will be ignored.



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### 5.4.13 W25Q02RV Status Register Memory Protection (WPS = 0, CMP = 0)

| STATUS REGISTER(1) | | | | | W25Q02RV (2G-BIT / 256M-BYTE) MEMORY PROTECTION(2) | | | |
|---|---|---|---|---|---|---|---|---|
| TB | BP3 | BP2 | BP1 | BP0 | PROTECTED BLOCK(S) | PROTECTED ADDRESSES | PROTECTED DENSITY | PROTECTED PORTION |
| 0 | 0 | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 0 | 0 | 0 | 1 | 4095 | 0FFF0000h – 0FFFFFFFh | 64KB | Upper 1/4096 |
| 0 | 0 | 0 | 1 | 0 | 4094 thru 4095 | 0FFE0000h – 0FFFFFFFh | 128KB | Upper 1/2048 |
| 0 | 0 | 0 | 1 | 1 | 4092 thru 4095 | 0FFC0000h – 0FFFFFFFh | 256KB | Upper 1/1024 |
| 0 | 0 | 1 | 0 | 0 | 4088 thru 4095 | 0FF80000h – 0FFFFFFFh | 512KB | Upper 1/512 |
| 0 | 0 | 1 | 0 | 1 | 4080 thru 4095 | 0FF00000h – 0FFFFFFFh | 1MB | Upper 1/256 |
| 0 | 0 | 1 | 1 | 0 | 4064 thru 4095 | 0FE00000h – 0FFFFFFFh | 2MB | Upper 1/128 |
| 0 | 0 | 1 | 1 | 1 | 4032 thru 4095 | 0FC00000h – 0FFFFFFFh | 4MB | Upper 1/64 |
| 0 | 1 | 0 | 0 | 0 | 3968 thru 4095 | 0F800000h – 0FFFFFFFh | 8MB | Upper 1/32 |
| 0 | 1 | 0 | 0 | 1 | 3840 thru 4095 | 0F000000h – 0FFFFFFFh | 16MB | Upper 1/16 |
| 0 | 1 | 0 | 1 | 0 | 3584 thru 4095 | 0E000000h – 0FFFFFFFh | 32MB | Upper 1/8 |
| 0 | 1 | 0 | 1 | 1 | 3072 thru 4095 | 0C000000h – 0FFFFFFFh | 64MB | Upper 1/4 |
| 0 | 1 | 1 | 0 | 0 | 2048 thru 4095 | 08000000h – 0FFFFFFFh | 128MB | Upper 1/2 |
| 0 | 1 | 1 | 0 | 1 | ALL | 00000000h – 0FFFFFFFh | ALL | ALL |
| 0 | 1 | 1 | 1 | 0 | ALL | 00000000h – 0FFFFFFFh | ALL | ALL |
| 0 | 1 | 1 | 1 | 1 | ALL | 00000000h – 0FFFFFFFh | ALL | ALL |
| 1 | 0 | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 1 | 0 | 0 | 0 | 1 | 0 | 00000000h - 0000FFFFh | 64KB | Lower 1/4096 |
| 1 | 0 | 0 | 1 | 0 | 0 thru 1 | 00000000h - 0001FFFFh | 128KB | Lower 1/2048 |
| 1 | 0 | 0 | 1 | 1 | 0 thru 3 | 00000000h - 0003FFFFh | 256KB | Lower 1/1024 |
| 1 | 0 | 1 | 0 | 0 | 0 thru 7 | 00000000h - 0007FFFFh | 512KB | Lower 1/512 |
| 1 | 0 | 1 | 0 | 1 | 0 thru 15 | 00000000h – 000FFFFFh | 1MB | Lower 1/256 |
| 1 | 0 | 1 | 1 | 0 | 0 thru 31 | 00000000h – 001FFFFFh | 2MB | Lower 1/128 |
| 1 | 0 | 1 | 1 | 1 | 0 thru 63 | 00000000h – 003FFFFFh | 4MB | Lower 1/64 |
| 1 | 1 | 0 | 0 | 0 | 0 thru 127 | 00000000h – 007FFFFFh | 8MB | Lower 1/32 |
| 1 | 1 | 0 | 0 | 1 | 0 thru 255 | 00000000h – 00FFFFFFh | 16MB | Lower 1/16 |
| 1 | 1 | 0 | 1 | 0 | 0 thru 511 | 00000000h – 01FFFFFFh | 32MB | Lower 1/8 |
| 1 | 1 | 0 | 1 | 1 | 0 thru 1023 | 00000000h – 03FFFFFFh | 64MB | Lower 1/4 |
| 1 | 1 | 1 | 0 | 0 | 0 thru 2047 | 00000000h – 07FFFFFFh | 128MB | Lower 1/2 |
| 1 | 1 | 1 | 0 | 1 | ALL | 00000000h – 0FFFFFFFh | ALL | ALL |
| 1 | 1 | 1 | 1 | X | ALL | 00000000h – 0FFFFFFFh | ALL | ALL |

**Notes:**
1. X = don't care
2. If any Erase or Program command specifies a memory region that contains a protected data portion, this command will be ignored.



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### 5.4.14 W25Q02RV Status Register Memory Protection (WPS = 0, CMP = 1)

| STATUS REGISTER | | | | | W25Q02RV (2G-BIT / 256M-BYTE) MEMORY PROTECTION(1) | | | |
|---|---|---|---|---|---|---|---|---|
| TB | BP3 | BP2 | BP1 | BP0 | PROTECTED BLOCK(S) | PROTECTED ADDRESSES | PROTECTED DENSITY | PROTECTED PORTION |
| 0 | 0 | 0 | 0 | 0 | ALL | 00000000h – 0FFFFFFFh | ALL | ALL |
| 0 | 0 | 0 | 0 | 1 | 0 thru 4094 | 00000000h – 0FFEFFFFh | 262,080KB | Lower 4095/4096 |
| 0 | 0 | 0 | 1 | 0 | 0 thru 4093 | 00000000h – 0FFDFFFFh | 262,016KB | Lower 2047/2048 |
| 0 | 0 | 0 | 1 | 1 | 0 thru 4091 | 00000000h – 0FFBFFFFh | 261,888KB | Lower 1023/1024 |
| 0 | 0 | 1 | 0 | 0 | 0 thru 4087 | 00000000h – 0FF7FFFFh | 261.632KB | Lower 511/512 |
| 0 | 0 | 1 | 0 | 1 | 0 thru 4079 | 00000000h – 0FEFFFFFh | 255MB | Lower 255/256 |
| 0 | 0 | 1 | 1 | 0 | 0 thru 4063 | 00000000h – 0FDFFFFFh | 254MB | Lower 127/128 |
| 0 | 0 | 1 | 1 | 1 | 0 thru 4031 | 00000000h – 0FBFFFFFh | 252MB | Lower 63/64 |
| 0 | 1 | 0 | 0 | 0 | 0 thru 3967 | 00000000h – 0F7FFFFFh | 248MB | Lower 31/32 |
| 0 | 1 | 0 | 0 | 1 | 0 thru 3839 | 00000000h – 0EFFFFFFh | 240MB | Lower 15/16 |
| 0 | 1 | 0 | 1 | 0 | 0 thru 3583 | 00000000h – 0DFFFFFFh | 224MB | Lower 7/8 |
| 0 | 1 | 0 | 1 | 1 | 0 thru 3071 | 00000000h – 0BFFFFFFh | 192MB | Lower 3/4 |
| 0 | 1 | 1 | 0 | 0 | 0 thru 2047 | 00000000h – 07FFFFFFh | 128MB | Lower 1/2 |
| 0 | 1 | 1 | 0 | 1 | NONE | NONE | NONE | NONE |
| 0 | 1 | 1 | 1 | 0 | NONE | NONE | NONE | NONE |
| 0 | 1 | 1 | 1 | 1 | NONE | NONE | NONE | NONE |
| 1 | 0 | 0 | 0 | 0 | ALL | 00000000h – 0FFFFFFFh | ALL | ALL |
| 1 | 0 | 0 | 0 | 1 | 1 thru 4095 | 00010000h – 0FFFFFFFh | 262,080KB | Upper 4095/4096 |
| 1 | 0 | 0 | 1 | 0 | 2 thru 4095 | 00020000h – 0FFFFFFFh | 262,016KB | Upper 2047/2048 |
| 1 | 0 | 0 | 1 | 1 | 4 thru 4095 | 00040000h – 0FFFFFFFh | 261,888KB | Upper 1023/1024 |
| 1 | 0 | 1 | 0 | 0 | 8 thru 4095 | 00080000h – 0FFFFFFFh | 261.632KB | Upper 511/512 |
| 1 | 0 | 1 | 0 | 1 | 16 thru 4095 | 00100000h – 0FFFFFFFh | 255MB | Upper 255/256 |
| 1 | 0 | 1 | 1 | 0 | 32 thru 4095 | 00200000h – 0FFFFFFFh | 254MB | Upper 127/128 |
| 1 | 0 | 1 | 1 | 1 | 64 thru 4095 | 00400000h – 0FFFFFFFh | 252MB | Upper 63/64 |
| 1 | 1 | 0 | 0 | 0 | 128 thru 4095 | 00800000h – 0FFFFFFFh | 248MB | Upper 31/32 |
| 1 | 1 | 0 | 0 | 1 | 256 thru 4095 | 01000000h – 0FFFFFFFh | 240MB | Upper 15/16 |
| 1 | 1 | 0 | 1 | 0 | 512 thru 4095 | 02000000h – 0FFFFFFFh | 224MB | Upper 7/8 |
| 1 | 1 | 0 | 1 | 1 | 1024 thru 4095 | 04000000h – 0FFFFFFFh | 192MB | Upper 3/4 |
| 1 | 1 | 1 | 0 | 0 | 2048 thru 4095 | 08000000h – 0FFFFFFFh | 128MB | Upper 1/2 |
| 1 | 1 | 1 | 0 | 1 | NONE | NONE | NONE | NONE |
| 1 | 1 | 1 | 1 | X | NONE | NONE | NONE | NONE |

**Notes:**
1. X = don't care
2. If any Erase or Program command specifies a memory region that contains a protected data portion, this command will be ignored.



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## 5.5 Flex Block Memory Protection (WPS=1)

### 5.5.1 W25Q33RV,64RV,12RV Flex Block Memory Protection (WPS=1)

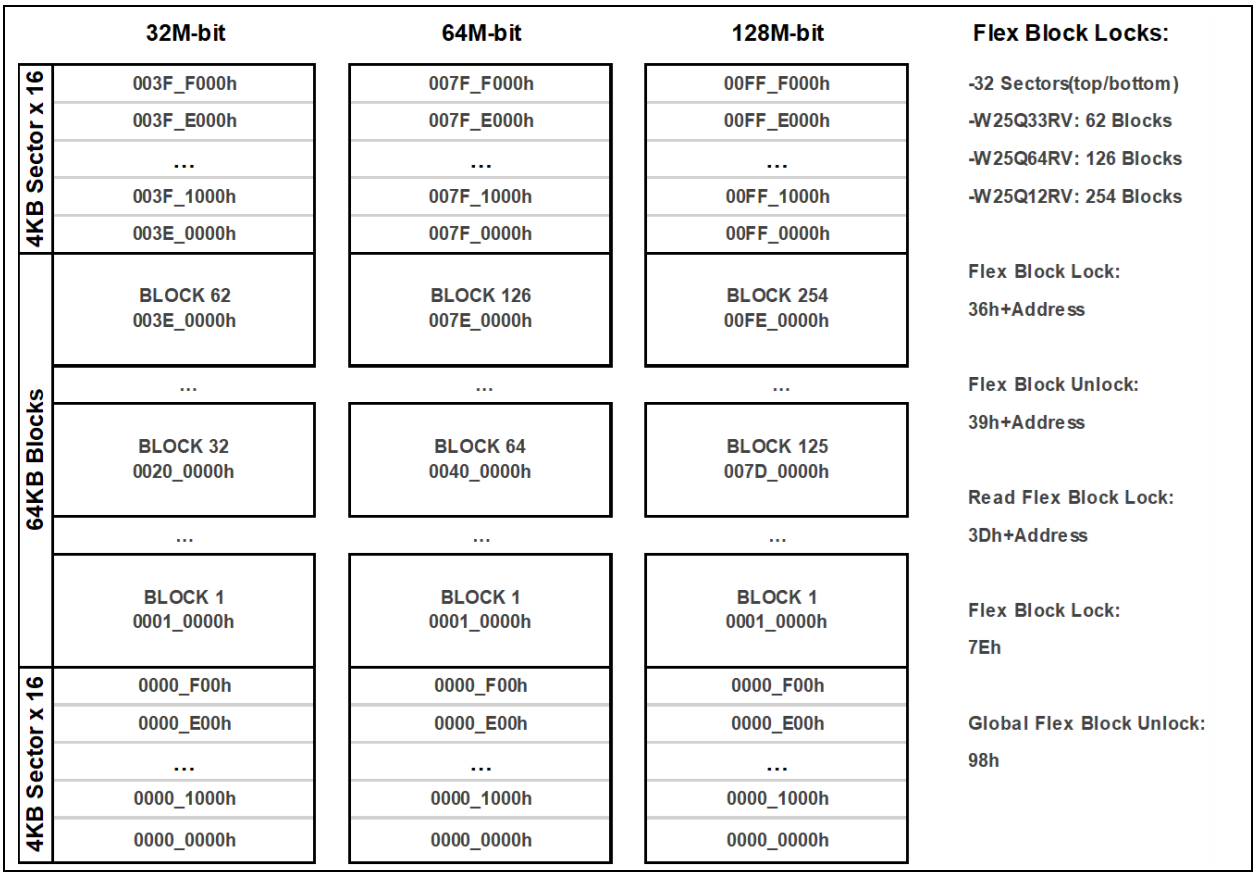



Figure 5.6.1. W25Q33RV,64RV,12RV Flex Block/Sector Locks

**Notes:**

1. Flex Block/Sector protection is only valid when WPS=1.
2. All Flex Block/Sector lock bits are set to 1 by default after power up, all memory array is protected.
3. When WPS = 1, the CMP, TB, and BP[3:0] settings are effective.



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### 5.5.2 W25Q25RV,51RV Flex Block Memory Protection (WPS=1)

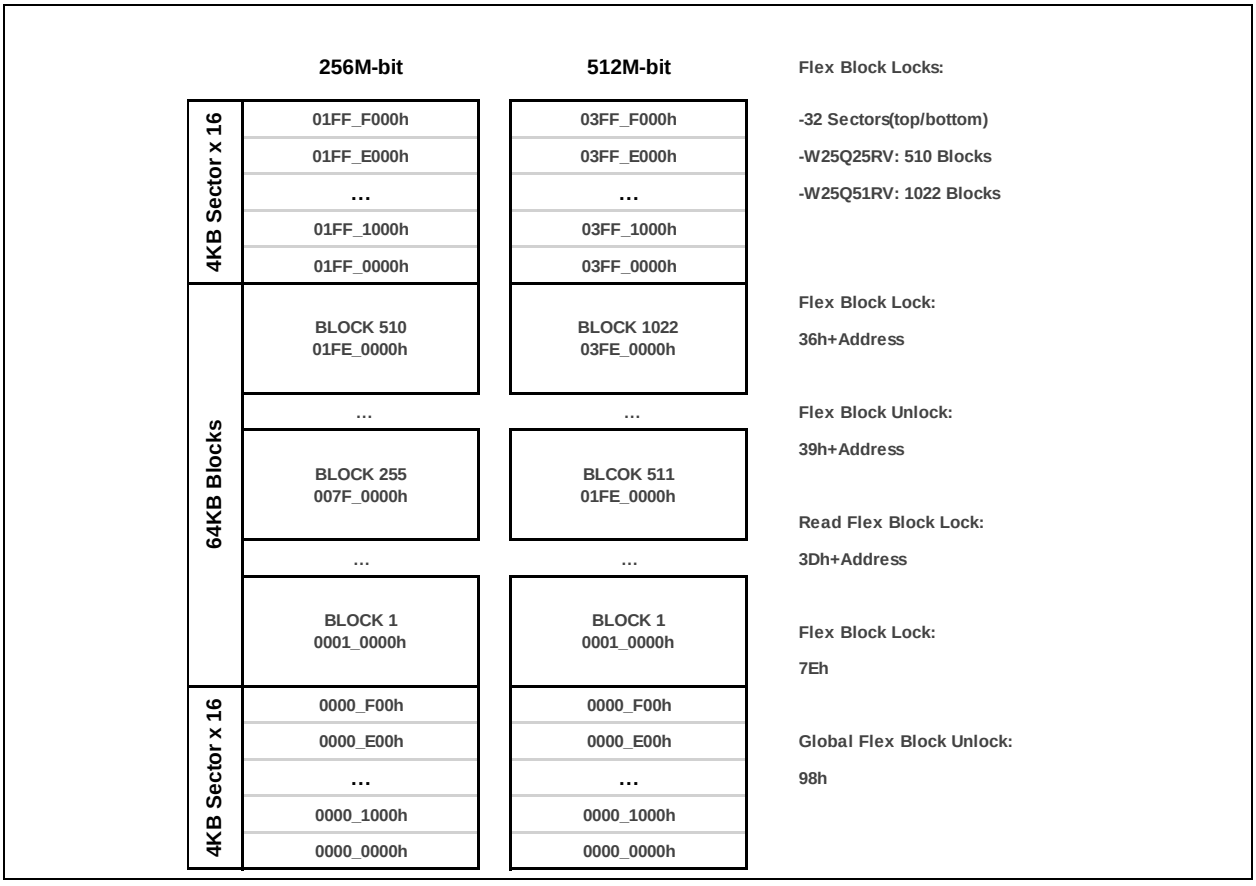



Figure 5.5.2. W25Q25RV, 51RV Flex Block/Sector Locks

**Notes:**

1. Flex Block/Sector protection is only valid when WPS=1.
2. All Flex Block/Sector lock bits are set to 1 by default after power up, all memory array is protected.
3. When WPS = 1, the CMP, TB, and BP[3:0] settings are effective.



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### 5.5.3 W25Q01RV Flex Block Memory Protection (WPS=1)

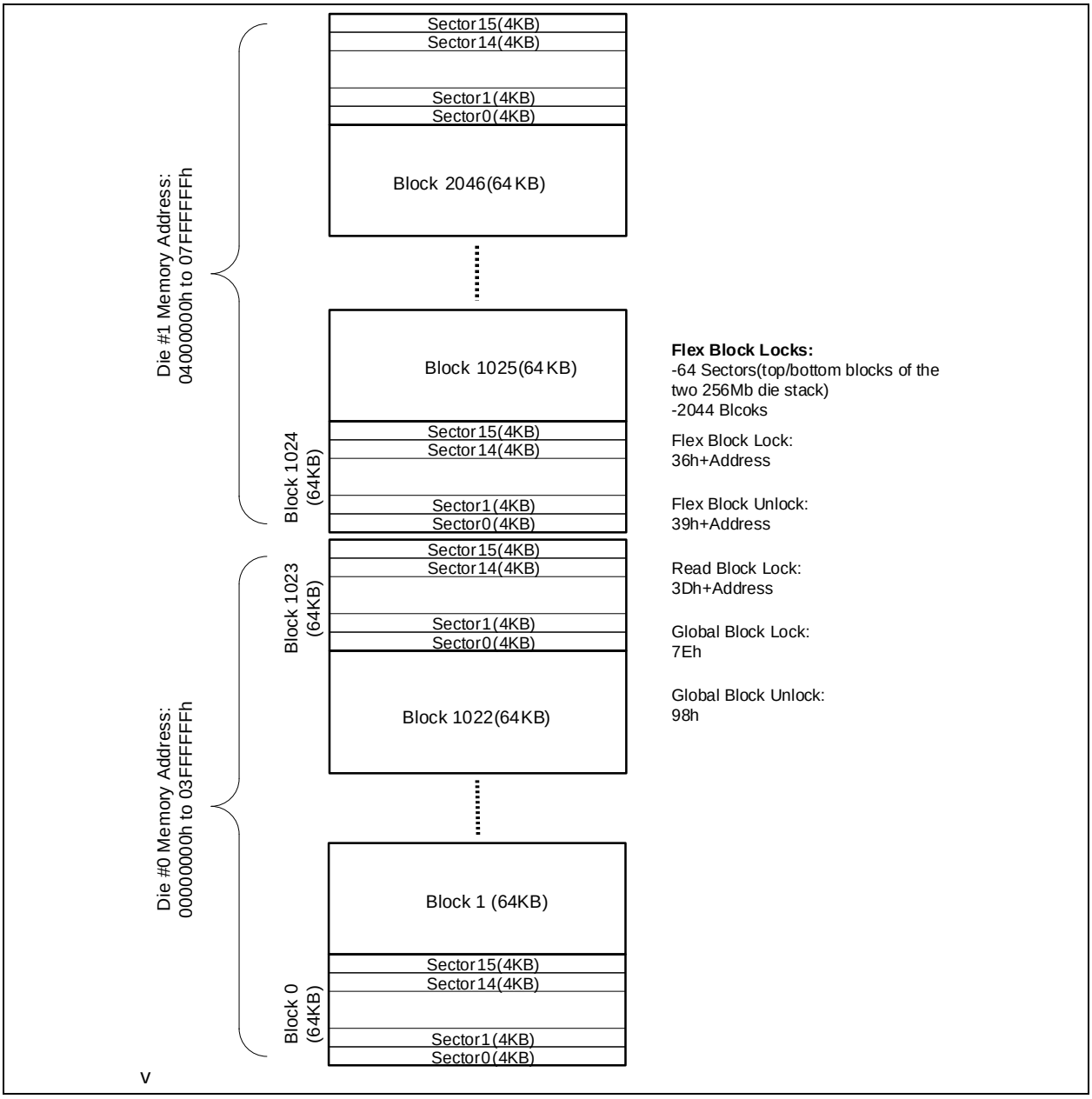



Figure 5.5.3.W25Q01RV Flex Block/Sector Locks

**Notes:**

1. Flex Block/Sector protection is only valid when WPS=1.
2. All Flex Block/Sector lock bits are set to 1 by default after power up, all memory array is protected.
3. When WPS = 1, the CMP, TB, and BP[3:0] settings are effective.



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### 5.5.4 W25Q02RV Flex Block Memory Protection (WPS=1)

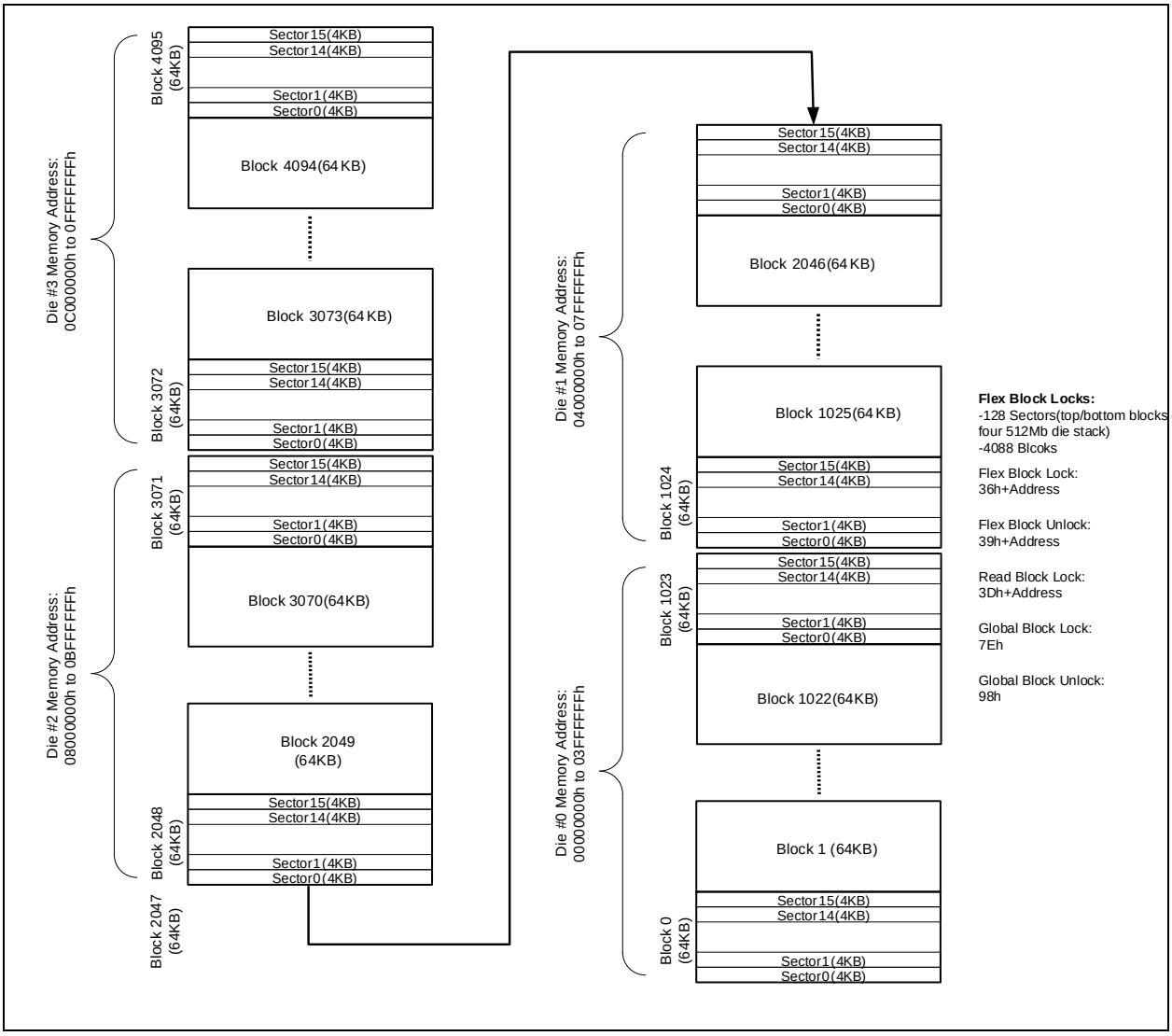



Figure 5.5.4.W25Q02RV. Flex Block/Sector Locks

**Notes**:

1. Flex Block/Sector protection is only valid when WPS=1.
2. All Flex Block/Sector lock bits are set to 1 by default after power up, all memory array is protected.
3. When WPS = 1, the CMP, TB, and BP[3:0] settings are effective.



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## 5.6 Extended Address Register – Volatile Writable Only

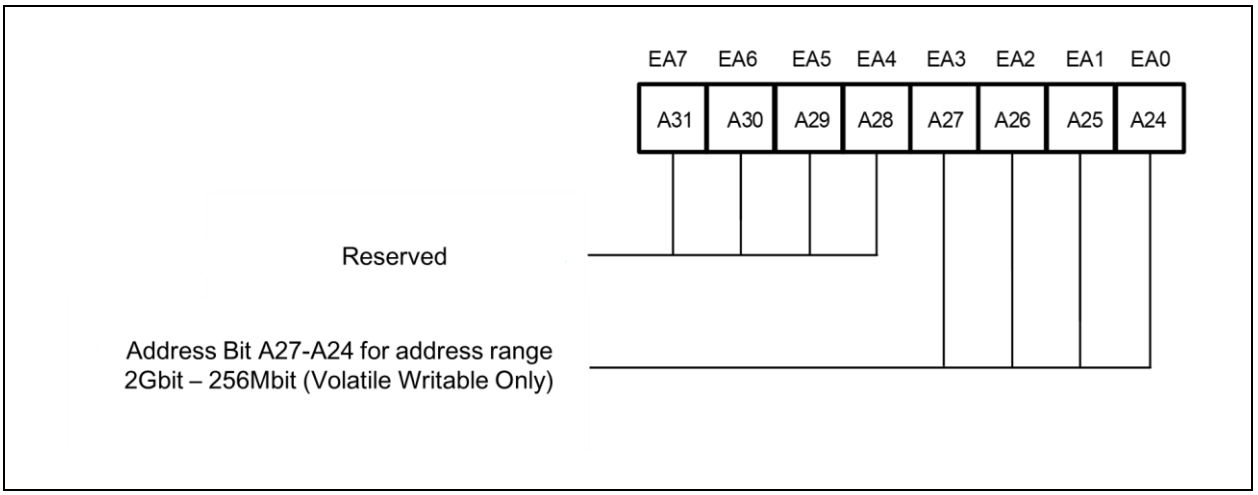



Figure 5.6. Extended Address Register

In addition to the Status Registers, the W25QxxRV provide a volatile Extended Address Register which consists of the 4th byte of memory address. The Extended Address Register is accessible by the Read Extended Address Register (C8h) and Write Extended Address Register (C5h) instructions. The Extended Address Register is used only when the device is operating in the 3-Byte Address Mode (ADS=0). The separate 128Mb memory array ranges are accessible depending on the setting of the Extended Address Register A27, A26, A25 and A24 bits as shown on the table below.



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**Memory Array range**

| | | | |
|---|---|---|---|
| 0FFFFFFFh<br>0F000000h | <A27-A24> = 1111 | 07FFFFFFh<br>07000000h | <A27-A24> = 0111 |
| 0EFFFFFFh<br>0E000000h | <A27-A24> = 1110 | 06FFFFFFh<br>06000000h | <A27-A24> = 0110 |
| 0DFFFFFFh<br>0D000000h | <A27-A24> = 1101 | 05FFFFFFh<br>05000000h | <A27-A24> = 0101 |
| 0CFFFFFFh<br>0C000000h | <A27-A24> = 1100 | 04FFFFFFh<br>04000000h | <A27-A24> = 0100 |
| 0BFFFFFFh<br>0B000000h | <A27-A24> = 1011 | 03FFFFFFh<br>03000000h | <A27-A24> = 0011 |
| 0AFFFFFFh<br>0A000000h | <A27-A24> = 1010 | 02FFFFFFh<br>02000000h | <A27-A24> = 0010 |
| 09FFFFFFh<br>09000000h | <A27-A24> = 1001 | 01FFFFFFh<br>01000000h | <A27-A24> = 0001 |
| 08FFFFFFh<br>08000000h | <A27-A24> = 1000 | 00FFFFFFh<br>00000000h | <A27-A24> = 0000 |

Any command with a dedicated 4-byte address input will use the 4th Address Byte (A31-A24) input and not the Extended Address Register. If the device powers up with ADP bit set to 1, or an “Enter 4-Byte Address Mode (B7h)” instruction is issued, the device will require 4-Byte address input for all address related instructions, and the Extended Address Register setting will be ignored. The 4th Byte Address input will not alter the content of Extended Address Register.

Upon power up, hardware reset, or after the execution of a Software Reset, the Extended Address Register values will be cleared to 0.



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## 5.7 Page Buffer

In Standard SPI mode, one of the new powerful features of the W25QxxRV is the integrated Serial SRAM buffer and its associated Program Buffer. Together, the 256-byte Serial SRAM provides usable SRAM storage. The SRAM can be used in conjunction with the Flash memory or independently. The main purpose of the Serial SRAM is to serve as the primary buffer for data to be written into the Serial Flash memory array. In case of need, it can help to transform random Byte Write to page Program Buffer.

Using the Write Buffer instruction, data is first shifted into the SRAM from the SPI bus. When the instruction sequence has been completed, the entire 256-bytes is transferred to the Program Buffer. The Program Buffer supports the array during the Erase/Write cycle (tWP), freeing the SRAM to accept new data. This double-buffering scheme increases erase/write transfer rates and can eliminate the need for external RAM buffers (Figure 5.7). The SRAM is fully byte addressable. Thus, the entire 256-bytes, a single byte, or a sequence of bytes can be read from or written to the SRAM. This allows the SRAM to be used as a temporary work area for read-modify-write operations prior to a sector write.

The Transfer Sector to SRAM instruction allows the contents of a specified sector of Flash memory to be moved to the SRAM. This can be useful when only a portion of a sector needs to be altered. In this case the sector is first transferred to the SRAM, where modifications are made using the Write to SRAM instruction. Once complete, a Transfer SRAM to Sector instruction is used to update the sector.

Page Buffer control instruction as below:

- Clear Buffer(81h): Reset all the bit in the Page Buffer becomes '1'.
- Write Buffer(82h): Write the data into the Page Buffer, from the 1st byte to the 256th byte.
- Read Buffer(83h): Read out the data from Page Buffer.
- Program Buffer(8Ah): Write the Page Buffer data into the specified Flash Physical memory page.
- Load Buffer(8Bh): Read the data from the specified Flash Physical memory page into the Page Buffer.

Upon power off or the execution of a reset, all bits in the Page Buffer become '1', effectively clearing the buffer. After Release Power-down (ABh), a clear buffer command must be issued."

For details, please refer to the application note on "AN0000078 Winbond SPI NOR Flash Page Buffer Operation"

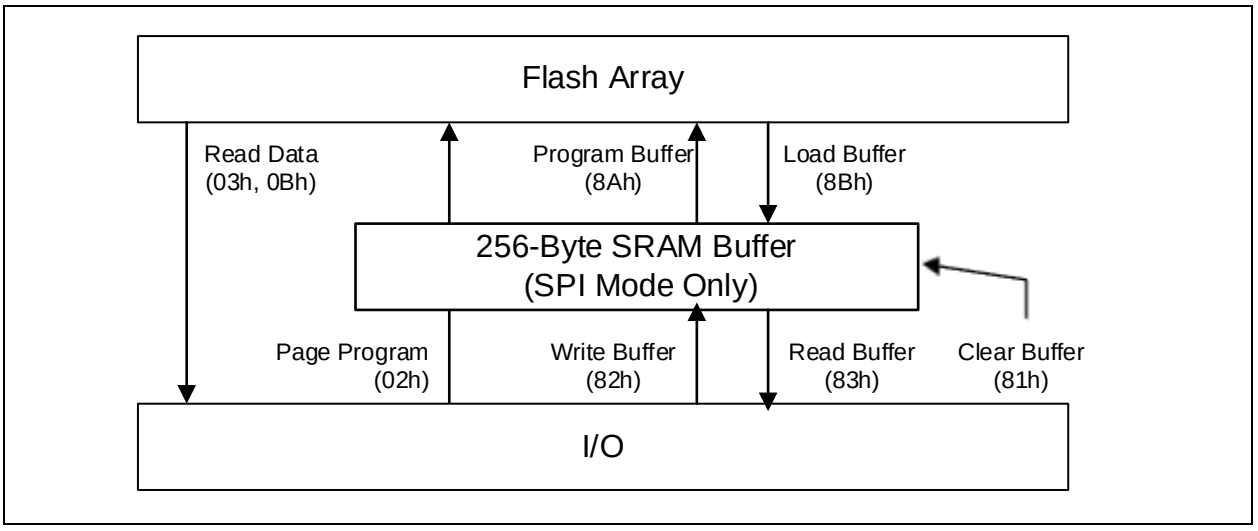



Figure 5.7. Serial Flash Buffer Mode



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# 6 INSTRUCTIONS

The Standard/Dual/Quad SPI instruction set of the W25QxxRV consists basic instructions that are fully controlled through the SPI bus. Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with the most significant bit (MSB) first.

The QPI instruction set of the W25QxxRV consists basic instructions that are fully controlled through the SPI bus. Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked through IO[3:0] pins provide the instruction code. Data on all four IO pins are sampled on the rising edge of clock with the most significant bit (MSB) first. All QPI instructions, addresses, data and dummy bytes use all four IO pins to transfer every byte of data with every two serial clocks (CLK).

For SPI/QPI DTR Read instructions, the address input is sampled on both the rising and falling edges of the clock; the data output is also ready on both edges of the clock

**Instruction Set Number table:**

| Instruction Set | 3 and 4-Byte Address Mode (ADS=0 & 1) | 3-Byte or 4 Address Mode (ADS=0 or 4) | Part Number Suffix(2) |
|---|---|---|---|
| Standard/Dual/Quad | 1, 2, 3 | 4, 5 | -Q, -N, -M |
| QPI | 6, 7 | 8-10 | -Q, -N, -M |
| SPI DTR/QPI DTR(1) | 12, 15 | 11, 13, 14 | -M |

**Notes:**
1. The SPI DTR and QPI DTR instructions are only supported with Part Number Suffix “M”
2. Please see the link to “”

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don’t care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in each chapter. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.



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## 6.1 Device ID and Instruction Set Tables

### Manufacturer and Device Identification

| | | | |
|---|---|---|---|
| **MANUFACTURER ID** | **(MF7 - MF0)** | | |
| Winbond Serial Flash | EFh | | |
| | | | |
| **Device ID** | **(ID7 - ID0)** | **(ID15 - ID0)** | |
| **Instruction** | **ABh, 90h, 92h, 94h** | **9Fh** | |
| **Part Number and Suffix** | | **-M** | **-Q, -N** |
| W25Q33RV | 15h | 7016h | 4016h |
| W25Q64RV | 16h | 7017h | 4017h |
| W25Q12RV | 17h | 7018h | 4018h |
| W25Q25RV | 18h | 7019h | 4019h |
| W25Q51RV | 19h | 7020h | 4020h |
| W25Q01RV | 20h | 7021h | 4021h |
| W25Q02RV | 21h | 7022h | 4022h |



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## 6.2 W25Q33RV/64RV/12RV Command Table with Maximum Clock Frequencies (MHz)(1)

### 6.2.1 SPI Commands Operable in Both 3-Byte and 4-Byte Address Modes

| Command-- *W25Q33RV/64RV/12RV* | Opcode | Address Bytes | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|
| Number of Clock (IO 1-1-1) | 8 | 8-8-8 | N dummy | 8 - 8… | MHz | MHz |
| Write Enable | 06h | -- | -- | -- | 166 | 166 |
| Volatile Status Register Write Enable | 50h | -- | -- | -- | 166 | 166 |
| Write Disable | 04h | -- | -- | -- | 166 | 166 |
| Release Power-down / ID | ABh | -- | 24 | ID7-ID0 | 166 | 166 |
| Read Manufacturer/Device ID | 90h | 00h,00h,00h | -- | (MF7-0) - (ID7-ID0) | 166 | 166 |
| Read JEDEC ID | 9Fh | -- | -- | (MF7-0) - (ID15-8) - (ID7-0) | 166 | 166 |
| Set Read Parameters | C0h | -- | -- | P7-P0 | 166 | 166 |
| Chip Erase | C7h/60h | -- | -- | -- | 166 | 166 |
| Read Status Register-1 | 05h | -- | -- | (S7-S0) | 166 | 166 |
| Write Status Register-1 | 01h | -- | -- | S7-S0 | 166 | 166 |
| Read Status Register-2 | 35h | -- | -- | (S15-S8) | 166 | 166 |
| Write Status Register-2 | 31h | -- | -- | S15-S8 | 166 | 166 |
| Read Status Register-3 | 15h | -- | -- | (S23-S16) | 166 | 166 |
| Write Status Register-3 | 11h | -- | -- | S23-S16 | 166 | 166 |
| Read SFDP Register | 5Ah | A23-A0 | 8 | (D7-D0) | 133 | 104 |
| Global Block Lock | 7Eh | -- | -- | -- | 166 | 166 |
| Global Block Unlock | 98h | -- | -- | -- | 166 | 166 |
| Erase / Program Suspend | 75h | -- | -- | -- | 166 | 166 |
| Erase / Program Resume | 7Ah | -- | -- | -- | 166 | 166 |
| Power-down | B9h | -- | -- | -- | 166 | 166 |
| Enter 4-Byte Address Mode | B7h | -- | -- | -- | 166 | 166 |
| Exit 4-Byte Address Mode | E9h | -- | -- | -- | 166 | 166 |
| Enter QPI Mode | 38h | -- | -- | -- | 166 | 166 |
| Enable Reset | 66h | -- | -- | -- | 166 | 166 |
| Reset Device | 99h | -- | -- | -- | 166 | 166 |
| Set Burst with Wrap | 77h | | 24 | | 166 | 166 |
| Recovery for Erase | A8h | -- | -- | -- | 166 | 166 |


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### 6.2.2 SPI Commands Operable in Both 3-Byte and 4-Byte Address Modes

| Command-*W25Q33RV/64RV/12RV* | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|
| Number of Clock (IO 1-1-1) | 8 | 8-8-8-8 | M7-0 | N dummy | 8 - 8… | MHz | MHz |
| Read Data with 4-Byte Addr | 13h | A31-A0 | -- | -- | (D7-D0) | 84 | 66 |
| Fast Read with 4-Byte Addr | 0Ch | A31-A0 | -- | 8 | (D7-D0) | 133 | 104 |
| Page Program with 4-Byte Addr | 12h | A31-A0 | -- | -- | (D7-D0) | 166 | 166 |
| 4KB Sector Erase with 4-Byte Addr | 21h | A31-A0 | -- | -- | -- | 166 | 166 |
| 64KB Block Erase with 4-Byte Addr | DCh | A31-A0 | -- | -- | -- | 166 | 166 |
| Read Extended Address Register | C8h | -- | -- | -- | (EA7-0) | 166 | 166 |
| Write Extended Address Register | C5h | -- | -- | -- | EA7-0 | 166 | 166 |

| Command-*W25Q33RV/64RV/12RV* | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|
| Number of Clock (IO 1-1-1) | 8 | --- | M7-0 | N dummy | 8 - 8… | MHz | MHz |
| Enter Factory Mode OP-1 | 51h | -- | -- | -- | -- | 166 | 166 |
| Enter Factory Mode OP-2 | A5h | -- | -- | -- | -- | 166 | 166 |
| Enter Factory Mode OP-3 | 41h | -- | -- | -- | -- | 166 | 166 |


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### 6.2.3 SPI Commands Operable in Both 3-Byte and 4-Byte Address Modes

| Command *W25Q33RV/64RV/12RV* | | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|---|
| Number of Clock (IO 1-1-2) | | 8 | 8-8-8-8 | M7-0 | N dummy | 4 - … Clock | MHz | MHz |
| Fast Read Dual Output | | 3Ch | A31-A0 | -- | 8 | (D7-D0)… | 133 | 104 |
| Number of Clock (1-1-4) | | 8 | 8-8-8-8 | M7-0 | N dummy | 2-…Clock | MHz | MHz |
| Quad Input Page Program | | 34h | A31-A0 | | -- | D7-D0... | 166 | 166 |
| Fast Read Quad Output | | 6Ch | A31-A0 | -- | 8 | (D7-D0) | 133 | 104 |
| Number of Clock (1-2-2) | | 8 | 4-4-4-4 | M7-0 | N dummy | 4-…Clock | MHz | MHz |
| Fast Read Dual I/O | | BCh | A31-A0, | 4 | 4 | (D7-D0) | 133 | 104 |
| Number of Clock (1-4-4) | | 8 | 2-2-2-2 | M7-0 | N dummy | 2-… Clock | MHz | MHz |
| Fast Read Quad I/O | | ECh | A31-A0 | 2 | 4 | (D7-D0) | 133 | 104 |
| Set Read Parameters (C0h) M7–0 serve as dummy bits | 0 0 0 | | A31-A0 | Disable | 6 (Def) | (D7-0)… | 133 | 104 |
| | 0 0 1 | | A31-A0 | Disable | 6 | (D7-0)… | 133 | 104 |
| | 0 1 0 | | A31-A0 | Disable | 6 | (D7-0)… | 133 | 104 |
| | 0 1 1 | | A31-A0 | Disable | 8 | (D7-0)… | 133 | 104 |
| | 1 0 0 | | A31-A0 | Disable | 10 | (D7-0)… | 133 | 104 |
| | 1 0 1 | | A31-A0 | Disable | 12 | (D7-0)… | 166 | 133 |
| | 1 1 0 | | A31-A0 | Disable | 14 | (D7-0)… | 166 | 133 |
| | 1 1 1 | | A31-A0 | Disable | 16 | (D7-0)… | 166 | 133 |


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### 6.2.4 SPI Commands Dependent in 3‐Byte / 4‐Byte Address Mode (ADS=1: A31–A0, ADS=0: A23–A0)

| Command *W25Q33RV/64RV/12RV* | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|
| Number of Clock (IO 1-1-1) | 8 | 8 / 8-8-8 | M7-0 | N dummy | 8-… Clock | MHz | MHz |
| Read Unique ID | 4Bh | -- | | 40 / 32 | (D7-D0)… | 133 | 104 |
| Read Data | 03h | A31 / A23-A0 | | -- | (D7-D0).. | 84 | 66 |
| Fast Read | 0Bh | A31 / A23-A0 | | 8 | (D7-D0)… | 133 | 104 |
| Page Program | 02h | A31 / A23-A0 | | -- | D7-D0… | 166 | 166 |
| 4KB Sector Erase | 20h | A31 / A23-A0 | | -- | -- | 166 | 166 |
| 32KB Block Erase | 52h | A31 / A23-A0 | | -- | -- | 166 | 166 |
| 64KB Block Erase | D8h | A31 / A23-A0 | | -- | -- | 166 | 166 |
| Erase Security Register(5) | 44h | A31 / A23-A0 | | -- | -- | 166 | 166 |
| Program Security Register(5) | 42h | A31 / A23-A0 | | -- | D7-D0… | 166 | 166 |
| Read Security Register(5) | 48h | A31 / A23-A0 | | 8 | (D7-D0)… | 133 | 104 |
| Read Flex Block Lock | 3Dh | A31 / A23-A0 | | -- | (L7-L0)… | 133 | 104 |
| Flex Block Lock | 36h | A31 / A23-A0 | | -- | -- | 166 | 166 |
| Flex Block Unlock | 39h | A31 / A23-A0 | | -- | -- | 166 | 166 |

| Command *W25Q33RV/64RV/12RV* | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|
| Number of Clock (IO 1-1-1) | 8 | 8 / 8-8-8 | M7-0 | N dummy/ Clock | 8 - 8… | MHz | MHz |
| Clear Buffer | 81h(14) | BA31 / BA23-BA0 | -- | -- | -- | 166 | 166 |
| Write Buffer | 82h(14) | BA31 / BA23-BA0 | -- | -- | (D7-D0) | 166 | 166 |
| Read Buffer | 83h(14) | BA31 / BA23-BA0 | -- | 8 | (D7-D0) | 166 | 166 |
| Program Buffer | 8Ah | A31 / A23-A0 | -- | -- | -- | 166 | 166 |
| Load Buffer | 8Bh | A31 / A23-A0 | -- | -- | -- | 166 | 166 |


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### 6.2.5 SPI Commands Dependent in 3-Byte / 4-Byte Address Mode (ADS=1: A31–A0, ADS=0: A23–A0)

| Command *W25Q33RV/64RV/12RV* | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|
| Number of Clock (IO 1-1-1) | 8 | 8 / 8-8-8 | M7-M0 | N dummy | 8-8-8-8,… | MHz | MHz |
| Read checksum | 9Ch | A31 / A23-A0 | -- | 8 | D(7-0,15-8,23-16,31-24),… | 133 | 104 |
| Command | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
| Number of Clock (IO 1-1-1) | 8 | 8 / 8-8-8,8-8-8 | | N dummy | 8-8-8-8 | MHz | MHz |
| Calculate checksum | 9Dh | SA31/SA23-0, EA31-EA0 | | -- | -- | 166 | 166 |

| Command *W25Q33RV/64RV/12RV* | | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|---|
| Number of Clock (IO 1-1-2) | | 8 | 8 / 8-8-8 | M7-M0 | N dummy | 4-… | MHz | MHz |
| Fast Read Dual Output | | 3Bh | A31 / A23-A0 | -- | 8 | (D7-0)… | 133 | 104 |
| Number of Clock (IO 1-1-4) | | 8 | 8 / 8-8-8 | M7-M0 | N dummy | 2-… | MHz | MHz |
| Quad Input Page Program | | 32h | A31 / A23-A0 | -- | -- | D7-0… | 166 | 166 |
| Fast Read Quad Output | | 6Bh | A31 / A23-A0 | -- | 8 | (D7-0)… | 133 | 104 |
| Number of Clock (IO 1-2-2) | | | 4 / 4-4-4 | M7-M0 | N dummy | 4-… | MHz | MHz |
| Mftr./Device ID Dual I/O | | 92h | A31 / A23-8,00h | 4-N/Allow | -- | (MF7-0, ID7-ID0) | 133 | 104 |
| Fast Read Dual I/O | | BBh | A31 / A23-A0 | 4 | -- | (D7-0) | 133 | 104 |
| Number of Clock (IO 1-4-4) | | | 2 / 2-2-2-2-2 | 2 | N dummy | 2-… Clock | MHz | MHz |
| Mftr./Device ID Quad I/O | | 94h | A31 / A23-8,00h | 2-N/Allow | 4 | (MF7-0, ID7-ID0) | 133 | 104 |
| Fast Read Quad I/O | | EBh | A31 / A23-A0 | 2 | 4 | (D7-0)… | 133 | 104 |
| Set Read Parameters (C0h) M7–0 serve as dummy bits | 0 0 0 | | A31 / A23-A0 | Disable | 6(Def.) | (D7-0)… | 133 | 104 |
| | 0 0 1 | | A31 / A23-A0 | Disable | 6 | (D7-0)… | 133 | 104 |
| | 0 1 0 | | A31 / A23-A0 | Disable | 6 | (D7-0)… | 133 | 104 |
| | 0 1 1 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 133 | 104 |
| | 1 0 0 | | A31 / A23-A0 | Disable | 10 | (D7-0)… | 133 | 104 |
| | 1 0 1 | | A31 / A23-A0 | Disable | 12 | (D7-0)… | 166 | 133 |
| | 1 1 0 | | A31 / A23-A0 | Disable | 14 | (D7-0)… | 166 | 133 |
| | 1 1 1 | | A31 / A23-A0 | Disable | 16 | (D7-0)… | 166 | 133 |


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### 6.2.6 QPI Commands Operable in Both 3-Byte and 4-Byte Address Modes

| Command *W25Q33RV/64RV/12RV* | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|
| Number of Clock (IO 4-4-4) | 2 | 2-2-2 | M7-M0 | N dummy | 2-2… | MHz | MHz |
| Write Enable | 06h | -- | -- | -- | -- | 166 | 166 |
| Volatile Status Register Write Enable | 50h | -- | -- | -- | -- | 166 | 166 |
| Write Disable | 04h | -- | -- | -- | -- | 166 | 166 |
| Release Power-down / ID | ABh | -- | -- | 6 | (ID7-ID0) | 166 | 166 |
| Read Manufacturer/Device ID | 90h | -- | -- | 4 Dummy + 00h | (MF7-0, ID7-ID0) | 166 | 166 |
| Read JEDEC ID | 9Fh | -- | -- | -- | (MF7-0) - (ID15-8) - (ID7-0) | 166 | 166 |
| Set Read Parameters | C0h | -- | -- | -- | P7-P0 | 166 | 166 |
| Chip Erase | C7h/60h | -- | -- | -- | -- | 166 | 166 |
| Read Status Register-1 | 05h | -- | -- | -- | (S7-S0) | 166 | 166 |
| Write Status Register-1 | 01h | -- | -- | -- | S7-S0 | 166 | 166 |
| Read Status Register-2 | 35h | -- | -- | -- | (S15-S8) | 166 | 166 |
| Write Status Register-2 | 31h | -- | -- | -- | S15-S8 | 166 | 166 |
| Read Status Register-3 | 15h | -- | -- | -- | (S23-S16) | 166 | 166 |
| Write Status Register-3 | 11h | -- | -- | -- | S23-S16 | 166 | 166 |
| Read SFDP Register | 5Ah | A23-16, A15-8, A7-0 | -- | 2 Dummy | (D7-D0) | 133 | 104 |
| Global Block Lock | 7Eh | -- | -- | -- | -- | 166 | 166 |
| Global Block Unlock | 98h | -- | -- | -- | -- | 166 | 166 |
| Erase / Program Suspend | 75h | -- | -- | -- | -- | 166 | 166 |
| Erase / Program Resume | 7Ah | -- | -- | -- | -- | 166 | 166 |
| Power-down | B9h | -- | -- | -- | -- | 166 | 166 |
| Enter 4-Byte Address Mode | B7h | -- | -- | -- | -- | 166 | 166 |
| Exit 4-Byte Address Mode | E9h | -- | -- | -- | -- | 166 | 166 |
| Exit QPI Mode | FFh | -- | -- | -- | -- | 166 | 166 |
| Enable Reset | 66h | -- | -- | -- | -- | 166 | 166 |
| Reset Device | 99h | -- | -- | -- | -- | 166 | 166 |
| Recovery for Erase | A8h | -- | -- | -- | -- | 166 | 166 |


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### 6.2.7 QPI Commands Operable in Both 3-Byte and 4-Byte Address Modes

| Command *W25Q33RV/64RV/12RV* | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|
| Number of Clock(IO 4-4-4) | 2 | 2-2-2-2 | M7-0 | N dummy | 2-2… | MHz | MHz |
| Page Program with 4-Byte Addr | 12h | A31-A0 | -- | -- | (D7-D0) | 166 | 166 |
| 4KB Sector Erase with 4-Byte Addr | 21h | A31-A0 | -- | -- | -- | 166 | 166 |
| 64KB Block Erase with 4-Byte Addr | DCh | A31-A0 | -- | -- | -- | 166 | 166 |
| Read Extended Address Register | C8h | -- | -- | -- | (EA7-0) | 166 | 166 |
| Write Extended Address Register | C5h | -- | -- | -- | EA7-0 | 166 | 166 |

| Command *W25Q33RV/64RV/12RV* | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|
| Number of Clock(IO 4-4-4) | 2 | --- | M7-0 | N dummy | 8 - 8… | MHz | MHz |
| Enter Factory Mode OP-1 | 51h | -- | -- | -- | -- | 166 | 166 |
| Enter Factory Mode OP-2 | A5h | -- | -- | -- | -- | 166 | 166 |
| Enter Factory Mode OP-3 | 41h | -- | -- | -- | -- | 166 | 166 |

### 6.2.8 QPI Commands Dependent in 3-Byte / 4-Byte Address Mode (ADS=1: A31–A0 / ADS=0: A23–A0)

| Command *W25Q33RV/64RV/12RV* | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|
| Number of Clock(IO 4-4-4) | 2 | 2 / 2-2-2 | M7-M0 | N dummy | 2-2… | MHz | MHz |
| Page Program | 02h | A31 / A23-A0 | -- | -- | D7-0.. | 166 | 166 |
| Sector Erase (4KB) | 20h | A31 / A23-A0 | -- | -- | -- | 166 | 166 |
| Block Erase (32KB) | 52h | A31 / A23-A0 | -- | -- | -- | 166 | 166 |
| Block Erase (64KB) | D8h | A31 / A23-A0 | -- | -- | | 166 | 166 |
| Read Flex Block Lock | 3Dh | A31 / A23-A0 | -- | -- | L7-L0 (2) | 133 | 104 |
| Flex Block Lock | 36h | A31 / A23-A0 | -- | -- | -- | 166 | 166 |
| Flex Block Unlock | 39h | A31 / A23-A0 | -- | -- | -- | 166 | 166 |


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### 6.2.9 QPI Commands Dependent in 3-Byte / 4-Byte Address Mode (ADS=1: A31–A0 / ADS=0: A23–A0)

| Command *W25Q33RV/64RV/12RV* | | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|---|
| Number of Clock(IO 4-4-4) | | 2 | 2 / 2-2-2 | M7-M0 | N dummy | 2 – 2… | MHz | MHz |
| **Fast Read** | | | A31 / A23-A0 | -- | 6 | (D7-0)… | 133 | 104 |
| Set Read Parameters (C0h) | 0 0 0 | 0Bh | A31 / A23-A0 | -- | 6 (Def) | (D7-0)… | 133 | 104 |
| | 0 0 1 | | A31 / A23-A0 | -- | 6 | (D7-0)… | 133 | 104 |
| | 0 1 0 | | A31 / A23-A0 | -- | 6 | (D7-0)… | 133 | 104 |
| | 0 1 1 | | A31 / A23-A0 | -- | 8 | (D7-0)… | 133 | 104 |
| | 1 0 0 | | A31 / A23-A0 | -- | 10 | (D7-0)… | 133 | 104 |
| | 1 0 1 | | A31 / A23-A0 | -- | 12 | (D7-0)… | 166 | 133 |
| | 1 1 0 | | A31 / A23-A0 | -- | 14 | (D7-0)… | 166 | 133 |
| | 1 1 1 | | A31 / A23-A0 | -- | 16 | (D7-0)… | 166 | 133 |
| **Burst Read with Wrap**(13) | | | A31 / A23-A0 | -- | 6 | (D7-0)… | 133 | 104 |
| Set Read Parameters (C0h) | 0 0 0 | 0Ch | A31 / A23-A0 | -- | 6 (Def) | (D7-0)… | 133 | 104 |
| | 0 0 1 | | A31 / A23-A0 | -- | 6 | (D7-0)… | 133 | 104 |
| | 0 1 0 | | A31 / A23-A0 | -- | 6 | (D7-0)… | 133 | 104 |
| | 0 1 1 | | A31 / A23-A0 | -- | 8 | (D7-0)… | 133 | 104 |
| | 1 0 0 | | A31 / A23-A0 | -- | 10 | (D7-0)… | 133 | 104 |
| | 1 0 1 | | A31 / A23-A0 | -- | 12 | (D7-0)… | 166 | 133 |
| | 1 1 0 | | A31 / A23-A0 | -- | 14 | (D7-0)… | 166 | 133 |
| | 1 1 1 | | A31 / A23-A0 | -- | 16 | (D7-0)… | 166 | 133 |
| **Fast Read Quad I/O** | | | A31 / A23-A0 | 2 | 4 | (D7-0)… | 133 | 104 |
| Set Read Parameters (C0h) M7–0 serve as dummy bits | 0 0 0 | EBh | A31 / A23-A0 | Disable | 6 (Def) | (D7-0)… | 133 | 104 |
| | 0 0 1 | | A31 / A23-A0 | Disable | 6 | (D7-0)… | 133 | 104 |
| | 0 1 0 | | A31 / A23-A0 | Disable | 6 | (D7-0)… | 133 | 104 |
| | 0 1 1 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 133 | 104 |
| | 1 0 0 | | A31 / A23-A0 | Disable | 10 | (D7-0)… | 133 | 104 |
| | 1 0 1 | | A31 / A23-A0 | Disable | 12 | (D7-0)… | 166 | 133 |
| | 1 1 0 | | A31 / A23-A0 | Disable | 14 | (D7-0)… | 166 | 133 |
| | 1 11 | | A31 / A23-A0 | Disable | 16 | (D7-0)… | 166 | 133 |


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### 6.2.10 QPI Commands Dependent in 3-Byte / 4-Byte Address Mode (ADS=1: A31–A0 / ADS=0: A23–A0)

| **Command** *W25Q33RV/64RV/12RV* | | **Opcode** | **Address Bytes** | **Read Bypass** | **Dummy Cycles** | **Data Bytes** | **Aligned Address** | **Any Address** |
|---|---|---|---|---|---|---|---|---|
| Number of Clock(IO 4-4-4) | | 2 | 2 / 2-2-2 | M7-M0 | N dummy | 2-2-2-2,… | MHz | MHz |
| Read checksum | | 9Ch | A31 / A23-A0 | -- | 6 | D(7-0,15-8,23-16,31-24)… | 133 | 104 |
| Set Read Parameters (C0h) | 0 0 0 | | A31 / A23-A0 | -- | 6 (Def) | D(7-0,15-8,23-16,31-24)… | 133 | 104 |
| | 0 0 1 | | A31 / A23-A0 | -- | 6 | D(7-0,15-8,23-16,31-24)… | 133 | 104 |
| | 0 1 0 | | A31 / A23-A0 | -- | 6 | D(7-0,15-8,23-16,31-24)… | 133 | 104 |
| | 0 1 1 | | A31 / A23-A0 | -- | 8 | D(7-0,15-8,23-16,31-24)… | 133 | 104 |
| | 1 0 0 | | A31 / A23-A0 | -- | 10 | D(7-0,15-8,23-16,31-24)… | 133 | 104 |
| | 1 0 1 | | A31 / A23-A0 | -- | 12 | D(7-0,15-8,23-16,31-24)… | 166 | 133 |
| | 1 1 0 | | A31 / A23-A0 | -- | 14 | D(7-0,15-8,23-16,31-24)… | 166 | 133 |
| | 1 1 1 | | A31 / A23-A0 | -- | 16 | D(7-0,15-8,23-16,31-24)… | 166 | 133 |
| Command | | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
| Number of Clock (IO 4-4-4) | | 2 | 2 / 2-2-2, 2-2-2-2 | M7-M0 | N dummy | 2 – 2… | MHz | MHz |
| Calculate checksum | | 9Dh | SA31/SA23-0, EA31-EA0 | | -- | -- | 166 | 166 |


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### 6.2.11 SPI DTR Commands Dependent in 3-Byte / 4-Byte Address Mode (ADS=1: A31–A0, ADS=0: A23–A0)

| Command *W25Q33RV/64RV/12RV* | | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|---|
| Number of Clock (IO 1-1d-1d) | | 8 | 8 / 8-8-8 | M7-0 | N dummy | 4-…Clock | MHz | MHz |
| DTR Fast Read | | 0Dh | A31 / A23-A0 | -- | 6 | (D7-0)… | 84 | 66 |
| Number of Clock (IO 1-2d-2d) | | 8 | 2 / 2-2-2 | M7-0 | N dummy | 2-…Clock | MHz | MHz |
| DTR Fast Read Dual I/O | | BDh | A31 / A23-A0 | 2 | 4 | (D7-0)… | 84 | 66 |
| Number of Clock (IO 1-4d-4d) | | 8 | 1 / 1-1-1 | M7-0 | N dummy | 1… | MHz | MHz |
| DTR Fast Read Quad I/O | | EDh | A31 / A23-A0 | 1 | 7 | (D7-0)… | 84 | 66 |
| Set Read Parameters (C0h) M7–0 serve as dummy bits | 0 0 0 | | A31 / A23-A0 | Disable | 8 (Def) | (D7-0)… | 84 | 66 |
| | 0 0 1 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 84 | 66 |
| | 0 1 0 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 84 | 66 |
| | 0 1 1 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 84 | 66 |
| | 1 0 0 | | A31 / A23-A0 | Disable | 10 | (D7-0)… | 84 | 66 |
| | 1 0 1 | | A31 / A23-A0 | Disable | 12 | (D7-0)… | 104 | 84 |
| | 1 1 0 | | A31 / A23-A0 | Disable | 14 | (D7-0)… | 104 | 84 |
| | 1 1 1 | | A31 / A23-A0 | Disable | 16 | (D7-0)… | 104 | 84 |


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### 6.2.12 SPI DTR Commands Operable in Both 3-Byte and 4-Byte Address Modes

| Command *W25Q33RV/64RV/12RV* | | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|---|
| Number of Clock(IO 1-4d-4d) | | 8 | 1-1-1-1 | M7-0 | N dummy | 1-…Clock | MHz | MHz |
| DTR Fast Read Quad I/O with 4-Byte Addr. | | EEh | A31-A0 | 1 | 7 | (D7-0)… | 84 | 66 |
| Set Read Parameters (C0h) M7–0 serve as dummy bits | 0 0 0 | | A31-A0 | Disable | 8 (Def) | (D7-0)… | 84 | 66 |
| | 0 0 1 | | A31-A0 | Disable | 8 | (D7-0)… | 84 | 66 |
| | 0 1 0 | | A31-A0 | Disable | 8 | (D7-0)… | 84 | 66 |
| | 0 1 1 | | A31-A0 | Disable | 8 | (D7-0)… | 84 | 66 |
| | 1 0 0 | | A31-A0 | Disable | 10 | (D7-0)… | 84 | 66 |
| | 1 0 1 | | A31-A0 | Disable | 12 | (D7-0)… | 104 | 84 |
| | 1 1 0 | | A31-A0 | Disable | 14 | (D7-0)… | 104 | 84 |
| | 1 1 1 | | A31-A0 | Disable | 16 | (D7-0)… | 104 | 84 |


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### 6.2.13 QPI DTR Commands Dependent in 3-Byte / 4-Byte Address Mode (ADS=1: A31–A0, ADS=0: A23–A0)

| Command *W25Q33RV/64RV/12RV* | | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|---|
| Number of Clock((IO 4-4d-4d) | | 2 | 1 / 1-1-1 | M7-0 | N dummy | 1-…Clock | MHz | MHz |
| **DTR Read with Wrap**(12) | | 0Eh | A31 / A23-A0 | 1 | 7 | (D7-0)… | 84 | 66 |
| Set Read Parameters (C0h) M7–0 serve as dummy bits | 0 0 0 | | A31 / A23-A0 | Disable | 8 (Def) | (D7-0)… | 84 | 66 |
| | 0 0 1 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 84 | 66 |
| | 0 1 0 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 84 | 66 |
| | 0 1 1 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 84 | 66 |
| | 1 0 0 | | A31 / A23-A0 | Disable | 10 | (D7-0)… | 84 | 66 |
| | 1 0 1 | | A31 / A23-A0 | Disable | 12 | (D7-0)… | 104 | 84 |
| | 1 1 0 | | A31 / A23-A0 | Disable | 14 | (D7-0)… | 104 | 84 |
| | 1 1 1 | | A31 / A23-A0 | Disable | 16 | (D7-0)… | 104 | 84 |
| **DTR Fast Read** | | 0Dh | A31 / A23-A0 | -- | 8 | (D7-0)… | 84 | 66 |
| Set Read Parameters (C0h) | 0 0 0 | | A31 / A23-A0 | - | 8 (Def) | (D7-0)… | 84 | 66 |
| | 0 0 1 | | A31 / A23-A0 | - | 8 | (D7-0)… | 84 | 66 |
| | 0 1 0 | | A31 / A23-A0 | - | 8 | (D7-0)… | 84 | 66 |
| | 0 1 1 | | A31 / A23-A0 | - | 8 | (D7-0)… | 84 | 66 |
| | 1 0 0 | | A31 / A23-A0 | - | 10 | (D7-0)… | 84 | 66 |
| | 1 0 1 | | A31 / A23-A0 | - | 12 | (D7-0)… | 104 | 84 |
| | 1 1 0 | | A31 / A23-A0 | - | 14 | (D7-0)… | 104 | 84 |
| | 1 1 1 | | A31 / A23-A0 | - | 16 | (D7-0)… | 104 | 84 |


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### 6.2.14 QPI DTR Commands Dependent in 3-Byte / 4-Byte Address Mode (ADS=1: A31–A0, ADS=0: A23–A0)

| Command *W25Q33RV/64RV/12RV* | | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|---|
| Number of Clock (IO 4-4d-4d) | | 2 | 1 / 1-1-1 | M7-0 | N dummy | 1-…Clock | MHz | MHz |
| DTR Fast Read Quad I/O | | EDh | A31 / A23-A0 | 1 | 7 | (D7-0)… | 84 | 66 |
| Set Read Parameters (C0h) M7–0 serve as dummy bits | 0 0 0 | | A31 / A23-A0 | Disable | 8 (Def) | (D7-0)… | 84 | 66 |
| | 0 0 1 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 84 | 66 |
| | 0 1 0 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 84 | 66 |
| | 0 1 1 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 84 | 66 |
| | 1 0 0 | | A31 / A23-A0 | Disable | 10 | (D7-0)… | 84 | 66 |
| | 1 0 1 | | A31 / A23-A0 | Disable | 12 | (D7-0)… | 104 | 84 |
| | 1 1 0 | | A31 / A23-A0 | Disable | 14 | (D7-0)… | 104 | 84 |
| | 1 1 1 | | A31 / A23-A0 | Disable | 16 | (D7-0)… | 104 | 84 |

### 6.2.15 QPI DTR Commands Operable in Both 3-Byte and 4-Byte Address Modes

| Command *W25Q33RV/64RV/12RV* | | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|---|
| Number of Clock (IO 4-4d-4d) | | 2 | 1-1-1-1 | M7-0 | N dummy | 1-…Clock | MHz | MHz |
| DTR Fast Read I/O with 4-Byte Address | | EEh | A31-A0 | 1 | 7 | (D7-0)… | 84 | 66 |
| Set Read Parameters (C0h) M7–0 serve as dummy bits | 0 0 0 | | A31-A0 | Disable | 8 (Def) | (D7-0)… | 84 | 66 |
| | 0 0 1 | | A31-A0 | Disable | 8 | (D7-0)… | 84 | 66 |
| | 0 1 0 | | A31-A0 | Disable | 8 | (D7-0)… | 84 | 66 |
| | 0 1 1 | | A31-A0 | Disable | 8 | (D7-0)… | 84 | 66 |
| | 1 0 0 | | A31-A0 | Disable | 10 | (D7-0)… | 84 | 66 |
| | 1 0 1 | | A31-A0 | Disable | 12 | (D7-0)… | 104 | 84 |
| | 1 1 0 | | A31-A0 | Disable | 14 | (D7-0)… | 104 | 84 |
| | 1 1 1 | | A31-A0 | Disable | 16 | (D7-0)… | 104 | 84 |


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## 6.3 W25Q25RV/51RV/01RV/02RV Command Table with Maximum Clock Frequencies (MHz)(1)

### 6.3.1 SPI Commands Operable in Both 3-Byte and 4-Byte Address Modes

| Command *W25Q25RV/51RV/01RV/02RV* | Opcode | Address Bytes | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|
| Number of Clock (IO 1-1-1) | 8 | 8-8-8 | N dummy | 8 - 8… | MHz | MHz |
| Write Enable | 06h | -- | -- | -- | 133 | 133 |
| Volatile Status Register Write Enable | 50h | -- | -- | -- | 133 | 133 |
| Write Disable | 04h | -- | -- | -- | 133 | 133 |
| Release Power-down / ID | ABh | -- | 24 | ID7-ID0 | 133 | 133 |
| Read Manufacturer/Device ID | 90h | 00h,00h,00h | -- | (MF7-0) - (ID7-ID0) | 133 | 133 |
| Read JEDEC ID | 9Fh | -- | -- | (MF7-0) - (ID15-8) - (ID7-0) | 133 | 133 |
| Set Read Parameters | C0h | -- | -- | P7-P0 | 133 | 133 |
| Chip Erase | C7h/60h | -- | -- | -- | 133 | 133 |
| Read Status Register-1 | 05h | -- | -- | (S7-S0) | 133 | 133 |
| Write Status Register-1 | 01h | -- | -- | S7-S0 | 133 | 133 |
| Read Status Register-2 | 35h | -- | -- | (S15-S8) | 133 | 133 |
| Write Status Register-2 | 31h | -- | -- | S15-S8 | 133 | 133 |
| Read Status Register-3 | 15h | -- | -- | (S23-S16) | 133 | 133 |
| Write Status Register-3 | 11h | -- | -- | S23-S16 | 133 | 133 |
| Read SFDP Register | 5Ah | A23-A0 | 8 | (D7-D0) | 104 | 66 |
| Global Block Lock | 7Eh | -- | -- | -- | 133 | 133 |
| Global Block Unlock | 98h | -- | -- | -- | 133 | 133 |
| Erase / Program Suspend | 75h | -- | -- | -- | 133 | 133 |
| Erase / Program Resume | 7Ah | -- | -- | -- | 133 | 133 |
| Power-down | B9h | -- | -- | -- | 133 | 133 |
| Enter 4-Byte Address Mode | B7h | -- | -- | -- | 133 | 133 |
| Exit 4-Byte Address Mode | E9h | -- | -- | -- | 133 | 133 |
| Enter QPI Mode | 38h | -- | -- | -- | 133 | 133 |
| Enable Reset | 66h | -- | -- | -- | 133 | 133 |
| Reset Device | 99h | -- | -- | -- | 133 | 133 |
| Set Burst with Wrap | 77h | | 24 | | 133 | 133 |
| Recovery for Erase | A8h | -- | -- | -- | 133 | 133 |



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### 6.3.2 SPI Commands Operable in Both 3-Byte and 4-Byte Address Modes

| Command *W25Q25RV/51RV/01RV/02RV* | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|
| Number of Clock (IO 1-1-1) | 8 | 8-8-8-8 | M7-0 | N dummy | 8 - 8… | MHz | MHz |
| Read Data with 4-Byte Addr | 13h | A31-A0 | -- | -- | (D7-D0) | 84 | 50 |
| Fast Read with 4-Byte Addr | 0Ch | A31-A0 | -- | 8 | (D7-D0) | 104 | 66 |
| Page Program with 4-Byte Addr | 12h | A31-A0 | -- | -- | (D7-D0) | 104 | 66 |
| 4KB Sector Erase with 4-Byte Addr | 21h | A31-A0 | -- | -- | -- | 133 | 133 |
| 64KB Block Erase with 4-Byte Addr | DCh | A31-A0 | -- | -- | -- | 133 | 133 |
| Read Extended Address Register | C8h | -- | -- | -- | (EA7-0) | 133 | 133 |
| Write Extended Address Register | C5h | -- | -- | -- | EA7-0 | 133 | 133 |

| Command | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|
| Number of Clock (IO 1-1-1) | 8 | --- | M7-0 | N dummy | 8 - 8… | MHz | MHz |
| Enter Factory Mode OP-1 | 51h | -- | -- | -- | -- | 133 | 133 |
| Enter Factory Mode OP-2 | A5h | -- | -- | -- | -- | 133 | 133 |
| Enter Factory Mode OP-3 | 41h | -- | -- | -- | -- | 133 | 133 |


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### 6.3.3 SPI Commands Operable in Both 3-Byte and 4-Byte Address Modes

| Command<br>*W25Q25RV/51RV/01RV/02RV* | | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|---|
| Number of Clock (IO 1-1-2) | | 8 | 8-8-8-8 | M7-0 | N dummy | 4 - … Clock | MHz | MHz |
| Fast Read Dual Output | | 3Ch | A31-A0 | -- | 8 | (D7-D0)… | 104 | 66 |
| Number of Clock (1-1-4) | | 8 | 8-8-8-8 | M7-0 | N dummy | 2-…Clock | MHz | MHz |
| Quad Input Page Program | | 34h | A31-A0 | | -- | D7-D0... | 104 | 66 |
| Fast Read Quad Output | | 6Ch | A31-A0 | -- | 8 | (D7-D0) | 104 | 66 |
| Number of Clock (1-2-2) | | 8 | 4-4-4-4 | M7-0 | N dummy | 4-…Clock | MHz | MHz |
| Fast Read Dual I/O | | BCh | A31-A0, | 4 | 4 | (D7-D0) | 104 | 66 |
| Number of Clock (1-4-4) | | 8 | 2-2-2-2 | M7-0 | N dummy | 2-… Clock | MHz | MHz |
| Fast Read Quad I/O | | ECh | A31-A0 | 2 | 4 | (D7-D0) | 104 | 66 |
| Set Read Parameters (C0h)<br>M7–0 serve as dummy bits | 0 0 0 | | A31-A0 | Disable | 6 (Def) | (D7-0)… | 104 | 66 |
| | 0 0 1 | | A31-A0 | Disable | 6 | (D7-0)… | 104 | 66 |
| | 0 1 0 | | A31-A0 | Disable | 6 | (D7-0)… | 104 | 66 |
| | 0 1 1 | | A31-A0 | Disable | 8 | (D7-0)… | 133 | 66 |
| | 1 0 0 | | A31-A0 | Disable | 10 | (D7-0)… | 133 | 66 |
| | 1 0 1 | | A31-A0 | Disable | 12 | (D7-0)… | 133 | 84 |
| | 1 1 0 | | A31-A0 | Disable | 14 | (D7-0)… | 133 | 84 |
| | 1 1 1 | | A31-A0 | Disable | 16 | (D7-0)… | 133 | 84 |


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### 6.3.4 SPI Commands Dependent in 3‑Byte / 4‑Byte Address Mode (ADS=1: A31–A0 / ADS=0: A23–A0)

| Command *W25Q25RV/51RV/01RV/02RV* | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|
| Number of Clock (IO 1-1-1) | 8 | 8 / 8-8-8 | M7-0 | N dummy | 8-… Clock | MHz | MHz |
| Read Unique ID | 4Bh | -- | | 40 / 32 | (D7-D0)… | 104 | 66 |
| Read Data | 03h | A31 / A23-A0 | | -- | (D7-D0).. | 84 | 50 |
| Fast Read | 0Bh | A31 / A23-A0 | | 8 | (D7-D0)… | 104 | 66 |
| Page Program | 02h | A31 / A23-A0 | | -- | D7-D0… | 104 | 66 |
| 4KB Sector Erase | 20h | A31 / A23-A0 | | -- | -- | 133 | 133 |
| 32KB Block Erase | 52h | A31 / A23-A0 | | -- | -- | 133 | 133 |
| 64KB Block Erase | D8h | A31 / A23-A0 | | -- | -- | 133 | 133 |
| Erase Security Register(5) | 44h | A31 / A23-A0 | | -- | -- | 133 | 133 |
| Program Security Register(5) | 42h | A31 / A23-A0 | | -- | D7-D0… | 133 | 133 |
| Read Security Register(5) | 48h | A31 / A23-A0 | | 8 | (D7-D0)… | 104 | 66 |
| Read Flex Block Lock | 3Dh | A31 / A23-A0 | | -- | (L7-L0)… | 104 | 66 |
| Flex Block Lock | 36h | A31 / A23-A0 | | -- | -- | 133 | 133 |
| Flex Block Unlock | 39h | A31 / A23-A0 | | -- | -- | 133 | 133 |

| Command *W25Q25RV/51RV/01RV/02RV* | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|
| Number of Clock (IO 1-1-1) | 8 | 8 / 8-8-8 | M7-0 | N dummy/ Clock | 8 - 8… | MHz | MHz |
| Clear Buffer | 81h(14) | BA31 / BA23-BA0 | -- | -- | -- | 133 | 133 |
| Write Buffer | 82h(14) | BA31 / BA23-BA0 | -- | -- | (D7-D0) | 133 | 133 |
| Read Buffer | 83h(14) | BA31 / BA23-BA0 | -- | 8 | (D7-D0) | 133 | 133 |
| Program Buffer | 8Ah | A31 / A23-A0 | -- | -- | -- | 133 | 133 |
| Load Buffer | 8Bh | A31 / A23-A0 | -- | -- | -- | 133 | 133 |


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### 6.3.5 SPI Commands Dependent in 3-Byte / 4-Byte Address Mode (ADS=1: A31–A0 / ADS=0: A23–A0)

| Command<br>*W25Q25RV/51RV/01RV/02RV* | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|
| Number of Clock (IO 1-1-1) | 8 | 8 / 8-8-8 | M7-M0 | N dummy | 8-8-8-8,… | MHz | MHz |
| Read checksum | 9Ch | A31 / A23-A0 | -- | 8 | D(7-0,15-8,23-16,31-24),… | 104 | 66 |
| Command | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
| Number of Clock (IO 1-1-1) | 8 | 8 / 8-8-8,8-8-8 | | N dummy | 8-8-8-8 | MHz | MHz |
| Calculate checksum | 9Dh | SA31/SA23-0, EA31-EA0 | | -- | -- | 133 | 133 |

| Command<br>*W25Q25RV/51RV/01RV/02RV* | | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|---|
| Number of Clock (IO 1-1-2) | | 8 | 8 / 8-8-8 | M7-M0 | N dummy | 4-… | MHz | MHz |
| Fast Read Dual Output | | 3Bh | A31 / A23-A0 | -- | 8 | (D7-0)… | 104 | 66 |
| Number of Clock (IO 1-1-4) | | 8 | 8 / 8-8-8 | M7-M0 | N dummy | 2-… | MHz | MHz |
| Quad Input Page Program | | 32h | A31 / A23-A0 | -- | -- | D7-0… | 104 | 66 |
| Fast Read Quad Output | | 6Bh | A31 / A23-A0 | -- | 8 | (D7-0)… | 104 | 66 |
| Number of Clock (IO 1-2-2) | | | 4 / 4-4-4 | M7-M0 | N dummy | 4-… | MHz | MHz |
| Mftr./Device ID Dual I/O | | 92h | A31 / A23-8,00h | 4-N/Allow | -- | (MF7-0, ID7-ID0) | 104 | 66 |
| Fast Read Dual I/O | | BBh | A31 / A23-A0 | 4 | -- | (D7-0) | 104 | 66 |
| Number of Clock (IO 1-4-4) | | | 2 / 2-2-2-2-2 | 2 | N dummy | 2-… Clock | MHz | MHz |
| Mftr./Device ID Quad I/O | | 94h | A31 / A23-8,00h | 2-N/Allow | 4 | (MF7-0, ID7-ID0) | 104 | 66 |
| Fast Read Quad I/O | | EBh | A31 / A23-A0 | 2 | 4 | (D7-0)… | 104 | 66 |
| Set Read Parameters (C0h) M7–0 serve as dummy bits | 0 0 0 | | A31 / A23-A0 | Disable | 6(Def.) | (D7-0)… | 104 | 66 |
| | 0 0 1 | | A31 / A23-A0 | Disable | 6 | (D7-0)… | 104 | 66 |
| | 0 1 0 | | A31 / A23-A0 | Disable | 6 | (D7-0)… | 104 | 66 |
| | 0 1 1 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 133 | 66 |
| | 1 0 0 | | A31 / A23-A0 | Disable | 10 | (D7-0)… | 133 | 66 |
| | 1 0 1 | | A31 / A23-A0 | Disable | 12 | (D7-0)… | 133 | 84 |
| | 1 1 0 | | A31 / A23-A0 | Disable | 14 | (D7-0)… | 133 | 84 |
| | 1 1 1 | | A31 / A23-A0 | Disable | 16 | (D7-0)… | 133 | 84 |



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### 6.3.6 QPI Commands Operable in Both 3-Byte and 4-Byte Address Modes

| Command<br>*W25Q25RV/51RV/01RV/02RV* | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|
| Number of Clock (IO 4-4-4) | 2 | 2-2-2 | M7-M0 | N dummy | 2-2… | MHz | MHz |
| Write Enable | 06h | -- | -- | -- | -- | 133 | 133 |
| Volatile Status Register Write Enable | 50h | -- | -- | -- | -- | 133 | 133 |
| Write Disable | 04h | -- | -- | -- | -- | 133 | 133 |
| Release Power-down / ID | ABh | -- | -- | 6 | (ID7-ID0) | 133 | 133 |
| Read Manufacturer/Device ID | 90h | -- | -- | 4 Dummy + 00h | (MF7-0, ID7-ID0) | 133 | 133 |
| Read JEDEC ID | 9Fh | -- | -- | -- | (MF7-0) - (ID15-8) - (ID7-0) | 133 | 133 |
| Set Read Parameters | C0h | -- | -- | -- | P7-P0 | 133 | 133 |
| Chip Erase | C7h/60h | -- | -- | -- | -- | 133 | 133 |
| Read Status Register-1 | 05h | -- | -- | -- | (S7-S0) | 133 | 133 |
| Write Status Register-1 | 01h | -- | -- | -- | S7-S0 | 133 | 133 |
| Read Status Register-2 | 35h | -- | -- | -- | (S15-S8) | 133 | 133 |
| Write Status Register-2 | 31h | -- | -- | -- | S15-S8 | 133 | 133 |
| Read Status Register-3 | 15h | -- | -- | -- | (S23-S16) | 133 | 133 |
| Write Status Register-3 | 11h | -- | -- | -- | S23-S16 | 133 | 133 |
| Read SFDP Register | 5Ah | A23-16, A15-8, A7-0 | -- | 2 Dummy | (D7-D0) | 133 | 133 |
| Global Block Lock | 7Eh | -- | -- | -- | -- | 133 | 133 |
| Global Block Unlock | 98h | -- | -- | -- | -- | 133 | 133 |
| Erase / Program Suspend | 75h | -- | -- | -- | -- | 133 | 133 |
| Erase / Program Resume | 7Ah | -- | -- | -- | -- | 133 | 133 |
| Power-down | B9h | -- | -- | -- | -- | 133 | 133 |
| Enter 4-Byte Address Mode | B7h | -- | -- | -- | -- | 133 | 133 |
| Exit 4-Byte Address Mode | E9h | -- | -- | -- | -- | 133 | 133 |
| Exit QPI Mode | FFh | -- | -- | -- | -- | 133 | 133 |
| Enable Reset | 66h | -- | -- | -- | -- | 133 | 133 |
| Reset Device | 99h | -- | -- | -- | -- | 133 | 133 |
| Recovery for Erase | A8h | -- | -- | -- | -- | 133 | 133 |



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### 6.3.7 QPI Commands Operable in Both 3-Byte and 4-Byte Address Modes

| Command<br>*W25Q25RV/51RV/01RV/02RV* | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|
| Number of Clock(IO 4-4-4) | 2 | 2-2-2-2 | M7-0 | N dummy | 2-2… | MHz | MHz |
| Page Program with 4-Byte Addr | 12h | A31-A0 | -- | -- | (D7-D0) | 133 | 133 |
| 4KB Sector Erase with 4-Byte Addr | 21h | A31-A0 | -- | -- | -- | 133 | 133 |
| 64KB Block Erase with 4-Byte Addr | DCh | A31-A0 | -- | -- | -- | 133 | 133 |
| Read Extended Address Register | C8h | -- | -- | -- | (EA7-0) | 133 | 133 |
| Write Extended Address Register | C5h | -- | -- | -- | EA7-0 | 133 | 133 |

| Command<br>*W25Q25RV/51RV/01RV/02RV* | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|
| Number of Clock(IO 4-4-4) | 2 | --- | M7-0 | N dummy | 8 - 8… | MHz | MHz |
| Enter Factory Mode OP-1 | 51h | -- | -- | -- | -- | 133 | 133 |
| Enter Factory Mode OP-2 | A5h | -- | -- | -- | -- | 133 | 133 |
| Enter Factory Mode OP-3 | 41h | -- | -- | -- | -- | 133 | 133 |

### 6.3.8 QPI Commands Dependent in 3-Byte / 4-Byte Address Mode (ADS=1: A31–A0 / ADS=0: A23–A0)

| Command<br>*W25Q25RV/51RV/01RV/02RV* | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|
| Number of Clock(IO 4-4-4) | 2 | 2 / 2-2-2 | M7-M0 | N dummy | 2-2… | MHz | MHz |
| Page Program | 02h | A31 / A23-A0 | -- | -- | D7-0.. | 133 | 133 |
| Sector Erase (4KB) | 20h | A31 / A23-A0 | -- | -- | -- | 133 | 133 |
| Block Erase (32KB) | 52h | A31 / A23-A0 | -- | -- | -- | 133 | 133 |
| Block Erase (64KB) | D8h | A31 / A23-A0 | -- | -- | | 133 | 133 |
| Read Flex Block Lock | 3Dh | A31 / A23-A0 | -- | -- | L7-L0 (2) | 104 | 66 |
| Flex Block Lock | 36h | A31 / A23-A0 | -- | -- | -- | 133 | 133 |
| Flex Block Unlock | 39h | A31 / A23-A0 | -- | -- | -- | 133 | 133 |



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### 6.3.9 QPI Commands Dependent in 3-Byte / 4-Byte Address Mode (ADS=1: A31–A0 / ADS=0: A23–A0)

| **Command** *W25Q25RV/51RV/01RV/02RV* | | **Opcode** | **Address Bytes** | **Read Bypass** | **Dummy Cycles** | **Data Bytes** | **Aligned Address** | **Any Address** |
|---|---|---|---|---|---|---|---|---|
| Number of Clock(IO 4-4-4) | | 2 | 2 / 2-2-2 | M7-M0 | N dummy | 2 – 2… | MHz | MHz |
| Fast Read | | 0Bh | A31 / A23-A0 | -- | 6 | (D7-0)… | 104 | 66 |
| Set Read Parameters (C0h) | 0 0 0 | | A31 / A23-A0 | -- | 6 (Def) | (D7-0)… | 104 | 66 |
| | 0 0 1 | | A31 / A23-A0 | -- | 6 | (D7-0)… | 104 | 66 |
| | 0 1 0 | | A31 / A23-A0 | -- | 6 | (D7-0)… | 104 | 66 |
| | 0 1 1 | | A31 / A23-A0 | -- | 8 | (D7-0)… | 133 | 66 |
| | 1 0 0 | | A31 / A23-A0 | -- | 10 | (D7-0)… | 133 | 66 |
| | 1 0 1 | | A31 / A23-A0 | -- | 12 | (D7-0)… | 133 | 84 |
| | 1 1 0 | | A31 / A23-A0 | -- | 14 | (D7-0)… | 133 | 84 |
| | 1 1 1 | | A31 / A23-A0 | -- | 16 | (D7-0)… | 133 | 84 |
| Burst Read with Wrap[13] | | 0Ch | A31 / A23-A0 | -- | 6 | (D7-0)… | 104 | 66 |
| Set Read Parameters (C0h) | 0 0 0 | | A31 / A23-A0 | -- | 6 (Def) | (D7-0)… | 104 | 66 |
| | 0 0 1 | | A31 / A23-A0 | -- | 6 | (D7-0)… | 104 | 66 |
| | 0 1 0 | | A31 / A23-A0 | -- | 6 | (D7-0)… | 104 | 66 |
| | 0 1 1 | | A31 / A23-A0 | -- | 8 | (D7-0)… | 133 | 66 |
| | 1 0 0 | | A31 / A23-A0 | -- | 10 | (D7-0)… | 133 | 66 |
| | 1 0 1 | | A31 / A23-A0 | -- | 12 | (D7-0)… | 133 | 84 |
| | 1 1 0 | | A31 / A23-A0 | -- | 14 | (D7-0)… | 133 | 84 |
| | 1 1 1 | | A31 / A23-A0 | -- | 16 | (D7-0)… | 133 | 84 |
| Fast Read Quad I/O | | EBh | A31 / A23-A0 | 2 | 4 | -- | 104 | 66 |
| Set Read Parameters (C0h) M7–0 serve as dummy bits | 0 0 0 | | A31 / A23-A0 | Disable | 6 (Def) | (D7-0)… | 104 | 66 |
| | 0 0 1 | | A31 / A23-A0 | Disable | 6 | (D7-0)… | 104 | 66 |
| | 0 1 0 | | A31 / A23-A0 | Disable | 6 | (D7-0)… | 104 | 66 |
| | 0 1 1 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 133 | 66 |
| | 1 0 0 | | A31 / A23-A0 | Disable | 10 | (D7-0)… | 133 | 66 |
| | 1 0 1 | | A31 / A23-A0 | Disable | 12 | (D7-0)… | 133 | 84 |
| | 1 1 0 | | A31 / A23-A0 | Disable | 14 | (D7-0)… | 133 | 84 |
| | 1 11 | | A31 / A23-A0 | Disable | 16 | (D7-0)… | 133 | 84 |



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### 6.3.10 QPI Commands Dependent in 3-Byte / 4-Byte Address Mode (ADS=1: A31–A0 / ADS=0: A23–A0)

| **Command** *W25Q25RV/51RV/01RV/02RV* | | **Opcode** | **Address Bytes** | **Read Bypass** | **Dummy Cycles** | **Data Bytes** | **Aligned Address** | **Any Address** |
|---|---|---|---|---|---|---|---|---|
| Number of Clock(IO 4-4-4) | | 2 | 2 / 2-2-2 | M7-M0 | N dummy | 2-2-2-2,… | MHz | MHz |
| Read checksum | | 9Ch | A31 / A23-A0 | -- | 6 | D(7-0,15-8,23-16,31-24)… | 104 | 66 |
| Set Read Parameters (C0h) | 0 0 0 | | A31 / A23-A0 | -- | 6 (Def) | D(7-0,15-8,23-16,31-24)… | 104 | 66 |
| | 0 0 1 | | A31 / A23-A0 | -- | 6 | D(7-0,15-8,23-16,31-24)… | 104 | 66 |
| | 0 1 0 | | A31 / A23-A0 | -- | 6 | D(7-0,15-8,23-16,31-24)… | 104 | 66 |
| | 0 1 1 | | A31 / A23-A0 | -- | 8 | D(7-0,15-8,23-16,31-24)… | 133 | 66 |
| | 1 0 0 | | A31 / A23-A0 | -- | 10 | D(7-0,15-8,23-16,31-24)… | 133 | 66 |
| | 1 0 1 | | A31 / A23-A0 | -- | 12 | D(7-0,15-8,23-16,31-24)… | 133 | 84 |
| | 1 1 0 | | A31 / A23-A0 | -- | 14 | D(7-0,15-8,23-16,31-24)… | 133 | 84 |
| | 1 1 1 | | A31 / A23-A0 | -- | 16 | D(7-0,15-8,23-16,31-24)… | 133 | 84 |
| Command | | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
| Number of Clock (IO 4-4-4) | | 2 | 2 / 2-2-2, 2-2-2-2 | M7-M0 | N dummy | 2 – 2… | MHz | MHz |
| Calculate checksum | | 9Dh | SA31/SA23-0, EA31-EA0 | | -- | -- | 133 | 133 |



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### 6.3.11 SPI DTR Commands Dependent in 3-Byte / 4-Byte Address Mode (ADS=1: A31–A0, ADS=0: A23–A0)

| Command<br>*W25Q25RV/51RV/01RV/02RV* | | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|---|
| Number of Clock (IO 1-1d-1d) | | 8 | 8 / 8-8-8 | M7-0 | N dummy | 4-…Clock | MHz | MHz |
| DTR Fast Read | | 0Dh | A31 / A23-A0 | -- | 6 | (D7-0)… | 84 | 50 |
| Number of Clock (IO 1-2d-2d) | | 8 | 2 / 2-2-2 | M7-0 | N dummy | 2-…Clock | | |
| DTR Fast Read Dual I/O | | BDh | A31 / A23-A0 | 2 | 4 | (D7-0)… | 84 | 50 |
| Number of Clock (IO 1-4d-4d) | | 8 | 1 / 1-1-1 | M7-0 | N dummy | 1… | MHz | MHz |
| DTR Fast Read Quad I/O | | EDh | A31 / A23-A0 | 1 | 7 | (D7-0)… | 84 | 50 |
| Set Read Parameters (C0h)<br>M7–0 serve as dummy bits | 0 0 0 | | A31 / A23-A0 | Disable | 8 (Def) | (D7-0)… | 84 | 50 |
| | 0 0 1 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 84 | 50 |
| | 0 1 0 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 84 | 50 |
| | 0 1 1 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 84 | 50 |
| | 1 0 0 | | A31 / A23-A0 | Disable | 10 | (D7-0)… | 84 | 50 |
| | 1 0 1 | | A31 / A23-A0 | Disable | 12 | (D7-0)… | 104 | 66 |
| | 1 1 0 | | A31 / A23-A0 | Disable | 14 | (D7-0)… | 104 | 66 |
| | 1 1 1 | | A31 / A23-A0 | Disable | 16 | (D7-0)… | 104 | 66 |



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### 6.3.12 SPI DTR Commands Operable in Both 3-Byte and 4-Byte Address Modes

| Command<br>*W25Q25RV/51RV/01RV/02RV* | | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|---|
| Number of Clock((IO 1-4d-4d) | | 8 | 1-1-1-1 | M7-0 | N dummy | 1-…Clock | MHz | MHz |
| DTR Fast Read Quad I/O with 4-Byte Addr. | | EEh | A31-A0 | 1 | 7 | (D7-0)… | 84 | 50 |
| Set Read Parameters (C0h) M7–0 serve as dummy bits | 0 0 0 | | A31-A0 | Disable | 8 (Def) | (D7-0)… | 84 | 50 |
| | 0 0 1 | | A31-A0 | Disable | 8 | (D7-0)… | 84 | 50 |
| | 0 1 0 | | A31-A0 | Disable | 8 | (D7-0)… | 84 | 50 |
| | 0 1 1 | | A31-A0 | Disable | 8 | (D7-0)… | 84 | 50 |
| | 1 0 0 | | A31-A0 | Disable | 10 | (D7-0)… | 84 | 50 |
| | 1 0 1 | | A31-A0 | Disable | 12 | (D7-0)… | 104 | 66 |
| | 1 1 0 | | A31-A0 | Disable | 14 | (D7-0)… | 104 | 66 |
| | 1 1 1 | | A31-A0 | Disable | 16 | (D7-0)… | 104 | 66 |



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### 6.3.13 QPI DTR Commands Dependent in 3-Byte / 4-Byte Address Mode (ADS=1: A31–A0, ADS=0: A23–A0)

| Command<br>*W25Q25RV/51RV/01RV/02RV* | | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|---|
| Number of Clock((IO 4-4d-4d) | | 2 | 1 / 1-1-1 | M7-0 | N dummy | 1-…Clock | MHz | MHz |
| DTR Read with Wrap[12] | | 0Eh | A31 / A23-A0 | 1 | 7 | (D7-0)… | 84 | 50 |
| Set Read Parameters (C0h) M7–0 serve as dummy bits | 0 0 0 | | A31 / A23-A0 | Disable | 8 (Def) | (D7-0)… | 84 | 50 |
| | 0 0 1 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 84 | 50 |
| | 0 1 0 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 84 | 50 |
| | 0 1 1 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 84 | 50 |
| | 1 0 0 | | A31 / A23-A0 | Disable | 10 | (D7-0)… | 84 | 50 |
| | 1 0 1 | | A31 / A23-A0 | Disable | 12 | (D7-0)… | 104 | 66 |
| | 1 1 0 | | A31 / A23-A0 | Disable | 14 | (D7-0)… | 104 | 66 |
| | 1 1 1 | | A31 / A23-A0 | Disable | 16 | (D7-0)… | 104 | 66 |
| DTR Fast Read | | 0Dh | A31 / A23-A0 | -- | 8 | (D7-0)… | 84 | 50 |
| Set Read Parameters (C0h) | 0 0 0 | | A31 / A23-A0 | - | 8 (Def) | (D7-0)… | 84 | 50 |
| | 0 0 1 | | A31 / A23-A0 | - | 8 | (D7-0)… | 84 | 50 |
| | 0 1 0 | | A31 / A23-A0 | - | 8 | (D7-0)… | 84 | 50 |
| | 0 1 1 | | A31 / A23-A0 | - | 8 | (D7-0)… | 84 | 50 |
| | 1 0 0 | | A31 / A23-A0 | - | 10 | (D7-0)… | 84 | 50 |
| | 1 0 1 | | A31 / A23-A0 | - | 12 | (D7-0)… | 104 | 66 |
| | 1 1 0 | | A31 / A23-A0 | - | 14 | (D7-0)… | 104 | 66 |
| | 1 1 1 | | A31 / A23-A0 | - | 16 | (D7-0)… | 104 | 66 |



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### 6.3.14 QPI DTR Commands Dependent in 3-Byte / 4-Byte Address Mode (ADS=1: A31–A0, ADS=0: A23–A0)

| Command *W25Q25RV/51RV/01RV/02RV* | | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|---|
| Number of Clock (IO 4-4d-4d) | | 2 | 1 / 1-1-1 | M7-0 | N dummy | 1-…Clock | MHz | MHz |
| DTR Fast Read Quad I/O | | EDh | A31 / A23-A0 | 1 | 7 | (D7-0)… | 84 | 50 |
| Set Read Parameters (C0h) M7–0 serve as dummy bits | 0 0 0 | | A31 / A23-A0 | Disable | 8 (Def) | (D7-0)… | 84 | 50 |
| | 0 0 1 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 84 | 50 |
| | 0 1 0 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 84 | 50 |
| | 0 1 1 | | A31 / A23-A0 | Disable | 8 | (D7-0)… | 84 | 50 |
| | 1 0 0 | | A31 / A23-A0 | Disable | 10 | (D7-0)… | 84 | 50 |
| | 1 0 1 | | A31 / A23-A0 | Disable | 12 | (D7-0)… | 104 | 66 |
| | 1 1 0 | | A31 / A23-A0 | Disable | 14 | (D7-0)… | 104 | 66 |
| | 1 1 1 | | A31 / A23-A0 | Disable | 16 | (D7-0)… | 104 | 66 |

### 6.3.15 QPI DTR Commands Operable in Both 3-Byte and 4-Byte Address Modes

| Command *W25Q25RV/51RV/01RV/02RV* | | Opcode | Address Bytes | Read Bypass | Dummy Cycles | Data Bytes | Aligned Address | Any Address |
|---|---|---|---|---|---|---|---|---|
| Number of Clock (IO 4-4d-4d) | | 2 | 1-1-1-1 | M7-0 | N dummy | 1-…Clock | MHz | MHz |
| DTR Fast Read I/O with 4-Byte Address | | EEh | A31-A0 | 1 | 7 | (D7-0)… | 84 | 50 |
| Set Read Parameters (C0h) M7–0 serve as dummy bits | 0 0 0 | | A31-A0 | Disable | 8 (Def) | (D7-0)… | 84 | 50 |
| | 0 0 1 | | A31-A0 | Disable | 8 | (D7-0)… | 84 | 50 |
| | 0 1 0 | | A31-A0 | Disable | 8 | (D7-0)… | 84 | 50 |
| | 0 1 1 | | A31-A0 | Disable | 8 | (D7-0)… | 84 | 50 |
| | 1 0 0 | | A31-A0 | Disable | 10 | (D7-0)… | 84 | 50 |
| | 1 0 1 | | A31-A0 | Disable | 12 | (D7-0)… | 104 | 66 |
| | 1 1 0 | | A31-A0 | Disable | 14 | (D7-0)… | 104 | 66 |
| | 1 1 1 | | A31-A0 | Disable | 16 | (D7-0)… | 104 | 66 |



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**Notes:**

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "***D7-D0***" indicate data output from the device on either 1, 2 or 4 IO pins. The output data address is increase through the clock input. " Byte fields with data in parenthesis "D7-D0" indicate data input to the device on either 1, 2 or 4 IO pins. The input data address is increase through the clock input. "
2. The Status Register contents, and Device ID will repeat continuously until /CS terminates the instruction.
3. At least one byte of data input is required for Page Program, Quad Page Program, Write Buffer and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. Security Register Address:
   Security Register 1: A23-16 = 00h; A15-8 = 10h; A7-0 = byte address
   Security Register 2: A23-16 = 00h; A15-8 = 20h; A7-0 = byte address
   Security Register 3: A23-16 = 00h; A15-8 = 30h; A7-0 = byte address
5. Dual SPI address input format:
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1
6. Dual SPI data input/output format:
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)
7. Quad SPI address input format:
   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3

   Set Burst with Wrap input format:
   IO0 = x, x, x, x, x, x, W4, x
   IO1 = x, x, x, x, x, x, W5, x
   IO2 = x, x, x, x, x, x, W6, x
   IO3 = x, x, x, x, x, x, x, x
8. Quad SPI data input/output format:
   IO0 = (D4, D0, …..)
   IO1 = (D5, D1, …..)
   IO2 = (D6, D2, …..)
   IO3 = (D7, D3, …..)
9. Fast Read Quad I/O data output format:
   IO0 = (x, x, x, x, D4, D0, D4, D0)
   IO1 = (x, x, x, x, D5, D1, D5, D1)
   IO2 = (x, x, x, x, D6, D2, D6, D2)
   IO3 = (x, x, x, x, D7, D3, D7, D3)
10. QPI Command, Address, Data input/output format:

| *CLK # 0* | *1* | *2* | *3* | *4* | *5* | *6* | *7* | *8* | *9* | *10* | *11* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| IO0 = C4, | C0, | A20, | A16, | A12, | A8, | A4, | A0, | D4, | D0, | D4, | D0 |
| IO1 = C5, | C1, | A21, | A17, | A13, | A9, | A5, | A1, | D5, | D1, | D5, | D1 |
| IO2 = C6, | C2, | A22, | A18, | A14, | A10, | A6, | A2, | D6, | D2, | D6, | D2 |
| IO3 = C7, | C3, | A23, | A19, | A15, | A11, | A7, | A3, | D7, | D3, | D7, | D3 |

11. The number of dummy clocks for QPI Fast Read, SPI/QPI Fast Read Quad I/O, SPI/QPI Read Checksum & QPI Burst Read with Wrap, Read Checksum & QPI Burst Read with Wrap is controlled by read parameter P7 – P4.
12. The wrap around length for QPI Burst Read with Wrap is controlled by read parameter P3 – P0.
13. The first dummy is M7-M0 should be set to FFh/Fxh; once read command bypass mode is not used.
14. The Buffer Address (BA) field is used to access the contents of the Page Buffer, which holds a total of 256 bytes.

    Clear Buffer 81h: BA31-26 = xxh;BA25-24 = Die Select / BA23-16 = xxh; BA15-8 = xxh; BA7-0 = xxh
    Write Buffer 82h: BA31-26 = xxh;BA25-24 = Die Select / BA23-16 = xxh; BA15-8 = xxh; BA7-0 = byte address
    Read Buffer 83h: BA31-26 = xxh;BA25-24 = Die Select / BA23-16 = xxh; BA15-8 = xxh; BA7-0 = byte address


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## 6.4 Instruction Descriptions

### 6.4.1 Write Enable (06h)

The Write Enable instruction Figure 6.4 sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Registers instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

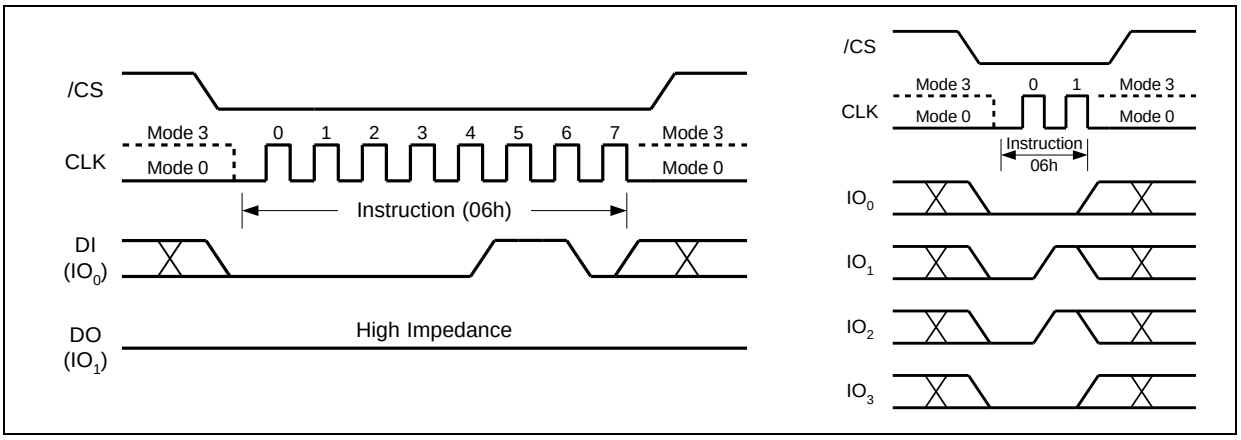



Figure 6.4.1 Write Enable instruction

### 6.4.2 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 7.1 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h/31h/11h) instruction. The Write Enable for Volatile Status Register Instruction-Figure 6.4.2 will not set the Write Enable Latch (WEL) bit. Only the Write Status Register instruction can change the volatile Status Register bit values.

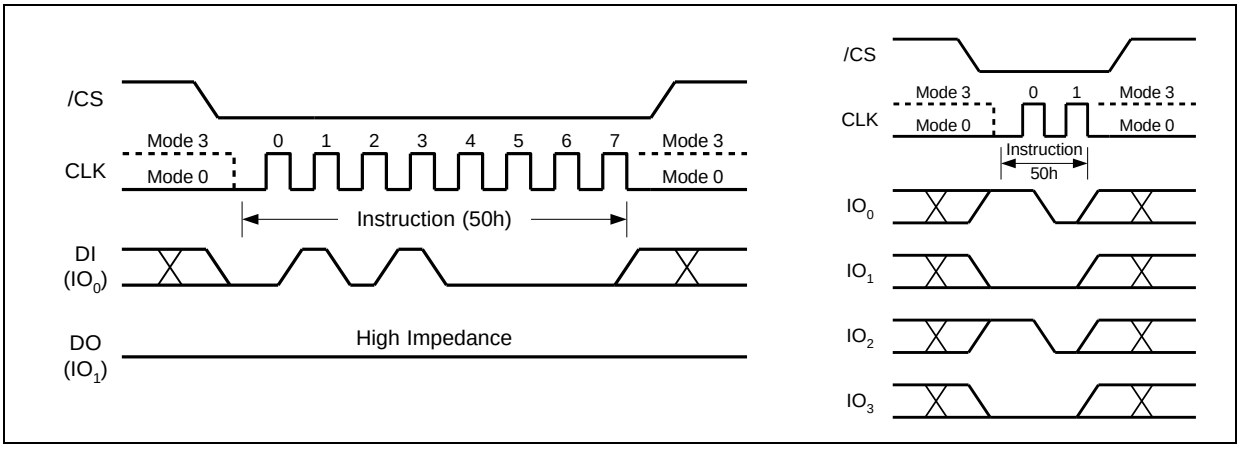



Figure 6.4.2 Write Enable for Volatile Status Register Instruction for SPI Mode (left) or QPI Mode (right)



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### 6.4.3 Write Disable (04h)

The Write Disable instruction (Figure 6.4.3) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Registers, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase and Reset instructions.

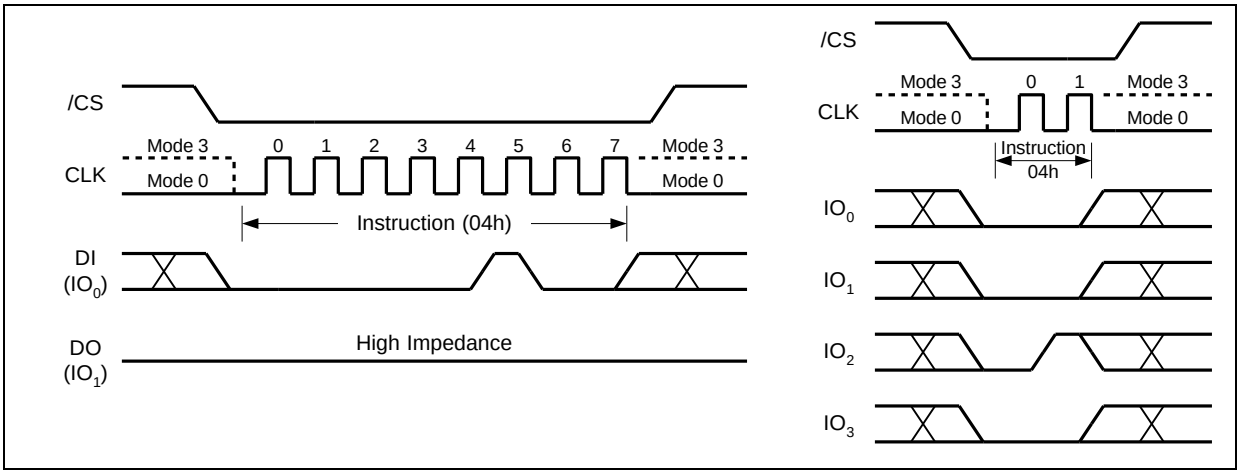



Figure 6.4.3 Write Disable Instruction for SPI Mode (left) or QPI Mode (right)

### 6.4.4 Read Status Register-1 (05h), Status Register-2 (35h) & Status Register-3 (15h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” for Status Register-1, “35h” for Status Register-2 or “15h” for Status Register-3 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with the most significant bit (MSB) first as shown in Figure 6.4.4..

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 6.4.4 The instruction is completed by driving /CS high.

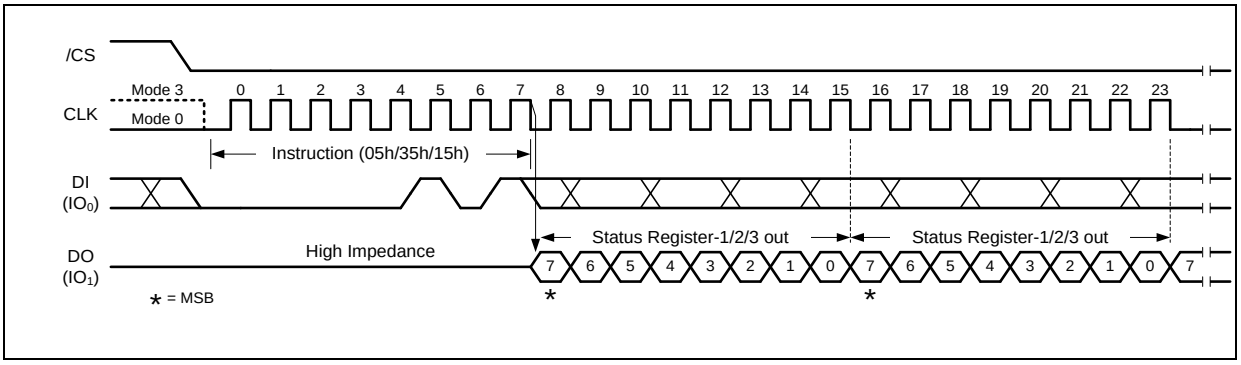



Figure 6.4.4a Read Status Register Instruction (SPI Mode)



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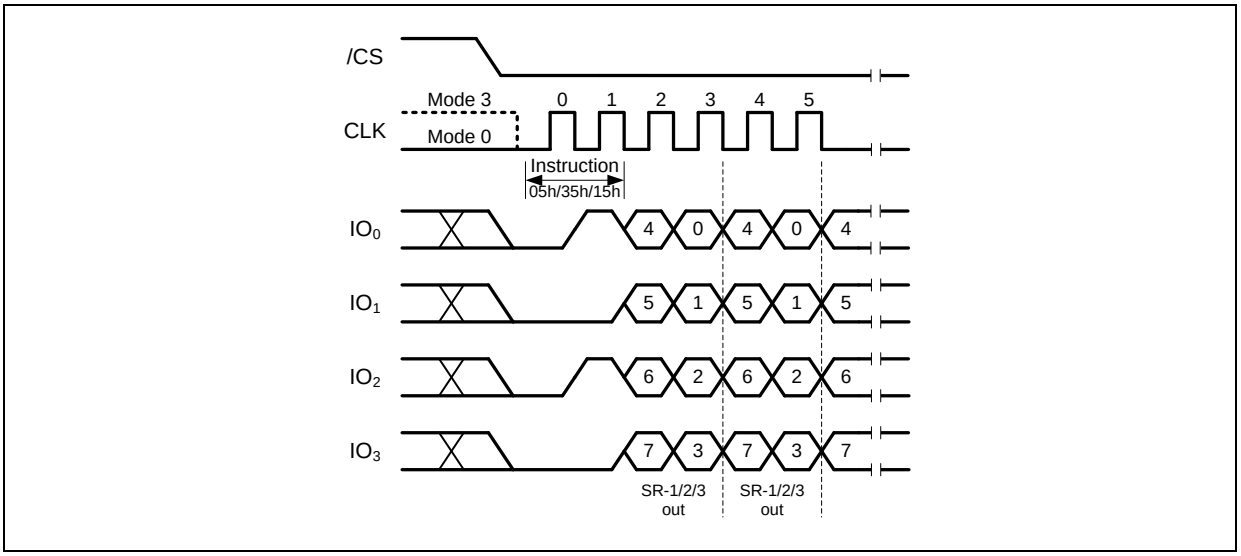



Figure 6.4.4b. Read Status Register Instruction (QPI Mode)

### 6.4.5 Write Status Register-1 (01h), Status Register-2 (31h) & Status Register-3 (11h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include SRP, TB, BP[3:0] in Status Register-1; CMP, LB[3:1], QE, SRL in Status Register-2; HOLD/RST, DRV1, DRV0, WPS & ADP in Status Register-3. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB[3:1] are non-volatile OTP bits. Once set to 1, the bits cannot be cleared to 0.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code "01h/31h/11h", and then writing the status register data byte as illustrated in Figure 6.4.5.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). However, SRL and LB[3:1] cannot be changed from "1" to "0" because of the OTP protection for these bits. Upon power off or the execution of a Software/Hardware Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

During the non-volatile Status Register write operation (06h combined with 01h/31h/11h), after /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of $t_W$ (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h/31h/11h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of $t_{SHSL2}$ (See AC Characteristics). The BUSY bit will remain 0 during the Status Register bit refresh period.

The Write Status Register instruction can be used in both SPI mode and QPI mode. However, the QE bit cannot be written to when the device is in the QPI mode, because QE=1 is required for the device to enter and operate in the QPI mode.



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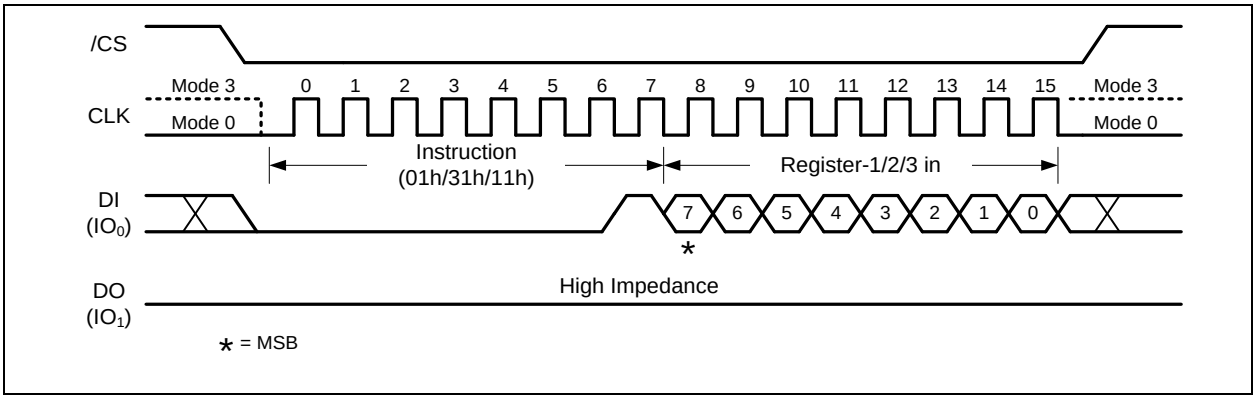



Figure 6.4.5a. Write Status Register-1/2/3 Instruction (SPI Mode)

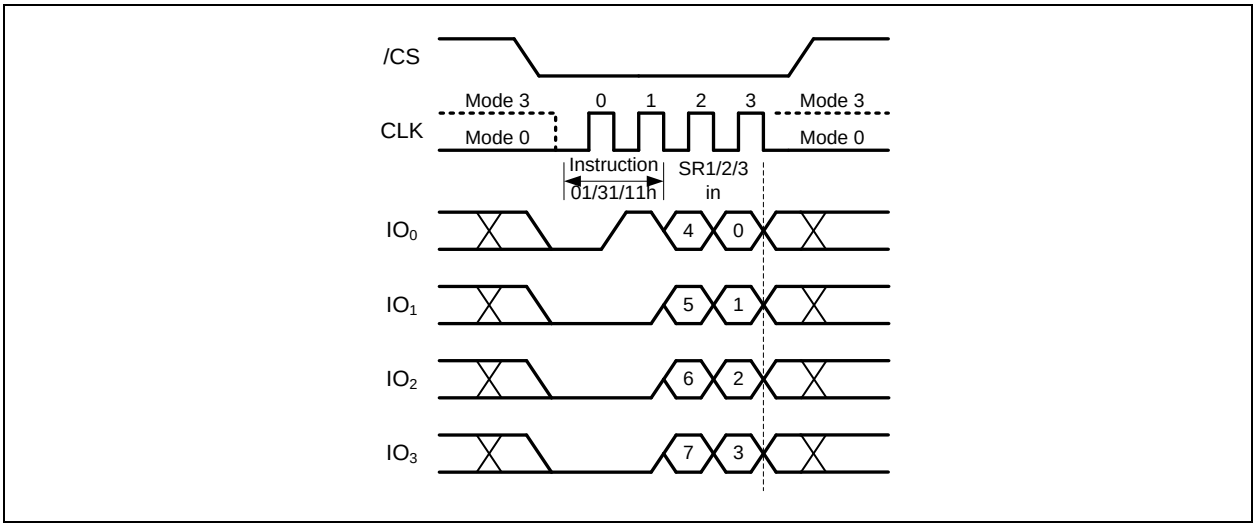



Figure 6.4.5b. Write Status Register-1/2/3 Instruction (QPI Mode)



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### 6.4.6 Read Extended Address Register (C8h)

When the device is in the 3-Byte Address Mode, the Extended Address Register is used as the 4th address byte A[31:24] to access memory regions beyond 128Mb. The Read Extended Address Register instruction is entered by driving /CS low and shifting the instruction code "C8h" into the DI pin on the rising edge of CLK. The Extended Address Register bits are then shifted out on the DO pin at the falling edge of CLK with the most significant bit (MSB) first as shown in Figure 6.4.6.

When the device is in the 4-Byte Address Mode, the Extended Address Register is not used.

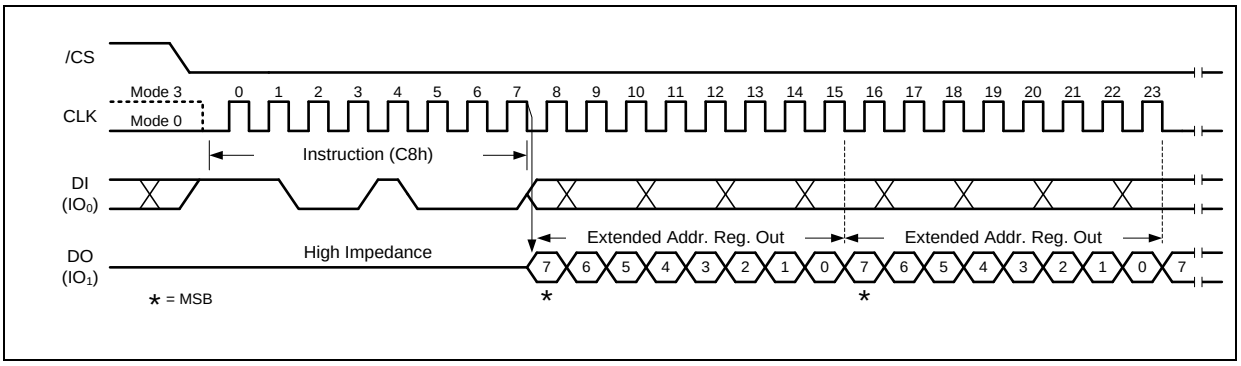



Figure 6.4.6 a. Read Extended Address Register Instruction (SPI Mode)

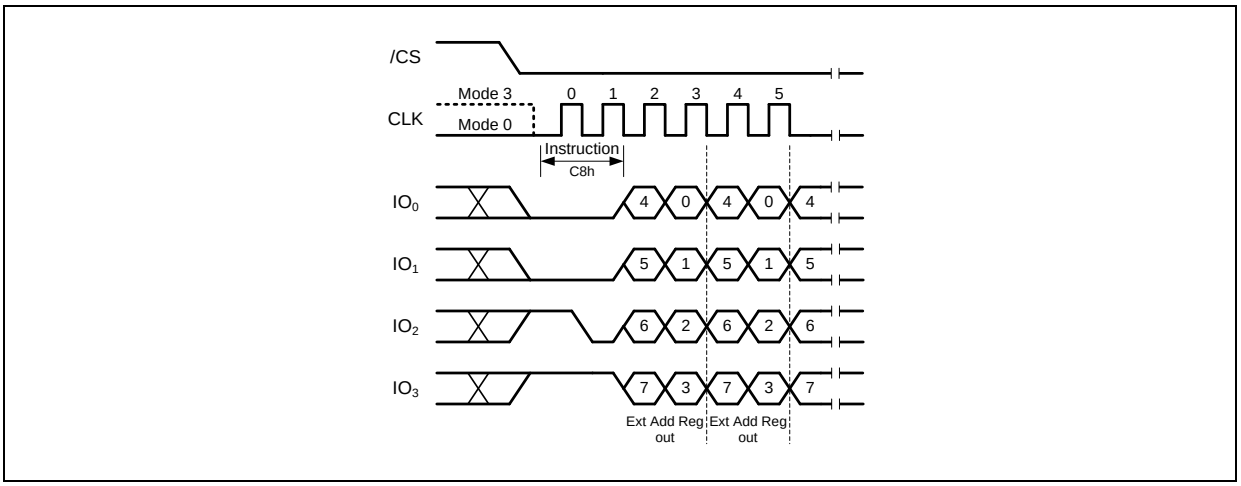



Figure 6.4.6 b. Read Extended Address Register Instruction (QPI Mode)



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### 6.4.7 Write Extended Address Register (C5h)

The Extended Address Register is a volatile register that stores the 4th byte address (A31-A24) when the device is operating in the 3-Byte Address Mode (ADS=0). To write the Extended Address Register bits, a Write Enable (06h) instruction must previously have been executed for the device to accept the Write Extended Address Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code "C5h", and then writing the Extended Address Register data byte as illustrated in Figure 6.4.7.

Upon power up or the execution of a Software/Hardware Reset, the Extended Address Register bit values will be cleared to 0.

The Extended Address Register is only effective when the device is in the 3-Byte Address Mode. When the device operates in the 4-Byte Address Mode (ADS=1), any command with address input of A31-A24 will replace the Extended Address Register values. It is recommended to check and update the Extended Address Register if necessary when the device is switched from 4-Byte to 3-Byte Address Mode.

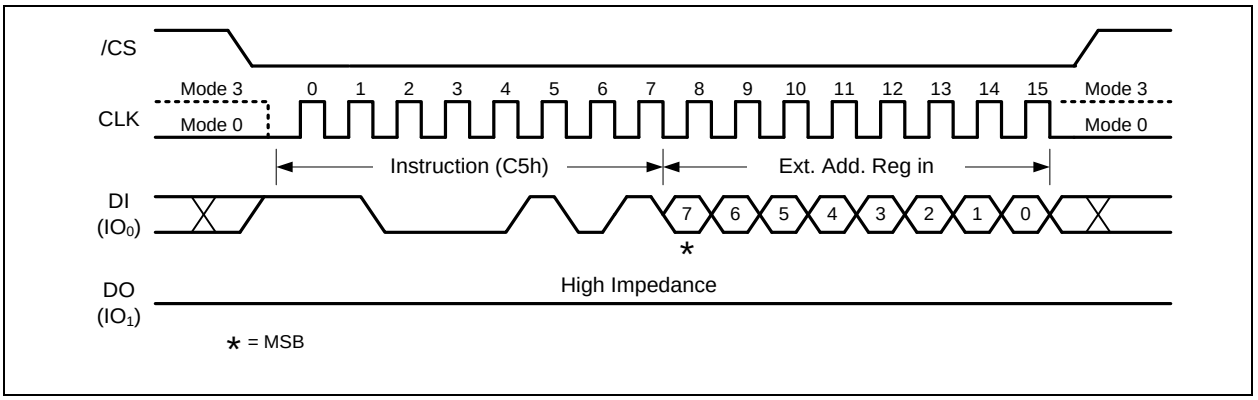



Figure 6.4.7a. Write Extended Address Register Instruction (SPI Mode)

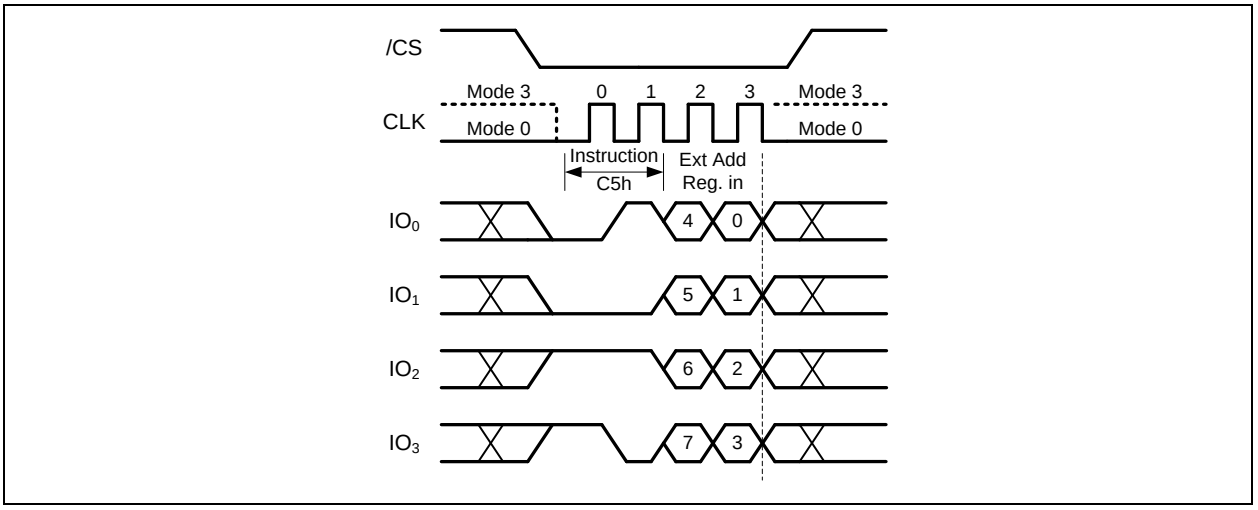



Figure 6.4.7b. Write Extended Address Register Instruction (QPI Mode)



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### 6.4.8 Enter 4-Byte Address Mode (B7h)

The Enter 4-Byte Address Mode instruction will allow 32-bit address (A31-A0) to be used to access the memory array beyond 128Mb. The Enter 4-Byte Address Mode instruction is entered by driving /CS low, shifting the instruction code “B7h” into the DI pin and then driving /CS high.

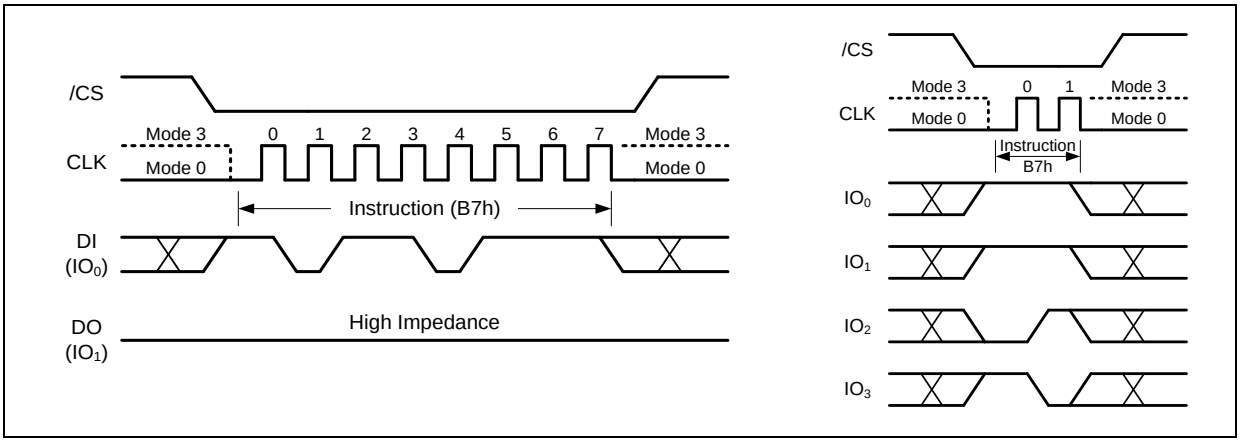



Figure 6.4.8. Enter 4-Byte Address Mode instruction for SPI Mode (left) or QPI Mode (right)

### 6.4.9 Exit 4-Byte Address Mode (E9h)

In order to be backward compatible, the Exit 4-Byte Address Mode instruction will only allow 24-bit address (A23-A0) to be used to access the memory array up to 128Mb. The Extended Address Register must be used to access the memory array beyond 128Mb. The Exit 4-Byte Address Mode instruction is entered by driving /CS low, shifting the instruction code “E9h” into the DI pin and then driving /CS high.

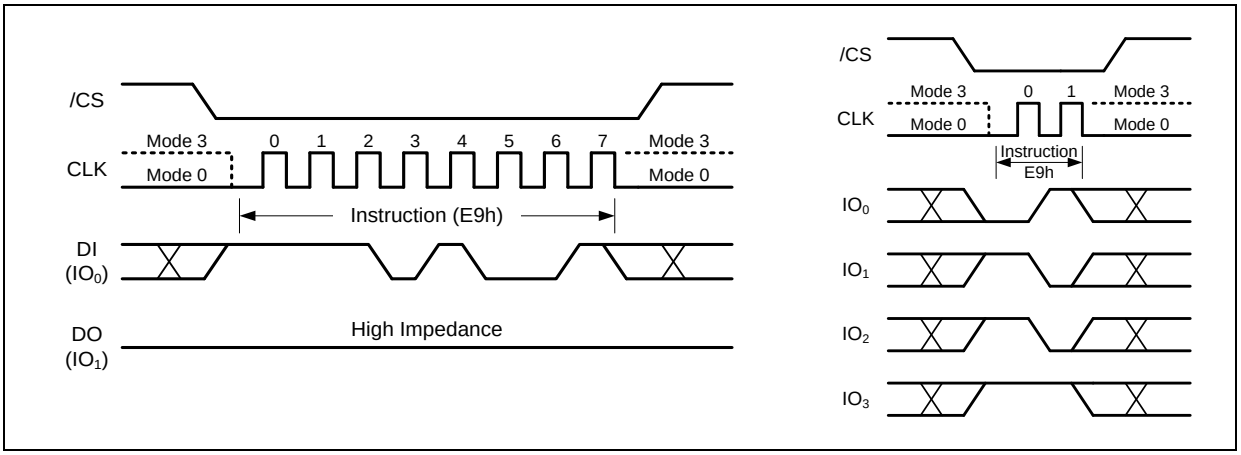



Figure 6.4.9. Exit 4-Byte Address Mode instruction for SPI Mode (left) or QPI Mode (right)



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### 6.4.10 Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 32/24-bit address (A31/A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown below. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1), the instruction is ignored and will not have any effect on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of $f_R$ (see AC Electrical Characteristics).

The Read Data (03h) instruction is only supported in Standard SPI mode.

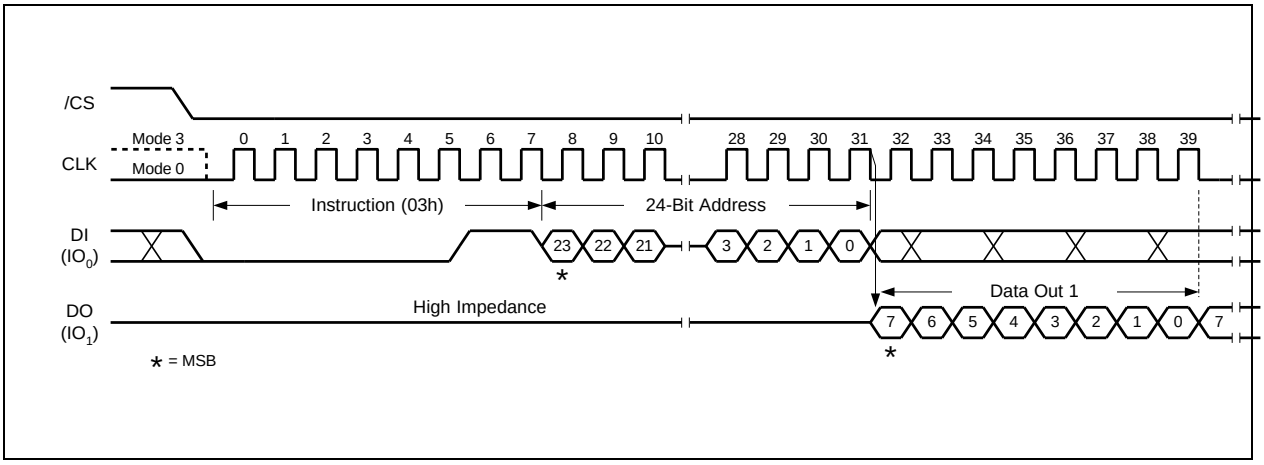



Figure 6.4.10. Read Data Instruction (SPI Mode only)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.11 Read Data with 4-Byte Address (13h)

The Read Data with 4-Byte Address instruction is similar to the Read Data (03h) instruction. Instead of a 24-bit address, a 32-bit address is needed following the instruction code 13h. Whether the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Read Data with 4-Byte Address instruction will always require 32-bit address to access the entire 256M-bit ~2G-bit memory.

The Read Data with 4-Byte Address instruction sequence is shown below. If this instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1), the instruction is ignored and will not have any effect on the current cycle. The Read Data with 4-Byte Address instruction allows clock rates from D.C. to a maximum of $f_R$ (see AC Electrical Characteristics).

The Read Data with 4-Byte Address (13h) instruction is only supported in Standard SPI mode.

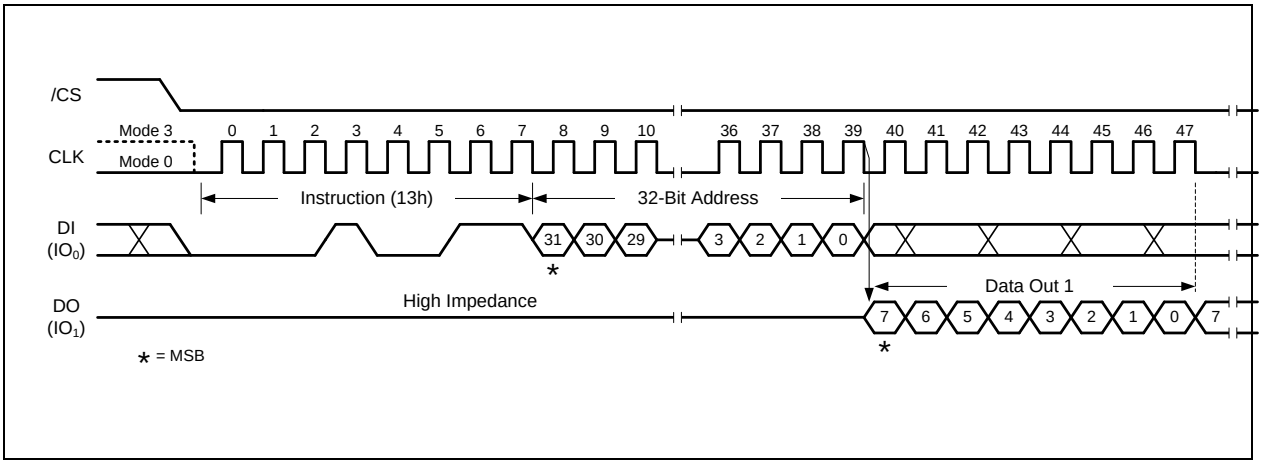



Figure 6.4.11. Read Data with 4-Byte Address Instruction (SPI Mode only)



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### 6.4.12 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see 7.5 AC Measurement Conditions). This is accomplished by adding eight "dummy" clocks after the 24/32-bit address as shown in Figure 6.4.12. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks, the data value on the DO pin is a "don't care".

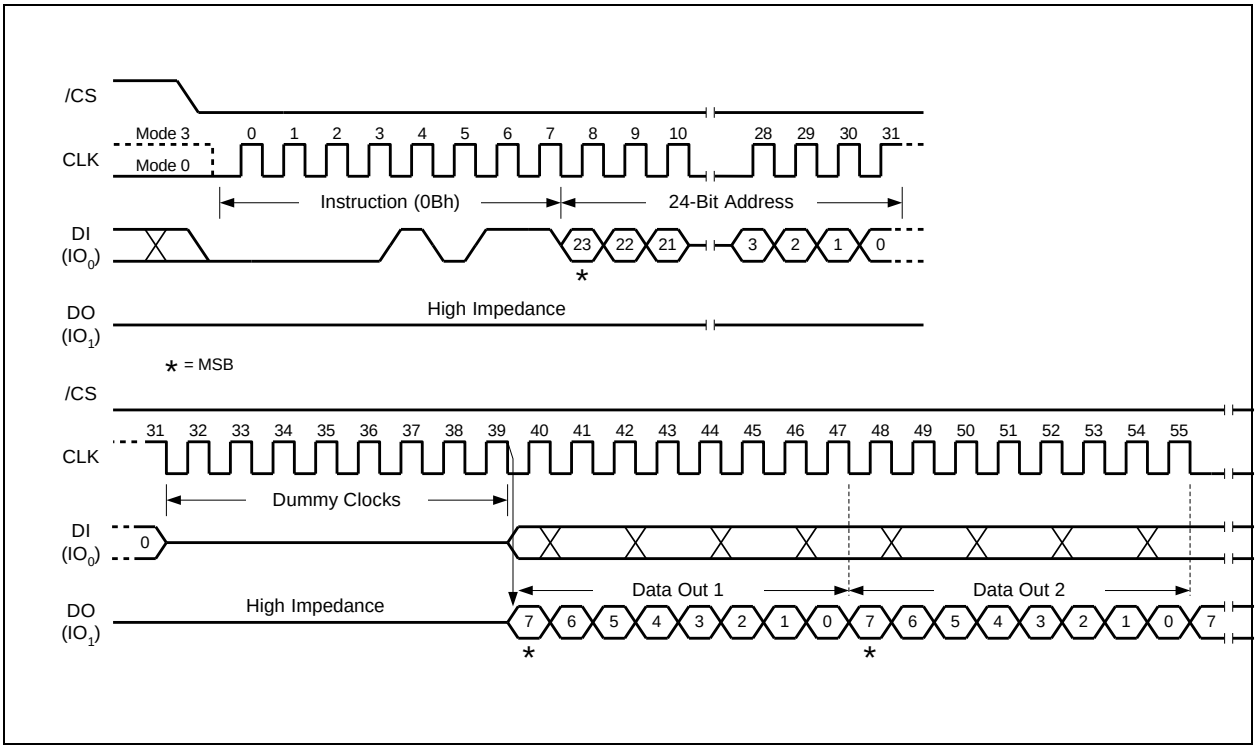



Figure 6.4.12a. Fast Read Instruction (SPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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**Fast Read (0Bh) in QPI Mode**

The Fast Read instruction is also supported in QPI mode. When QPI mode is enabled, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[6:4] setting, the number of dummy clocks can be configured as either 6, 8, 10, 12, 14 or 16. The default number of dummy clocks upon power up or after a Reset instruction is 6.

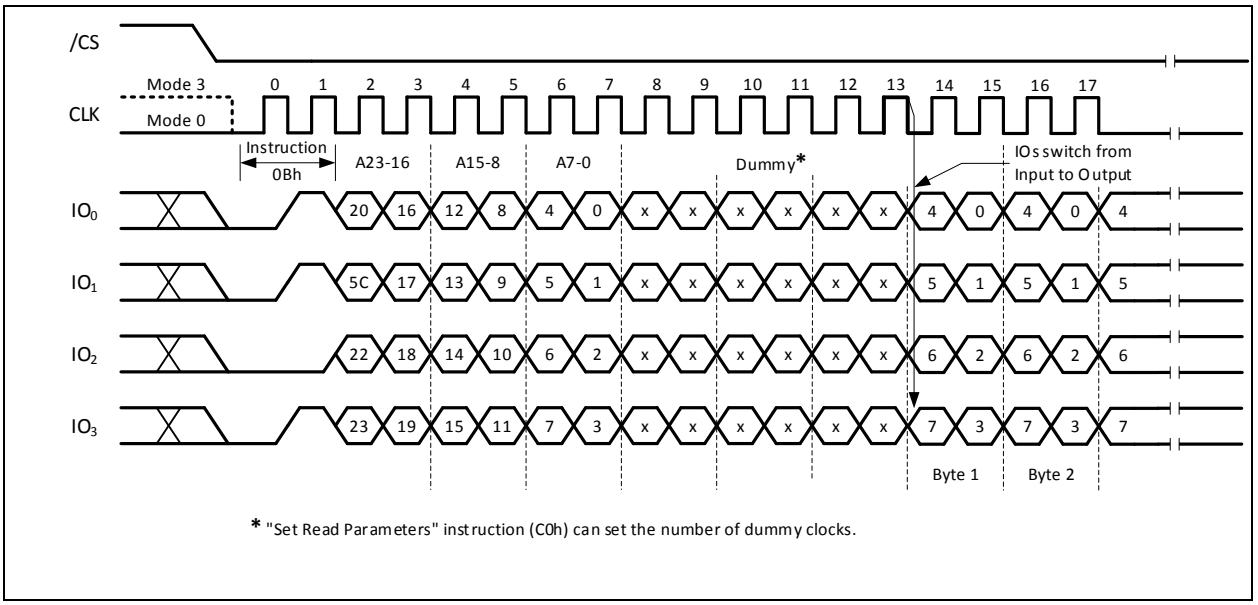



Figure 6.4.12b. Fast Read Instruction (QPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.13 DTR Fast Read (0Dh)

The DTR Fast Read instruction is similar to the Fast Read instruction except that the 24/32-bit address input and the data output require DTR (Double Transfer Rate) operation. This is accomplished by adding six “dummy” clocks after the 24/32-bit address as shown below. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks, the data value on the DO pin is a “don’t care”.

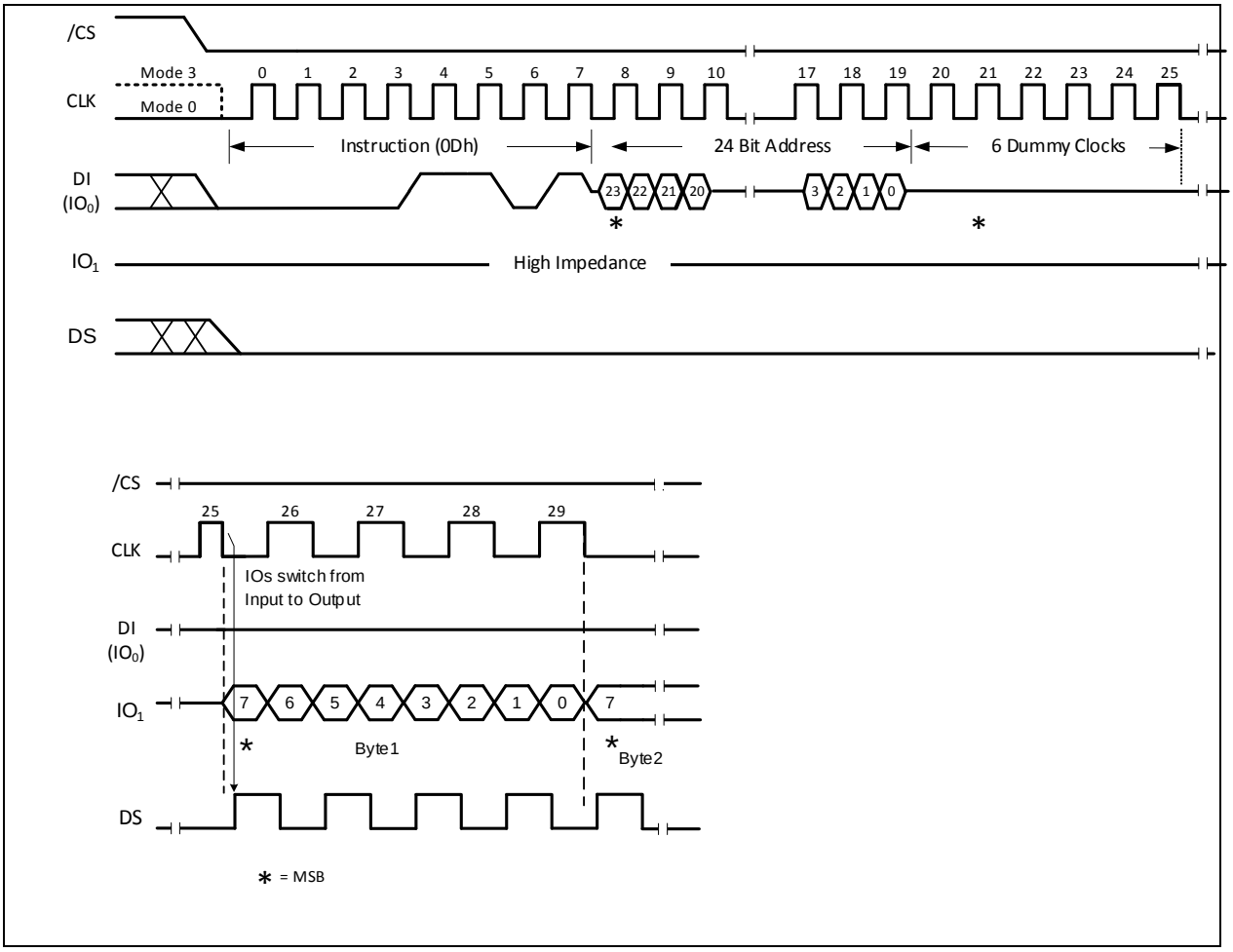



Figure 6.4.13a. DTR Fast Read Instruction (SPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### DTR Fast Read (0Dh) in QPI Mode

The DTR Fast Read instruction is also supported in QPI mode.

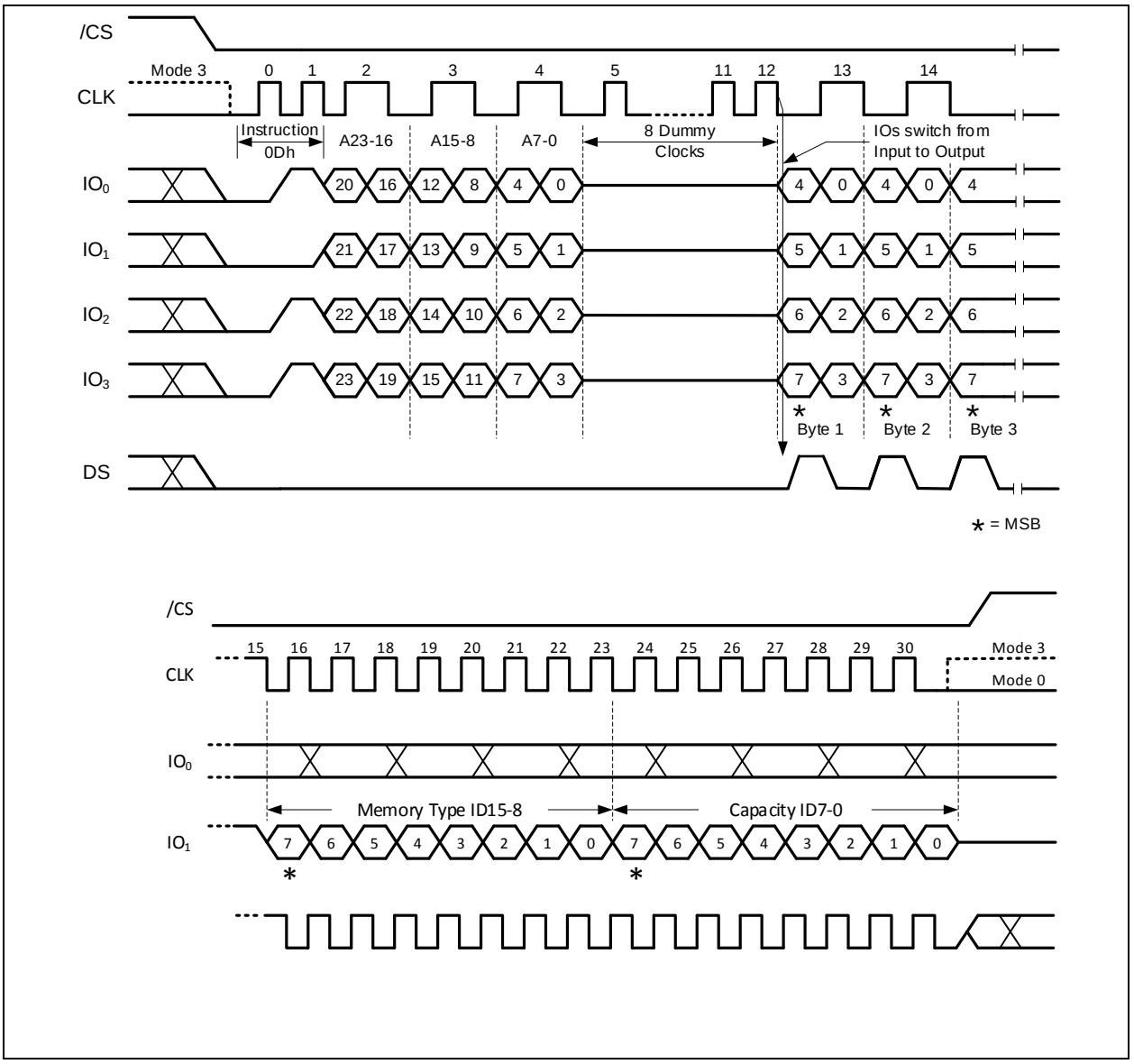



Figure 6.4.13b. DTR Fast Read Instruction (QPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.14 Fast Read with 4-Byte Address (0Ch)

The Fast Read with 4-Byte Address instruction is similar to the Fast Read instruction except that it requires a 32-bit address instead of a 24-bit address. Whether, the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Read Data with 4-Byte Address instruction will always require a 32-bit address to access the entire 256M-bit ~2G-bit memory.

The Fast Read with 4-Byte Address (0Ch) instruction is only supported in Standard SPI mode. In QPI mode, the instruction code 0Ch is used for the “Burst Read with Wrap” instruction.

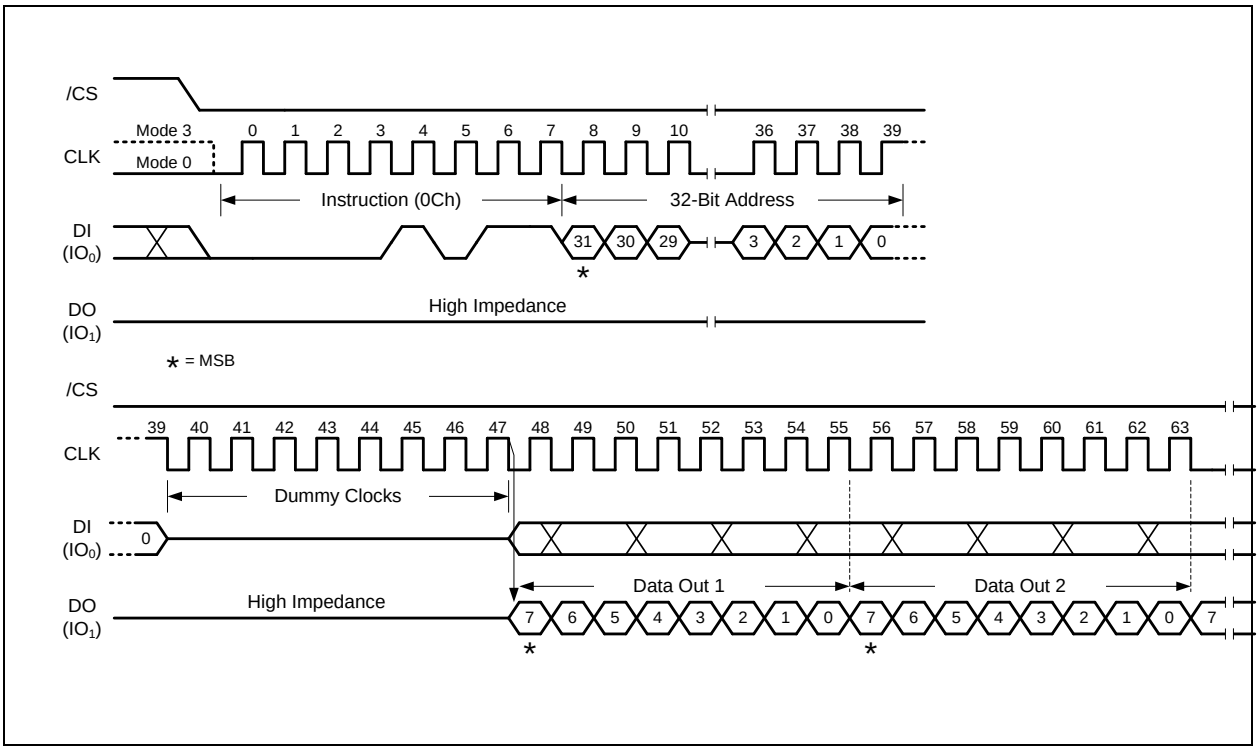



Figure 6.4.14. Fast Read with 4-Byte Address Instruction (SPI Mode only)



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### 6.4.15 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; $IO_0$ and $IO_1$. This allows data to be transferred at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24/32-bit address as shown in below. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the $IO_0$ pin should be high-impedance prior to the falling edge of the first data out clock.

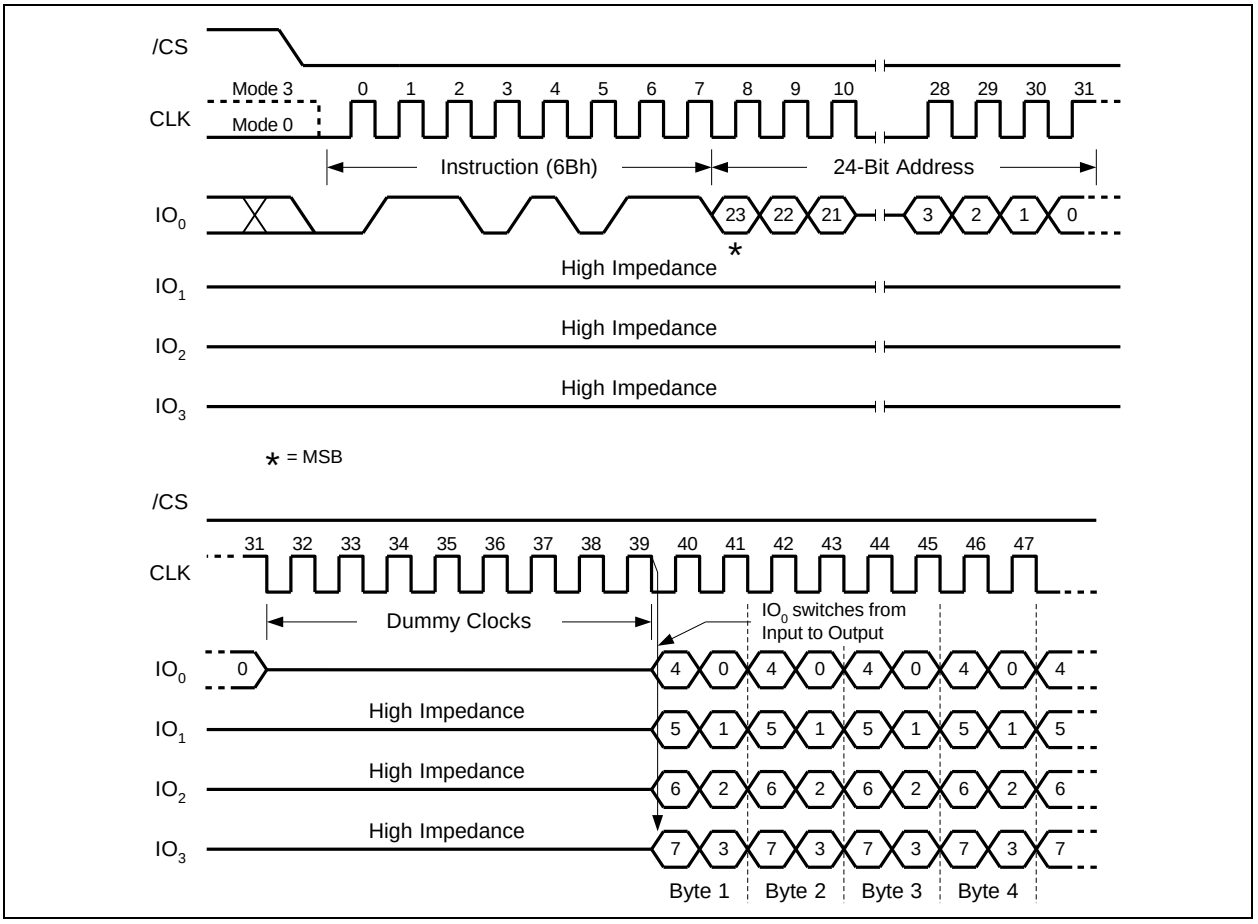



Figure 6.4.15. Fast Read Dual Output Instruction (SPI Mode only)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.16 Fast Read Dual Output with 4-Byte Address (3Ch)

The Fast Read Dual Output with 4-Byte Address instruction is similar to the Fast Read Dual Output instruction except that it requires a 32-bit address instead of a 24-bit address. Whether, the device is operating in a 3-Byte Address Mode or a 4-byte Address Mode, the Fast Read Dual Output with 4-Byte Address instruction will always require a 32-bit address to access the entire 256M-bit ~2G-bit memory.

The Fast Read Dual Output with 4-Byte Address (3Ch) instruction is only supported in Standard SPI mode.

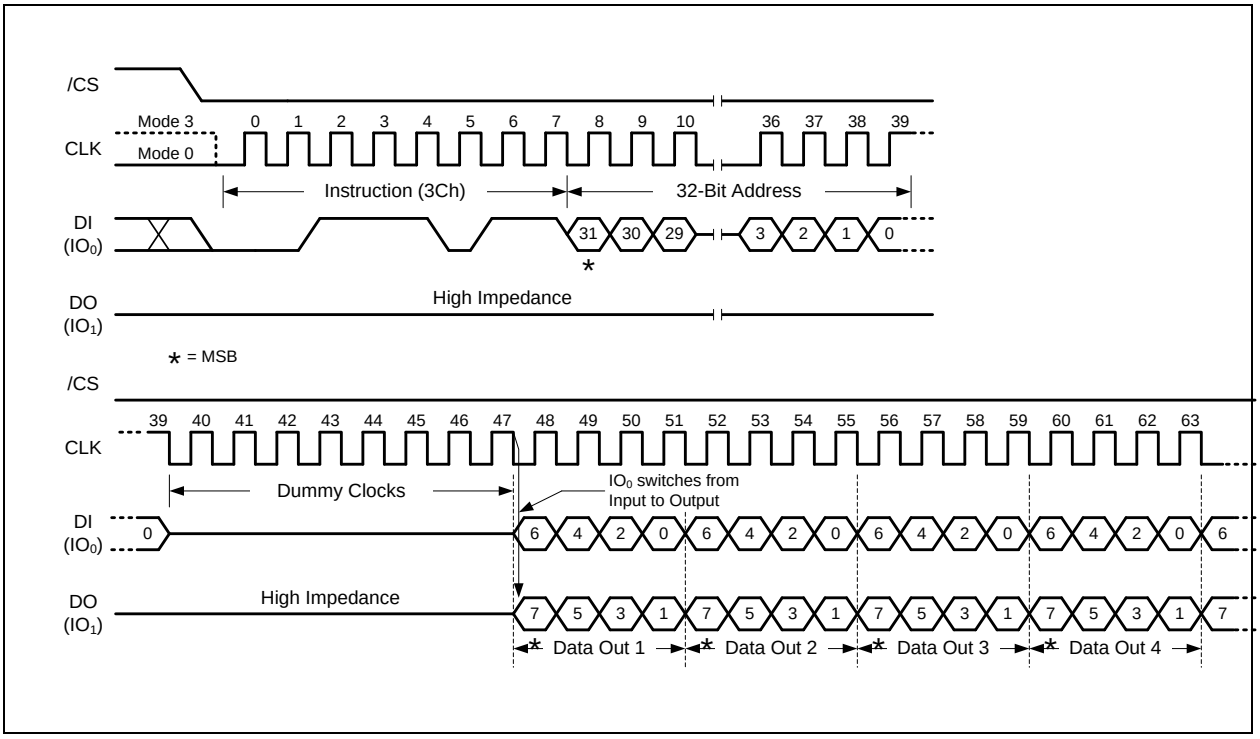



Figure 6.2.16. Fast Read Dual Output with 4-Byte Address Instruction (SPI Mode only)



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### 6.4.17 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, $IO_0$, $IO_1$, $IO_2$, and $IO_3$. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the Fast Read Quad Output Instruction. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24/32-bit address as shown in Figure 6.4.17. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

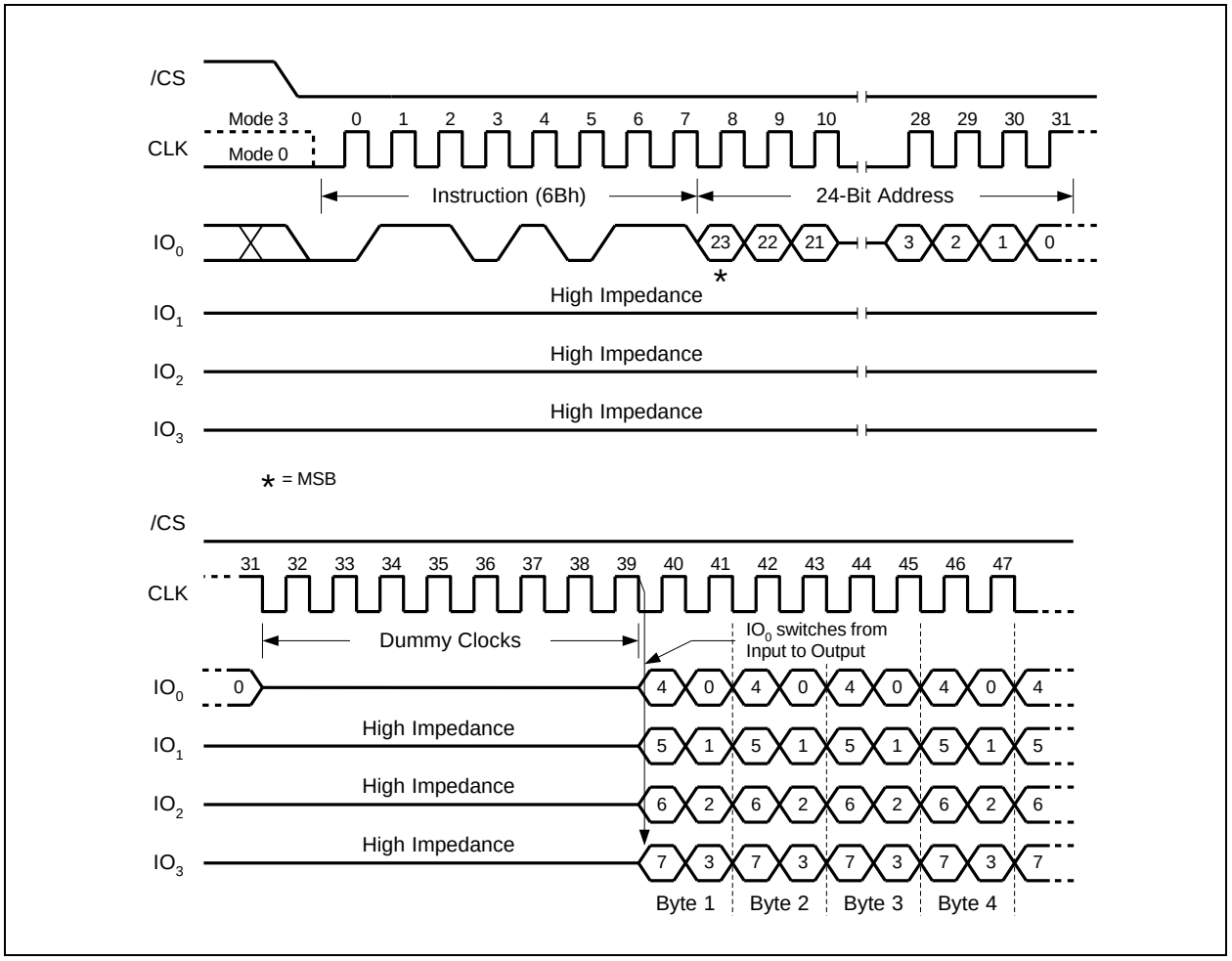



Figure 6.4.17. Fast Read Quad Output Instruction (SPI Mode only)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.18 Fast Read Quad Output with 4-Byte Address (6Ch)

The Fast Read Quad Output with 4-Byte Address instruction is similar to the Fast Read Quad Output instruction except that it requires a 32-bit address instead of a 24-bit address. Whether the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Quad Output with 4-Byte Address instruction will always require a 32-bit address to access the entire 256M-bit ~2G-bit memory.

The Fast Read Quad Output with 4-Byte Address (6Ch) instruction is only supported in Standard SPI mode.

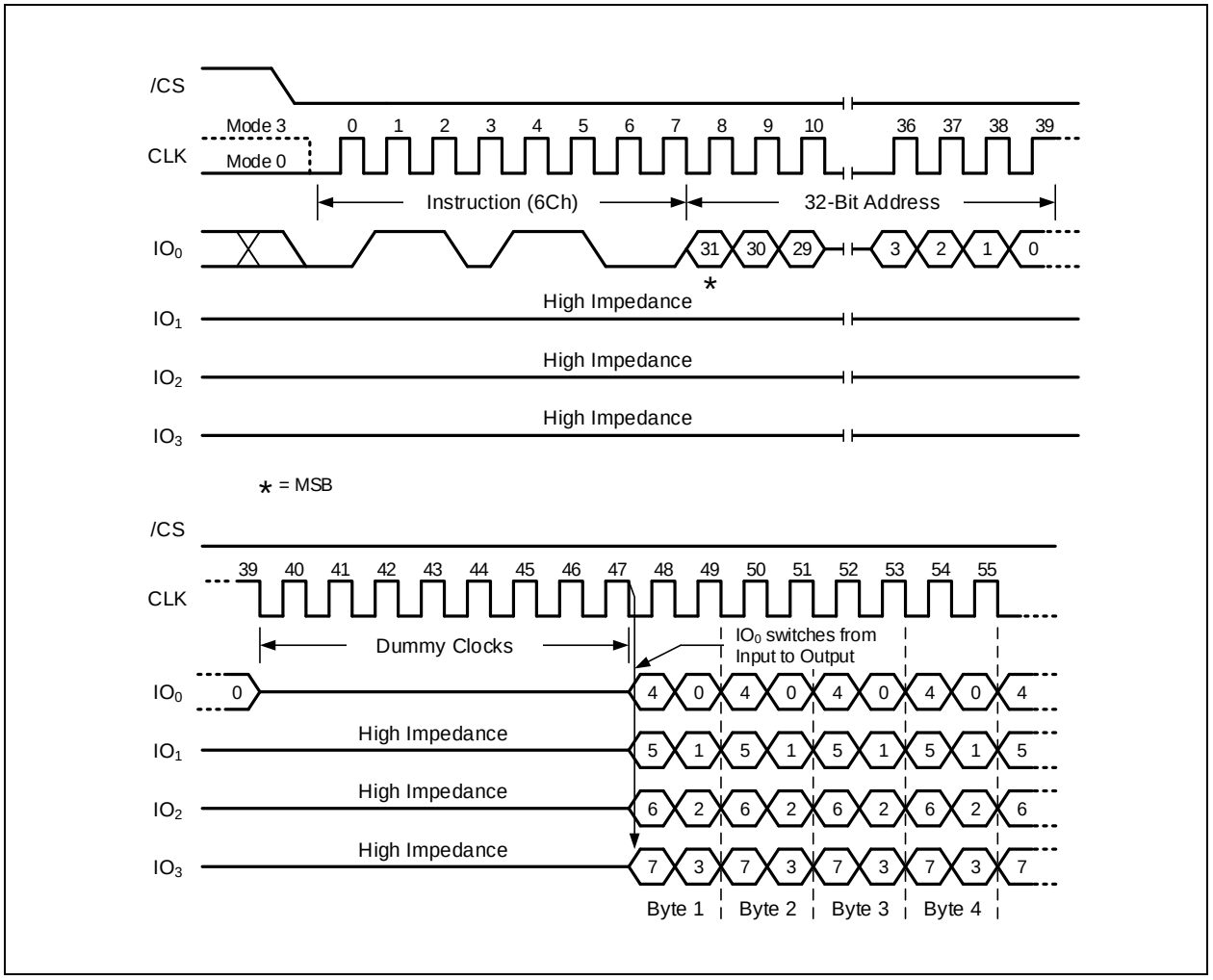



Figure 6.4.18. Fast Read Quad Output with 4-Byte Address Instruction (SPI Mode only)



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### 6.4.19 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, $IO_0$ and $IO_1$. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23/A31-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Similar to the Fast Read Dual Output (3Bh) instruction, the Fast Read Dual I/O instruction can operate at the highest possible frequency of $F_R$ (see AC Electrical Characteristics). This is accomplished by adding four "dummy" clocks after the 24/32-bit address as shown in Figure 6.2.19a. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the $IO_0$ pin should be high-impedance prior to the falling edge of the first data out clock.

**Fast Read Dual I/O with "Read Command Bypass Mode"**

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the Read Command Bypass Mode bits (M7-0) after the input Address bits (A23-0), as shown in Figure 6.2.19b. The upper nibble (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the Read Command Bypass Mode bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in Figure 6.4.19. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the Read Command Bypass Mode bits M5-4 do not equal (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh on IO0 for the next instruction (16 clocks), to ensure M4 = 1 and return the device to normal operation.

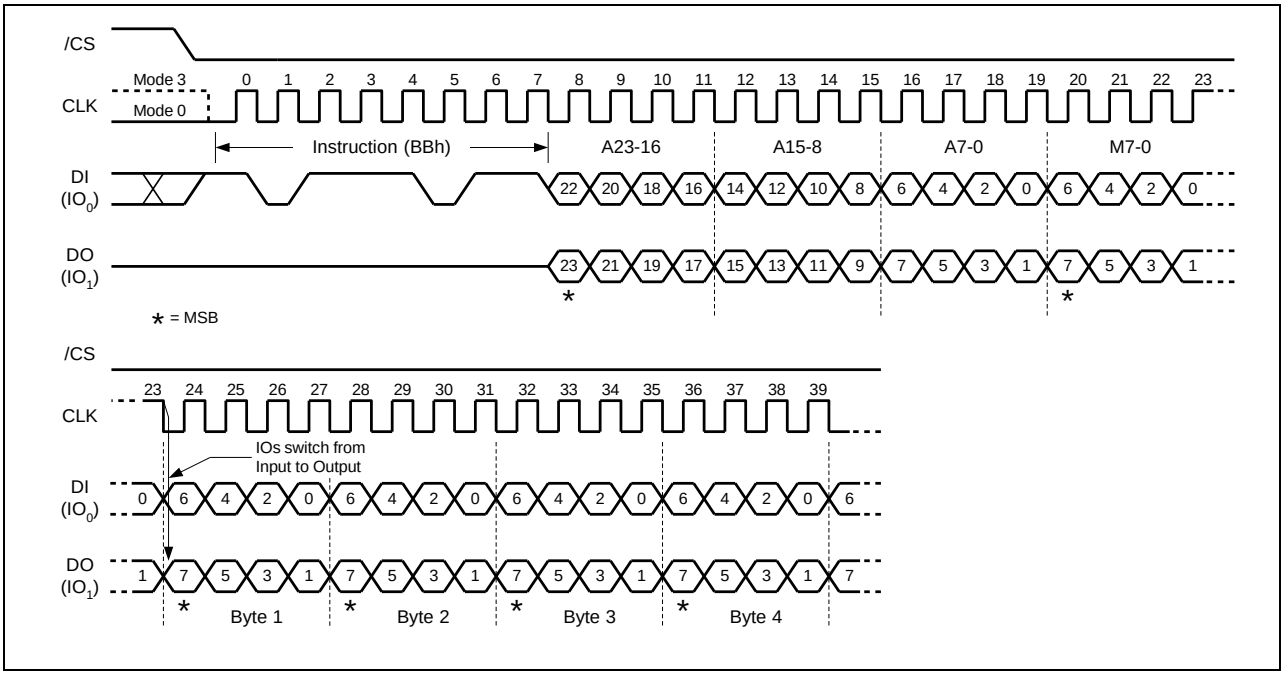



Figure 6.4.19a. Fast Read Dual I/O (Initial instruction or previous M5-4¹10, SPI Mode only)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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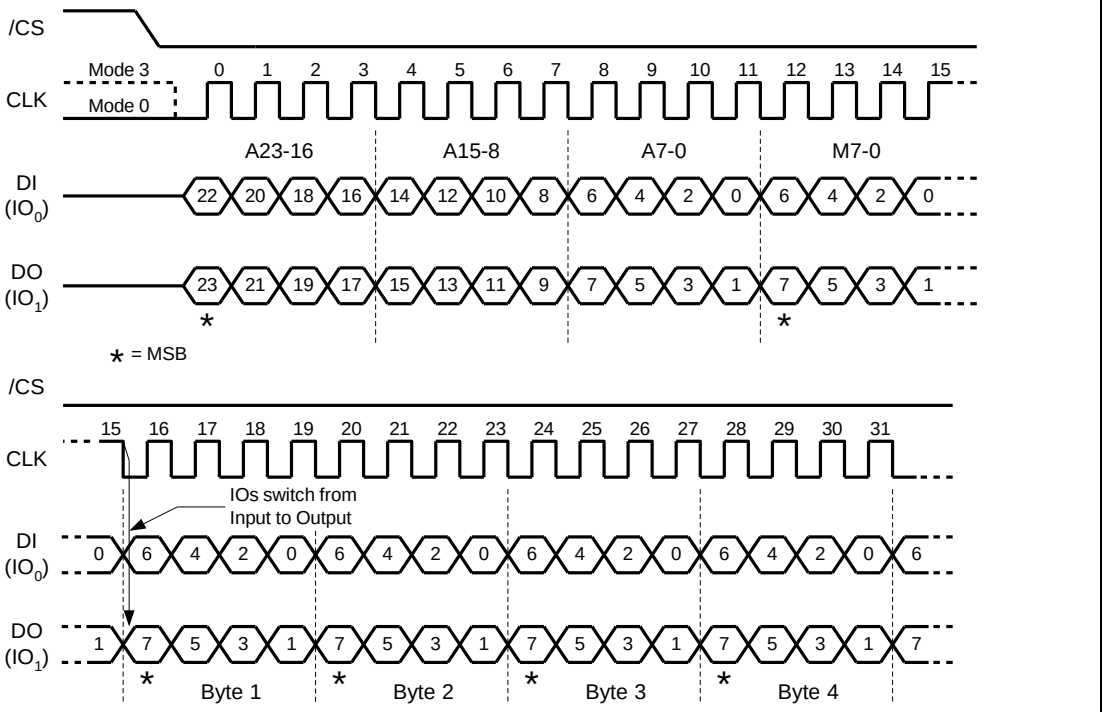



Figure 6.4.19b. Fast Read Dual I/O (Previous instruction set M5-4=10, SPI Mode only)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.20 DTR Fast Read Dual I/O (BDh)

The DTR Fast Read Dual I/O (BDh) instruction allows for improved random access while maintaining two IO pins, $IO_0$ and $IO_1$. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23/A31-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

**DTR Fast Read Dual I/O with (Read Command Bypass Mode)**

The DTR Fast Read Dual I/O instruction can further reduce instruction overhead through setting the Read Command Bypass Mode bits (M7-0) after the input Address bits (A23-0), as shown in Figure 6.2.20a. The upper nibble (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the Read Command Bypass Mode bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in Figure 6.2.20b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the Read Command Bypass Mode bits M5-4 do not equal (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh/FFFFFh on IO0 for the next instruction (16/20 clocks), to ensure M4 = 1 and return the device to normal operation.

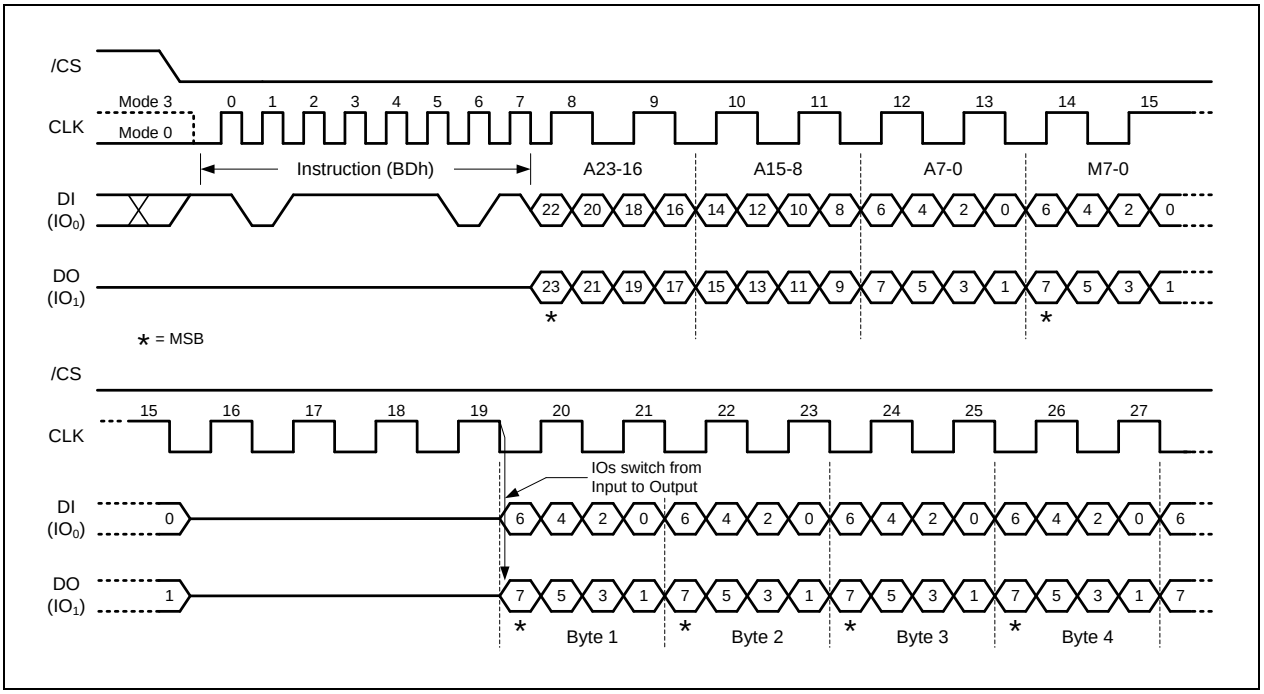



Figure 6.4.20a. DTR Fast Read Dual I/O (Initial instruction or previous M5-4¹10, SPI Mode only)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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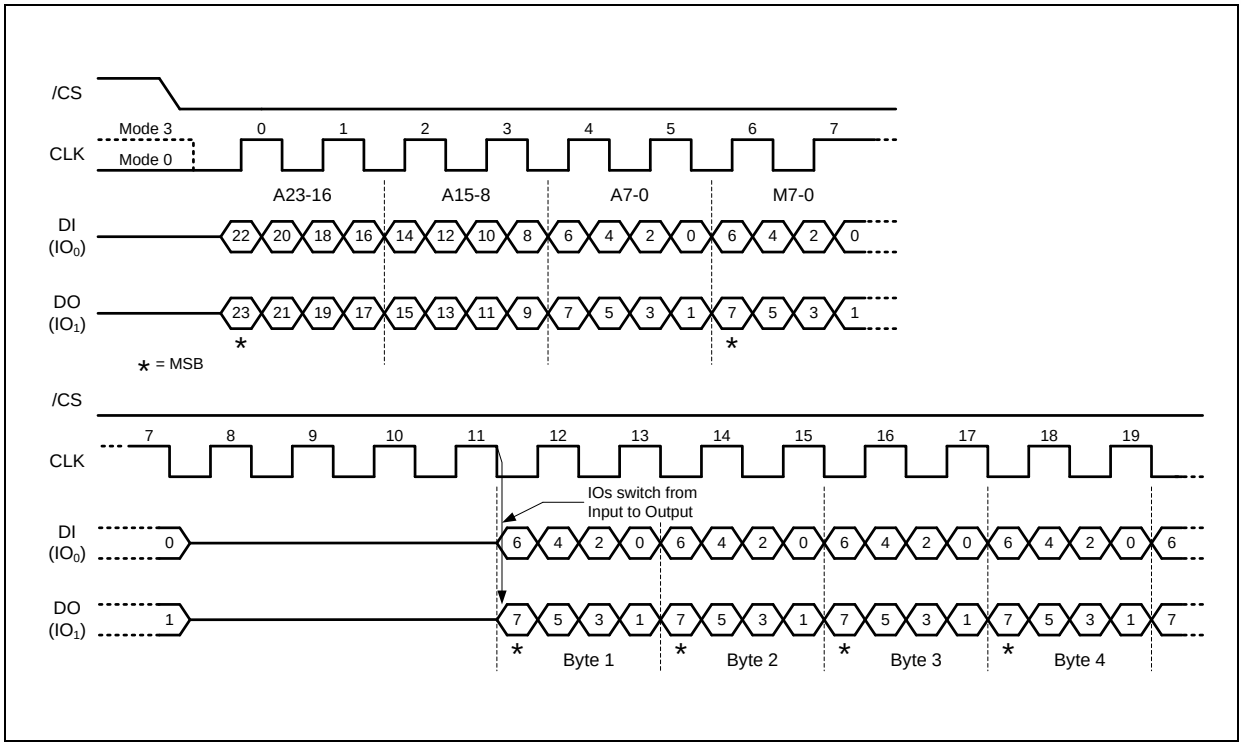



Figure 6.4.20b. DTR Fast Read Dual I/O (Previous instruction set M5-4=10, SPI Mode only)



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### 6.4.21 Fast Read Dual I/O with 4-Byte Address (BCh)

The Fast Read Dual I/O with 4-Byte Address instruction is similar to the Fast Read Dual I/O instruction except that it requires a 32-bit address instead of a 24-bit address. Whether the device is operating in a 3-Byte Address Mode or a 4-byte Address Mode, the Fast Read Dual I/O with 4-Byte Address instruction will always require a 32-bit address to access the entire 256M-bit ~2G-bit memory.

The Fast Read Dual I/O with 4-Byte Address (BCh) instruction is only supported in Standard SPI mode.

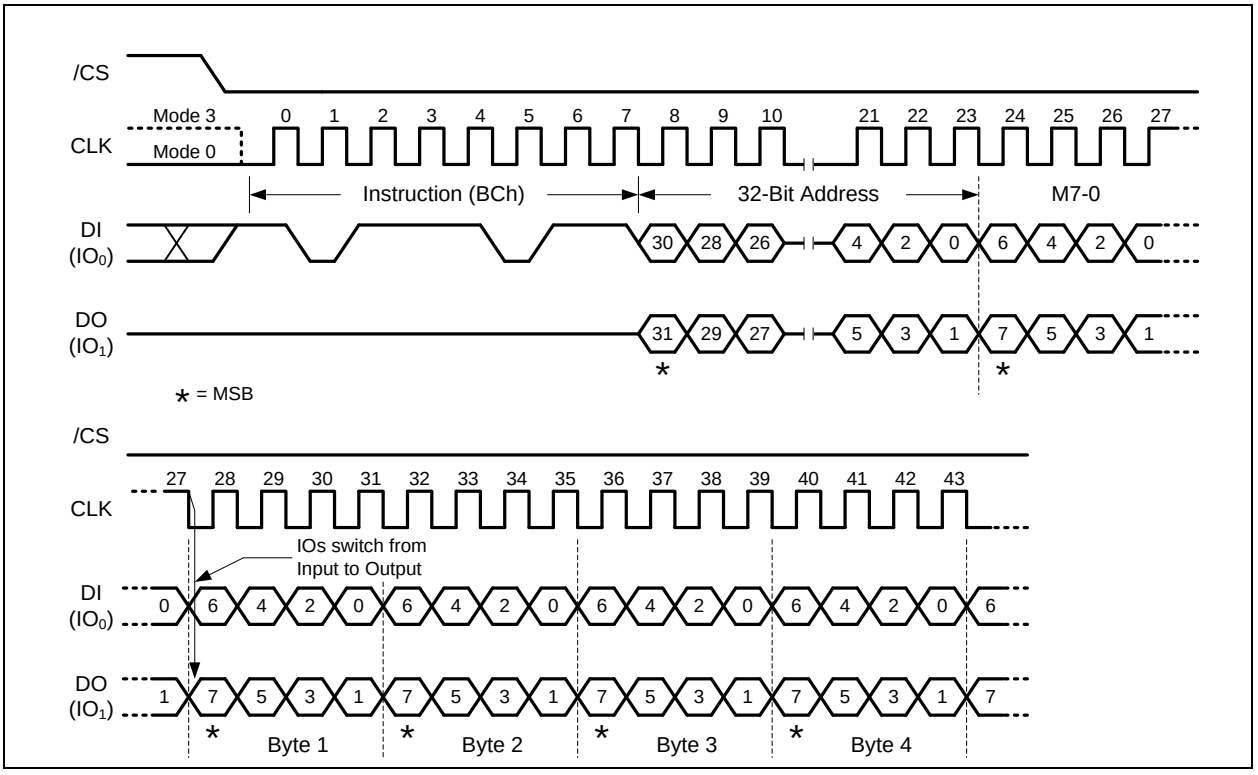



Figure 6.4.21a. Fast Read Dual I/O w/ 4-Byte Addr. (Initial instruction or previous M5-4¹10, SPI Mode only)



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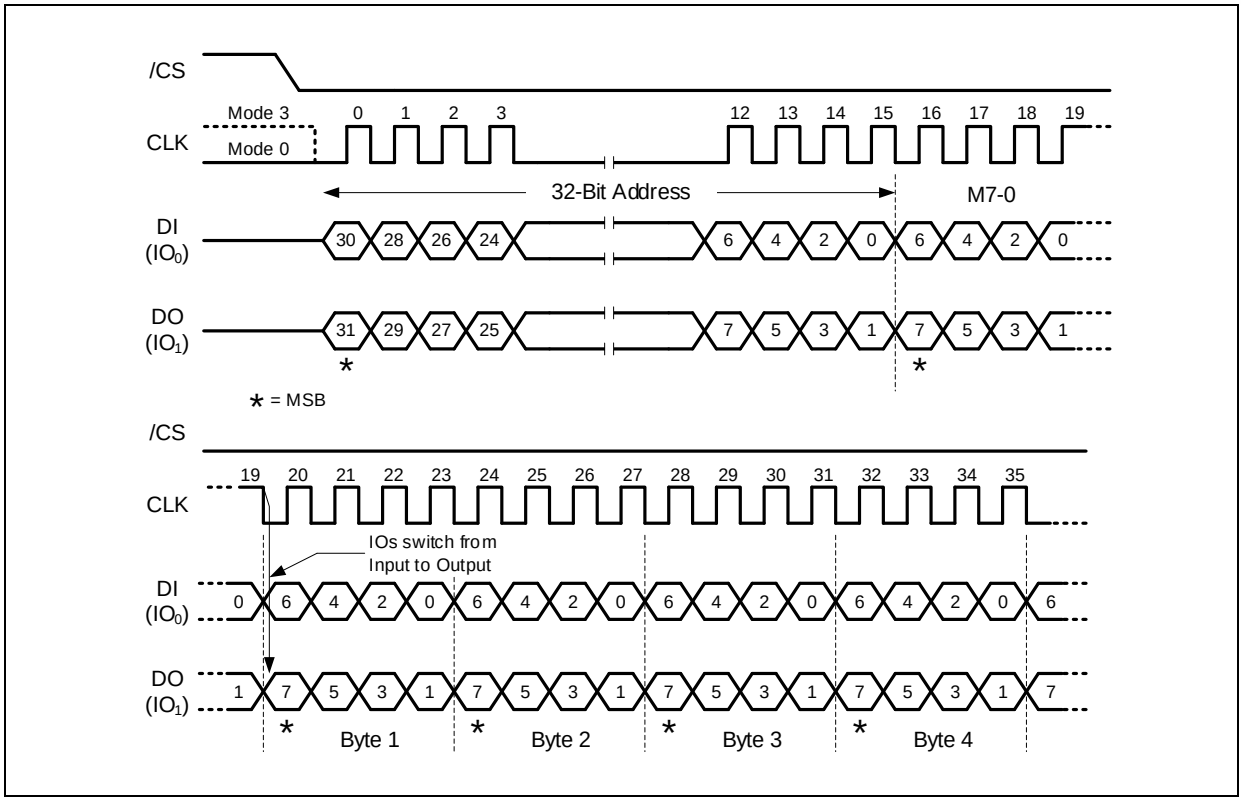



Figure 6.4.21b. Fast Read Dual I/O w/ 4-Byte Addr. (Previous instruction set M5-4=10, SPI Mode only)



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### 6.4.22 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that the address and data bits are input and output through four pins $IO_0$, $IO_1$, $IO_2$ and $IO_3$ and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

**Fast Read Quad I/O with "Read Command Bypass Mode"**

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the Read Command Bypass Mode bits (M7-0) after the input Address bits (A23-0), as shown in Figure 6.2.22a. The upper nibble (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the Read Command Bypass Mode bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in Figure 6.2.22b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the Read Command Bypass Mode bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

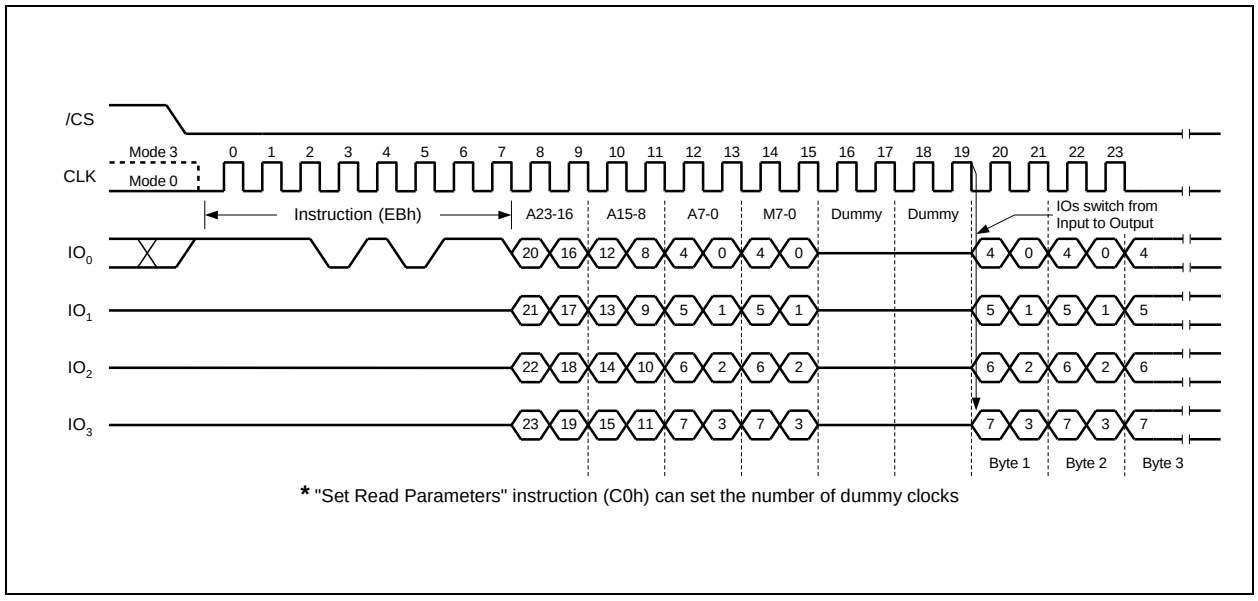



Figure 6.4.22a. Fast Read Quad I/O (Initial instruction or previous M5-4¹10, SPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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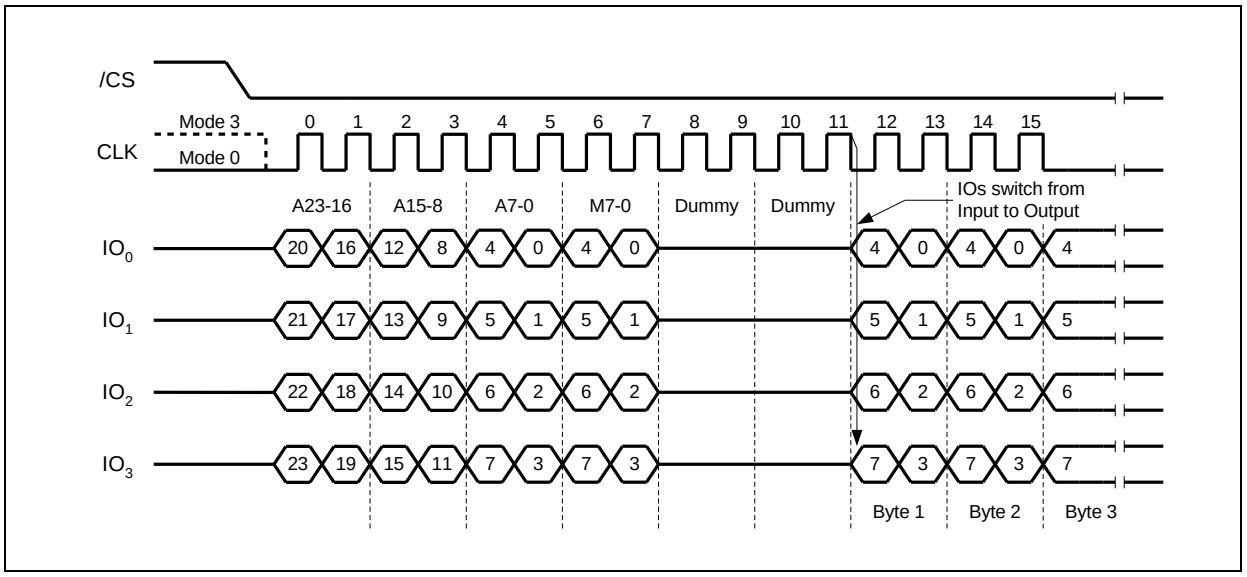



Figure 6.4.22b. Fast Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode)

### Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EBh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction. Once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while bits W6-5 are used to specify the length of the wrap around section within a page. Refer to the link " 6.4.26 Set Burst with Wrap (77h)"



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**Fast Read Quad I/O (EBh) in QPI Mode**

The Fast Read Quad I/O instruction is also supported in QPI mode, as shown in Figure 26c. When QPI mode is enabled, the number of dummy clocks is configured by the "Set Read Parameters (C0h)" instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 6, 8, 10, 12, 14 or 16. The default number of dummy clocks upon power up or after a Reset instruction is 6.

The "Wrap Around" feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length, wrap around in QPI mode, a dedicated "Burst Read with Wrap" (0Ch) instruction must be used. Please refer to the link " 6.4.14 Fast Read with 4-Byte Address (0Ch) "for details.

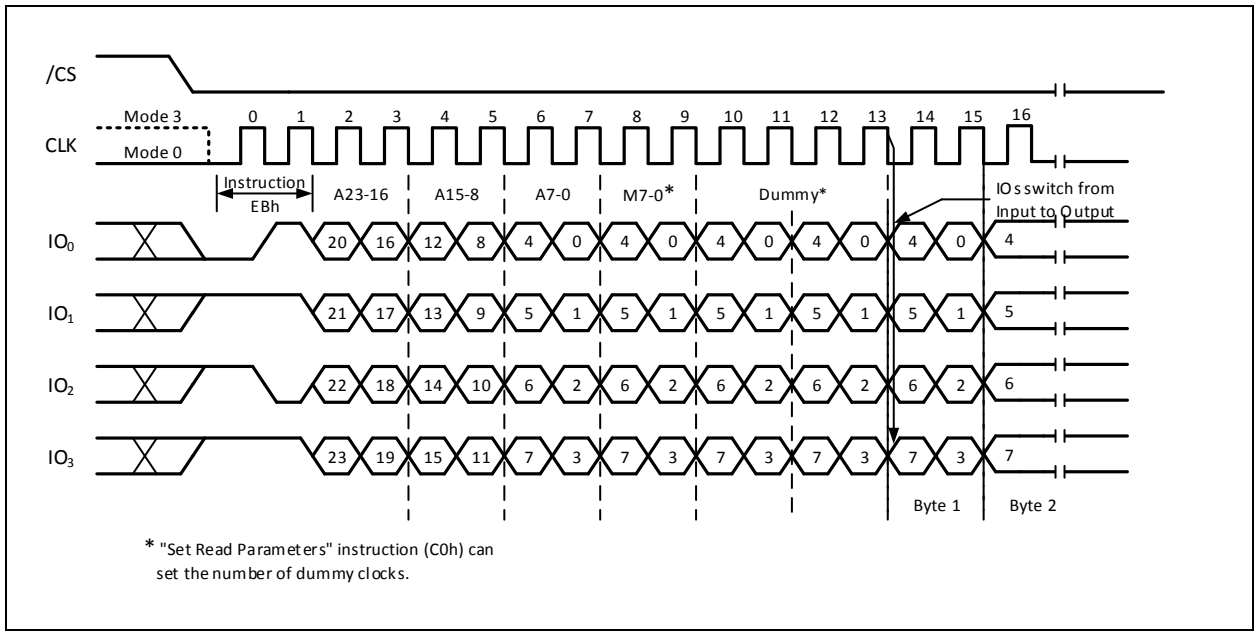



Figure **Error! Reference source not found.**c. Fast Read Quad I/O (Initial instruction or previous M5-4≠10, QPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.23 DTR Fast Read Quad I/O (EDh)

The DTR Fast Read Quad I/O (EDh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins $IO_0$, $IO_1$, $IO_2$ and $IO_3$ and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

**DTR Fast Read Quad I/O with "Read Command Bypass Mode"**

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the Read Command Bypass Mode bits (M7-0) after the input Address bits (A23/A31-0), as shown in Figure 6.2.23a. The upper nibble (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits (M3-0) are don't care ("x"). However, the IO pins should be high impedance prior to the falling edge of the first data out clock.

If the Read Command Bypass Mode bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in Figure 6.2.23b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the Read Command Bypass Mode bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh/3FFh on IO0 for the next instruction (8/10 clocks), to ensure M4 = 1 and return the device to normal operation.

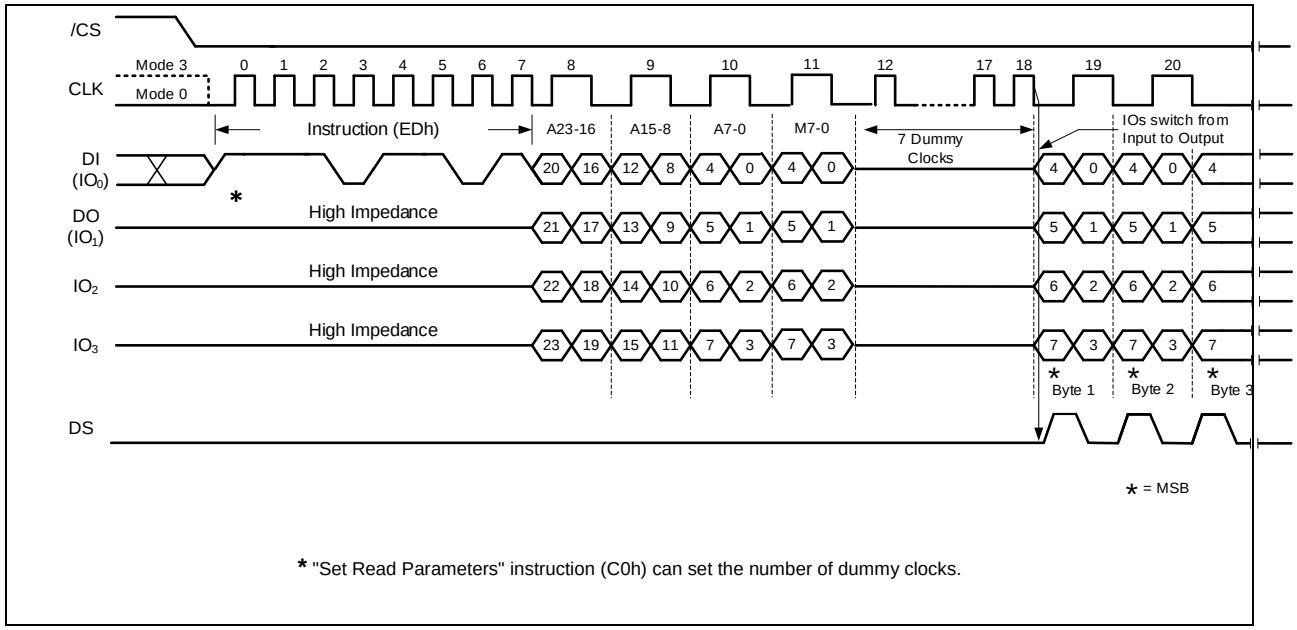



Figure 6.4.23a. DTR Fast Read Quad I/O (Initial instruction or previous M5-4¹10, SPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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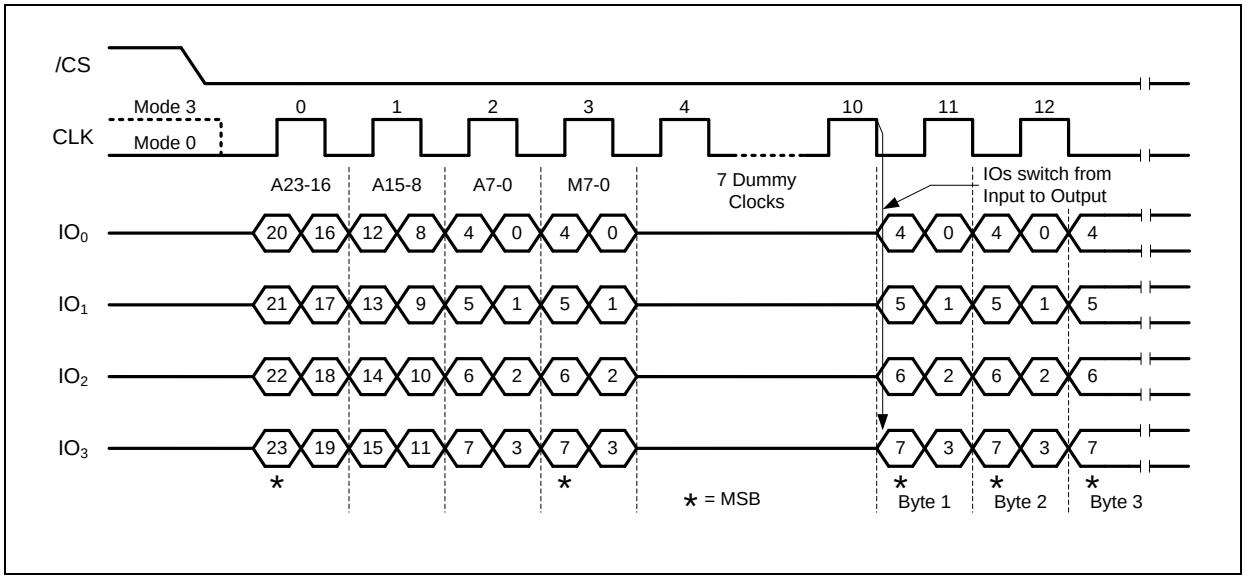



Figure 6.4.23b. Fast Read Quad I/O (Previous instruction set M5-4=10, SPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*

### DTR Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EDh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EDh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction. Once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while bits W6-5 are used to specify the length of the wrap around section within a page. Refer to the link " 6.4.26 Set Burst with Wrap (77h)



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### DTR Fast Read Quad I/O (EDh) in QPI Mode

The DTR Fast Read Quad I/O instruction is also supported in QPI mode, as shown in Figure 6.2.23c
The “Wrap Around” feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated “Burst Read with Wrap” (0Ch) instruction must be used. Please refer to the link “6.4.51 Burst Read with Wrap (0Ch)” for details.

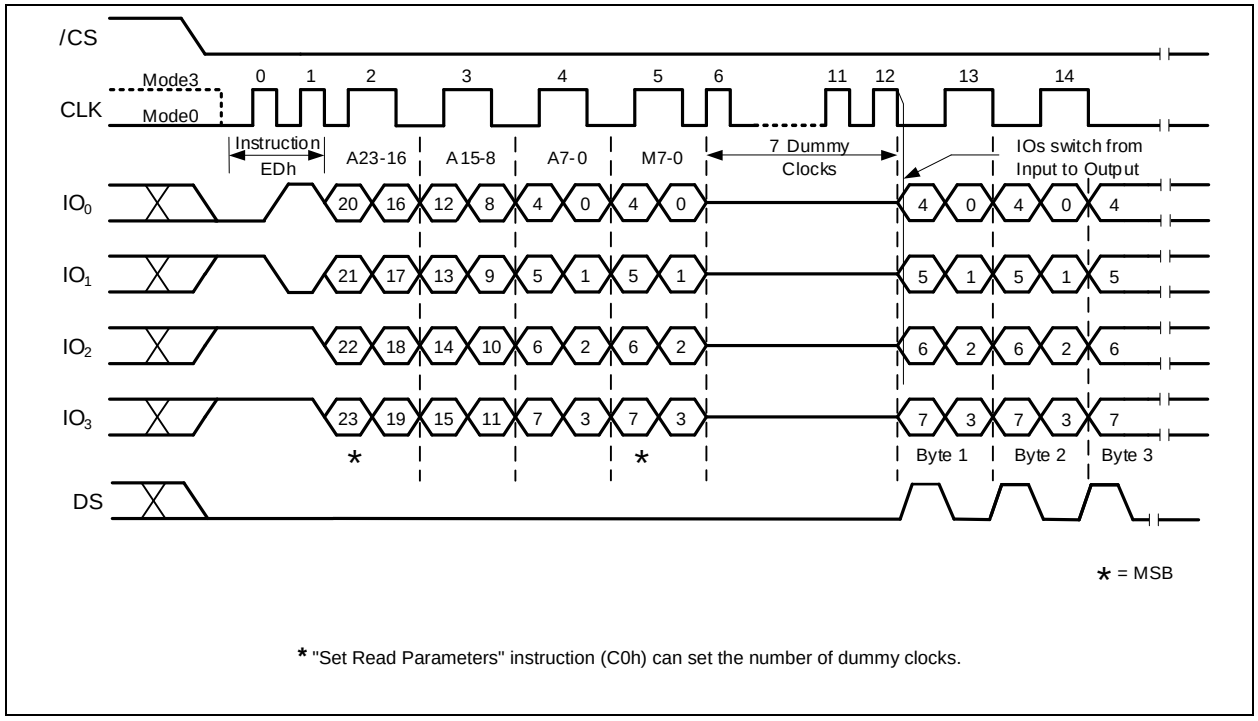



Figure 6.4.23c. DTR Fast Read Quad I/O (Initial instruction or previous M5-4¹10, QPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.24 DTR Fast Read Quad I/O with 4-Byte Address (EEh)

The DTR Fast Read Quad I/O with 4-Byte Address instruction is similar to the DTR Fast Read Quad I/O instruction except that it requires 32-bit address instead of 24-bit address. Whether the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the DTR Fast Read Quad I/O with 4-Byte Address instruction will always require a 32-bit address to access the entire memory.

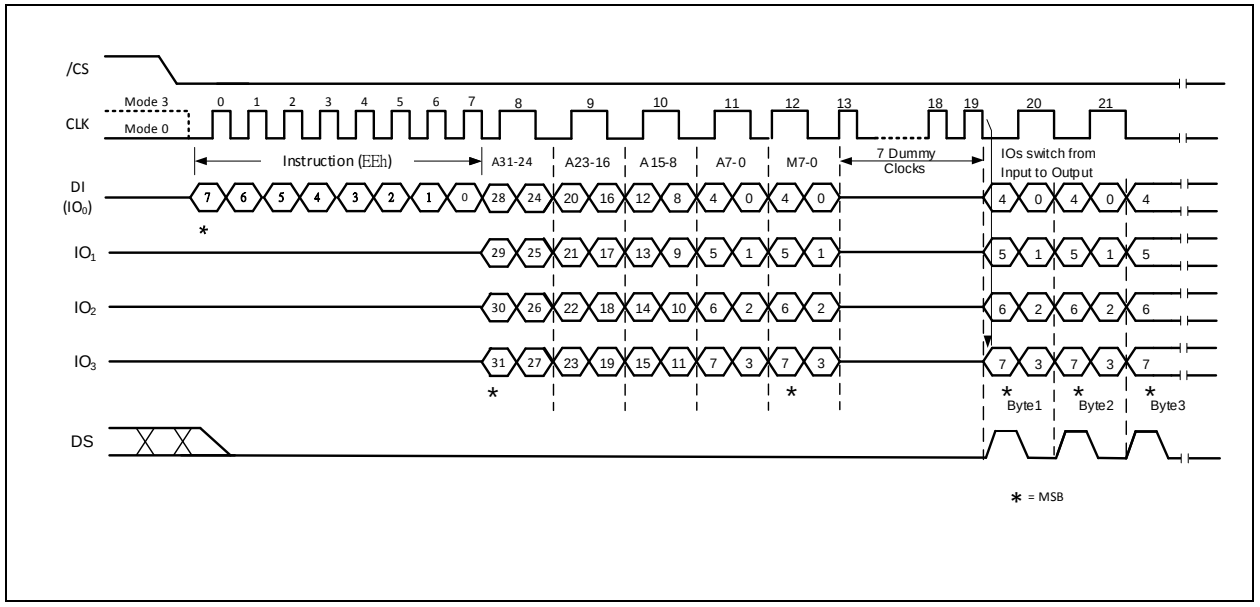



Figure 6.4.24a. DTR Fast Read Dual I/O w/ 4-Byte Addr. (Initial instruction or previous M5-4¹10, SPI Mode only)

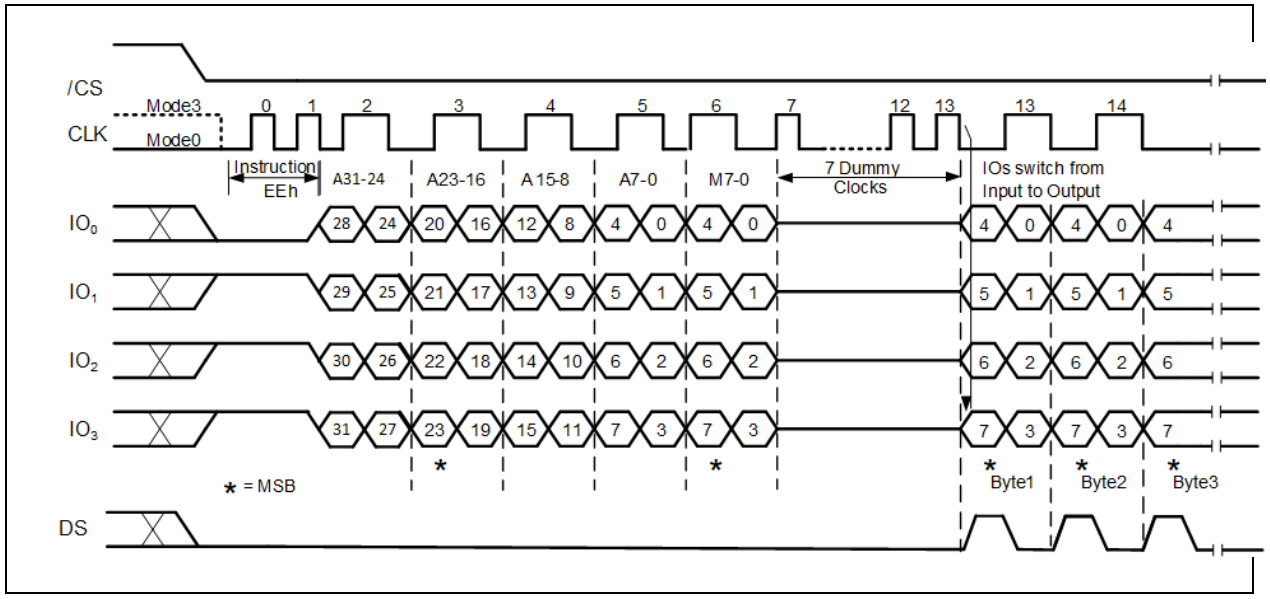



Figure 6.4.24b. DTR Fast Read Dual I/O w/ 4-Byte Addr. (Initial instruction or previous M5-4¹10, QPI Mode only)



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### 6.4.25 Fast Read Quad I/O with 4-Byte Address (ECh)

The Fast Read Quad I/O with 4-Byte Address instruction is similar to the Fast Read Quad I/O instruction except that it requires a 32-bit address instead of a 24-bit address. Whether the device is operating in a 3-Byte Address Mode or a 4-byte Address Mode, the Fast Read Quad I/O with 4-Byte Address instruction will always require a 32-bit address to access the entire 256M-bit ~2G-bit memory.

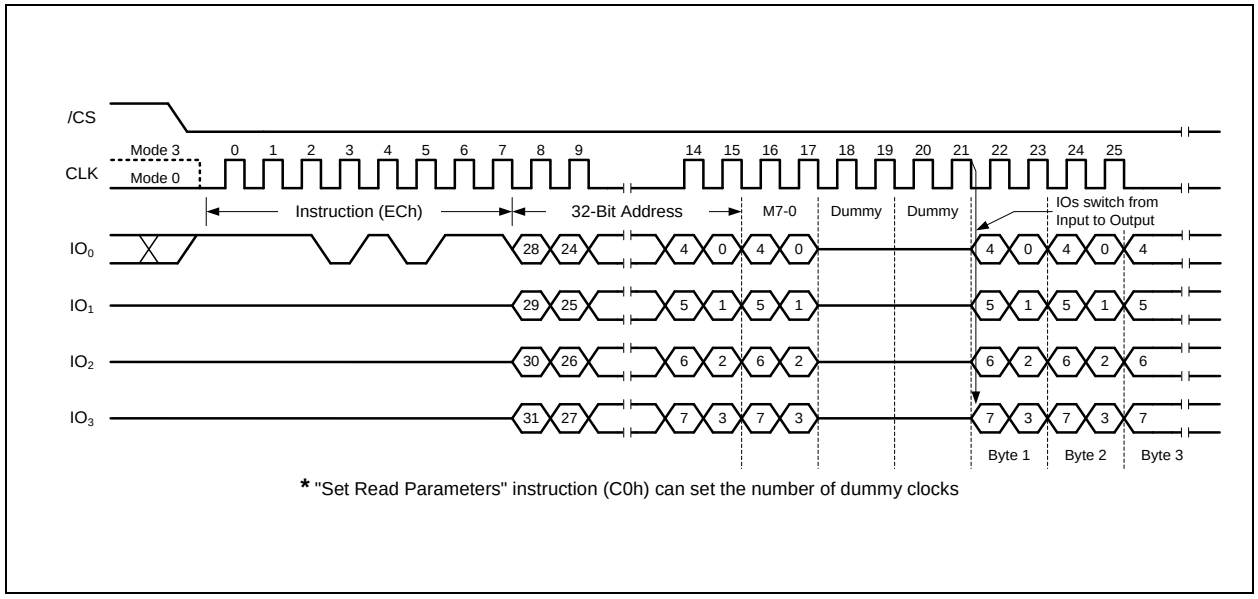



Figure 6.4.25a. Fast Read Quad I/O w/ 4-Byte Addr. (Initial instruction or previous M5-4¹10, SPI Mode)

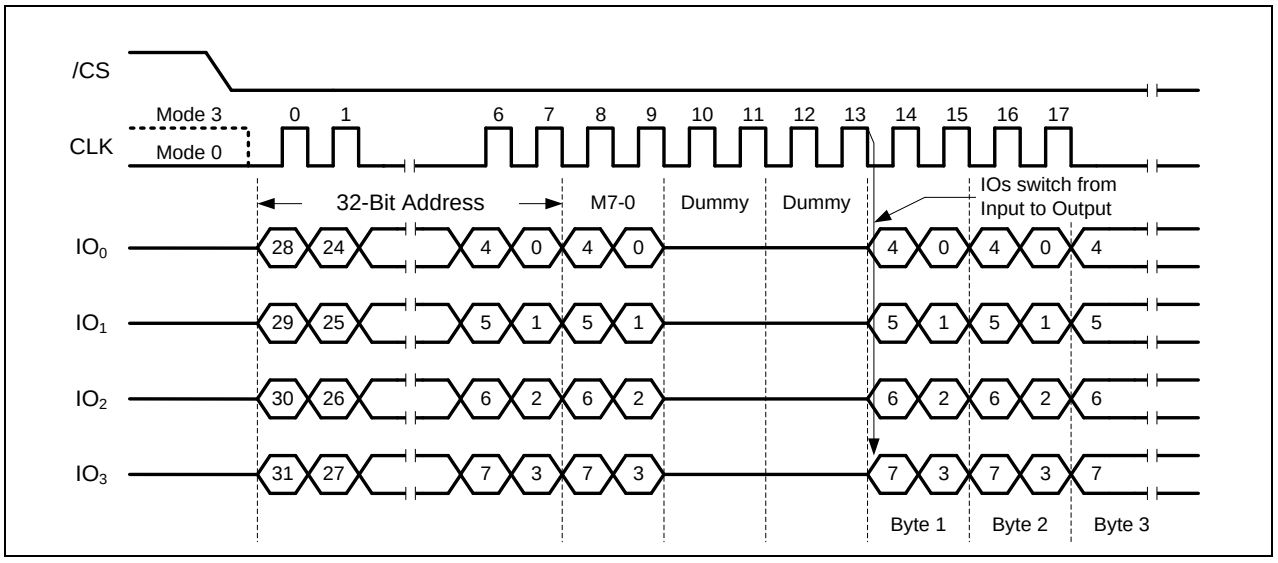



Figure 6.4.25b. Fast Read Quad I/O w/ 4-Byte Addr. (Previous instruction set M5-4=10, SPI Mode only)



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**Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode**

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to ECh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following ECh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction. Once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

**Fast Read Quad I/O with 4-Byte Address (ECh) in QPI Mode**

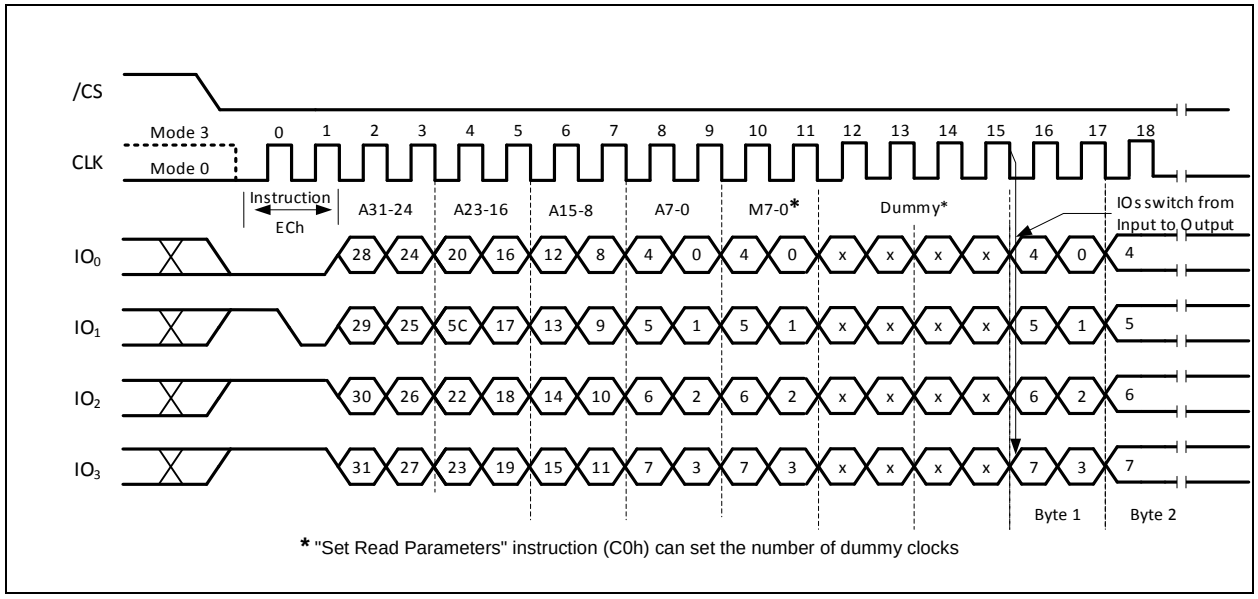



Figure 6.4.25a. Fast Read Quad I/O w/ 4-Byte Addr. (Initial instruction or previous M5-4¹10, SPI Mode)



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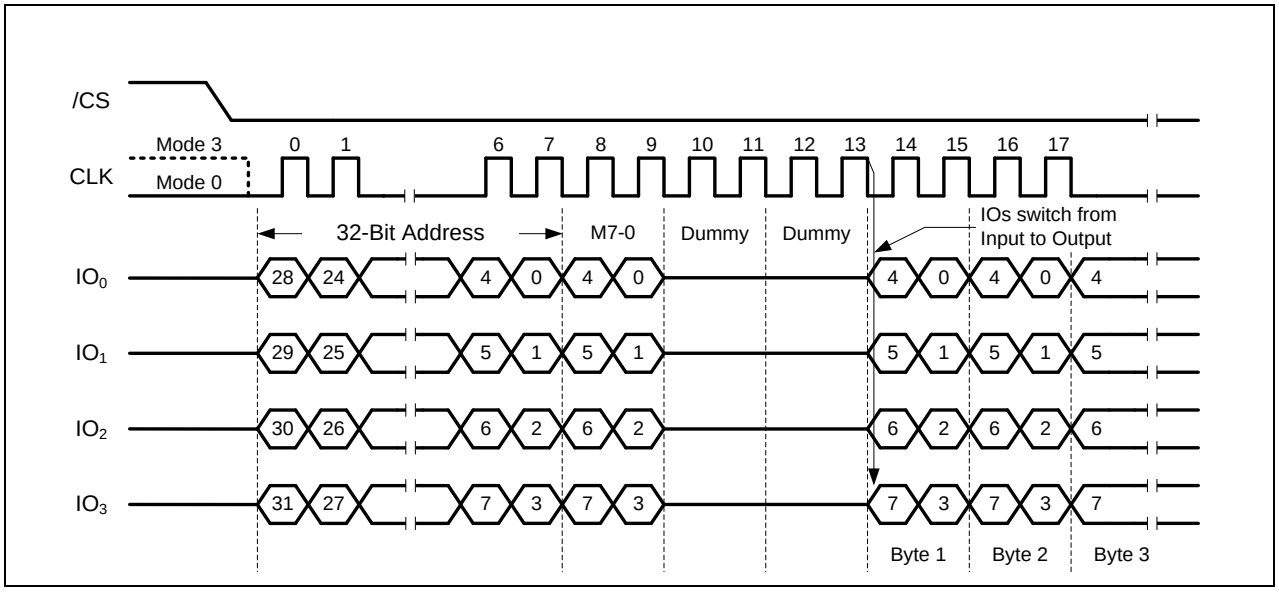



Figure 6.4.25b. Fast Read Quad I/O w/ 4-Byte Addr. (Previous instruction set M5-4=10, SPI Mode only)



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### 6.4.26 Set Burst with Wrap (77h)

In Standard SPI mode, the Set Burst with Wrap (77h) instruction is used in conjunction with “Fast Read Quad I/O(EBh)”, Fast Read Quad I/O with 4-Byte Address (ECh),“DTR Fast Read Quad I/O (EDh)” , and DTR Fast Read Quad I/O with 4-Byte Address(EEh) instructions, to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the /CS pin low and then shifting the instruction code “77h” followed by 24dummy bits and 8 “Wrap Bits”, W7-0. The instruction sequence is shown in Figure 0 . Wrap bit W7 and the lower nibble W3-0 are not used.

| W6, W5 | W4 = 0 | | W4 =1 (DEFAULT) | |
|---|---|---|---|---|
| | Wrap Around | Wrap Length | Wrap Around | Wrap Length |
| 0 0 | Yes | 8-byte | No | N/A |
| 0 1 | Yes | 16-byte | No | N/A |
| 1 0 | Yes | 32-byte | No | N/A |
| 1 1 | Yes | 64-byte | No | N/A |

Once W6-4 is set by a Set Burst with Wrap instruction, the “Fast Read Quad I/O(EBh)”, Fast Read Quad I/O with 4-Byte Address (ECh), “DTR Fast Read Quad I/O (EDh)”, and DTR Fast Read Quad I/O with 4-Byte Address(EEh) instructions will access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on or after a software/hardware reset is 1.

In QPI mode, the “Burst Read with Wrap (0Ch)” instruction should be used to perform the Read operation with “Wrap Around” feature. The Wrap Length set by W5-4 in Standard SPI mode is still valid in QPI mode and can also be re-configured by “Set Read Parameters (C0h)” instruction. Refer to the link “6.4.51 Burst Read with Wrap (0Ch)” and “6.4.14 Fast Read with 4-Byte Address (0Ch)” for details.

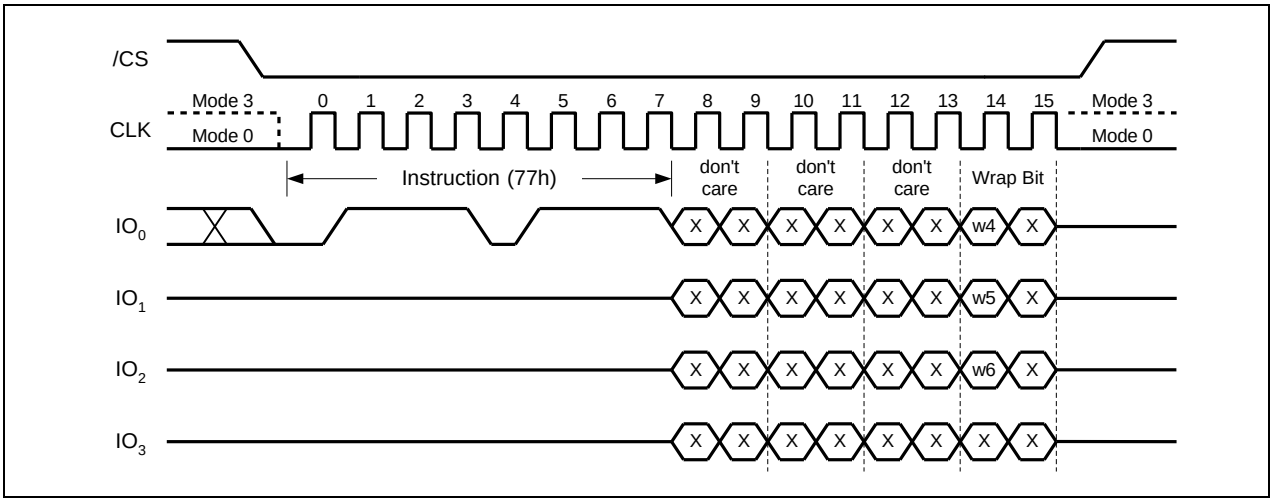



Figure 0. Set Burst with Wrap Instruction (SPI Mode only)



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### 6.4.27 Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24/32-bit address (A23/A31-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 6.4.27.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP3, BP2, BP1, and BP0) bits or the Flex Block/Sector Locks.

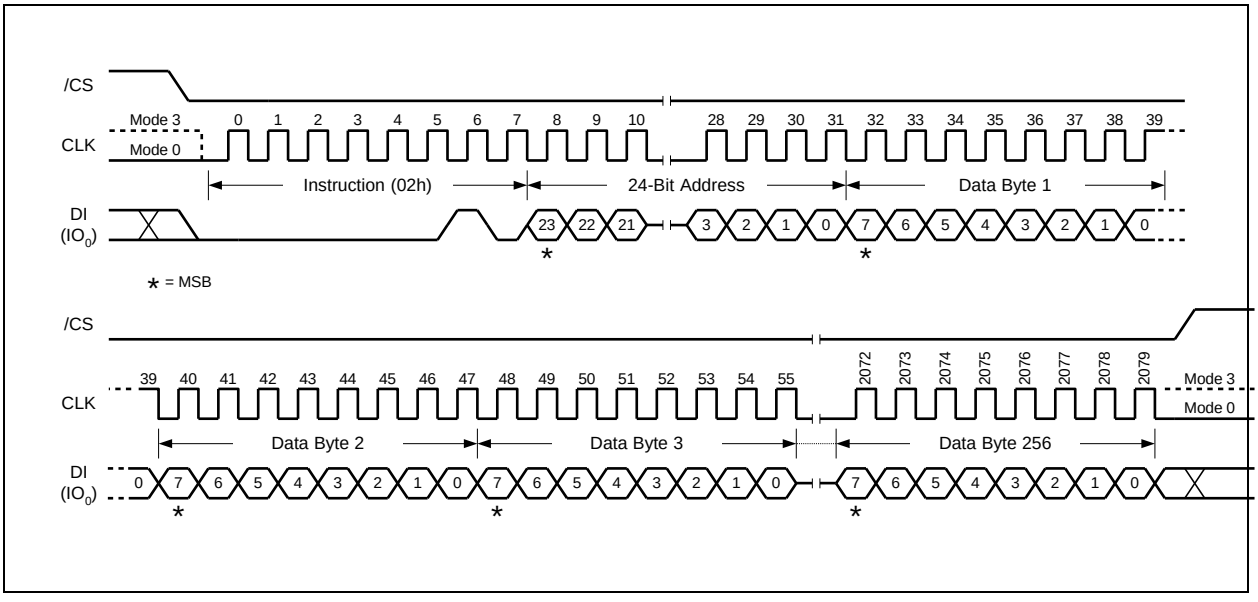



Figure 6.4.27a. Page Program Instruction (SPI Mode)



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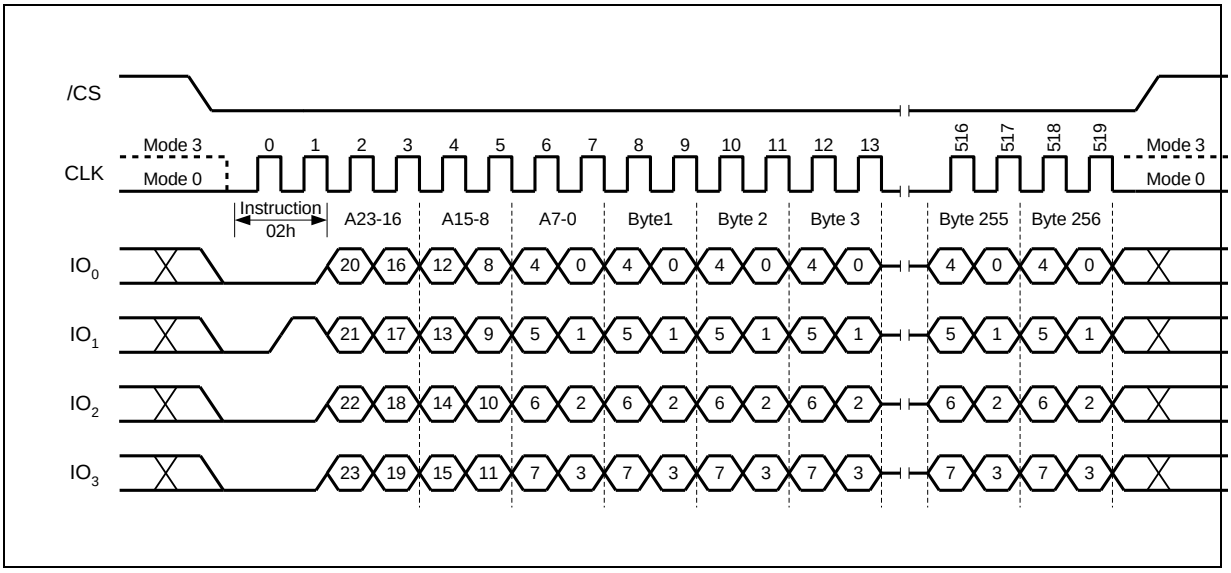



Figure 6.4.27b. Page Program Instruction (QPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.28 Page Program with 4-Byte Address (12h)

The Page Program with 4-Byte Address instruction is similar to the Page Program instruction except that it requires a 32-bit address instead of a 24-bit address. Whether the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Page Program with 4-Byte Address instruction will always require a 32-bit address to access the entire 256M-bit ~2G-bit memory.

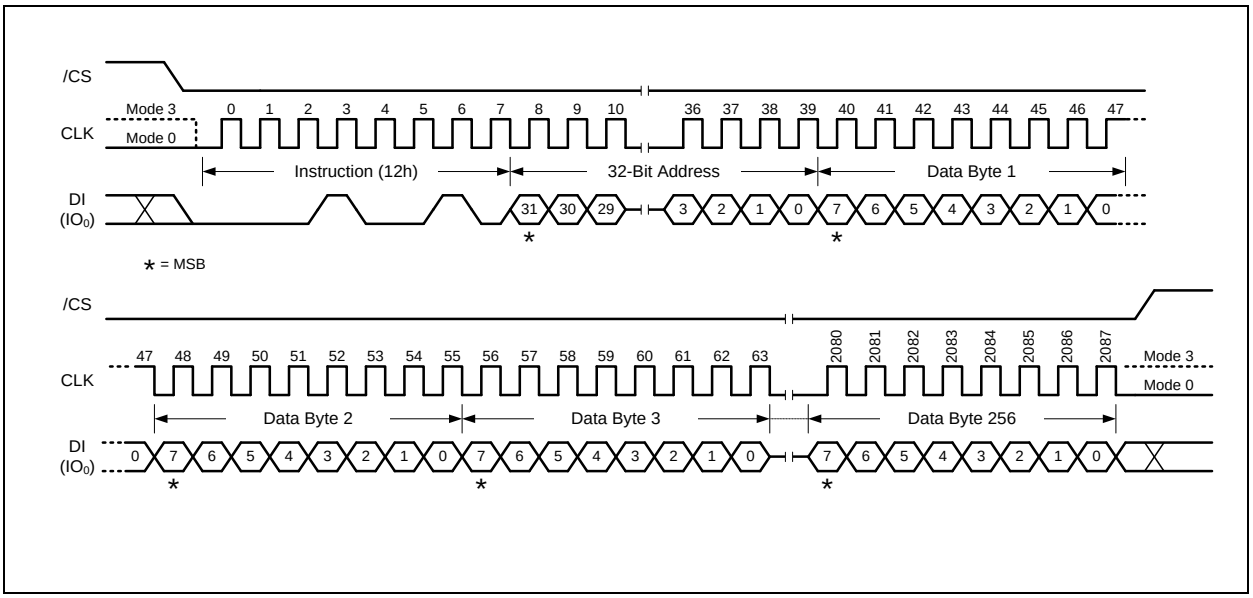



Figure 6.4.28. Page Program with 4-Byte Addr. (SPI Mode Only)



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### 6.4.29 Quad Input Page Program (32h)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: $IO_0$, $IO_1$, $IO_2$, and $IO_3$. The Quad Page Program can improve performance for PROM Programmers and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it takes to clock-in the data.

To use Quad Page Program, the Quad Enable (QE) bit in Status Register-2 must be set to 1. A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the /CS pin low then shifting the instruction code "32h" followed by a 24/32-bit address (A23/A31-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program instruction sequence is shown in Figure 6.2.29.

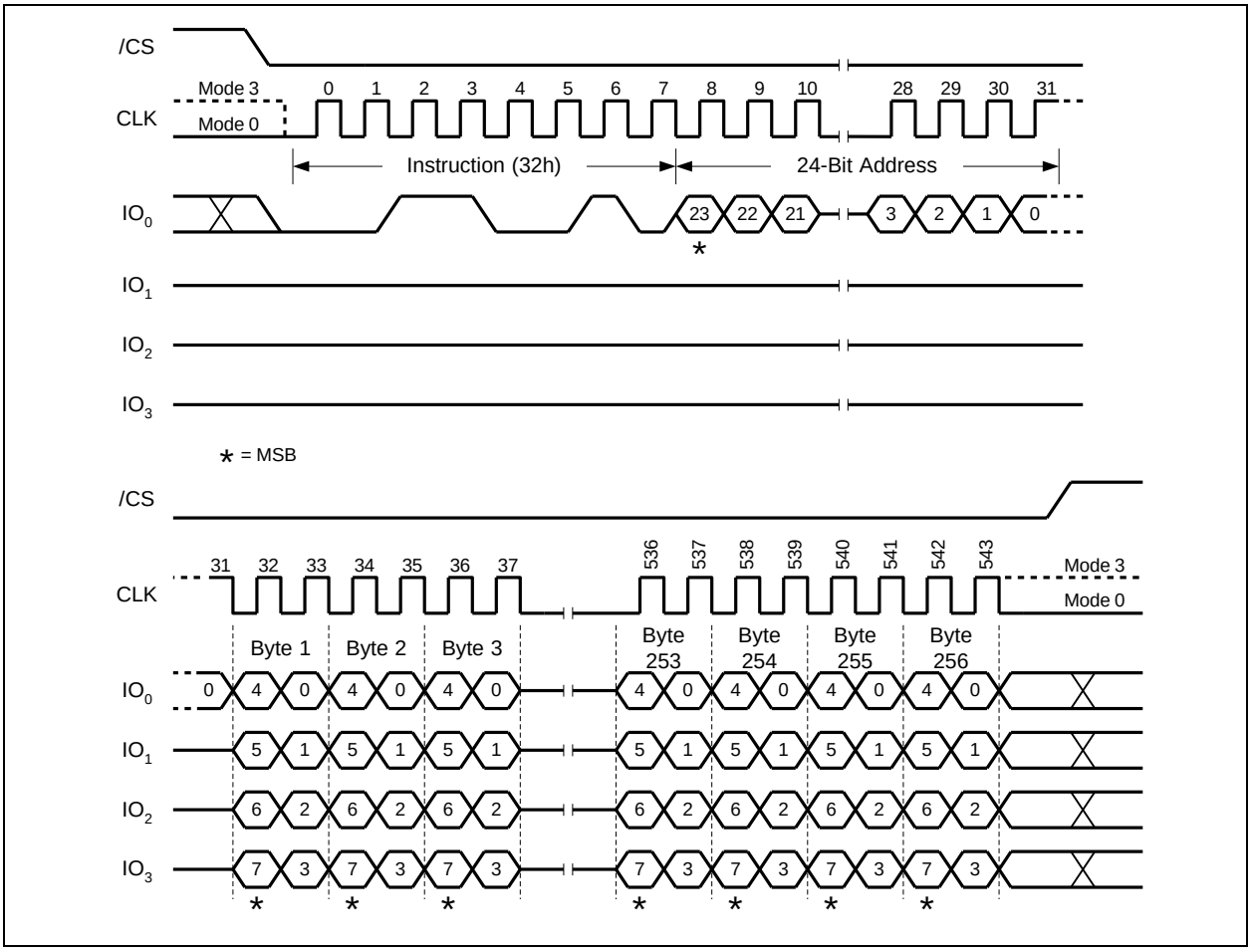



Figure 6.4.29. Quad Input Page Program Instruction (SPI Mode only)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.30 Quad Input Page Program with 4-Byte Address (34h)

The Quad Input Page Program with 4-Byte Address instruction is similar to the Quad Input Page Program instruction except that it requires a 32-bit address instead of a 24-bit address. Whether the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Quad Input Page Program with 4-Byte Address instruction will always require a 32-bit address to access the entire 256M-bit ~2G-bit memory.

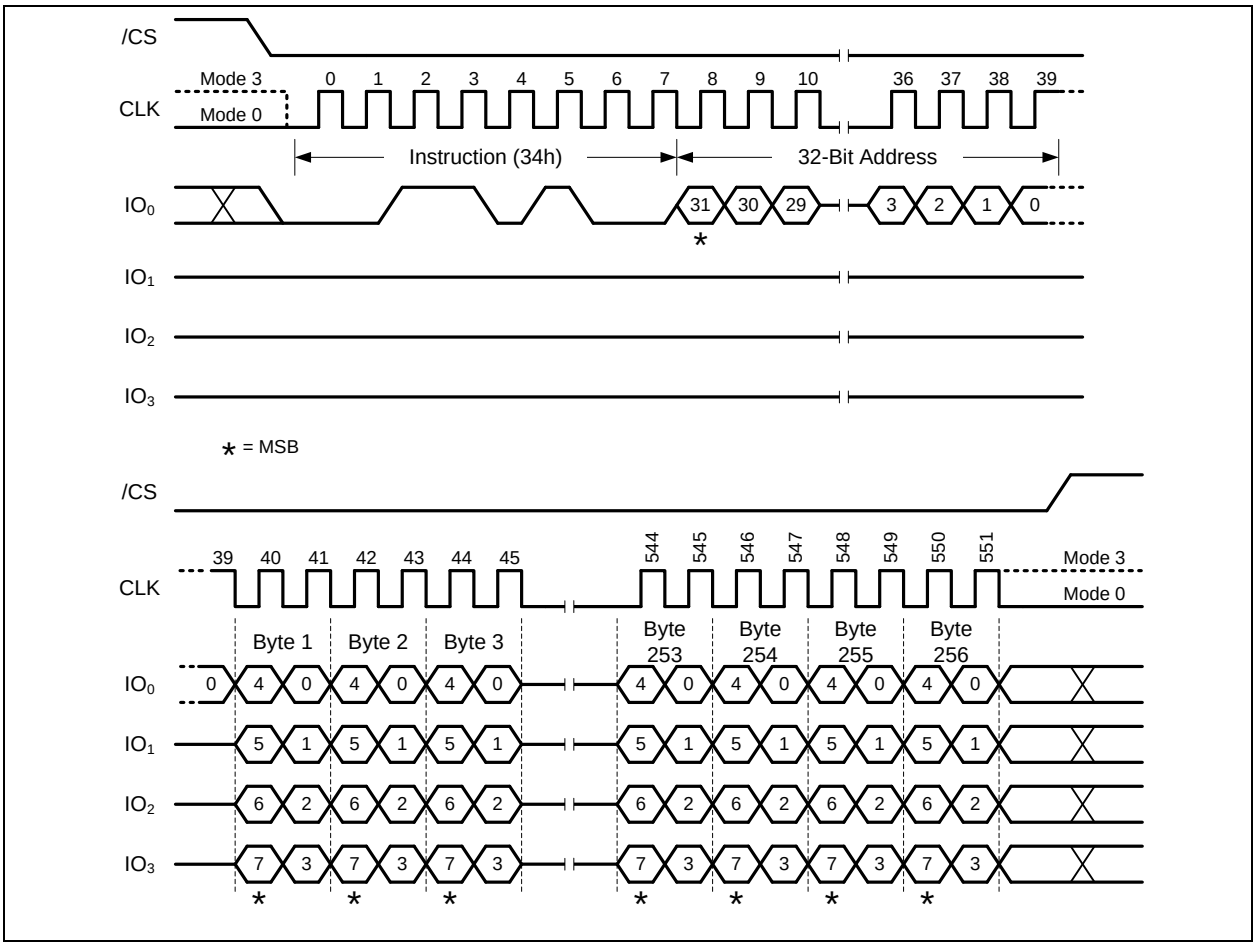



Figure 6.4.30. Quad Input Page Program with 4-Byte Addr. (SPI Mode only)



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### 6.4.31 Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24/32-bit sector address (A23/A31-A0). The Sector Erase instruction sequence is shown in Figure 6.2.31.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of $t_{SE}$ (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished, and the device is ready to accept other instructions again. After the Sector Erase cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP3, BP2, BP1, and BP0) bits or the Flex Block/Sector Locks.

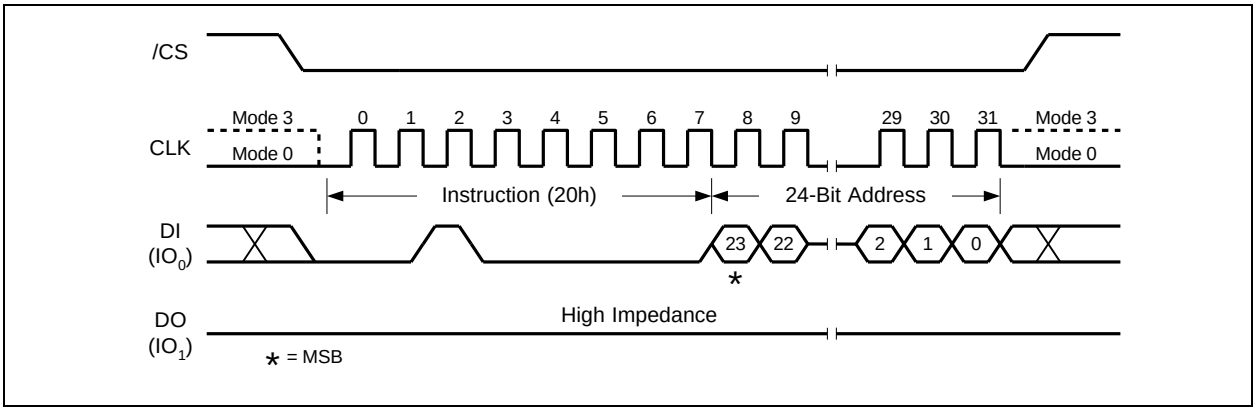



Figure 6.4.31a. Sector Erase Instruction (SPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*

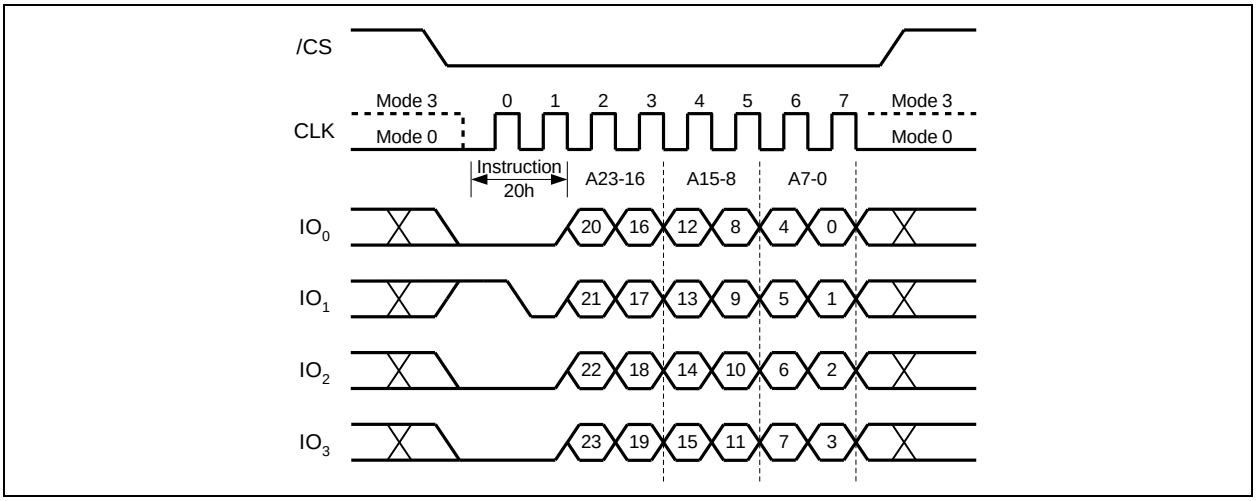



Figure 6.4.31b. Sector Erase Instruction (QPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.32 Sector Erase with 4-Byte Address (21h)

The Sector Erase with 4-Byte Address instruction is similar to the Sector Erase instruction except that it requires a 32-bit address instead of a 24-bit address. Whether the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Sector Erase with 4-Byte Address instruction will always require a 32-bit address to access the entire 256M-bit ~2G-bit memory.

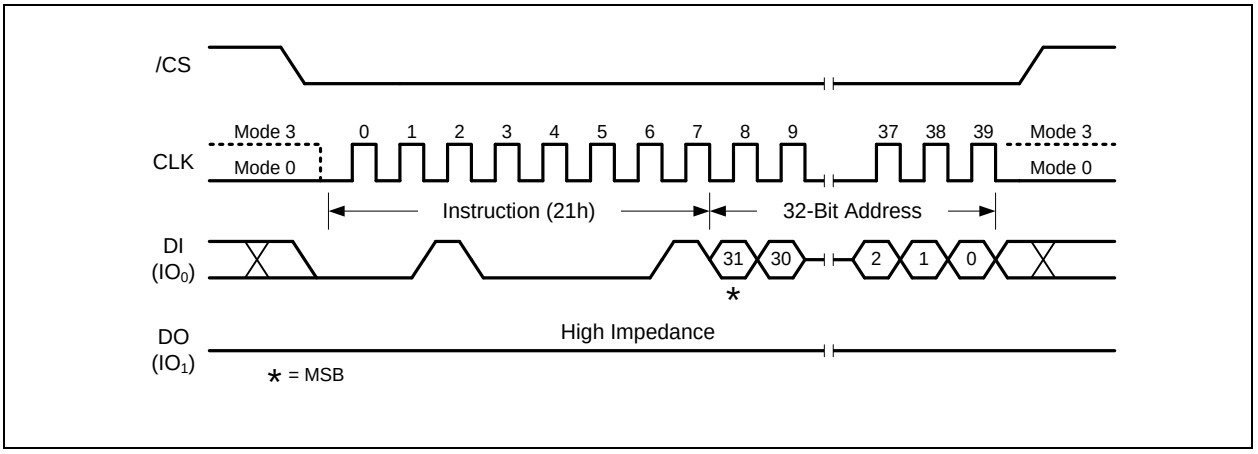



Figure 6.4.32. Sector Erase with 4-Byte Address Instruction (SPI Mode Only)

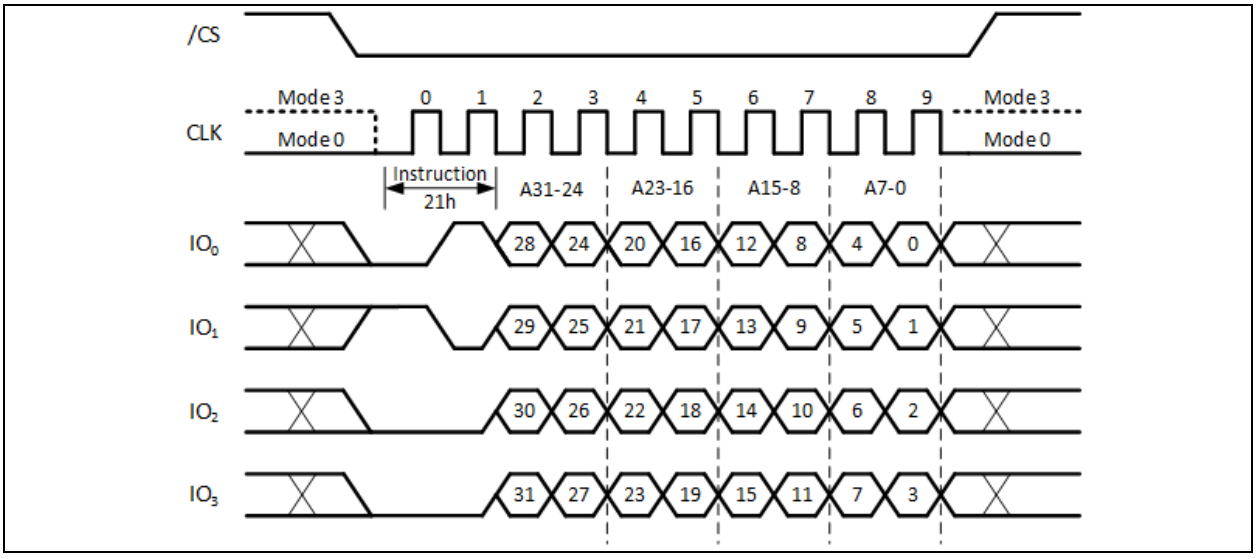



Figure 6.4.32b. Sector Erase with 4-Byte Address Instruction (QPI Mode)



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### 6.4.33 32KB Block Erase (52h)

The Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "52h" followed a 24/32-bit block address (A23/A31-A0). The Block Erase instruction sequence is shown in Figure 6.2.33.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of $t_{BE1}$ (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished, and the device is ready to accept other instructions again. After the Block Erase cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP3, BP2, BP1, and BP0) bits or the Flex Block/Sector Locks.

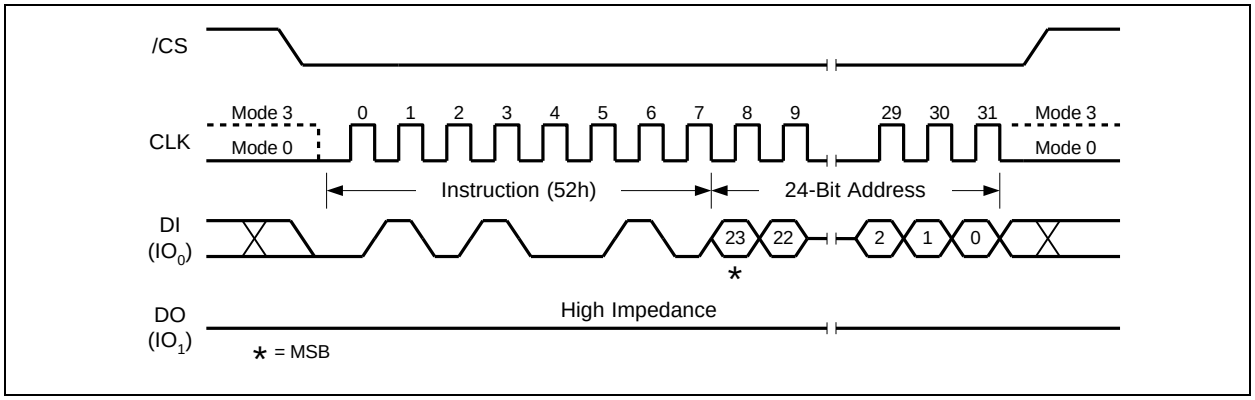



Figure 6.4.33a. 32KB Block Erase Instruction (SPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*

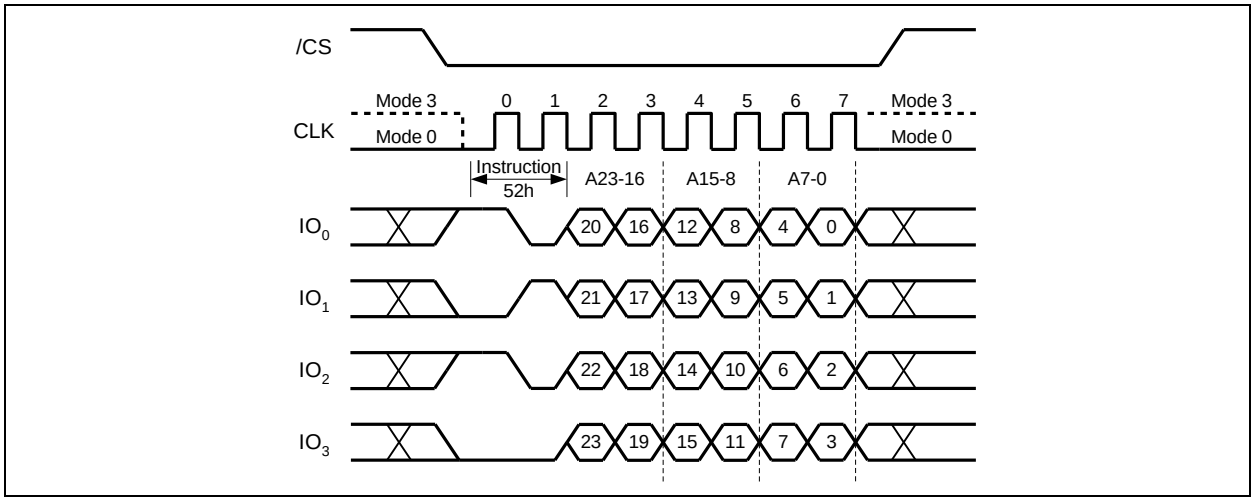



Figure 6.4.33b. 32KB Block Erase Instruction (QPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.34 64KB Block Erase (D8h)

The Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” followed a 24/32-bit block address (A23/A31-A0). The Block Erase instruction sequence is shown in Figure 6.2.34.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of $t_{BE}$ (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished, and the device is ready to accept other instructions again. After the Block Erase cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP3, BP2, BP1, and BP0) bits or the Flex Block/Sector Locks.

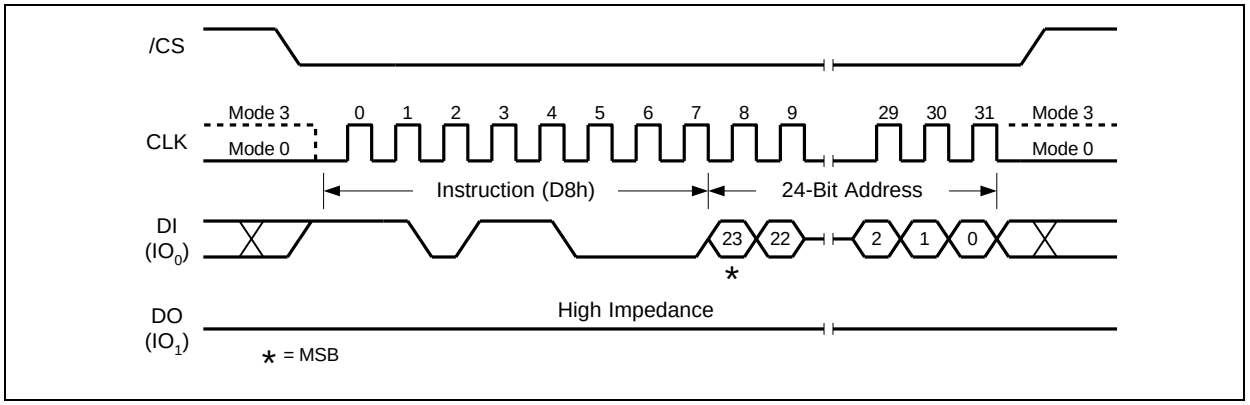



Figure 6.4.34a. 64KB Block Erase Instruction (SPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*

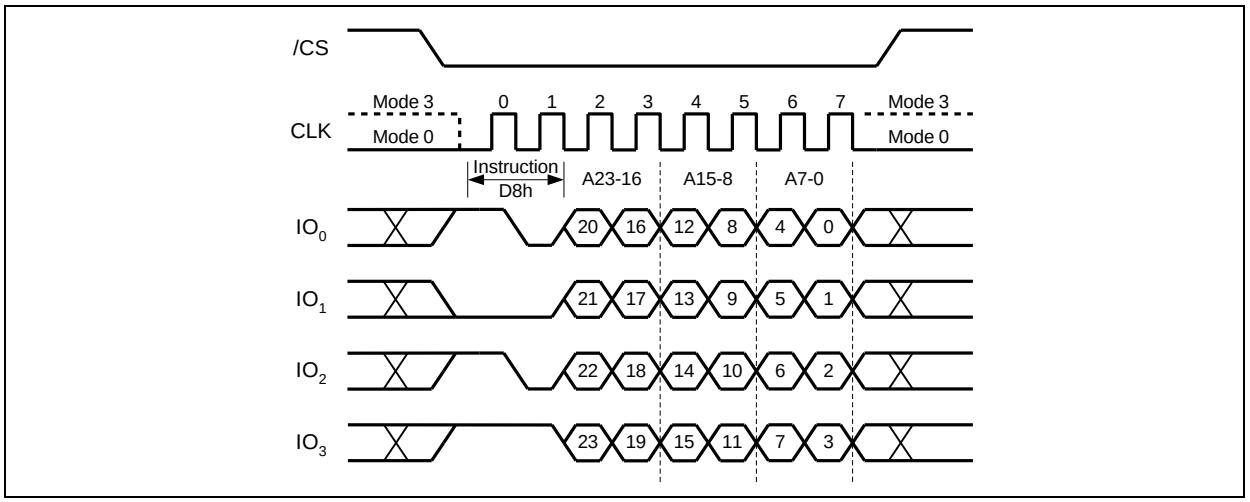



Figure 6.4.34b. 64KB Block Erase Instruction (QPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.35 64KB Block Erase with 4-Byte Address (DCh)

The 64KB Block Erase with 4-Byte Address instruction is similar to the 64KB Block Erase instruction except that it requires a 32-bit address instead of a 24-bit address. Whether the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the 64KB Block Erase with 4-Byte Address instruction will always require 32-bit address to access the entire 256M-bit ~2G-bit memory.

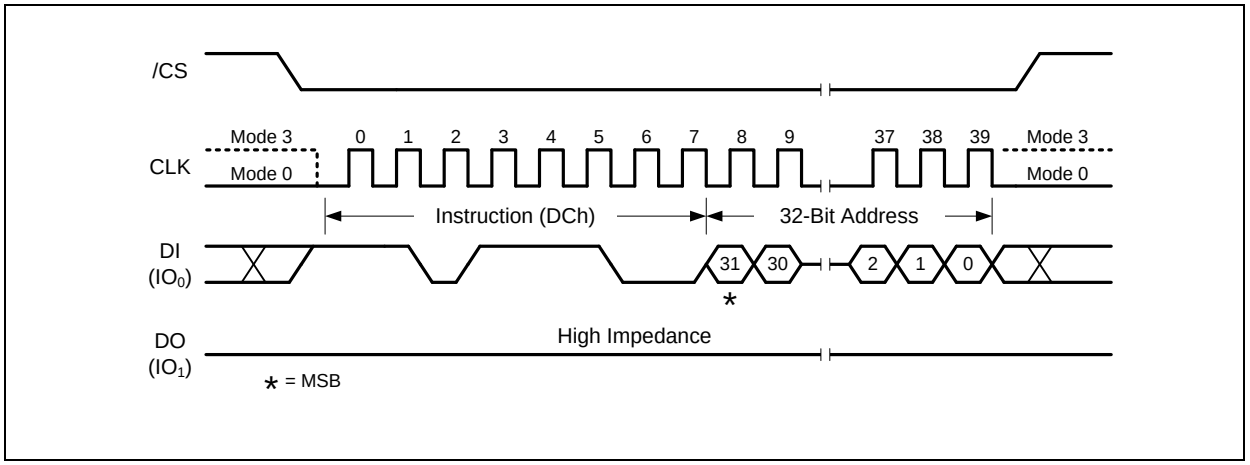



Figure 6.4.35. 64KB Block Erase with 4-Byte Address Instruction (SPI Mode Only)



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### 6.4.36 Chip Erase (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 6.2.36.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done, the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of $t_{CE}$ (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished, and the device is ready to accept other instructions again. After the Chip Erase cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any memory region is protected by the Block Protect (CMP, TB, BP3, BP2, BP1, and BP0) bits or the Flex Block/Sector Locks.

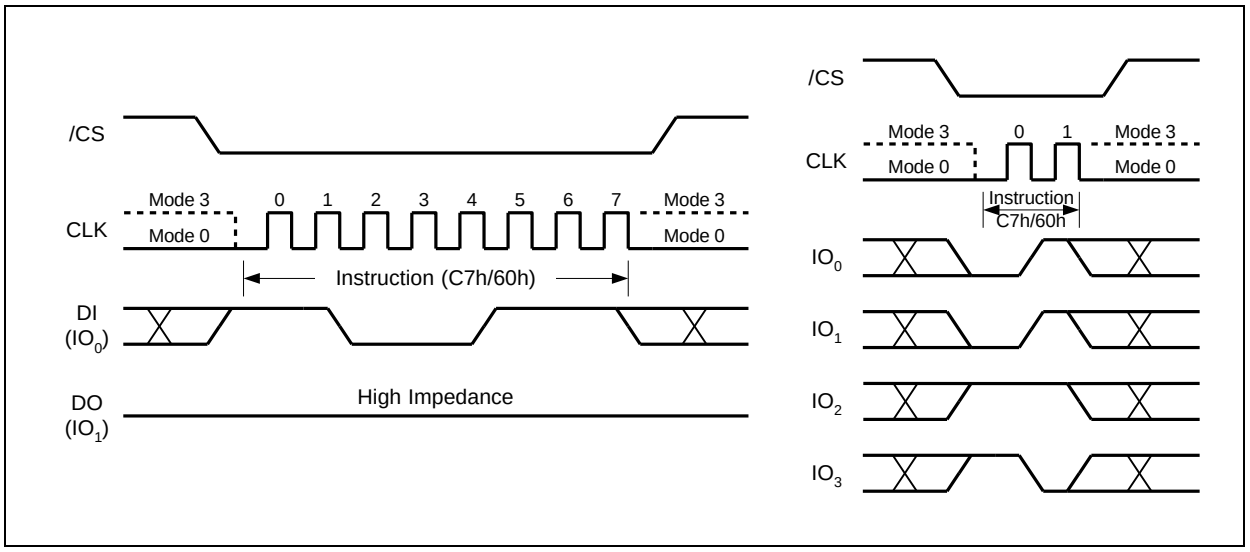



Figure 6.4.36. Chip Erase Instruction for SPI Mode (left) or QPI Mode (right)



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### 6.4.37 Erase / Program Suspend (75h)

The Erase/Program Suspend instruction “75h”, allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from or program/erase data to, any other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in Figure 6.2.37.

The Write Status Register instruction (01h/31h/11h) and Erase instructions (20h, 21h, 52h, D8h, DCh, C7h, 60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend instruction is ignored. The Write Status Register instruction (01h/31h/11h) and Program instructions (02h, 12h, 32h, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program or Quad Page Program operation.

The Erase/Program Suspend instruction “75h” will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of “$t_{SUS}$” (See AC Characteristics) is required to suspend the erase or program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within “$t_{SUS}$”, and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction “75h” is not issued earlier than a minimum of time of “$t_{SUS}$” following the preceding Resume instruction “7Ah”.

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. The SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended that the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state.

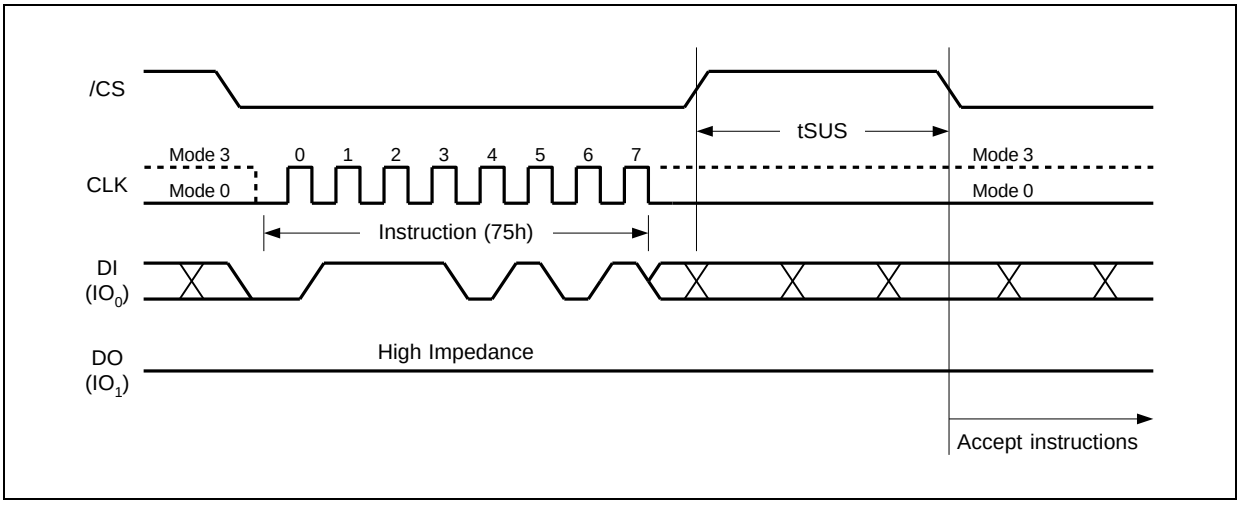



Figure 6.4.37a. Erase/Program Suspend Instruction (SPI Mode)



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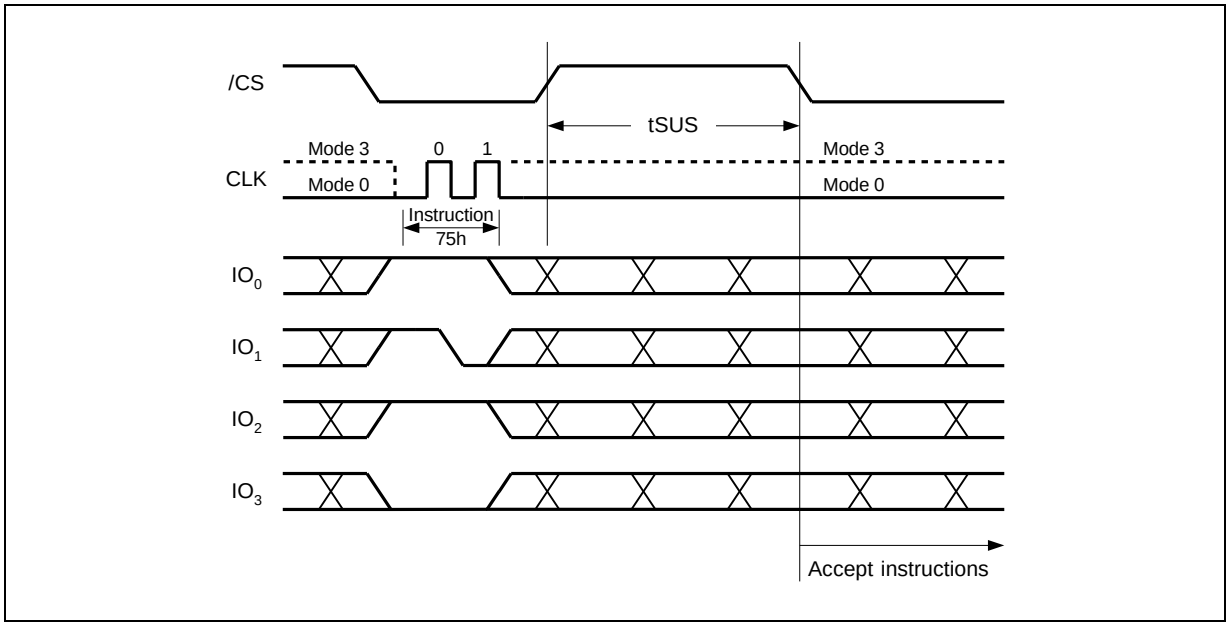



Figure 6.4.37b. Erase/Program Suspend Instruction (QPI Mode)



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### 6.4.38 Erase / Program Resume (7Ah)

The Erase/Program Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction “7Ah” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the BUSY bit equals to 0. After issued, the SUS bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200ns, and the Sector or Block will complete the erase operation, or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Erase/Program Resume instruction sequence is shown in Figure 6.4.38.

Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of “$t_{SUS}$” following a previous Resume instruction.

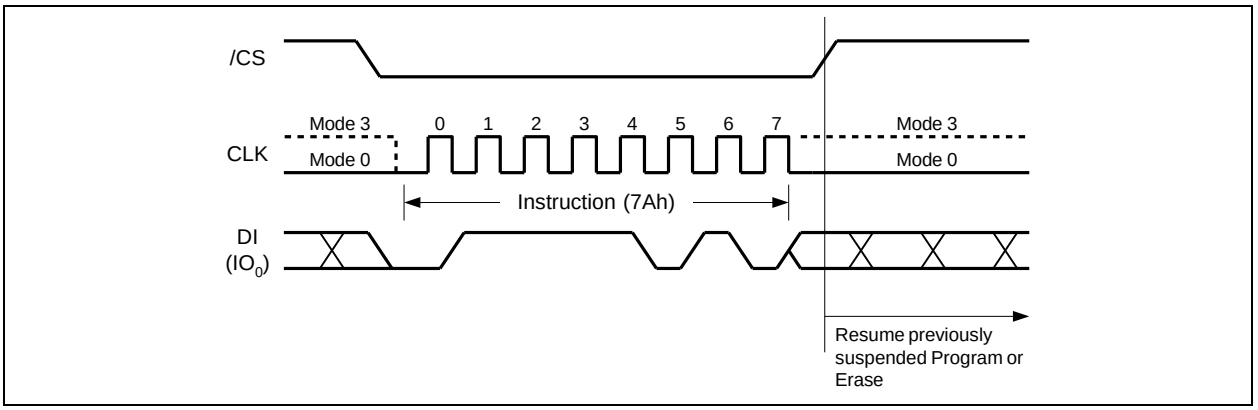



Figure 6.4.38a. Erase/Program Resume Instruction (SPI Mode)

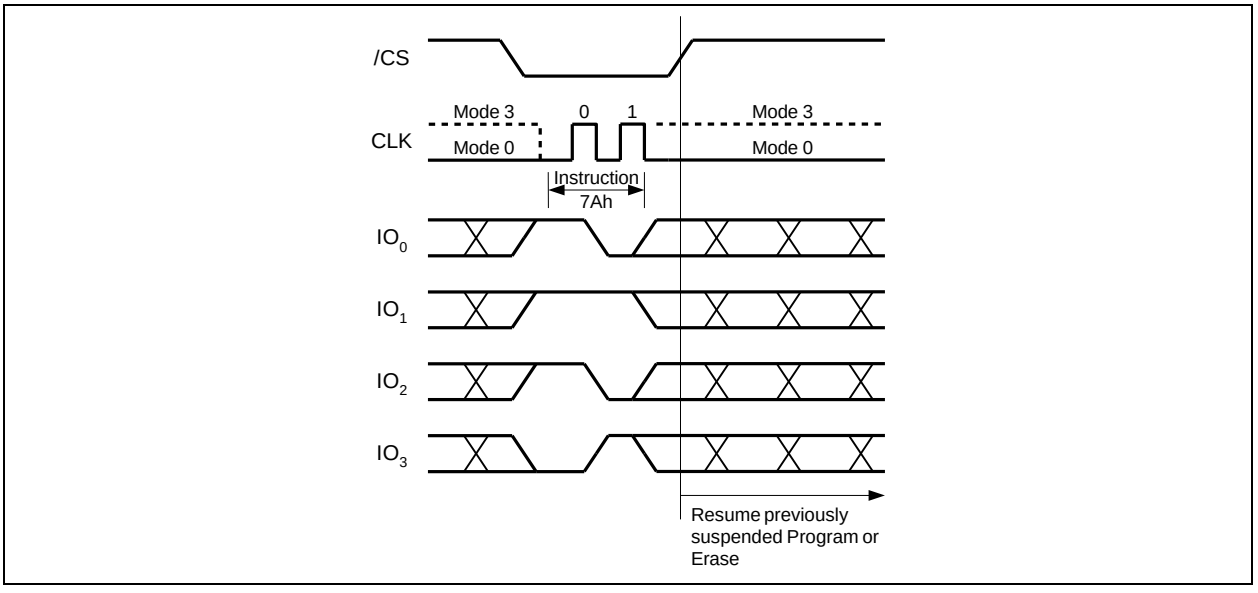



Figure 6.4.38b. Erase/Program Resume Instruction (QPI Mode)



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### 6.4.39 Power-down (B9h)

Although the standby current during normal operation is relatively low, the standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code “B9h” as shown in Figure 6.4.39.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done, the Power-down instruction will not be executed. After /CS is driven high, the power-down state will be entered within the time duration of $t_{DP}$ (See AC Characteristics). While in the power-down state, only the Release Power-down (ABh) instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in normal operation with the standby current of ICC1.

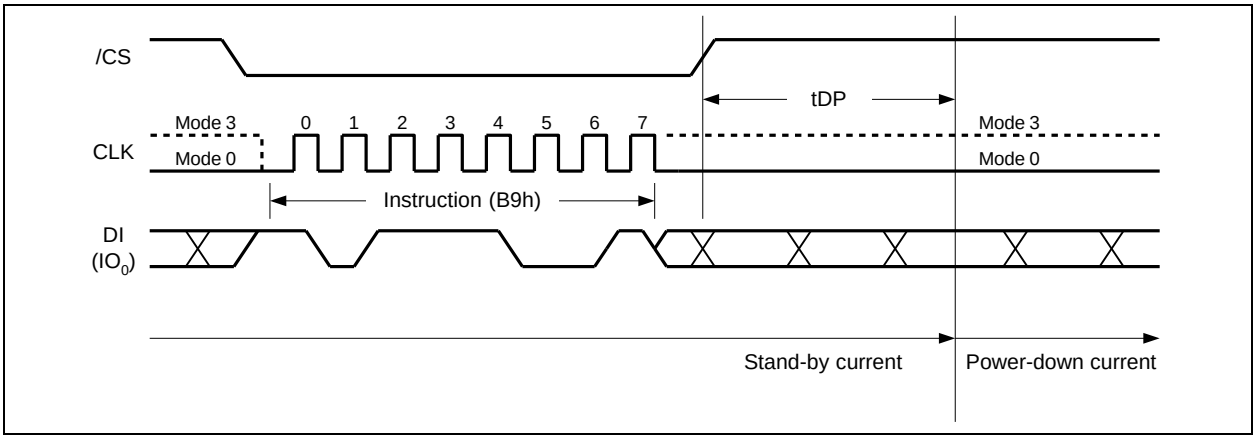



Figure 6.4.39a. Deep Power-down Instruction (SPI Mode)

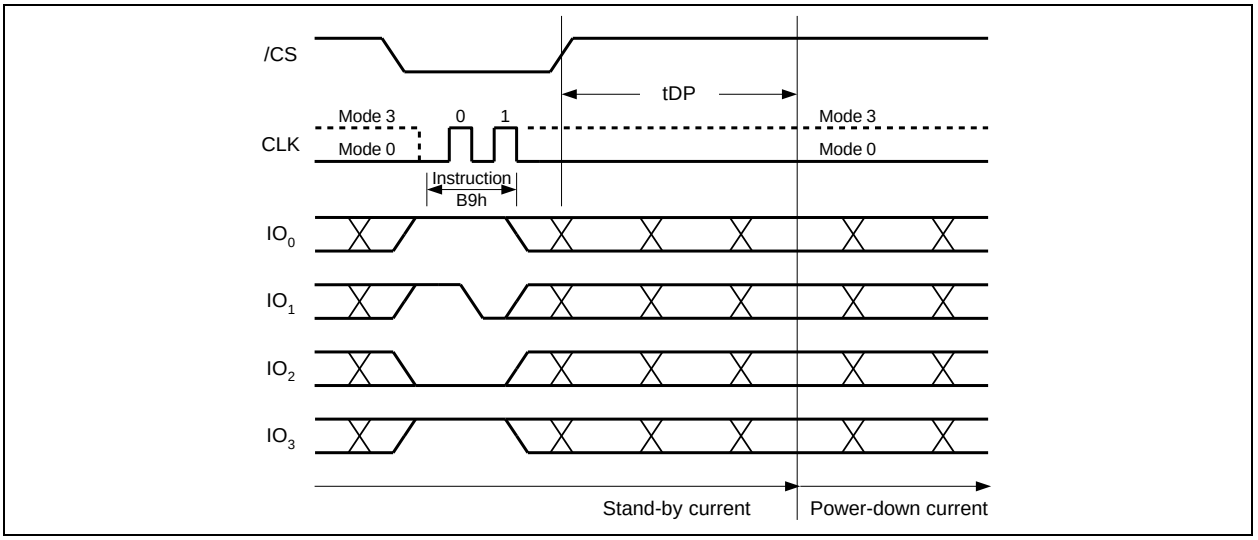



Figure 6.4.39b. Deep Power-down Instruction (QPI Mode)



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### 6.4.40 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high as shown in Figure 6.4.40a & b. Release from power-down will take a time of $t_{RES1}$ (See AC Characteristics) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the $t_{RES1}$ time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first. The Device ID values for the W25Q SERIALS are listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in Figure 6.4.40c & d, except that after /CS is driven high, it must remain high for a time duration of $t_{RES2}$ (See AC Characteristics). After this time duration, the device will resume normal operation, and other instructions will be accepted. If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1), the instruction is ignored and will not have any effect on the current cycle.

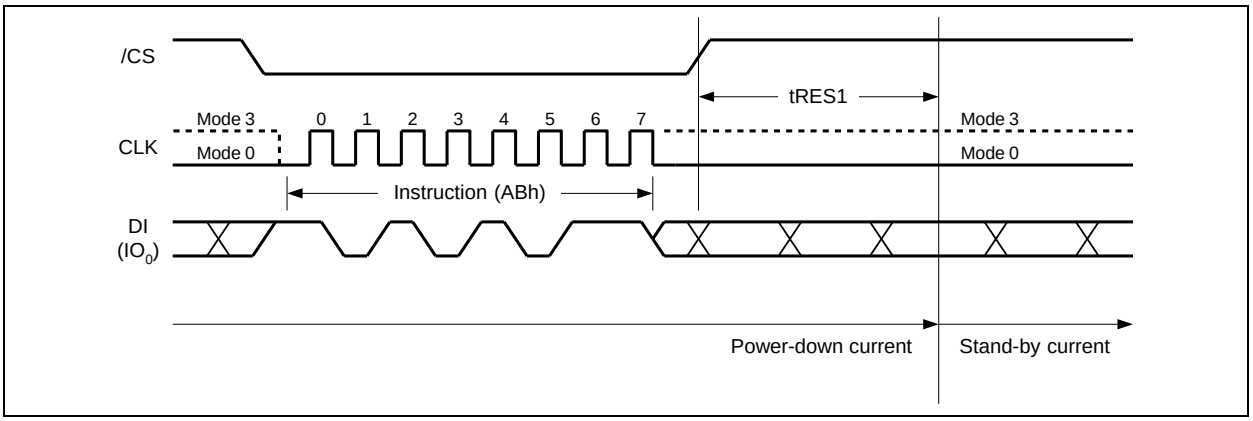



Figure 6.4.40a. Release Power-down Instruction (SPI Mode)

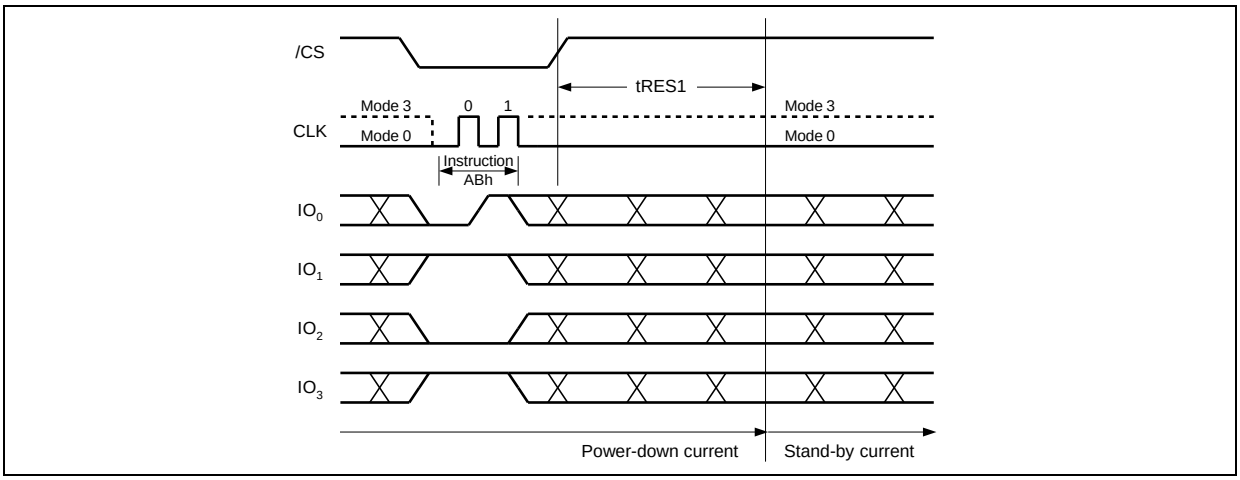



Figure 6.4.40b. Release Power-down Instruction (QPI Mode)



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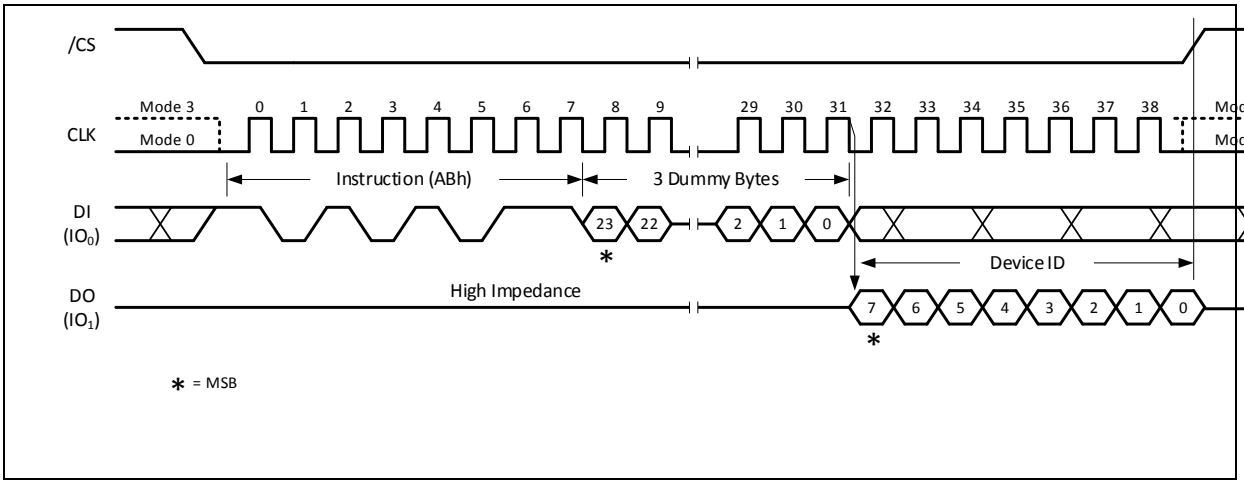



Figure 6.4.40c Device ID Instruction (SPI Mode)

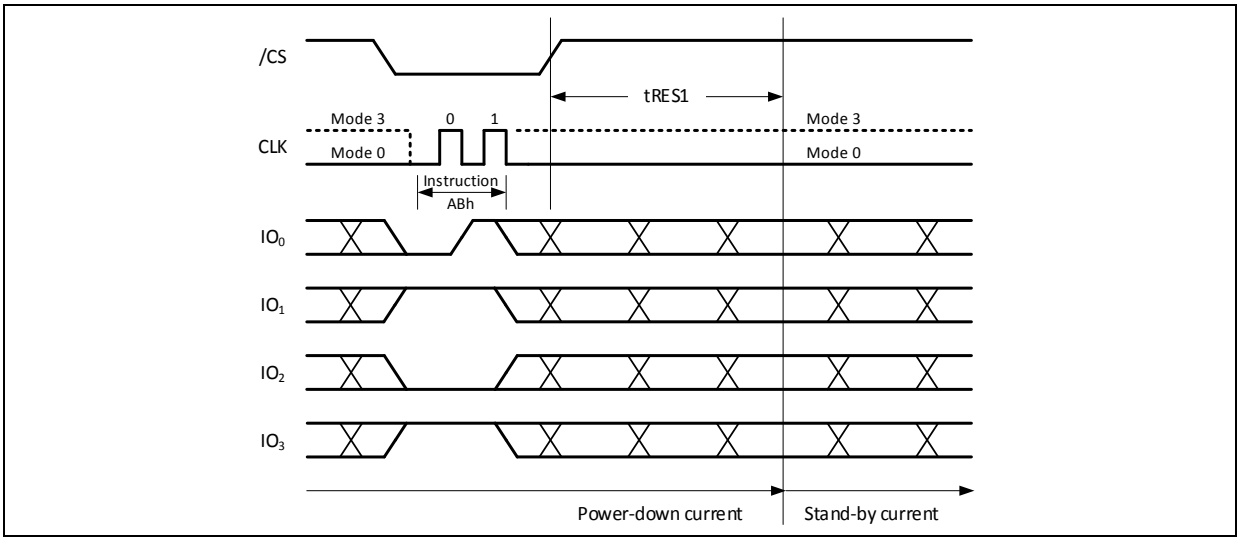



Figure 6.4.40d. Device ID Instruction (QPI Mode)



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### 6.4.41 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out on the falling edge of CLK with the most significant bit (MSB) first as shown in Figure 6.4.41. The Device ID values are listed in Manufacturer and Device Identification table. The instruction is completed by driving /CS high.

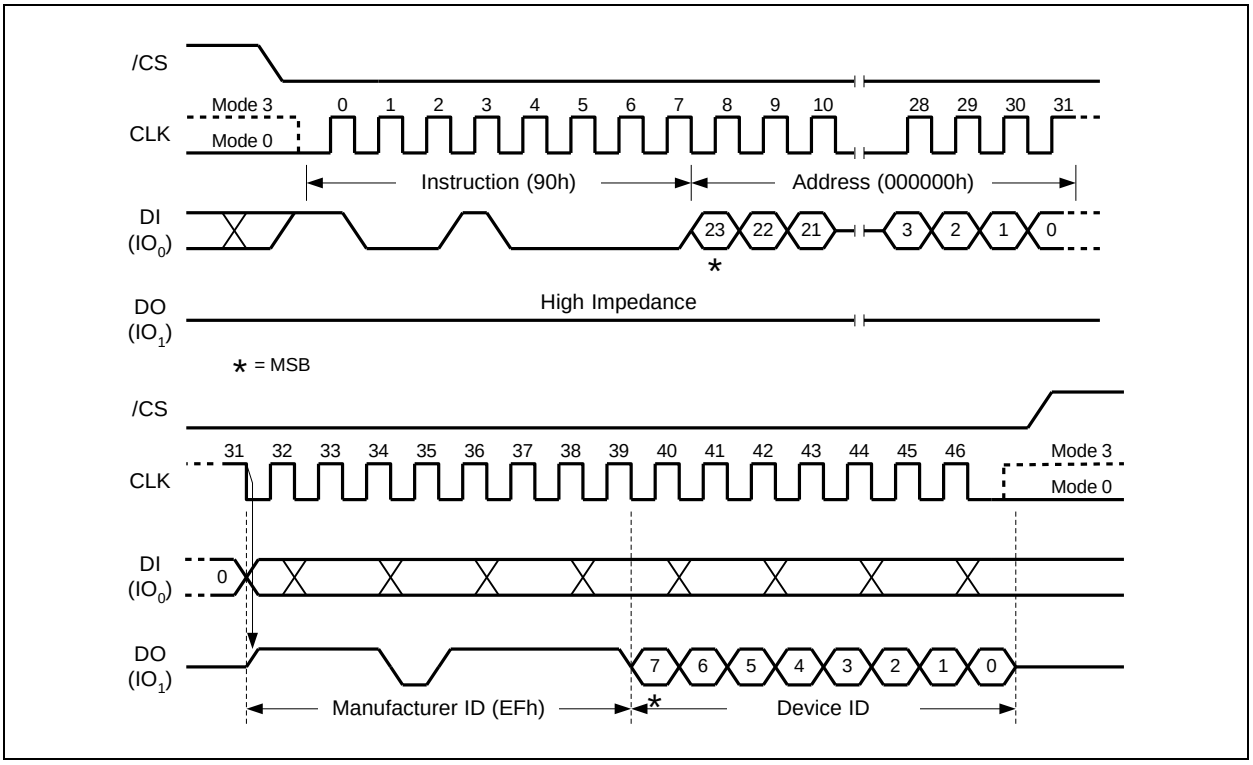



Figure 6.4.41. Read Manufacturer / Device ID Instruction (SPI Mode)



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### 6.4.42 Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “92h” followed by a 24/32-bit address (A23/A31-A0) of 000000h, but with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown in Figure 6.4.42. The Device ID values are listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

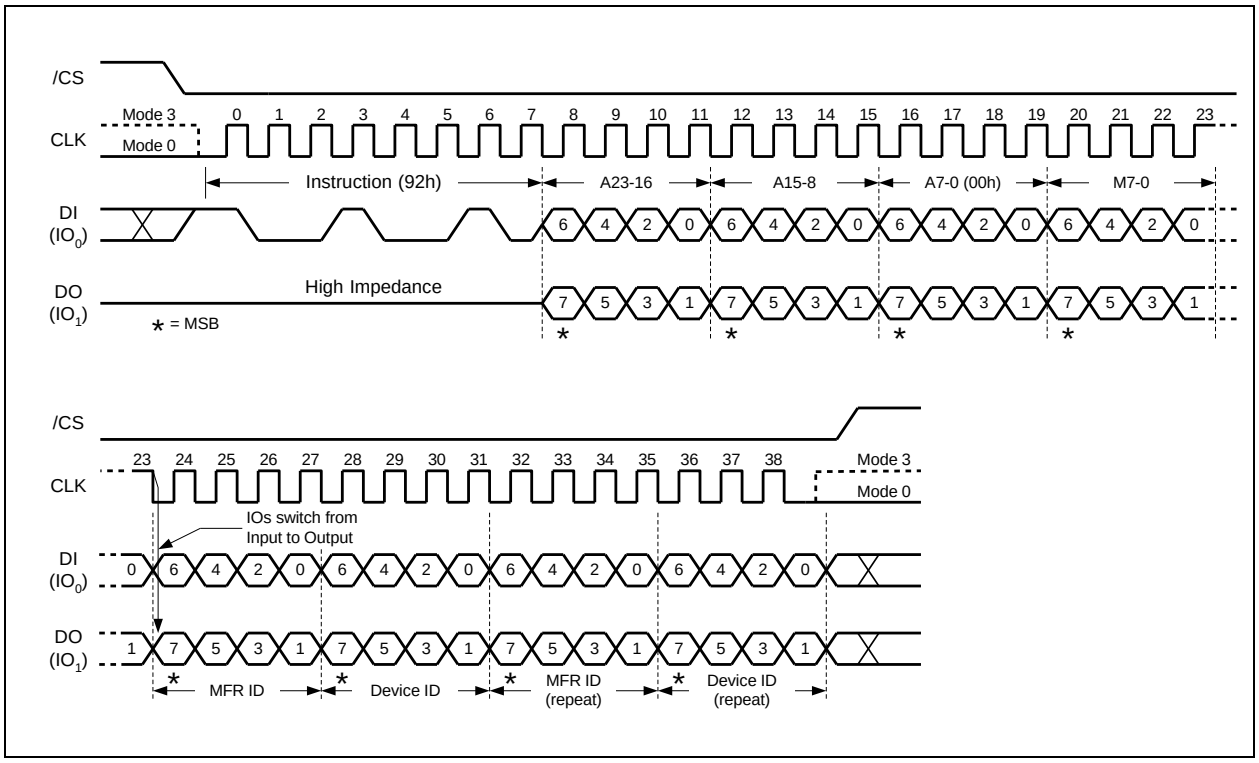



Figure 6.4.42. Read Manufacturer / Device ID Dual I/O Instruction (SPI Mode only)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*

Note:

The Read Command Bypass Mode bits M(7-0) must be set to Fxh to be compatible with Fast Read Dual I/O instruction.



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### 6.4.43 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O instruction is similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “94h” followed by a four clock dummy cycles and then a 24/32-bit address (A23/A31-A0) of 000000h, but with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out four bits per clock on the falling edge of CLK with the most significant bit (MSB) first as shown in Figure 6.4.43. The Device ID values are listed in the Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

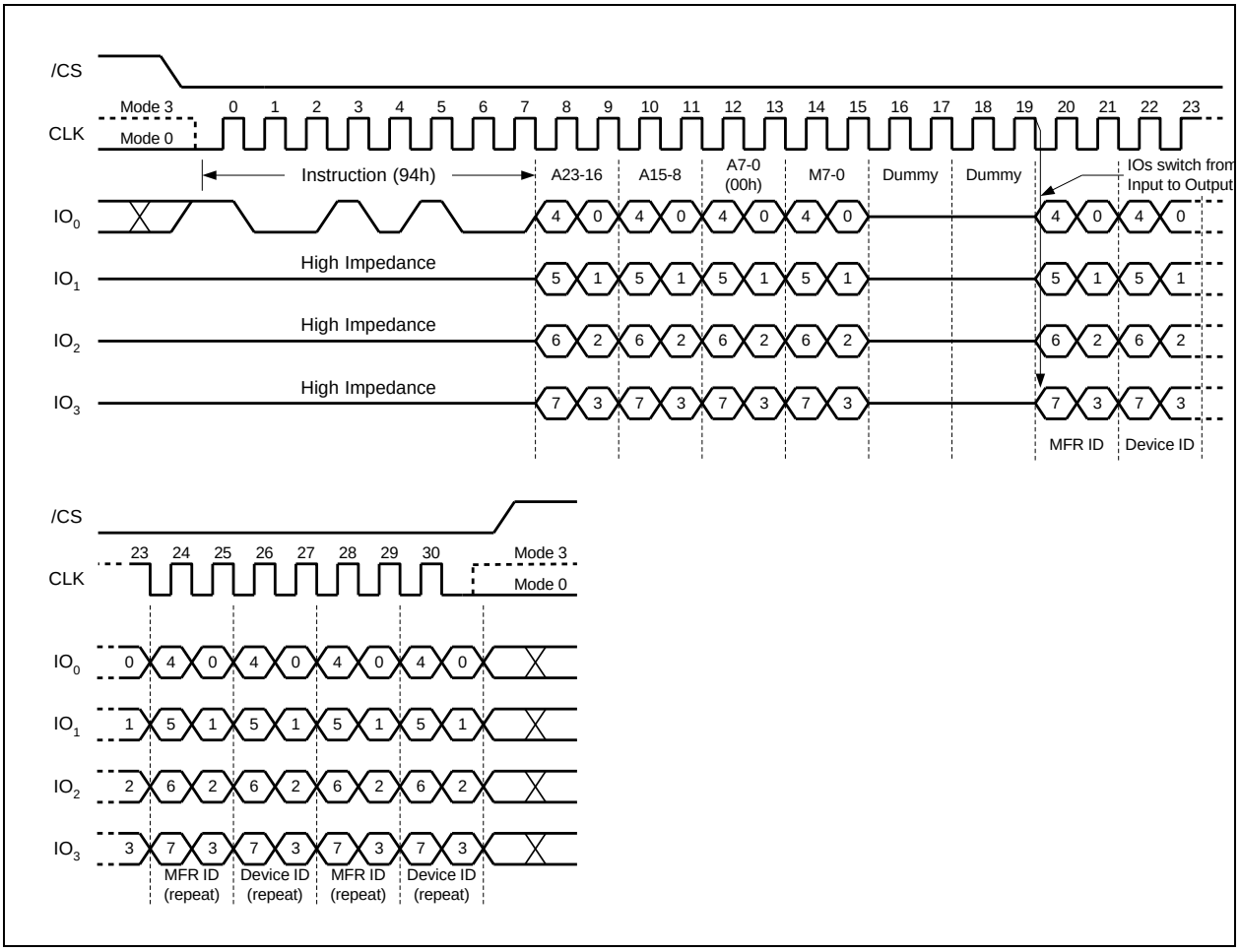



Figure 6.4.43. Read Manufacturer / Device ID Quad I/O Instruction (SPI Mode only)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*

**Note:** The Read Command Bypass Mode bits M(7-0) must be set to Fxh to be compatible with Fast Read Quad I/O instruction.



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### 6.4.44 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code “4Bh” followed by four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of CLK as shown in Figure 6.4.44.

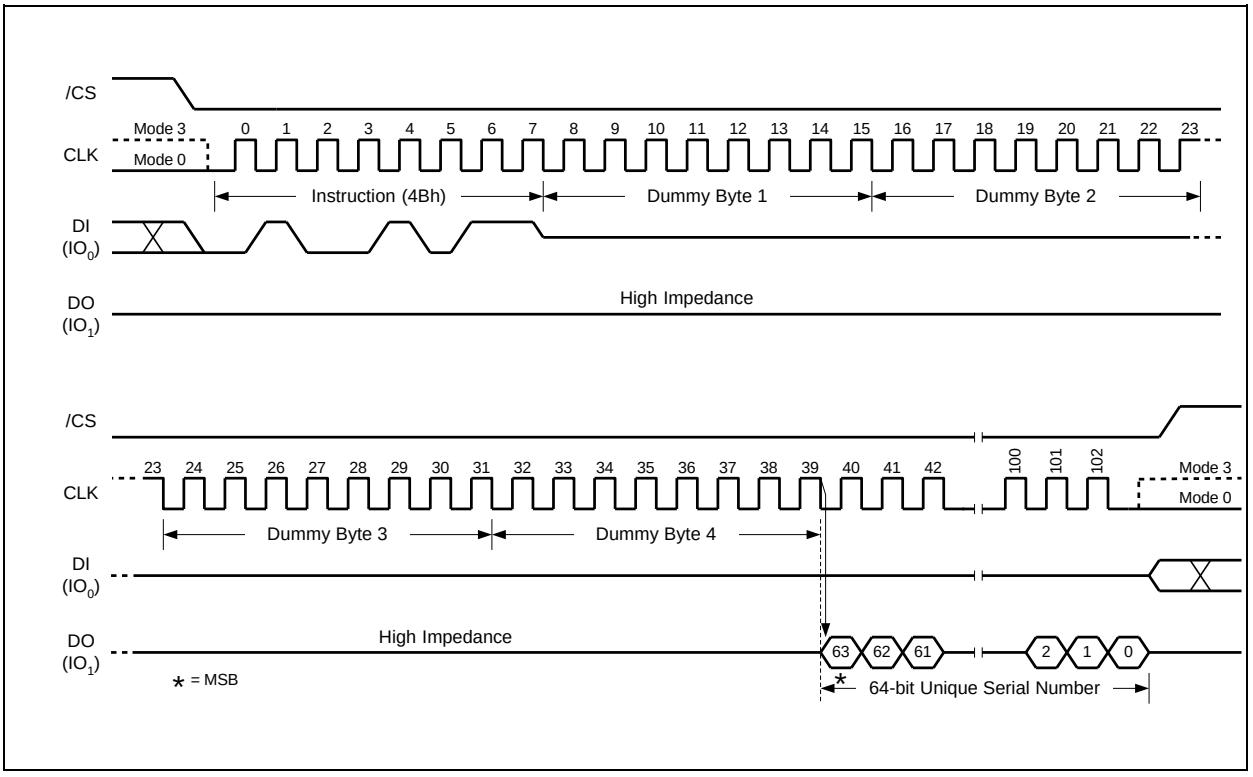



Figure 6.4.44. Read Unique ID Number Instruction (SPI Mode only)

*5 Dummy Bytes are required when the device is operating in 4-Byte Address Mode*



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### 6.4.45 Read JEDEC ID (9Fh)

For compatibility reasons, the W25QxxRV provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for Winbond (EFh) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with the most significant bit (MSB) first as shown in Figure 6.4.45. For memory type and capacity values refer to the Manufacturer and Device Identification table.

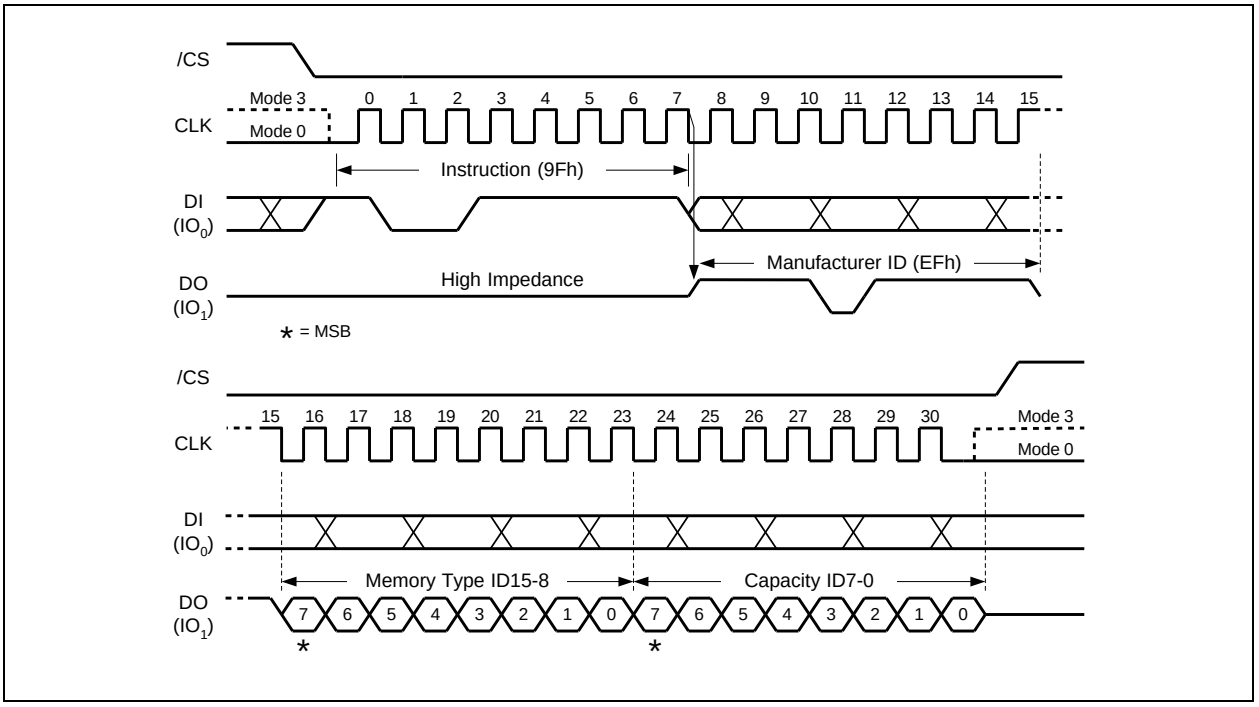



Figure 6.4.45a. Read JEDEC ID Instruction (SPI Mode)

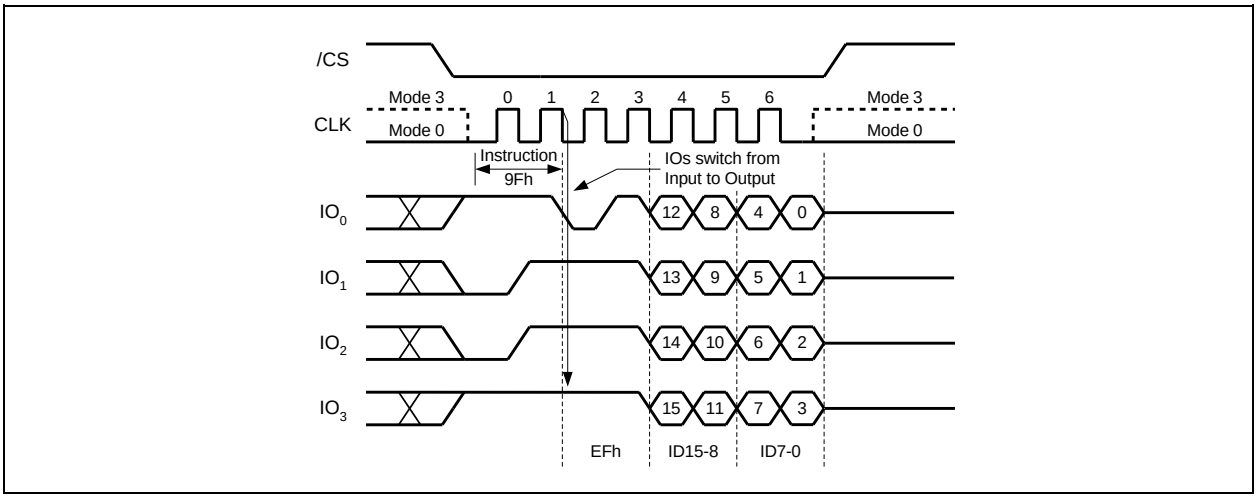



Figure 6.4.45b. Read JEDEC ID Instruction (QPI Mode)



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### 6.4.46 Read SFDP Register (5Ah)

The W25QxxRV features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available instructions and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified, but more may be added in the future. The Read SFDP Register instruction is compatible with the SFDP standard initially established in 2010 for PC and other applications, as well as the JEDEC standard JESD216-Serials that is published in 2011. Most Winbond SpiFlash Memories shipped after June 2011 (date code 1124 and beyond) support the SFDP feature as specified in the applicable datasheet.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code "5Ah" followed by a 24-bit address (A23-A0)(1) into the DI pin. Eight "dummy" clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with most significant bit (MSB) first as shown in Figure 6.4.46. For SFDP register values and descriptions, please refer to the Winbond Application Note for SFDP Definition Table.

Note: 1. A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.

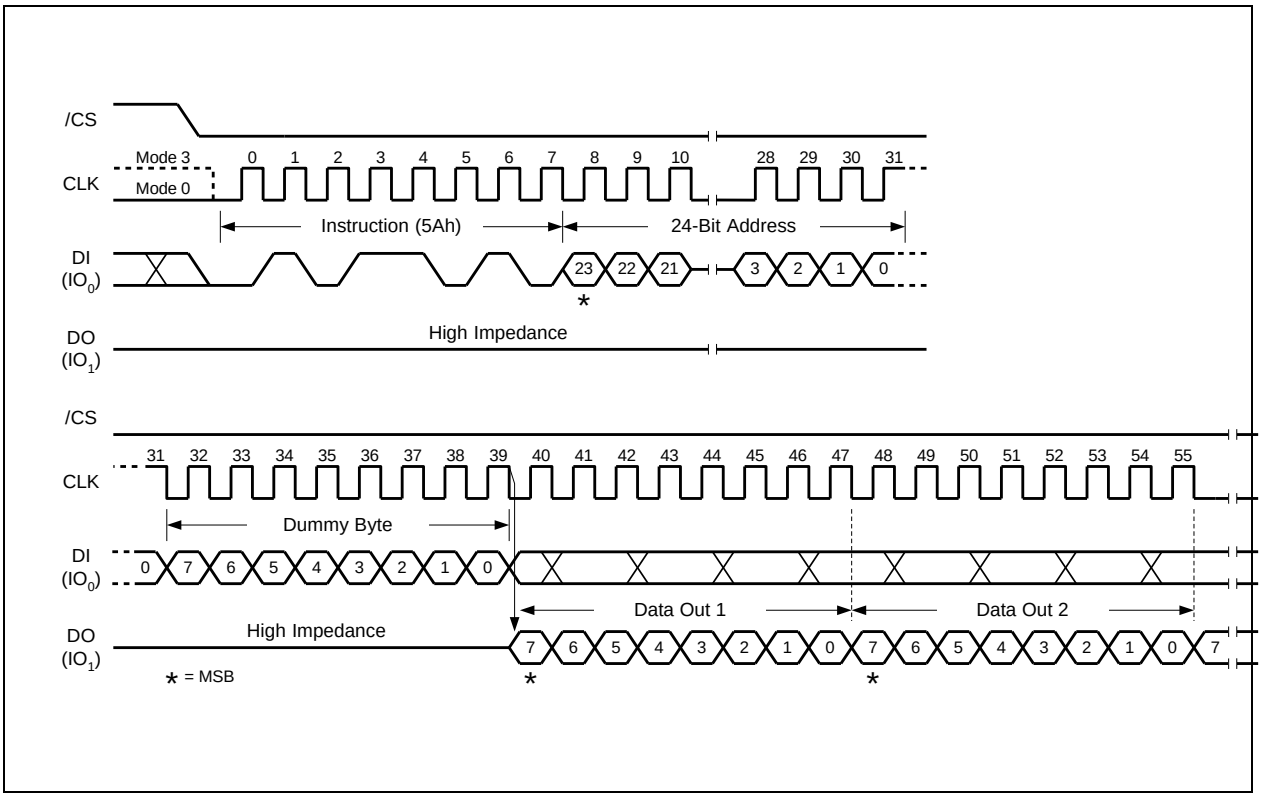



Figure 6.4.46. Read SFDP Register Instruction Sequence Diagram (SI Mode only)

*Only 24-Bit Address is required when the device is operating in either 3-Byte or 4-Byte Address Mode*



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**Read SFDP Register (5Ah) in QPI Mode**

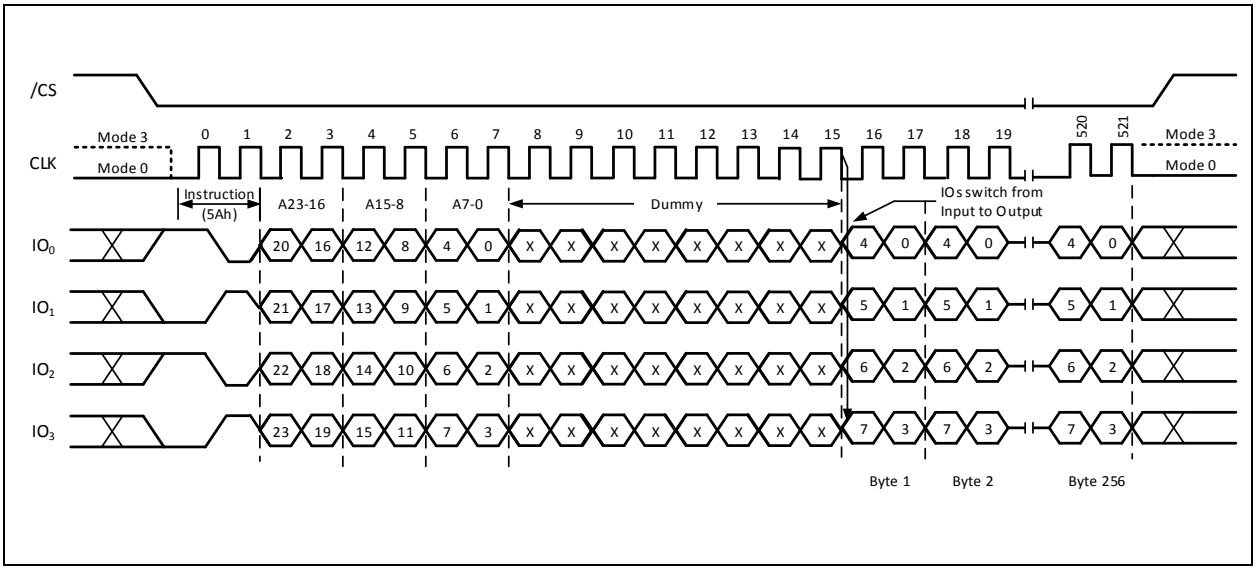



Figure 6.4.46. Read SFDP Register Instruction Sequence Diagram (QPI Mode only)

*Only 24-Bit Address is required when the device is operating in either 3-Byte or 4-Byte Address Mode*



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### 6.4.47 Erase Security Registers (44h)

The W25QxxRV offers three 256-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register instruction is similar to the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase Security Register Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "44h" followed by a 24/32-bit address (A23/A31-A0) to erase one of the three security registers.

| ADDRESS | {A23/A31}-16 | A15-12 | A11-8 | A7-0 |
|---|---|---|---|---|
| Security Register #1 | 00h/0000h | 0 0 0 1 | 0 0 0 0 | Don't Care |
| Security Register #2 | 00h/0000h | 0 0 1 0 | 0 0 0 0 | Don't Care |
| Security Register #3 | 00h/0000h | 0 0 1 1 | 0 0 0 0 | Don't Care |

The Erase Security Register instruction sequence is shown in Figure 6.4.47. The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the instruction will not be executed. After /CS is driven high, the self-timed Erase Security Register operation will commence for a time duration of $t_{SE}$ (See AC Characteristics). While the Erase Security Register cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished, and the device is ready to accept other instructions again. After the Erase Security Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB[3:1]) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, and the Erase Security Register instruction to that register will be ignored (Refer to the link "5.3.10 Security Register Lock Bits (LB3, LB2, LB1, SFDP Lock) –Non-Volatile *OTP Writable*").

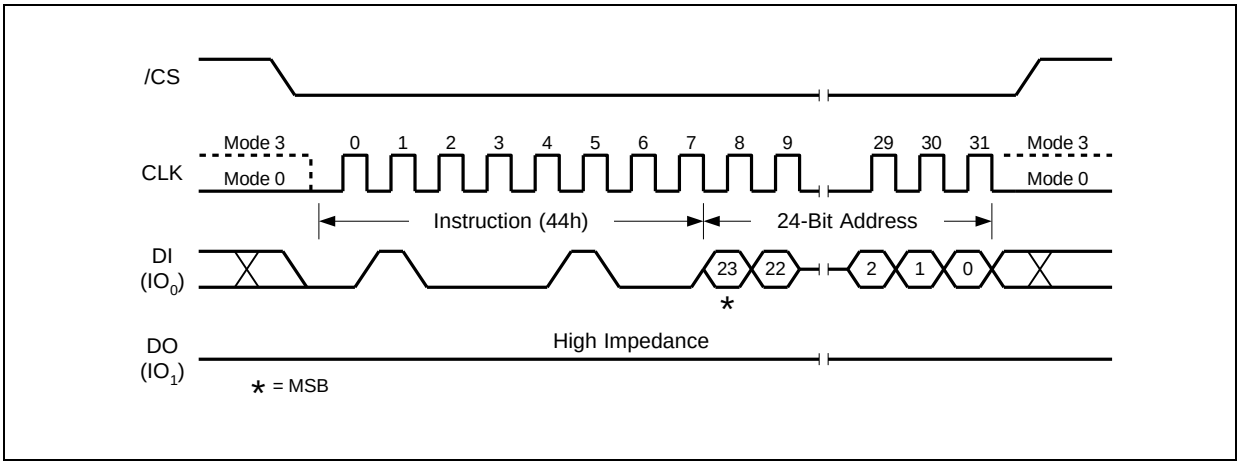



Figure 6.4.47. Erase Security Registers Instruction (SPI Mode only)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.48 Program Security Registers (42h)

The Program Security Register instruction is similar to the Page Program instruction. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Register Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “42h” followed by a 24/32-bit address (A23/A31-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

| ADDRESS | {A23/A31}-16 | A15-12 | A11-8 | A7-0 |
|---|---|---|---|---|
| Security Register #1 | 00h/0000h | 0 0 0 1 | 0 0 0 0 | Byte Address |
| Security Register #2 | 00h/0000h | 0 0 1 0 | 0 0 0 0 | Byte Address |
| Security Register #3 | 00h/0000h | 0 0 1 1 | 0 0 0 0 | Byte Address |

The Program Security Register instruction sequence is shown in Figure 6.4.48. The Security Register Lock Bits (LB[3:1]) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Program Security Register instruction to that register will be ignored (See 7.1.8 for detail descriptions).

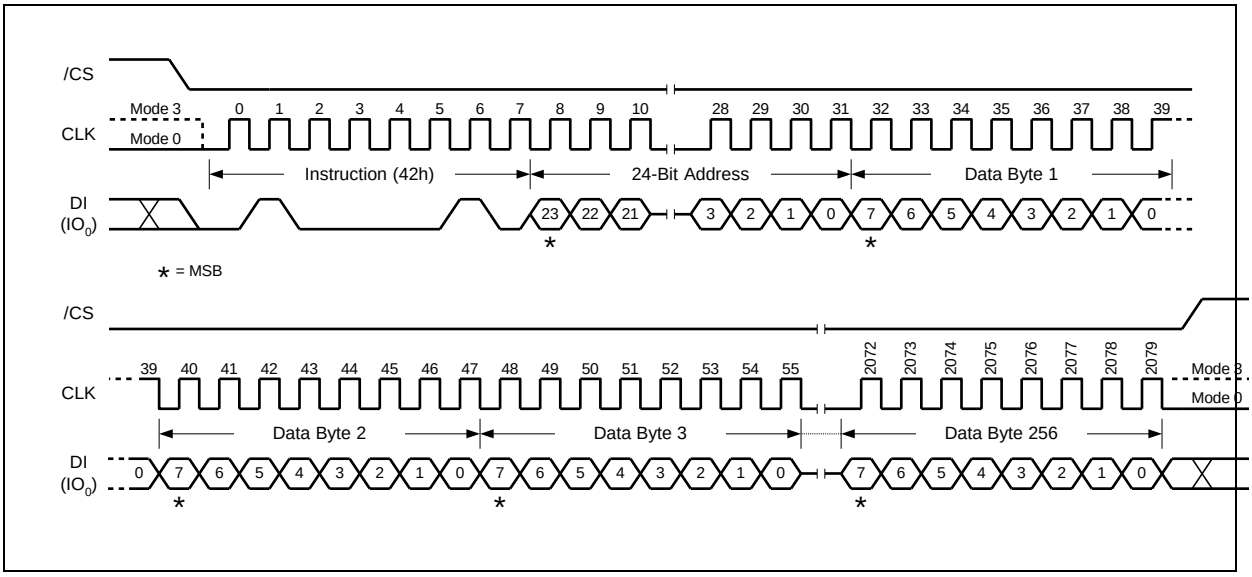



Figure 6.4.48. Program Security Registers Instruction (SPI Mode only)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.49 Read Security Registers (48h)

The Read Security Register instruction is similar to the Fast Read instruction and allows one or more data bytes to be sequentially read from one of the three security registers. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “48h” followed by a 24/32-bit address (A23/A31-A0) and eight “dummy” clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte address FFh), it will reset to address 00h, the first byte of the register, and continue to increment. The instruction is completed by driving /CS high. The Read Security Register instruction sequence is shown in Figure 6.4.48. If a Read Security Register instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1), the instruction is ignored and will not have any effect on the current cycle. The Read Security Register instruction allows clock rates from D.C. to a maximum of FR (see AC Electrical Characteristics).

| ADDRESS | {A23/A31}-16 | A15-12 | A11-8 | A7-0 |
|---|---|---|---|---|
| Security Register #1 | 00h/0000h | 0 0 0 1 | 0 0 0 0 | Byte Address |
| Security Register #2 | 00h/0000h | 0 0 1 0 | 0 0 0 0 | Byte Address |
| Security Register #3 | 00h/0000h | 0 0 1 1 | 0 0 0 0 | Byte Address |

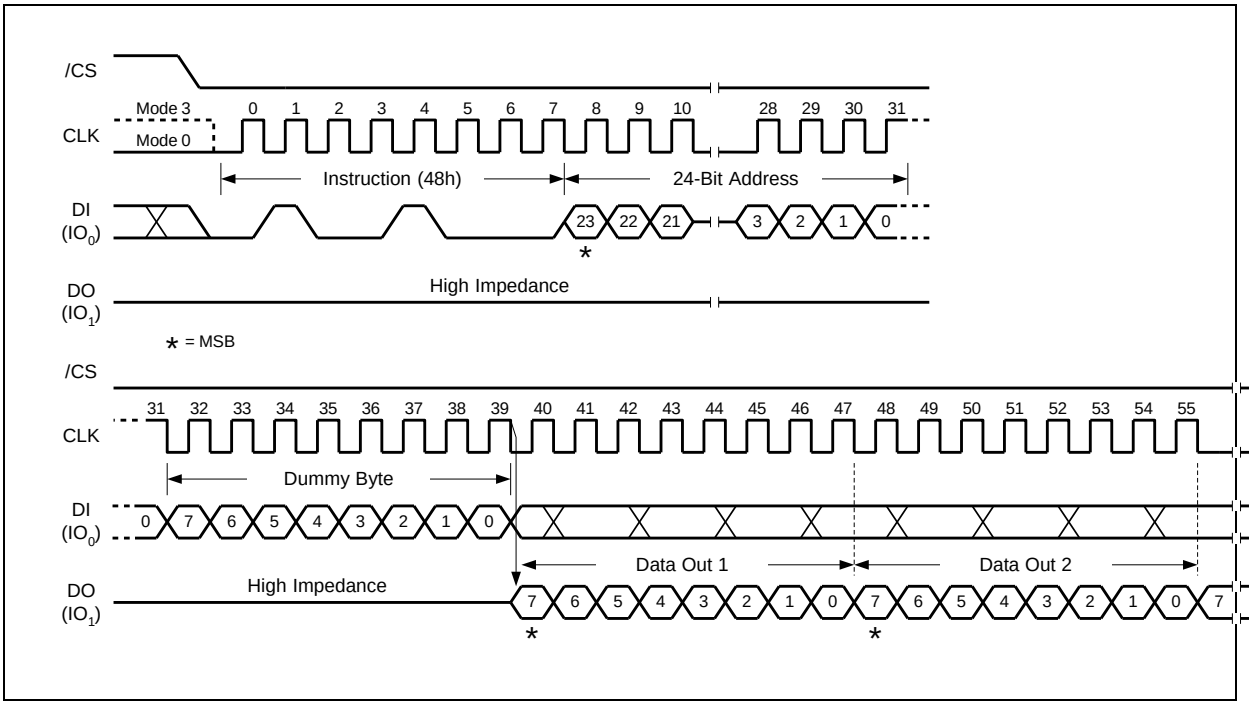



Figure 6.4.49. Read Security Registers Instruction (SPI Mode only)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.50 Set Read Parameters (C0h)

The “Set Read Parameters (C0h)” instruction is used to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency. This is accomplished by setting the number of dummy clocks and wrap length configurations for set of selected instructions. Set Read Parameters (C0h) instruction writes to the Read Parameter Register (P[7:0]). P[6:4] bits is the dummy clocks configuration, while P[1:0] bits is the wrap length configuration for QPI mode only.

In SPI mode, SPI Set Read Parameters (C0h)" instruction writes to ‘Dummy Clocks’ P[6:4] bits only, while it will ignore ‘Wrap Length’ P[1:0] bits input as they are don’t care in SPI mode. Conversely, QPI Set Read Parameters instruction will write both to the P[6:4] and P[1:0] Read Parameter bits. The Set Read Parameters instruction sequence is shown in Figure 6.4.50.

Set Read Parameters instruction (SPI or QPI or DTR) is used to configure **the number of dummy cycles** through P[6:4] Read Parameter bits for the following SPI, QPI, SPI DTR, and QPI DTR instructions:

- **Standard SPI mode:**
  Fast Read Quad I/O (EBh)
  Fast Read Quad I/O with 4-Byte Address (ECh)

- **QPI mode:**
  Fast Read (0Bh)
  Read Checksum (9Ch)
  Fast Read Quad I/O (EBh)
  Burst Read with Wrap (0Ch)
  Fast Read Quad I/O with 4-Byte Address (ECh)

  **SPI DTR mode:**
  DTR Fast Read Quad I/O (EDh)
  DTR Fast Read Quad I/O with 4-Byte Address (EEh)

- **QPI DTR mode:**
  DTR Fast Read (0Dh)
  DTR Burst Read with Wrap (0Eh)
  DTR Fast Read Quad I/O (EDh)
  DTR Fast Read Quad I/O with 4-Byte Address (EEh)

In QPI mode only, Set Read Parameters instruction to P[1:0] Read Parameter bits is used to configure the “**Wrap Length**” for the following QPI and QPI DTR read with wrap instructions:

- **QPI mode:**
  Burst Read with Wrap (0Ch) instruction

- **QPI DTR mode:**
  DTR Burst Read with Wrap (0Eh) instruction.

The Wrap bits (Set Burst with Wrap ‘77h’) as well as Read Parameter bits P[7:0] setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode or vice versa. It is very important that the required dummy cycles and wrap length are set properly before executing the SPI (EBh, ECh), QPI (0Bh, 9Ch, 0Ch, EBh, ECh), SPI DTR (EDh, EEh), and QPI DTR (0Dh, EDh, 0Eh, EEh) instructions.

The default Parameter Read “Dummy Clocks” and “Wrap Length“ settings for selected SPI, QPI, DTR, and QPI DTR read instructions after power up or reset are defined in the tables below. After power up or reset, Read Parameter bits are reset to 00h. Detailed Read Parameter bits configuration are also shown below.


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**QPI/QPI DTR Wrap Length:** QPI: 0Ch /QPI DTR: 0Eh

| P1 – P0 | WRAP LENGTH (QPI: 0Ch ; QPI DTR: 0Eh) |
|---|---|
| 0 0 | 8-byte(1) |
| 0 1 | 16-byte |
| 1 0 | 32-byte |
| 1 1 | 64-byte |

### Dummy Clocks and Wrap Length Configurations

**SPI/QPI Dummy Clocks*:* SPI: EBh/ECh or QPI: 0Bh/EBh/0Ch/ECh/9Ch- *W25Q33RV/64RV/12RV***

| SPI / QPI | | QPI | | QPI | | SPI / QPI | |
|---|---|---|---|---|---|---|---|
| Address Mode | | Fast Read /Read Checksum | | Burst Read With Wrap | | Fast Read Quad I/O | |
| 3-/4-byte Address | | 0Bh / 9Ch | | x | | EBh(2) | |
| Fixed 4-byte Address | | X | | 0Ch | | ECh (2) | |
| Starting Address(1) | | Aligned | Any | Aligned | Any | Aligned | Any |
| Dummy Cycle | 6(Def.)(3) | 133 | 104 | 133 | 104 | 133 | 104 |
| | 8 | 133 | 104 | 133 | 104 | 133 | 104 |
| | 10 | 133 | 104 | 133 | 104 | 133 | 104 |
| | 12–16 | 166 | 133 | 166 | 133 | 166 | 133 |

**DTR Dummy Clocks: SPI DTR: EDh/EEh and QPI DTR: 0Dh/0Eh/EDh/EEh- *W25Q33RV/64RV/12RV***

| SPI_DTR / QPI_DTR | | QPI_DTR | | QPI_DTR | | SPI_DTR / QPI_DTR | |
|---|---|---|---|---|---|---|---|
| Address Mode | | Fast Read | | Burst Read With Wrap | | Fast Read Quad I/O | |
| 3-/4-byte Address Mode | | 0Dh | | 0Eh | | EDh(2) | |
| Fixed 4-byte Address | | X | | X | | EEh(2) | |
| Starting Address(1) | | Aligned | Any | Aligned | Any | Aligned | Any |
| Dummy Cycle | 8(Def.)(3) | 84 | 66 | 84 | 66 | 84 | 66 |
| | 10 | 84 | 66 | 84 | 66 | 84 | 66 |
| | 12–16 | 104 | 84 | 104 | 84 | 104 | 84 |

**Notes**:

1. Aligned: 4-bytes address alignment for Read, read address start from A1,A0=0,0.
   Any: no alignment requirements; reads may begin at any address.
2. EB, ECh, EDh and EEh support “Read Command Bypass Mode”. When the M7–M0 is set to Fxh, Read Command Bypass Mode is disabled, and M7–M0 is treated as the dummy-cycle field.
3. Default from power up



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### SPI/QPI Dummy Clocks: SPI: EBh/ECh or QPI: 0Bh/EBh/0Ch/ECh/9Ch- *W25Q25/51RV/01RV/02RV*

| SPI / QPI | | QPI | | QPI | | SPI / QPI | |
|---|---|---|---|---|---|---|---|
| **Address Mode** | | **Fast Read /Read Checksum** | | **Burst Read With Wrap** | | **Fast Read Quad I/O** | |
| 3-/4-byte Address | | 0Bh / 9Ch | | x | | EBh(2) | |
| Fixed 4-byte Address | | X | | 0Ch | | ECh(2) | |
| Starting Address(1) | | Aligned | Any | Aligned | Any | Aligned | Any |
| Dummy Cycle | 6(Def.)(3) | 104 | 66 | 104 | 66 | 104 | 66 |
| | 8 | 133 | 66 | 133 | 66 | 133 | 66 |
| | 10 | 133 | 66 | 133 | 66 | 133 | 66 |
| | 12–16 | 133 | 84 | 133 | 84 | 133 | 84 |

### DTR Dummy Clocks: SPI DTR: EDh/EEh and QPI DTR: 0Dh/0Eh/EDh/EEh- *W25Q25/51RV/01RV/02RV*

| SPI_DTR / QPI_DTR | | QPI_DTR | | QPI_DTR | | SPI_DTR / QPI_DTR | |
|---|---|---|---|---|---|---|---|
| **Address Mode** | | **Fast Read** | | **Burst Read With Wrap** | | **Fast Read Quad I/O** | |
| 3-/4-byte Address Mode | | 0Dh | | 0Eh | | EDh(2) | |
| Fixed 4-byte Address | | X | | X | | EEh(2) | |
| Starting Address(1) | | Aligned | Any | Aligned | Any | Aligned | Any |
| Dummy Cycle | 8(Def.)(3) | 84 | 50 | 84 | 50 | 84 | 50 |
| | 10 | 104 | 50 | 104 | 50 | 84 | 50 |
| | 12–16 | 104 | 66 | 104 | 66 | 104 | 66 |

**Notes**:

1. Aligned: 4-bytes address alignment for Read, read address start from A1,A0=0,0.
   Any: no alignment requirements; reads may begin at any address.
2. EDh and EEh support “Read Command Bypass Mode”. When the M7–M0 is set to Fxh, Read Command Bypass Mode is disabled, and M7–M0 is treated as the dummy-cycle field.
3. Default from power up


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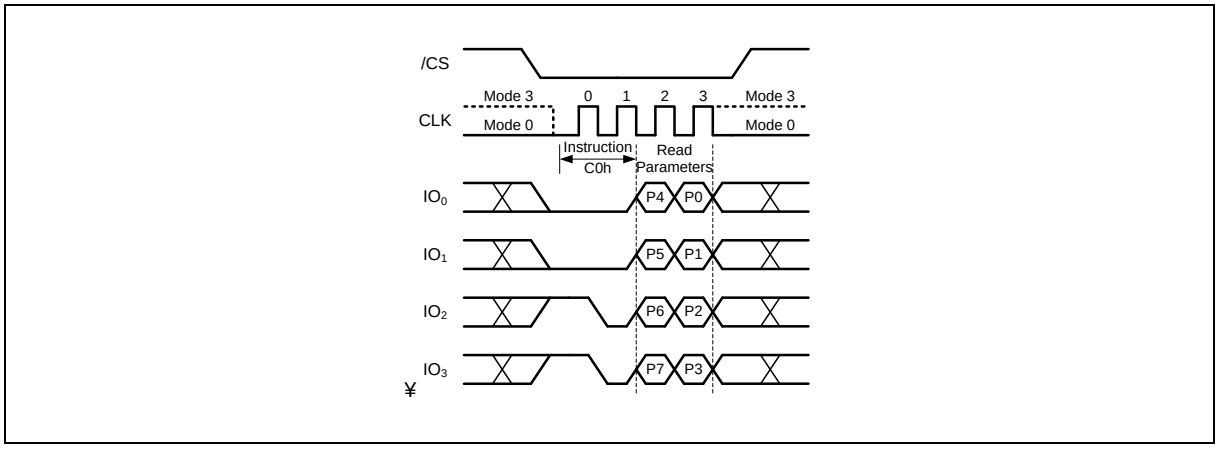



Figure 6.4.50a. Set Read Parameters (C0h) Instruction for QPI Mode

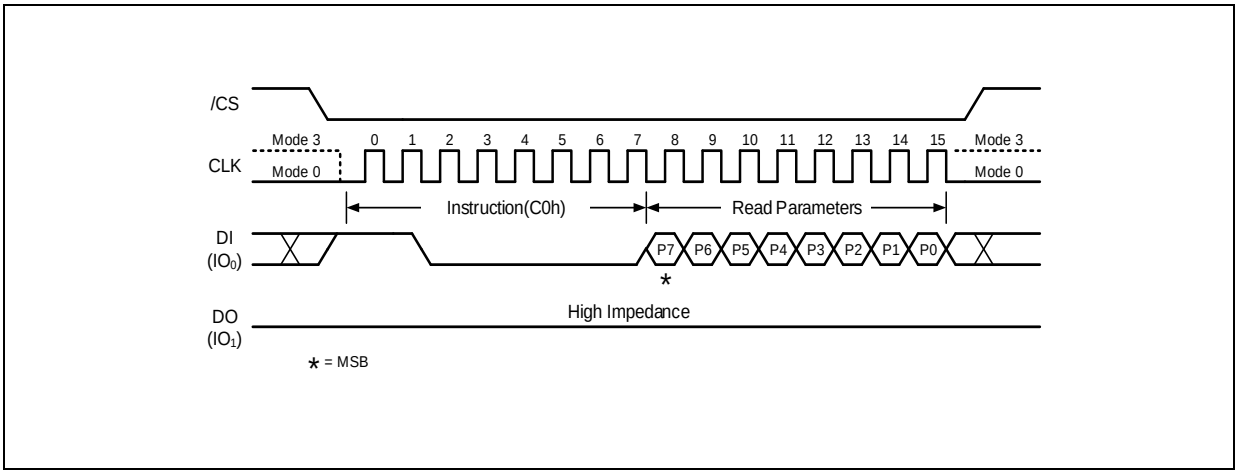



Figure *6.4.50b*. Set Read Parameters (C0h) Instruction for SPI Mode

***** SPI Set Read Parameters(C0h) instruction writes to "Dummy Clock" P[6:4] bit only. It will ignore Warp Length P[0:1] bits input was they are don't care in SPI mode.



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### 6.4.51 Burst Read with Wrap (0Ch)

The “Burst Read with Wrap (0Ch)” instruction provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. The instruction is similar to the “Fast Read (0Bh)” instruction in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “Wrap Length” and the number of dummy clocks can be configured by the “Set Read Parameters (C0h)” instruction.

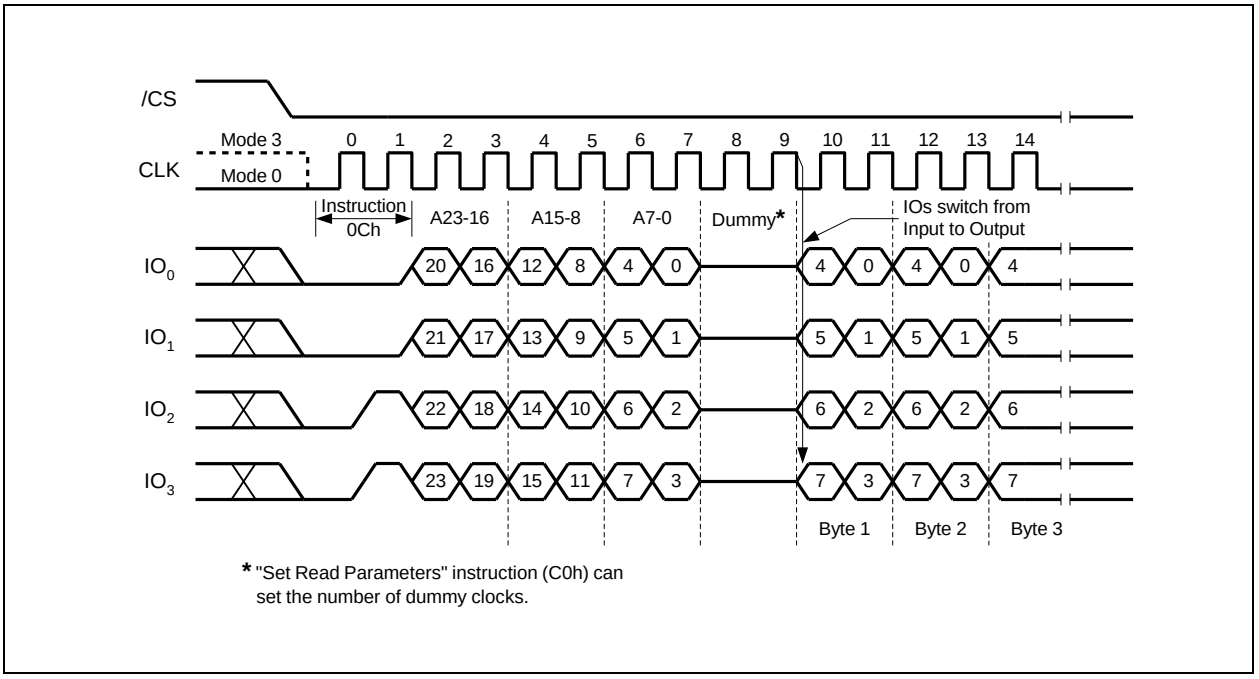



Figure6.4.51. Burst Read with Wrap Instruction (QPI Mode only)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.52 DTR Burst Read with Wrap (0Eh)

The “DTR Burst Read with Wrap (0Eh)” instruction provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. The instruction is similar to the “Fast Read (0Bh)” instruction in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “Wrap Length” can be configured by the “Set Read Parameters (C0h)” instruction.

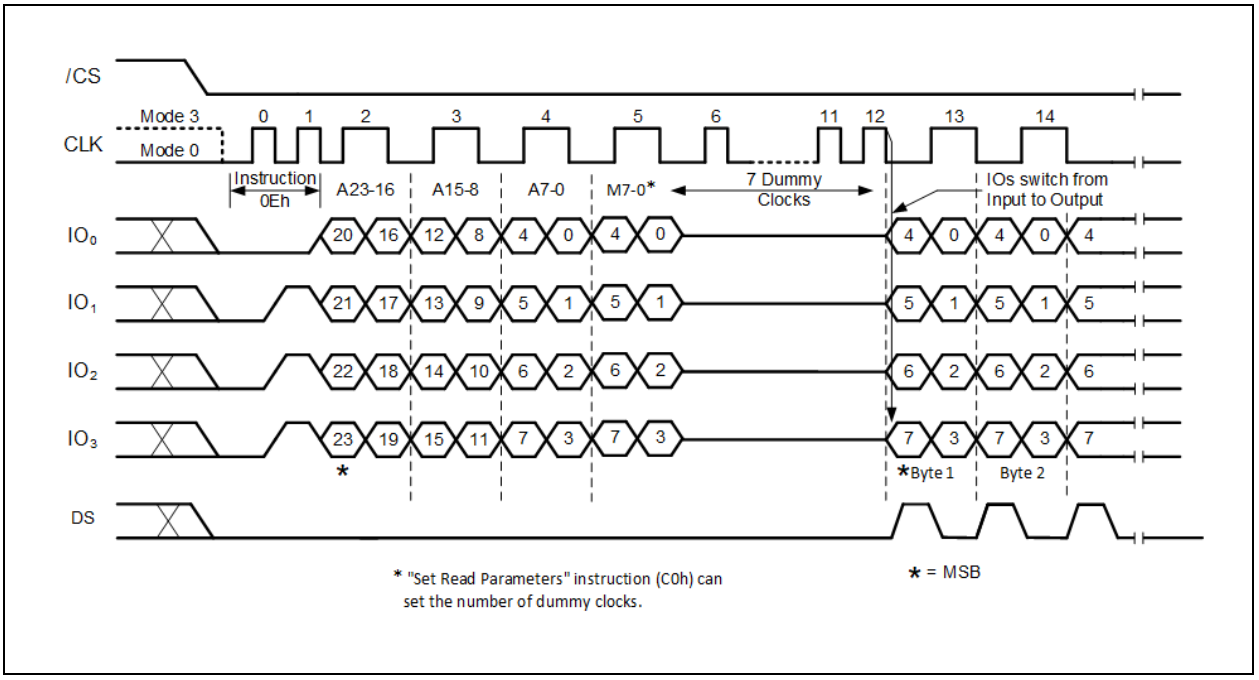



Figure 6.4.52. DTR Burst Read with Wrap Instruction (QPI Mode only)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.53 Enter QPI Mode (38h)

The W25QxxRV supports both Standard/Dual/Quad Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode cannot be used at the same time. “Enter QPI (38h)” instruction is the only way to switch the device from SPI mode to QPI mode.

Upon power-up, the default state of the device upon is Standard/Dual/Quad SPI mode. This provides full backward compatibility with earlier generations of Winbond serial flash memories. See Instruction Set Table 1-4 & 7-8 for all supported SPI commands. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register-2 must be set to 1 first, and an “Enter QPI (38h)” instruction must be issued. If the Quad Enable (QE) bit is 0, the “Enter QPI (38h)” instruction will be ignored, and the device will remain in SPI mode.

Refer to the QPI Instruction Set Table, sections link “6.2.6-6.2.10” & “6.2.13- 6.2.15”for all the commands supported in QPI/QPI DTR Security Register Lock Bits (LB3, LB2, LB1, SFDP Lock) –Non-Volatile *OTP Writable* mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

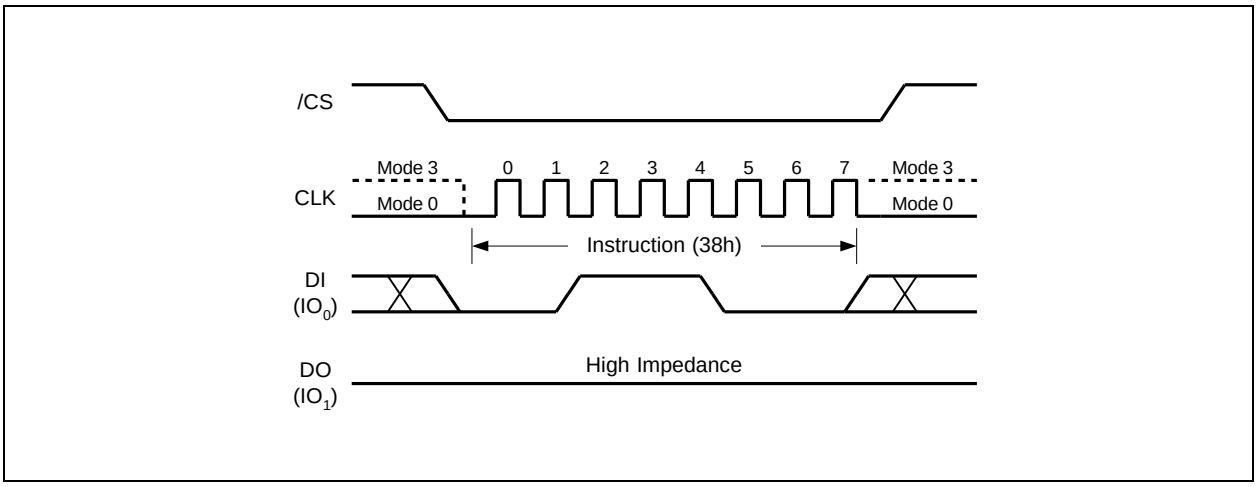



Figure 6.4.53. Enter QPI Instruction (SPI Mode only)



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### 6.4.54 Exit QPI Mode (FFh)

In order to exit the QPI mode and return to the Standard/Dual/Quad SPI mode, an “Exit QPI (FFh)” instruction must be issued.

When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

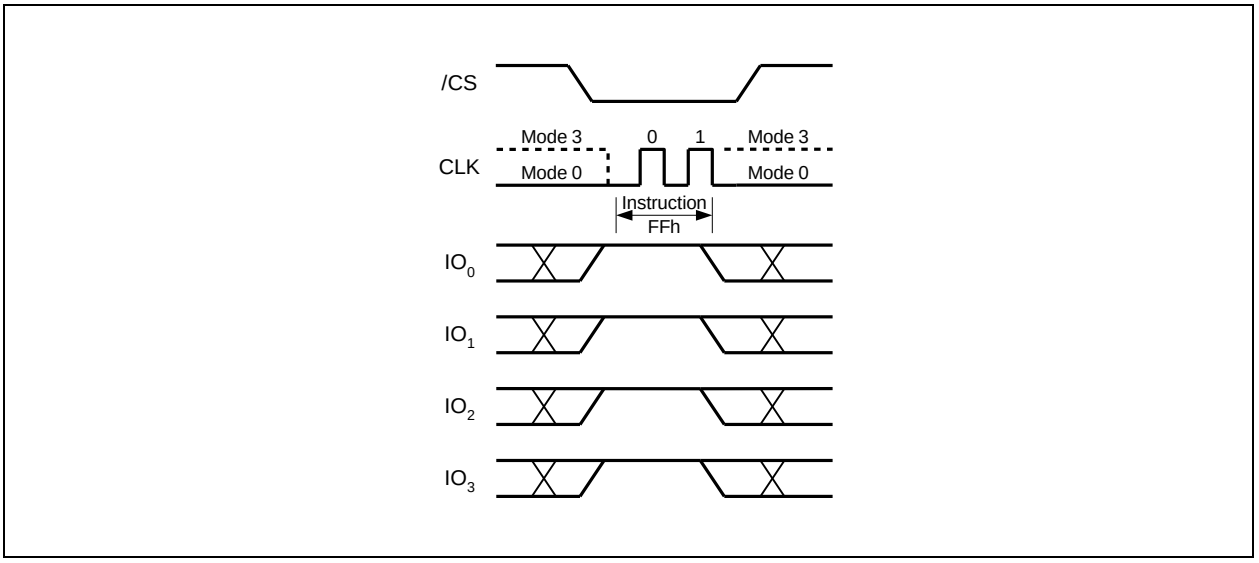



Figure 6.4.54. Exit QPI Instruction (QPI Mode only)



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### 6.4.55 Flex Block/Sector Lock (36h)

The Flex Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. The Flex Block/Sector Lock bits are volatile bits.

To lock a specific block or sector as illustrated in Figure 6.2.55a, a Flex Block/Sector Lock command must be issued by driving /CS low, shifting the instruction code “36h” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24/32-bit address and then driving /CS high. A Write Enable instruction must be executed before the device will accept the Flex Block/Sector Lock Instruction (Status Register bit WEL= 1).

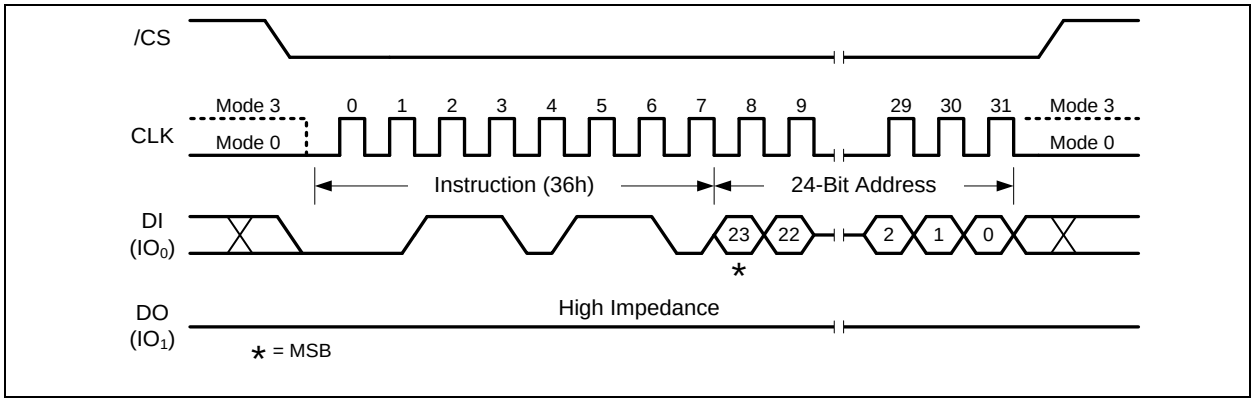



Figure 6.4.55a. Flex Block/Sector Lock Instruction (SPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*

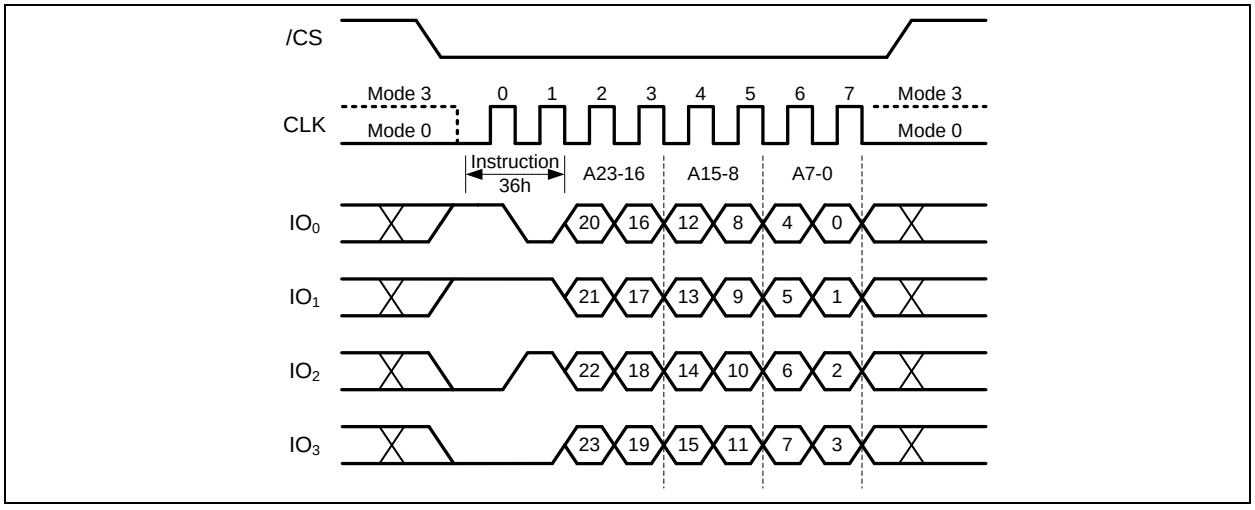



Figure 6.4.55b. Flex Block/Sector Lock Instruction (QPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.56 Flex Block/Sector Unlock (39h)

The Flex Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program operations. The Flex Block/Sector Lock bits are volatile bits.

To unlock a specific block or sector as illustrated in Figure 6.4.56, a Flex Block/Sector Unlock command must be issued by driving /CS low, shifting the instruction code “39h” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24/32-bit address and then driving /CS high. A Write Enable instruction must be executed before the device will accept the Flex Block/Sector Lock Instruction (Status Register bit WEL= 1).

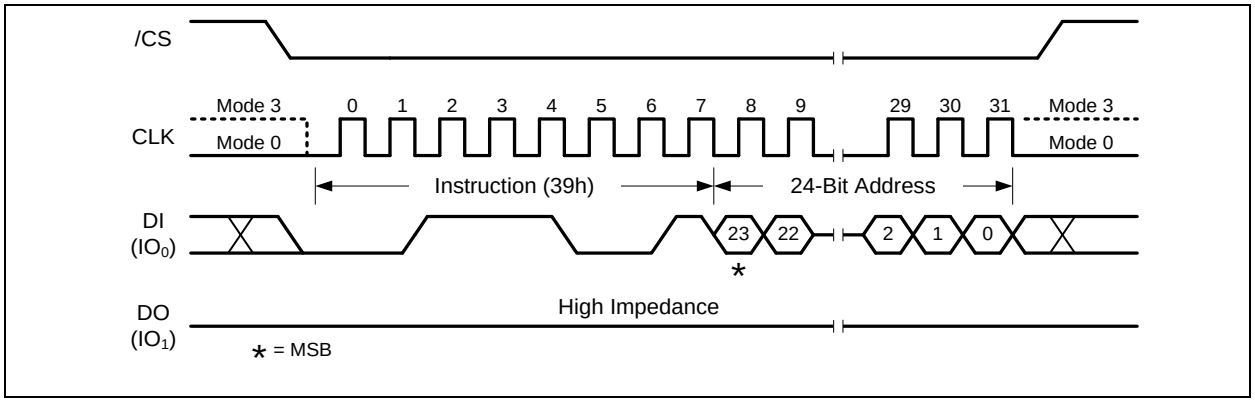



Figure 6.4.56a. Block/Sector Unlock Instruction (SPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*

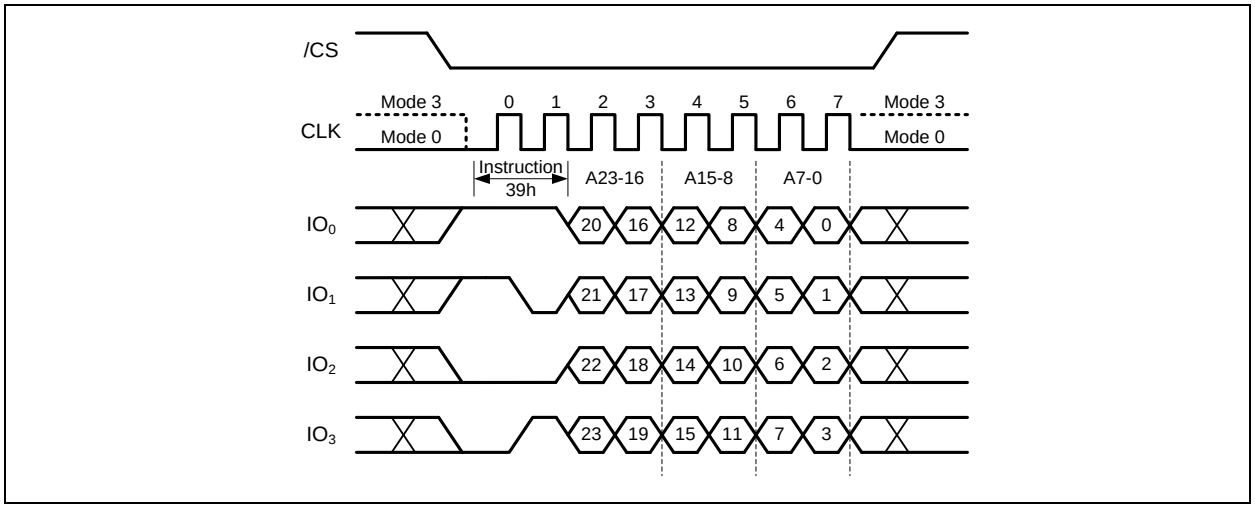



Figure 6.4.56b. Block/Sector Unlock Instruction (QPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.57 Read Flex Block/Sector Lock Bit (3Dh)

The Read Flex Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program operations. The Flex Block/Sector Lock bits are volatile bits.

To read out the lock bit value of a specific block or sector as illustrated in Figure 6.2.57, a Read Block/Sector Lock Bit command must be issued by driving /CS low, shifting the instruction code “3Dh” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24/32-bit address. The Block/Sector Lock bit value will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 6.2.57. If the least significant bit (LSB) is 1, the corresponding block/sector is locked; if LSB=0, the corresponding block/sector is unlocked, and an Erase/Program operation can be performed.

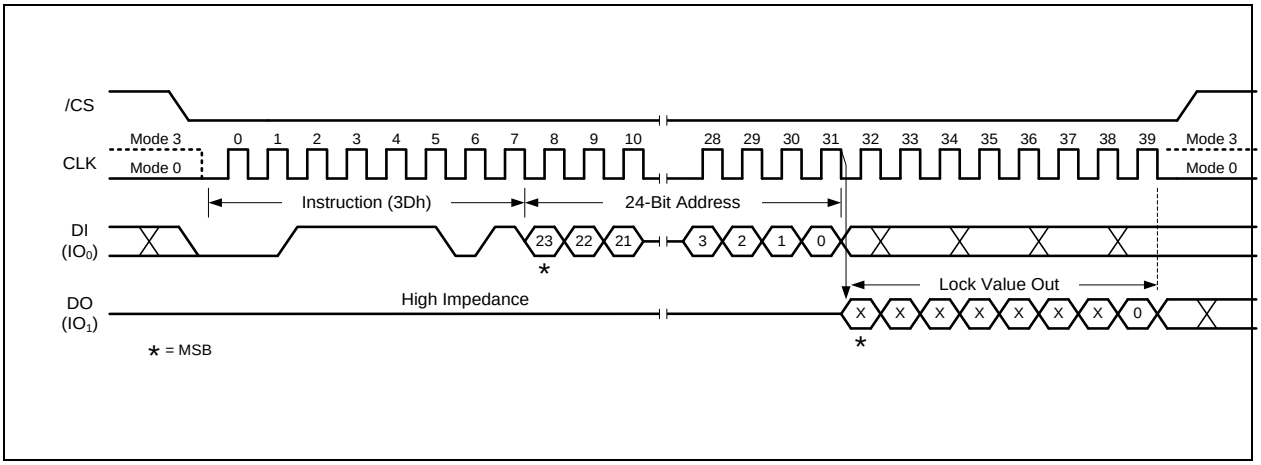



Figure 6.4.57a. Read Block Lock Instruction (SPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*

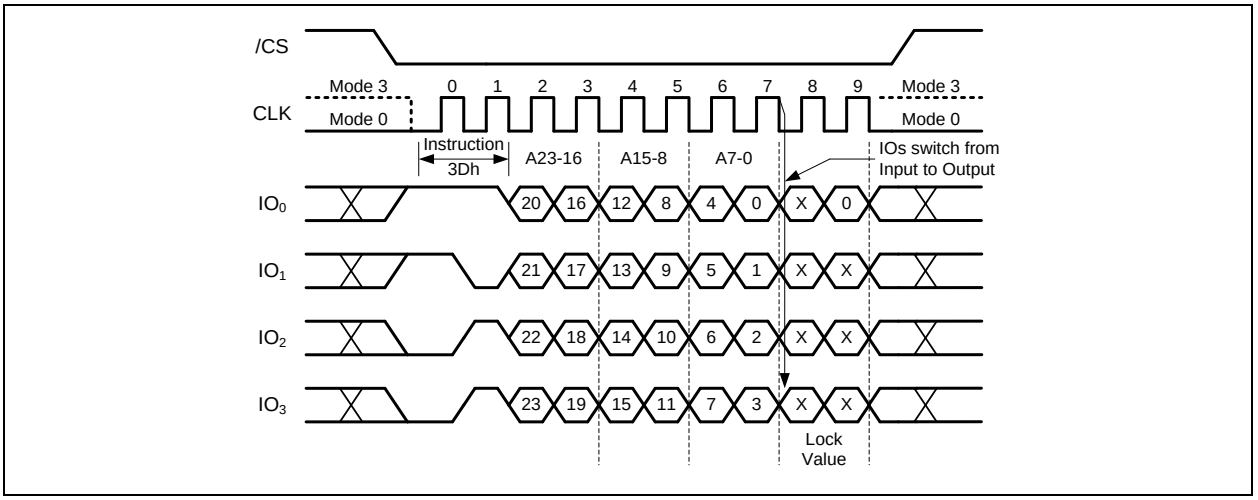



Figure 6.4.57b. Read Block Lock Instruction (QPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.58 Global Flex Block/Sector Lock (7Eh)

All Flex Block/Sector Lock bits can be set to 1 by the Global Flex Block/Sector Lock instruction. The command must be issued by driving /CS low, shifting the instruction code “7Eh” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high. A Write Enable instruction must be executed before the device will accept the Flex Block/Sector Lock Instruction (Status Register bit WEL= 1).

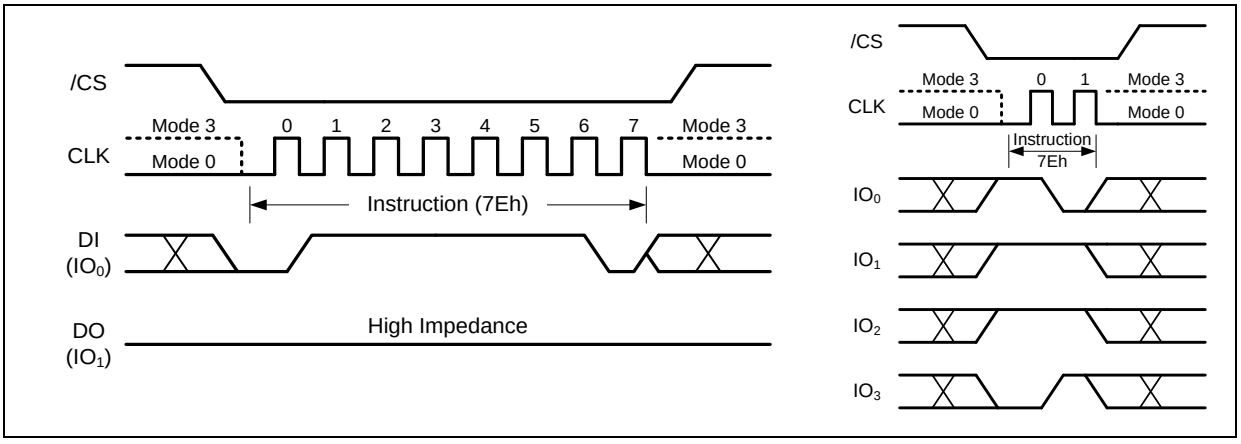



Figure 6.4.58. Global Flex Block/Sector Lock Instruction for SPI Mode (left) or QPI Mode (right)

### 6.4.59 Global Flex Block/Sector Unlock (98h)

All Flex Block/Sector Lock bits can be set to 0 by the Global Flex Block/Sector Unlock instruction. The command must be issued by driving /CS low, shifting the instruction code “98h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high. A Write Enable instruction must be executed before the device will accept the Flex Block/Sector Lock Instruction (Status Register bit WEL= 1).

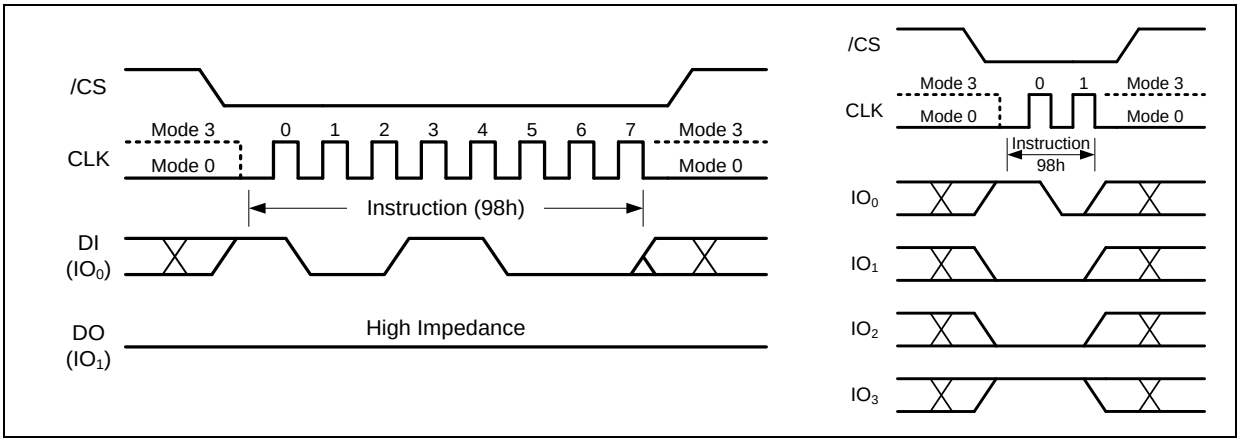



Figure 6.4.59. Global Flex Block/Sector Unlock Instruction for SPI Mode (left) or QPI Mode (right)



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### 6.4.60 Enable Reset (66h) and Reset Device (99h)

Because of the small package and the limitation on the number of pins, the W25QxxRV provides a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated, and the device will return to its default power-on state and lose all the current volatile settings, such as Write Enable Latch (WEL) status, Program/Erase Suspend status, Read parameter setting (P7-P0), setting (M7-M0) and Wrap Bit setting (W6-W4).

"Enable Reset (66h)" and "Reset (99h)" instructions can be issued in either SPI mode or QPI mode. To avoid accidental reset, both instructions must be issued in sequence. Any other commands other than "Reset (99h)" after the "Enable Reset (66h)" command will disable the "Reset Enable" state. A new sequence of "Enable Reset (66h)" and "Reset (99h)" is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately tRST=30us to reset. During this period, no command will be accepted.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when the Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

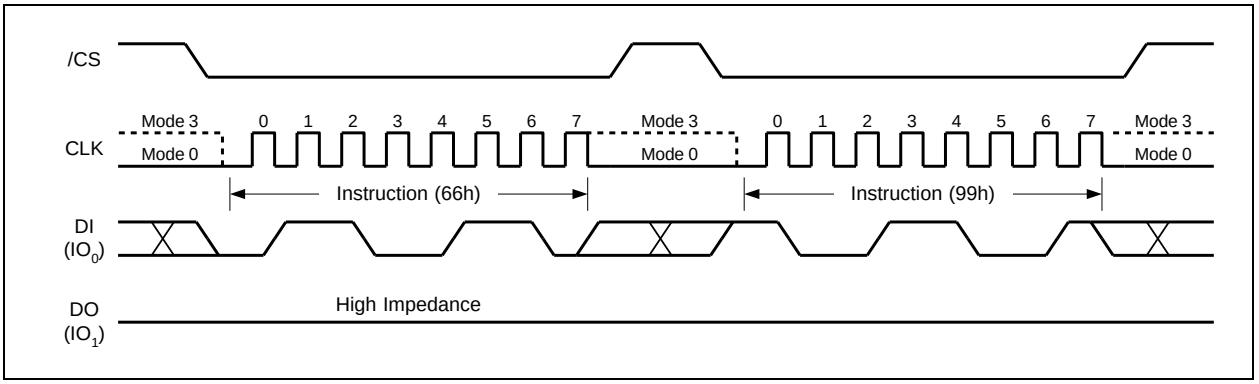



Figure 6.4.60a. Enable Reset and Reset Instruction Sequence (SPI Mode)

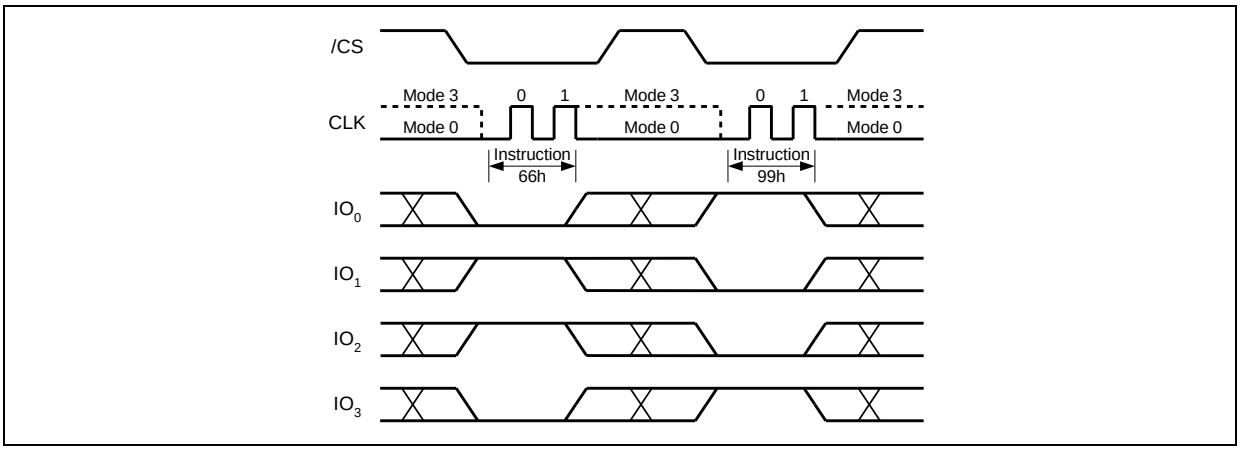



Figure 6.4.60b. Enable Reset and Reset Instruction Sequence (QPI Mode)



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### 6.4.61 Clear Buffer(81h)

The Clear Buffer command allows all data in the buffer to be written as "1". A Write Enable instruction is not required and the instruction is initiated by driving the /CS pin low and then shifting the instruction code "81h" and a 32/24-bit address (BA31-BA24/BA23-A0) to the DI pin. The /CS pin must be held low while instruction and address are transferred to the device. Then by driving /CS pin high, clearing the buffer with all "1". The Clear Buffer instruction sequence is shown in Figure 6.2.61.

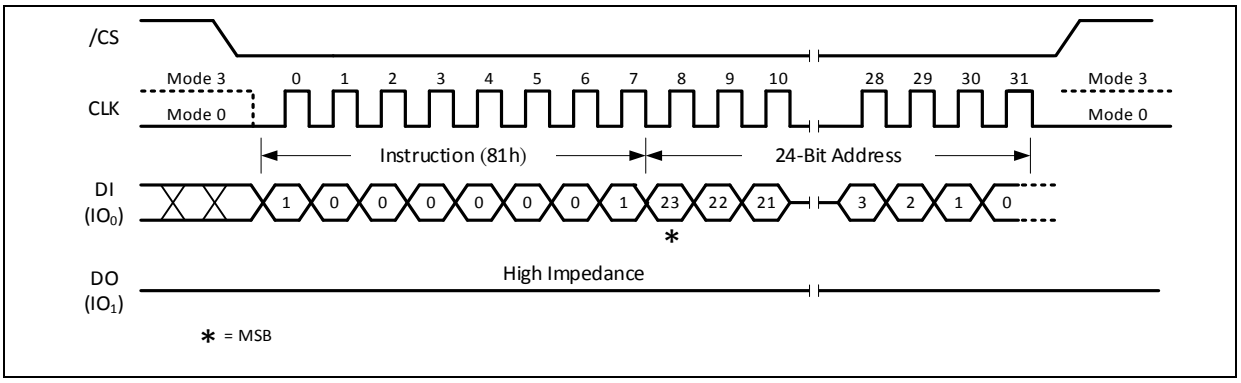



Figure 6.4.61. Clear Buffer (SPI Mode)
32-Bit Buffer Address is required when the device is operating in 4-Byte Address Mode
The Address field in the Clear Buffer (81h) command is Don't care.


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### 6.4.62 Write Buffer(82h)

The Write Buffer instruction allows to write from 1 byte to 256 bytes of data to the buffer. A Write Enable instruction is not required, and the instruction is initiated by driving the /CS pin low and then shifting the instruction code "82h" followed by a 32/24-bit address (BA31-BA24/BA23-A0) and at least one data byte to the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being transferred to the device. The Write Buffer instruction sequence is shown in Figure 6.4.62.

To write the entire 256-byte buffer, the last address byte (the 8 least significant address bits) must be set to 0. The first 16 most significant address bits can be any address. If the last address byte is not zero, and the number of clocks exceeds the remaining buffer length, the addressing is wrapped to the beginning of the buffer. In some cases, less than 256 bytes (partial buffer) can be written without affecting other bytes within the buffer. One condition for performing a partial-buffer write is that the number of clocks cannot exceed the remaining buffer length. If more than 256 bytes are sent to the device, the addressing is wrapped to the beginning of the buffer, overwriting previously sent data.

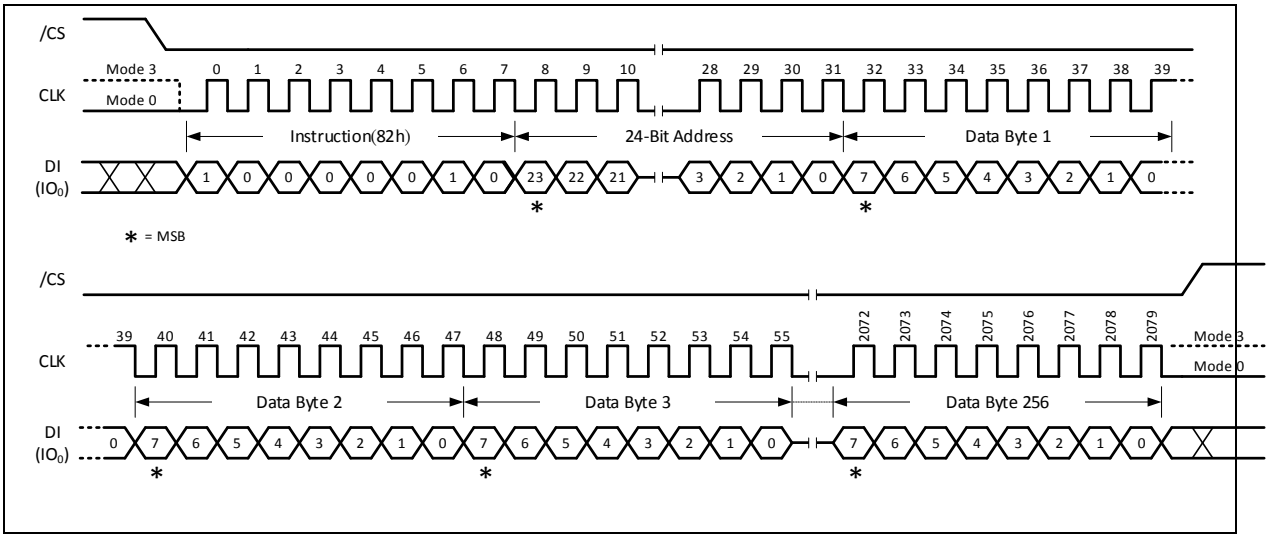



Figure 6.4.62. Write Buffer (SPI Mode)
32-Bit Buffer Address is required when the device is operating in 4-Byte Address Mode


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### 6.4.63 Read Buffer(83h)

The Read Buffer instruction allows one or more data bytes to be sequentially read from the buffer. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “83h” followed by a 32/24-bit address (BA31-BA24/BA23-A0) and an 8-bit dummy into the DI pin. The code and address bits are latched on the rising edge of CLK. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with the most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire buffer can be accessed with a single instruction as long as clock continues. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in Figure 6.4.63. If a Read Buffer instruction is issued while an Erase, Program or Write cycle is in progress (BUSY=1), the instruction is ignored and will not have any effects on the current cycle. The Read Buffer instruction allows clock rates from D.C. to a maximum of fR (see AC Electrical Characteristics).

The Read Buffer (83h) instruction is only supported in Standard SPI mode.

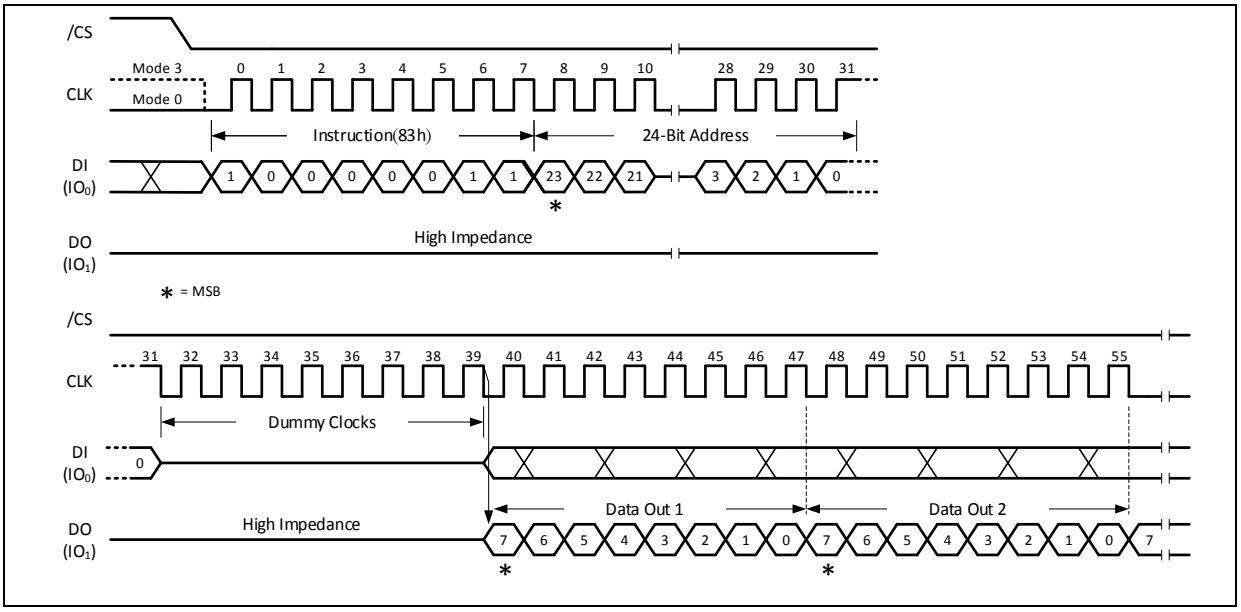



Figure 6.4.63. Read Buffer (SPI Mode)

*32-Bit Buffer Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.64 Program Buffer(8Ah)

The program buffer instruction will program the buffer content into the physical memory page that is specified in the instruction. A Write Enable instruction must be executed before the device will accept the Program Buffer instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “8Ah” followed by a 32/24-bit address (A31-A24/A23-A0) into the DI pin as shown in Figure 6.4.64.

After /CS is driven high to complete the instruction cycle, the self-timed Program Buffer instruction will commence for a time duration of tPP (See AC Characteristics). While the Program Buffer cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit.

The BUSY bit is a 1 during the Program Buffer cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Program Buffer cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Program Execute instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP2, BP1, and BP0) bits.

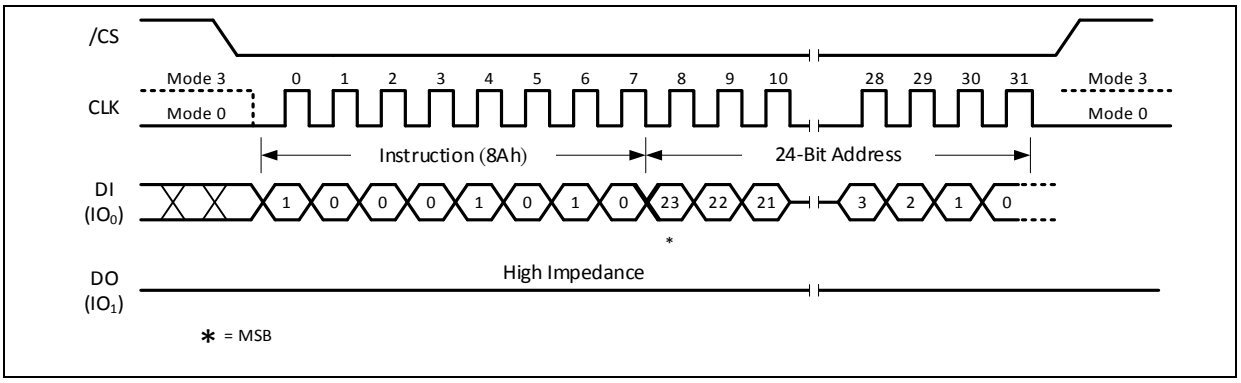



Figure 6.4.64. Program Buffer (SPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.65 Load Buffer(8Bh)

The Load Buffer instruction will write the contents of the physical memory page specified in the instruction to the buffer. A Write Enable instruction is not required, and the instruction is initiated by driving the /CS pin low then shifting the instruction code "8Bh" followed by a32/24-bit address (A31-A24/A23-A0), and then driving /CS high as shown in Figure 6.4.65.

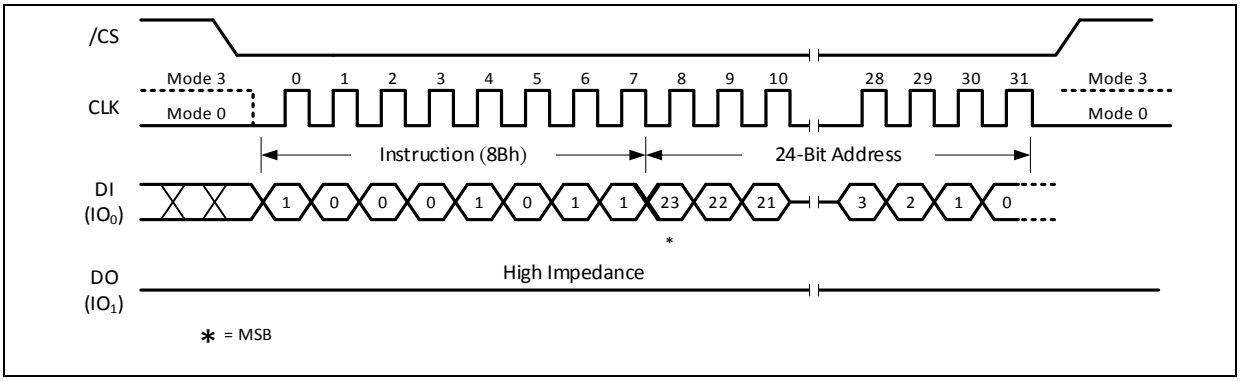



Figure 6.4.65. Load Buffer (SPI Mode)

*32-Bit Address is required when the device is operating in 4-Byte Address Mode*



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### 6.4.66 Calculate Checksum(9Dh)

The Calculate Checksum instruction is used to compute the checksum for a specified range within the flash memory. This is accomplished by providing the starting address (SA) and ending address (EA) in a 24/32-bit format. The instruction is initiated by driving the /CS pin low and shifting the instruction code "9Dh" followed by the starting address and ending address. The checksum is then calculated and can be read out by driving the /CS pin high. After the Calculate Checksum cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

1. Code “9Dh” followed by the 24/32-bit starting address (SA23-SA0/SA31-24) and ending address (EA31-A0)
2. Erase/Program Suspend (75h) is not accepted during Calculate Checksum.
3. The 32-bit BYTESUM register is reset by Power-On Reset (POR), Hardware/Software Reset (HW/SW RESET), or the FFh instruction.

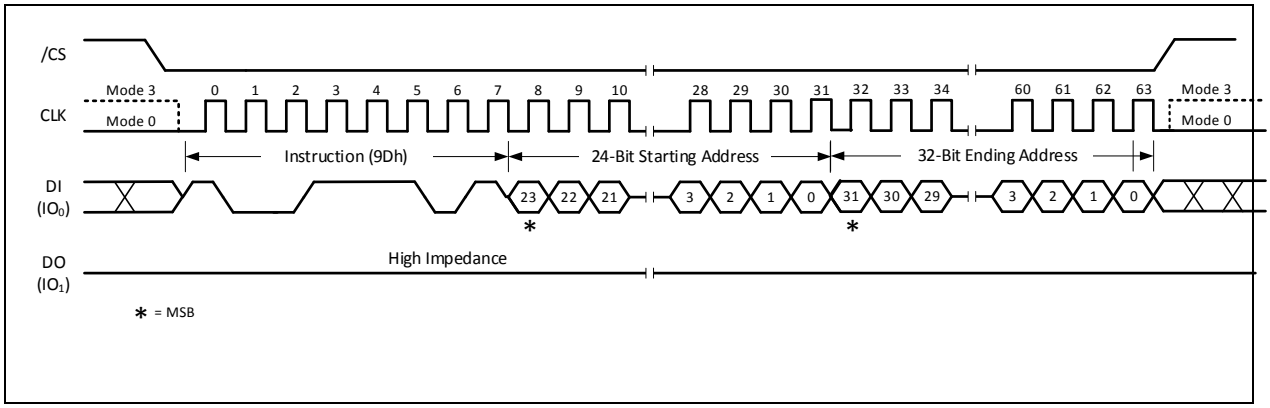



Figure 6.4.66a. Calculate Checksum (SPI Mode)
*32-Bit* Starting *Address is required when the device is operating in 4-Byte Address Mode*

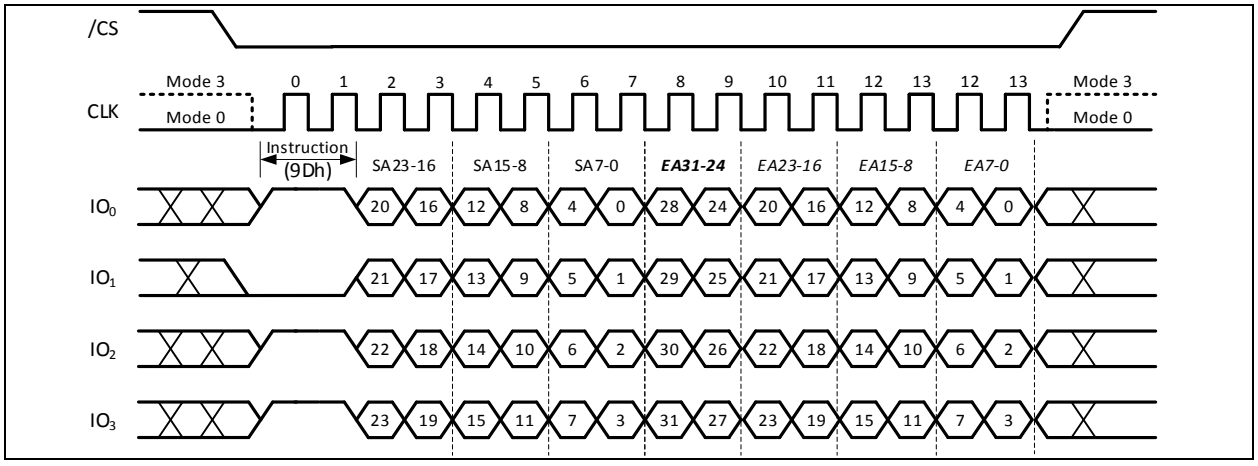



Figure 6.4.66b. Calculate Checksum (QPI Mode)
*32-Bit* Starting *Address is required when the device is operating in 4-Byte Address Mode*


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### 6.4.67 Read Checksum (9Ch)

The Read Checksum instruction is similar to the Fast Read instruction(0Bh) except that it retrieves the checksum data for a specified range. This is accomplished by adding eight “dummy” clocks after the 24/32-bit address as shown in Figure 6.4.67. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. During the dummy clocks, the data value on the DO pin is a “don’t care”.

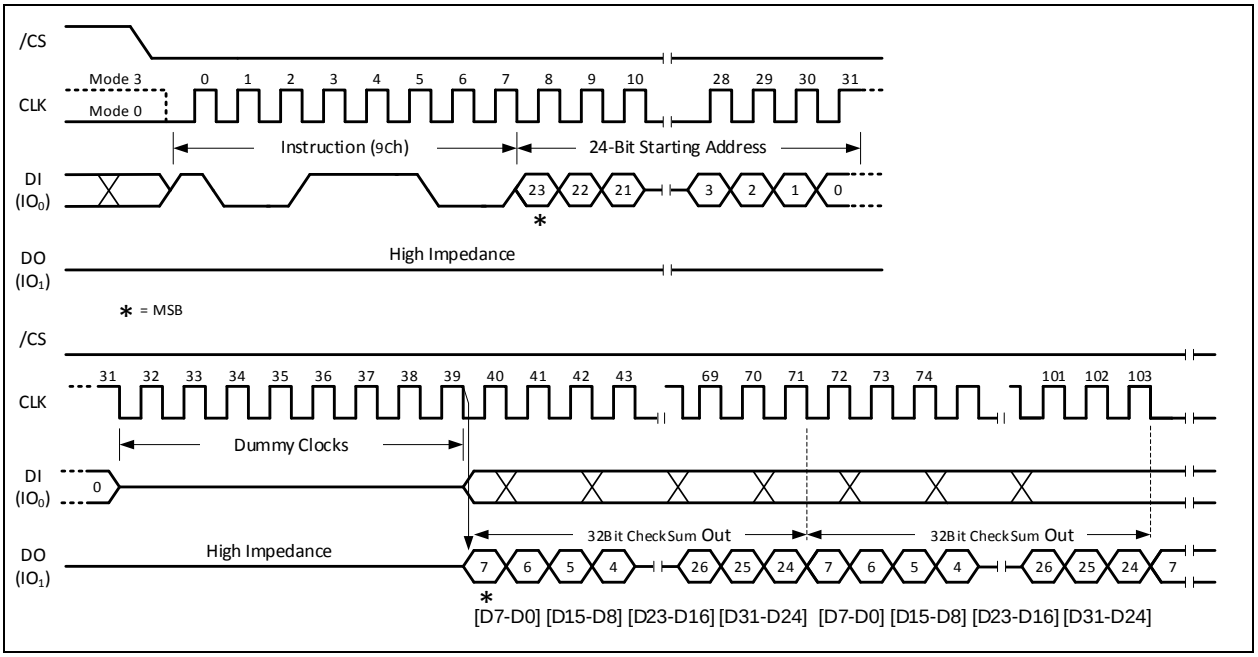



Figure 6.4.67a. Read Checksum (SPI Mode)
32-Bit Starting Address is required when the device is operating in 4-Byte Address Mode

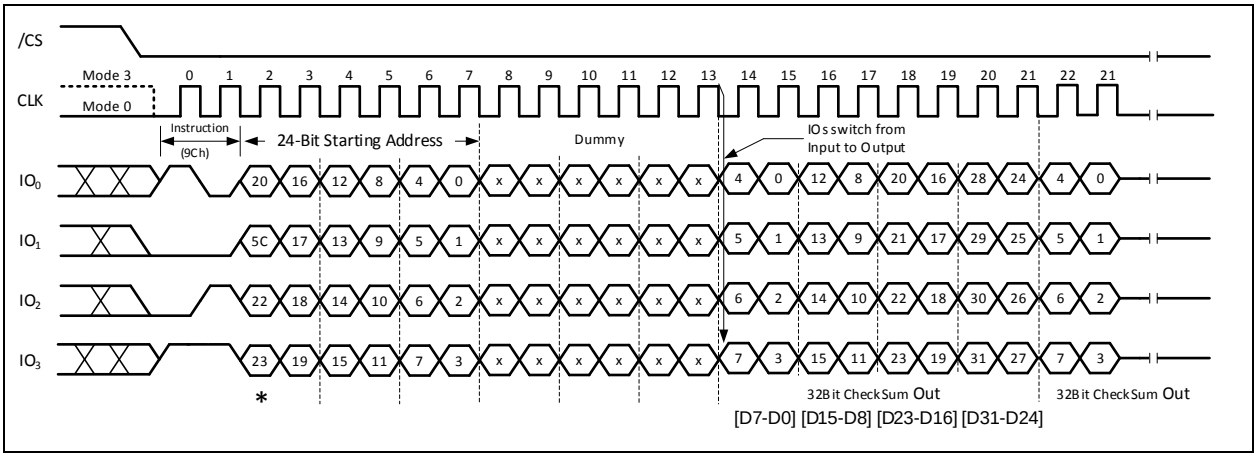



Figure 6.4.67b. Read Checksum (QPI Mode)
32-Bit Starting Address is required when the device is operating in 4-Byte Address Mode
* "Set Read Parameters" instruction (C0h) can set the number of dummy clocks



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### 6.4.68 Recovery for Erase (A8h)

The Recovery for Erase instruction identifies whether a power drop has occurred before completing the erase operation. Upon detecting an incomplete erase due to a power drop, the device performs an internal recovery process to prevent system data influence in non-erase areas.

A Write Enable instruction must be executed prior to accepting the Recovery for Erase instruction (Status Register bit WEL must equal 1). The instruction begins by driving the /CS pin low and shifting the instruction code “A8h”. The sequence for the Recovery for Erase instruction is illustrated in the Figure 6.4.68.

Once /CS is driven high, the self-timed Recovery for Erase instruction initiates for a duration of tRCV (See AC Characteristics). During the Recovery for Erase cycle, the Read Status Register instruction can still be accessed to check the BUSY bit status. The BUSY bit remains at 1 during the Block Erase cycle and switches to 0 once the cycle completes, indicating the device is ready for other instructions. After the Recovery for Erase cycle concludes, the Write Enable Latch (WEL) bit in the Status Register is reset to 0.

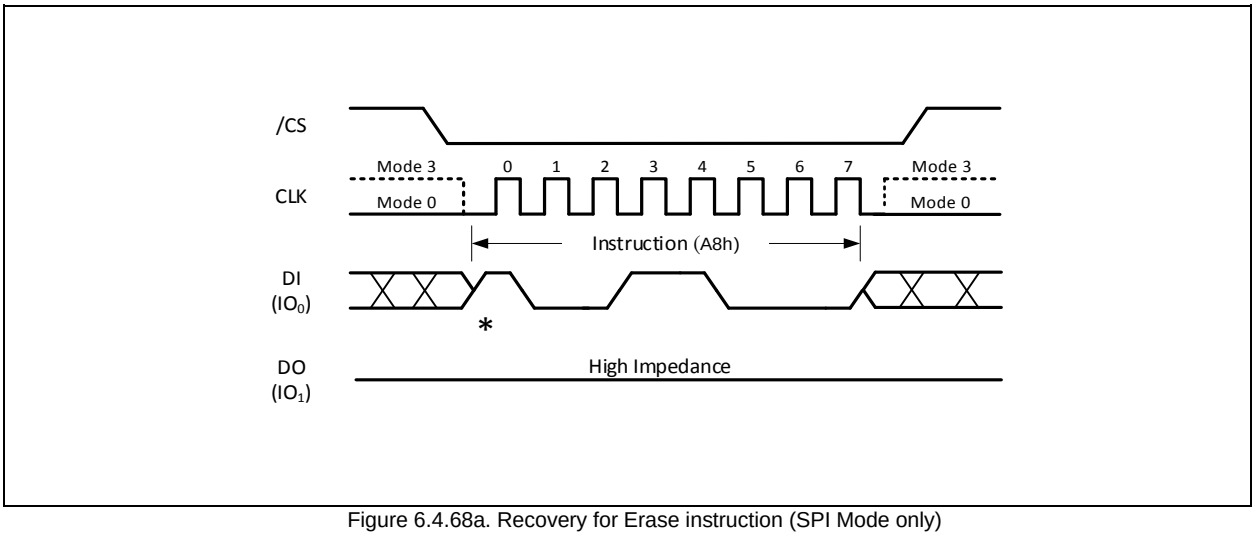



Figure 6.4.68a. Recovery for Erase instruction (SPI Mode only)

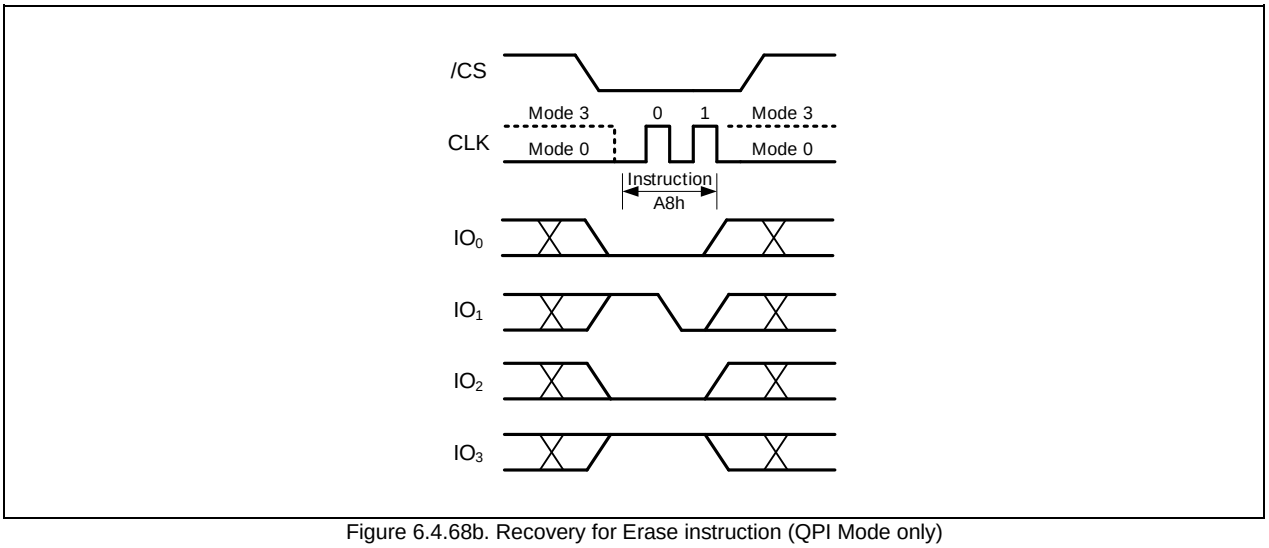



Figure 6.4.68b. Recovery for Erase instruction (QPI Mode only)



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### 6.4.69 Enter Factory Mode (51h-A5h-41h)

Winbond provides a method to speedy-up the erase time, which supports maximum of 50 program-erase cycles.

Upon power-up, the default state of the device upon is Standard SPI mode. This provides full backward compatibility with earlier generations of Winbond serial flash memories. See Instruction Set Table 1-4 & 7-8 for all supported Factory Mode instruction. In order to switch the device to Factory Mode, “Enter Factor Mode (51h-A5h-41h) instruction must be issued.

A hardware reset, a software reset (66h/99h), or upon power up can the device switch from Factory Mode to SPI Standby Mode. During suspend mode, entering factory mode is not allowed. Similarly, during factory mode, issuing a suspend command is not allowed.

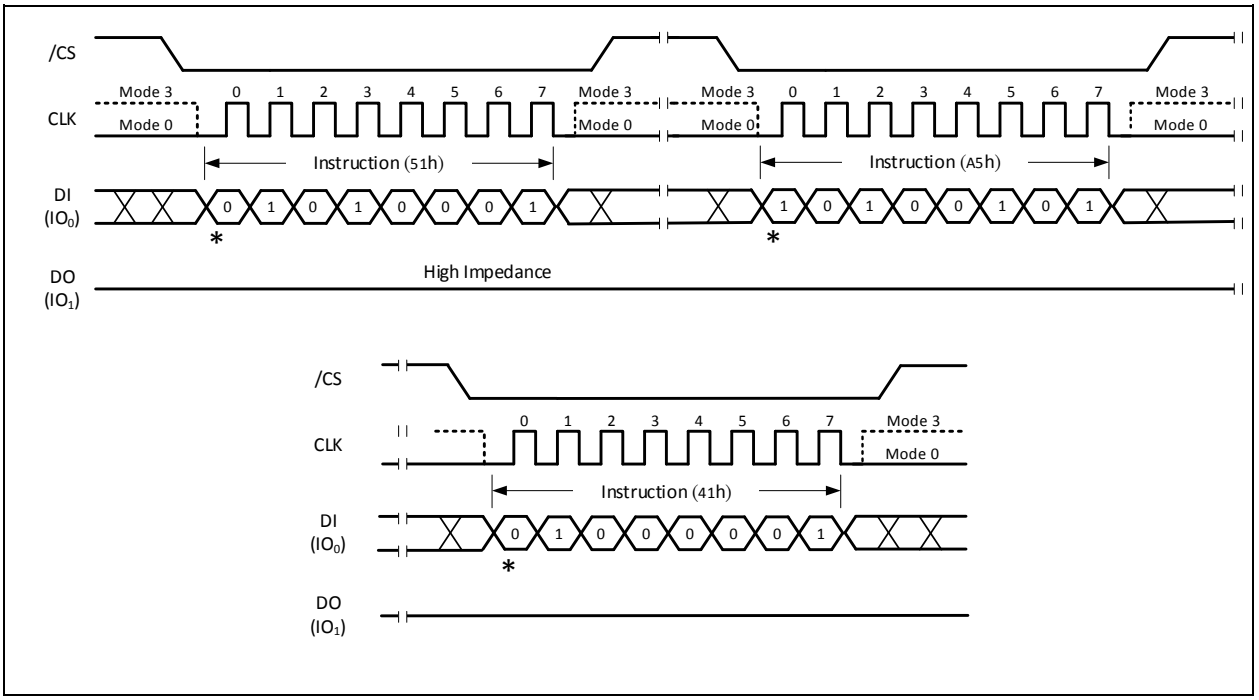



Figure 6.4.69a. Entry Factory Mode Instruction Sequence (SPI Mode)

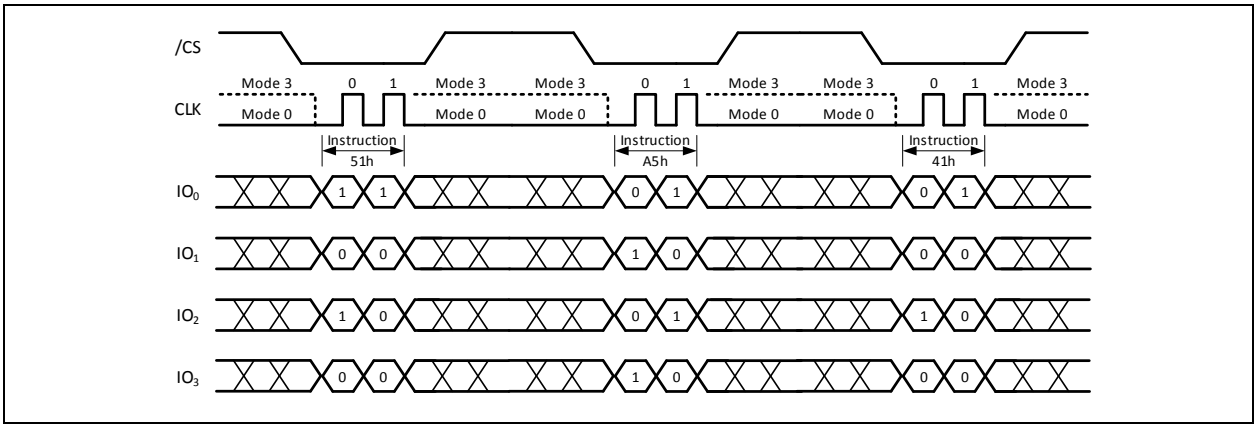



Figure 6.4.69b. Entry Factory Mode Instruction Sequence (QPI Mode)



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# 7 ELECTRICAL CHARACTERISTICS

## 7.1 Absolute Maximum Ratings (1)

| PARAMETERS | SYMBOL | CONDITIONS | RANGE | UNIT |
|---|---|---|---|---|
| Supply Voltage | VCC | | –0.6 to +4.6V | V |
| Voltage Applied to Any Pin | VIO | Relative to Ground | –0.6 to VCC+0.4 | V |
| Transient Voltage on any Pin | VIOT | <20nS Transient Relative to Ground | –2.0 to VCC+2.0 | V |
| Storage Temperature | TSTG | | –65 to +150 | °C |
| Lead Temperature | TLEAD | | See Note (2) | °C |
| Electrostatic Discharge Voltage | VESD | Human Body Model(3) | –2000 to +2000 | V |

**Notes:**

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

## 7.2 Operating Ranges

| PARAMETER | SYMBOL | CONDITIONS | SPEC | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| Supply Voltage(1) | VCC | $F_R$ = 133MHz<br>fR = 104MHz | 2.7 | 3.6 | V |
| Ambient Temperature, Operating | TA | Industrial plus | –40 | +105 | °C |

**Note:**

1. VCC voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage.



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## 7.3 Power-Up Power-Down Timing and Requirements

| PARAMETER | | SYMBOL | SPEC | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| VCC (min) to /CS Low | | $t_{VSL}$(1) | 20 | | µs |
| Time Delay Before Write Instruction | | $t_{PUW}$(1) | 5 | | ms |
| Write Inhibit Threshold Voltage | | $V_{WI}$(1) | 1.0 | 2.0 | V |
| The minimum duration for ensuring initialization will occur | | $t_{PWD}$(1) | 100 | | µs |
| VCC voltage needed to below $V_{PWD}$ for ensuring initialization will occur | W25Q33RV-12RV | $V_{PWD}$(1) | | 0.8 | V |
| | W25Q25RV-02RV | | | 0.9 | V |

**Note:**

1. These parameters are characterized only.

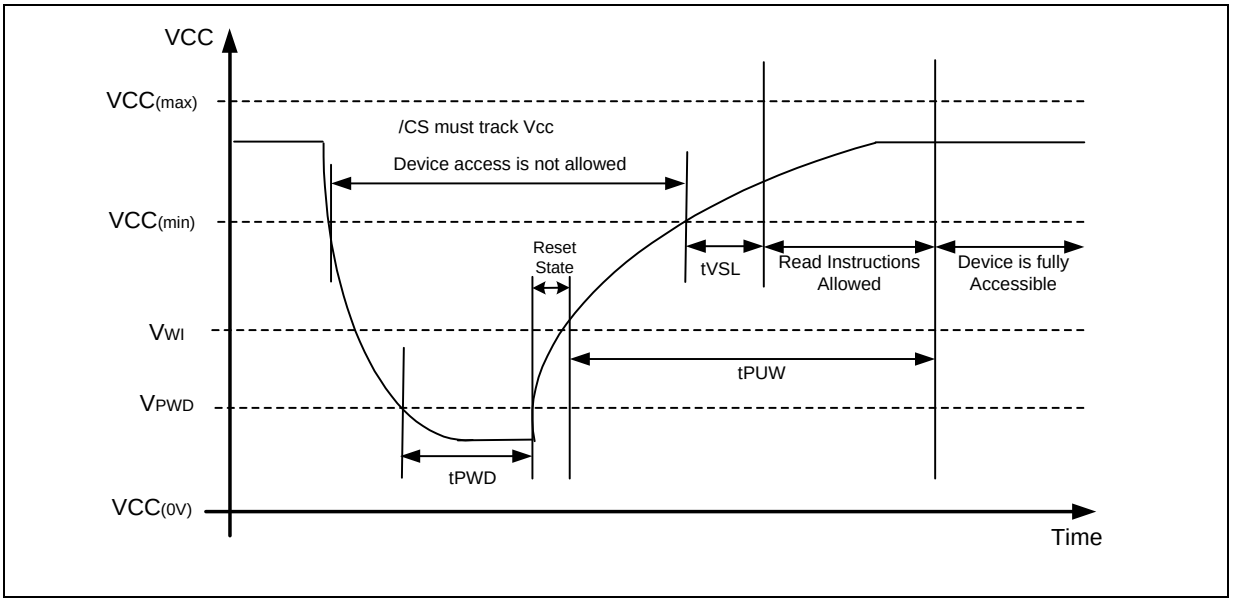



Figure 7.3a. Power-up, Power cycle Timing and Voltage Levels

**Note:**

1. For power cycle, the system must not initial the power-up sequence until Vcc drops down to VPWD and keeps tPWD for device to initialize correctly.



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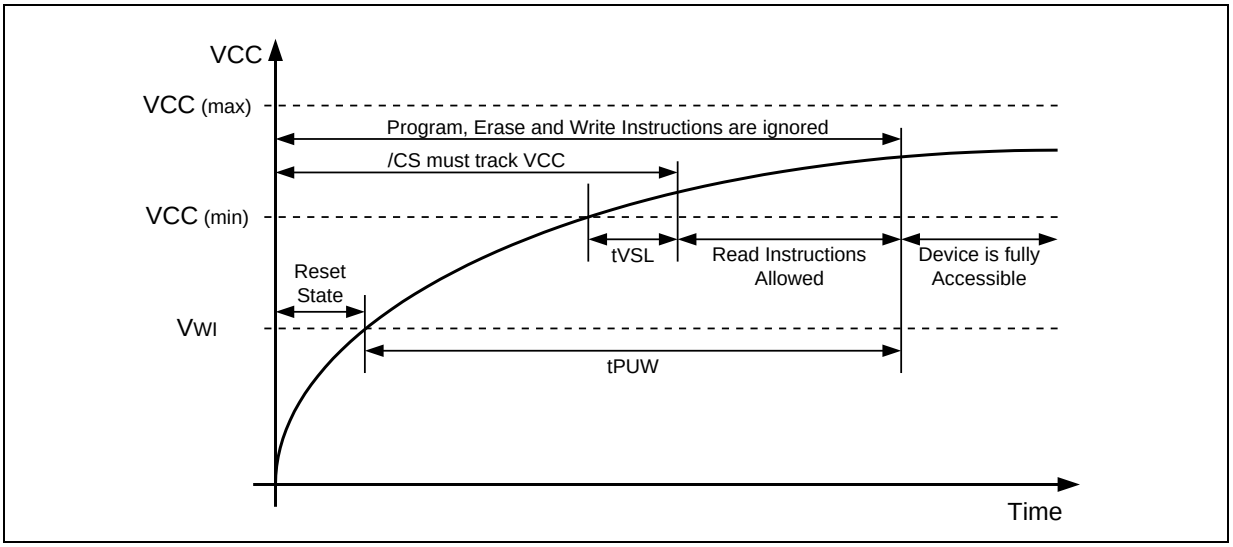



Figure 7.3b. Power-up Timing and Voltage Levels

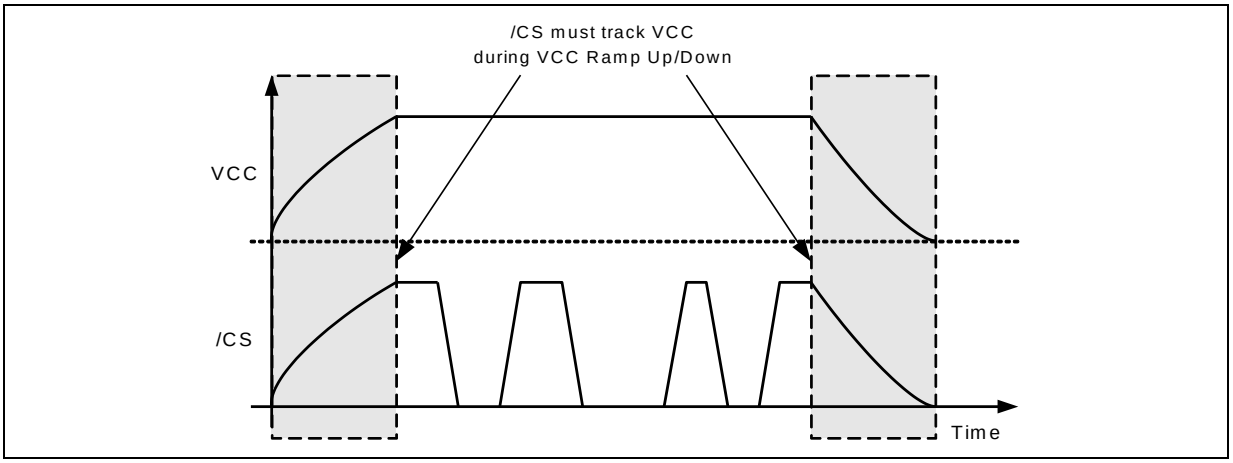



Figure 7.3c. Power-up, Power-Down Requirement



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## 7.4 DC Electrical Characteristics[1]

| PARAMETER | SYMBOL | CONDITIONS | | SPEC | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| Input Capacitance | $C_{IN}$[1] | $V_{IN}$ = 0V | W25Q33RV<br>W25Q64RV<br>W25Q12RV<br>W25Q25RV<br>W25Q51RV | | | 6 | pF |
| | | | W25Q01RV | | | 12 | |
| | | | W25Q02RV | | | 24 | |
| Output Capacitance | Cout[1] | Vout = 0V | W25Q33RV<br>W25Q64RV<br>W25Q12RV<br>W25Q25RV<br>W25Q51RV | | | 8 | pF |
| | | | W25Q01RV | | | 16 | |
| | | | W25Q02RV | | | 32 | |
| Standby Current | ICC1 | /CS = VCC, VIN = GND or VCC | W25Q33RV<br>W25Q64RV<br>W25Q12RV<br>W25Q25RV<br>W25Q51RV | | 15 | 50 | µA |
| | | | | | 15 | 50 | |
| | | | | | 15 | 50 | |
| | | | | | 15 | 170 | |
| | | | | | 15 | 185 | |
| | | | W25Q01RV | | 60 | 400 | |
| | | | W25Q02RV | | 120 | 800 | |
| Power-down Current | $I_{CC2}$ | /CS = VCC, VIN = GND or VCC | W25Q33RV<br>W25Q64RV<br>W25Q12RV<br>W25Q25RV<br>W25Q51RV | | 0.1 | 20 | µA |
| | | | W25Q01RV | | 0.2 | 25 | |
| | | | W25Q02RV | | 0.4 | 30 | |



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| Parameter | Symbol | Conditions | | SPEC | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| Read Data / Dual /Quad Current | Icc3 | C = 0.1VCC / 0.9 VCC DO = Open | W25Q33RV, W25Q64RV, W25Q12RV | | | | |
| | | | FR = 50MHz | | 10 | 15 | mA |
| | | | FR =84MHz | | 12 | 18 | mA |
| | | | FR =104MHz | | 14 | 20 | mA |
| | | | FR =133MHz | | 16 | 25 | mA |
| | | | DTR=104MHz | | 10/12/15 | 17/19/23 | mA |
| | | | W25Q25RV, W25Q51RV | | | | |
| | | | FR = 50MHz | | 10 | 15 | mA |
| | | | FR =84MHz | | 12 | 18 | mA |
| | | | FR =104MHz | | 14 | 22 | mA |
| | | | FR =133MHz | | 16 | 25 | mA |
| | | | DTR=104MHz | | 10/12/15 | 17/19/23 | mA |
| | | | W25Q01RV | | | | |
| | | | FR = 50MHz | | 20 | 30 | mA |
| | | | FR =84MHz | | 24 | 36 | mA |
| | | | FR =104MHz | | 28 | 44 | mA |
| | | | FR =133MHz | | 32 | 50 | mA |
| | | | DTR=104MHz | | 20/24/30 | 34/38/46 | mA |
| | | | W25Q02RV | | | | |
| | | | FR = 50MHz | | 40 | 60 | mA |
| | | | FR =84MHz | | 48 | 72 | mA |
| | | | FR =104MHz | | 52 | 88 | mA |
| | | | FR =133MHz | | 64 | 100 | mA |
| | | | DTR=104MHz | | 40/48/60 | 68/76/92 | mA |


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| PARAMETER | SYMBOL | CONDITIONS | | SPEC | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| Write Status Register Current | $I_{CC4}$ | /CS = VCC | W25Q33RV<br>W25Q64RV<br>W25Q12RV<br>W25Q25RV<br>W25Q51RV | | 20 | 25 | mA |
| | | | W25Q01RV | | 20 | 30 | |
| | | | W25Q02RV | | 20 | 60 | |
| Page Program Current | $I_{CC5}$ (2) | /CS = VCC | | | 20 | 25 | mA |
| Sector/Block Erase Current | $I_{CC6}$ | /CS = VCC | | | 20 | 25 | mA |
| Chip Erase Current | $I_{CC7}$ | /CS = VCC | W25Q33RV<br>W25Q64RV<br>W25Q12RV<br>W25Q25RV<br>W25Q51RV | | 20 | 25 | mA |
| | | | W25Q01RV | | 20 | 35 | |
| | | | W25Q02RV | | 20 | 50 | |
| Input Leakage | $I_{LI}$ | | | | | ±2 | µA |
| I/O Leakage | $I_{LO}$ | | | | | ±2 | µA |
| Input Low Voltage | $V_{IL}$ | | | –0.5 | | VCC x 0.3 | V |
| Input High Voltage | $V_{IH}$ | | | VCC x 0.7 | | VCC + 0.4 | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 100 µA | | | | 0.2 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = –100 µA | | VCC – 0.2 | | | V |

**Notes:**

1. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.0V.
2. Checkerboard Pattern.
3. TBD stands for To Be Determined.



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## 7.5 AC Measurement Conditions

| PARAMETER | SYMBOL | SPEC | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| Load Capacitance | $C_L$ | | 30 | pF |
| Input Rise and Fall Times | $T_R$, $T_F$ | | 5 | ns |
| Input Pulse Voltages | $V_{IN}$ | 0.1 VCC to 0.9 VCC | | V |
| Input Timing Reference Voltages | IN | 0.3 VCC to 0.7 VCC | | V |
| Output Timing Reference Voltages | OUT | 0.5 VCC to 0.5 VCC | | V |

**Note:**
1. Output Hi-Z is defined as the point where data out is no longer driven.

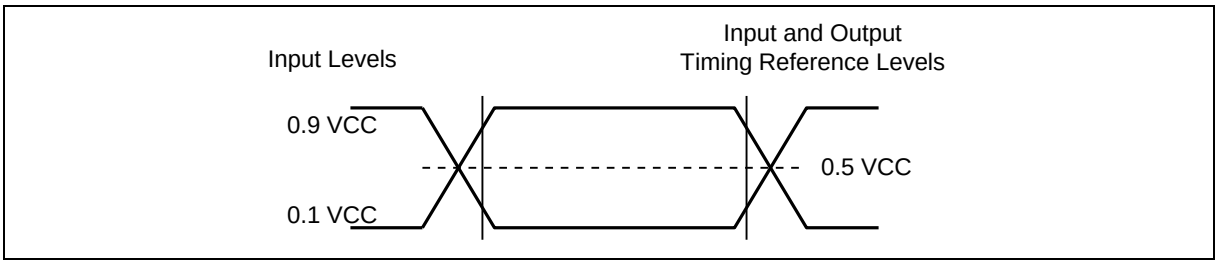



Figure 7.5. AC Measurement I/O Waveform



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## 7.6 AC Electrical Characteristics- Maximum Clock Frequencies (MHz) for Read Data

### SPI Mode Maximum Clock Frequencies (MHz) for Read Data - *W25Q33RV/64RV/12RV*

| Address Mode | | Fast Read/Read Checksum | | Fast Read Dual Output | | Fast Read Dual I/O | | Fast Read Quad Output | | Fast Read Quad I/O | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 3-/4-byte Address | | 0Bh/9Ch | | 3Bh | | BBh | | 6Bh | | EBh | |
| Fixed 4-byte | | 0Ch | | 3Ch | | BCh | | 6Ch | | ECh | |
| Default dummy | | Fixed dummy -8(2) | | Fixed dummy -8(2) | | Fixed dummy -4(2) (3) | | Fixed dummy -8(2) | | Variable dummy Default dummy -6(3) | |
| Starting Address(1) | | Aligned | Any | Aligned | Any | Aligned | Any | Aligned | Any | Aligned | Any |
| Dummy Cycle | 4 | x | x | x | x | 133 | 104 | x | x | x | x |
| | 6 | x | x | x | x | x | x | x | x | 133 | 104 |
| | 8 | 133 | 104 | 133 | 104 | x | x | 133 | 104 | 133 | 104 |
| | 10 | x | x | x | x | x | x | x | x | 133 | 104 |
| | 12–16 | x | x | x | x | x | x | x | x | 166 | 133 |

Notes:

1. Aligned: 4-bytes address alignment for Read, read address start from A1,A0=0,0. Any: no alignment requirements; reads may begin at any address.
2. 0Bh, 3Bh, BBh, 6Bh, 0Ch, 3Ch, BCh, and 6Ch with fixed dummy clock support.
3. BBh, EBh, BCh and ECh support “Read Command Bypass Mode”. When the M7–M0 is set to Fxh, Read Command Bypass Mode is disabled, and M7–M0 is treated as the dummy-cycle field.

### SPI_DTR Mode Maximum Clock Frequencies (MHz) for Read Data - *W25Q33RV/64RV/12RV*

| Address Mode | | Fast Read | | Fast Read Dual I/O | | Fast Read Quad I/O | |
|---|---|---|---|---|---|---|---|
| 3-/4-byte Address | | 0Dh | | BDh | | EDh | |
| Fixed 4-byte | | X | | X | | EEh | |
| Default dummy | | Fixed dummy -6 | | Fixed dummy -6(2) (3) | | Variable dummy Default dummy -8(3) | |
| Starting Address(1) | | Aligned | Any | Aligned | Any | Aligned | Any |
| Dummy Cycle | 6 | 84 | 66 | 84 | 66 | x | x |
| | 8 | x | x | x | x | 84 | 66 |
| | 10 | x | x | x | x | 84 | 66 |
| | 12–16 | x | x | x | x | 104 | 84 |

Notes:

1. Aligned: 4-bytes address alignment for Read, read address start from A1,A0=0,0. Any: no alignment requirements; reads may begin at any address.
2. 0Dh and BDh with fixed dummy clock support.
3. BDh, EDh and EEh support “Read Command Bypass Mode”. When the M7–M0 is set to Fxh, Read Command Bypass Mode is disabled, and M7–M0 is treated as the dummy-cycle field.



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### QPI Mode Maximum Clock Frequencies (MHz) for Read Data - *W25Q33RV/64RV/12RV*

| Address Mode | | Fast Read /Read Checksum | | Burst Read With Wrap | | Fast Read Quad I/O | |
|---|---|---|---|---|---|---|---|
| 3-/4-byte Address | | 0Bh / 9Ch | | x | | EBh(2) | |
| Fixed 4-byte Address | | X | | 0Ch | | ECh (2) | |
| Starting Address(1) | | Aligned | Any | Aligned | Any | Aligned | Any |
| Dummy Cycle | 6 | 133 | 104 | 133 | 104 | 133 | 104 |
| | 8 | 133 | 104 | 133 | 104 | 133 | 104 |
| | 10 | 133 | 104 | 133 | 104 | 133 | 104 |
| | 12–16 | 166 | 133 | 166 | 133 | 166 | 133 |

Notes:

1. Aligned: 4-bytes address alignment for Read, read address start from A1,A0=0,0. Any: no alignment requirements; reads may begin at any address.
2. EBh and ECh support “Read Command Bypass Mode”. When the M7–M0 is set to Fxh, Read Command Bypass Mode is disabled, and M7–M0 is treated as the dummy-cycle field

### QPI_DTR Mode Maximum Clock Frequencies (MHz) for Read Data - *W25Q33RV/64RV/12RV*

| Address Mode | | Fast Read | | Burst Read With Wrap | | Fast Read Quad I/O | |
|---|---|---|---|---|---|---|---|
| 3-/4-byte Address Mode | | 0Dh | | 0Eh | | EDh(2) | |
| Fixed 4-byte Address | | X | | X | | EEh(2) | |
| Starting Address(1) | | Aligned | Any | Aligned | Any | Aligned | Any |
| Dummy Cycle | 8 | 84 | 66 | 84 | 66 | 84 | 66 |
| | 10 | 84 | 66 | 84 | 66 | 84 | 66 |
| | 12–16 | 104 | 84 | 104 | 84 | 104 | 84 |

Notes:

1. Aligned: 4-bytes address alignment for Read, read address start from A1,A0=0,0. Any: no alignment requirements; reads may begin at any address..
2. EDh and EEh support “Read Command Bypass Mode”. When the M7–M0 is set to Fxh, Read Command Bypass Mode is disabled, and M7–M0 is treated as the dummy-cycle field



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## SPI Mode Maximum Clock Frequencies (MHz) for Read Data - *W25Q25RV/51RV/01RV/02RV*

| Address Mode | | Fast Read/Read Checksum | | Fast Read Dual Output | | Fast Read Dual I/O | | Fast Read Quad Output | | Fast Read Quad I/O | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 3-/4-byte Address | | 0Bh/9Ch | | 3Bh | | BBh | | 6Bh | | EBh | |
| Fixed 4-byte | | 0Ch | | 3Ch | | BCh | | 6Ch | | ECh | |
| Default dummy | | Fixed dummy -8(2) | | Fixed dummy -8(2) | | Fixed dummy -4(2) (3) | | Fixed dummy -8(2) | | Variable dummy Default dummy -6(3) | |
| Starting Address(1) | | Aligned | Any | Aligned | Any | Aligned | Any | Aligned | Any | Aligned | Any |
| Dummy Cycle | 4 | x | x | x | x | 104 | 66 | x | x | x | x |
| | 6 | x | x | x | x | x | x | x | x | 104 | 66 |
| | 8 | 104 | 66 | 104 | 66 | x | x | 104 | 66 | 133 | 66 |
| | 10 | x | x | x | x | x | x | x | x | 133 | 66 |
| | 12–16 | x | x | x | x | x | x | x | x | 133 | 84 |

Notes:

1. Aligned: 4-bytes address alignment for Read, read address start from A1,A0=0,0. Any: no alignment requirements; reads may begin at any address..
2. 0Bh, 3Bh, BBh, 6Bh, 0Ch, 3Ch, BCh, and 6Ch with fixed dummy clock support.
3. BBh, EBh, BCh and ECh support “Read Command Bypass Mode”. When the M7–M0 is set to Fxh, Read Command Bypass Mode is disabled, and M7–M0 is treated as the dummy-cycle field.

## SPI_DTR Mode Maximum Clock Frequencies (MHz) for Read Data- *W25Q25RV/51RV/01RV/02RV*

| Address Mode | | Fast Read | | Fast Read Dual I/O | | Fast Read Quad I/O | |
|---|---|---|---|---|---|---|---|
| 3-/4-byte Address | | 0Dh | | BDh | | EDh | |
| Fixed 4-byte | | X | | X | | EEh | |
| Default dummy | | Fixed dummy -6 | | Fixed dummy -6(2) (3) | | Variable dummy Default dummy -8(3) | |
| Starting Address(1) | | Aligned | Any | Aligned | Any | Aligned | Any |
| Dummy Cycle | 6 | 84 | 50 | 84 | 50 | x | x |
| | 8 | x | x | x | x | 84 | 50 |
| | 10 | x | x | x | x | 84 | 50 |
| | 12–16 | x | x | x | x | 104 | 66 |

Notes:

1. Aligned: 4-bytes address alignment for Read, read address start from A1,A0=0,0. Any: no alignment requirements; reads may begin at any address..
2. 0Dh and BDh with fixed dummy clock support.
3. BDh, EDh and EEh support “Read Command Bypass Mode”. When the M7–M0 is set to Fxh, Read Command Bypass Mode is disabled, and M7–M0 is treated as the dummy-cycle field.



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### QPI Mode Maximum Clock Frequencies (MHz) for Read Data- *W25Q25RV/51RV/01RV/02RV*

| Address Mode | | Fast Read /Read Checksum | | Burst Read With Wrap | | Fast Read Quad I/O | |
|---|---|---|---|---|---|---|---|
| 3-/4-byte Address | | 0Bh / 9Ch | | x | | EBh(2) | |
| Fixed 4-byte Address | | X | | 0Ch | | ECh (2) | |
| Starting Address(1) | | Aligned | Any | Aligned | Any | Aligned | Any |
| Dummy Cycle | 6 | 104 | 66 | 104 | 66 | 104 | 66 |
| | 8 | 133 | 66 | 133 | 66 | 133 | 66 |
| | 10 | 133 | 66 | 133 | 66 | 133 | 66 |
| | 12–16 | 133 | 84 | 133 | 84 | 133 | 84 |

Notes:

1. Aligned: 4-bytes address alignment for Read, read address start from A1,A0=0,0. Any: no alignment requirements; reads may begin at any address.
2. EBh and ECh support “Read Command Bypass Mode”. When the M7–M0 is set to Fxh, Read Command Bypass Mode is disabled, and M7–M0 is treated as the dummy-cycle field

### QPI_DTR Mode Maximum Clock Frequencies (MHz) for Read Data- *W25Q25RV/51RV/01RV/02RV*

| Address Mode | | Fast Read | | Burst Read With Wrap | | Fast Read Quad I/O | |
|---|---|---|---|---|---|---|---|
| 3-/4-byte Address Mode | | 0Dh | | 0Eh | | EDh(2) | |
| Fixed 4-byte Address | | X | | X | | EEh(2) | |
| Starting Address(1) | | Aligned | Any | Aligned | Any | Aligned | Any |
| Dummy Cycle | 8 | 84 | 50 | 84 | 50 | 84 | 50 |
| | 10 | 104 | 50 | 104 | 50 | 84 | 50 |
| | 12–16 | 104 | 66 | 104 | 66 | 104 | 66 |

Notes:

1. Aligned: 4-bytes address alignment for Read, read address start from A1,A0=0,0. Any: no alignment requirements; reads may begin at any address.
2. EDh and EEh support “Read Command Bypass Mode”. When the M7–M0 is set to Fxh, Read Command Bypass Mode is disabled, and M7–M0 is treated as the dummy-cycle field



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## 7.7 AC Electrical Characteristics

| Description | Symbol | Condition | Spec | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Min | Min | |
| Clock High, Low Time for all Instructions except for Read Data (03h) | $t_{CLH}$, $t_{CLL}$ (1) | | 45%PC | | | ns |
| Clock High, Low Time for Read Data (03h) Instruction | $t_{CRLH}$, $t_{CRLL}$ (1) | | 45%PC | | | ns |
| Clock Rise Time peak to peak | $t_{CLCH}$ (2) | | 0.1 | | | V/ns |
| Clock Fall Time peak to peak | $t_{CHCL}$ (2) | | 0.1 | | | V/ns |
| /CS Active Setup Time relative to CLK | $t_{SLCH}$ | | 3 | | | ns |
| /CS Active Setup Time relative to CLK (DTR only) | $t_{SLCH1}$ | | 4 | | | ns |
| /CS Not Active Hold Time relative to CLK | $t_{CHSL}$ | | 3.5 | | | ns |
| Data In Setup Time | $t_{DVCH}$ | | 2 | | | ns |
| Data In Hold Time | $t_{DCHX}$ | | 2 | | | ns |
| /CS Active Hold Time relative to CLK | $t_{CHSH}$ | | 3 | | | ns |
| /CS Not Active Setup Time relative to CLK | $t_{SHCH}$ | | 3 | | | ns |
| /CS Active Hold Time relative to CLK （DTR only） | $t_{SHCH}$ | | 3 | | | ns |
| /CS Deselect Time (for Read) | $t_{SHSL1}$ | | 10 | | | ns |
| /CS Deselect Time (for Erase or Program or Write) | $t_{SHSL2}$ | | 50 | | | ns |
| Output Disable Time | $t_{SHQZ}$ (2) | | | | 7 | ns |



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| DESCRIPTION | SYMBOL | CONDITION | SPEC | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Clock Low to Output Valid<br>VCC=2.7~3.0V / VCC=3.0~3.6V | $t_{CLQV}$ | W25Q33RV<br>W25Q64RV<br>W25Q12RV | | | 5 / 4.5 | ns |
| | | W25Q25RV<br>W25Q51RV | | | 6 / 5 | |
| | | W25Q01RV | | | 7.5 / 5 | ns |
| | | W25Q02RV | | | 7.5 / 6 | ns |
| Output Hold Time | $t_{CLQX}$ | | 1.5 | | | ns |
| /HOLD Active Setup Time relative to CLK | $t_{HLCH}$ | | 5 | | | ns |
| /HOLD Active Hold Time relative to CLK | $t_{CHHH}$ | | 5 | | | ns |
| /HOLD Not Active Setup Time relative to CLK | $t_{HHCH}$ | | 5 | | | ns |
| /HOLD Not Active Hold Time relative to CLK | $t_{CHHL}$ | | 5 | | | ns |
| /HOLD to Output Low-Z | $t_{HHQX}$[2] | | | | 7 | ns |
| /HOLD to Output High-Z | $t_{HLQZ}$[2] | | | | 12 | ns |
| Write Protect Setup Time Before /CS Low | $t_{WHSL}$[3] | | 20 | | | ns |
| Write Protect Hold Time After /CS High | $t_{SHWL}$[3] | | 100 | | | ns |
| /CS High to Power-down Mode | $t_{DP}$[2] | | | | 3 | µs |
| /CS High to Standby Mode without ID Read | $t_{RES1}$[2] | | | | 5 | µs |
| /CS High to Standby Mode with ID Read | $t_{RES2}$[2] | | | | 1.8 | µs |
| /CS High to next Instruction after Suspend | $t_{SUS}$[2] | | | | 20 | µs |
| /CS High to next Instruction after Reset | $t_{RST}$[2] | | | | 30 | µs |
| /RESET pin Low period to reset the device | $t_{RESET}$[2] | | 1[5] | | | µs |



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**Program and Erase Time**

| DESCRIPTION | SYMBOL | CONDITION | SPEC | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Write Status Register Time | $t_W$ | | | 1 | 15 | ms |
| Page Program Time | $t_{PP}$ | | | 0.18 | 0.6 | ms |
| Sector Erase Time (4KB) | $t_{SE}$ | W25Q33RV<br>W25Q64RV<br>W25Q12RV | | 30 | 250 | ms |
| | | W25Q25RV<br>W25Q51RV<br>W25Q01RV<br>W25Q02RV | | 30 | 150 | ms |
| Block Erase Time (32KB) | $t_{BE_1}$ | | | 120 | 1,600 | ms |
| Block Erase Time (64KB) | $t_{BE_2}$ | | | 150 | 2,000 | ms |
| Chip Erase Time | $t_{CE}$ | W25Q33RV | | 8 | 40 | s |
| | | W25Q64RV | | 15 | 80 | |
| | | W25Q12RV | | 30 | 160 | |
| | | W25Q25RV | | 60 | 320 | |
| | | W25Q51RV | | 120 | 640 | |
| | | W25Q01RV | | 120 | 640 | |
| | | W25Q02RV | | 120 | 640 | |



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**DS SPEC:**

| DESCRIPTION | SYMBOL | CONDITION | SPEC | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| DS Low after First CLK | $t_{DS}$ | | | | 10 | ns |
| DS to Output Data Valid | $t_{DSSQ}$ | | | | 0.4 | ns |
| Data Valid Window | $t_{DVW}$ | | 1.6 | | | ns |

**/BUSY SPEC:**

| DESCRIPTION | SYMBOL | CONDITION | SPEC | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| /CS Deselect Time (for program/erase) to /BUSY Low | $t_{SHBL}$ | | | | 80 | ns |
| /BUSY High to /CS Active | $t_{BHSL}$ | | | 0 | | ns |



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**Factory mode** (9)

| DESCRIPTION | SYMBOL | CONDITION | SPEC | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| 4KB Sector Erase Time (20h) | $t_{SE}$ | | | 15 | | ms |
| 32KB Block Erase Time (52h) | $t_{BE1}$ | | | 60 | | ms |
| 64KB Block Erase Time (D8h) | $t_{BE2}$ | | | 75 | | ms |
| Chip Erase Time (C7h) | $t_{CE}$ | W25Q51RV<br>W25Q01RV<br>W25Q02RV | | 60 | | s |
| | | W25Q25RV | | 30 | | s |
| | | W25Q12RV | | 15 | | s |
| | | W25Q64RV | | 8 | | s |
| | | W25Q33RV | | 4 | | s |
| Program/Erase Cycling Count | cycling | VCC=3.0V~3.6V | | | 50 | count |



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**Notes:**

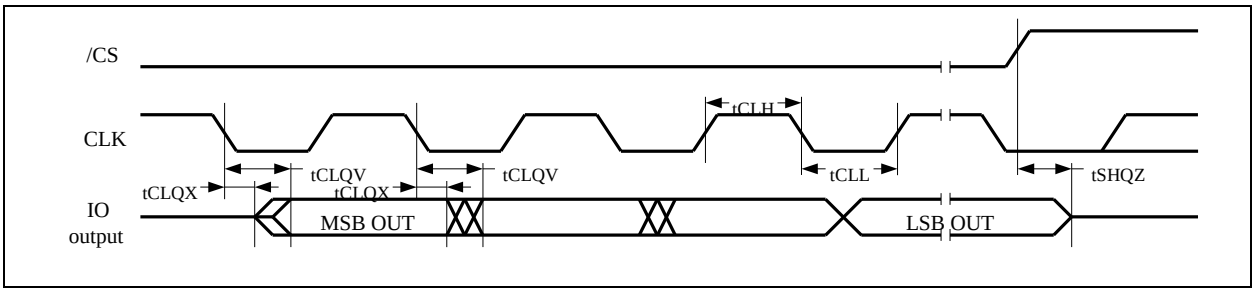
1. Clock high + Clock low must be less than or equal to Pc. Pc = 1/fc(max.)
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write Status Register instruction when SRP=1.
4. It is possible to reset the device with shorter tRESET (as short as a few hundred ns), a 1us minimum is recommended to ensure reliable operation.
5. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.0V
6. 4-bytes address alignment for Read: read address start from A1,A0=0,0.
7. No restrictions on the starting address, such as 4-bytes address alignment for Read.
8. Certain commands support Dummy settings. For detailed information, please refer to the link “6.4.50 Set Read Parameters (C0h)”
9. Factory mode is only supported with the input VCC range from 3.0V to 3.6V.

## 7.8 AC Electrical Characteristics Alternative Symbol table

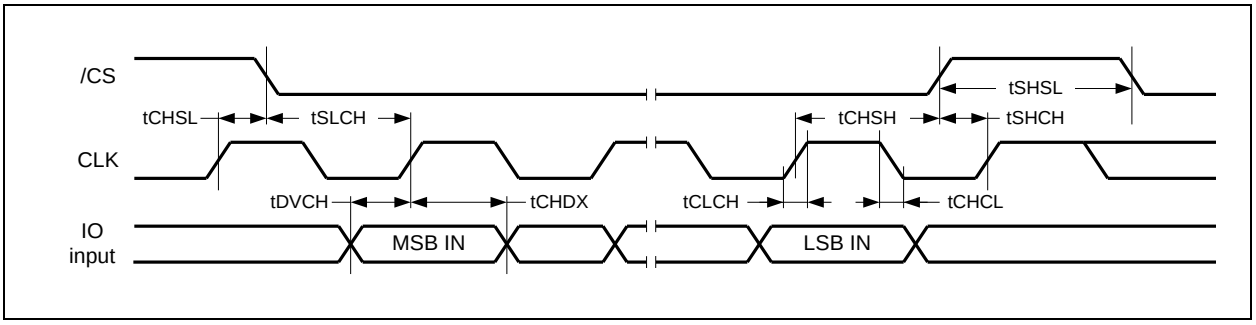
| Description | Symbol | Alt |
|---|---|---|
| Clock frequency for SPI & QPI Instructions | $F_R$ | $f_{C1}$ |
| /CS Active Setup Time relative to CLK | $t_{SLCH}$ | $t_{CSS}$ |
| Data In Setup Time | $t_{DVCH}$ | $t_{DSU}$ |
| Data In Hold Time | $t_{CHDX}$ | $t_{DH}$ |
| /CS Deselect Time (for Read) | $t_{SHSL1}$ | $t_{CSH}$ |
| /CS Deselect Time (for Erase or Program or Write) | $t_{SHSL2}$ | $t_{CSH}$ |
| Output Disable Time | $t_{SHQZ}$(2) | $t_{DIS}$ |
| Clock Low to Output Valid | $t_{CLQV}$ | $t_V$ |
| Output Hold Time | $t_{CLQX}$ | $t_{HO}$ |


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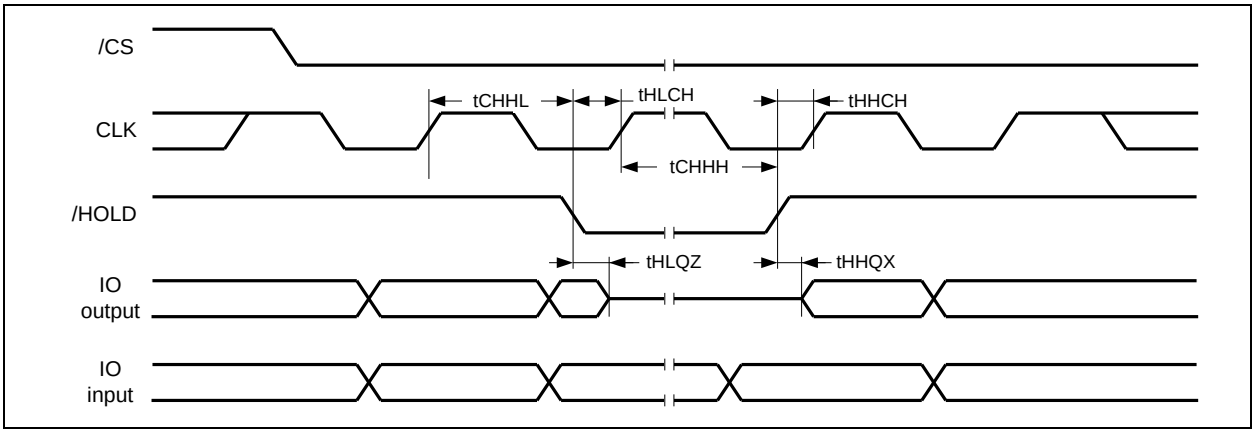
## 7.9 Serial Output Timing



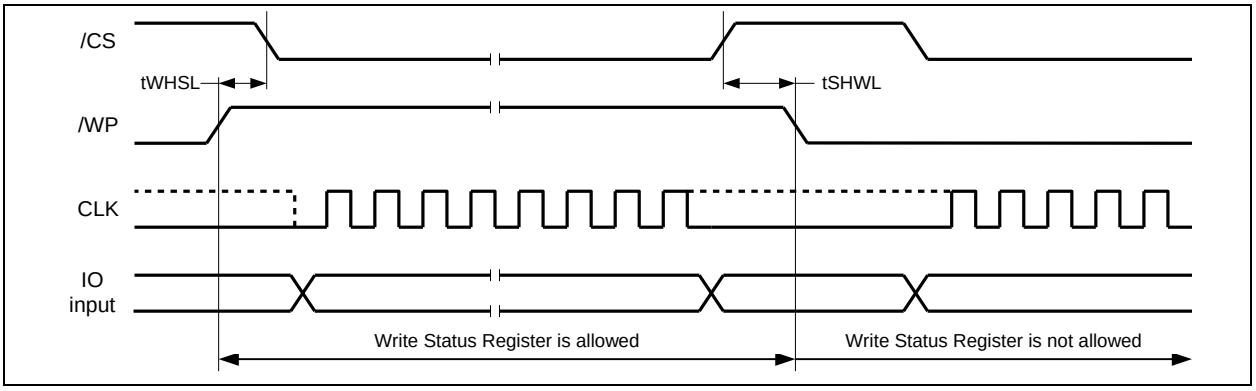

## 7.10 Serial Input Timing




## 7.11 /HOLD Timing



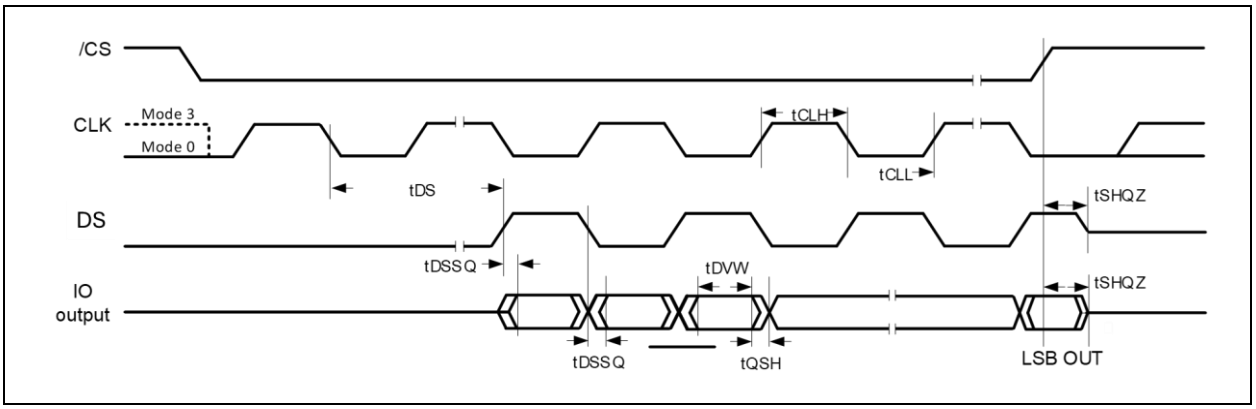

## 7.12 /WP Timing



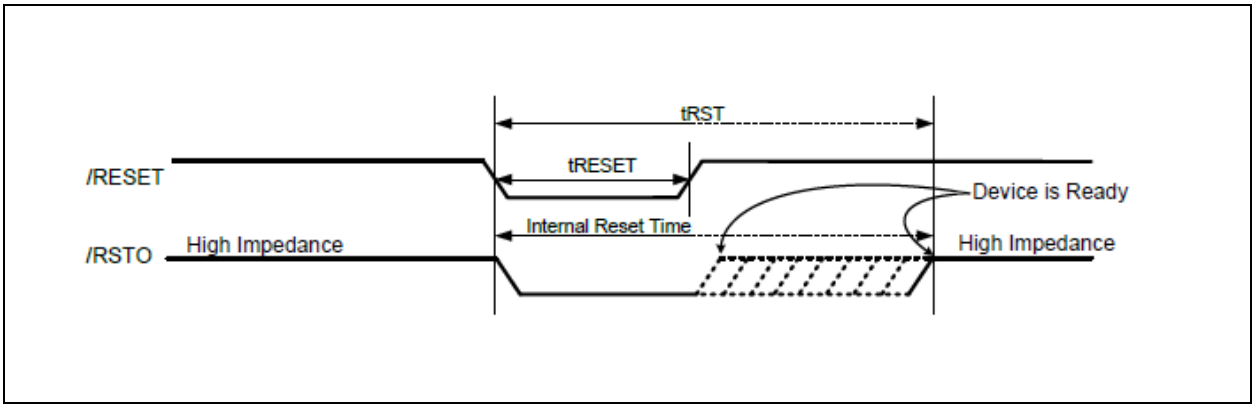



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## 7.13 DS Timing




## 7.14 Hardware /RESET Timing

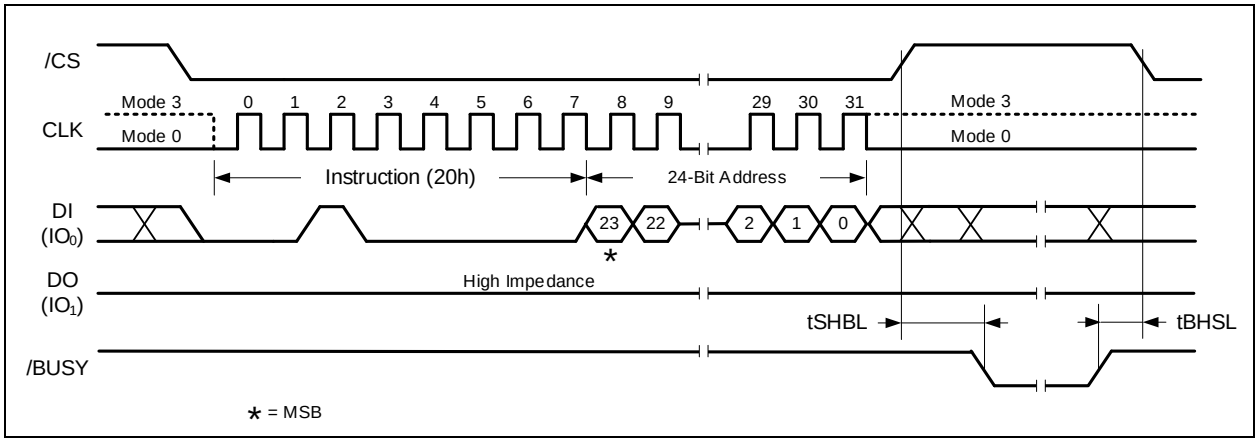





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## 7.15 /BUSY Timing

The following timing diagram illustrates /BUSY signal behavior during Sector Erase (20h) instruction. All other ***Erase and Program*** instructions have similar timing relationship between /CS and /BUSY.

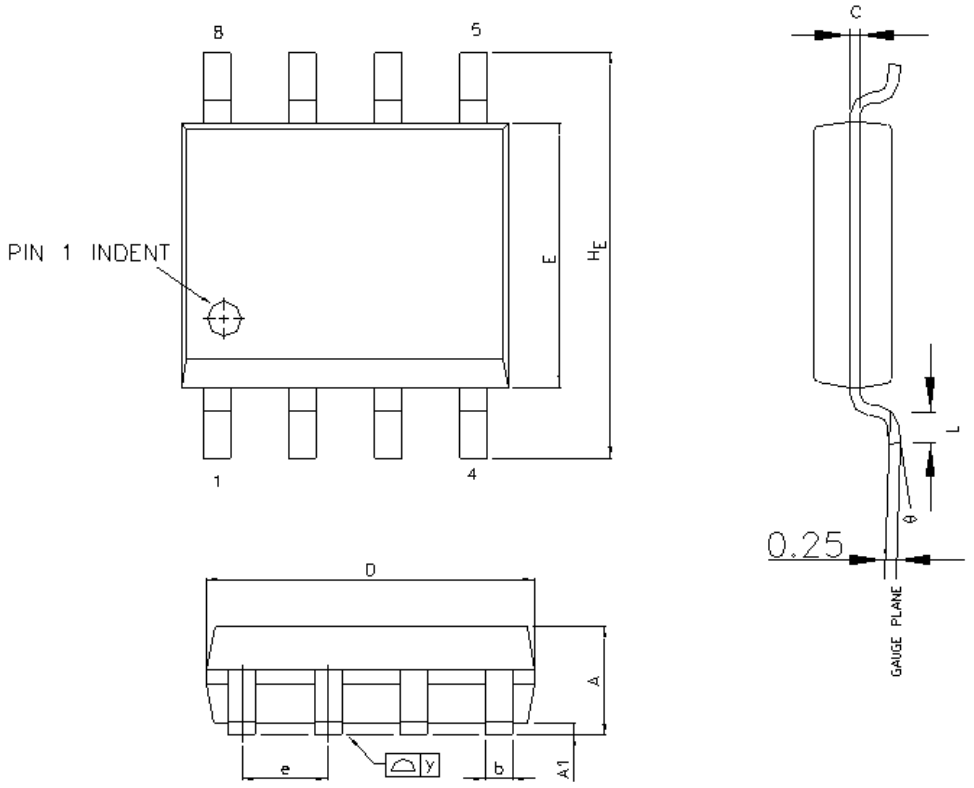





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# 8 PACKAGE SPECIFICATIONS

## 8.1 8-Pin SOP 150-mil (Package Code SN/CN)




| SYMBOL | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 1.35 | 1.60 | 1.75 | 0.053 | 0.062 | 0.069 |
| A1 | 0.10 | 0.15 | 0.25 | 0.004 | 0.006 | 0.010 |
| b | 0.33 | 0.41 | 0.51 | 0.013 | 0.016 | 0.020 |
| C | 0.19 | 0.20 | 0.25 | 0.0075 | 0.0078 | 0.0098 |
| D | 4.80 | 4.85 | 5.00 | 0.188 | 0.190 | 0.197 |
| E | 3.80 | 3.90 | 4.00 | 0.150 | 0.153 | 0.157 |
| $H_E$ | 5.80 | 6.00 | 6.20 | 0.288 | 0.236 | 0.244 |
| e | 1.27BSC | | | 0.050BSC | | |
| L | 0.40 | 0.71 | 1.27 | 0.016 | 0.027 | 0.050 |
| y | --- | --- | 0.10 | --- | --- | 0.004 |
| θ | 0° | --- | 10° | 0° | --- | 10° |

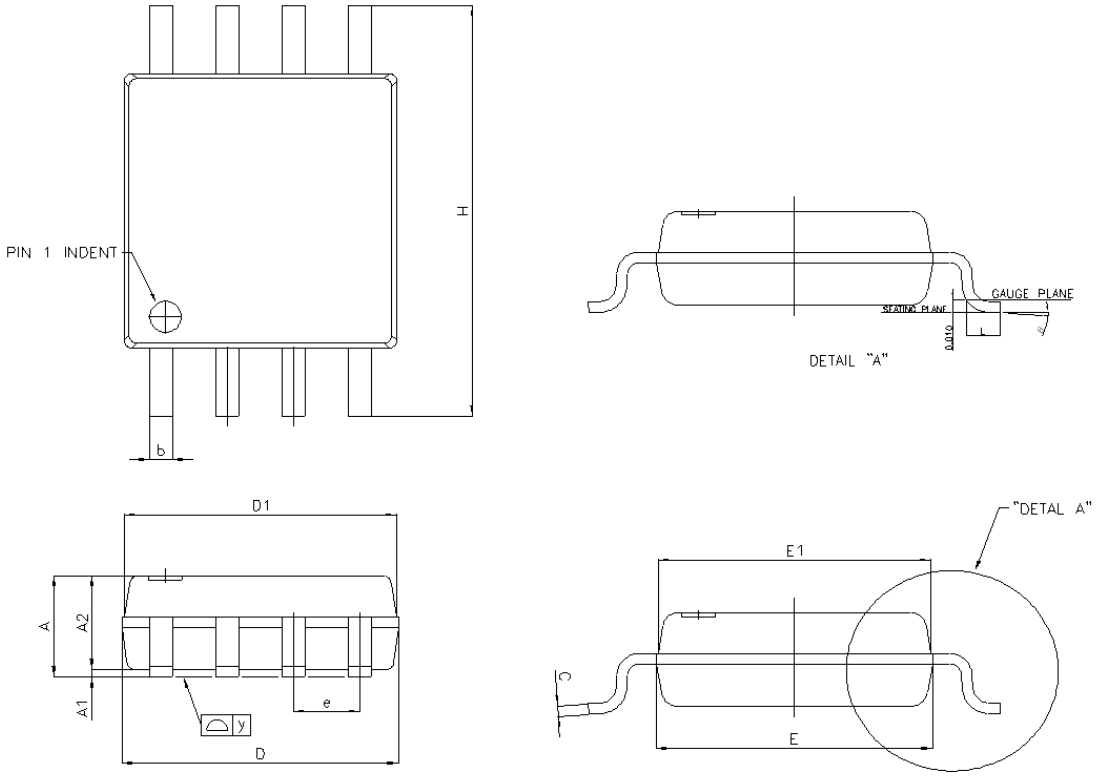
**Note:**

1. Control dimensions are in millimeter.
2. Both the package length and width do not include the mold flash. (Refer JEDEC MS-012)



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## 8.2 8-Pin SOP 208-mil (Package Code SS/CS)




| Symbol | Millimeters | | | Inches | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 1.75 | 1.95 | 2.16 | 0.069 | 0.077 | 0.085 |
| A1 | 0.05 | 0.15 | 0.25 | 0.002 | 0.006 | 0.010 |
| A2 | 1.70 | 1.80 | 1.91 | 0.067 | 0.071 | 0.075 |
| b | 0.35 | 0.42 | 0.48 | 0.014 | 0.017 | 0.019 |
| C | 0.19 | 0.20 | 0.25 | 0.007 | 0.008 | 0.010 |
| D | 5.18 | 5.28 | 5.38 | 0.204 | 0.208 | 0.212 |
| D1 | 5.13 | 5.23 | 5.33 | 0.202 | 0.206 | 0.210 |
| E | 5.18 | 5.28 | 5.38 | 0.204 | 0.208 | 0.212 |
| E1 | 5.13 | 5.23 | 5.33 | 0.202 | 0.206 | 0.210 |
| e | | 1.27 BSC | | | 0.050 BSC | |
| H | 7.70 | 7.90 | 8.10 | 0.303 | 0.311 | 0.319 |
| L | 0.50 | 0.65 | 0.80 | 0.020 | 0.026 | 0.031 |
| y | --- | --- | 0.10 | --- | --- | 0.004 |
| θ | 0° | --- | 8° | 0° | --- | 8° |

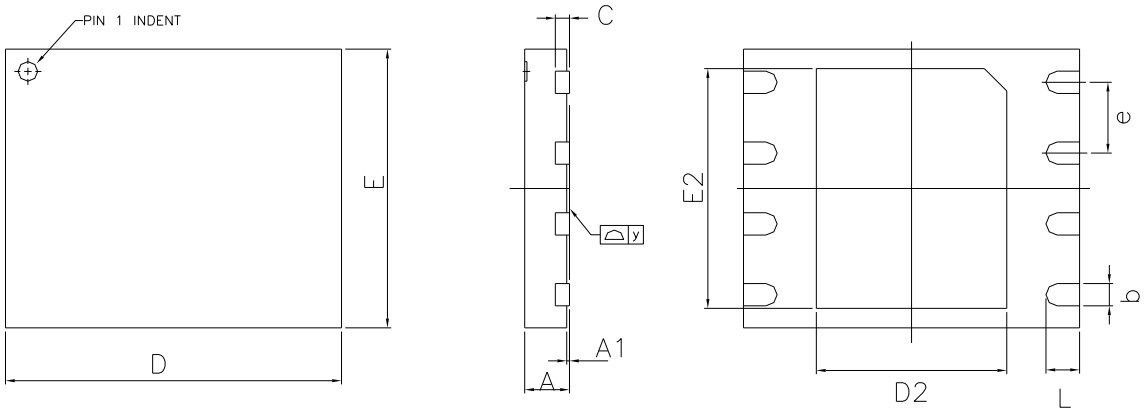
**Note:**

1. Control dimensions are in millimeter.
2. Both the package length and width do not include the mold flash. (Refer JEDEC MS-012)



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## 8.3 8-Pad WSON 6x5-mm (Package Code ZP/CP)




| Symbol | Millimeters | | | Inches | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.70 | 0.75 | 0.80 | 0.028 | 0.030 | 0.031 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| b | 0.35 | 0.40 | 0.48 | 0.014 | 0.016 | 0.019 |
| C | --- | 0.20 REF | --- | --- | 0.008 REF | --- |
| D | 5.90 | 6.00 | 6.10 | 0.232 | 0.236 | 0.240 |
| D2 | 3.35 | 3.40 | 3.45 | 0.132 | 0.134 | 0.136 |
| E | 4.90 | 5.00 | 5.10 | 0.193 | 0.197 | 0.201 |
| E2 | 4.25 | 4.30 | 4.35 | 0.167 | 0.169 | 0.171 |
| e | 1.27 BSC | | | 0.050 BSC | | |
| L | 0.55 | 0.60 | 0.65 | 0.022 | 0.024 | 0.026 |
| y | 0.00 | --- | 0.075 | 0.000 | --- | 0.003 |

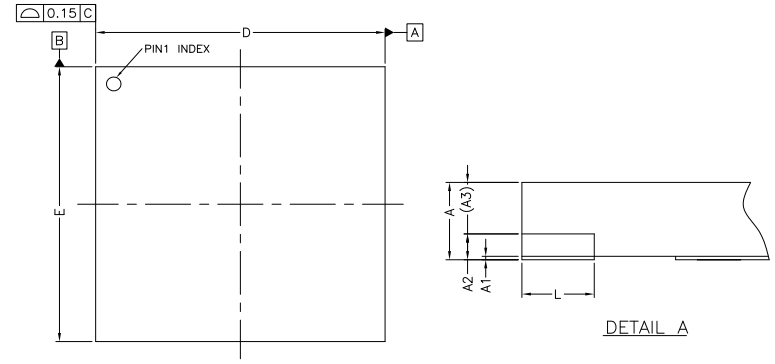
**Note:**

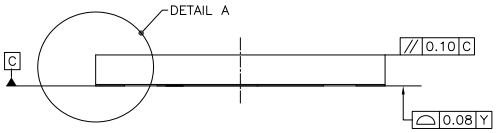
1. The metal pad area on the bottom center of the package is not connected to any internal electrical signals. It can be left floating or connected to the device ground (GND pin). Avoid placement of exposed PCB vias under the pad.

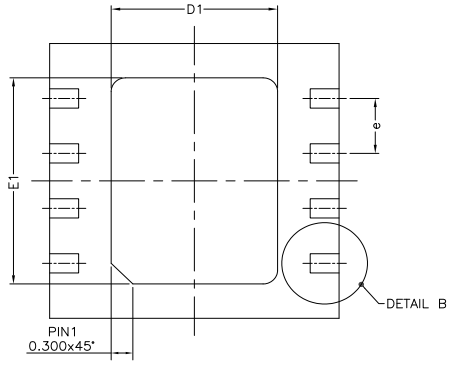


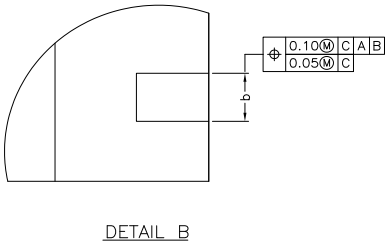
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## 8.4 8-Pad XSON 4x4x0.45-mm (Package Code XG)




| SYMBOL | DIMENSION (MM) | | | DIMENSION (Inch) | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.40 | 0.45 | 0.50 | 0.0157 | 0.0177 | 0.0196 |
| A1 | 0.00 | 0.02 | 0.05 | 0 | 0.0007 | 0.0019 |
| A2 | – | 0.15 | – | – | 0.0059 | – |
| A3 | 0.25 | 0.30 | 0.35 | 0.0098 | 0.0118 | 0.0137 |
| b | 0.25 | 0.30 | 0.35 | 0.0098 | 0.0118 | 0.0137 |
| D | 3.90 | 4.00 | 4.10 | 0.1535 | 0.1574 | 0.1614 |
| D1 | 2.20 | 2.30 | 2.40 | 0.0866 | 0.0905 | 0.0944 |
| E | 3.90 | 4.00 | 4.10 | 0.1535 | 0.1574 | 0.1614 |
| E1 | 2.90 | 3.00 | 3.10 | 0.1141 | 0.1181 | 0.1220 |
| e | 0.80 BSC | | | 0.0314 BSC | | |
| L | 0.35 | 0.40 | 0.45 | 0.0137 | 0.0157 | 0.0177 |

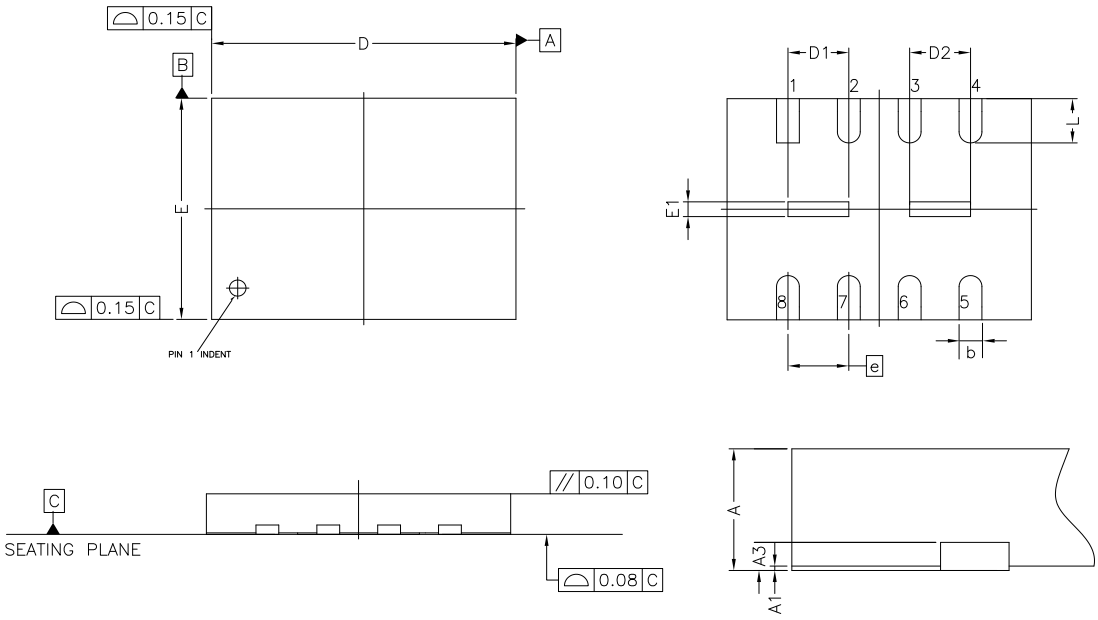
**Note:**

1. The metal pad area on the bottom center of the package is not connected to any internal electrical signals. It can be left floating or connected to the device ground (GND pin). Avoid placement of exposed PCB vias under the pad.



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## 8.5 8-Pad USON 4x3-mm (Package Code UU)




| Symbol | Millimeters | | | Inches | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.50 | 0.55 | 0.60 | 0.020 | 0.022 | 0.024 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| A3 | --- | 0.15 | --- | --- | 0.006 | --- |
| b | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |
| D | 3.90 | 4.00 | 4.10 | 0.153 | 0.157 | 0.161 |
| D1 | 0.70 | 0.80 | 0.90 | 0.027 | 0.031 | 0.035 |
| D2 | 0.70 | 0.80 | 0.90 | 0.027 | 0.031 | 0.035 |
| E | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| E1 | 0.10 | 0.20 | 0.30 | 0.004 | 0.008 | 0.012 |
| e | 0.80 BSC | | | 0.031 BSC | | |
| L | 0.55 | 0.60 | 0.65 | 0.022 | 0.024 | 0.026 |

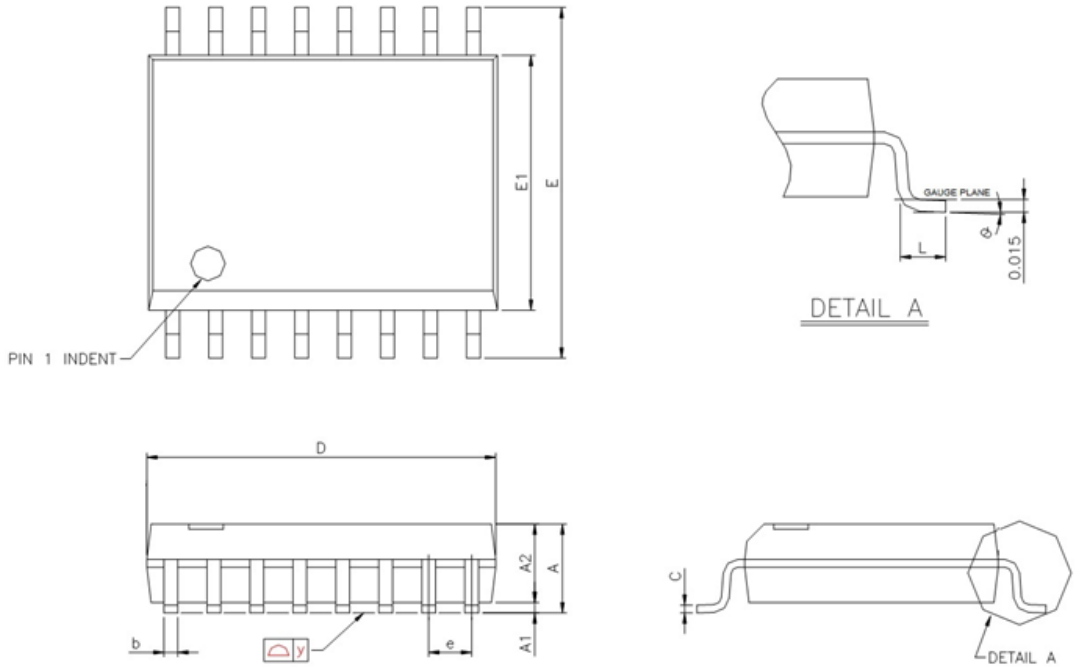
**Note:**

1. The metal pad area on the bottom center of the package is not connected to any internal electrical signals. It can be left floating or connected to the device ground (GND pin). Avoid placement of exposed PCB vias under the pad.



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## 8.6 16-Pin SOP 300-mil (Package Code SF/CF)




| Symbol | Millimeters | | | Inches | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 2.36 | 2.49 | 2.64 | 0.093 | 0.098 | 0.104 |
| A1 | 0.10 | --- | 0.30 | 0.004 | --- | 0.012 |
| A2 | --- | 2.31 | --- | --- | 0.091 | --- |
| b | 0.33 | 0.41 | 0.51 | 0.013 | 0.016 | 0.020 |
| C | 0.18 | 0.23 | 0.28 | 0.007 | 0.009 | 0.011 |
| D | 10.08 | 10.31 | 10.49 | 0.397 | 0.406 | 0.413 |
| E | 10.01 | 10.31 | 10.64 | 0.394 | 0.406 | 0.419 |
| E1 | 7.39 | 7.49 | 7.59 | 0.291 | 0.295 | 0.299 |
| e | 1.27 BSC | | | 0.050 BSC | | |
| L | 0.38 | 0.81 | 1.27 | 0.015 | 0.032 | 0.050 |
| y | --- | --- | 0.076 | --- | --- | 0.003 |
| θ | 0° | --- | 8° | 0° | --- | 8° |

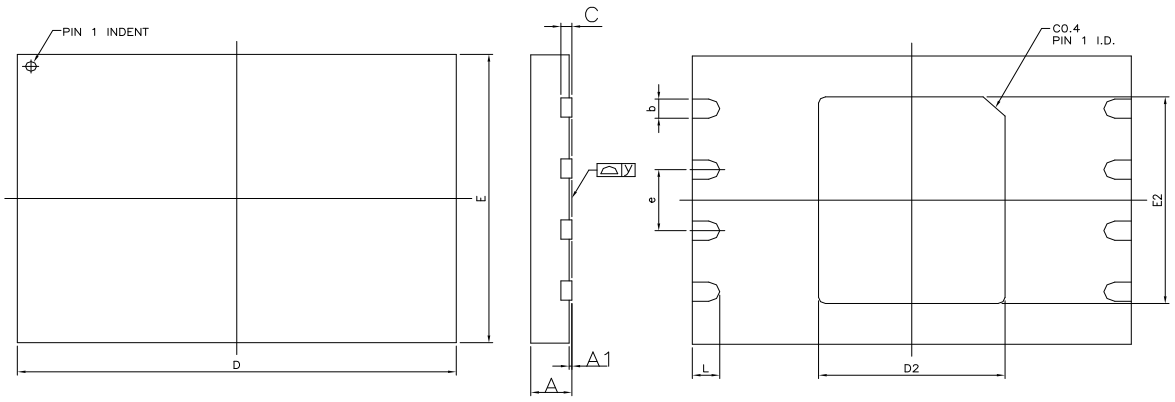
**Note:**

1. Both the package length and width do not include the mold flash. (Refer JEDEC MS-012)



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## 8.7 8-Pad WSON 8x6-mm (Package Code ZE/CE)




| SYMBOL | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.70 | 0.75 | 0.80 | 0.028 | 0.030 | 0.031 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| b | 0.35 | 0.40 | 0.48 | 0.014 | 0.016 | 0.019 |
| C | --- | 0.20 Ref. | --- | --- | 0.008 Ref. | --- |
| D | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| D2 | 3.35 | 3.40 | 3.45 | 0.132 | 0.134 | 0.136 |
| E | 5.90 | 6.00 | 6.10 | 0.232 | 0.236 | 0.240 |
| E2 | 4.25 | 4.30 | 4.35 | 0.167 | 0.169 | 0.171 |
| e | 1.27 BSC | | | 0.050 BSC | | |
| L | 0.45 | 0.50 | 0.55 | 0.018 | 0.020 | 0.022 |
| y | 0.00 | --- | 0.05 | 0.000 | --- | 0.002 |

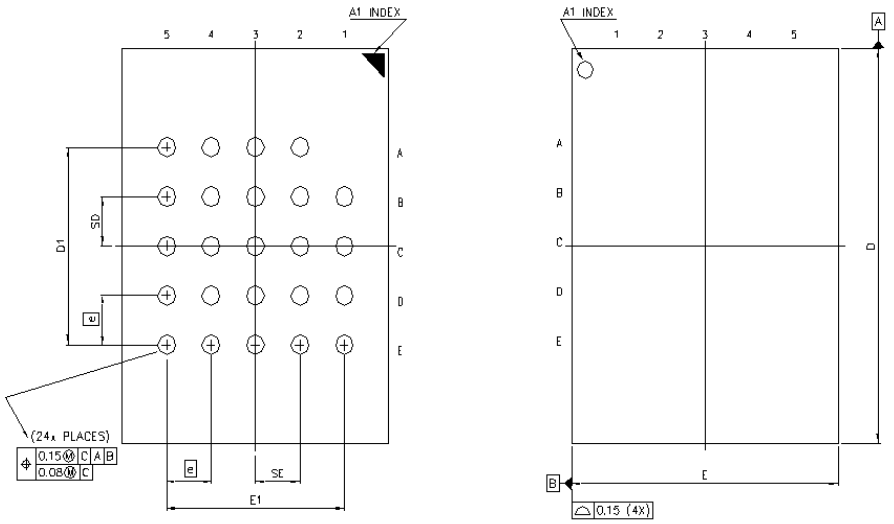
**Note:**

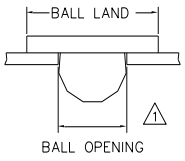
1. The metal pad area on the bottom center of the package is connected to the device ground (VSS pin). Avoid placement of exposed PCB vias under the pad.



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## 8.8 24-Ball TFBGA 8x6-mm (Package Code TB/CB, 5x5-1 Ball Array)



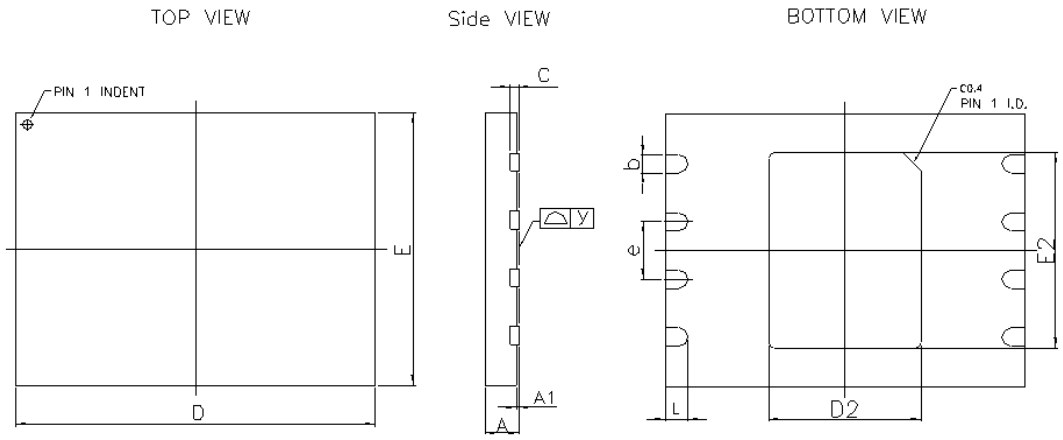




Note:
Ball land: 0.45mm. Ball Opening: 0.35mm
PCB ball land suggested <= 0.35mm

| Symbol | Millimeters | | | Inches | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | --- | --- | 1.20 | --- | --- | 0.047 |
| A1 | 0.26 | 0.31 | 0.36 | 0.010 | 0.012 | 0.014 |
| A2 | --- | 0.85 | --- | --- | 0.033 | --- |
| b | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| D | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| D1 | 4.00 BSC | | | 0.157 BSC | | |
| E | 5.90 | 6.00 | 6.10 | 0.232 | 0.236 | 0.240 |
| E1 | 4.00 BSC | | | 0.157 BSC | | |
| SE | 1.00 TYP | | | 0.039 TYP | | |
| SD | 1.00 TYP | | | 0.039 TYP | | |
| e | 1.00 BSC | | | 0.039 BSC | | |
| ccc | --- | --- | 0.10 | --- | --- | 0.0039 |


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## 8.9 8-Pad VSON 8x6-mm (Package Code ZH)



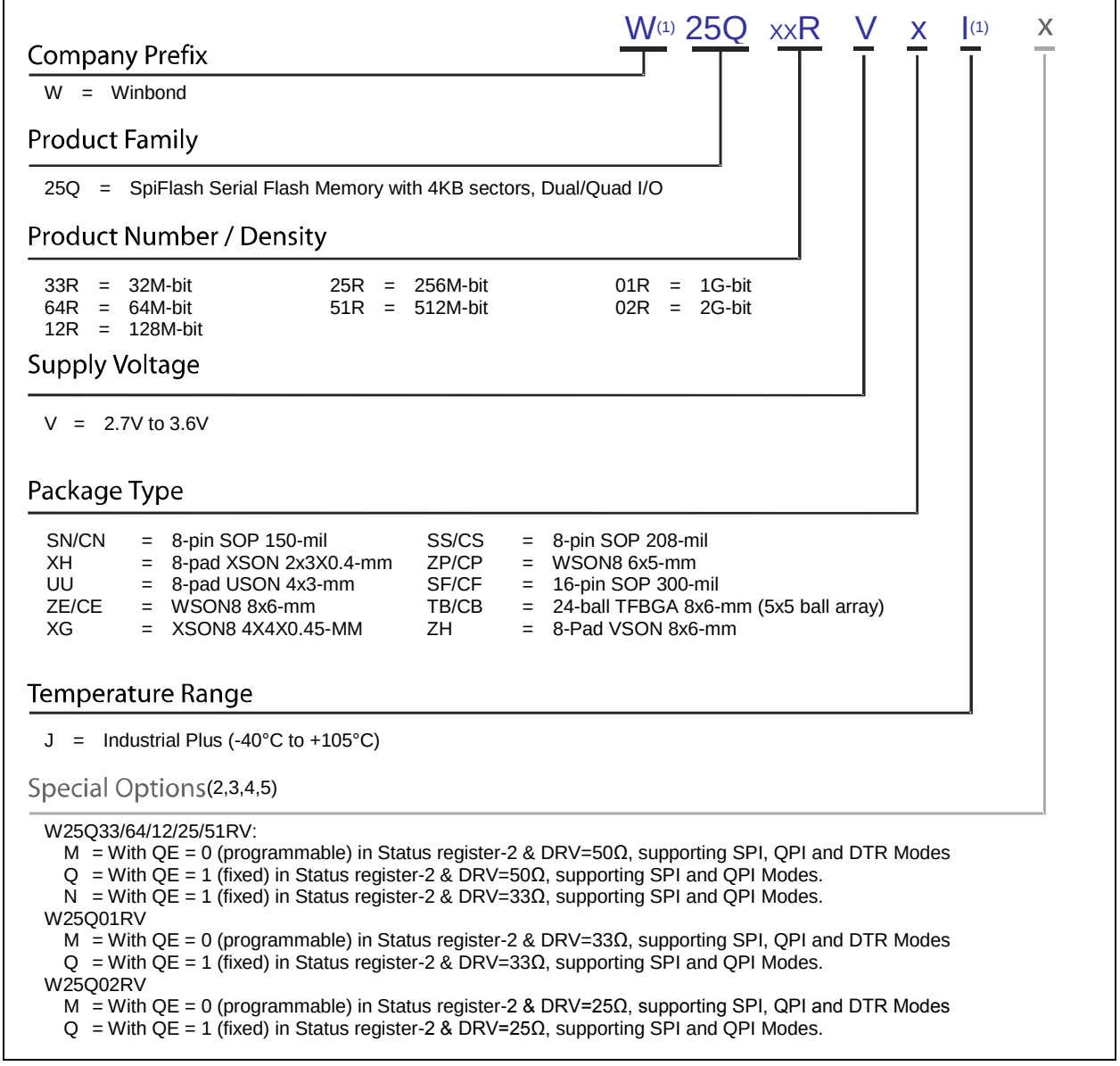

| Symbol | Millimeters | | | Inches | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.90 | 0.95 | 1.00 | 0.035 | 0.037 | 0.039 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.008 | 0.002 |
| b | 0.35 | 0.40 | 0.48 | 0.014 | 0.016 | 0.019 |
| C | --- | 0.20 REF | --- | --- | 0.008 REF | --- |
| D | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| D2 | 3.35 | 3.40 | 3.45 | 0.132 | 0.134 | 0.136 |
| E | 5.90 | 6.00 | 6.10 | 0.232 | 0.236 | 0.240 |
| E2 | 4.25 | 4.30 | 4.35 | 0.167 | 0.169 | 0.171 |
| e | 1.27 BSC | | | 0.050 BSC | | |
| L | 0.45 | 0.50 | 0.55 | 0.018 | 0.020 | 0.022 |
| y | 0.00 | — | 0.08 | 0.000 | — | 0.003 |

Note: The metal pad area on the bottom center of the package is not connected to any internal electrical signals. It can be left floating or connected to the device ground (VSS pin). Avoid placement of exposed PCB vias under the pad.



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# 9 ORDERING INFORMATION




**Note:**

1. The “W” prefix and the Temperature designator “I” are not included on the part marking.
2. Standard bulk shipments are in Tube (shape E). Please specify alternate packing method, such as Tape and Reel (shape T) or Tray (shape S), when placing orders.
3. For shipments with special order options, please contact Winbond.
4. For shipments with OTP feature, please contact Winbond for details.
5. All devices are in compliance of RoHs, Halogen free, TSCA, and REACH.



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## 9.1 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the W25QxxRV SpiFlash Memory. Please contact Winbond for specific availability by density and package type. Winbond SpiFlash memories use a 12-digit Product Number for ordering. However, due to limited space, the Top Side Marking on all packages uses an abbreviated 10-digit number.

**W25Q33RV-JQ valid part numbers:** Industrial Plus(-40°C to +105°C)

| PACKAGE TYPE | DENSITY | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|
| **SN**<br>SOP-8 150mil | 32M-bit | W25Q33RVSNJQ | 25Q33RVNJQ |
| **SS**<br>SOP-8 208-mil | 32M-bit | W25Q33RVSSJQ | 25Q33RVSJQ |
| **UU**<br>USON-8 4x3mm | 32M-bit | W25Q33RVUUJQ | Q33RVUUJQ |
| **XG**<br>XSON-8<br>4x4x0.45-mm | 32M-bit | W25Q33RVXGJQ | Q33RVXGJQ |
| **ZP**<br>WSON-8 6x5-mm | 32M-bit | W25Q33RVZPJQ | 25Q33RVJQ |



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**W25Q33RV-JM valid part numbers:** Industrial Plus(-40°C to +105°C)

| PACKAGE TYPE | DENSITY | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|
| **SN**<br>SOP-8 150mil | 32M-bit | W25Q33RVSNJM | 25Q33RVNJM |
| **SS**<br>SOP-8 208-mil | 32M-bit | W25Q33RVSSJM | 25Q33RVSJM |
| **UU**<br>USON-8 4x3mm | 32M-bit | W25Q33RVUUJM | Q33RVUUJM |
| **XG**<br>XSON-8<br>4x4x0.45-mm | 32M-bit | W25Q33RVXGJM | Q33RVXGJM |
| **ZP**<br>WSON-8 6x5-mm | 32M-bit | W25Q33RVZPJM | 25Q33RVJM |



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**W25Q64RV-JQ valid part numbers:** Industrial Plus(-40°C to +105°C)

| PACKAGE TYPE | DENSITY | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|
| **CN**<br>SOP-8 150mil | 64M-bit | W25Q64RVCNJQ | 25Q64RVCNJQ |
| **CS**<br>SOP-8 208-mil | 64M-bit | W25Q64RVCSJQ | 25Q64RVCSJQ |
| **XG**<br>XSON-8<br>4x4x0.45-mm | 64M-bit | W25Q64RVXGJQ | Q64RVXGJQ |
| **CP**<br>WSON-8 6x5-mm | 64M-bit | W25Q64RVCPJQ | 25Q64RVCPJQ |

**W25Q64RV-JM valid part numbers:** Industrial Plus(-40°C to +105°C)

| PACKAGE TYPE | DENSITY | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|
| **CN**<br>SOP-8 150mil | 64M-bit | W25Q64RVCNJM | 25Q64RVCNJM |
| **CS**<br>SOP-8 208-mil | 64M-bit | W25Q64RVCSJM | 25Q64RVCSJM |
| **XG**<br>XSON-8<br>4x4x0.45-mm | 64M-bit | W25Q64RVXGJM | Q64RVXGJM |
| **CP**<br>WSON-8 6x5-mm | 64M-bit | W25Q64RVCPJM | 25Q64RVCPJM |



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**W25Q12RV-JQ valid part numbers:** Industrial Plus(-40°C to +105°C)

| PACKAGE TYPE | DENSITY | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|
| **CF** SOP-16 300mil | 128M-bit | W25Q12RVCFJQ | W25Q12RVCFJQ |
| **CS** SOP-8 208-mil | 128M-bit | W25Q12RVCSJQ | W25Q12RVCSJQ |
| **CP** WSON-8 6x5-mm | 128M-bit | W25Q12RVCPJQ | W25Q12RVCPJQ |

**W25Q12RV-JM valid part numbers:** Industrial Plus(-40°C to +105°C)

| PACKAGE TYPE | DENSITY | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|
| **CF** SOP-16 300mil | 128M-bit | W25Q12RVCFJM | W25Q12RVCFJM |
| **CS** SOP-8 208-mil | 128M-bit | W25Q12RVCSJM | W25Q12RVCSJM |
| **CP** WSON-8 6x5-mm | 128M-bit | W25Q12RVCPJM | W25Q12RVCPJM |



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**W25Q25RV-JQ valid part numbers:** Industrial Plus(-40°C to +105°C)

| PACKAGE TYPE | DENSITY | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|
| **CF**<br>SOP-16 300mil | 256M-bit | W25Q25RVCFJQ | 25Q25RVCFJQ |
| **CP**<br>WSON-8 6x5-mm | 256M-bit | W25Q25RVCPJQ | 25Q25RVCPJQ |
| **CB**(1)<br>TFBGA-24 8x6-mm<br>(5x5-1 Ball Array) | 256M-bit | W25Q25RVCBJQ | 25Q25RVCBJQ |
| **CE**<br>WSON-8 8x6-mm | 256M-bit | W25Q25RVCEJQ | 25Q25RVCEJQ |

**W25Q25RV-JM valid part numbers:** Industrial Plus(-40°C to +105°C)

| PACKAGE TYPE | DENSITY | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|
| **CF**<br>SOP-16 300mil | 256M-bit | W25Q25RVCFJM | 25Q25RVCFJM |
| **CP**<br>WSON-8 6x5-mm | 256M-bit | W25Q25RVCPJM | 25Q25RVCPJM |
| **CB**(1)<br>TFBGA-24 8x6-mm<br>(5x5-1 Ball Array) | 256M-bit | W25Q25RVCBJM | 25Q25RVCBJM |
| **CE**<br>WSON-8 8x6-mm | 256M-bit | W25Q25RVCEJM | 25Q25RVCEJM |



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**W25Q51RV-JQ valid part numbers:** Industrial Plus(-40°C to +105°C)

| PACKAGE TYPE | DENSITY | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|
| **CF**<br>SOP-16 300mil | 512M-bit | W25Q51RVCFJQ | 25Q51RVCFJQ |
| **CE**<br>WSON-8 8x6-mm | 512M-bit | W25Q51RVCEJQ | 25Q51RVCEJQ |
| **CB**<br>TFBGA-24 8x6-mm<br>(5x5-1 Ball Array) | 512M-bit | W25Q51RVCBJQ | 25Q51RVCBJQ |

**W25Q51RV-JN valid part numbers:** Industrial Plus(-40°C to +105°C)

| PACKAGE TYPE | DENSITY | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|
| **CF**<br>SOP-16 300mil | 512M-bit | W25Q51RVCFJN | 25Q51RVCFJN |
| **CE**<br>WSON-8 8x6-mm | 512M-bit | W25Q51RVCEJN | 25Q51RVCEJN |

**W25Q51RV-JM valid part numbers:** Industrial Plus(-40°C to +105°C)

| PACKAGE TYPE | DENSITY | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|
| **CF**<br>SOP-16 300mil | 512M-bit | W25Q51RVCFJM | 25Q51RVCFJM |
| **CE**<br>WSON-8 8x6-mm | 512M-bit | W25Q51RVCEJM | 25Q51RVCEJM |
| **CB**<br>TFBGA-24 8x6-mm<br>(5x5-1 Ball Array) | 512M-bit | W25Q51RVCBJM | 25Q51RVCBJM |



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**W25Q01RV-JQ valid part numbers:** Industrial Plus(-40°C to +105°C)

| PACKAGE TYPE | DENSITY | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|
| **SF**<br>SOP-16 300mil | 1G-bit | W25Q01RVSFJQ | 25Q01RVFJQ |
| **ZE**<br>WSON-8 8x6-mm | 1G-bit | W25Q01RVZEJQ | 25Q01RVJQ |
| **TB**<br>TFBGA-24 8x6-mm<br>(5x5 Ball Array) | 1G-bit | W25Q01RVTBJQ | 25Q01RVBJQ |

**W25Q01RV-JM valid part numbers:** Industrial Plus(-40°C to +105°C)

| PACKAGE TYPE | DENSITY | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|
| **SF**<br>SOP-16 300mil | 1G-bit | W25Q01RVSFJM | 25Q01RVFJM |
| **ZE**<br>WSON-8 8x6-mm | 1G-bit | W25Q01RVZEJM | 25Q01RVJM |
| **TB**<br>TFBGA-24 8x6-mm<br>(5x5 Ball Array) | 1G-bit | W25Q01RVTBJM | 25Q01RVBJM |



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**W25Q02RV-JQ valid part numbers:** Industrial Plus(-40°C to +105°C)

| PACKAGE TYPE | DENSITY | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|
| **SF**<br>SOP-16 300mil | 2G-bit | W25Q02RVSFJQ | 25Q02RVFJQ |
| **ZH**<br>VSON-8 8x6-mm | 2G-bit | W25Q02RVZHJQ | 25Q02RVJQ |
| **TB**<br>TFBGA-24 8x6-mm<br>(5x5 Ball Array) | 2G-bit | W25Q02RVTBJQ | 25Q02RVBJQ |

**W25Q02RV-JM valid part numbers:** Industrial Plus(-40°C to +105°C)

| PACKAGE TYPE | DENSITY | PRODUCT NUMBER | TOP SIDE MARKING |
|---|---|---|---|
| **SF**<br>SOP-16 300mil | 2G-bit | W25Q02RVSFJM | 25Q02RVFJM |
| **ZH**<br>VSON-8 8x6-mm | 2G-bit | W25Q02RVZHJM | 25Q02RVJM |
| **TB**<br>TFBGA-24 8x6-mm<br>(5x5 Ball Array) | 2G-bit | W25Q02RVTBJM | 25Q02RVBJM |

**Note:**

1. These package types are special order, please contact Winbond for more information.
2. USON. has special top side marking due to size limitation
3. “yw” is date code “xxxx” is lot ID



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## 9.2 Initial delivery status

The memory array is delivered in the erased state, where all data bits are set to '1' (FFh per byte). This covers all Part Numbers listed in Section "Valid Part Numbers and Top Side Marking".



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## 10 REVISION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---|---|---|---|
| A01 | 09/25/2025 | | New create Preliminary datasheet |
| A02 | 10/03/2025 | 51,96<br><br>8,9<br>151,156<br>148<br>173 | Update 77h/Set Burst with Wrap instruction flow in 4-byte address mode.<br>Updated /RSTO to /BUSY for SOP16 and TFBGA<br>Updated /BUSY AC timing<br>Updated ICC1 for W25Q01RV and W25Q02RV<br>Updated W25Q02RV-JQ valid part numbers |
| B | 10/09/2025 | All | Remove Preliminary information for W25Q51RV, W25Q01RV and W25Q02RV |
| C | 12/05/2025 | 149-150<br>151<br>175<br>57-59,124-125 | Updated Icc3 and with DTR and Icc7<br>Updated tCLQV<br>Updated ZH package for W25Q02RV<br>Updated: 9Ch in QPI mode supports the C0h dummy setting, while 9Ch in SPI mode does not support C0h |
| D | 01/05/2025 | 59,82<br>164<br>172<br>176 | Updated BDh command table & waveform<br>Updated Note for WSON center-Pad<br>Added W25Q25RVCE Part No<br>Added Initial delivery status |
| E | 02/12/2026 | 175 | Removed duplicate EEh from instruction description<br>Added tCLSH for DTR |
| | | 0, 3 , 48-60, 138<br>140--141,164-166,168-170 | W25Q33RV/64RV/12RV:<br>- Removed “Preliminary”<br>- Added command table with operating frequency<br>- Updated ICC1 and tSE (max.) specifications. |
| | | 61-71,139<br>168-169 | W25Q25RV/51RV/01RV/02RV<br>- Added command table with operating frequency |

## Preliminary Designation

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