W25N02LVxxxx

3.3V 2G-BIT
SLC QSPI NAND FLASH MEMORY
DUAL/QUAD SPI WITH 133MHZ STR & 66MHZ DTR
BUFFER READ, CONTINUOUS READ &
SEQUENTIAL READ

Release Date: March 24th, 2026

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com
微信扫码咨询客服

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1. GENERAL DESCRIPTIONS

The W25N02LV (2G-bit) Serial SLC NAND Flash Memory provides a storage solution for systems with limited space, pins, and power. The W25N SpiFlash family incorporates the popular SPI interface and the traditional large NAND non-volatile memory space. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 20mA active (for Program and Erase) and 10µA for standby. All W25N SpiFlash family devices are offered in space-saving packages which were not available in the past for typical NAND flash memories.

The W25NxxLV supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 133MHz are supported allowing equivalent clock rates of 266MHz (133MHz x2) for Dual I/O and 532MHz (133MHz x4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions.

The W25NxxLV provides a Continuous Read Mode and a Sequential Read Mode that allows for efficient access to the entire memory array with a single Read instruction. This feature is ideal for code shadowing applications.

A Hold pin, Write Protect pin and programmable write protection provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device ID, Unique ID page, Parameter page and ten OTP pages.

2. FEATURES

- **New W25N Family of SpiFlash Memories**
  - W25N02LV: 2G-bit / 256M-Bytes
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - Compatible SPI Serial Flash instructions
- **Organization**
  - Page size: 2,176 Bytes (2048+128 Bytes)
  - Block size: 64 pages (128K + 8K Bytes)
- **Highest Performance Serial NAND Flash**
  - STR 133MHz Standard/Dual/Quad SPI clocks
  - DTR 66MHz Standard/Quad SPI clocks
  - 266/532MHz equivalent Dual/Quad SPI
  - Max 66MB/s data transfer rate
  - Fast Program/Erase performance
  - Factory Program Mode reduce Program time
  - Endurance: 60,000 Erase/Program Cycles (1)
  - Data Retention: 10-years
- **Supported Read Modes (2)**
  - Buffer Read (Buffer Read with Cache is also available by setting the Status Register bit BRC-E)
  - Continuous Read
  - Sequential Read
- **Low Power, Wide Temperature Range**
  - Single 2.7 to 3.6V power supply
  - 20mA active (for Program and Erase)
  - 10µA standby current
  - -40 to +85°C operating range for Industrial Grade
  - -40 to +105°C operating range for Industrial Plus Grade
- **Flexible Architecture with 128KB blocks**
  - Uniform 128K-Bytes Block Erase
  - Flexible page data load methods
- **Advanced Features**
  - Built-in 8-Bit ECC for memory array
  - ECC status bits indicate ECC results
  - Bad Block Management and LUT (3) access
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down and OTP protection
  - Unique ID and Parameter page (4)
  - Ten OTP pages per die (5)
  - "/HOLD or /RESET (IO3)" pin function switch for WSON package
- **Space Efficient Packaging**
  - 8-pad WSON 8x6-mm
  - 24-ball TFBGA 8x6-mm
  - Contact Winbond for other package options

Notes:

1. Endurance specification is based on 8bit/544 bytes ECC (Error Correcting Code).
2. Only the Read instruction structures are different between the "Continuous Read Mode", "Sequential Read Mode" and the "Buffer Read Mode". All other instructions are identical.
   W25NxxLVxxxG: Buffer Read Mode as default after power-up and can be switch to Continuous Read Mode
   W25NxxLVxxxT: Continuous Read Mode as default after power-up and can be switch to Buffer Read Mode
   W25NxxLVxxxE: Buffer Read Mode as default after power-up and can be switched to Sequential Read Mode
   W25NxxLVxxxU: Sequential Read Mode as default after power-up and can be switched to Buffer Read Mode
   W25NxxLVxxxR: Buffer Read Mode only
3. LUT stands for Look-Up Table.
4. Please refer to 8.2.30 and 8.2.3130 for detailed information.
5. OTP pages can only be programmed.

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3. PACKAGE TYPES AND PIN CONFIGURATIONS

The W25NxxLV is offered in an 8-pad WSON 8x6-mm (package code CE) and a 24-ball 8x6-mm TFBGA (package code CB) package as shown in Figure 3-1 and 3-2 respectively. Package diagrams and dimensions are illustrated at the end of this datasheet.

3.1 Pad Configuration WSON 8x6-mm

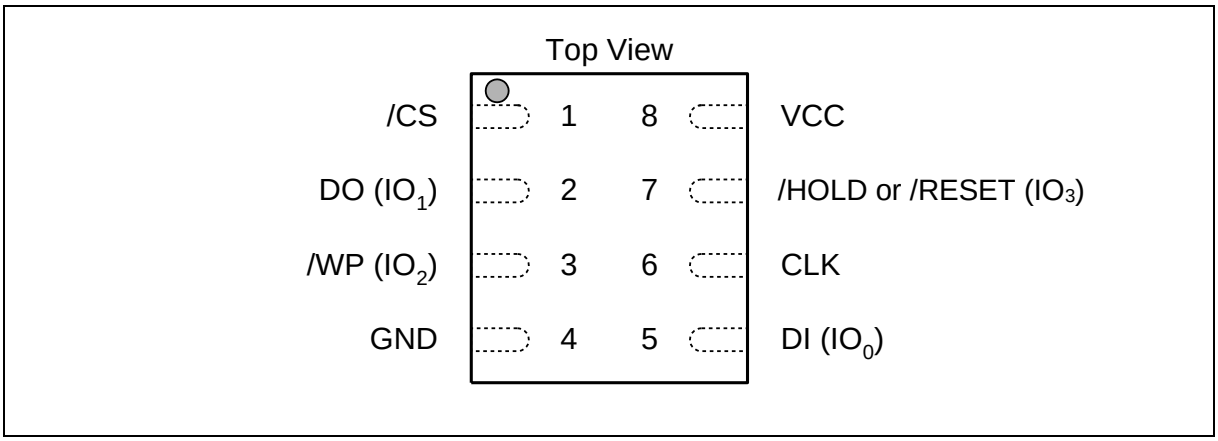


Figure 3-1 W25NxxLV Pad Assignments, 8-pad WSON 8x6-mm (Package Code CE)

3.2 Pad Description WSON 8x6-mm

PAD NO.	PAD NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1) (1)
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2) (2)
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0) (1)
6	CLK	I	Serial Clock Input
7	/HOLD or /RESET (IO3)	I/O	Hold or Reset Input (Data Input Output 3) (2)
8	VCC		Power Supply

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions.
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD functions are only available for Standard/Dual SPI.

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3.3 Ball Configuration TFBGA 8x6-mm (5x5-1 Ball Array)

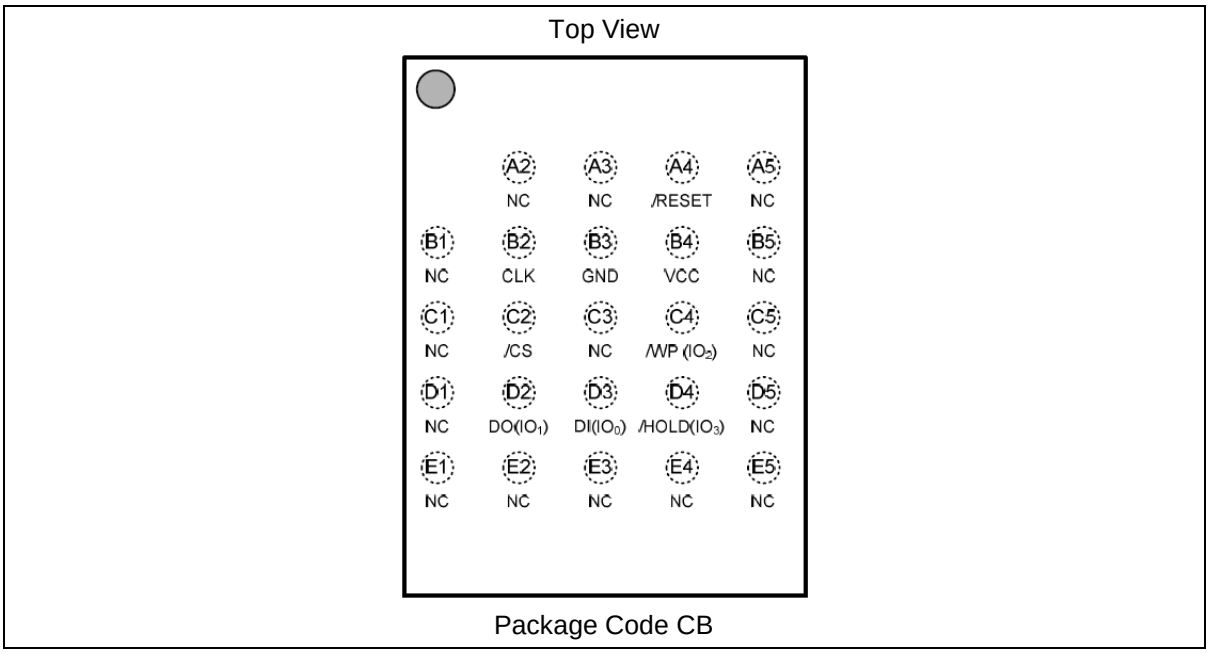


Figure 3-2 W25NxxLV Ball Assignments, 24-ball TFBGA 8x6-mm (Package Code CB)

3.4 Ball Description TFBGA 8x6-mm

BALL NO.	PIN NAME	I/O	FUNCTION
A4	/RESET	I	Reset Input
B2	CLK	I	Serial Clock Input
B3	GND		Ground
B4	VCC		Power Supply
C2	/CS	I	Chip Select Input
C4	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2) (2)
D2	DO (IO1)	I/O	Data Output (Data Input Output 1) (1)
D3	DI (IO0)	I/O	Data Input (Data Input Output 0) (1)
D4	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3) (2)
Multiple	NC		No Connect: NCs are not internally connected. They can be driven or left unconnected.

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions.
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD functions are only available for Standard/Dual SPI.
3. The /RESET pin on the TFBGA package is a dedicated hardware reset pin.

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4. PIN DESCRIPTIONS

4.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high, the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down. If needed, a pull-up resistor on the /CS pin can be used to accomplish this.

4.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25NxxLV supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of the CLK and read data or status from the device on the falling edge of the CLK.

4.3 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect bits BP[3:0] and the Status Register Protect SRP bits SRP[1:0], a portion as small as 256K-Bytes (2x128KB blocks) or the entire memory array can be hardware protected. The WP-E bit in the Protection Register (SR-1) controls the functions of the /WP pin.

When WP-E=0, the device is in the Software Protection mode such that only SR-1 can be protected. The /WP pin functions as a data I/O pin for the Quad SPI operations, as well as an active low input pin for the Write Protection function for SR-1.

When WP-E=1, the device is in the Hardware Protection mode such that /WP becomes a dedicated active low input pin for the Write Protection of the entire device. If /WP is tied to GND, all "Write/Program/Erase" functions are disabled. The entire device (including all registers, memory array and OTP pages) will become read-only. Quad SPI read operations are also disabled when WP-E is set to 1.

4.4 Hold (/HOLD)

During Standard and Dual SPI operations, the /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When H-DIS=1, the /HOLD pin function is not available since this pin is used for IO3. /HOLD (IO3) must be driven high by the host, or an external pull-up resistor must be placed on the PCB, to avoid allowing the /HOLD input to float.

4.5 Serial Clock (CLK)

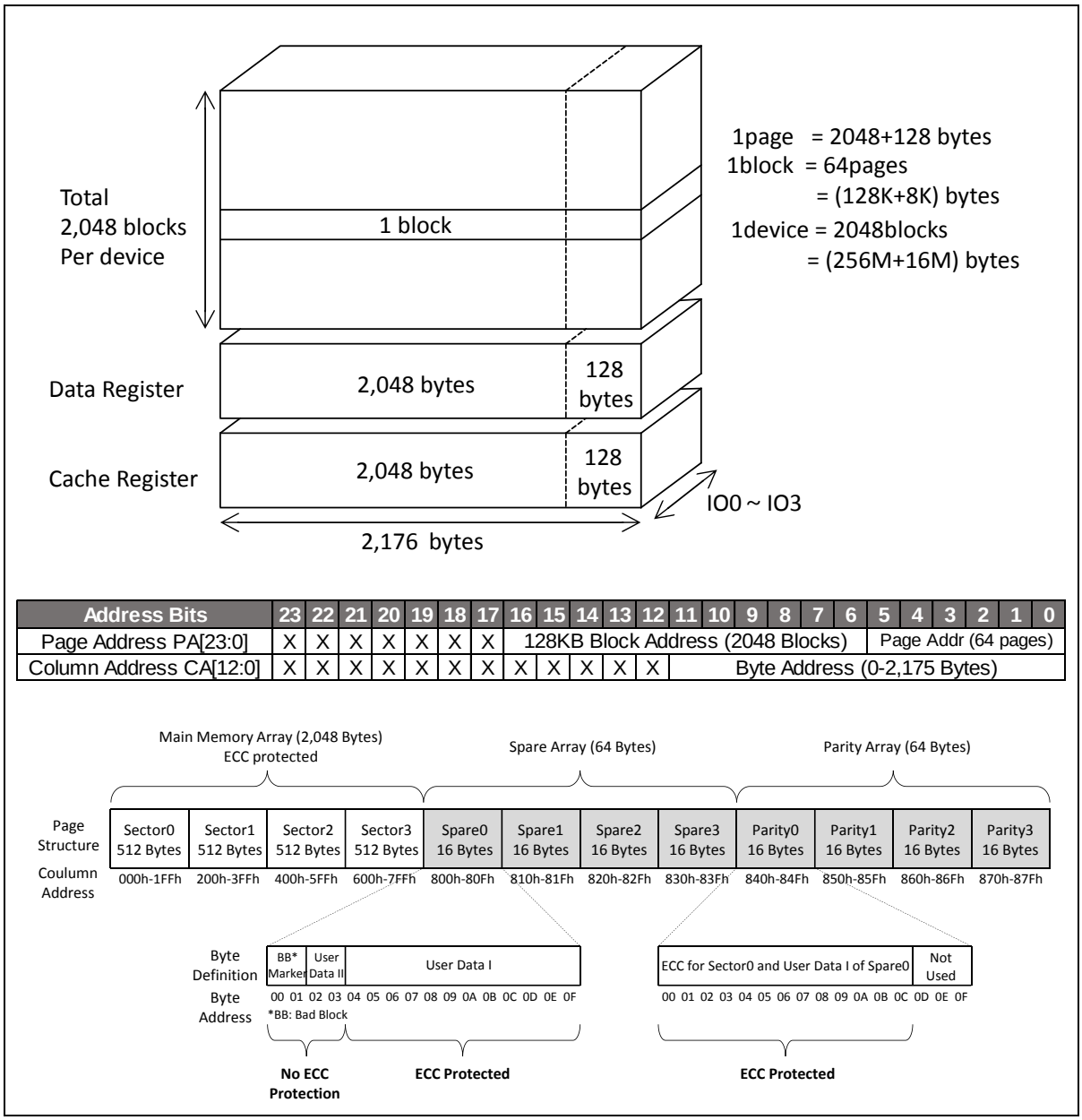
The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations.

4.6 Reset (/RESET)

The /RESET pin allows the device to be reset by the controller and provides hardware level resetting. This is the highest priority among all the input signals. The /RESET pin is available on WSON and TFBGA package types.

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5. BLOCK DIAGRAM



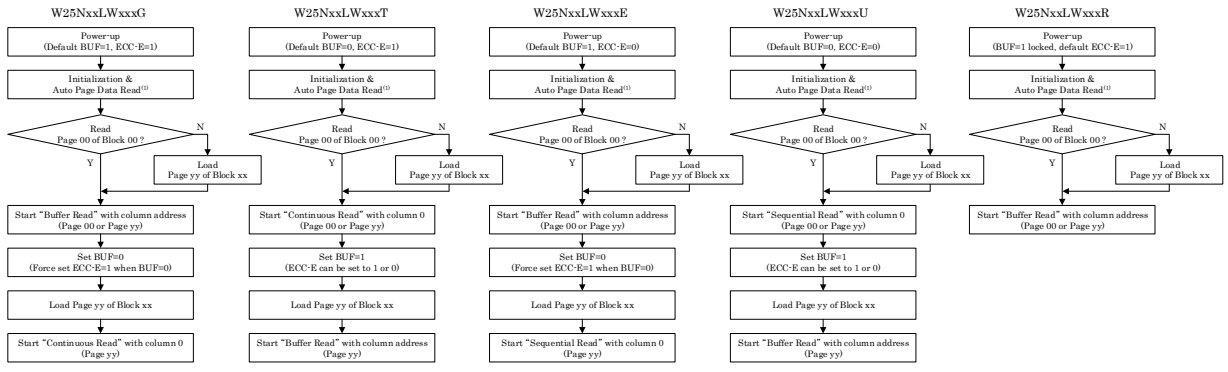
Address Bits	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Page Address PA[23:0]	X	X	X	X	X	X	X	128KB Block Address (2048 Blocks)											Page Addr (64 pages)					
Column Address CA[12:0]	X	X	X	X	X	X	X	X	X	X	X	X	Byte Address (0-2,175 Bytes)											

Figure 5-1 W25N02LV Flash Memory Architecture and Addressing

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6. FUNCTIONAL DESCRIPTIONS

6.1 Device Operation Flow



Notes:

Automatic execution of Page Data Read (13h) instruction for Page 0 of Block 0.

Figure 6-1 W25NxxLV Flash Memory Operation Diagram

6.1.1 Standard SPI Instructions

The W25NxxLV is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0, 0) and 3 (1, 1) are supported. The primary difference between Mode 0 and Mode 3 is the normal state of the CLK signal when the SPI bus master is in standby, and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

6.1.2 Dual SPI Instructions

The W25NxxLV supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)”, “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

6.1.3 Quad SPI Instructions

The W25NxxLV supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, “Fast Read Quad I/O (EBh)” and “Quad Program Data Load (32h/34h)”. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. When using Quad SPI instructions, the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively.

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6.1.4 Hold Function

For Standard SPI and Dual SPI operations, the /HOLD signal allows the W25NxxLV operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case, the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI. When H-DIS=1 or DTR operation is enabled, the /HOLD function is not available.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low, the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low, the /HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

6.1.5 Software Reset

6.1.5.1 Device Reset (FFh) instruction

The Device Reset (FFh) instruction terminates any on-going internal operations without initialization for all volatile writable bits in the Status Registers. If the instruction sequence is successfully accepted, the device will take approximately tRST to reset. No instruction will be accepted during the reset period. Please refer to “8.2.1 Device Reset (FFh), Enable Reset (66h) and Reset Device (99h)” for detailed information about the instruction sequence and the value of each Status Registers after reset.

6.1.5.2 Enable Reset (66h) and Reset Device (99h) instructions

The W25NxxLV can be reset to the initial state by the Enable Reset (66h) & the Reset (99h) instructions. If the instruction sequence is successfully accepted, the device will take approximately tRST to reset. No instruction will be accepted during the reset period. Please refer to “8.2.1 Device Reset (FFh), Enable Reset (66h) and Reset Device (99h)” for detailed information about the instruction sequence and the value of each Status Register after reset.

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6.1.6 Hardware Reset

6.1.6.1 /RESET Pin

For the WSON package, the W25NxxLV has a "/HOLD or /RESET (IO3)" pin, and its function can be switched by the HOLD/RST bit of the Status Register-3. For the TFBGA package, the W25NxxLV provides a dedicated /RESET pin. Driving the /RESET pin low for a minimum period of 1us (tRESET) will reset the device to its initial power-on state. The busy time (tVSL + tPUW + tRST) is the same during a hardware reset or during initial power on. No instruction will be accepted during the tVSL period. The Hardware /RESET pin has the highest priority among all the input signals. Driving /RESET low for a minimum of 1us (tRESET) will interrupt any on-going external/internal operations, regardless of the status of the other SPI signals (/CS, CLK, IOs, /WP and /HOLD). Please refer to “8.2.1 Device Reset (FFh), Enable Reset (66h) and Reset Device (99h)” for detailed information about the value of each Status Register after reset.

Notes:

1. While a faster /RESET pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum pulse is recommended to ensure reliable operation.
2. There is an internal pull-up resistor for the dedicated /RESET pin on the WSON and the TFBGA package. If the reset function is not used, this pin can be left floating in the system.

6.1.6.2 Reset Signaling Protocol

The W25NxxLV provides an additional Hardware Reset by a signaling protocol. This is useful if on the host side it is difficult to reserve a dedicated IO pin for controlling the W25NxxLV's /RESET pin. If the host side supports this signaling protocol, the user can perform a Hardware Reset by using only the /CS, CLK, and DI(IO0) pins. Reset Signaling Protocol will be ignored during busy time for Hardware Reset by /RESET pin. Reset Signaling Protocol is available for all package types.

The key points for the Reset Signaling Protocol are:

- CLK remains stable in either High or Low state. Toggle /CS instead of CLK. This prevents any confusion with instructions, as no instruction bits are transferred (clocked).
- W25NxxLV captures the state of DI(IO0) on the rising edge of /CS.
- DI(IO0) have to be low on the first /CS, high on the second, low on the third, high on the fourth. This 5h pattern (=0b0101) is for differentiation from random noise.

Once the Reset Signaling Protocol is accepted, any on-going internal operations will be terminated, and the device will be reset to its initial power-on state. The busy time (tVSL + tPUW + tRST) is the same during a hardware reset or during initial power on. No instruction will be accepted during the tVSL period. Please refer to “8.2.1 Device Reset (FFh), Enable Reset (66h) and Reset Device (99h)” for detailed information about the value of each Status Register after reset. If there is an on-going internal Erase or Program operation when the Reset instruction sequence is accepted by the device, data corruption may happen at only the address that is the target of the on-going operation. It is recommended to check the BUSY bit in the Status Register before issuing the Reset instruction.

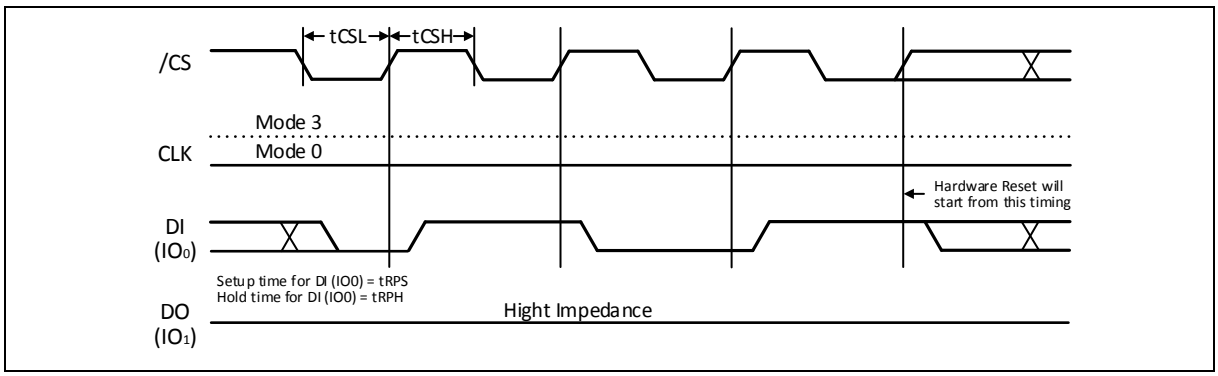


Figure 6-2 Reset Signaling Protocol

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6.2 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25NxxLV provides several means to protect the data from inadvertent writes.

- Device resets when VCC is below the threshold
- Write enable/disable instructions and automatic write disable after Program Execute, Block Erase, Page Data Read and Program Execute for OTP pages
- Software and Hardware (/WP pin) write protection using Protection Register (SR-1)
- Lock Down write protection for Protection Register (SR-1) until the next power-up
- One Time Program (OTP) write protection for memory array using Protection Register (SR-1)
- Hardware write protection using /WP pin when WP-E is set to 1

Upon power-up or at power-down, the W25NxxLV will maintain a reset condition while VCC is below the threshold value of V_{WI}. While reset, all operations are disabled, and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Program Execute, Block Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse instruction sequence. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up, the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Load Program Data, Quad Load Program Data and Block Erase instruction will be accepted. After completing a Program Execute, Block Erase, Page Data Read and Program Execute for OTP pages instruction, the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (TB, BP[3:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control.

The WP-E bit in Protection Register (SR-1) is used to enable the hardware protection. When WP-E is set to 1, bringing /WP low in the system will block any Write/Program/Erase instruction to the W25NxxLV. The device will become read-only. The Quad SPI operations are also disabled when WP-E is set to 1.

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6.3 Interface States

This section describes the input and output signal levels.

	/RESET (1)	/CS	CLK	/HOLD (IO3) (2)	/WP (IO2)	DO (IO1)	DI (IO0)
Power-off	X	X	X	X	X	Z	X
Power-on Reset	- (3)	- (3)	X	X	X	Z	X
Reset (during tRST)	X	X	X	X	X	Z	X
HW Reset	L	X	X	X	X	Z	X
Interface Standby	H	H	X	X	X	Z	X
Hold Cycle	H	L	L or H or T	L	X	Z (4)	X
Single Input Cycle	H	L	T	H	X	Z	L or H
Single Dummy Cycle	H	L	T	H	X	Z	Z
Single Output Cycle	H	L	T	H	X	L or H	X
Dual Input Cycle	H	L	T	H	X	L or H	L or H
Dual Dummy Cycle	H	L	T	H	X	Z	Z
Dual Output Cycle	H	L	T	H	X	L or H	L or H
Quad Input Cycle	H	L	T	L or H	L or H	L or H	L or H
Quad Dummy Cycle	H	L	T	Z	Z	Z	Z
Quad Output Cycle	H	L	T	L or H	L or H	L or H	L or H

H= High input/output level
L= Low input/output level
Z= Hi-Z
X= H or L level
T= Toggling between H and L

Notes:

1. The dedicated /RESET pin is available only for the TFBGA package.
2. For the WSON package, the pin name is "/HOLD or /RESET (IO3)", and its function can be switched by the HOLD/RST bit of the Status Register-3.
3. Refer to Figure 9-2 Power-up, Power-down Requirement.
4. During the input sequence in Dual or Quad mode, this state is “X”.

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7. PROTECTION, CONFIGURATION AND STATUS REGISTERS

Three Status Registers are provided for W25NxxLV: Protection Register (SR-1), Configuration Register (SR-2) & Status Register (SR-3). Each register is accessed by the Read Status Register and the Write Status Register instructions combined with a 1-Byte Register Address respectively.

The Read Status Register instruction (05h/0Fh) can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Read modes, Protection Register/OTP area lock status and Erase/Program results.

The Write Status Register instruction can be used to configure the device write protection features, Software/Hardware write protection, read modes, Protection Register/OTP area lock, number of dummy clocks, and enable/disable Quad operation. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and when WP-E is set to 1, the /WP pin.

7.1 Protection Register / Status Register-1 (Volatile Writable, OTP lockable, Address Axh)

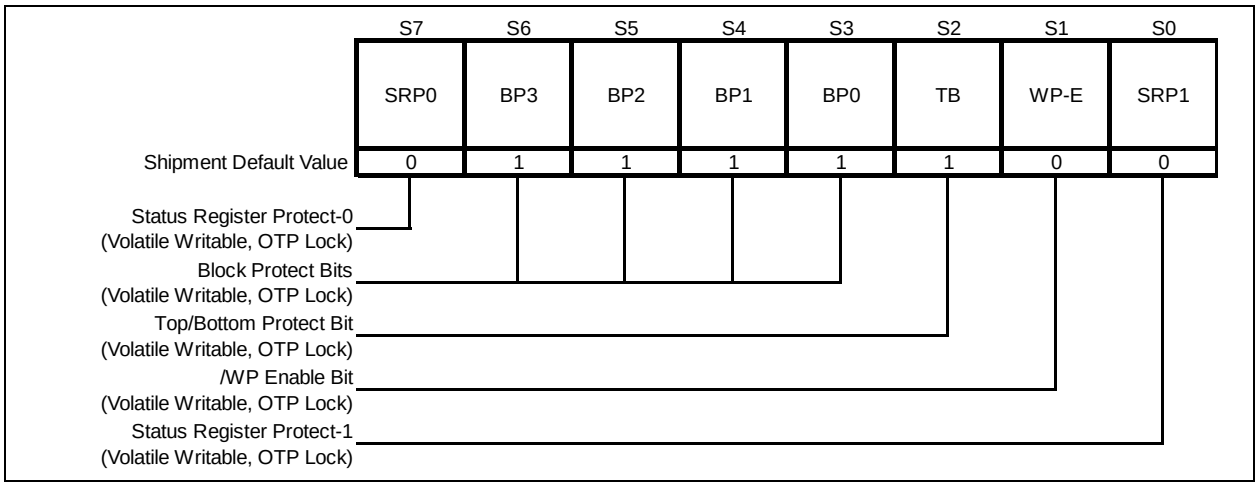


Figure 7-1 Protection Register / Status Register-1 (Address Axh)

7.1.1 Block Protect Bits (BP3, BP2, BP1, BP0, TB) – *Volatile Writable, OTP lockable*

The Block Protect bits (BP3, BP2, BP1, BP0 and TB) are volatile read/write bits in the status register-1 (S6, S5, S4, S3 and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction. All, none or a portion of the memory array can be protected from Program and Erase instructions. The default values for the Block Protection bits are 1 after power-up to protect the entire array. If the SR1-L bit in the Configuration Register (SR-2) is set to 1, the default values will be the values that are OTP locked.

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7.1.2 Write Protection Enable Bit (WP-E) – *Volatile Writable, OTP lockable*

The Write Protection Enable bit (WP-E) is a volatile read/write bit in the status register-1 (S1). The WP-E bit, in conjunction with SRP1 & SRP0, controls the method of write protection: software protection, hardware protection, power supply lock-down or one-time programmable (OTP) protection, /WP pin functionality, and Quad SPI operation enable/disable. When WP-E = 0 (default value), the device is in Software Protection mode, /WP & /HOLD pins are multiplexed as IO pins, and Quad program/read functions are enabled all the time. When WP-E is set to 1, the device is in Hardware Protection mode, all Quad functions are disabled, and the /WP & /HOLD pins become dedicated control input pins.

7.1.3 Status Register Protect Bits (SRP1, SRP0) – *Volatile Writable, OTP lockable*

The Status Register Protect bits (SRP1 and SRP0) are volatile read/write bits in the status register (S0 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one-time programmable (OTP) protection.

Software Protection (Driven by Controller, WP-E is disabled)				
SRP1	**SRP0**	**WP-E**	**/WP/IO2**	**Descriptions**
0	0	0	X	No /WP functionality */WP pin will always function as IO2*
0	1	0	0	SR-1 cannot be changed (/WP = 0 during Write Status) */WP pin will function as IO2 for Quad operations*
0	1	0	1	SR-1 can be changed (/WP = 1 during Write Status) */WP pin will function as IO2 for Quad operations*
1	0	0	X	Power Lock Down (1) SR-1 */WP pin will always function as IO2*
1	1	0	X	Enter OTP mode to protect SR-1 (allow SR1-L=1) */WP pin will always function as IO2*

Hardware Protection (System Circuit / PCB layout, Quad Program/Read is disabled)				
SRP1	**SRP0**	**WP-E**	**/WP only**	**Descriptions**
0	X	1	VCC	SR-1 can be changed
1	0	1	VCC	Power Lock-Down (1) SR-1
1	1	1	VCC	Enter OTP mode to protect SR-1 (allow SR1-L=1)
X	X	1	GND	All "Write/Program/Erase" instructions are blocked Entire device (SRs, Array, OTP area) is read-only

Notes:

1. When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to the (0, 0) state.

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7.2 Configuration Register / Status Register-2 (Volatile Writable, Address Bxh)

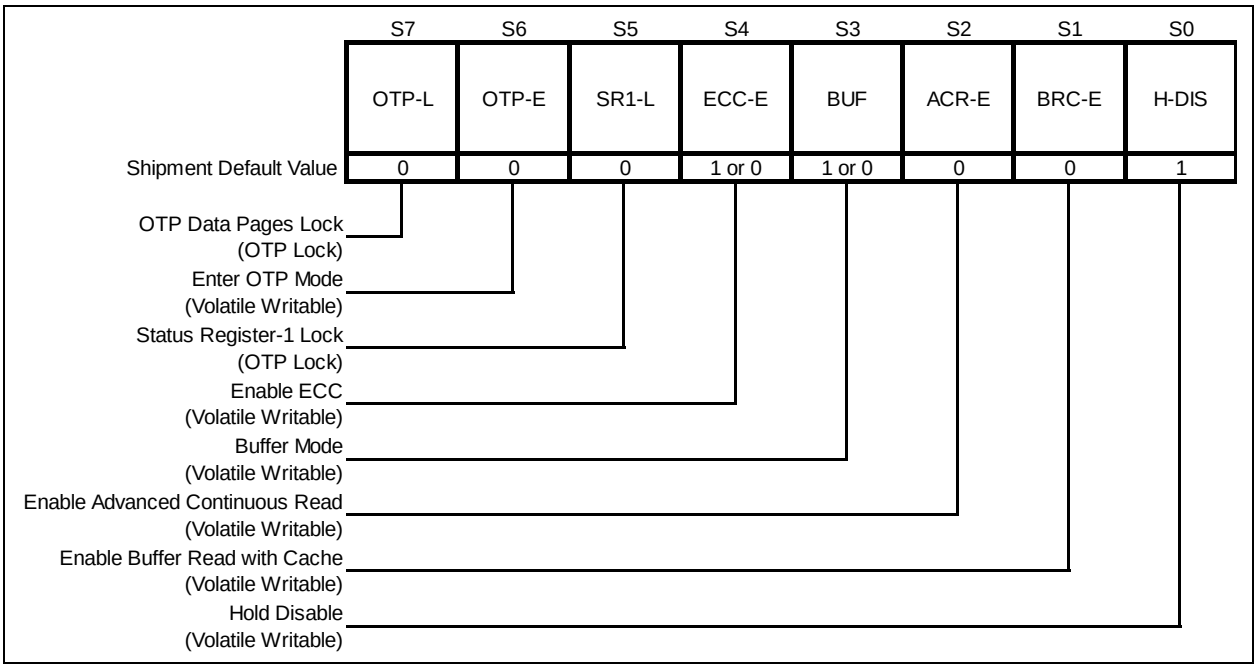


Figure 7-2 Configuration Register / Status Register-2 (Address Bxh)

7.2.1 One Time Program Lock Bit (OTP-L) – *OTP lockable*

In addition to the main memory array, W25NxxLV also provides an OTP area for the system to store critical data that cannot be changed once it's locked. The OTP area consists of 10 pages each. The default data in the OTP area is FFh. Only Program instruction can be issued to the OTP area to change the data from "1" to "0", and data is not reversible ("0" to "1") by using the Erase instruction. Once the correct data is programmed in and verified, the system developer can set OTP-L bit to 1, so that the entire OTP area will be locked to prevent further alteration to the data.

7.2.2 Enter OTP Access Mode Bit (OTP-E) – *Volatile Writable*

The OTP-E bit must be set to 1 to use the standard Program/Read instructions to access the OTP area as well as to read the Unique ID / Parameter Page information. The default value after power-up or a RESET instruction is 0.

7.2.3 Status Register-1 Lock Bit (SR1-L) – *OTP lockable*

The SR1-L lock bit is used to OTP lock the values in the Protection Register (SR-1). Depending on the settings in the SR-1, the device can be configured to have a portion of or up to the entire array to be write-protected, and the setting can be OTP locked by setting SR1-L bit to 1. SR1-L bit can only be set to 1 permanently when SRP1 & SRP0 are set to (1, 1), and OTP Access Mode must be entered (OTP-E=1) to execute the programming.

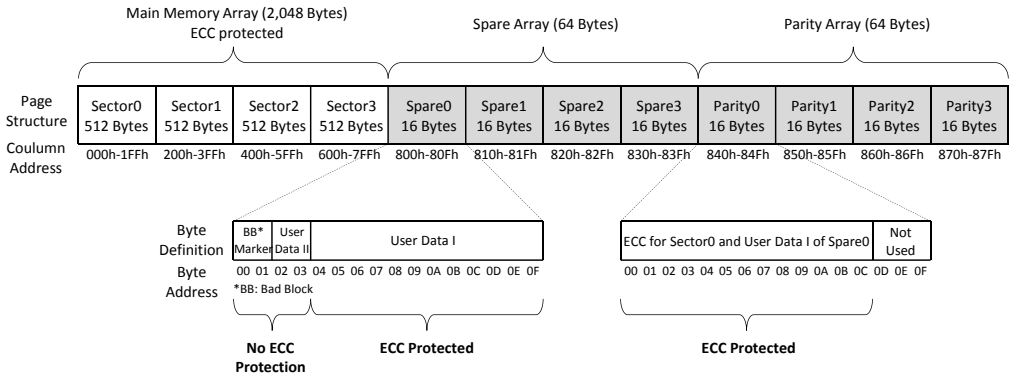
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7.2.4 ECC Enable Bit (ECC-E) – *Volatile Writable*

The W25NxxLV has a built-in ECC algorithm that can be used to preserve the data integrity. Internal ECC calculation is done during page programming, and the result is stored in the extra 128-Bytes parity area for each page. During the data read operation, the ECC engine will verify the data values according to the previously stored ECC information and make the necessary corrections if needed. The verification and correction status are indicated by the ECC Status Bit. The ECC function is enabled by default during power on (ECC-E=1), and it will not be reset to 0 by the Device Reset instruction.

The constraints when ECC-E=1 are as follows:

- The areas protected by ECC are shown in the table below. User Data I is protected by ECC, but User Data II is not protected by ECC.
- The Number of Partial Page Program operations (NoP) is 4 for the entire page, including the spare area. Therefore, the user needs to program one sector and optionally User Data 1 of pared spare area (example, main area-sector 0 and spare area-spare 0) at one time to properly and automatically program the ECC parity code.



Area	Main area			
	Sector 0	Sector 1	Sector 2	Sector 3
Address (Start)	000h	200h	400h	600h
Address (End)	1FFh	3FFh	5FFh	7FFh
Size	512B	512B	512B	512B

Area	Spare area							
	Spare 0		Spare 1		Spare 2		Spare 3	
	UD2	UD1	UD2	UD1	UD2	UD1	UD2	UD1
Address (Start)	800h	804h	810h	814h	820h	824h	830h	834h
Address (End)	803h	80Fh	813h	81Fh	823h	82Fh	833h	83Fh
Size	4B	12B	4B	12B	4B	12B	4B	12B

Area	Parity area							
	Parity 0		Parity 1		Parity 2		Parity 3	
	EPC	NU	EPC	NU	EPC	NU	EPC	NU
Address (Start)	840h	84Dh	850h	85Dh	860h	86Dh	870h	87Dh
Address (End)	84Ch	84Fh	85Ch	85Fh	86Ch	86Fh	87Ch	87Fh
Size	13B	3B	13B	3B	13B	3B	13B	3B

Figure 7-3 ECC Protected Area

Notes:

1. UD2: User Data II
2. UD1: User Data I
3. EPC: ECC parity code
4. NU: Not Used
5. The gray area in the above table is protected by ECC

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7.2.5 Read Mode Bit (BUF) – *Volatile Writable*

The W25NxxLV provides multiple modes for read operations, Buffer Read (BUF=1, ECC-E=1 or 0, ACR-E is ignored, BRC-E=0), Buffer Read with Cache (BUF=1, ECC-E=1 or 0, ACR-E is ignored, BRC-E=1), Continuous Read (BUF=0, ECC-E=1, ACR-E=0, BRC-E is ignored), Advanced Continuous Read (BUF=0, ECC-E=1, ACR-E=1, BRC-E is ignored) and Sequential Read (BUF=0, ECC-E=0, ACR-E is ignored, BRC-E is ignored). Prior to any Read operation, a Page Data Read instruction is needed to initiate the data transfer from a specified page in the memory array to the Data Buffer. By default, after power-up, the data in page 0 of block 0 will automatically be loaded into the Data Buffer and the device will be ready to accept any read instructions.

The Buffer Read (BUF=1, ECC-E=1 or 0, ACR-E is ignored, BRC-E=0) and Buffer Read with Cache (BUF=1, ECC-E=1 or 0, ACR-E is ignored, BRC-E=1) requires a Column Address to start outputting the existing data inside the Data Buffer, and once it reaches the end of the data buffer, the DO (IO1) pin will become high-Z state.

The Continuous Read (BUF=0, ECC-E=1, ACR-E=0, BRC-E is ignored), Advanced Continuous Read (BUF=0, ECC-E=1, ACR-E=1, BRC-E is ignored) and Sequential Read (BUF=0, ECC-E=0, ACR-E is ignored, BRC-E is ignored) don't require the starting Column Address. The device will always start outputting the data from the first column (Byte 0) of the Data buffer, and once the end of the data buffer is reached, the data output will continue through the next memory page. With the Continuous Read and Sequential Read, it is possible to read out the entire memory array using a single read instruction. Please refer to the respective instruction descriptions for the dummy cycle requirements for each read instructions under different read modes.

- W25NxxLVxxxG: The default setting after power-on is BUF=1, ECC-E=1, ACR-E=0 and BRC-E=0, Buffer Read. It can be switched to Continuous Read and Advanced Continuous Read by writing 0 to the BUF bit and the ACR-R bit. ECC-E is forced to 1 and BRC-E is ignored when BUF=0.

- W25NxxLVxxxT: The default setting after power-on is BUF=0, ECC-E=1, ACR-E=0 (ignored) and BRC-E=0 (ignored), Continuous Read. It can be switched to Buffer Read, Buffer Read with Cache or Advanced Continuous Read by writing 1 to the BUF bit and the ACR-E bit. ECC-E and BRC-E can be set to 1 or 0 when BUF=1. ACR-E can be set to 1 or 0 when BUF=0.

- W25NxxLVxxxE: The default setting after power-on is BUF=1, ECC-E=0 and BRC-E=0, Buffer Read. It can be switched to Sequential Read by writing 0 to the BUF bit. ECC-E is forced to 0 and BRC-E is ignored when BUF=0.

- W25NxxLVxxxU: The default setting after power-on is BUF=0, ECC-E=0 and BRC-E=0 (ignored), Sequential Read. It can be switched to Buffer Read or Buffer Read with Cache by writing 1 to the BUF bit. ECC-E and BRC-E can be set to 1 or 0 when BUF=1.

- W25NxxLVxxxR: The default setting after power-on is BUF=1, ECC-E=1 and BRC-E=0, Buffer Read. The value of BUF bit is fixed as 1. BUF bit cannot be written to 0.

BUF	ECC-E	ACR-E	BRC-E	Read Mode	Data Output Structure	Available Part Numbers
1	0	Ignored	0	Buffer Read	2,048 + 128	W25N02LVxxxG W25N02LVxxxT W25N02LVxxxE W25N02LVxxxU W25N02LVxxxR
1	1	Ignored	0	Buffer Read	2,048 + 64	
1	0	Ignored	1	Buffer Read with Cache	2,048 + 128	
1	1	Ignored	1	Buffer Read with Cache	2,048 + 64	
0	Forced 0	Ignored	Ignored	Sequential Read	2,048 + 128	W25N02LVxxxE W25N02LVxxxU
0	Forced 1	0	Ignored	Continuous Read	2,048	W25N02LVxxxG W25N02LVxxxT
0	Forced 1	1	Ignored	Advanced Continuous Read	2,048	

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7.2.6 Enable Advanced Continuous Read (ACR-E) – *Volatile Writable*

Continuous Read is terminated by /CS=H, but in Advanced Continuous Read, Continuous Read can be temporarily paused by /CS=H. When BUF=0, ACR-E can be set to 1 or 0, and when BUF=1, ACR-E is ignored. When ACR-E=0 (factory default), Continuous Read is enabled. When ACR-E=1, Advanced Continuous Read is enabled.

In the Advanced Continuous Read:

- First read starts from always byte 0.
- /CS de-assert to pause Advanced Continuous Read can only be on byte boundaries. If /CS is de-asserted at other than byte boundary, the data output after Resume is not guaranteed to be correct.
- If Advanced Continuous Read is paused after outputting byte n, only output from byte n+1 is possible when resumed.
- The same Read command must be inputted before and after Pause and Resume.
- To terminate Advanced Continuous Read, execute HWRESET or Terminate Advanced Continuous Read command (F0h) or SWRESET. Anything other than Terminate Advanced Continuous Read (F0h) command will be ignored (Read SR is also ignored).
- The busy time after inputting Terminate Advanced Continuous Read (F0h) command and terminate Advanced Continuous Read is tRDCR (just same as when terminate Continuous Read).
- The busy time after executing Hardware RESET and terminate Advanced Continuous Read is tVSL + tPUW.
- The busy time after executing Software RESET and terminate Advanced Continuous Read is tRST.
- ACR-E will not reset to 0 when terminate Advanced Continuous Read by Terminate Advanced Continuous Read (F0h) command and Software RESET.
- ACR-E will reset to 0 when terminate Advanced Continuous Read by Hardware RESET.

Notes:

1. When SPI bus operation is Mode 3 (1, 1) and DTR, Advanced Continuous Read is not supported.
2. There is no function to temporarily pause Sequential Read by /CS=H.

7.2.7 Enable Buffer Read with Cache (BRC-E) – *Volatile Writable*

When BRC-E=1, the max value of the busy time tRD1 or tRD2 due to Page Data Read (13h) command is shortened to tRD1_BRC or tRD2_BRC by enabling Cache Register. The command sequence is the same as the Buffer Read Mode. When BUF=1, BRC-E can be set to 1 or 0. When BUF=0, BRC-E is ignored. When BRC-E=0 (factory default), Buffer Read with Cache is disabled.

To obtain the effect of shortening tRD1 or tRD2, the Page Address PA[23:0] input to Page Data Read (13h) command must be in sequential order. For example, first execute the Page Data Read (13h) command for Page N, next execute the Page Data Read (13h) command for Page N+1.

For all Read operations in the Buffer Read with Cache, once the /CS signal is brought high to terminate the read operation, the device will still remain busy for tRDBRC (BUSY=1). During this period, the Read Status Register instruction can still be used to check the BUSY bit status. The BUSY bit remains at 1 during tRDBRC and changes to 0 when the cycle is completed, indicating that the device is ready to accept other instructions. If /CS is brought high immediately after reading approximately one page of data, tRDBRC will be at its minimum value. However, if /CS is brought high immediately after reading several bytes of data, tRDBRC will reach its maximum value.

7.2.8 Hold Disable (H-DIS) – *Volatile Writable*

When the Hold Disable (H-DIS) bit is set to 1 (factory default), the hold function will be disabled. If the user wants to use the hold function, the H-DIS bit has to be set 0.

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7.3 Status Register-3 (Volatile Writable and Status Only, Address Cxh)

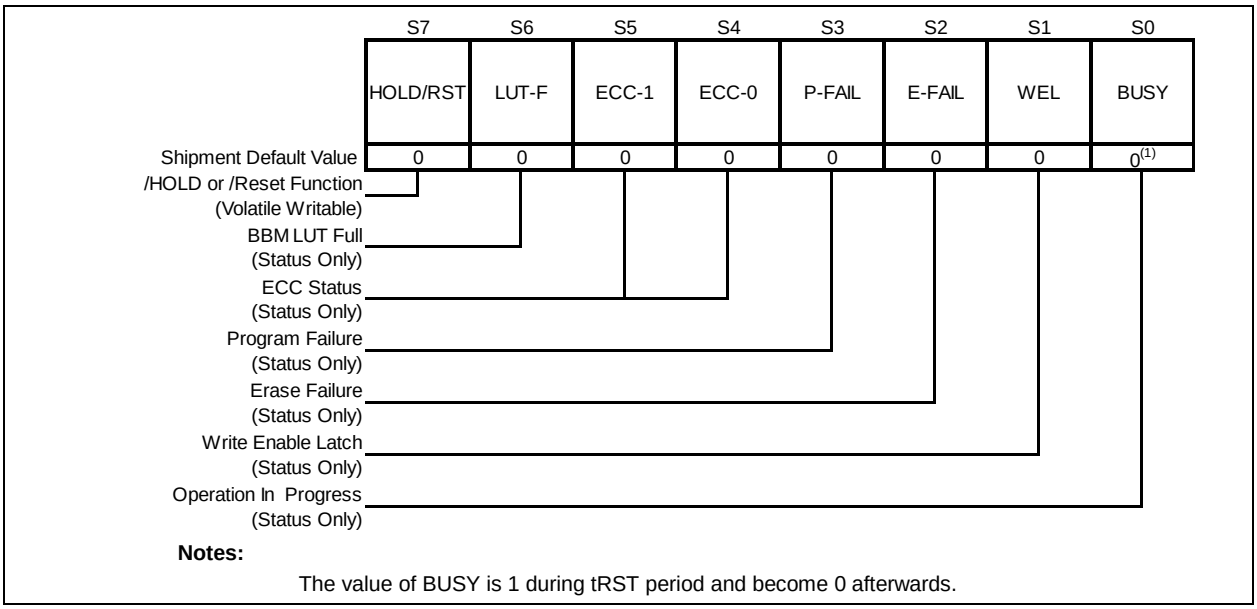


Figure 7-4 Status Register-3 (Address Cxh)

7.3.1 /HOLD or /RESET Function (HOLD/RST)

The HOLD/RST bit is only available in the WSON package and is used in conjunction with the H-DIS bit to determine the function assigned to hardware pin number 7. The factory default value of HOLD/RST bit is 0. /HOLD or /RESET functions are only available when H-DIS bit in the Status Register-2 is 0. If H-DIS bit is set to 1, the /HOLD and /RESET functions are disabled, the pin acts as IO3.

HOLD/RST	H-DIS	DTR operation	Pin Function
0	0	Disable	**/HOLD**
0	0	Enable	**IO3**
0	1	Disable	**IO3**
0	1	Enable	**IO3**
1	0	Disable	**/RESET**
1	0	Enable	**/RESET**
1	1	Disable	**IO3**
1	1	Enable	**IO3**

Notes:
1. The shipment default value of HOLD/RST is 0.
2. The shipment default value of H-DIS is 1.

7.3.2 Look-Up Table Full (LUT-F) – *Status Only*

To facilitate the NAND flash memory bad block management, the W25NxxLV is equipped with an internal Bad Block Management Look-Up-Table (BBM LUT). Up to 40 bad memory blocks may be replaced by a good memory block respectively. The addresses of the bad blocks are stored in the internal Look-Up Table as Logical Block Address (LBA, the bad block) & Physical Block Address (PBA, the good block). The LUT-F bit indicates whether the 40 memory block links have been fully utilized or not. The default value of LUT-F is 0. Once all 40 links are used, LUT-F will become 1, and no more memory block links may be established.

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7.3.3 Cumulative ECC Status (ECC-1, ECC-0) – *Status Only*

The ECC function is used in NAND flash memory to correct limited memory errors during read operations. The ECC Status Bits (ECC-1, ECC-0) should be checked after the completion of a Read operation to verify the data integrity. The ECC Status bits values are don't care if ECC-E=0. These bits will be cleared to 0 after a power cycle, a RESET instruction, or a Page Data Read instruction.

ECC Status		Descriptions
ECC-1	ECC-0	
0	0	No bit flips were detected after reading either single or multiple pages.
0	1	Bit flips were detected and corrected after reading either single or multiple pages. Bit flip count did not exceed the bit flip detection threshold (1).
1	0	After reading either single or multiple pages, multiple bit flips were detected and not corrected.
1	1	After reading either single or multiple pages, bit flips were detected and corrected. Bit flip count exceeded the bit flip detection threshold (1).

Notes:

1. The threshold is set by BFD bits in address 1xh in the Extended Internal ECC Setting Registers.

7.3.4 Program Failure (P-FAIL) – *Status Only*

The Program Failure (P-FAIL) is used to indicate whether the internally controlled Program operation was executed successfully (P-FAIL=0) or timed out (P-FAIL=1). The P-FAIL bit is also set when the Program instruction is issued to a locked or protected memory array or OTP area. This bit is cleared at the beginning of the Program Execute instruction on an unprotected memory array or OTP area. The Device Reset instruction can also clear the P-FAIL bit.

7.3.5 Erase Failure (E-FAIL) – *Status Only*

The Erase Failure (P-FAIL) is used to indicate whether the internally controlled Erase operation was executed successfully (E-FAIL=0) or timed out (E-FAIL=1). The E-FAIL bit is also set when the Erase instruction is issued to a locked or protected memory array. This bit is cleared at the beginning of the Block Erase instruction on an unprotected memory array. The Device Reset instruction can also clear the E-FAIL bit.

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7.3.6 Write Enable Latch (WEL) – *Status Only*

The Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled.

It must be in the write enable state before executing the following instructions:

- Bad Block Management (A1h)
- Built-in ECC Encode Check (A3h)
- Built-in ECC Decode Check (A7h)
- Built-in ECC Diagnostic (ADh)
- Block Erase (D8h)
- Load Program Data (02h)
- Random Load Program Data (84h)
- Quad Load Program Data (32h)
- Quad Random Load Program Data (34h)
- Program Execute (10h)

A Write Disable state occurs upon power-up, Hardware Reset or after any of the following instructions:

- Enable Reset (66h) and Reset Device (99h)
- Device Reset (FFh)
- Write Disable (04h)
- Bad Block Management (A1h)
- Built-in ECC Encode Check (A3h)
- Built-in ECC Decode Check (A7h)
- Built-in ECC Diagnostic (ADh)
- Block Erase (D8h)
- Program Execute (10h)
- Page Data Read (13h)

7.3.7 Read/Erase/Program in Progress (BUSY) – *Status Only*

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is powering up or executing a Page Data Read, Program Execute, Block Erase and Program Execute for OTP area, OTP Locking or after a Continuous / Sequential Read / Buffer Read with Cache instruction. During this time, the device will ignore further instructions except for the Read Status Register, Reset and Read JEDEC ID instructions. When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0-state indicating the device is ready for further instructions.

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7.4 Configuration Register / Status Register-4 (Volatile Writable, Address Dxh)

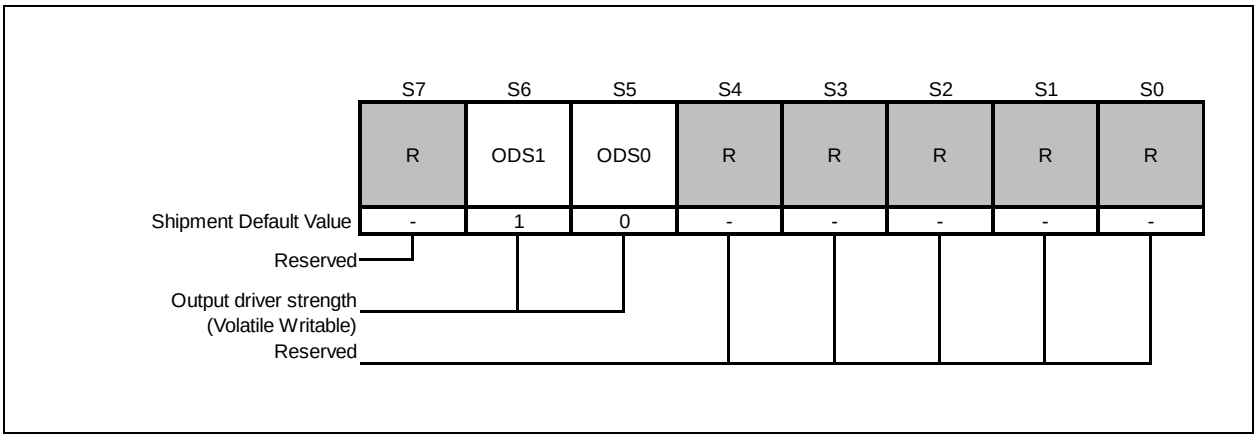


Figure 7-5 Status Register-4 (Address Dxh)

7.4.1 Output Driver Strength (ODS1, ODS0) – *Volatile Writable*

The ODS1 & ODS0 bits are used to determine the output driver strength for Read operations.

ODS1, ODS0	Output Driver Strength
0, 0	25Ω (100%)
0, 1	33Ω (75%)
1, 0	50Ω (50%, Default)
1, 1	100Ω (25%)

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7.5 Configuration Register / Status Register-5 (Status only, Volatile Writable, Address Exh)

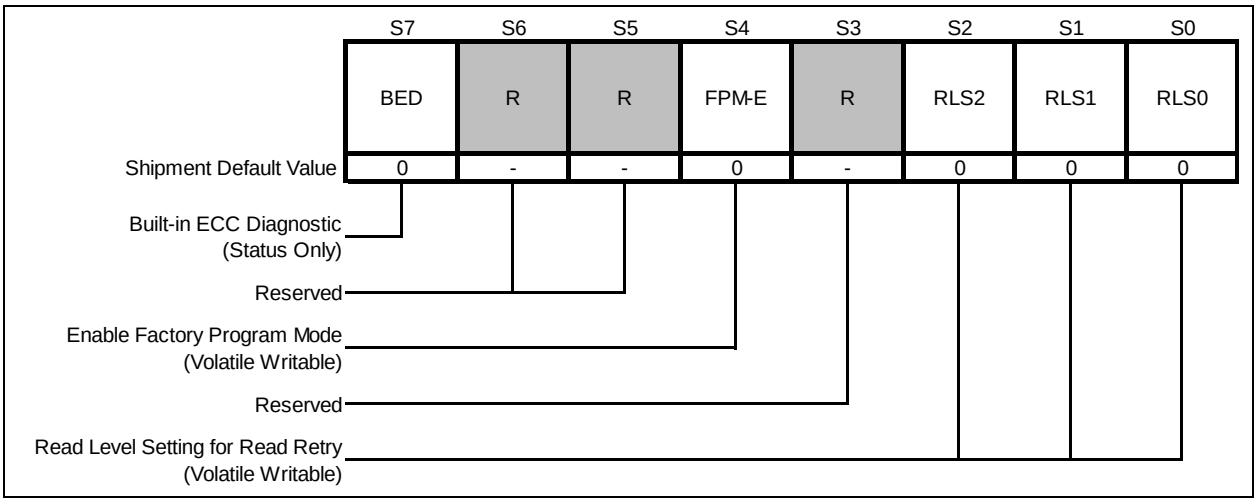


Figure 7-6 Status Register-5 (Address Exh)

7.5.1 Built-in ECC Diagnostic (BED) – *Status Only*

The BED bit is used to indicate the result by Built-in ECC Diagnostic operation whether pass (BED=0) or fail (BED=1).

7.5.2 Enable Factory Program Mode (FPM-E) – *Volatile Writable*

When Factory Program Mode is enabled (FPM-E=1), the page program time is reduced from tPP1 to tPP1_FM (Built-in ECC disabled) or from tPP2 to tPP2_FM (Built-in ECC enabled). This feature is intended for use in factory production environments, where faster programming helps improve manufacturing throughput and efficiency. Please note that while this mode accelerates programming speed, it may impact on the cycling endurance of the Flash array. Therefore, the usage of Factory Program Mode is limited to a maximum of 100 Program/Erase cycles.

7.5.3 Read Level Setting for Read Retry (RLS2, RLS1, RLS0) – *Volatile Writable*

The RLS bits (RLS2, RLS1 and RLS0) are used to determine the Read Level Setting for Read Retry operations. If ECC fails to correct the bit errors, changing the Read Level Setting and reading again (Read Retry) may succeed in correcting the bit errors. In such cases, it is recommended to move the data to a page of another good block.

RLS2	RLS1	RLS0	Read Level
0	0	0	0 (Default)
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Notes:

1. Regarding details about Read Level Setting for Read Retry, please confirm the Application Note “AN0000063: Read Retry feature for QspiNAND”.

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7.6 Extended Internal ECC Setting Registers

This device has the functions of bit error detection and maximum bit flip count report. Internal ECC detects bit errors in each sector and the maximum bit flip count in a page. These results are indicated in the Extended Internal ECC Setting Registers as shown below.

Address	Bits							
	S7	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**
1xh	BFD3	BFD2	BFD1	BFD0	R	R	R	R
2xh	R	R	R	R	BFS3	BFS2	BFS1	BFS0
3xh	MBF3	MBF2	MBF1	MBF0	R	MFS2	MFS1	MFS0
4xh	BFR7	BFR6	BFR5	BFR4	BFR3	BFR2	BFR1	BFR0
5xh	BFR15	BFR14	BFR13	BFR12	BFR11	BFR10	BFR9	BFR8

7.6.1 ECC Bit Flip Count Detection (BFD) – *Volatile Writable*

The ECC Bit Flip Count Detection function detects the bit flip count in a page. The user sets the threshold bit count using the Write Extended Internal ECC Setting Registers instruction. The threshold bit count is decided by the bit flip detection setting bit (BFD) in address 1xh. The detected results will be indicated in the BFS bits (bits [7:0]) in address 2xh. When bit flips exceed the threshold in a sector, the BFS bits are set after the Read instructions other than the Page Data Read (13h) instruction.

BFD3	BFD2	BFD1	BFD0	Description
0	0	0	0	Reserved
0	0	0	1	Detect 1-bit flip in a sector
0	0	1	0	Detect 2-bits flip in a sector
0	0	1	1	Detect 3-bits flip in a sector
0	1	0	0	Detect 4-bits flip in a sector
0	1	0	1	Detect 5-bits flip in a sector
0	1	1	0	Detect 6-bits flip in a sector
0	1	1	1	Detect 7-bits flip in a sector (default)
1	0	0	0	Detect 8-bits flip in a sector
1	1	1	1	Detect over 9-bits flip in a sector

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7.6.2 ECC Bit Flip Count Detection Status (BFS) – *Status Only*

Symbol	Parameter	Status	Description
BFS3	Bit flip count detection status in sector 3	1	Bit flip count in sector 3 is equal to or more than threshold bit count
		0	Bit flip count in sector 3 is less than the threshold
BFS2	Bit flip count detection status in sector 2	1	Bit flip count in sector 2 is equal to or more than threshold bit count
		0	Bit flip count in sector 2 is less than the threshold
BFS1	Bit flip count detection status in sector 1	1	Bit flip count in sector 1 is equal to or more than threshold bit count
		0	Bit flip count in sector 1 is less than the threshold
BFS0	Bit flip count detection status in sector 0	1	Bit flip count in sector 0 is equal to or more than threshold bit count
		0	Bit flip count in sector 0 is less than the threshold

7.6.3 ECC Maximum Bit Flip Count Report (MBF, MFS) – *Status Only*

The ECC Maximum Bit Flip Count Report function provides the maximum bit flip count in a page. The maximum count is indicated in address 3xh. The sector number in which the maximum bit flip occurred in a page is indicated in the MFS bit (bits [2:0]) in address 3xh. When several sector's maximum bit flip count is the same, the lowest sector number is indicated in these bits. When MBF[3:0]=[0,0,0,0], it means no bit error is detected in the page (all sectors) so please ignore the value of MFS[2:0]. The user can get the report using the Read Extended Internal ECC Setting Registers instruction.

MBF3	MBF2	MBF1	MBF0	Description
0	0	0	0	No bit flip in a sector
0	0	0	1	Maximum bit flip count is 1-bit in a sector. Bit flip was corrected.
0	0	1	0	Maximum bit flip count is 2-bits in a sector. Bit flips were corrected
0	0	1	1	Maximum bit flip count is 3-bits in a sector. Bit flips were corrected
0	1	0	0	Maximum bit flip count is 4-bits in a sector. Bit flips were corrected
0	1	0	1	Maximum bit flip count is 5-bits in a sector. Bit flips were corrected
0	1	1	0	Maximum bit flip count is 6-bits in a sector. Bit flips were corrected
0	1	1	1	Maximum bit flip count is 7-bits in a sector. Bit flips were corrected
1	0	0	0	Maximum bit flip count is 8-bits in a sector. Bit flips were corrected
1	1	1	1	Maximum bit flip count exceeds 8-bits in a sector. Bit flips were not corrected

MFS2	MFS1	MFS0	Description
0	0	0	Maximum bit flips occurred in sector 0
0	0	1	Maximum bit flips occurred in sector 1
0	1	0	Maximum bit flips occurred in sector 2
0	1	1	Maximum bit flips occurred in sector 3

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7.6.4 ECC Bit Flip Count Report (BFR) – *Status Only*

The ECC Bit Flip Count Report function reports the bit flip count of each sector in a page. The users can read the bit flip count using the Read Extended Internal ECC Setting Registers instruction with address 4xh and 5xh.

BFR15, 11, 7, 3	BFR14, 10, 6, 2	BFR13, 9, 5, 1	BFR12, 8, 4, 0	Description
0	0	0	0	No bit flip in a sector
0	0	0	1	Detect 1-bit flip in a sector and corrected
0	0	1	0	Detect 2-bits flip in a sector and corrected
0	0	1	1	Detect 3-bits flip in a sector and corrected
0	1	0	0	Detect 4-bits flip in a sector and corrected
0	1	0	1	Detect 5-bits flip in a sector and corrected
0	1	1	0	Detect 6-bits flip in a sector and corrected
0	1	1	1	Detect 7-bits flip in a sector and corrected
1	0	0	0	Detect 8-bits flip in a sector and corrected
1	1	1	1	Detect over 9-bits flip in a sector and were not corrected

BFR set	Parameter
BFR [15:12]	Bit flip count detection report for sector 3
BFR [11:8]	Bit flip count detection report for sector 2
BFR [7:4]	Bit flip count detection report for sector 1
BFR [3:0]	Bit flip count detection report for sector 0

7.7 Reserved Bits – *Non-Functional*

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of these bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effects.

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7.8 Status Register Memory Protection

STATUS REGISTER (1)					W25N02LV (2G-BIT / 256M-BYTES) MEMORY PROTECTION		
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED DENSITY	PROTECTED PORTION
X	0	0	0	0	NONE	NONE	NONE
0	0	0	0	1	2046:2047	256KB	Upper 1/1024 locked
0	0	0	1	0	2044:2047	512KB	Upper 1/512 locked
0	0	0	1	1	2040:2047	1MB	Upper 1/256 locked
0	0	1	0	0	2032:2047	2MB	Upper 1/128 locked
0	0	1	0	1	2016:2047	4MB	Upper 1/64 locked
0	0	1	1	0	1984:2047	8MB	Upper 1/32 locked
0	0	1	1	1	1920:2047	16MB	Upper 1/16 locked
0	1	0	0	0	1792:2047	32MB	Upper 1/8 locked
0	1	0	0	1	1536:2047	64MB	Upper 1/4 locked
0	1	0	1	0	1024:2047	128MB	Upper 1/2 locked
All others					0:2047	All locked	All locked
1	0	0	0	1	0:1	256KB	Lower 1/1024 locked
1	0	0	1	0	0:3	512KB	Lower 1/512 locked
1	0	0	1	1	0:7	1MB	Lower 1/256 locked
1	0	1	0	0	0:15	2MB	Lower 1/128 locked
1	0	1	0	1	0:31	4MB	Lower 1/64 locked
1	0	1	1	0	0:63	8MB	Lower 1/32 locked
1	0	1	1	1	0:127	16MB	Lower 1/16 locked
1	1	0	0	0	0:255	32MB	Lower 1/8 locked
1	1	0	0	1	0:511	64MB	Lower 1/4 locked
1	1	0	1	0	0:1023	128MB	Lower 1/2 locked
1	1	1	1	1	0:2047	All locked (default)	All locked (default)

Notes:

1. X = don't care.
2. If any Erase or Program instruction specifies a memory region that contains a protected data portion, this instruction will be ignored.

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8. INSTRUCTIONS

The Standard/Dual/Quad SPI instruction set of the W25NxxLV is fully controlled through the SPI bus. Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with the most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of /CS. Clock relative timing diagrams for each instruction are included in the Figures of each instruction's description. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the device is performing Program or Erase operation, Page Data Read or OTP locking operations, the BUSY bit will be high, and all instructions except for Read Status Register or Read JEDEC ID will be ignored until the current operation cycle has completed.

8.1 Device ID and Instruction Set Tables

8.1.1 Manufacturer and Device Identification

MANUFACTURER ID	**(MF7 - MF0)**
Winbond Serial Flash	EFh
Device ID	**(ID15 - ID0)**
W25N02LV	8A22h

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8.1.2 Instruction Set Table

Instruction	Command Op code	Command-Address-Data			Address Input Cycles [2]	Dummy Cycles		Data Output Cycles [3]
		Single SPI	Dual SPI	Quad SPI		BUF=1	BUF=0	
Software Reset Operations								
Enable Reset	66h	1-0-0	-	-	-	-		-
Reset Device	99h	1-0-0	-	-	-	-		-
Device Reset	FFh	1-0-0	-	-	-	-		-
Read ID Operations								
Read JEDEC ID	9Fh	1-0-1	-	-	-	8		1 to 24
Read / Write Register Operations								
Read Status Register [7]	0Fh/05h	1-1-1	-	-	8	0		1 to ∞
Read Extended Internal ECC Setting Register [7]	0Fh/05h	1-1-1	-	-	8	0		1 to ∞
Write Status Register [7]	1Fh/01h	1-1-1	-	-	8	0		-
Write Extended Internal ECC Setting Register [7]	1Fh/01h	1-1-1	-	-	8	0		-
Pre-Write Setup Operations								
Write Enable	06h	1-0-0	-	-	-	-		-
Write Disable	04h	1-0-0	-	-	-	-		-
Winbond Original Operations								
Bad Block Management (Swap Blocks)	A1h	1-1-0	-	-	32	-		-
Read BBM LUT	A5h	1-0-1	-	-	-	8		1 to 1,280
Last ECC Failure Page Address	A9h	1-0-1	-	-	-	8		24
Built-in ECC Encode Check	A3h	1-1-0	-	-	24	-		-
Built-in ECC Decode Check	A7h	1-1-0	-	-	24	-		-
Built-in ECC Diagnostic	ADh	1-1-0	-	-	24	-		-
Deep Power-down Operations								
Deep Power-down	B9h	1-0-0	-	-	-	-		-
Release Deep Power-down	ABh	1-0-0	-	-	-	-		-
Block Erase Operation								
Block Erase	D8h	1-1-0	-	-	24	-		-
Program Operations								
Load Program Data	02h	1-1-1	-	-	16	-		-
Random Load Program Data	84h	1-1-1	-	-	16	-		-
Quad Load Program Data	32h	-	-	1-1-4	16	-		-
Quad Random Load Program Data	34h	-	-	1-1-4	16	-		-
Program Execute	10h	1-1-0	-	-	24	-		-
Page Read Operation								
Page Data Read	13h	1-1-0	-	-	24	-		-
Read Data Operations						BUF=1	BUF=0	
Read Data	03h	1-1-1	-	-	16	8	24	1 to ∞
Fast Read	0Bh	1-1-1	-	-	16	8	32	1 to ∞
Fast Read Dual Output	3Bh	-	1-1-2	-	16	8	32	1 to ∞
Fast Read Quad Output	6Bh	-	-	1-1-4	16	8	32	1 to ∞
Fast Read Dual I/O	BBh	-	1-2-2	-	8	4	16	1 to ∞
Fast Read Quad I/O	EBh	-	-	1-4-4	4	4	12	1 to ∞
DTR Fast Read	0Dh	1-1d-1d	-	-	8	8	18	1 to ∞
DTR Fast Read Quad Output	6Dh	-	-	1-1d-4d	8	8	20	1 to ∞
DTR Fast Read Quad I/O	EDh	-	-	1-4d-4d	2	8	11	1 to ∞

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Notes:

1. C-A-D format: "C" stands for Command input; "A" stands for Address input; "D" stands for either Data input or Output.

2. Continuous Read Mode and Sequential Read Mode ignore the address input.

3. For all Read Data operations, Data Cycles in Continuous Read Mode and Sequential Read Mode have no limitation. Data Cycles in Buffer Read Mode is up to the page size.

4. Column Address (CA) only requires CA[11:0], CA[15:12] are considered as dummy bits.

5. Page Address (PA) requires 17 bits. PA[16:6] is the address for 128KB blocks (total 2,048 blocks), PA[5:0] is the address for 2KB pages (total 64 pages for each block).

6. Logical and Physical Block Address (LBA & PBA) each consists of 16 bits. LBA[10:0] & PBA[10:0] are effective Block Addresses. LBA[15:14] is used for additional information.

7. Register Addresses:

Status Register-1 / Protection Register:	Address = Axh
Status Register-2 / Configuration Register:	Address = Bxh
Status Register-3 / Status Register:	Address = Cxh
Status Register-4 / Configuration Register:	Address = Dxh
Status Register-5 / Configuration Register:	Address = Exh
Extended Internal ECC Setting Registers:	Address = 1xh, 2xh, 3xh, 4xh, 5xh, 6xh, 7xh

8. Dual SPI Address Input (**CA15-8** and **CA7-0**) format:

IO0 =	x,	CA12,	CA10,	CA8,	CA6,	CA4,	CA2,	CA0
IO1 =	x,	x,	CA11,	CA9,	CA7,	CA5,	CA3,	CA1

9. Dual SPI Data Output (***D7-0***) format:

IO0 =	D6,	D4,	D2,	D0,	……
IO1 =	D7,	D5,	D3,	D1,	……

10. Quad SPI Address Input (**CA15-8** and **CA7-0**) format:

IO0 =	CA12,	CA8,	CA4,	CA0
IO1 =	x,	CA9,	CA5,	CA1
IO2 =	x,	CA10,	CA6,	CA2
IO3 =	x,	CA11,	CA7,	CA3

11. Quad SPI Data Input/Output (***D7-0***) format:

IO0 =	D4,	D0,	……	
IO1 =	D5,	D1,	……	
IO2 =	D6,	D2,	……	
IO3 =	D7,	D3,	……	

12. All Quad Program/Read instructions are disabled when WP-E bit is set to 1 in the Protection Register.

13. For all Read operations in the Continuous Read Mode, once the /CS signal is brought high to terminate the read operation, the device will still remain busy for tRDCR (BUSY=1), and all the data inside the Data buffer will be lost and un-reliable to use. A new Page Data Read instruction must be issued to reload the correct page data into the Data Buffer.

14. For all Read operations in the Sequential Read Mode, once the /CS signal is brought high to terminate the read operation, the device will still remain busy for tRDSR (BUSY=1), and all the data inside the Data buffer will be lost and un-reliable to use. A new Page Data Read instruction must be issued to reload the correct page data into the Data Buffer.

15. For all Read operations in the Buffer Read Mode, as soon as /CS signal is brought high to terminate the read operation, the device will be ready to accept new instructions and all the data inside the Data Buffer will remain unchanged from the previous Page Data Read instruction.

16. For all Read operations in the Buffer Read with Cache, once the /CS signal is brought high to terminate the read operation, the device will still remain busy for tRDBRC (BUSY=1), and all the data inside the Data buffer will be lost and un-reliable to use. A new Page Data Read instruction must be issued to reload the correct page data into the Data Buffer.

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8.2 Instruction Descriptions

8.2.1 Device Reset (FFh), Enable Reset (66h) and Reset Device (99h)

Once the Reset instruction is accepted, any on-going internal operations will be terminated and will take approximately tRST to reset. Depending on the current operation the device is performing, tRST can be 5us~500us. During this period, no instruction will be accepted. After the execution of the Reset instruction is completed, each bit of the Status Register will follow the following table.

If there is an on-going internal Erase or Program operation when the Reset instruction sequence is accepted by the device, data corruption may happen at only the address that is the target of the on-going operation. It is recommended to check the BUSY bit in the Status Register before issuing the Reset instruction.

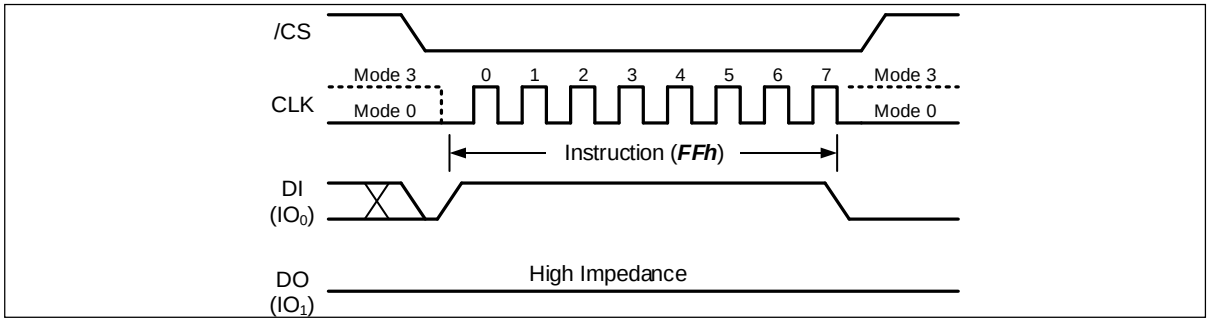


Figure 8-1 Device Reset Instruction (FFh)

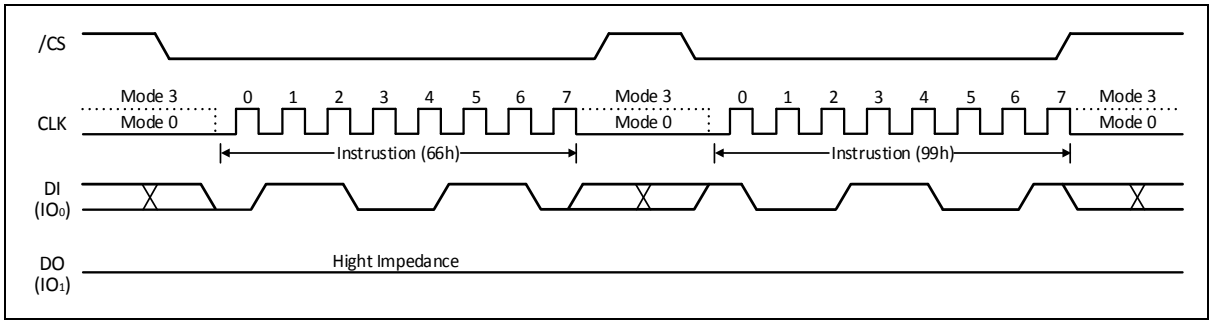


Figure 8-2 Device Reset Instruction (66h+99h)

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Register	Address	Bits		Shipment Default Value	Default Value after Power-up with LUT full	Default Value after Power-up with OTP locked	Default Value after Power-up with SR-1 locked	Default Value after Power-up with OTP locked and SR-1 locked	After Reset command (FFh)	After Reset command (66h+99h) or Reset by /RESET pin or Reset by Reset Protocol or Release Deep Power-down (ABh)
Status Register-1	Axh	S7	SRP0	0	0	0	1 (locked)	1 (locked)	No Change	0
		S6	BP3	1	1	1	x (locked)	x (locked)	No Change	1
		S5	BP2	1	1	1	x (locked)	x (locked)	No Change	1
		S4	BP1	1	1	1	x (locked)	x (locked)	No Change	1
		S3	BP0	1	1	1	x (locked)	x (locked)	No Change	1
		S2	TB	1	1	1	x (locked)	x (locked)	No Change	1
		S1	WP-E	0	0	0	x (locked)	x (locked)	No Change	0
		S0	SRP1	0	0	0	1 (locked)	1 (locked)	No Change	0
Status Register-2	Bxh	S7	OTP-L	0	0	1	0	1	Clear to 0 befor OTP set	Clear to 0 before OTP set
		S6	OTP-E	0	0	0	0	0	0	0
		S5	SR1-L	0	0	0	1	1	Clear to 0 befor OTP set	Clear to 0 before OTP set
		S4	ECC-E W25NxxLVxxxG/T/R	1	1	1	1	1	No Change	1
			ECC-E W25NxxLVxxxE/U	0	0	0	0	0	No Change	0
		S3	BUF W25NxxLVxxxG/E/R	1	1	1	1	1	No Change	1
			BUF W25NxxLVxxxT/U	0	0	0	0	0	No Change	0
		S2	ACR-E	0	0	0	0	0	No Change	0
		S1	BRC-E	0	0	0	0	0	No Change	0
		S0	H-DIS	1	1	1	1	1	No Change	1
Status Register-3	Cxh	S7	HOLD/RST	0	0	0	0	0	No Change	0
		S6	LUT-F	0	1	0	0	0	No Change	0 (1)
		S5	ECC-1	0	0	0	0	0	0	0
		S4	ECC-0	0	0	0	0	0	0	0
		S3	P-FAIL	0	0	0	0	0	0	0
		S2	E-FAIL	0	0	0	0	0	0	0
		S1	WEL	0	0	0	0	0	0	0
		S0	BUSY	0	0	0	0	0	0	0
Status Register-4	Dxh	S7	Reserved	-	-	-	-	-	-	-
		S6	ODS1	1	1	1	1	1	No Change	1
		S5	ODS0	0	0	0	0	0	No Change	0
		S4	Reserved	-	-	-	-	-	-	-
		S3	Reserved	-	-	-	-	-	-	-
		S2	Reserved	-	-	-	-	-	-	-
		S1	Reserved	-	-	-	-	-	-	-
		S0	Reserved	-	-	-	-	-	-	-
Status Register-5	Exh	S7	BED	0	0	0	0	0	0	0
		S6	Reserved	-	-	-	-	-	-	-
		S5	Reserved	-	-	-	-	-	-	-
		S4	FPM-E	0	0	0	0	0	No Change	0
		S3	Reserved	-	-	-	-	-	-	-
		S2	RLS2	0	0	0	0	0	No Change	0
		S1	RLS1	0	0	0	0	0	No Change	0
		S0	RLS0	0	0	0	0	0	No Change	0
Extended Internal ECC Setting Registers	1xh	S7	BFD3	0	0	0	0	0	No Change	0
		S6	BFD2	1	1	1	1	1	No Change	1
		S5	BFD1	1	1	1	1	1	No Change	1
		S4	BFD0	1	1	1	1	1	No Change	1
		S3	Reserved	-	-	-	-	-	-	-
		S2	Reserved	-	-	-	-	-	-	-
		S1	Reserved	-	-	-	-	-	-	-
		S0	Reserved	-	-	-	-	-	-	-
	2xh	S7	Reserved	-	-	-	-	-	-	-
		S6	Reserved	-	-	-	-	-	-	-
		S5	Reserved	-	-	-	-	-	-	-
		S4	Reserved	-	-	-	-	-	-	-
		S3	BFS3	0	0	0	0	0	0	0
		S2	BFS2	0	0	0	0	0	0	0
		S1	BFS1	0	0	0	0	0	0	0
		S0	BFS0	0	0	0	0	0	0	0
	3xh	S7	MBF3	0	0	0	0	0	0	0
		S6	MBF2	0	0	0	0	0	0	0
		S5	MBF1	0	0	0	0	0	0	0
		S4	MBF0	0	0	0	0	0	0	0
		S3	Reserved	-	-	-	-	-	-	-
		S2	MFS2	0	0	0	0	0	0	0
		S1	MFS1	0	0	0	0	0	0	0
		S0	MFS0	0	0	0	0	0	0	0
	4xh~5xh	S7	BFR7, 15	0	0	0	0	0	0	0
		S6	BFR6, 14	0	0	0	0	0	0	0
		S5	BFR5, 13	0	0	0	0	0	0	0
		S4	BFR4, 12	0	0	0	0	0	0	0
		S3	BFR3, 11	0	0	0	0	0	0	0
		S2	BFR2, 10	0	0	0	0	0	0	0
		S1	BFR1, 9	0	0	0	0	0	0	0
		S0	BFR0, 8	0	0	0	0	0	0	0

Default values of the Status Registers after power-up and Device Reset

Notes:

1. If LUT is full, the bit indicates to "1" after Reset instruction (66h+99h) and HW RESET.

	During Power Up Sequence or Release Deep Power-down (ABh) or Hardware Reset	After Reset command (FFh)	After Reset command (66h+99h)
Auto Page Data Read (1)	Execute	Not execute	Not execute

Auto Page Data Read execution during power up and after Reset

Notes:

1. Automatic execution of Page Data Read (13h) instruction for Page 0 of Block0.

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Email:sales@manduic.com

8.2.2 Read JEDEC ID (9Fh)

The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh” followed by 8 dummy clocks.

The JEDEC assigned Manufacturer ID byte for Winbond (EFh) and two Device ID bytes are then shifted out on the falling edge of CLK with most significant bit (MSB) first. For memory type and capacity values refer to the Manufacturer and Device Identification table.

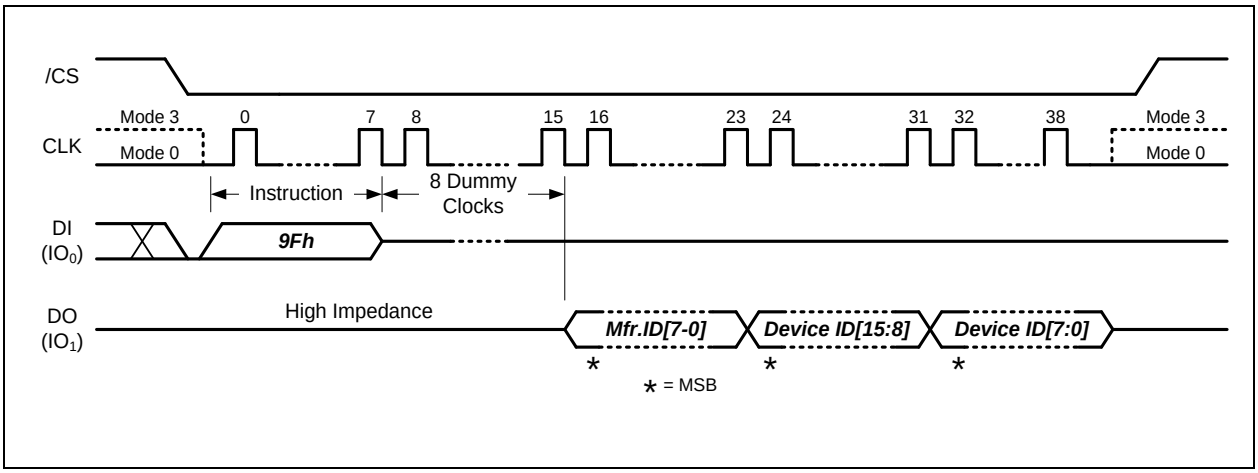


Figure 8-3 Read JEDEC ID Instruction

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8.2.3 Read Status Register (0Fh / 05h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code “0Fh or 05h” into the DI pin on the rising edge of CLK followed by 8 Status Register Address bits. The status register bits are then shifted out on the DO pin on the falling edge of CLK with the most significant bit (MSB) first. Refer to section 7 for Status Register descriptions.

The read status register instruction can be used, even while a Program or Erase cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously. The instruction is completed by driving /CS high.

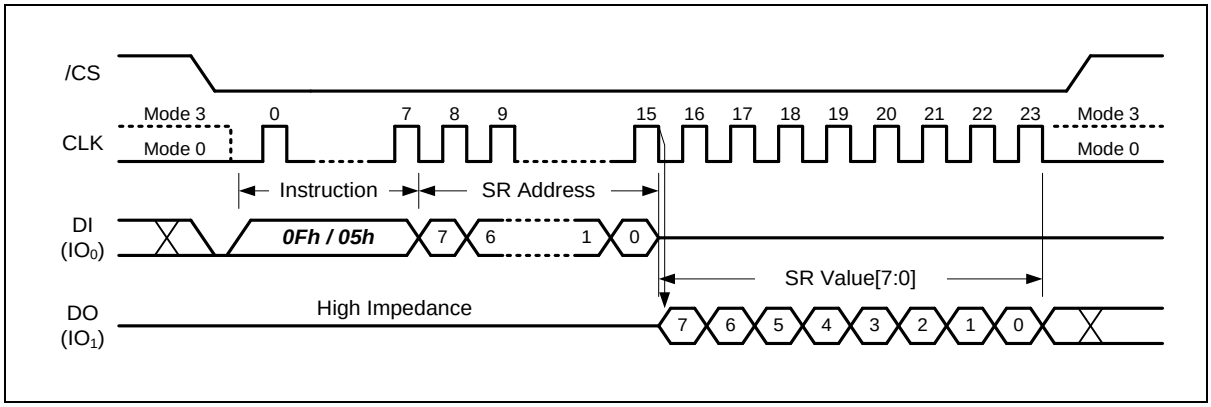


Figure 8-4 Read Status Register Instruction

8.2.4 Write Status Register (1Fh / 01h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include SRP[1:0], TB, BP[3:0] and WP-E bit in Status Register-1; OTP-L, OTP-E, SR1-L and BUF bits in Status Register-2. All other Status Register bit’s locations are read-only and will not be affected by the Write Status Register instruction.

To write the Status Register bits, the instruction is entered by driving /CS low, sending the instruction code “1Fh or 01h”, followed by 8 Status Register Address bits, and then writing the status register data byte. Refer to section 7 for Status Register descriptions. After power-up, the factory defaults for BP[3:0], TB bits are 1, while for the other bits are 0.

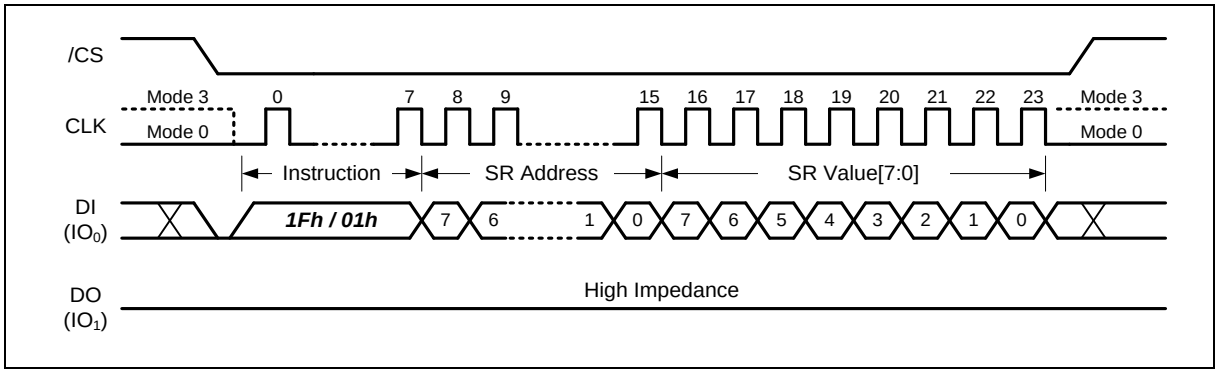


Figure 8-5 Write Status Register Instruction

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8.2.5 Write Enable (06h)

The Write Enable instruction sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program and Block Erase instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

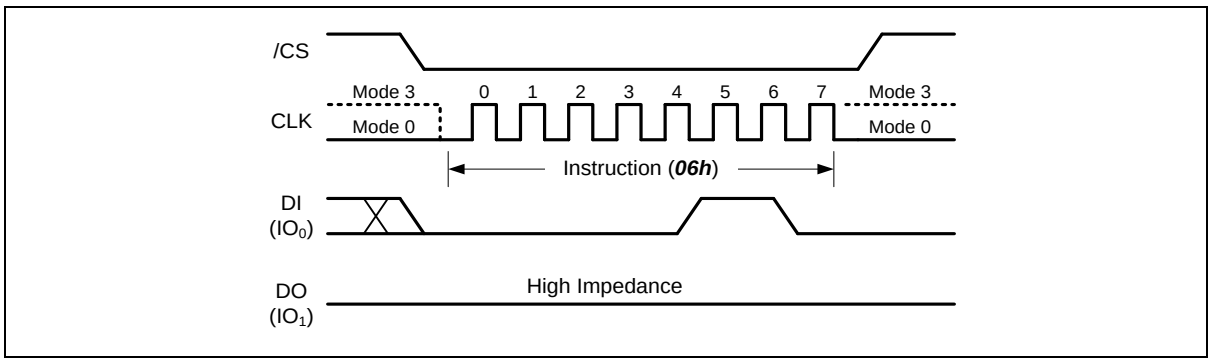


Figure 8-6 Write Enable Instruction

8.2.6 Write Disable (04h)

The Write Disable instruction resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Program Execute, Block Erase, Page Data Read and Program Execute for OTP pages.

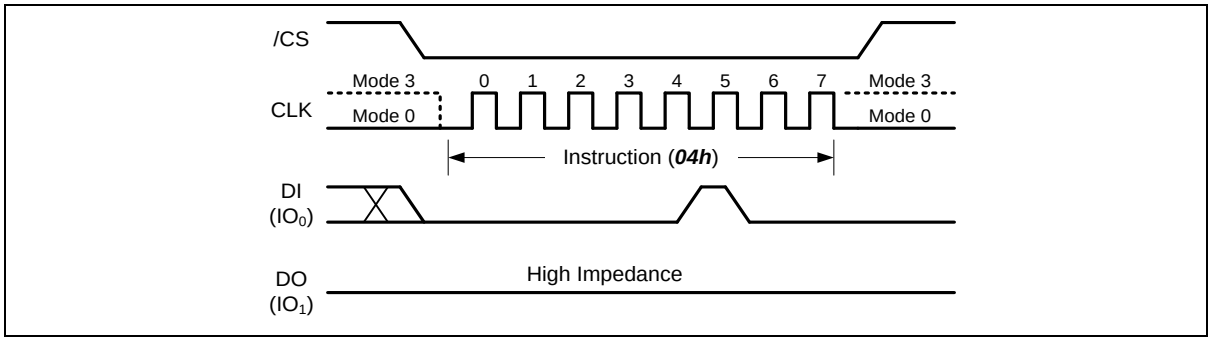


Figure 8-7 Write Disable Instruction

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8.2.7 Bad Block Management (A1h)

Due to the large NAND memory density size and technology limitations, NAND memory devices are allowed to be shipped to the end customers with a certain amount of “Bad Blocks” found during the factory testing. Up to 2% of the memory blocks can be marked as “Bad Blocks” upon shipment, which is a maximum of 40 blocks per die. To identify these bad blocks, it is recommended to scan the entire memory array for bad block markers set in the factory. A “Bad Block Marker” is a non-FFh data byte stored at Byte 0 of Page 0 for each bad block. An additional marker is also stored in the first byte of the 128-Bytes spare area.

The W25NxxLV offers a convenient method to manage the bad blocks typically found in NAND flash memory after extensive use. The “Bad Block Management” instruction is initiated by shifting the instruction code “A1h” into the DI pin followed by 16 “Logical Block Address” bits and 16 “Physical Block Address” bits. The logical block address is the address for the “bad” block that will be replaced by the “good” block indicated by the physical block address.

A Write Enable instruction must be executed before the device will accept the Bad Block Management instruction (Status Register bit WEL=1). The Bad Block Management instruction is initiated by driving the /CS pin low and shifting the instruction code “A1h” followed by 16 LBA (Bad Block address) bits and 16 PBA (Good Block address) bits. After /CS is driven high to complete the instruction cycle, the self-timed Bad Block Management instruction will commence for a time duration of tPP1 (See AC Characteristics). While the Bad Block Management cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Bad Block Management cycle and becomes a 0 when the cycle is finished, and the device is ready to accept other instructions again. After the Bad Block Management cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

Once a Bad Block Management instruction is successfully executed, the specified LBA-PBA link will be added to the internal Look Up Table (LUT). Up to 40 links can be established in the non-volatile LUT. If all 40 links have been written, the LUT-F bit in the Status Register will become a 1, and no more LBA-PBA links can be established. Therefore, prior to issuing the Bad Block Management instruction, the LUT-F bit value should be checked or a “Read BBM Look Up Table” instruction can be issued to confirm if any spare links are still available in the LUT.

To guarantee a Continuous / Sequential Read Mode on the blocks, the manufacturer may have used some of the BBM LUT entrees. It is advisable for the user to scan all blocks and keep a table of all manufacturer bad blocks prior to the first erase/program operation.

Registering the same address in multiple PBAs is prohibited. It may cause unexpected behavior.

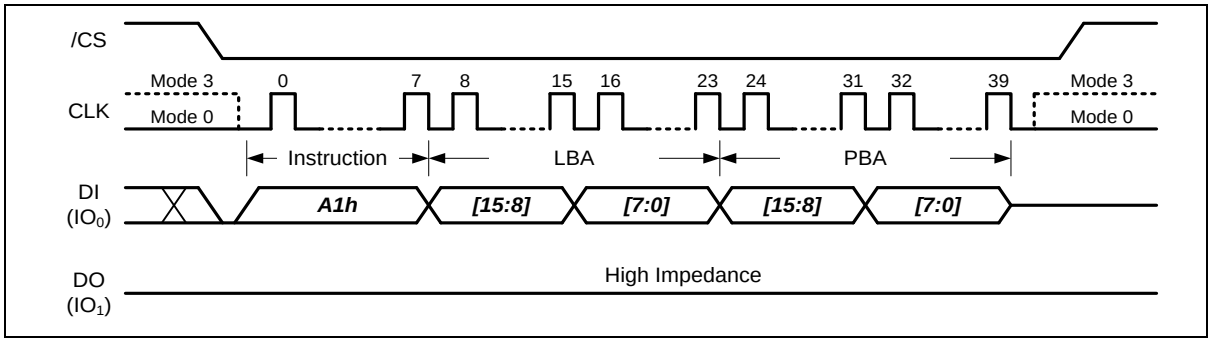


Figure 8-8 Bad Block Management Instruction

Notes:

1. Regarding details about BBM LUT, please confirm the Application Note “AN0000083: Winbond SPI NAND Pre-Applied BBM LUT”.

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8.2.8 Read BBM Look Up Table (A5h)

The internal Look Up Table (LUT) consists of 40 Logical-Physical memory block links (from LBA0/PBA0 to LBA39/PBA39) per die. The “Read BBM Look Up Table” instruction can be used to check the existing address links stored inside the LUT.

The “Read BBM Look Up Table” instruction is initiated by shifting the instruction code “A5h” into the DI pin followed by 8 dummy clocks. At the falling edge of the 16th clock, the device will start to output 16 “Logical Block Address” bits, and 16 “Physical Block Address” bits as illustrated in Figure 8-10. All block address links will be output sequentially starting from the first link (LBA0 & PBA0) in the LUT. If there are available links that are unused, the output will contain all “00h” data.

The MSB bits LBA[15:14] of each link are used to indicate the status of the link.

LBA[15] (Enable)	LBA[14] (Invalid)	Descriptions
0	0	This link is available to use.
1	0	This link is enabled, and it is a valid link.
1	1	This link was enabled, but it is not valid anymore.
0	1	Not applicable.

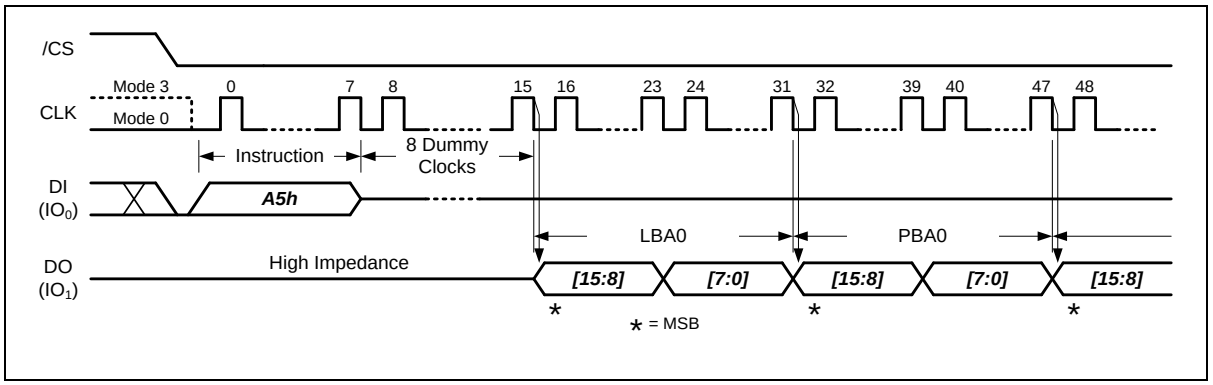


Figure 8-9 Read BBM Look Up Table Instruction

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8.2.9 Last ECC Failure Page Address (A9h)

When the ECC-E bit in the Status/Configuration Register is set to 1 (also power up default), the internal ECC algorithm is enabled for all Program and Read operations. During a “Program Execute” instruction for a specific page, the ECC algorithm will calculate the ECC information based on the data inside the data buffer and write the ECC data into the spare area in the same physical memory page.

During Read operations, ECC information will be used to verify the data read out from the physical memory array and possible corrections can be made to the limited amount of data bits that contain errors. The ECC Status Bits (ECC-1 & ECC-0) will also be set, indicating the result of the ECC calculation.

For the Continuous Read Mode, multiple pages of main array data can be read out continuously by issuing a single read instruction. Upon finishing the read operation, the ECC status bits should be checked to verify if there’s any ECC correction or if un-correctable errors existed in the data read out. If ECC-1 & ECC-0 equal to (1, 0) or (1, 1), the previous data read out contains one or more pages that contain ECC un-correctable errors.

The failure page address (or the last page address if it’s multiple pages) can be obtained by issuing the “Last ECC failure Page Address” instruction. The 24 Page Address bits that contain un-correctable ECC errors will be presented on the DO pin following the instruction code “A9h” and 8 dummy clocks on the DI pin.

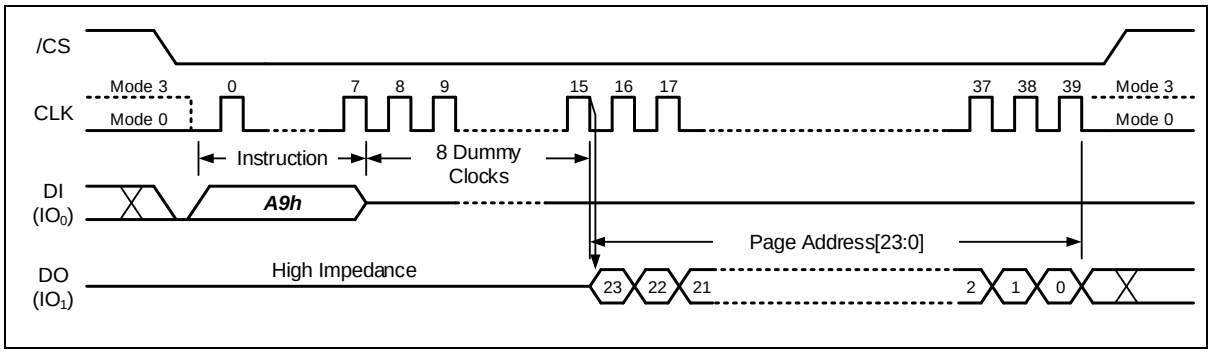


Figure 8-10 Last ECC Failure Page Address Instruction

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8.2.10 Built-in ECC Encode Check (A3h)

Built-in ECC operation can be checked by combining the Built-in ECC Encode Check (A3h), Load Program Data instruction (02h), Page Data Read (13h), and Built-in ECC Decode Check (A7h) instructions. It works using Built-in ECC and Data Buffer without giving the actual Program and Erase operations to the memory cells.

By executing the instructions in the following procedure, it is possible to check the ECC encode processing by Built-in ECC based on arbitrary data. As a result, the ECC Parity Data can be output.

1. Set BUF bit in the Status Register equal 1 and set ECC-E bit in the Status Register equal 0
2. Execute Write Enable (06h) instruction to set WEL bit in the Status Register equal 1
3. Input arbitrary data to the Data Buffer with the Load Program Data (02h) instruction
4. Execute the Built-in ECC Encode Check (A3h) instruction
5. Wait busy time tRDEPC
6. Execute any Read instructions (03h, 0Bh, 3Bh, 6Bh, BBh, EBh, 0Dh, 6Dh, EDh) with Column Address is don't care

A Write Enable instruction must be executed before the device will accept the Built-in ECC Encode Check instruction (Status Register bit WEL must equal 1). The Built-in ECC Encode Check instruction is initiated by driving the /CS pin low then shifting the instruction code "A3h" followed by the 24 Parameter bits into the DI pin. After /CS is driven high to complete the instruction cycle, the self-timed Built-in ECC Encode Check instruction will commence for a time duration of tRDEPC. While the Built-in ECC Encode Check cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Built-in ECC Encode Check cycle and becomes a 0 when the cycle is finished, and the device is ready to accept other instructions again. Note that the Built-in ECC Encode Check instruction will be ignored when BUF=0.

After the ECC Parity Data is loaded into the Data Buffer, any Read instructions can be issued to access the Data Buffer and read out the data. The Column Address for any Read instructions are don't care.

Parameter	23:19	18	17	16:0
W25N02LV	All 0	0	0	All 0

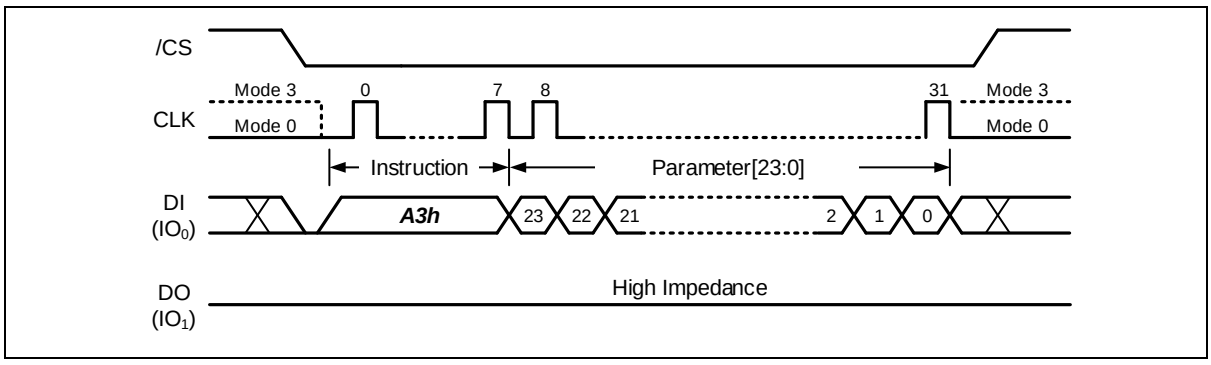


Figure 8-11 Built-in ECC Encode Check Instruction

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8.2.11 Built-in ECC Decode Check (A7h)

By executing the instruction in the following procedure, it is possible to check the ECC decode processing by Built-in ECC based on arbitrary data and arbitrary ECC Parity Data.

1. Set BUF bit in the Status Register equal 1 and set ECC-E bit in the Status Register equal 0
2. Execute Write Enable (06h) instruction to set WEL bit in the Status Register equal 1
3. Input arbitrary data and arbitrary ECC Parity Data to the Data Buffer with the Load Program Data (02h) instruction
4. Execute the Built-in ECC Decode Check (A7h) instruction
5. Wait busy time tRDEPC
6. Execute any Read instructions (03h, 0Bh, 3Bh, 6Bh, BBh, EBh, 0Dh, 6Dh, EDh) with Column Address is don't care

A Write Enable instruction must be executed before the device will accept the Built-in ECC Decode Check instruction (Status Register bit WEL must equal 1). The Built-in ECC Decode Check instruction is initiated by driving the /CS pin low then shifting the instruction code "A7h" followed by 24 Parameter bits into the DI pin. After /CS is driven high to complete the instruction cycle, the self-timed Built-in ECC Decode Check instruction will commence for a time duration of tRDEPC. While the Built-in ECC Decode Check cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Built-in ECC Decode Check cycle and becomes a 0 when the cycle is finished, and the device is ready to accept other instructions again. Note that the Built-in ECC Decode Check instruction will be ignored when BUF=0.

After the error detected and corrected data is loaded into the Data Buffer, any Read instructions can be issued to access the Data Buffer and read out the data. The Column Address for any Read instructions is don't care.

Parameter	23:19	18	17	16:0
W25N02LV	All 0	0	0	All 0

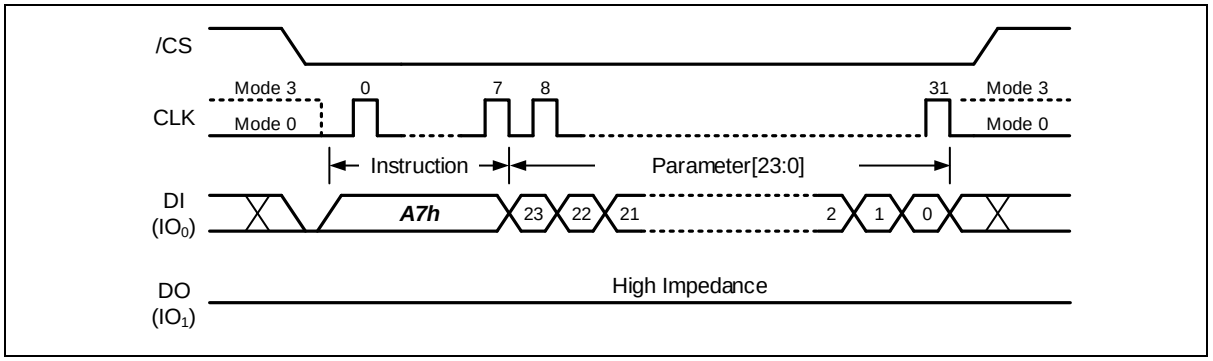


Figure 8-12 Built-in ECC Decode Check Instruction

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8.2.12 Built-in ECC Diagnostic (ADh)

The W25NxxLV offers diagnostic function for Built-in ECC circuit. It detects failures in the Built-in ECC circuit.

A Write Enable instruction must be executed before the device will accept the Built-in ECC Diagnostic instruction (Status Register bit WEL must equal 1). The Built-in ECC Diagnostic instruction is initiated by driving the /CS pin low then shifting the instruction code "ADh" followed by 24 Parameter bits into the DI pin. After /CS is driven high to complete the instruction cycle, the self-timed Built-in ECC Diagnostic instruction will commence for a time duration of tED. While the Built-in ECC Diagnostic cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Built-in ECC Diagnostic cycle and becomes a 0 when the cycle is finished, and the device is ready to accept other instructions again.

After the Built-in ECC Diagnostic cycle has finished, Read Status Register instruction can be issued to read the BED bit, and the following bits are cleared to default value.

- Status Register-3: ECC-1 and ECC-0
- Extended Internal ECC Setting Registers: BFS[3:0], MBF[3:0], MFS[2:0], BFR[15:0]

Parameter	23:19	18	17	16:0
W25N02LV	All 0	0	0	All 0

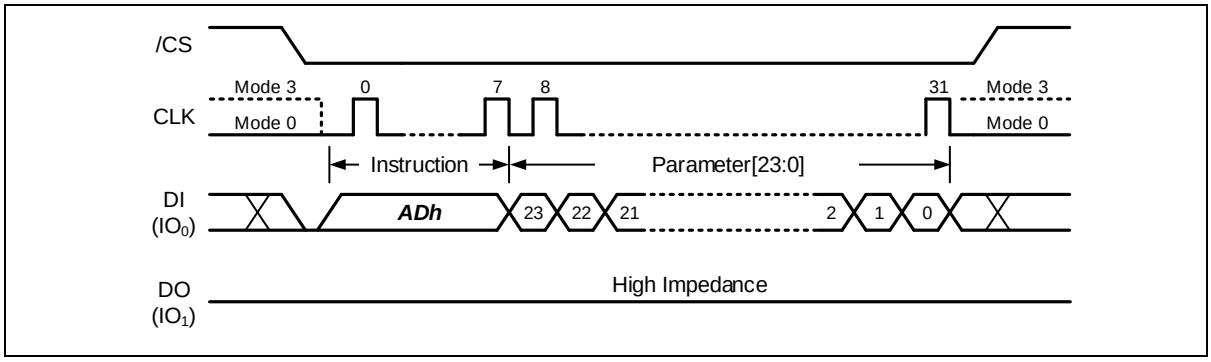


Figure 8-13 Built-in ECC Diagnostic Instruction

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8.2.13 Terminate Advanced Continuous Read (F0h)

Continuous Read is terminated by /CS=H, but in Advanced Continuous Read, Continuous Read can be temporarily paused by /CS=H. To terminate Advanced Continuous Read, execute HWRESET or Terminate Advanced Continuous Read command (F0h) or SWRESET.

The Terminate Advanced Continuous Read instruction is entered by driving /CS low, shifting the instruction code “F0h” into the DI pin and then driving /CS high. The busy time after input Terminate Advanced Continuous Read (F0h) command and terminate Advanced Continuous Read is tRDCR (just same as when terminate Continuous Read). The ACR-E bit of the Status Register-2 will not reset to 0 when terminate Advanced Continuous Read by Terminate Advanced Continuous Read (F0h) command.

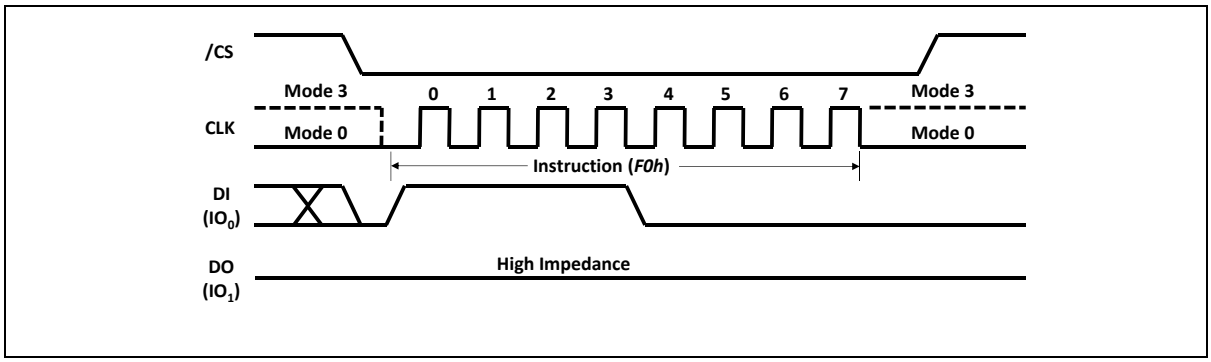


Figure 8-14 Terminate Advanced Continuous Read Instruction

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8.2.14 Deep Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code "B9h".

The /CS pin must be driven high after the eighth bit has been latched. If this is not done, the Deep Power-down instruction will not be executed. After /CS is driven high, the deep power-down state will entered within the time duration of tDP (See AC Characteristics).

While in the deep power-down state, only the Release Deep Power-down (ABh), Devise Reset (FFh or 66h/99h) instructions and Hardware Reset (/RESET pin or Reset Signaling Protocol), which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring most instructions makes the Deep Power-down state a useful condition for securing maximum write protection. The device always powers-up in normal operation with the standby current ICC1.

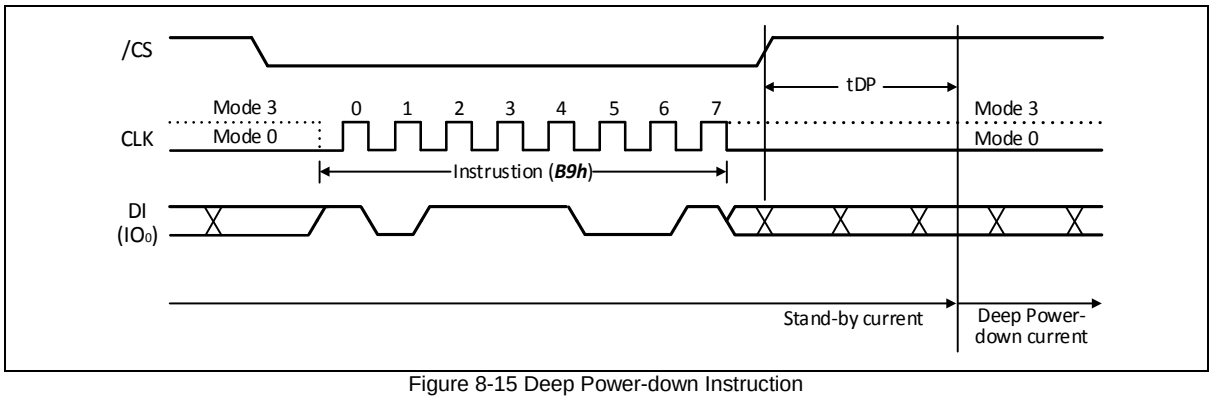


Figure 8-15 Deep Power-down Instruction

8.2.15 Release Deep Power-down (ABh)

The Release Deep Power-down instruction can be used to release the device from the power-down state. To release the device from the deep power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code "ABh" and driving /CS high. Release from the deep power-down state will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the tRES1 time duration. During tRES1, all bits of the Status Registers return to the shipment default values (However, OTP-L, SR1-L, and LUT-F depend on the values immediately before entering the Deep Power-down state), and Auto Page Data Read operation (Automatically execution of Page Data Read (13h) instruction for Page 0 of Block0) is executed.

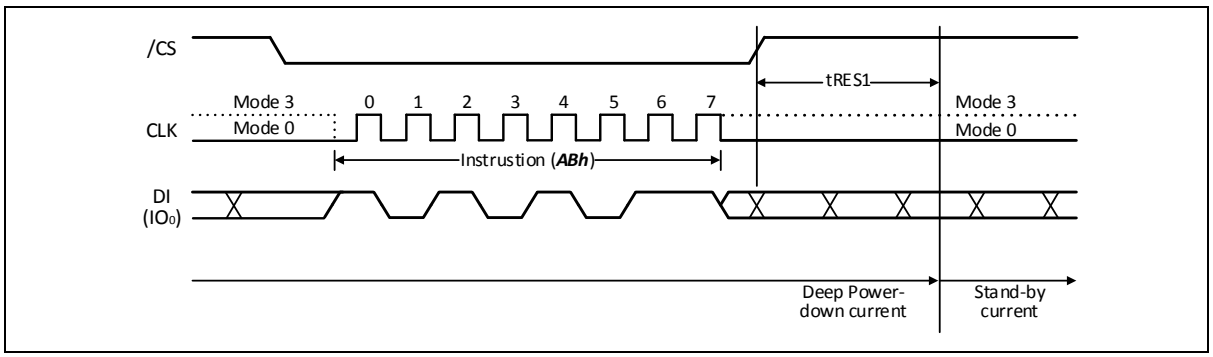


Figure 8-16 Release Deep Power-down Instruction

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8.2.16 Block Erase (D8h)

The Block Erase instruction sets all bits within a specified block (64-Pages) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” followed by 24 Page Address bits. The Block Erase instruction sequence is shown below.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE}. While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished, and the device is ready to accept other instructions again.

After the Block Erase cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed block is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits.

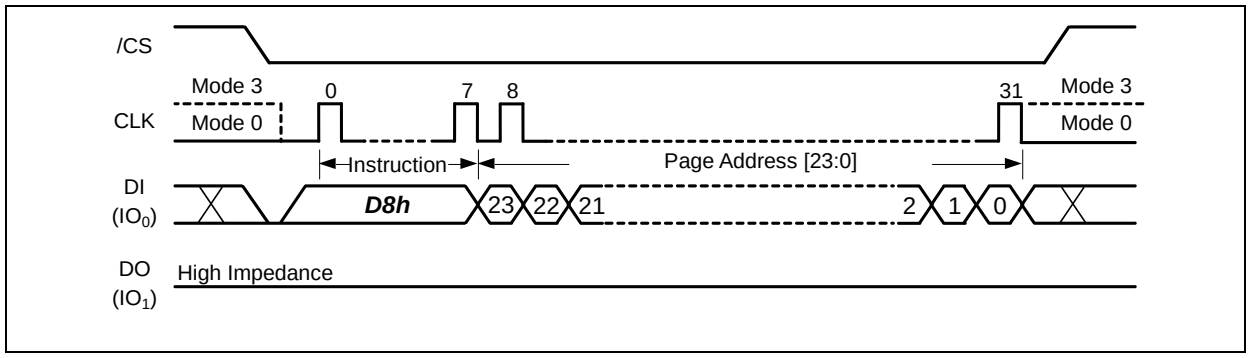


Figure 8-17 Block Erase Instruction

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8.2.17 Load Program Data (02h) / Random Load Program Data (84h)

The Program operation allows from one byte to 2,176 bytes or 4,352 bytes (a page) of data to be programmed at previously erased (FFh) memory locations.

A Program operation involves two steps:

1. Load the program data into the Data Buffer
2. Issue the “Program Execute” instruction to transfer data from the Data Buffer to the specified memory page

A Write Enable instruction must be executed before the device will accept the Load Program Data Instructions (Status Register bit WEL=1). The “Load Program Data” or “Random Load Program Data” instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” or “84h” followed by 16 Column Address bits (only CA[12:0] is effective). The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. If the number of data bytes sent to the device exceeds the number of data bytes in the Data Buffer, the extra data will be ignored by the device. The Load Program Data instruction sequence is shown below.

Both “Load Program Data” and “Random Load Program Data” instructions share the same instruction sequence. The difference is that “Load Program Data” instruction will reset the unused data bytes in the Data Buffer to the FFh value, while the “Random Load Program Data” instruction will only update the data bytes that are specified by the instruction input sequence. The rest of the Data Buffer will remain unchanged.

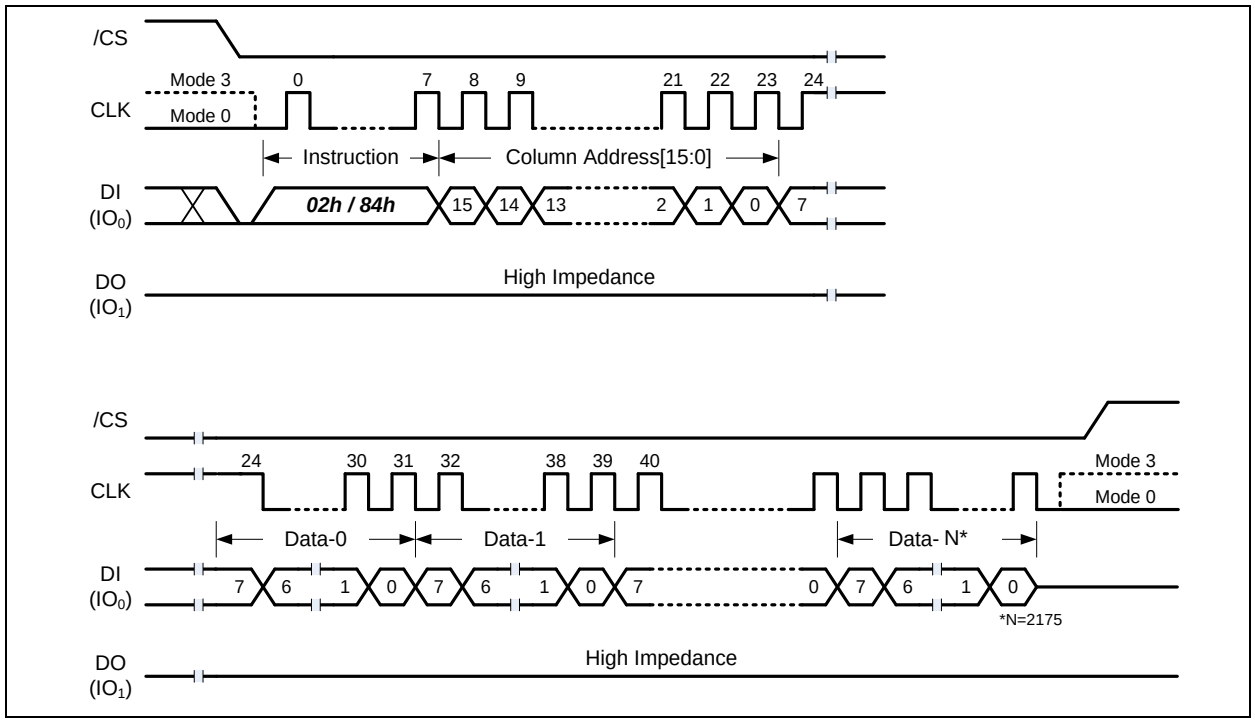


Figure 8-18 Load / Random Load Program Data Instruction

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8.2.18 Quad Load Program Data (32h) / Quad Random Load Program Data (34h)

The “Quad Load Program Data” and “Quad Random Load Program Data” instructions are identical to the “Load Program Data” and “Random Load Program Data” in terms of the operation sequence and functionality. The only difference is that “Quad Load” instructions will input the data bytes from all four IO pins instead of the single DI pin. This method will significantly shorten the data input time when a large amount of data needs to be loaded into the Data Buffer. The instruction sequence is shown below.

Both “Quad Load Program Data” and “Quad Random Load Program Data” instructions share the same instruction sequence. The difference is that “Quad Load Program Data” instruction will reset the unused data bytes in the Data Buffer to an FFh value, while the “Quad Random Load Program Data” instruction will only update the data bytes that are specified by the instruction input sequence. The rest of the Data Buffer will remain unchanged.

When the WP-E bit in the Status Register is set to a 1, all Quad SPI instructions are disabled.

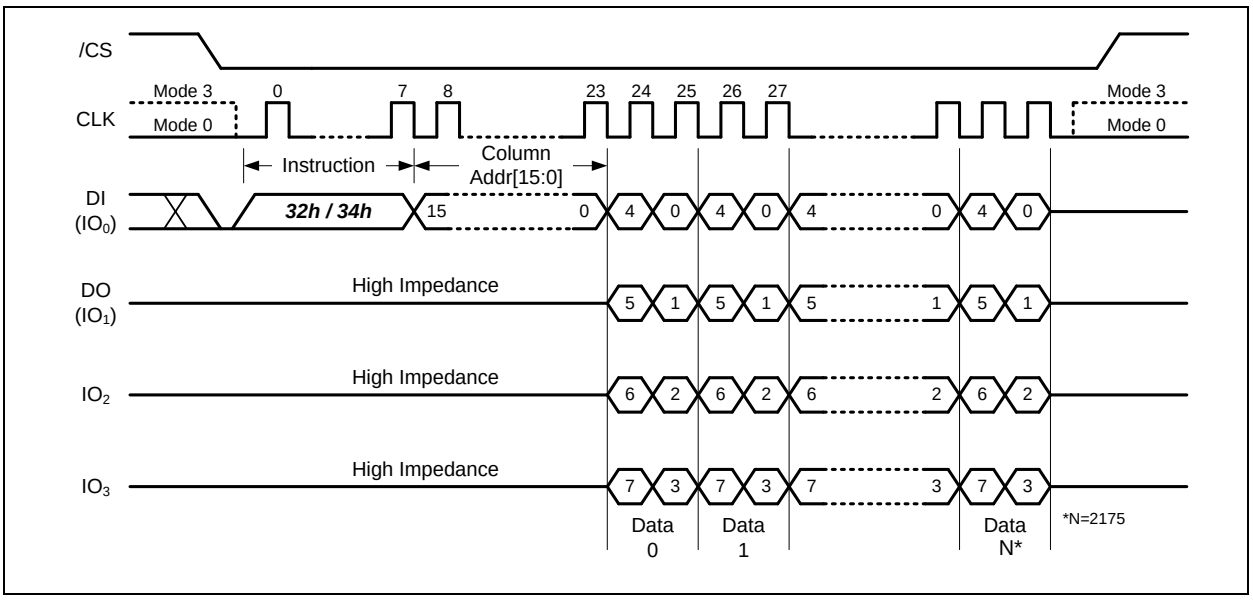


Figure 8-19 Quad Load / Quad Random Load Program Data Instruction

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8.2.19 Program Execute (10h)

The Program Execute instruction is the second step of the Program operation. After the program data is loaded into the Data Buffer, the Program Execute instruction will program the Data Buffer content into the physical memory page that is specified in the instruction. The instruction is initiated by driving the /CS pin low then shifting the instruction code “10h” followed by 24 Page Address bits into the DI pin.

After /CS is driven high to complete the instruction cycle, the self-timed Program Execute instruction will commence for a time duration of tPP1 or tPP2. While the Program Execute cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Program Execute cycle and becomes a 0 when the cycle is finished, and the device is ready to accept other instructions again. After the Program Execute cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Program Execute instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits.

The pages within the block have to be programmed sequentially from the lower order page address to the higher order page address within the block. Programming pages out of sequence is prohibited.

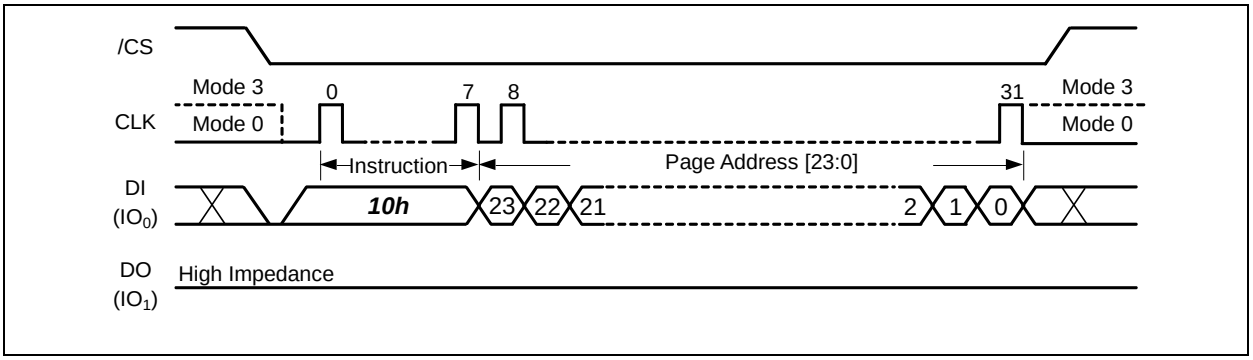


Figure 8-20 Program Execute Instruction

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8.2.20 Page Data Read (13h)

The Page Data Read instruction will transfer the data of the specified memory page into the Data Buffer. The instruction is initiated by driving the /CS pin low then shifting the instruction code “13h” followed by 24 Page Address bits into the DI pin.

After /CS is driven high to complete the instruction cycle, the self-timed Read Page Data instruction will commence for a time duration of tRD. While the Read Page Data cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Read Page Data cycle and becomes a 0 when the cycle is finished, and the device is ready to accept other instructions again.

After the 2,176 bytes or 4,352 bytes of page data is loaded into the Data Buffer, several Read instructions can be issued to access the Data Buffer and read out the data. Depending on the BUF bit and the ECC-E bit settings in the Status Register, either “Buffer Read Mode”, “Continuous Read Mode” or “Sequential Read Mode” may be used to accomplish the read operations.

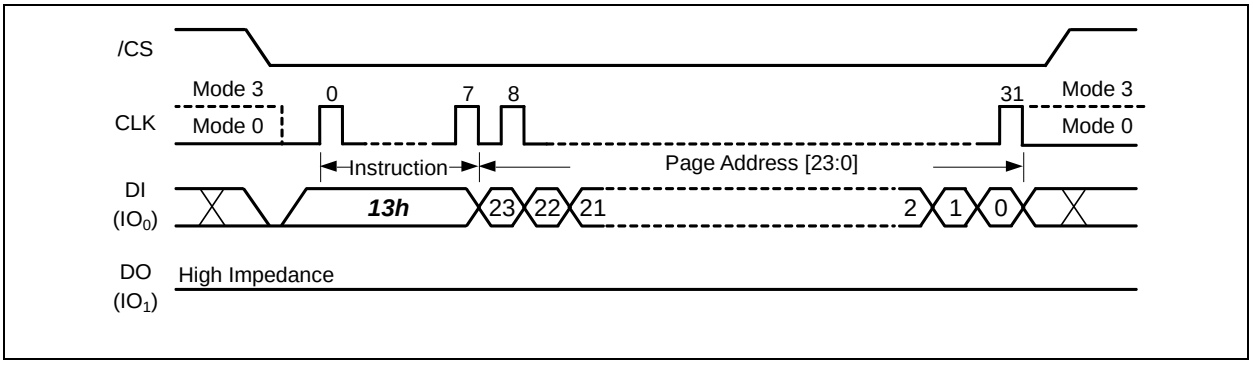


Figure 8-21 Page Data Read Instruction

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8.2.21 Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Read Data instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by 16 Column Address bits and 8 dummy clocks or 24 dummy clocks into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with the most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving /CS high.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16 Column Address bits and continues to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode or Sequential Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of the next memory page will follow and continue through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible with Winbond’s SpiFlash NOR flash memory instruction sequence.

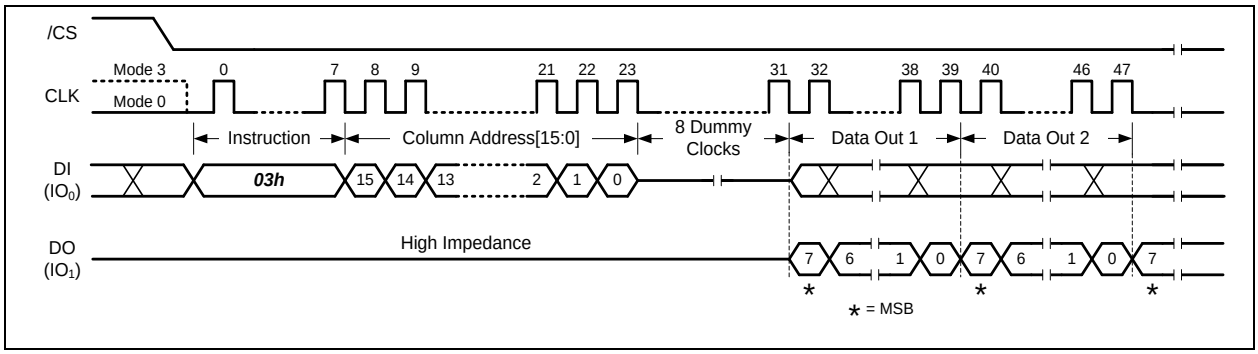


Figure 8-22 Read Data Instruction (Buffer Read Mode, BUF=1)

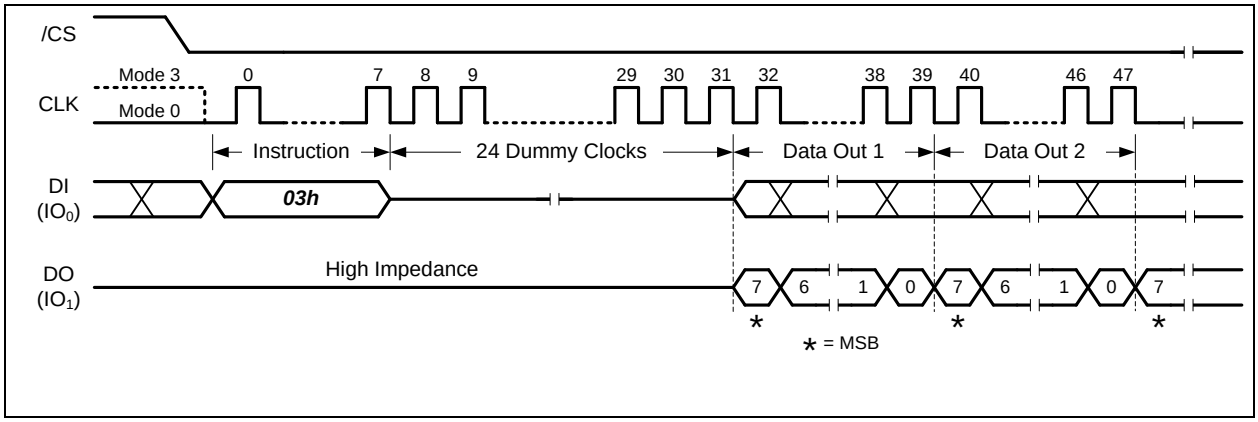


Figure 8-23 Read Data Instruction (Continuous Read Mode or Sequential Read Mode, BUF=0)

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8.2.22 Fast Read (0Bh)

The Fast Read instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Fast Read instruction is initiated by driving the /CS pin low and then shifting the instruction code “0Bh” followed by 16 Column Address bits and 8 dummy clocks or 32 dummy clocks into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving /CS high.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16 Column Address bits and continues to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode or Sequential Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of the next memory page will follow and continue through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible with Winbond’s SpiFlash NOR flash memory instruction sequence.

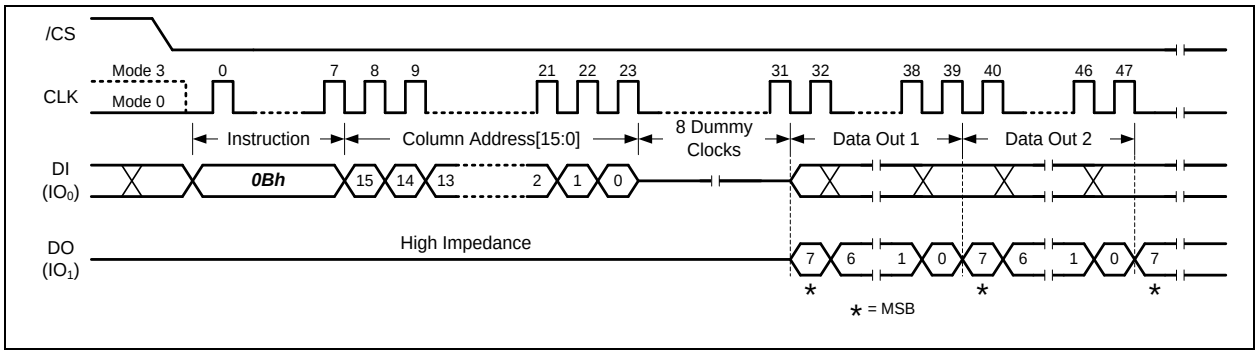


Figure 8-24 Fast Read Instruction (Buffer Read Mode, BUF=1)

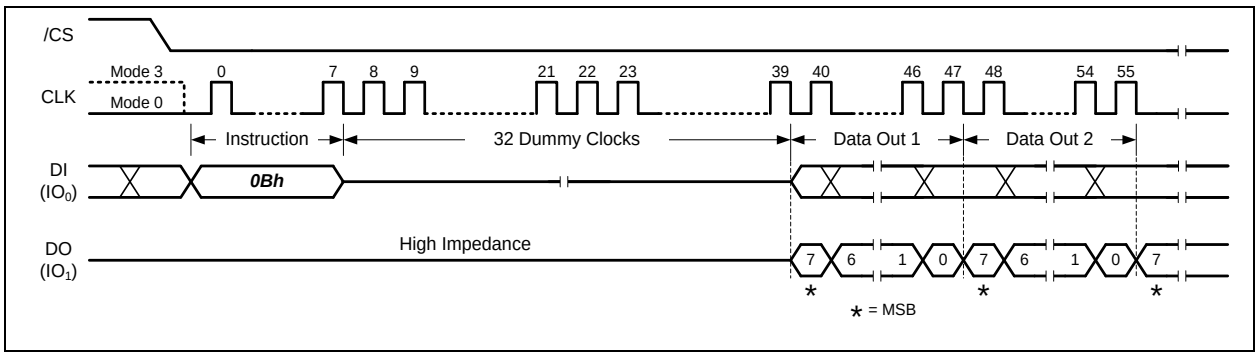


Figure 8-25 Fast Read Instruction (Continuous Read Mode or Sequential Read Mode, BUF=0)

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8.2.23 Fast Read Dual Output (3Bh)

The Fast Read Dual Output instruction is like the standard Fast Read (0Bh) instruction except that data is output on two pins: IO_0 and IO_1. This allows data to be transferred at twice the rate of standard SPI devices.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by 16 Column Address bits and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode or Sequential Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of the next memory page will follow and continue through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible with Winbond's SpiFlash NOR flash memory instruction sequence.

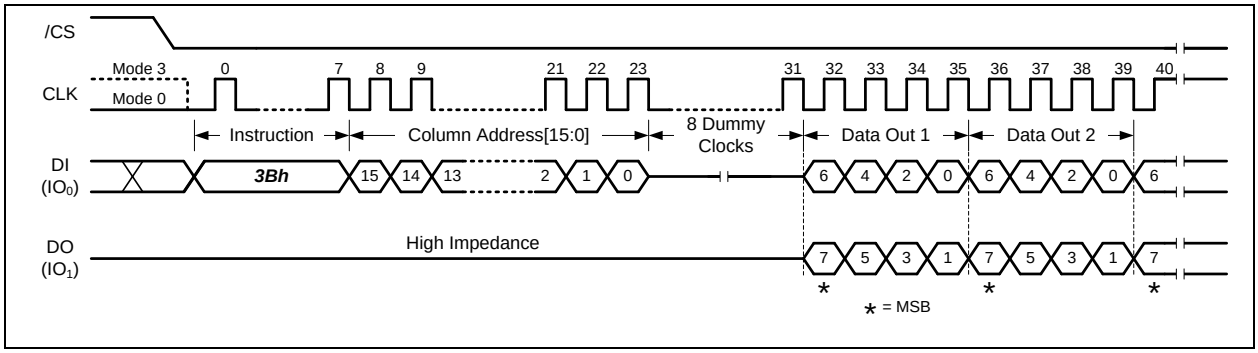


Figure 8-26 Fast Read Dual Output Instruction (Buffer Read Mode, BUF=1)

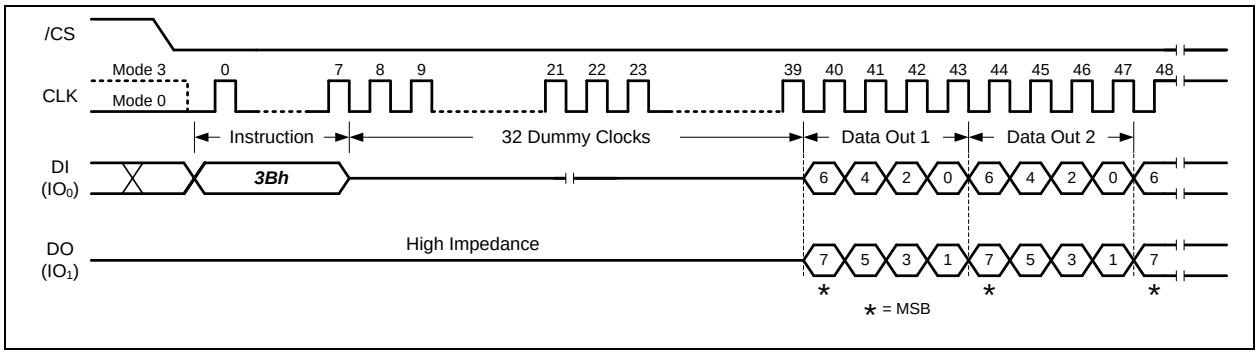


Figure 8-27 Fast Read Dual Output Instruction (Continuous Read Mode or Sequential Read Mode, BUF=0)

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8.2.24 Fast Read Quad Output (6Bh)

The Fast Read Quad Output instruction is like the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO_0, IO_1, IO_2, and IO_3. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by 16-bits Column Address bits and continues to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode or Sequential Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of the next memory page will follow and continue through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible with Winbond's SpiFlash NOR flash memory instruction sequence.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

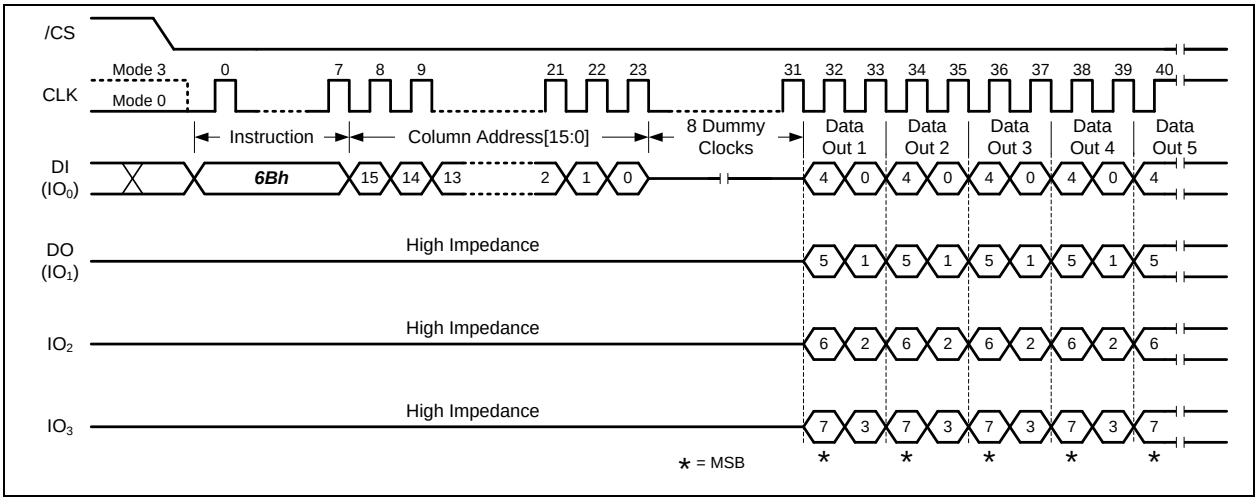


Figure 8-28 Fast Read Quad Output Instruction (Buffer Read Mode, BUF=1)

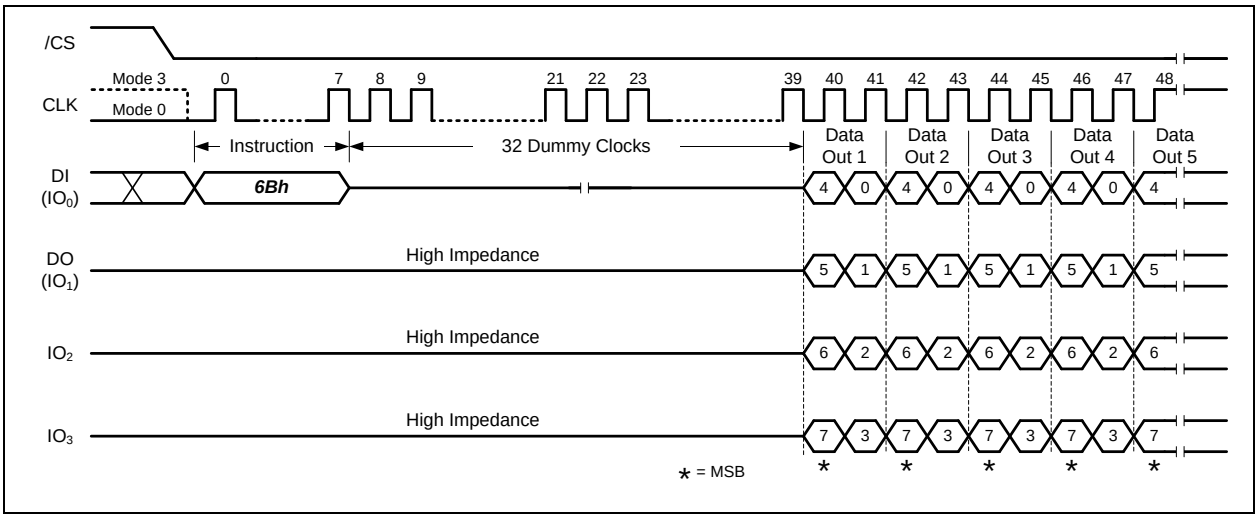


Figure 8-29 Fast Read Quad Output Instruction (Continuous Read Mode or Sequential Read Mode, BUF=0)

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8.2.25 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO_0 and IO_1. It is like the Fast Read Dual Output (3Bh) instruction but with the capability to input the Column Address or the dummy clocks two bits per clock.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by 16 Column Address bits and continues to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode or Sequential Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of the next memory page will follow and continue through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible with Winbond's SpiFlash NOR flash memory instruction sequence.

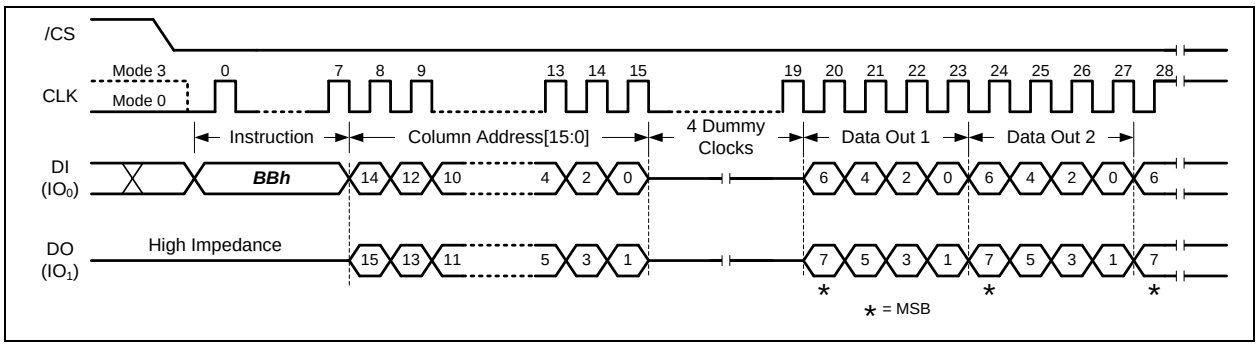


Figure 8-30 Fast Read Dual I/O Instruction (Buffer Read Mode, BUF=1)

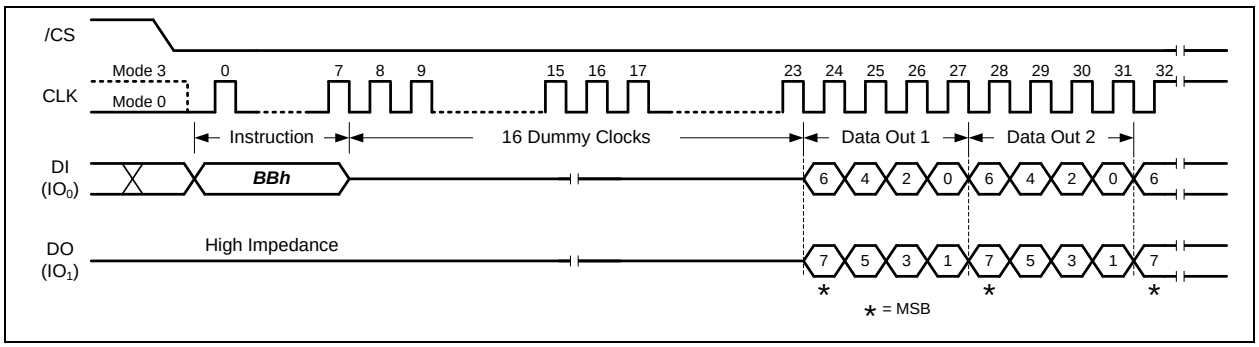


Figure 8-31 Fast Read Dual I/O Instruction (Continuous Read Mode or Sequential Read Mode, BUF=0)

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8.2.26 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O instruction is like the Fast Read Dual I/O (BBh) instruction except that the address and data bits are input and output through four pins IO_0, IO_1, IO_2 and IO_3 prior to the data output.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by 16 Column Address bits and continues to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode or Sequential Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of the next memory page will follow and continue through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible with Winbond's SpiFlash NOR flash memory instruction sequence.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

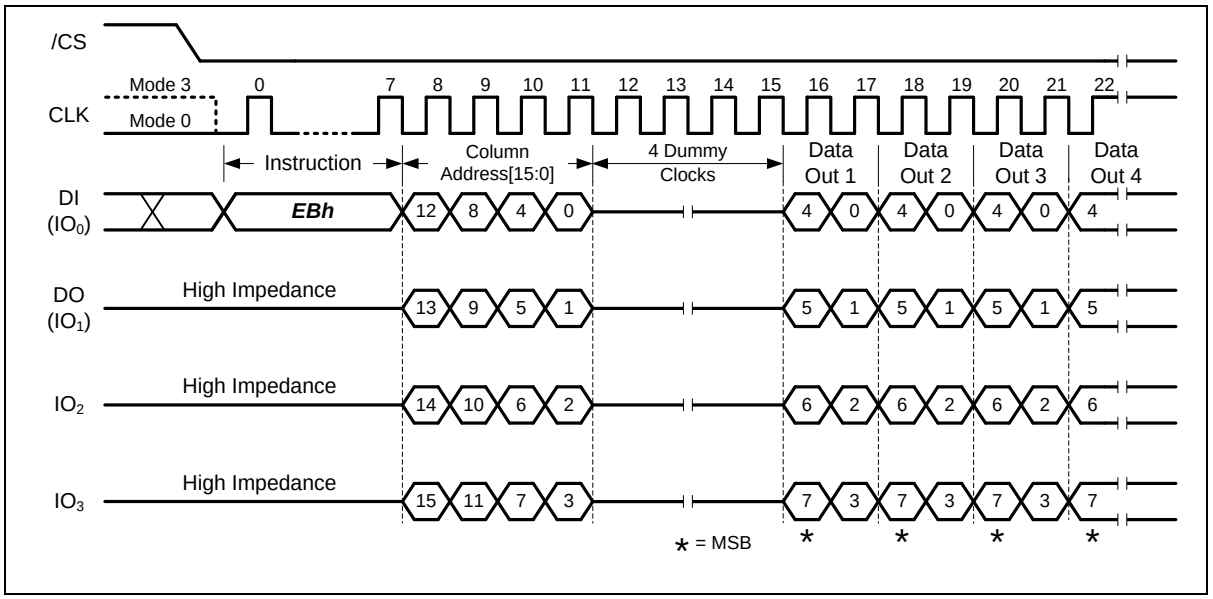


Figure 8-32 Fast Read Quad I/O Instruction (Buffer Read Mode, BUF=1)

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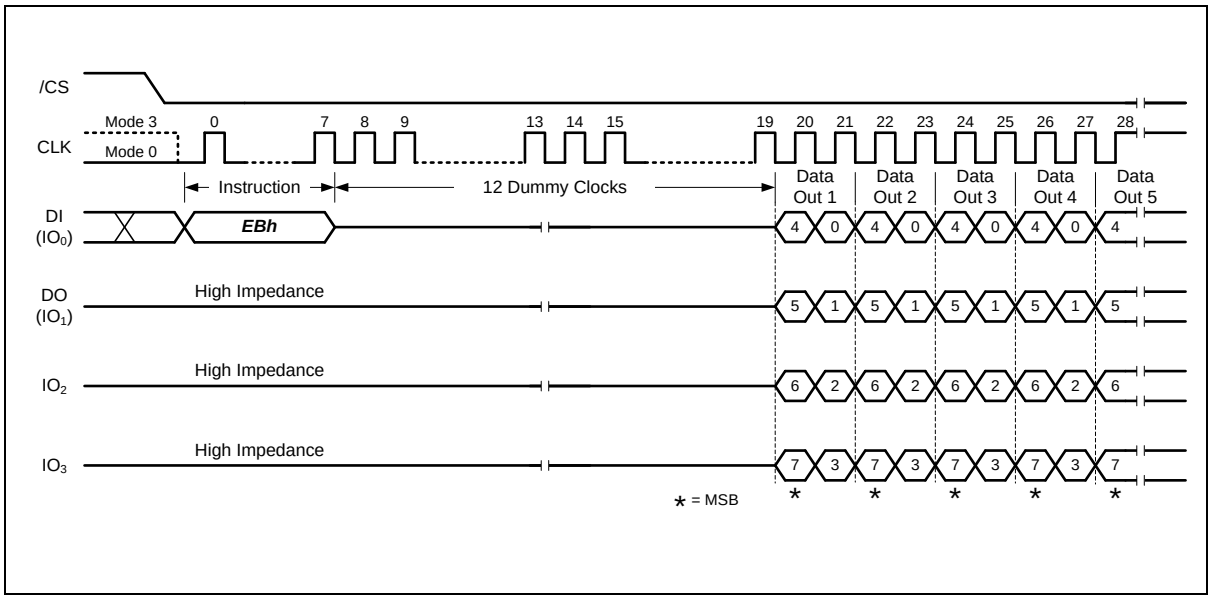


Figure 8-33 Fast Read Quad I/O Instruction (Continuous Read Mode or Sequential Read Mode, BUF=0)

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8.2.27 DTR Fast Read (0Dh)

The DTR Fast Read instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The DTR Fast Read instruction is initiated by driving the /CS pin low and then shifting the instruction code “0Dh” followed by 16 Column Address bits and 8 dummy clocks or 18 dummy clocks into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at both edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving /CS high.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by 16 Column Address bits and continues to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode or Sequential Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of the next memory page will follow and continue through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible with Winbond’s SpiFlash NOR flash memory instruction sequence.

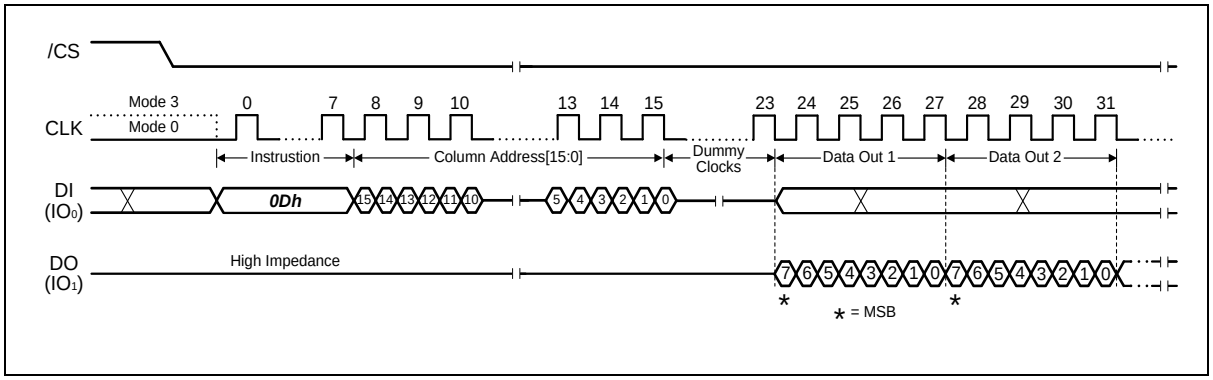


Figure 8-34 DTR Fast Read Instruction (Buffer Read Mode, BUF=1)

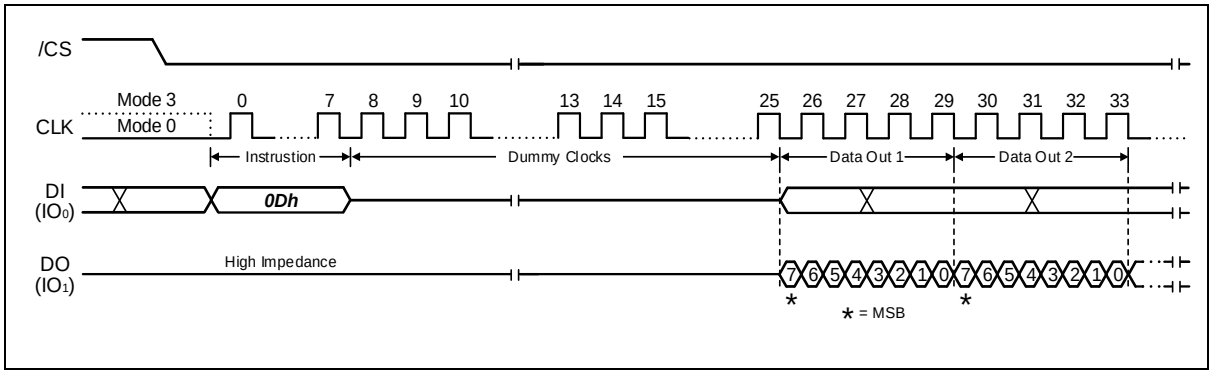


Figure 8-35 DTR Fast Read Instruction (Continuous Read Mode or Sequential Read Mode, BUF=0)

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8.2.28 DTR Fast Read Quad Output (6Dh)

The DTR Fast Read Quad Output instruction is like the DTR Fast Read Dual Output (3Dh) instruction except that data is output on four pins, IO_0, IO_1, IO_2, and IO_3. The DTR Fast Read Quad Output Instruction allows data to be transferred at four times the rate of the DTR Fast Read (0Dh) instruction.
When BUF=1, the device is in the Buffer Read Mode or Sequential Read Mode. The data output sequence will start from the Data Buffer location specified by 16 Column Address bits and continues to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.
When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of the next memory page will follow and continue through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible to Winbond's SpiFlash NOR flash memory instruction sequence.
When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

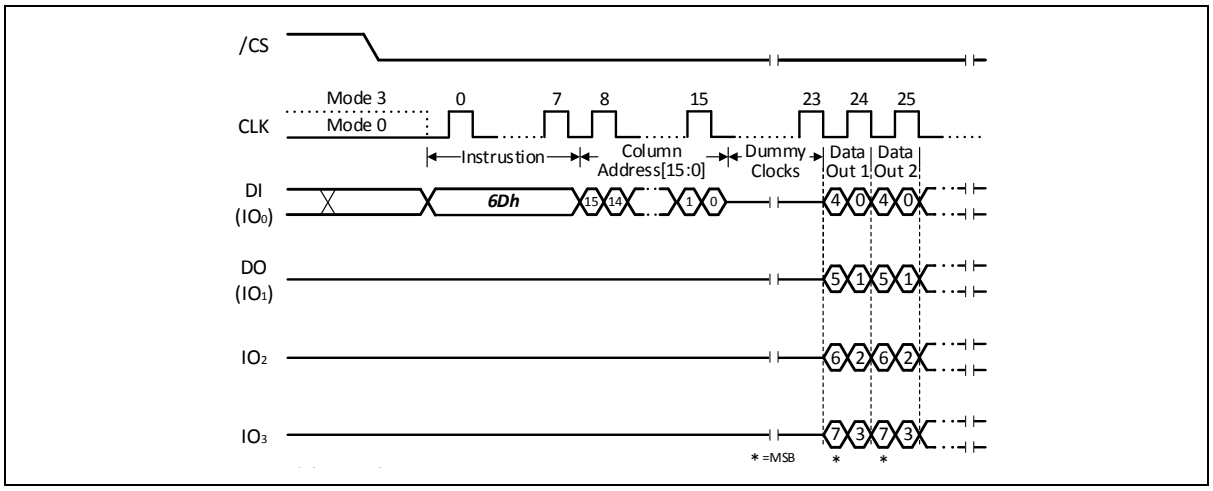


Figure 8-36 DTR Fast Read Quad Output Instruction (Buffer Read Mode, BUF=1)

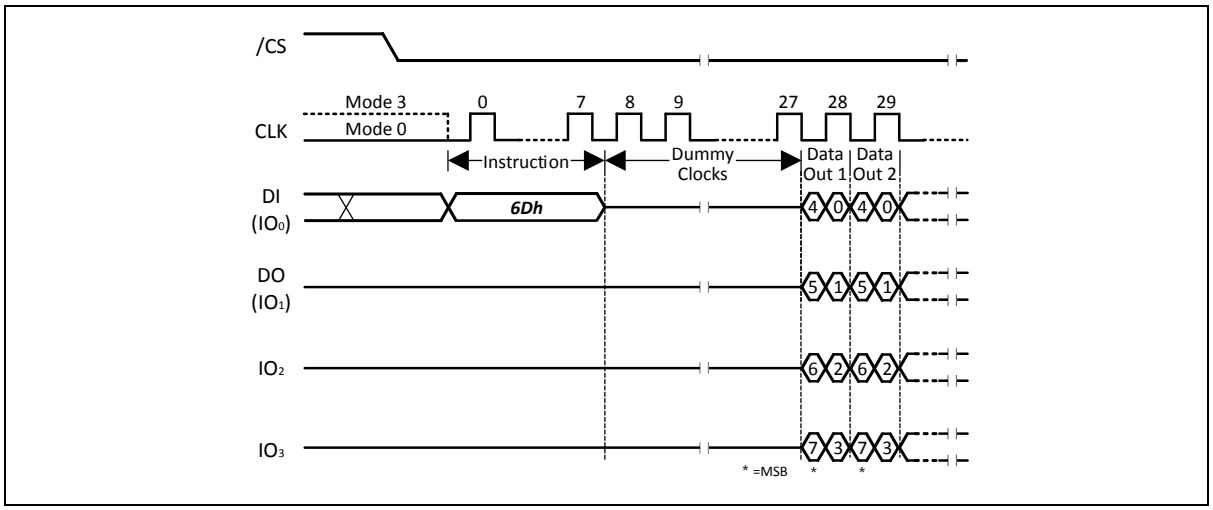


Figure 8-37 DTR Fast Read Quad Output Instruction (Continuous Read Mode or Sequential Read Mode, BUF=0)

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8.2.29 DTR Fast Read Quad I/O (EDh)

The DTR Fast Read Quad I/O instruction is like the DTR Fast Read Dual I/O (BDh) instruction except that address and data bits are input and output through four pins IO_0, IO_1, IO_2 and IO_3 prior to the data output.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by 16 Column Address bits and continues to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode or Sequential Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of the next memory page will follow and continue through the entire memory array. This allows using a single Read instruction to read out the entire memory array and is also compatible with Winbond's SpiFlash NOR flash memory instruction sequence. When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

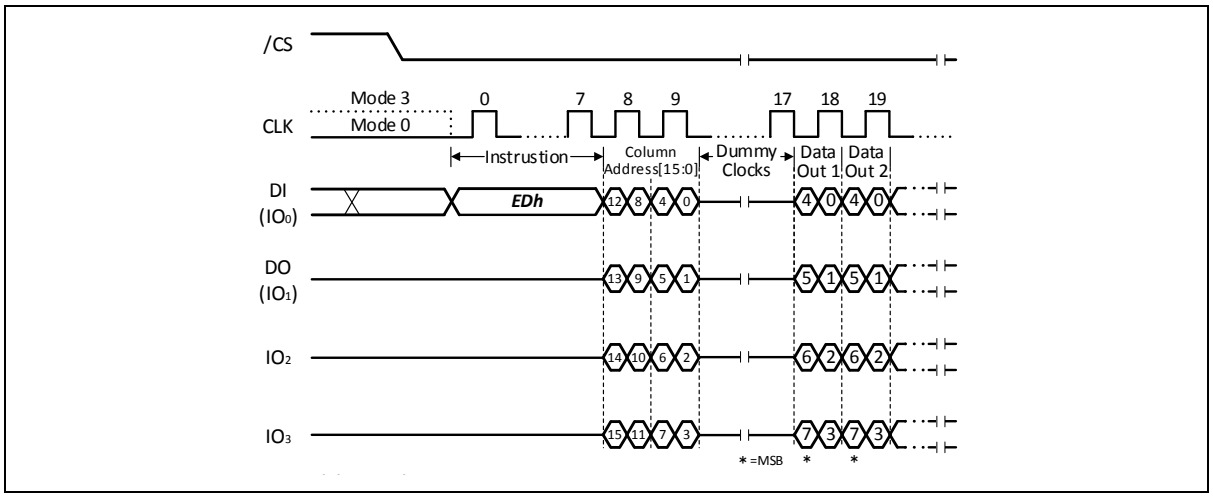


Figure 8-38 DTR Fast Read Quad I/O Instruction (Buffer Read Mode, BUF=1)

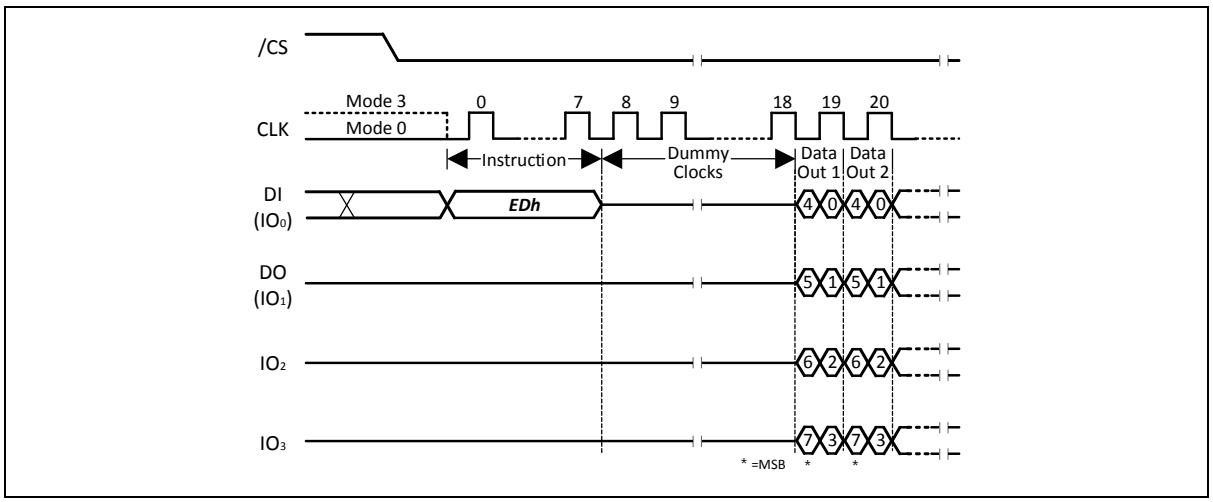


Figure 8-39 DTR Fast Read Quad I/O Instruction (Continuous Read Mode or Sequential Read Mode, BUF=0)

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8.2.30 Accessing Unique ID / Parameter / OTP Pages (OTP-E=1)

In addition to the main memory array, the W25N02LV is also equipped with one Unique ID Page, one Parameter Page, one CASN page, and ten OTP Pages.

Page Address	Column Address	Page Name	Descriptions	Data Length
00h	00h	Unique ID Page	Factory programmed, Read Only	32-Bytes x 16
01h	00h	Parameter Page	Factory programmed, Read Only	256-Bytes x 3
01h	300h	CASN Page (1)	Factory programmed, Read Only	256-Bytes x 3
02h	00h	OTP Page [0]	Program Only, OTP lockable	2,176-Bytes
…	00h	OTP Pages [1:8]	Program Only, OTP lockable	2,176-Bytes
0Bh	00h	OTP Page [9]	Program Only, OTP lockable	2,176-Bytes

To access these additional data pages, the OTP-E bit in Status Register-2 must be set to "1" first. Then, the Read operations can be performed on Unique ID and Parameter Pages, Read and Program operations can be performed on the OTP pages if it's not already locked. To return to the main memory array operation, OTP-E bit needs to be to set to 0.

Read Operations

A "Page Data Read" instruction must be issued followed by a specific page address shown in the table above to load the page data into the main Data Buffer. After the device finishes the data loading (BUSY=0), all Read instructions may be used to read the Data Buffer starting from any specified Column Address. Please note all Read instructions must now follow only the "Buffer Read Mode" instruction structure (CA[15:0], number of dummy clocks) regardless the previous BUF bit and BRC-E bit setting.

Program and OTP Lock Operations

OTP pages provide additional space (4K-Bytes x 10) to store important data or security information that can be locked to prevent further modification in the field. These OTP pages are in an erased state set in the factory and can only be programmed (change data from "1" to "0") until being locked by OTP-L bit in the Configuration/Status Register-2. OTP-E must be first set to "1" to enable the access to these OTP pages, then the program data must be loaded into the main Data Buffer using any "Program Data Load" instructions. The "Program Execute" instruction followed by a specific OTP Page Address is used to initiate the data transfer from the Data Buffer to the OTP page.

Once the OTP pages are correctly programmed, OTP-L bit can be used to permanently lock these pages so that no further modification is possible. While still in the "OTP Access Mode" (OTP-E=1), the user needs to set OTP-L bit in the Configuration/Status Register-2 to "1" and issue a "Program Execute" instruction without any Page Address. After the device finishes the OTP lock setting (BUSY=0), the user can set OTP-E to "0" to return to the main memory array operation.

SR1-L OTP Lock Operation

The Protection/Status Register-1 contains protection bits that can be set to protect either a portion or the entire memory array from being Programmed/Erased or set the device to either Software Write Protection (WP-E=0), or Hardware Write Protection (WP-E=1). Once the BP[3:0], TB, WP-E bits are set correctly, SRP1 and SRP0 should also be set to "1"s as well to allow SR1-L bit being set to "1" to permanently lock the protection settings in the Status Register-1 (SR1). Like the OTP-L setting procedure above, to set SR1-L lock bit, the device must enter the "OTP Access Mode" (OTP-E=1) first, and SR1-L bit should be set to "1" prior to the "Program Execute" instruction without any Page Address. Once SR1-L is set to "1" (BUSY=0), the user can set OTP-E to "0" to return to the main memory array operation.

Notes:

1. Regarding details about CASN (Common Attributes for SPI-NAND), please confirm the Application Note "AN0000075: Winbond CASN Page Data Information".

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8.2.31 Parameter Page Data Definitions

The Parameter Page contains 3 identical copies of the 256-Bytes Parameter Data. The table below lists all the key data byte locations. All other unspecified byte locations have 00h data as default.

Byte Number	Descriptions	Values
0~3	Parameter page signature	4Fh, 4Eh, 46h, 49h
4~5	Revision number	00h, 00h
6~7	Feature supported	00h, 00h
8~9	Optional command supported	00h, 00h
10~31	Reserved	All 00h
32~43	Device manufacturer	57h, 49h, 4Eh, 42h, 4Fh, 4Eh, 44h, 20h, 20h, 20h, 20h, 20h
44~63	Device model	57h, 32h, 35h, 4Eh, 30h, 32h, 4Ch, 56h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	JEDEC manufacturer ID	EFh
65~66	Date code	00h, 00h
67~79	Reserved	All 00h
80~83	Number of data bytes per page	00h, 08h, 00h, 00h
84~85	Number of spare bytes per page	80h, 00h
86~91	Reserved	All 00h
92~95	Number of pages per block	40h, 00h, 00h, 00h
96~99	Number of blocks per logical unit	00h, 08h, 00h, 00h
100	Number of logical units	01h
101	Number of address bytes	00h
102	Number of bits per cell	01h
103~104	Bad blocks maximum per unit	28h, 00h
105~106	Block endurance	01h, 05h
107	Guaranteed valid blocks at beginning of target	01h
108~109	Block endurance for guaranteed valid blocks	00h, 00h
110	Number of programs per page	04h
111	Reserved	00h
112	Number of ECC bits	00h
113	Number of plane address bits	00h
114	Multi-plane operation attributes	00h
115~127	Reserved	All 00h
128	I/O pin capacitance, maximum	08h
129~132	Reserved	All 00h
133~134	Maximum page program time (us)	58h, 02h
135~136	Maximum block erase time (us)	10h, 27h
137~138	Maximum page read time (us)	3Ch, 00h
139~163	Reserved	All 00h
164~165	Vendor specific revision number	00h, 00h
166~253	Vendor specific	All 00h
254~255	Integrity CRC	4Ch, 85h
256~511	Value of bytes 0~255	
512~767	Value of bytes 0~255	
768~4351	Reserved	

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9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to +4.6	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to 4.6	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–2.0 to VCC+2.0	V
Storage Temperature	TSTG		–65 to +150	℃
Lead Temperature	TLEAD		See Note (2)	℃
Electrostatic Discharge Voltage	VESD	Human Body Model (3)	–2000 to +2000	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Standard JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

9.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	VCC		2.7	3.6	V
Ambient Temperature, Operating	TA	Industrial	–40	+85	°C
		Industrial Plus		+105	

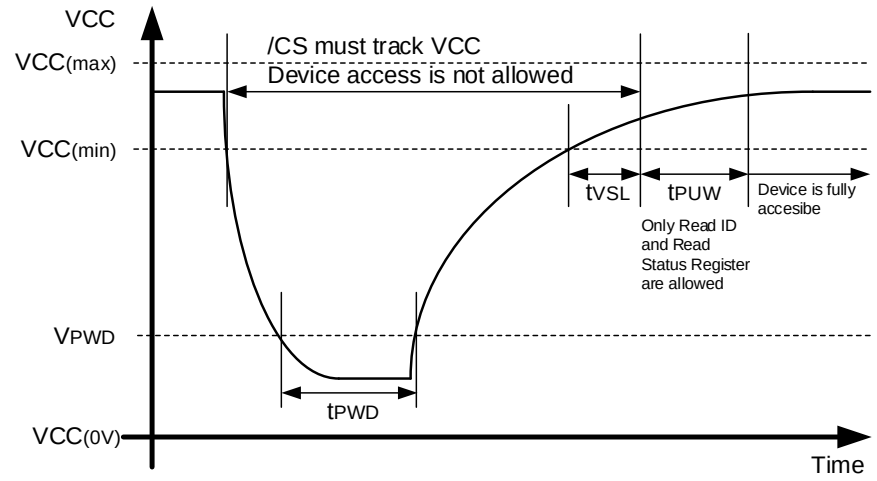
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9.3 Power-up Power-down Timing Requirements

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS low	t_{VSL} (1)	200		µs
Time Delay Before Write Instruction	t_{PUW} (1)	2.2		ms
Minimum duration for ensuring initialization will occur	t_{PWD} (1)	1		ms
VCC voltage for ensuring initialization will occur	V_{PWD} (1)		0.7	V

Notes:

1. These parameters are characterized only.



Notes:

Only the BUSY bit of Status Register-3 can be read during the tPUW period.

Figure 9-1 Power-up Timing and Voltage Levels

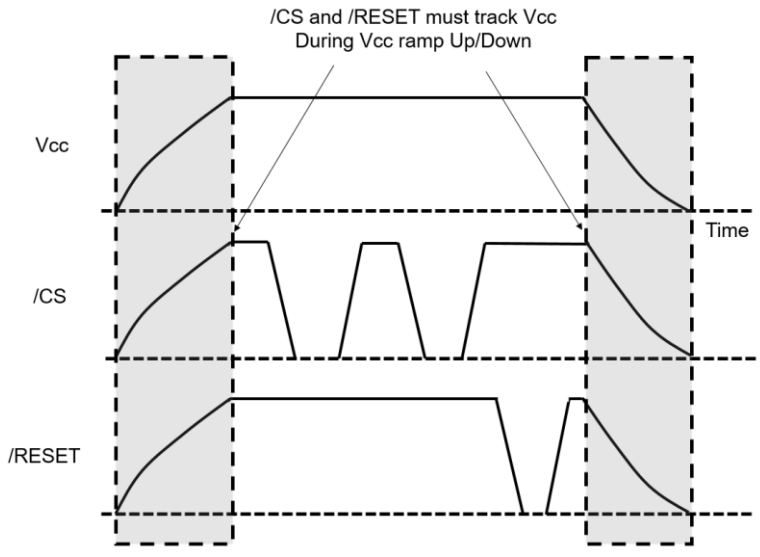


Figure 9-2 Power-up, Power-down Requirement

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9.4 DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	C_{IN} (1)	V_{IN} = 0V (1)			6	pF
Output Capacitance	C_{OUT} (1)	V_{OUT} = 0V (1)			8	pF
Input Leakage	I_{LI}				±2	µA
I/O Leakage	I_{LO}				±2	µA
Standby Current	I_{CC1}	/CS=VCC, VIN=GND or VCC, -40℃≤ T_A ≤ 85℃		10	50	µA
		/CS=VCC, VIN=GND or VCC, -40℃≤ Ta ≤ 105℃			70	
Deep Power-down Current	I_{CC2}	/CS=VCC, VIN=GND or VCC, -40℃≤ T_A ≤ 85℃		1	15	µA
		/CS=VCC, VIN=GND or VCC, -40℃≤ Ta ≤ 105℃			15	
Read Current	I_{CC3}	C = 0.1 VCC / 0.9 VCC at 133MHz, DO = Open, Fast Read with Buffer Read		15	25	mA
		C = 0.1 VCC / 0.9 VCC at 133MHz, DO = Open, Fast Read with Continuous Read		45	65	mA
		C = 0.1 VCC / 0.9 VCC at 133MHz, DO = Open, Fast Read Dual I/O with Buffer Read		20	30	mA
		C = 0.1 VCC / 0.9 VCC at 133MHz, DO = Open, Fast Read Dual I/O with Continuous Read		50	70	mA
		C = 0.1 VCC / 0.9 VCC at 133MHz, DO = Open, Fast Read Quad I/O with Buffer Read		25	35	mA
		C = 0.1 VCC / 0.9 VCC at 133MHz, DO = Open, Fast Read Quad I/O with Continuous Read		55	75	mA
Current Page Program	I_{CC4}	/CS = VCC		20	25	mA
Current Block Erase	I_{CC5}	/CS = VCC		20	25	mA
Input Low Voltage	V_{IL}		–0.5		VCC x 0.3	V
Input High Voltage	V_{IH}		VCC x 0.7		VCC + 0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = –400 µA	2.4			V

Notes:

1. The typical (TYP) value is tested on a sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.3V.

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9.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC		V

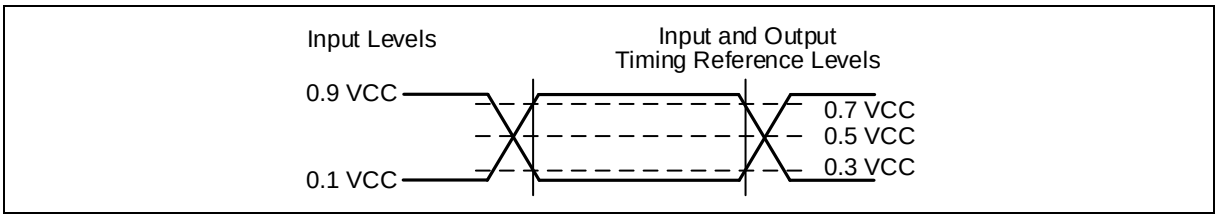


Figure 9-3 AC Measurement I/O Waveform

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9.6 AC Electrical Characteristics

DESCRIPTION	SYMBOL	ALT	DATA TRANSFER RATE	SPEC			UNIT
				MIN	TYP	MAX	
Clock frequency for all instructions except for DTR instructions	F_R	f_{C1}	STR only	D.C.		133	MHz
Clock frequency for all DTR instructions	F_R	f_{C1}	DTR only	D.C.		66	MHz
Clock High, Low Time for all instructions	t_{CLH}, t_{CLL} (1)		STR/DTR	0.45× 1/ F_R			ns
/CS High, Low Time for Reset Signaling Protocol	t_{CSH}, t_{CSL}		STR/DTR	500			ns
Clock Rise Time peak to peak	t_{CLCH} (2)		STR/DTR	0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL} (2)		STR/DTR	0.1			V/ns
/CS Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	STR/DTR	4			ns
/CS Not Active Hold Time relative to CLK	t_{CHSL}		STR/DTR	4			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	STR/DTR	2			ns
	t_{DVCL}		DTR only	2			
Data In Setup Time for Reset Signaling Protocol	t_{RPS}		STR/DTR	5			ns
Data In Hold Time	t_{CHDX}	t_{DH}	STR/DTR	2			ns
	t_{CLDX}		DTR only	2			
Data In Hold Time for Reset Signaling Protocol	t_{RPH}		STR/DTR	5			ns
/CS Active Hold Time relative to CLK	t_{CHSH}		STR	3			ns
			DTR	6			
/CS Active Hold Time relative to CLK LOW	t_{CLSH}		DTR only	3			ns
/CS Not Active Setup Time relative to CLK	t_{SHCH}		STR	3			ns
			DTR	6			
/CS Deselect Time (for Read (6) → Read (6))	$t_{SHSL}1$	t_{CSH}	STR/DTR	10			ns
/CS Deselect Time (for Self-timed instructions (7) → Read Status Register, Read Status Register → Read Status Register)	$t_{SHSL}2$	t_{CSH}	STR/DTR	50			ns
Output Disable Time	t_{SHQZ} (2)	t_{DIS}	STR/DTR			7	ns
Clock Low to Output Valid	t_{CLQV}	t_V	STR/DTR			6	ns
Clock High to Output Valid	t_{CHQV}		DTR only			6	ns
Output Hold Time	t_{CLQX}	t_{HO}	STR/DTR	1			ns
	t_{CHQX}		DTR only	1			
/HOLD Active Setup Time relative to CLK	t_{HLCH}		STR	3.375			ns
/HOLD Active Hold Time relative to CLK	t_{CHHH}		STR	3.375			ns
/HOLD Not Active Setup Time relative to CLK	t_{HHCH}		STR	3.375			ns
/HOLD Not Active Hold Time relative to CLK	t_{CHHL}		STR	3.375			ns
/HOLD to Output Low-Z	t_{HHQX} (2)	t_{LZ}	STR			7	ns

Continued – next page

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AC Electrical Characteristics (cont'd)

DESCRIPTION	SYMBOL	ALT	DATA TRANSFER RATE	SPEC			UNIT
				MIN	TYP	MAX	
/HOLD to Output High-Z	tHLQZ (2)	tHZ	STR			12	ns
Write Protect Setup Time Before /CS Low	tWHSL		STR/DTR	20			ns
Write Protect Hold Time After /CS High	tSHWL		STR/DTR	100			ns
Status Register Write Time	tW		STR/DTR			50	ns
Clock High to Deep Power-down	tDP		STR/DTR			10	µs
/CS High to Release Deep Power-down	tRES1		STR/DTR			1.5	ms
/CS High to next Instruction after Reset during Idle / Page Data Read / Program Execute / Block Erase / Built-in ECC Encode, Decode, Diagnostic	tRST (2) (3)		STR/DTR			0/5/10/ 500/6	µs
/RESET pin Low period to reset the device	tRESET (2)		STR/DTR	1			µs
Read Page Data Time (ECC disable)	tRD1 (3)		STR/DTR			25	µs
Read Page Data Time (ECC disabled and Buffer Read with Cache)	tRD1_BRC (3)		STR/DTR			10	µs
Read Page Data Time (ECC enable)	tRD2 (3)		STR/DTR		45	60	µs
Read Page Data Time (ECC enabled and Buffer Read with Cache)	tRD2_BRC (3)		STR/DTR		30	40	µs
Continuous Read Stop to Device Ready Time	tRDCR		STR/DTR	7		50	µs
Sequential Read Stop to Device Ready Time	tRDSR		STR/DTR			7	µs
Buffer Read with Cache Stop to Device Ready Time	tRDBRC		STR/DTR	0		25	µs
ECC Parity Calculation Time	tRDEPC		STR/DTR			75	µs
Page Program, OTP Lock and Bad Block Management Time (Built-in ECC disabled)	tPP1		STR/DTR		310	600	µs
Page Program and OTP Lock Time (Built-in ECC enabled)	tPP2		STR/DTR		350	600	µs
Page Program Time with Factory Program Mode (Built-in ECC disabled)	tPP1_FM (8)		STR/DTR		230	600	µs
Page Program Time with Factory Program Mode (Built-in ECC enabled)	tPP2_FM (8)		STR/DTR		270	600	µs
Block Erase Time	tBE		STR/DTR		3	10	ms
Built-in ECC Diagnostic Time	tED		STR/DTR		3	5	ms
Number of Partial Page Program operations	NoP		STR/DTR			4	Times

Notes:

1. Clock high + Clock low must be less than or equal to 1/fC.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. The product which re-loads page0 data after Reset takes tRST + tRD busy time.
4. The typical (TYP) value is tested on a sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.3V.
5. AC electrical characteristics are based on default setting of ODS.
6. Read means the following instructions: 03h, 0Bh, 3Bh, 6Bh, BBh, EBh, 0Dh, 6Dh, EDh.
7. Self-timed instructions mean the following instructions: A3h, A7h, ADh, D8h, 10h, 13h.
8. Please refer to 7.5.2 for detailed information.

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9.7 Serial Output Timing

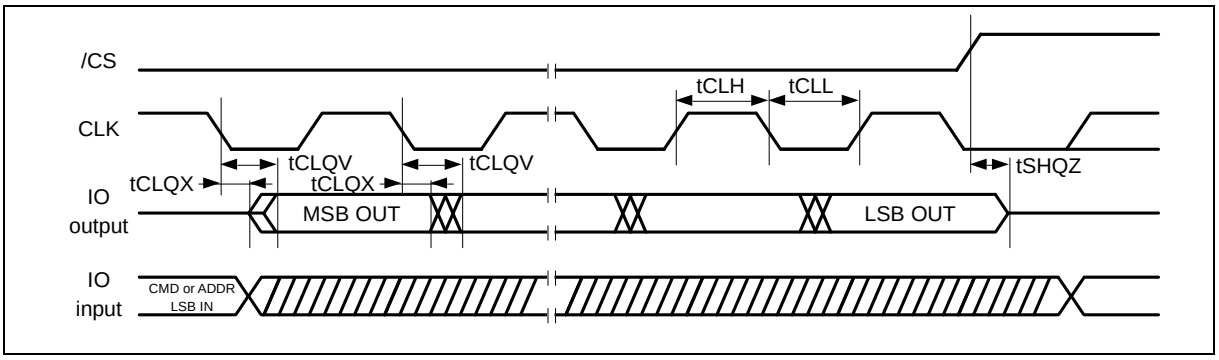


Figure 9-4 Serial Output Timing (STR)

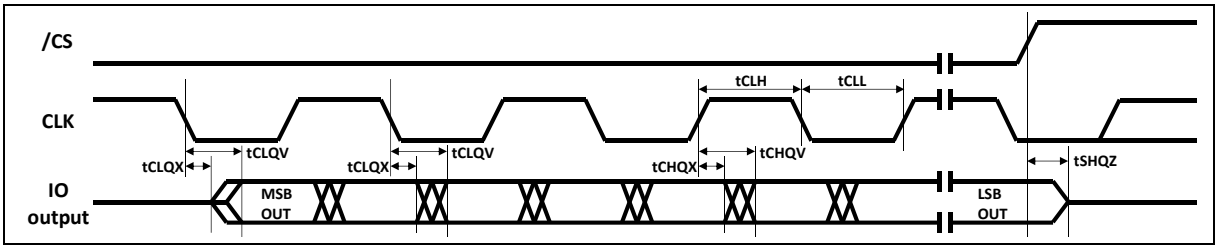


Figure 9-5 Serial Output Timing (DTR)

9.8 Serial Input Timing

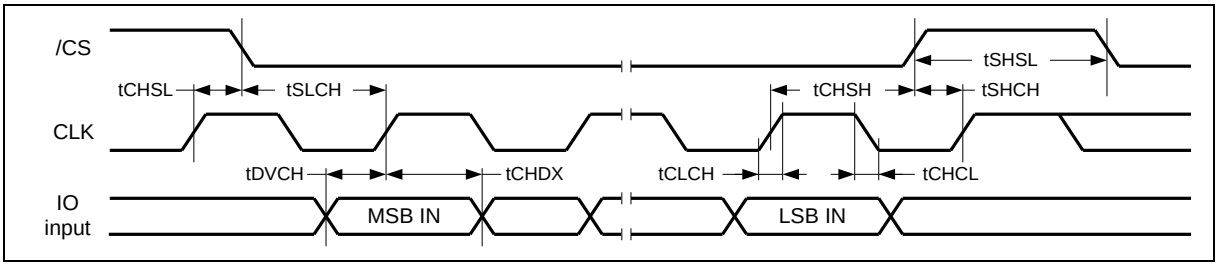


Figure 9-6 Serial Input Timing (STR)

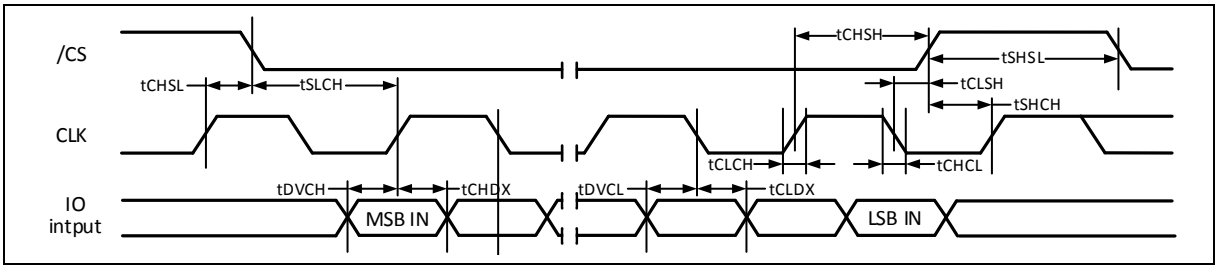


Figure 9-7 Serial Input Timing (DTR)

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9.9 /HOLD Timing

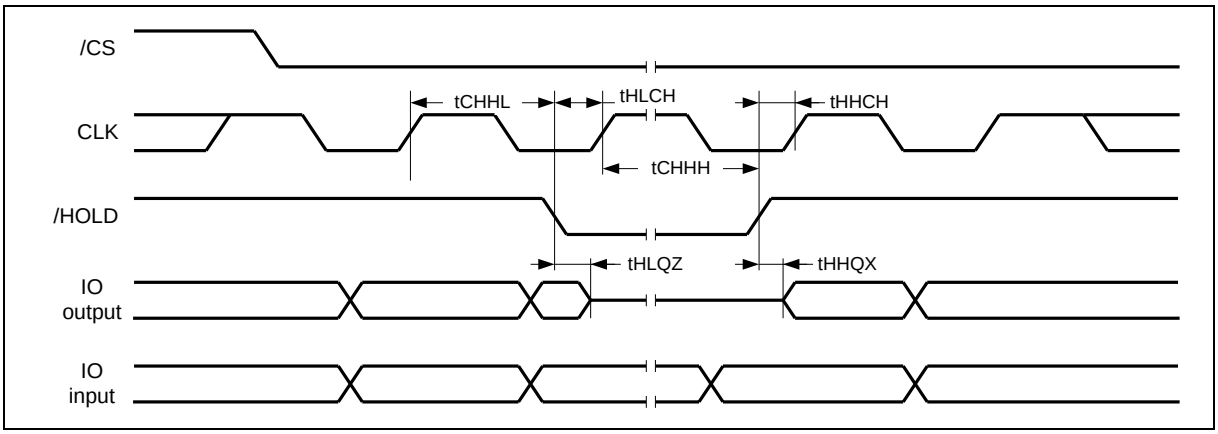


Figure 9-8 /HOLD Timing

9.10 /WP Timing

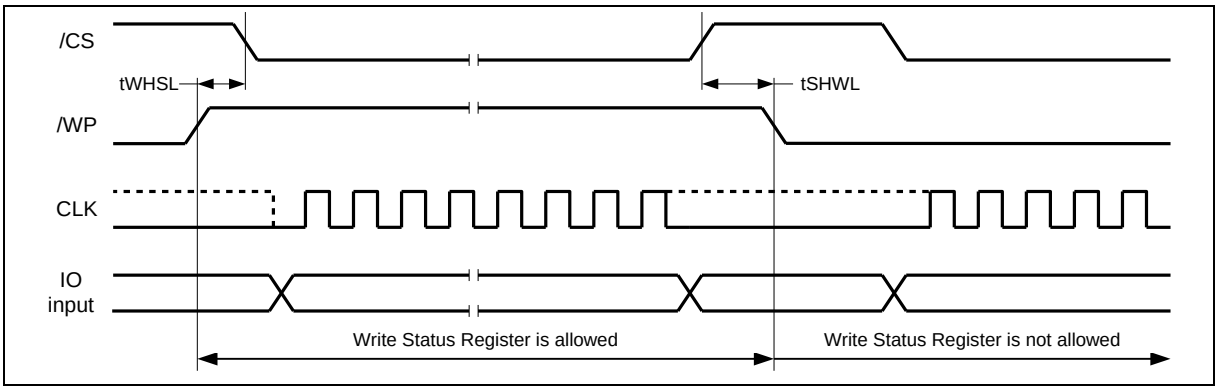


Figure 9-9 /WP Timing

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10. INVALID BLOCK MANAGEMENT

10.1 Invalid Blocks

The W25NxxLV may have initial invalid blocks when it ships from the factory. Also, additional invalid blocks may develop during the use of the device. Nvb represents the minimum number of valid blocks in the total number of available blocks. An invalid block is defined as blocks that contain Built-in ECC uncorrectable bad bits. The first eight blocks, block 0 to block 7 and the last four blocks, block 2044 to block 2047 are guaranteed to be valid blocks at the time of shipment with Built-in ECC enabled.

Parameter	Symbol	Min	Max	Unit
Valid block number	Nvb	2008	2048	blocks

10.2 Initial Invalid Blocks

Initial invalid blocks are defined as blocks that contain uncorrectable bits when shipped from the factory.

Although the device contains initial invalid blocks, a valid block of the device is of the same quality and reliability as all valid blocks in the device with reference to AC and DC specifications. The W25NxxLV has internal circuits to isolate each block from other blocks and therefore, the invalid blocks will not affect the performance of the entire device.

Before the device is shipped from the factory, it will be erased, and invalid blocks are permanently marked. The mark information cannot be erased. All initial invalid blocks are marked with non-FFh at the 1st byte of main array and the 1st byte of spare area on the 1st page. It should be checked for invalid blocks by reading the marked locations and creating a table of initial invalid blocks as shown in the following flow chart.

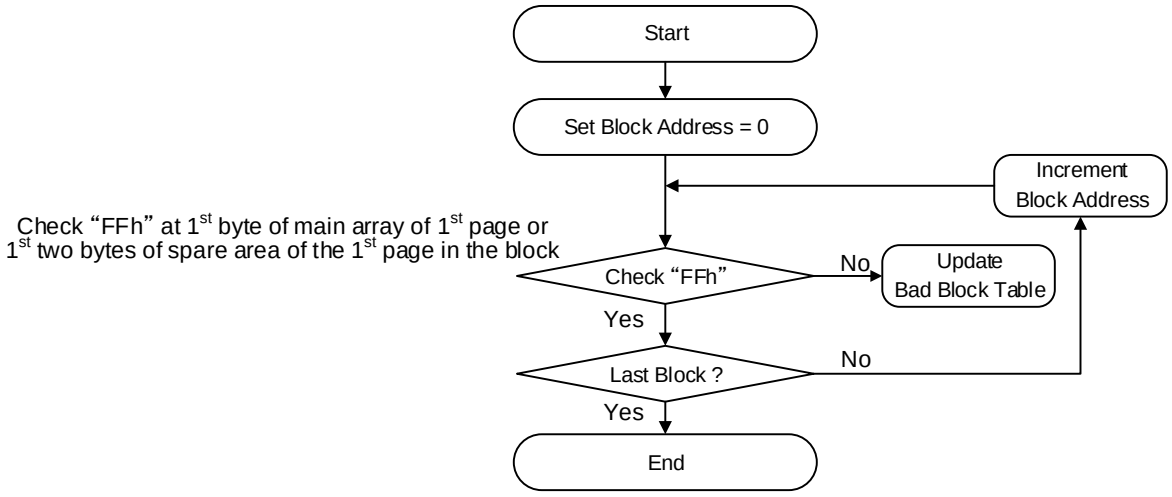


Figure 10-1 Flow Chart to Create Initial Invalid Block Table

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10.3 Error in Operation

Additional invalid blocks may develop in the device during its life cycle. Following the procedure herein is required to guarantee reliable data in the device.

After each program and erase operation, check the status read to determine if the operation failed. In case of failure, a block replacement should be done with a bad-block management algorithm. The system has to use a minimum 8-bit ECC per 544 bytes of data to ensure data recovery.

Operation	Detection and recommended procedure
Erase	Status read after erase → Block replacement
Program	Status read after program → Block replacement
Read	Verify ECC → ECC correction

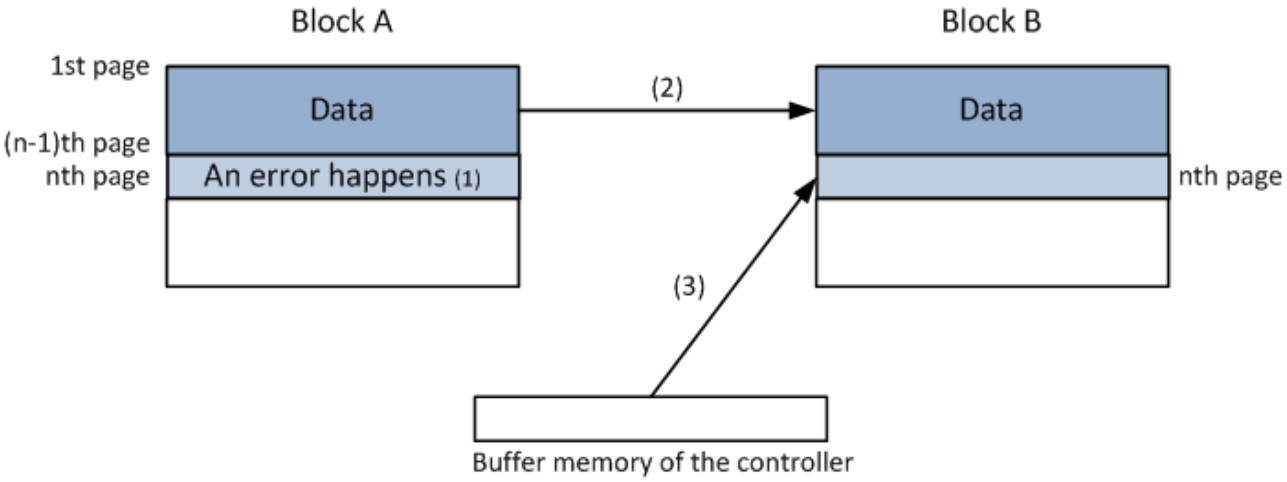


Figure 10-2 Bad Block Replacement

Notes:

1. An error happens in the nth page of block A during a program or erase operation.
2. Copy the data in block A to the same location of block B which is a valid block.
3. Copy the nth page data of block A in the buffer memory to the nth page of block B.
4. Creating or updating the bad block table prevents further program or erase operations to block A.

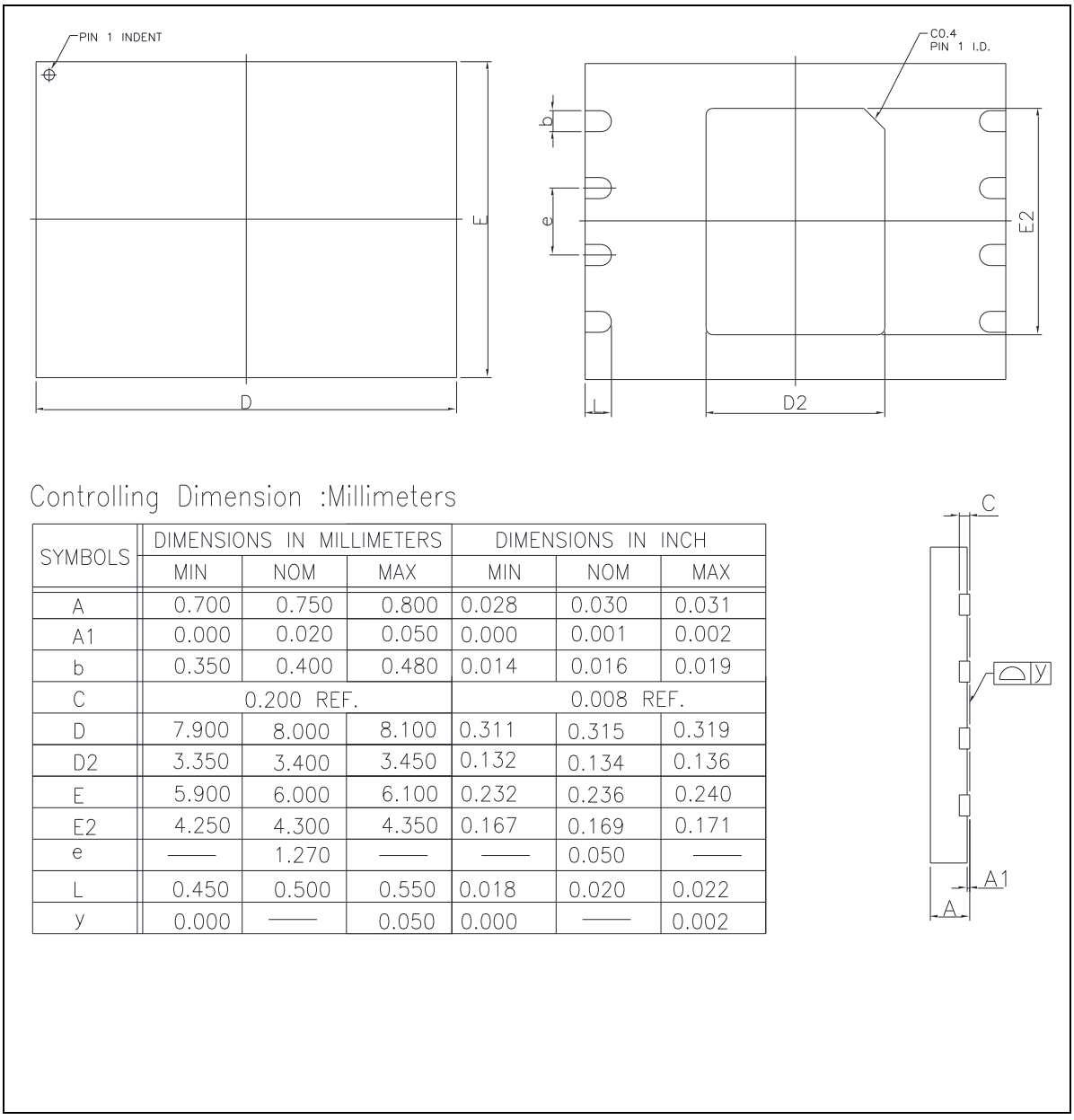
10.4 Addressing in Program Operation

The pages within the block have to be programmed sequentially from the LSB (least significant bit) page to the MSB (most significant bit) within the block. The LSB is defined as the start page to program. It does not need to be page 0 in the block. Random page programming is prohibited.

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11. PACKAGE SPECIFICATIONS

11.1 8-Pad WSON 8x6-mm (Package Code CE)



Controlling Dimension :Millimeters

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	0.000	0.020	0.050	0.000	0.001	0.002
b	0.350	0.400	0.480	0.014	0.016	0.019
C	0.200 REF.			0.008 REF.		
D	7.900	8.000	8.100	0.311	0.315	0.319
D2	3.350	3.400	3.450	0.132	0.134	0.136
E	5.900	6.000	6.100	0.232	0.236	0.240
E2	4.250	4.300	4.350	0.167	0.169	0.171
e	——	1.270	——	——	0.050	——
L	0.450	0.500	0.550	0.018	0.020	0.022
y	0.000	——	0.050	0.000	——	0.002

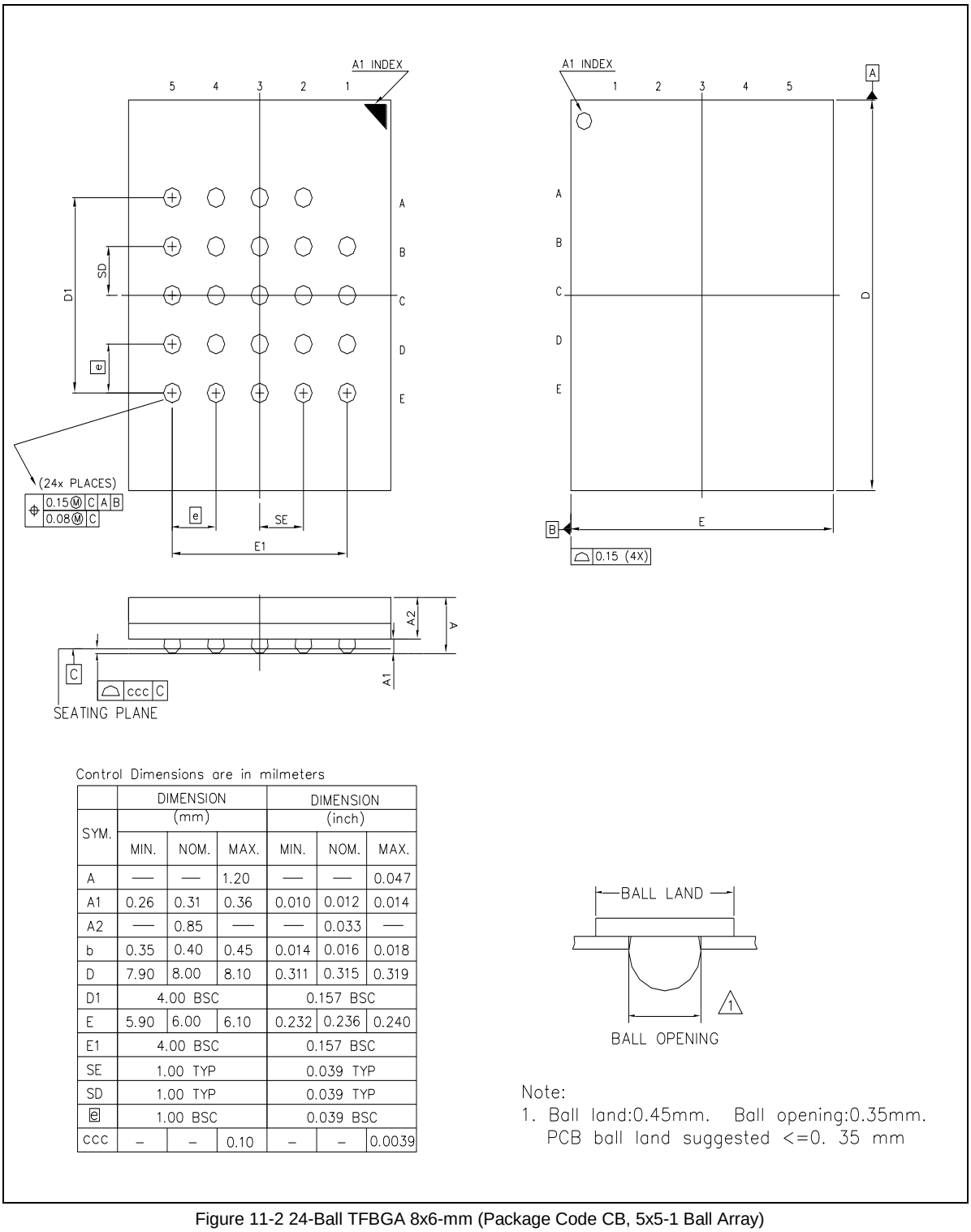
Figure 11-1 8-Pad WSON 8x6-mm (Package Code CE)

Notes:

1. The metal pad area on the bottom center of the package is not connected to any internal electrical signals. It can be left floating or connected to the device ground (GND pin). Avoid placement of exposed PCB vias under the pad.

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11.2 24-Ball TFBGA 8x6-mm (Package Code CB, 5x5-1 Ball Array)



Control Dimensions are in milmeters

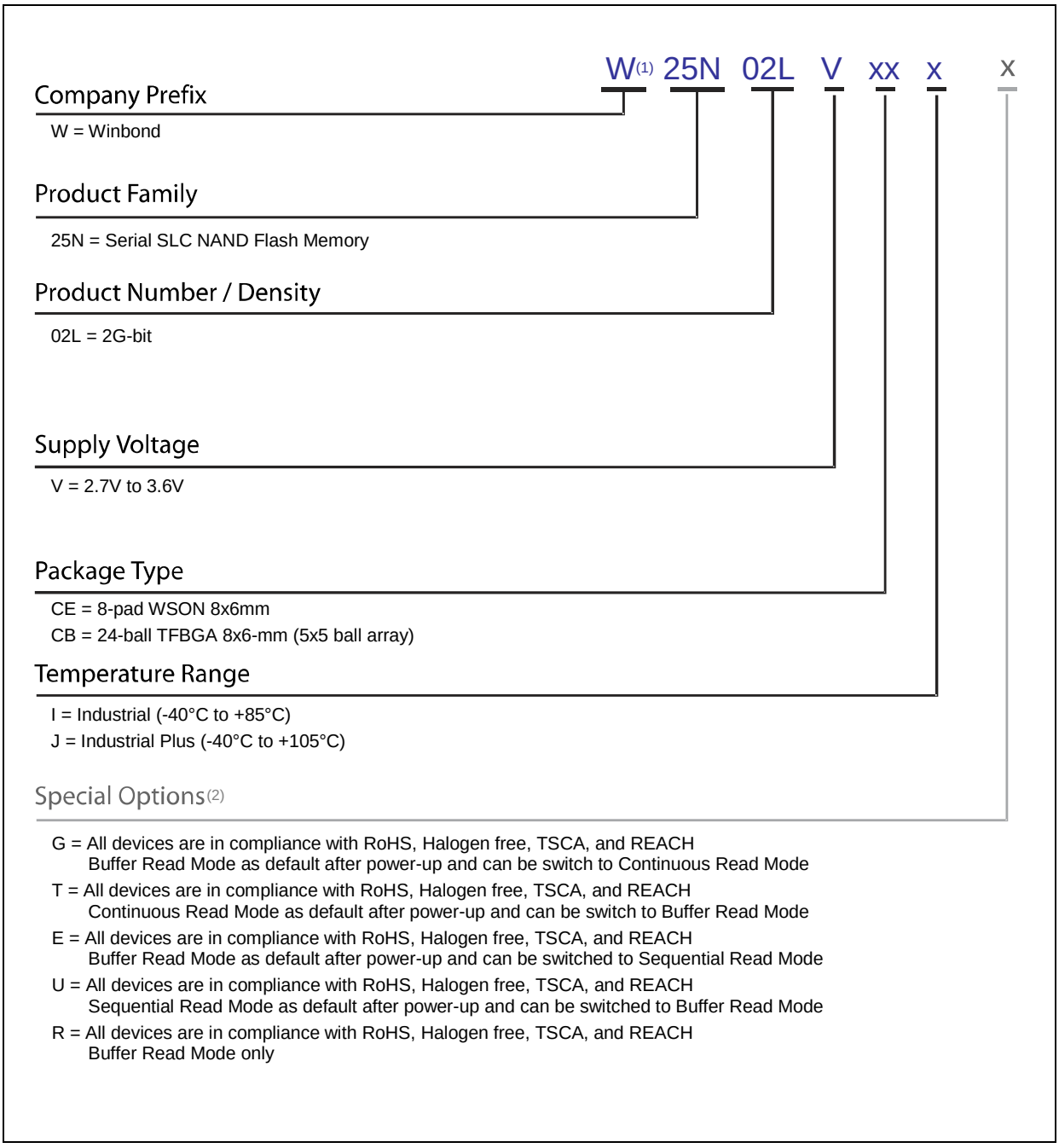
SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.26	0.31	0.36	0.010	0.012	0.014
A2	—	0.85	—	—	0.033	—
b	0.35	0.40	0.45	0.014	0.016	0.018
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	4.00 BSC			0.157 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	4.00 BSC			0.157 BSC		
SE	1.00 TYP			0.039 TYP		
SD	1.00 TYP			0.039 TYP		
e	1.00 BSC			0.039 BSC		
ccc	–	–	0.10	–	–	0.0039

Note:
1. Ball land:0.45mm. Ball opening:0.35mm. PCB ball land suggested <=0. 35 mm

Figure 11-2 24-Ball TFBGA 8x6-mm (Package Code CB, 5x5-1 Ball Array)

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12. ORDERING INFORMATION



Notes:

1. The "W" prefix is not included on the part marking.
2. Standard bulk shipments are in tray for WSON and TFBGA packages. For other packing options, please specify when placing orders.

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12.1 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the W25NxxLV SpiFlash Memory. Please contact Winbond for specific availability by density and package type. Winbond SpiFlash memories use a 12-digit Product Number for ordering. However, due to limited space, the Top Side Marking on all packages uses an abbreviated 11-digit number.

Industrial Grade:

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
CE WSON-8 8x6mm	2G-bit	W25N02LVCEIG W25N02LVCEIT W25N02LVCEIE W25N02LVCEIU W25N02LVCEIR	25N02LVCEIG 25N02LVCEIT 25N02LVCEIE 25N02LVCEIU 25N02LVCEIR
CB TFBGA-24 8x6mm (5x5-1 Ball Array)	2G-bit	W25N02LVCBIG W25N02LVCBIT W25N02LVCBIE W25N02LVCBIU W25N02LVCBIR	25N02LVCBIG 25N02LVCBIT 25N02LVCBIE 25N02LVCBIU 25N02LVCBIR

Industrial Plus Grade:

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
CE WSON-8 8x6mm	2G-bit	W25N02LVCEJG W25N02LVCEJT W25N02LVCEJE W25N02LVCEJU W25N02LVCEJR	25N02LVCEJG 25N02LVCEJT 25N02LVCEJE 25N02LVCEJU 25N02LVCEJR
CB TFBGA-24 8x6mm (5x5-1 Ball Array)	2G-bit	W25N02LVCBJG W25N02LVCBJT W25N02LVCBJE W25N02LVCBJU W25N02LVCBJR	25N02LVCBJG 25N02LVCBJT 25N02LVCBJE 25N02LVCBJU 25N02LVCBJR

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13. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.1	2025-11-04		New Create as Preliminary
0.2	2025-12-26	6, 64, 66, 76, 77 69 69	Added Industrial Plus Grade Removed Bad Block Management from the definition of tPP2 Added max values for tPP1_FM and tPP2_FM
0.3	2026-01-23	18, 20, 21, 35 21 24 33 62 69	Changed shipment default value for BRC-E Added explanation about tRDBRC Added Buffer Read with Cache as a condition for BUSY=1 Added note for tRDBRC Added BRC-E to the description for Read operation with OTP-E Added tRDBRC with min and max values
A	2026-03-24	 32	Removed Preliminary Corrected Instruction Set Table

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