STM8S103F2 STM8S103F3 STM8S103K3

Access line, 16 MHz STM8S 8-bit MCU, up to 8 Kbytes Flash, data EEPROM,10-bit ADC, 3 timers, UART, SPI, I²C

Datasheet - production data

Features

Core

- 16 MHz advanced STM8 core with Harvard architecture and 3-stage pipeline
- Extended instruction set

Memories

- Program memory: 8 Kbyte Flash; data retention 20 years at 55 °C after 10 kcycle
- Data memory: 640 byte true data EEPROM; endurance 300 kcycle
- RAM: 1 Kbyte

Clock, reset and supply management

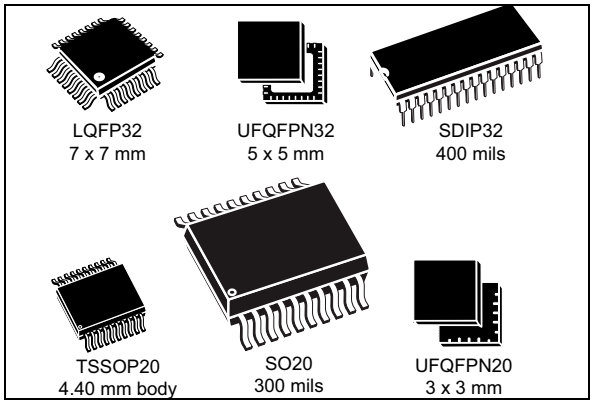
- 2.95 to 5.5 V operating voltage
- Flexible clock control, 4 master clock sources
  - Low power crystal resonator oscillator
  - External clock input
  - Internal, user-trimmable 16 MHz RC
  - Internal low-power 128 kHz RC
- Clock security system with clock monitor
- Power management:
  - Low-power modes (wait, active-halt, halt)
  - Switch-off peripheral clocks individually
- Permanently active, low-consumption power-on and power-down reset

Interrupt management

- Nested interrupt controller with 32 interrupts
- Up to 27 external interrupts on 6 vectors

Timers

- Advanced control timer: 16-bit, 4 CAPCOM channels, 3 complementary outputs, dead-time insertion and flexible synchronization



- 16-bit general purpose timer, with 3 CAPCOM channels (IC, OC or PWM)
- 8-bit basic timer with 8-bit prescaler
- Auto wake-up timer
- Window watchdog and independent watchdog timers

Communication interfaces

- UART with clock output for synchronous operation, SmartCard, IrDA, LIN master mode
- SPI interface up to 8 Mbit/s
- I2C interface up to 400 kbit/s

Analog to digital converter (ADC)

- 10-bit, ±1 LSB ADC with up to 5 multiplexed channels, scan mode and analog watchdog

I/Os

- Up to 28 I/Os on a 32-pin package including 21 high sink outputs
- Highly robust I/O design, immune against current injection

Unique ID

- 96-bit unique key for each device

This is information on a product in full production. www.st.com

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Contents

1 Introduction 9

2 Description 10

3 Block diagram 11

4 Product overview 12

4.1 Central processing unit STM8 12

4.2 Single wire interface module (SWIM) and debug module (DM) 13

4.3 Interrupt controller 13

4.4 Flash program and data EEPROM memory 13

4.5 Clock controller 15

4.6 Power management 16

4.7 Watchdog timers 16

4.8 Auto wakeup counter 17

4.9 Beeper 17

4.10 TIM1 - 16-bit advanced control timer 17

4.11 TIM2 - 16-bit general purpose timer 17

4.12 TIM4 - 8-bit basic timer 18

4.13 Analog-to-digital converter (ADC1) 18

4.14 Communication interfaces 18

4.14.1 UART1 19

4.14.2 SPI 19

4.14.3 I^2C 20

5 Pinout and pin description 21

5.1 STM8S103K3 UFQFPN32/LQFP32/SDIP32 pinout and pin description 22

5.2 STM8S103F2/F3 TSSOP20/SO20/UFQFPN20 pinout and pin description 26

5.2.1 STM8S103F2/F3 TSSOP20/SO20 pinout 26

5.2.2 STM8S103F2/F3 UFQFPN20 pinout 27

5.3 Alternate function remapping 30

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6 Memory and register map 31

6.1 Memory map 31

6.2 Register map 32

6.2.1 I/O port hardware register map 32

6.2.2 General hardware register map 33

6.2.3 CPU/SWIM/debug module/interrupt controller registers 41

7 Interrupt vector mapping 43

8 Option byte 45

8.1 Alternate function remapping bits 47

9 Unique ID 49

10 Electrical characteristics 50

10.1 Parameter conditions 50

10.1.1 Minimum and maximum values 50

10.1.2 Typical values 50

10.1.3 Typical curves 50

10.1.4 Loading capacitor 50

10.1.5 Pin input voltage 50

10.2 Absolute maximum ratings 51

10.3 Operating conditions 52

10.3.1 VCAP external capacitor 55

10.3.2 Supply current characteristics 55

10.3.3 External clock sources and timing characteristics 64

10.3.4 Internal clock sources and timing characteristics 67

10.3.5 Memory characteristics 69

10.3.6 I/O port pin characteristics 70

10.3.7 Reset pin characteristics 75

10.3.8 SPI serial peripheral interface 77

10.3.9 I^2C interface characteristics 81

10.3.10 10-bit ADC characteristics 82

10.3.11 EMC characteristics 86

11 Package information 89

11.1 LQFP32 package information 89

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Email:sales@manduic.com

11.2 UFQFPN32 package information 92
11.3 UFQFPN20 package information 95
11.4 SDIP32 package information 98
11.5 TSSOP20 package information 100
11.6 SO20 package information 103
11.7 UFQFPN recommended footprint 104

12 Thermal characteristics 106
12.1 Reference document 106
12.2 Selecting the product temperature range 107

13 Ordering information 108
13.1 STM8S103 FASTROM microcontroller option list 109

14 STM8 development tools 113
14.1 Emulation and in-circuit debugging tools 113
14.1.1 STice key features 113
14.2 Software tools 114
14.2.1 STM8 toolset 114
14.2.2 C and assembly toolchains 114
14.3 Programming tools 115

15 Revision history 116

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List of tables

Table 1. STM8S103F2/x3 access line features . . . 10
Table 2. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers . . . 15
Table 3. TIM timer features . . . 18
Table 4. Legend/abbreviations for pin description tables . . . 21
Table 5. STM8S103K3 pin descriptions . . . 23
Table 6. STM8S103F2 and STM8S103F3 pin descriptions . . . 28
Table 7. I/O port hardware register map . . . 32
Table 8. General hardware register map . . . 33
Table 9. CPU/SWIM/debug module/interrupt controller registers . . . 41
Table 10. Interrupt mapping . . . 43
Table 11. Option byte . . . 45
Table 12. Option byte description . . . 46
Table 13. STM8S103K3 alternate function remapping bits for 32-pin devices . . . 47
Table 14. STM8S103Fx alternate function remapping bits for 20-pin devices . . . 48
Table 15. Unique ID registers (96 bits) . . . 49
Table 16. Voltage characteristics . . . 51
Table 17. Current characteristics . . . 51
Table 18. Thermal characteristics . . . 52
Table 19. General operating conditions . . . 52
Table 20. Operating conditions at power-up/power-down . . . 53
Table 21. Total current consumption with code execution in run mode at V_{DD} = 5 V . . . 55
Table 22. Total current consumption with code execution in run mode at V_{DD} = 3.3 V . . . 56
Table 23. Total current consumption in wait mode at V_{DD} = 5 V . . . 57
Table 24. Total current consumption in wait mode at V_{DD} = 3.3 V . . . 57
Table 25. Total current consumption in active halt mode at V_{DD} = 5 V . . . 58
Table 26. Total current consumption in active halt mode at V_{DD} = 3.3 V . . . 58
Table 27. Total current consumption in halt mode at V_{DD} = 5 V . . . 59
Table 28. Total current consumption in halt mode at V_{DD} = 3.3 V . . . 59
Table 29. Wakeup times . . . 59
Table 30. Total current consumption and timing in forced reset state . . . 60
Table 31. Peripheral current consumption . . . 60
Table 32. HSE user external clock characteristics . . . 64
Table 33. HSE oscillator characteristics . . . 65
Table 34. HSI oscillator characteristics . . . 67
Table 35. LSI oscillator characteristics . . . 68
Table 36. RAM and hardware registers . . . 69
Table 37. Flash program memory/data EEPROM memory . . . 69
Table 38. I/O static characteristics . . . 70
Table 39. Output driving current (standard ports) . . . 71
Table 40. Output driving current (true open drain ports) . . . 72
Table 41. Output driving current (high sink ports) . . . 72
Table 42. NRST pin characteristics . . . 75
Table 43. SPI characteristics . . . 77
Table 44. I^2C characteristics . . . 81
Table 45. ADC characteristics . . . 82
Table 46. ADC accuracy with R_{AIN}< 10 kΩ, V_{DD}= 5 V . . . 83
Table 47. ADC accuracy with R_{AIN}< 10 kΩ, V_{DD}= 3.3 V . . . 84
Table 48. EMS data . . . 86

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Table 49. EMI data . . . 87
Table 50. ESD absolute maximum ratings . . . 87
Table 51. Electrical sensitivities . . . 88
Table 52. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data. . . . 90
Table 53. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data . . . 93
Table 54. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data . . . 95
Table 55. SDIP32 package mechanical data . . . 98
Table 56. TSSOP20 package mechanical data . . . 100
Table 57. SO20 mechanical data . . . 103
Table 58. Thermal characteristics . . . 106
Table 59. Document revision history . . . 116

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List of figures

Figure 1. STM8S103F2/x3 block diagram . . . 11
Figure 2. Flash memory organization . . . 14
Figure 3. STM8S103K3 UFQFPN32/LQFP32 pinout . . . 22
Figure 4. STM8S103K3 SDIP32 pinout . . . 23
Figure 5. STM8S103F2/F3 TSSOP20/SO20 pinout . . . 26
Figure 6. STM8S103F2/F3 UFQFPN20-pin pinout . . . 27
Figure 7. Memory map . . . 31
Figure 8. Pin loading conditions . . . 50
Figure 9. Pin input voltage . . . 51
Figure 10. f_{CPUmax} versus V_{DD} . . . 53
Figure 11. External capacitor C_{EXT} . . . 55
Figure 12. Typ $I_{DD(RUN)}$ vs. V_{DD} HSE user external clock, f_{CPU} = 16 MHz . . . 61
Figure 13. Typ $I_{DD(RUN)}$ vs. f_{CPU} HSE user external clock, V_{DD} = 5 V . . . 61
Figure 14. Typ $I_{DD(RUN)}$ vs. V_{DD} HSI RC osc, f_{CPU} = 16 MHz . . . 62
Figure 15. Typ $I_{DD(WFI)}$ vs. V_{DD} HSE external clock, f_{CPU} = 16 MHz . . . 62
Figure 16. Typ $I_{DD(WFI)}$ vs. f_{CPU} HSE external clock, V_{DD} = 5 V . . . 63
Figure 17. Typ $I_{DD(WFI)}$ vs. V_{DD} HSI RC osc., f_{CPU} = 16 MHz . . . 63
Figure 18. HSE external clock source . . . 64
Figure 19. HSE oscillator circuit diagram . . . 66
Figure 20. Typical HSI frequency variation vs V_{DD} @ 4 temperatures . . . 67
Figure 21. Typical LSI frequency variation vs V_{DD}@ 4 temperatures . . . 68
Figure 22. Typical V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures . . . 71
Figure 23. Typical pull-up current vs V_{DD} @ 4 temperatures . . . 71
Figure 24. Typical pull-up resistance vs VDD @ 4 temperatures . . . 71
Figure 25. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports) . . . 72
Figure 26. Typ. V_{OL} @ V_{DD} = 5.0 V (standard ports) . . . 72
Figure 27. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports) . . . 73
Figure 28. Typ. V_{OL} @ V_{DD} = 5.0 V (true open drain ports) . . . 73
Figure 29. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports) . . . 73
Figure 30. Typ. V_{OL} @ V_{DD} = 5.0 V (high sink ports) . . . 73
Figure 31. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports) . . . 74
Figure 32. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (standard ports) . . . 74
Figure 33. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports) . . . 74
Figure 34. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (high sink ports) . . . 74
Figure 35. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures . . . 75
Figure 36. Typical NRST pull-up resistance R_{PU} vs V_{DD} @ 4 temperatures . . . 76
Figure 37. Typical NRST pull-up current I_{pu} vs V_{DD} @ 4 temperatures . . . 76
Figure 38. Recommended reset pin protection . . . 77
Figure 39. SPI timing diagram where slave mode and CPHA = 0 . . . 79
Figure 40. SPI timing diagram where slave mode and CPHA = 1 . . . 79
Figure 41. SPI timing diagram - master mode . . . 80
Figure 42. Typical application with I^2C bus and timing diagram . . . 81
Figure 43. ADC accuracy characteristics . . . 84
Figure 44. Typical application with ADC . . . 85
Figure 45. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline . . . 89
Figure 46. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint . . . 90
Figure 47. LQFP32 marking example (package top view) . . . 91
Figure 48. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat

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package outline . . . 92
Figure 49. UFQFPN32 - 32-pin, 5 x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package recommended footprint . . . 93
Figure 50. UFQFPN32 marking example (package top view) . . . 94
Figure 51. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline . . . 95
Figure 52. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint . . . 96
Figure 53. UFQFPN20 marking example (package top view) . . . 97
Figure 54. SDIP32 package outline . . . 98
Figure 55. SDIP32 marking example (package top view) . . . 99
Figure 56. TSSOP20 package outline . . . 100
Figure 57. TSSOP20 recommended package footprint . . . 101
Figure 58. TSSOP20 marking example (package top view) . . . 102
Figure 59. SO20 package outline . . . 103
Figure 60. SO20 marking example (package top view) . . . 104
Figure 61. UFQFPN recommended footprint for on-board emulation . . . 104
Figure 62. UFQFPN recommended footprint without on-board emulation . . . 105
Figure 63. STM8S103F2/x3 access line ordering information scheme(1) . . . 108

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1 Introduction

This datasheet contains the description of the device features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S microcontroller family reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

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2 Description

The STM8S103F2/x3 access line 8-bit microcontrollers offer 8 Kbyte Flash program memory, plus integrated true data EEPROM. The STM8S microcontroller family reference manual (RM0016) refers to devices in this family as low-density. They provide the following benefits: performance, robustness, and reduced system cost.

Device performance and robustness are ensured by advanced core and peripherals made in a state-of-the art technology, a 16 MHz clock frequency, robust I/Os, independent watchdogs with separate clock source, and a clock security system.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 k write/erase cycles and a high system integration level with internal clock oscillators, watchdog and brown-out reset.

Full documentation is offered as well as a wide choice of development tools.

Table 1. STM8S103F2/x3 access line features

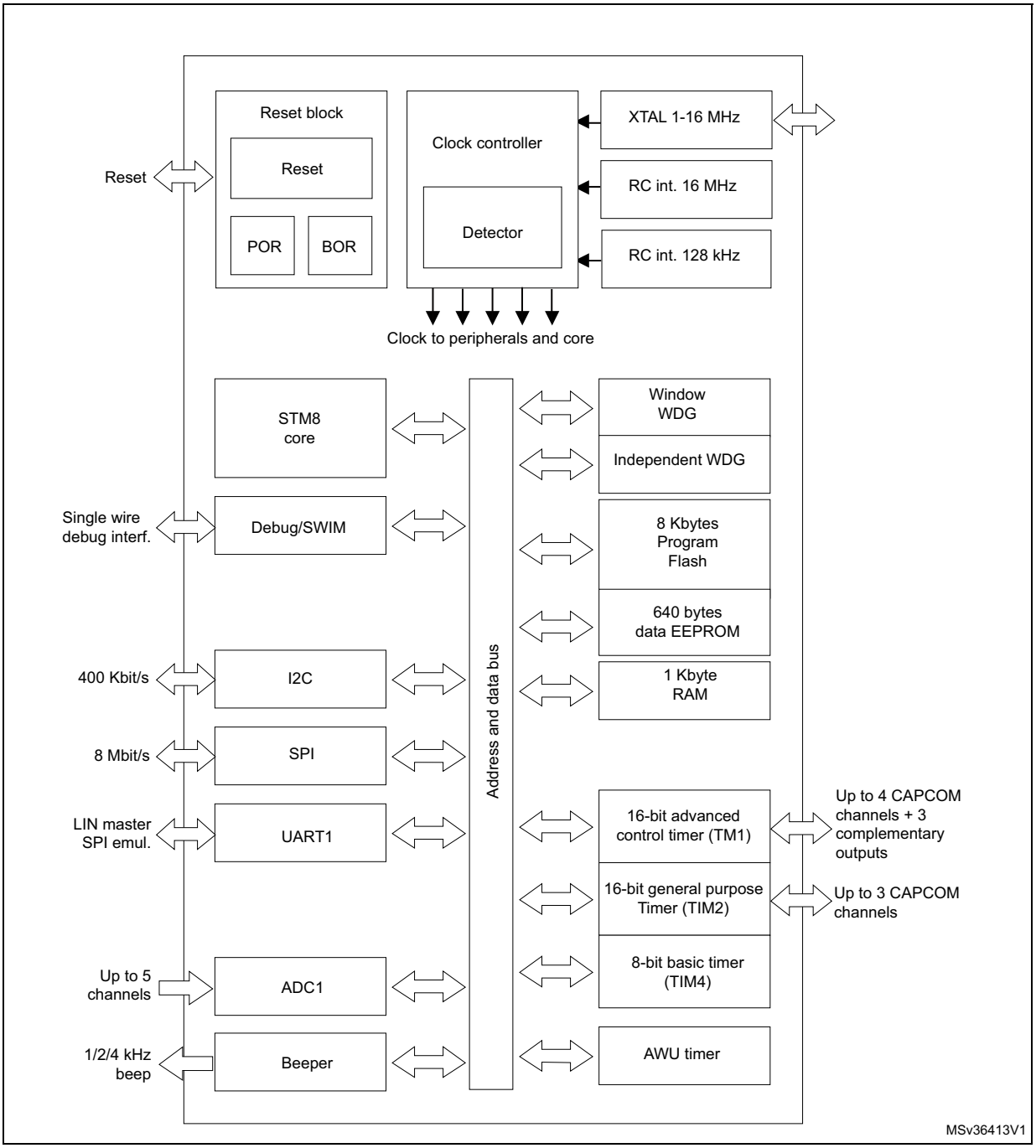
Device	STM8S103K3	STM8S103F3	STM8S103F2
Pin count	32	20	20
Maximum number of GPIOs (I/Os)	28	16	16
Ext. interrupt pins	27	16	16
Timer CAPCOM channels	7	7	7
Timer complementary outputs	3	2	2
A/D converter channels	4	5	5
High sink I/Os	21	12	12
Low density Flash program memory (bytes)	8K	8K	4K
Data EEPROM (bytes)	640(1)	640(1)	640(1)
RAM (bytes)	1K	1K	1K
Peripheral set	Multipurpose timer (TIM1), SPI, I2C, UART window WDG, independent WDG, ADC, PWM timer (TIM2), 8-bit timer (TIM4)		

1. No read-while-write (RWW) capability.

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3 Block diagram

Figure 1. STM8S103F2/x3 block diagram



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4 Product overview

The following section provides an overview of the basic features of the device functional modules and peripherals.

For more detailed information please refer to the corresponding family reference manual (RM0016).

4.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

Architecture and registers

- Harvard architecture,
- 3-stage pipeline,
- 32-bit wide program memory bus - single cycle fetching for most instructions,
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations,
- 8-bit accumulator,
- 24-bit program counter - 16-Mbyte linear memory space,
- 16-bit stack pointer - access to a 64 K-level stack,
- 8-bit condition code register - 7 condition flags for the result of the last instruction.

Addressing

- 20 addressing modes,
- Indexed indirect addressing mode for look-up tables located anywhere in the address space,
- Stack pointer relative addressing mode for local variables and parameter passing.

Instruction set

- 80 instructions with 2-byte average instruction size,
- Standard data movement and logic/arithmetic functions,
- 8-bit by 8-bit multiplication,
- 16-bit by 8-bit and 16-bit by 16-bit division,
- Bit manipulation,
- Data transfer between stack and accumulator (push/pop) with direct stack access,
- Data transfer using the X and Y registers or direct memory-to-memory transfers.

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4.2 Single wire interface module (SWIM) and debug module (DM)

The single wire interface module and debug module permits non-intrusive, real-time in-circuit debugging and fast memory programming.

SWIM

Single wire interface module for direct access to the debug module and memory programming. The interface can be activated in all device operation modes. The maximum data transmission speed is 145 bytes/ms.

Debug module

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

- R/W to RAM and peripheral registers in real-time
- R/W access to all resources by stalling the CPU
- Breakpoints on all program-memory instructions (software breakpoints)
- Two advanced breakpoints, 23 predefined configurations

4.3 Interrupt controller

- Nested interrupts with three software priority levels,
- 32 interrupt vectors with hardware priority,
- Up to 27 external interrupts on 6 vectors including TLI,
- Trap and reset interrupts

4.4 Flash program and data EEPROM memory

- 8 Kbyte of Flash program single voltage Flash memory,
- 640 byte true data EEPROM,
- User option byte area.

Write protection (WP)

Write protection of Flash program memory and data EEPROM is provided to avoid unintentional overwriting of memory that could result from a user software malfunction.

There are two levels of write protection. The first level is known as MASS (memory access security system). MASS is always enabled and protects the main Flash program memory, data EEPROM and option bytes.

To perform in-application programming (IAP), this write protection can be removed by writing a MASS key sequence in a control register. This allows the application to write to data EEPROM, modify the contents of main program memory or the device option bytes.

A second level of write protection, can be enabled to further protect a specific area of memory known as UBC (user boot code). Refer to the figure below.

The size of the UBC is programmable through the UBC option byte, in increments of 1 page (64-byte block) by programming the UBC option byte in ICP mode.

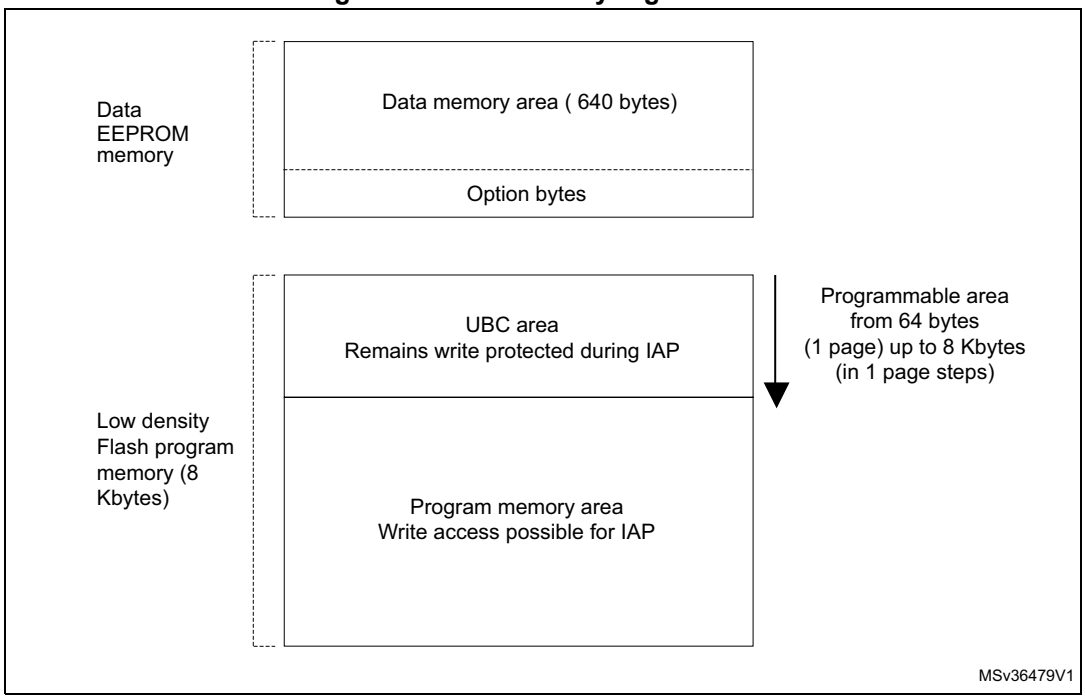
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This divides the program memory into two areas:

- Main program memory: up to 8 Kbyte minus UBC
- User-specific boot code (UBC): Configurable up to 8 Kbyte

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2. Flash memory organization



Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

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4.5 Clock controller

The clock controller distributes the system clock (fMASTER) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock sources:** four different clock sources can be used to drive the master clock:
  - 1-16 MHz high-speed external crystal (HSE)
  - Up to 16 MHz high-speed user-external clock (HSE user-ext)
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS and an interrupt can optionally be generated.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

Table 2. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers

Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock
PCKEN17	TIM1	PCKEN13	UART1	PCKEN27	Reserved	PCKEN23	ADC
PCKEN16	Reserved	PCKEN12	Reserved	PCKEN26	Reserved	PCKEN22	AWU
PCKEN15	TIM2	PCKEN11	SPI	PCKEN25	Reserved	PCKEN21	Reserved
PCKEN14	TIM4	PCKEN10	I2C	PCKEN24	Reserved	PCKEN20	Reserved

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4.6 Power management

For efficient power management, the application can be put in one of four different low-power modes. You can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- **Wait mode:** In this mode, the CPU is stopped, but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- **Active halt mode with regulator on:** In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in active halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- **Active halt mode with regulator off:** This mode is the same as active halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- **Halt mode:** In this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: At 16 MHz CPU clock the time-out period can be adjusted between 75 µs up to 64 ms.
2. Refresh out of window: The downcounter is refreshed before its value is lower than the one stored in the window register.

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Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

The IWDG time base spans from 60 µs to 1 s.

4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode,
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock,
- LSI clock can be internally connected to TIM1 input capture channel 1 for calibration.

4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

The beeper output port is only available through the alternate function remap option bit AFR7.

4.10 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

4.11 TIM2 - 16-bit general purpose timer

- 16-bit auto reload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- 3 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update

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4.12 TIM4 - 8-bit basic timer

- 8-bit auto reload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update

Table 3. TIM timer features

Timer	Counter size (bits)	Prescaler	Counting mode	CAPCOM channels	Complementary outputs	Ext. trigger	Timer synchronization/ chaining
TIM1	16	Any integer from 1 to 65536	Up/down	4	3	Yes	No
TIM2	16	Any power of 2 from 1 to 32768	Up	3	0	No	
TIM4	8	Any power of 2 from 1 to 128	Up	0	0	No	

4.13 Analog-to-digital converter (ADC1)

The STM8S103F2/x3 family products contain a 10-bit successive approximation A/D converter (ADC1) with up to 5 external multiplexed input channels and the following main features:

- Input voltage range: 0 to VDD
- Conversion time: 14 clock cycles
- Single and continuous and buffered continuous conversion modes
- Buffer size (n x 10 bits) where n = number of input channels
- Scan mode for single and continuous conversion of a sequence of channels
- Analog watchdog capability with programmable upper and lower thresholds
- Analog watchdog interrupt
- External trigger input
- Trigger from TIM1 TRGO
- End of conversion (EOC) interrupt

4.14 Communication interfaces

The following communication interfaces are implemented:

- UART1: Full feature UART, synchronous mode, SPI master mode, Smartcard mode, IrDA mode, single wire mode, LIN2.1 master capability
- SPI: Full and half-duplex, 8 Mbit/s
- I²C: Up to 400 kbit/s

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4.14.1 UART1

Main features

- 1 Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- LIN master mode
- Single wire half duplex mode

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (fCPU/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz (fCPU/16)

LIN master mode

- Emission: Generates 13-bit synch. break frame
- Reception: Detects 11-bit break frame

4.14.2 SPI

- Maximum speed: 8 Mbit/s (fMASTER/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave/master selection input pin

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4.14.3 I²C

- I²C master features:
  - Clock generation
  - Start and stop generation
- I²C slave features:
  - Programmable I2C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz)
  - Fast speed (up to 400 kHz)

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5 Pinout and pin description

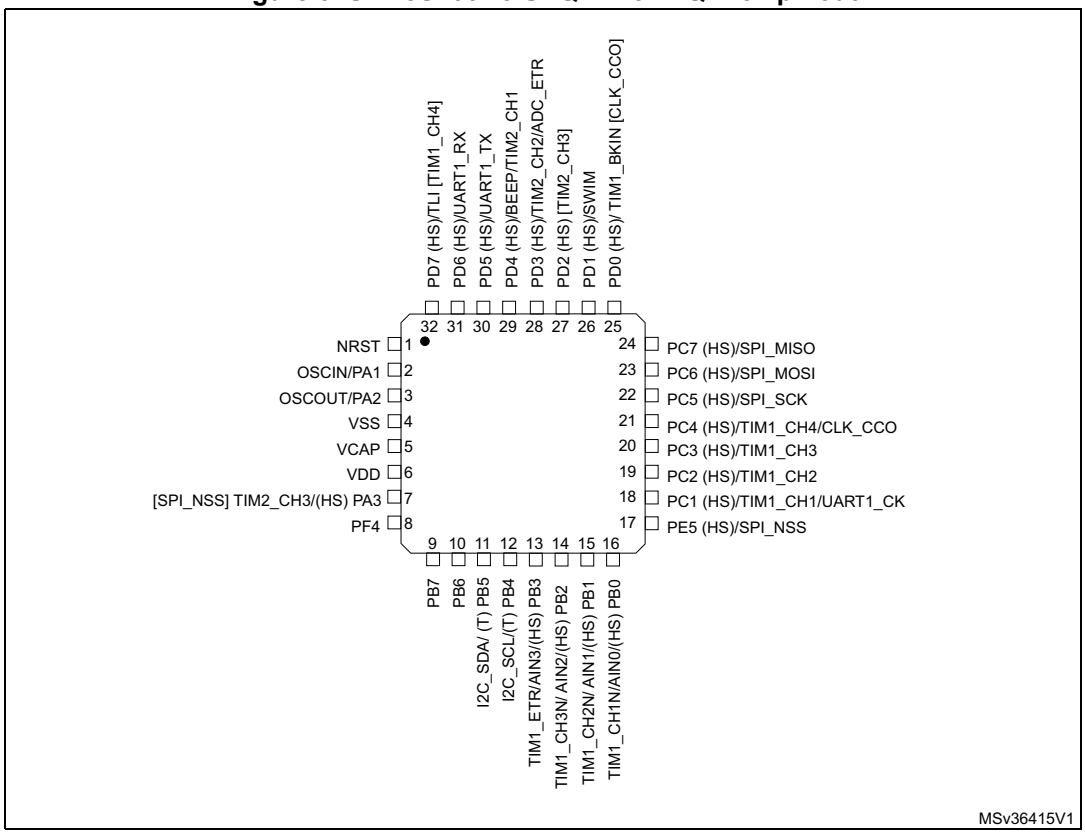
Table 4. Legend/abbreviations for pin description tables

Type	I= Input, O = Output, S = Power supply	
Level	Input	CM = CMOS
	Output	HS = High sink
Output speed	O1 = Slow (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = True open drain, OD = Open drain, PP = Push pull
Reset state	Bold **X** (pin state after internal reset release). Unless otherwise specified, the pin state is the same during the reset phase and after the internal reset release.	

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5.1 STM8S103K3 UFQFPN32/LQFP32/SDIP32 pinout and pin description

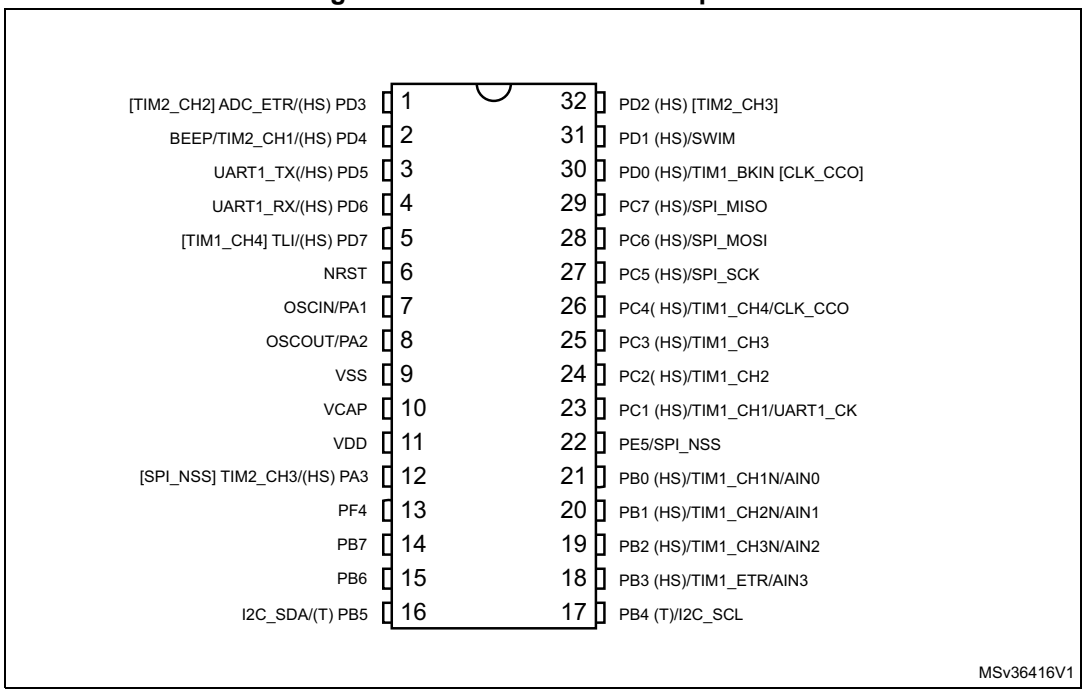
Figure 3. STM8S103K3 UFQFPN32/LQFP32 pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

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Figure 4. STM8S103K3 SDIP32 pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 5. STM8S103K3 pin descriptions

SDIP32	LQFP/ UFQFP32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
6	1	NRST	I/O	-	**X**	-	-	-	-	-	Reset		-
7	2	PA1/ OSCIN(2)	I/O	**X**	X	X	-	O1	X	X	Port A1	Resonator/ crystal in	-
8	3	PA2/ OSCOUT	I/O	**X**	X	X	-	O1	X	X	Port A2	Resonator/ crystal out	-
9	4	VSS	S	-	-	-	-	-	-	-	Digital ground		-
10	5	VCAP	S	-	-	-	-	-	-		1.8 V regulator capacitor		-
11	6	VDD	S	-	-	-	-	-	-	-	Digital power supply		-
12	7	PA3/ TIM2_CH3 [SPI_NSS]	I/O	**X**	X	X	HS	O3	X	X	Port A3	Timer 2 channel 3	SPI master/ slave select [AFR1]
13	8	PF4	I/O	**X**	X	-	-	O1	X	X	Port F4	-	-
14	9	PB7	I/O	**X**	X	X	-	O1	X	X	Port B7	-	-

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Table 5. STM8S103K3 pin descriptions (continued)

SDIP32	LQFP/ UFQFP32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
15	10	PB6	I/O	**X**	X	X	-	O1	X	X	Port B6	-	-
16	11	PB5/ I2C_SDA	I/O	**X**	-	X	-	O1	T(3)	-	Port B5	I2C data	-
17	12	PB4/ I2C_SCL	I/O	**X**	-	X	-	O1	T	-	Port B4	I2C clock	-
18	13	PB3/AIN3/ TIM1_ETR	I/O	**X**	X	X	HS	O3	X	X	Port B3	Analog input 3/ Timer 1 external trigger	-
19	14	PB2/AIN2/ TIM1_CH3N	I/O	**X**	X	X	HS	O3	X	X	Port B2	Analog input 2/ Timer 1 - inverted channel 3	-
20	15	PB1/AIN1/ TIM1_CH2N	I/O	**X**	X	X	HS	O3	X	X	Port B1	Analog input 1/ Timer 1 - inverted channel 2	-
21	16	PB0/AIN0/ TIM1_CH1N	I/O	**X**	X	X	HS	O3	X	X	Port B0	Analog input 0/ Timer 1 - inverted channel 1	-
22	17	PE5/SPI_NSS	I/O	**X**	X	X	HS	O3	X	X	Port E5	SPI master/slave select	-
23	18	PC1/ TIM1_CH1/ UART1_CK	I/O	**X**	X	X	HS	O3	X	X	Port C1	Timer 1 - channel 1 UART1 clock	-
24	19	PC2/ TIM1_CH2	I/O	**X**	X	X	HS	O3	X	X	Port C2	Timer 1 - channel 2	-
25	20	PC3/ TIM1_CH3	I/O	**X**	X	X	HS	O3	X	X	Port C3	Timer 1 - channel 3	-
26	21	PC4/ TIM1_CH4/ CLK_CCO	I/O	**X**	X	X	HS	O3	X	X	Port C4	Timer 1 - channel 4 /configurable clock output	-
27	22	PC5/ SPI_SCK	I/O	**X**	X	X	HS	O3	X	X	Port C5	SPI clock	-
28	23	PC6/ SPI_MOSI	I/O	**X**	X	X	HS	O3	X	X	Port C6	SPI master out/slave in	-

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Table 5. STM8S103K3 pin descriptions (continued)

SDIP32	LQFP/ UFQFP32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
29	24	PC7/ SPI_MISO	I/O	**X**	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	-
30	25	PD0/ TIM1_BKIN [CLK_CCO]	I/O	**X**	X	X	HS	O3	X	X	Port D0	Timer 1 - break input	Configurable clock output [AFR5]
31	26	PD1/ SWIM(4)	I/O	**X**	X	X	HS	O4	X	X	Port D1	SWIM data interface	-
32	27	PD2 [TIM2_CH3]	I/O	**X**	X	X	HS	O3	X	X	Port D2	-	Timer 2 - channel 3[AFR1]
1	28	PD3/ TIM2_CH2/ ADC_ETR	I/O	**X**	X	X	HS	O3	X	X	Port D3	Timer 2 - channel 2/ADC external trigger	-
2	29	PD4/BEEP/ TIM2_CH1	I/O	**X**	X	X	HS	O3	X	X	Port D4	Timer 2 - channel 1/BEEP output	-
3	30	PD5/ UART1_TX	I/O	**X**	X	X	HS	O3	X	X	Port D5	UART1 data transmit	-
4	31	PD6/ UART1_RX	I/O	**X**	X	X	HS	O3	X	X	Port D6	UART1 data receive	-
5	32	PD7/ TLI [TIM1_CH4]	I/O	**X**	X	X	HS	O3	X	X	Port D7	Top level interrupt	Timer 1 - channel 4 [AFR6]

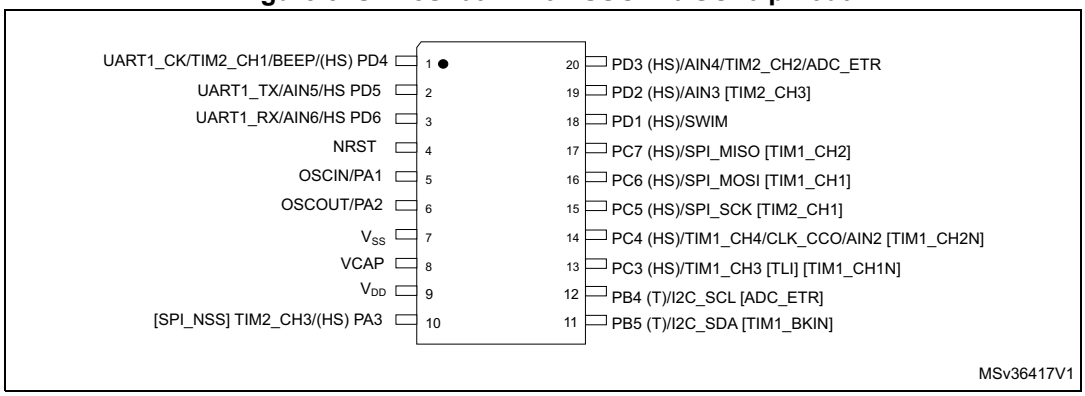
1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings (see *Section 10: Electrical characteristics*).
2. When the MCU is in Halt/Active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if Halt/Active-halt is used in the application.
3. In the open-drain output column, “T” defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to V_{DD} are not implemented).
4. The PD1 pin is in input pull-up during the reset phase and after internal reset release.

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5.2 STM8S103F2/F3 TSSOP20/SO20/UFQFPN20 pinout and pin description

5.2.1 STM8S103F2/F3 TSSOP20/SO20 pinout

Figure 5. STM8S103F2/F3 TSSOP20/SO20 pinout

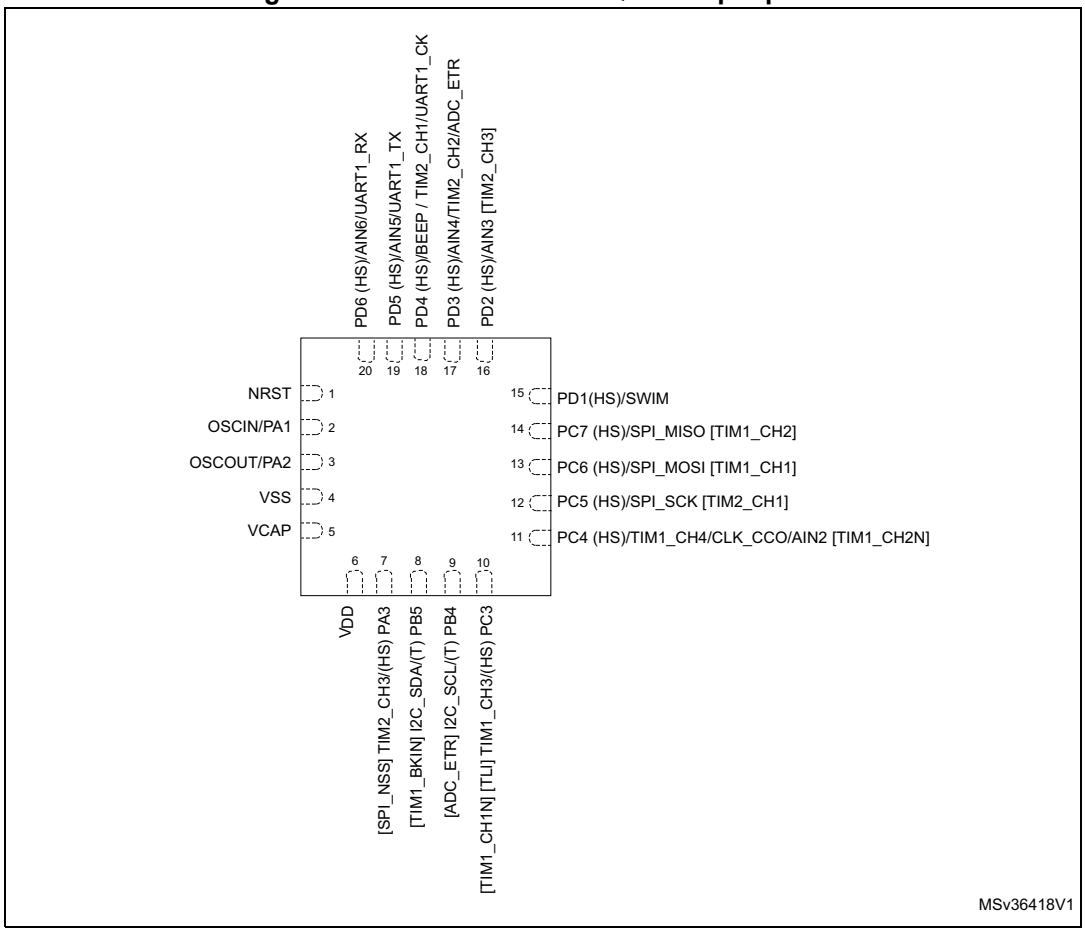


1. HS high sink capability.
2. (T) True open drain (P-buffer and protection diode to VDD not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function)

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5.2.2 STM8S103F2/F3 UFQFPN20 pinout

Figure 6. STM8S103F2/F3 UFQFPN20-pin pinout



1. HS high sink capability.
2. (T) True open drain (P-buffer and protection diode to VDD not implemented).
3. [ ] alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

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Table 6. STM8S103F2 and STM8S103F3 pin descriptions

TSSOP/SO20	UFQFPN20	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
1	18	PD4/ BEEP/ TIM2_ CH1/ UART1 _CK	I/O	**X**	X	X	HS	O3	X	X	Port D4	Timer 2 - channel 1/BEEP output/ UART1 clock	-
2	19	PD5/ AIN5/ UART1 _TX	I/O	**X**	X	X	HS	O3	X	X	Port D5	Analog input 5/ UART1 data transmit	-
3	20	PD6/ AIN6/ UART1 _RX	I/O	**X**	X	X	HS	O3	X	X	Port D6	Analog input 6/ UART1 data receive	-
4	1	NRST	I/O	-	**X**	-	-	-	-	-	Reset		-
5	2	PA1/ OSCIN(2)	I/O	**X**	X	X	-	O1	X	X	Port A1	Resonator/ crystal in	-
6	3	PA2/ OSCOUT	I/O	**X**	X	X	-	O1	X	X	Port A2	Resonator/ crystal out	-
7	4	VSS	S	-	-	-	-	-	-	-	Digital ground		-
8	5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		
9	6	VDD	S	-	-	-	-	-	-	-	Digital power supply		-
10	7	PA3/ TIM2_ CH3 [SPI_ NSS]	I/O	**X**	X	X	HS	O3	X	X	Port A3	Timer 2 channel 3	SPI master/ slave select [AFR1]
11	8	PB5/ I2C_ SDA [TIM1_ BKIN]	I/O	**X**	-	-	X	O1	T(3)	-	Port B5	I2C data	Timer 1 - break input [AFR4]
12	9	PB4/ I2C_ SCL	I/O	**X**	-	-	X	O1	T(3)	-	Port B4	I2C clock	ADC external trigger [AFR4]
13	10	PC3/ TIM1_CH3 [TLI] [TIM1_ CH1N]	I/O	**X**	X	X	HS	O3	X	X	Port C3	Timer 1 - channel 3	Top level interrupt [AFR3] Timer 1 - inverted channel 1 [AFR7]

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Table 6. STM8S103F2 and STM8S103F3 pin descriptions (continued)

TSSOP/SO20	UFQFPN20	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
				floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
14	11	PC4/ CLK_CCO/ TIM1_ CH4/AIN2/[TIM1_ CH2N]	I/O	**X**	X	X	HS	O3	X	X	Port C4	Configurable clock output/Timer 1 - channel 4/Analog input 2	Timer 1 - inverted channel 2 [AFR7]
15	12	PC5/ SPI_SCK [TIM2_ CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C5	SPI clock	Timer 2 - channel 1 [AFR0]
16	13	PC6/ SPI_MOSI [TIM1_ CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C6	SPI master out/slave in	Timer 1 - channel 1 [AFR0]
17	14	PC7/ SPI_MISO [TIM1_ CH2]	I/O	**X**	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	Timer 1 - channel 2 [AFR0]
18	15	PD1/ SWIM	I/O	**X**	X	X	HS	O4	X	X	Port D1	SWIM data interface	-
19	16	PD2/AIN3/[T IM2_ CH3]	I/O	**X**	X	X	HS	O3	X	X	Port D2	Analog input 3	Timer 2 - channel 3 [AFR1]
20	17	PD3/ AIN4/ TIM2_ CH2/ ADC_ ETR	I/O	**X**	X	X	HS	O3	X	X	Port D3	Analog input 4/ Timer 2 - channel 2/ADC external trigger	-

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings.
2. When the MCU is in halt/active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if halt/active-halt is used in the application.
3. In the open-drain output column, “T” defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to VDD are not implemented).1

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5.3 Alternate function remapping

As shown in the rightmost column of the pin description table, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

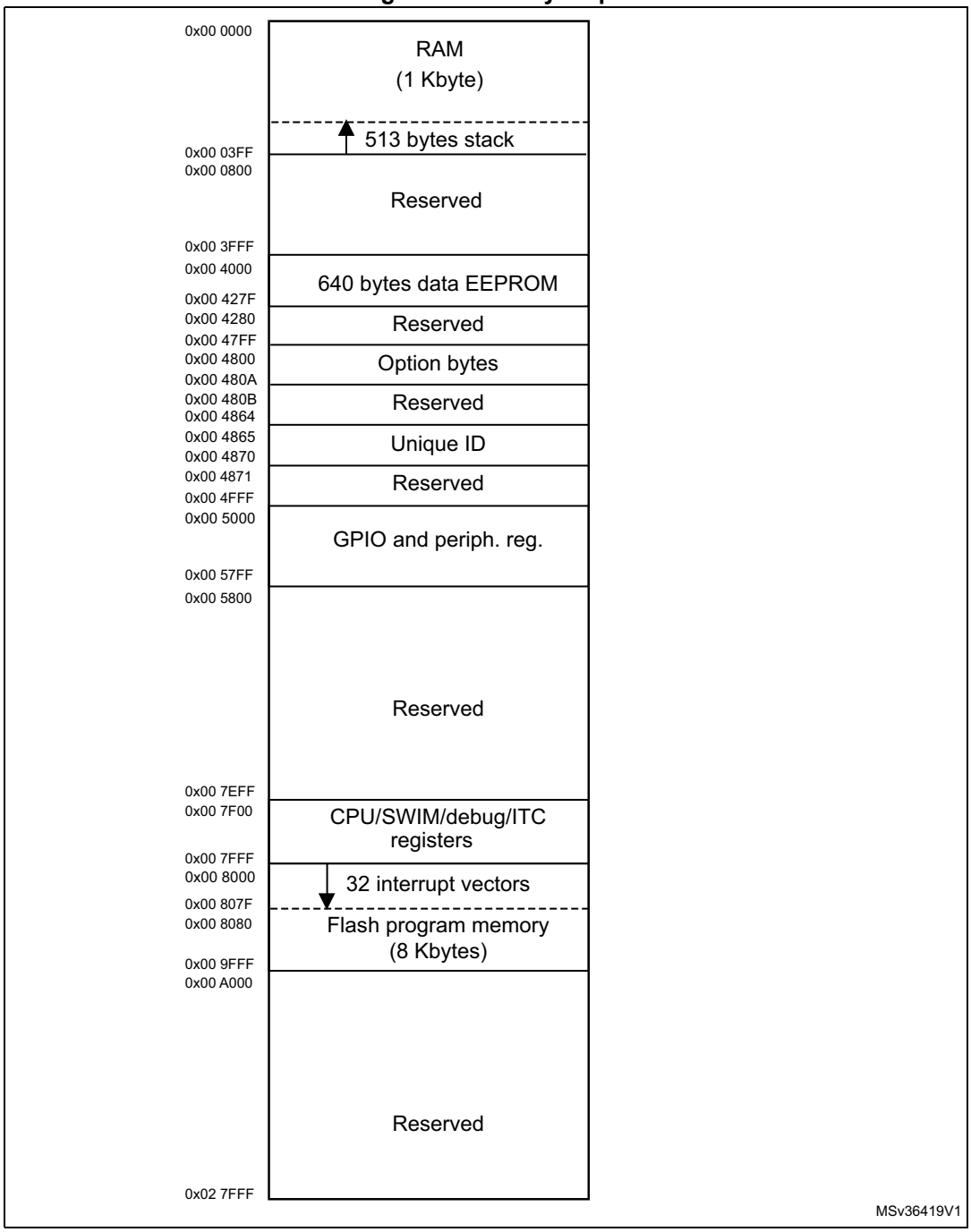
Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of the family reference manual, RM0016).

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6 Memory and register map

6.1 Memory map

Figure 7. Memory map



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6.2 Register map

6.2.1 I/O port hardware register map

Table 7. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX(1)
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX(1)
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0xXX(1)
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX(1)
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX(1)
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX(1)
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00

1. Depends on the external circuitry.

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6.2.2 General hardware register map

Table 8. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 501E to 0x00 5059	Reserved area (60 byte)			
0x00 505A	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 505B		FLASH_CR2	Flash control register 2	0x00
0x00 505C		FLASH_NCR2	Flash complementary control register 2	0xFF
0x00 505D		FLASH _FPR	Flash protection register	0x00
0x00 505E		FLASH _NFPR	Flash complementary protection register	0xFF
0x00 505F		FLASH _IAPSR	Flash in-application programming status register	0x00
0x00 5060 to 0x00 5061	Reserved area (2 byte)			
0x00 5062	Flash	FLASH _PUKR	Flash program memory unprotection register	0x00
0x00 5063	Reserved area (1 byte)			
0x00 5064	Flash	FLASH _DUKR	Data EEPROM unprotection register	0x00
0x00 5065 to 0x00 509F	Reserved area (59 byte)			
0x00 50A0	ITC	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2 to 0x00 50B2	Reserved area (17 byte)			
0x00 50B3	RST	RST_SR	Reset status register	0xXX(1)
0x00 50B4 to 0x00 50BF	Reserved area (12 byte)			
0x00 50C0	CLK	CLK_ICKR	Internal clock control register	0x01
0x00 50C1		CLK_ECKR	External clock control register	0x00
0x00 50C2	Reserved area (1 byte)			

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Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50C3	CLK	CLK_CMSR	Clock master status register	0xE1
0x00 50C4		CLK_SWR	Clock master switch register	0xE1
0x00 50C5		CLK_SWCR	Clock switch control register	0xXX
0x00 50C6		CLK_CKDIVR	Clock divider register	0x18
0x00 50C7		CLK_PCKENR1	Peripheral clock gating register 1	0xFF
0x00 50C8		CLK_CSSR	Clock security system register	0x00
0x00 50C9		CLK_CCOR	Configurable clock control register	0x00
0x00 50CA		CLK_PCKENR2	Peripheral clock gating register 2	0xFF
0x00 50CC		CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CD		CLK_SWIMCCR	SWIM clock control register	0bXXXX XXX0
0x00 50CE to 0x00 50D0	Reserved area (3 byte)			
0x00 50D1	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D2		WWDG_WR	WWDR window register	0x7F
0x00 50D3 to 00 50DF	Reserved area (13 byte)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX(2)
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 byte)			
0x00 50F0	AWU	AWU_CSR1	AWU control/status register 1	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 50FF	Reserved area (12 byte)			
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205		SPI_CRCPR	SPI CRC polynomial register	0x07
0x00 5206		SPI_RXCRCR	SPI Rx CRC register	0xFF
0x00 5207		SPI_TXCRCR	SPI Tx CRC register	0xFF

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Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5208 to 0x00 520F	Reserved area (8 byte)			
0x00 5210	I2C	I2C_CR1	I2C control register 1	0x00
0x00 5211		I2C_CR2	I2C control register 2	0x00
0x00 5212		I2C_FREQR	I2C frequency register	0x00
0x00 5213		I2C_OARL	I2C Own address register low	0x00
0x00 5214		I2C_OARH	I2C Own address register high	0x00
0x00 5215		Reserved		
0x00 5216		I2C_DR	I2C data register	0x00
0x00 5217		I2C_SR1	I2C status register 1	0x00
0x00 5218		I2C_SR2	I2C status register 2	0x00
0x00 5219		I2C_SR3	I2C status register 3	0x0X
0x00 521A		I2C_ITR	I2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I2C Clock control register low	0x00
0x00 521C		I2C_CCRH	I2C Clock control register high	0x00
0x00 521D		I2C_TRISER	I2C TRISE register	0x02
0x00 521E		I2C_PECR	I2C packet error checking register	0x00
0x00 521F to 0x00 522F	Reserved area (17 byte)			
0x00 5230	UART1	UART1_SR	UART1 status register	0xC0
0x00 5231		UART1_DR	UART1 data register	0xXX
0x00 5232		UART1_BRR1	UART1 baud rate register 1	0x00
0x00 5233		UART1_BRR2	UART1 baud rate register 2	0x00
0x00 5234		UART1_CR1	UART1 control register 1	0x00
0x00 5235		UART1_CR2	UART1 control register 2	0x00
0x00 5236		UART1_CR3	UART1 control register 3	0x00
0x00 5237		UART1_CR4	UART1 control register 4	0x00
0x00 5238		UART1_CR5	UART1 control register 5	0x00
0x00 5239		UART1_GTR	UART1 guard time register	0x00
0x00 523A		UART1_PSCR	UART1 prescaler register	0x00
0x00 523B to 0x00 523F	Reserved area (21 byte)			

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Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00
0x00 525F		TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00
0x00 5265		TIM1_CCR1H	TIM1 capture/compare register 1 high	0x00
0x00 5266		TIM1_CCR1L	TIM1 capture/compare register 1 low	0x00
0x00 5267		TIM1_CCR2H	TIM1 capture/compare register 2 high	0x00
0x00 5268		TIM1_CCR2L	TIM1 capture/compare register 2 low	0x00
0x00 5269		TIM1_CCR3H	TIM1 capture/compare register 3 high	0x00

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Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 526A	TIM1	TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 byte)			

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Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5300	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5301		Reserved		
0x00 5302		Reserved		
0x00 5303		TIM2_IER	TIM2 Interrupt enable register	0x00
0x00 5304		TIM2_SR1	TIM2 status register 1	0x00
0x00 5305		TIM2_SR2	TIM2 status register 2	0x00
0x00 5306		TIM2_EGR	TIM2 event generation register	0x00
0x00 5307		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5308		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 5309		TIM2_CCMR3	TIM2 capture/compare mode register 3	0x00
0x00 530A		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 530B		TIM2_CCER2	TIM2 capture/compare enable register 2	0x00
0x00 530C		TIM2_CNTRH	TIM2 counter high	0x00
0x00 530D		TIM2_CNTRL	TIM2 counter low	0x00
0x00 530E		TIM2_PSCR	IM2 prescaler register	0x00
0x00 530F		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 5310		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 5311		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5312		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5313		TIM2_CCR2H	TIM2 capture/compare reg. 2 high	0x00
0x00 5314		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5315		TIM2_CCR3H	TIM2 capture/compare register 3 high	0x00
0x00 5316		TIM2_CCR3L	TIM2 capture/compare register 3 low	0x00
0x00 5317 to 0x00 533F	Reserved area (43 byte)			

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Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5340	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 5341		Reserved		
0x00 5342		Reserved		
0x00 5343		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 5344		TIM4_SR	TIM4 status register	0x00
0x00 5345		TIM4_EGR	TIM4 event generation register	0x00
0x00 5346		TIM4_CNTR	TIM4 counter	0x00
0x00 5347		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 5348		TIM4_ARR	TIM4 auto-reload register	0xFF
0x00 5349 to 0x00 53DF	Reserved area (153 byte)			
0x00 53E0 to 0x00 53F3	ADC1	ADC_DBxR	ADC data buffer registers	0x00
0x00 53F4 to 0x00 53FF	Reserved area (12 byte)			

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Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5400	ADC1 cont'd	ADC_CSR	ADC control/status register	0x00
0x00 5401		ADC_CR1	ADC configuration register 1	0x00
0x00 5402		ADC_CR2	ADC configuration register 2	0x00
0x00 5403		ADC_CR3	ADC configuration register 3	0x00
0x00 5404		ADC_DRH	ADC data register high	0xXX
0x00 5405		ADC_DRL	ADC data register low	0xXX
0x00 5406		ADC_TDRH	ADC Schmitt trigger disable register high	0x00
0x00 5407		ADC_TDRL	ADC Schmitt trigger disable register low	0x00
0x00 5408		ADC_HTRH	ADC high threshold register high	0x03
0x00 5409		ADC_HTRL	ADC high threshold register low	0xFF
0x00 540A		ADC_LTRH	ADC low threshold register high	0x00
0x00 540B		ADC_LTRL	ADC low threshold register low	0x00
0x00 540C		ADC_AWSRH	ADC analog watchdog status register high	0x00
0x00 540D		ADC_AWSRL	ADC analog watchdog status register low	0x00
0x00 540E		ADC _AWCRH	ADC analog watchdog control register high	0x00
0x00 540F		ADC_AWCRL	ADC analog watchdog control register low	0x00
0x00 5410 to 0x00 57FF	Reserved area (1008 byte)			

1. Depends on the previous reset source.
2. Write-only register.

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6.2.3 CPU/SWIM/debug module/interrupt controller registers

Table 9. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x03
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 byte)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC	ITC_SPR1	Interrupt software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 byte)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 byte)			

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Table 9. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM debug module control register 1	0x00
0x00 7F97		DM_CR2	DM debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 byte)			

1. Accessible by debug module only.

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7 Interrupt vector mapping

Table 10. Interrupt mapping

IRQ no.	Source block	Description	Wakeup from halt mode	Wakeup from active-halt mode	Vector address
-	RESET	Reset	Yes	Yes	0x00 8000
-	TRAP	Software interrupt	-	-	0x00 8004
0	TLI	External top level interrupt	-	-	0x00 8008
1	AWU	Auto wake up from halt	-	Yes	0x00 800C
2	CLK	Clock controller	-	-	0x00 8010
3	EXTI0	Port A external interrupts	Yes(1)	Yes(1)	0x00 8014
4	EXTI1	Port B external interrupts	Yes	Yes	0x00 8018
5	EXTI2	Port C external interrupts	Yes	Yes	0x00 801C
6	EXTI3	Port D external interrupts	Yes	Yes	0x00 8020
7	EXTI4	Port E external interrupts	Yes	Yes	0x00 8024
8	Reserved	-	-	-	0x00 8028
9	Reserved	-	-	-	0x00 802C
10	SPI	End of transfer	Yes	Yes	0x00 8030
11	TIM1	TIM1 update/ overflow/ underflow/ trigger/ break	-	-	0x00 8034
12	TIM1	TIM1 capture/ compare	-	-	0x00 8038
13	TIM2	TIM2 update/ overflow	-	-	0x00 803C
14	TIM2	TIM2 capture/ compare	-	-	0x00 8040
15	Reserved	-	-	-	0x00 8044
16	Reserved	-	-	-	0x00 8048
17	UART1	Tx complete	-	-	0x00 804C
18	UART1	Receive register DATA FULL	-	-	0x00 8050
19	I2C	I2C interrupt	Yes	Yes	0x00 8054
20	Reserved	-	-	-	0x00 8058

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Table 10. Interrupt mapping (continued)

IRQ no.	Source block	Description	Wakeup from halt mode	Wakeup from active-halt mode	Vector address
21	Reserved	-	-	-	0x00 805C
22	ADC1	ADC1 end of conversion/ analog watchdog interrupt	-	-	0x00 8060
23	TIM4	TIM4 update/ overflow	-	-	0x00 8064
24	Flash	EOP/WR_PG_DIS	-	-	0x00 8068
Reserved					0x00 806C to 0x00 807C

1. Except PA1.

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8 Option byte

Option byte contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Except for the ROP (read-out protection) byte, each option byte has to be stored twice, in a regular form (OPTx) and a complemented one (NOPTx) for redundancy.

Option byte can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in the table below.

Option byte can also be modified ‘on the fly’ by the application in IAP mode, except the ROP option that can only be modified in ICP mode (via SWIM).

Refer to the STM8S Flash programming manual (PM0051) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

Table 11. Option byte

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x4800	Read-out protection (ROP)	OPT0	ROP [7:0]								0x00
0x4801	User boot code (UBC)	OPT1	UBC [7:0]								0x00
0x4802		NOPT1	NUBC [7:0]								0xFF
0x4803	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	AFR4	AFR3	AFR2	AFR1	AFR0	0x00
0x4804		NOPT2	NAFR7	NAFR6	NAFR5	NAFR4	NAFR3	NAFR2	NAFR1	NAFR0	0xFF
0x4805h	Misc. option	OPT3	Reserved			HSI TRIM	LSI _ EN	IWDG _HW	WWDG _HW	WWDG _HALT	0x00
0x4806		NOPT3	Reserved			NHSI TRIM	NLSI _ EN	NIWDG _HW	NWWDG _HW	NWWG _HALT	0xFF
0x4807	Clock option	OPT4	Reserved				EXT CLK	CKAWU SEL	PRS C1	PRS C0	0x00
0x4808		NOPT4	Reserved				NEXT CLK	NCKA WUSEL	NPRSC1	NPR SC0	0xFF
0x4809	HSE clock startup	OPT5	HSECNT [7:0]								0x00
0x480A		NOPT5	NHSECNT [7:0]								0xFF

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Table 12. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]** Memory readout protection (ROP) 0xAA: Enable readout protection (write access via SWIM protocol) *Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[7:0]** User boot code area 0x00: no UBC, no write-protection 0x01: Page 0 defined as UBC, memory write-protected Page 0 and 1 contain the interrupt vectors. ... 0x7F: Pages 0 to 126 defined as UBC, memory write-protected Other values: Pages 0 to 127 defined as UBC, memory write-protected *Note: Refer to the family reference manual (RM0016) section on Flash write protection for more details.*
OPT2	**AFR[7:0]** Refer to the following section for alternate function remapping descriptions of bits [7:2] and [1:0] respectively.
OPT3	**HSITRIM:** High speed internal clock trimming register size 0: 3-bit trimming supported in CLK_HSITRIMR register 1: 4-bit trimming supported in CLK_HSITRIMR register
	LSI_EN: Low speed internal clock enable 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: Independent watchdog 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware
	WWDG_HW: Window watchdog activation 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: Window watchdog reset on halt 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active

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Table 12. Option byte description (continued)

Option byte no.	Description
OPT4	**EXTCLK:** External clock selection 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: Auto wake-up unit/clock 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for AWU
	PRSC[1:0] AWU clock prescaler 0x: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]:** HSE crystal oscillator stabilization time 0x00: 2048 HSE cycles 0xB4: 128 HSE cycles 0xD2: 8 HSE cycles 0xE1: 0.5 HSE cycles

8.1 Alternate function remapping bits

Table 13. STM8S103K3 alternate function remapping bits for 32-pin devices

Option byte no.	Description(1)
OPT2	**AFR7** Alternate function remapping option 7 Reserved.
	AFR6 Alternate function remapping option 6 0: AFR6 remapping option inactive: Default alternate function.(2) 1: Port D7 alternate function = TIM1_CH4.
	AFR5 Alternate function remapping option 5 0: AFR5 remapping option inactive: Default alternate function.(2) 1: Port D0 alternate function = CLK_CCO.
	AFR[4:2] Alternate function remapping options 4:2 Reserved.
	AFR1 Alternate function remapping option 1 0: AFR1 remapping option inactive: Default alternate functions.(2) 1: Port A3 alternate function = SPI_NSS; port D2 alternate function = TIM2_CH3.
	AFR0 Alternate function remapping option 0 Reserved.

1. Do not use more than one remapping option in the same port. It is forbidden to enable both AFR1 and AFR0.
2. Refer to pinout description.

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Table 14. STM8S103Fx alternate function remapping bits for 20-pin devices

Option byte no.	Description
OPT2	**AFR7** Alternate function remapping option 7 0: AFR7 remapping option inactive: Default alternate functions.(1) 1: Port C3 alternate function = TIM1_CH1N; port C4 alternate function = TIM1_CH2N.
	AFR6 Alternate function remapping option 6 Reserved.
	AFR5 Alternate function remapping option 5 Reserved.
	AFR4 Alternate function remapping options 4:2 0: AFR4 remapping option inactive: Default alternate functions.(1) 1: Port B4 alternate function = ADC_ETR; port B5 alternate function = TIM1_BKIN.
	AFR3 Alternate function remapping option 3 0: AFR3 remapping option inactive: Default alternate function.(1) 1: Port C3 alternate function = TLI.
	AFR2 Alternate function remapping option 2 Reserved
	AFR1 Alternate function remapping option 1(2) 0: AFR1 remapping option inactive: Default alternate functions.(1) 1: Port A3 alternate function = SPI_NSS; port D2 alternate function = TIM2_CH3.
	AFR0 Alternate function remapping option 0 0: AFR0 remapping option inactive: Default alternate functions.(1) 1: Port C5 alternate function = TIM2_CH1; port C6 alternate function = TIM1_CH1; port C7 alternate function = TIM1_CH2.

1. Refer to pinout description.
2. Do not use more than one remapping option in the same port. It is forbidden to enable both AFR1 and AFR0.

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9 Unique ID

The devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single byte and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

Table 15. Unique ID registers (96 bits)

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x4865	X co-ordinate on the wafer	U_ID[7:0]							
0x4866		U_ID[15:8]							
0x4867	Y co-ordinate on the wafer	U_ID[23:16]							
0x4868		U_ID[31:24]							
0x4869	Wafer number	U_ID[39:32]							
0x486A	Lot number	U_ID[47:40]							
0x486B		U_ID[55:48]							
0x486C		U_ID[63:56]							
0x486D		U_ID[71:64]							
0x486E		U_ID[79:72]							
0x486F		U_ID[87:80]							
0x4870		U_ID[95:88]							

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10 Electrical characteristics

10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C, and T_A = T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 Σ).

10.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2 Σ).

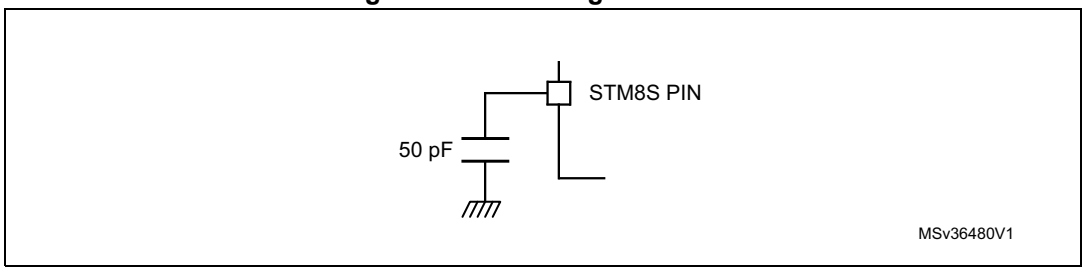
10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

10.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

Figure 8. Pin loading conditions

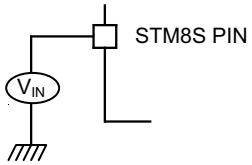


10.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

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Figure 9. Pin input voltage



MSv36481V1

10.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 16: Voltage characteristics*, *Table 17: Current characteristics* and *Table 18: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and a functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device's reliability.

The device's mission profile (application conditions) is compliant with the JEDEC JESD47 Qualification Standard, the extended mission profiles are available on demand.

Table 16. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins(2)	V_{SS} - 0.3	6.5	V
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{DD} \rvert$	Variations between different power pins	-	50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins	-	50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 87*		

1. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply
2. This pin must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Table 17. Current characteristics

Symbol	Ratings	Max.(1)	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(2)	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	80	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	-20	

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Table 17. Current characteristics (continued)

Symbol	Ratings	Max.(1)	Unit
$I_{INJ(PIN)}$ (3) (4)	Injected current on NRST pin	±4	mA
	Injected current on OSCIN pin	±4	
	Injected current on any other pin(5)	±4	
ΣI_{INJ}(3)	Total injected current (sum of all I/O and control pins)(5)	±20	

1. Guaranteed by characterization results.
2. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external supply.
3. I_{INJ} must never be exceeded. This condition is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current allowed and the corresponding V_{IN} maximum must always be respected.
4. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for IINJ(PIN) and $\Sigma I_{INJ(PIN)}$ in the I/O port pin characteristics section does not affect the ADC accuracy.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 18. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	150	

10.3 Operating conditions

Table 19. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	-	0	16	MHz
V_{DD}	Standard operating voltage	-	2.95	5.5	V
V_{CAP}(1)	C_{EXT}: capacitance of external capacitor	-	470	3300	nF
	ESR of external capacitor	at 1 MHz(2)	-	0.3	Ω
	ESL of external capacitor		-	15	nH
P_D(3)	Power dissipation at T_A = 75 °C for suffix 6	TSSOP20	-	238	mW
		SO20W	-	220	
		UFQFPN20	-	220	
		LQFP32	-	330	
		UFQFPN32	-	526	
		SDIP32	-	330	

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Table 19. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
P_D(3)	Power dissipation at T_A = 125 °C for suffix 3	TSSOP20	-	59	mW
		SO20W	-	55	
		UFQFPN20	-	55	
		LQFP32	-	83	
		UFQFPN32	-	132	
		SDIP32	-	83	
T_A	Ambient temperature for suffix 6 version	Maximum power dissipation	-40	85	°C
T_A	Ambient temperature for suffix 3 version	Maximum power dissipation	-40	125	
T_J	Junction temperature range	Suffix 6 version	-40	105	
		Suffix 3 version	-40	130	

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.
2. This frequency of 1 MHz as a condition for V_{CAP} parameters is given by design of internal regulator.
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax}=(T_{Jmax}- T_A)/\Theta_{JA}$ (see *Section 12: Thermal characteristics*) with the value for T_{Jmax} given in the previous table and the value for Θ_{JA} given in *Section 12: Thermal characteristics*

Figure 10. f_{CPUmax} versus V_{DD}

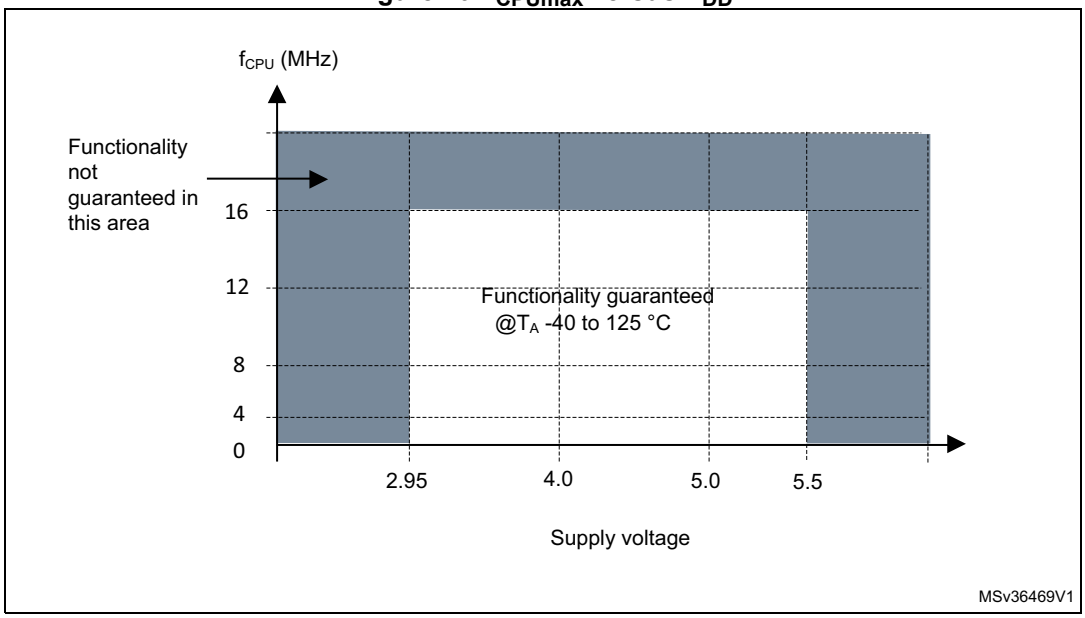


Table 20. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	2	-	∞	µs/V
	V_{DD} fall time rate(1)	-	2	-	∞	

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Table 20. Operating conditions at power-up/power-down (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{TEMP}	Reset release delay	V_{DD} rising	-	-	1.7	ms
V_{IT+}	Power-on reset threshold	-	2.6	2.7	2.85	V
V_{IT-}	Brown-out reset threshold	-	2.5	2.65	2.8	
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70	-	mV

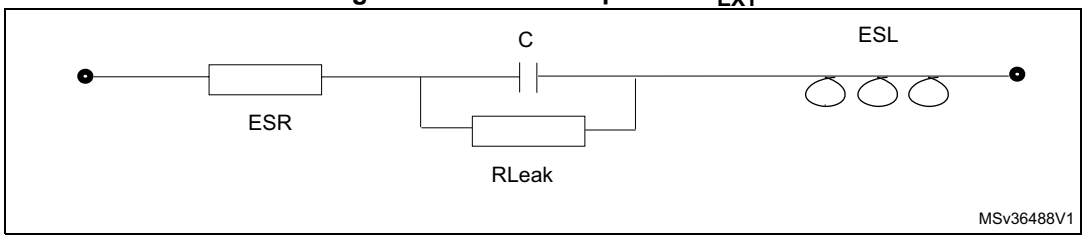
1. Reset is always generated after a t_{TEMP} delay. The application must ensure that V_{DD} is still above the minimum operating voltage (V_{DD} min) when the t_{TEMP} delay has elapsed.

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10.3.1 VCAP external capacitor

The stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in *Table 19*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 11. External capacitor C_{EXT}



1. ESR is the equivalent series resistance and ESL is the equivalent inductance.

10.3.2 Supply current characteristics

The current consumption is measured as illustrated in *Figure 9: Pin input voltage*.

Total supply current consumption in run mode

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled (clock stopped by peripheral clock gating registers) except if explicitly mentioned.

Subject to general operating conditions for V_{DD} and T_A.

Table 21. Total current consumption with code execution in run mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in Run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	2.3	-	mA
			HSE user ext. clock (16 MHz)	2	2.35	
			HSI RC osc. (16 MHz)	1.7	2	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSE user ext. clock (16 MHz)	0.86	-	
			HSI RC osc. (16 MHz)	0.7	0.87	
		$f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.41	0.55	

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Table 21. Total current consumption with code execution in run mode at V_{DD} = 5 V (continued)

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in Run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	4.5	-	mA
			HSE user ext. clock (16 MHz)	4.3	4.75	
			HSI RC osc. (16 MHz)	3.7	4.5	
		$f_{CPU} = f_{MASTER}$ = 2 MHz	HSI RC osc. (16 MHz/8)(2)	0.84	1.05	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSI RC osc. (16 MHz)	0.72	0.9	
		$f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.42	0.57	

1. Guaranteed by characterization results. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

Table 22. Total current consumption with code execution in run mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in Run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.8	-	mA
			HSE user ext. clock (16 MHz)	2	2.35	
			HSI RC osc. (16 MHz)	1.5	2	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSE user ext. clock (16 MHz)	0.81	-	
			HSI RC osc. (16 MHz)	0.7	0.87	
		$f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.41	0.55	
$I_{DD(RUN)}$	Supply current in Run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	4	-	mA
			HSE user ext. clock (16 MHz)	4.3	4.75	
			HSI RC osc. (16 MHz)	3.9	4.7	
		$f_{CPU} = f_{MASTER}$ = 2 MHz	HSI RC osc. (16 MHz/8)(2)	0.84	1.05	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSI RC osc. (16 MHz)	0.72	0.9	
		$f_{CPU} = f_{MASTER}$ /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.42	0.57	

1. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

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Total current consumption in wait mode

Table 23. Total current consumption in wait mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.6	-	mA
			HSE user ext. clock (16 MHz)	1.1	1.3	
			HSI RC osc. (16 MHz)	0.89	1.1	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSI RC osc. (16 MHz)	0.7	0.88	
		$f_{CPU} = f_{MASTER}$ /s128 = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.45	0.57	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.4	0.54	

1. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

Table 24. Total current consumption in wait mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.1	-	mA
			HSE user ext. clock (16 MHz)	1.1	1.3	
			HSI RC osc. (16 MHz)	0.89	1.1	
		$f_{CPU} = f_{MASTER}$ /128 = 125 kHz	HSI RC osc. (16 MHz)	0.7	0.88	
		$f_{CPU} = f_{MASTER}$ /s128 = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.45	0.57	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.4	0.54	

1. Guaranteed by characterization results.
2. Default clock configuration measured with all peripherals off.

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Total current consumption in active halt mode

Table 25. Total current consumption in active halt mode at V_{DD} = 5 V

Symbol	Parameter	Conditions			Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source				
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	1030	-	-	µA
			Operating mode	LSI RC osc. (128 kHz)	200	260	300	
			Power down mode	HSE crystal osc. (16 MHz)	970	-	-	
			Power down mode	LSI RC osc. (128 kHz)	150	200	230	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	85	110	
			Power down mode	LSI RC osc. (128 kHz)	10	20	40	

1. Guaranteed by characterization results.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Table 26. Total current consumption in active halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions			Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source				
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	550	-	-	µA
			Operating mode	LSI RC osc. (128 kHz)	200	260	290	
			Power down mode	HSE crystal osc. (16 MHz)	970	-	-	
			Power down mode	LSI RC osc. (128 kHz)	150	200	230	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	80	105	
			Power down mode	LSI RC osc. (128 kHz)	10	18	35	

1. Guaranteed by characterization results.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

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Total current consumption in halt mode

Table 27. Total current consumption in halt mode at V_{DD} = 5 V

Symbol	Parameter	Conditions	Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	63	75	105	µA
		Flash in power-down mode, HSI clock after wakeup	6.0	20	55	

1. Guaranteed by characterization results.

Table 28. Total current consumption in halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max at 85 °C(1)	Max at 85 °C(1)	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	60	75	100	µA
		Flash in power-down mode, HSI clock after wakeup	4.5	17	30	

1. Guaranteed by characterization results.

Low power mode wakeup times

Table 29. Wakeup times

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
$t_{WU(WFI)}$	Wakeup time from wait mode to run mode(2)	0 to 16 MHz			-	See note(3)	µs
$t_{WU(WFI)}$	Wakeup time from run mode(2)	f_{CPU}= f_{MASTER}= 16 MHz			0.56	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode(2)	MVR voltage regulator on(4)	Flash in operating mode(5)	HSI (after wakeup)	1(6)	2(6)	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode(2)	MVR voltage regulator off(4)	Flash in operating mode(5)	HSI (after wakeup)	3(6)	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode(2)	MVR voltage regulator off(4)	Flash in operating mode(5)	HSI (after wakeup)	48(6)	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode(2)	MVR voltage regulator off(4)	Flash in power-down mode(5)	HSI (after wakeup)	50(6)	-	
$t_{WU(H)}$	Wakeup time from halt mode to run mode(2)	Flash in operating mode(5)			52	-	
$t_{WU(H)}$	Wakeup time from halt mode to run mode(2)	Flash in power-down mode(5)			54	-	

1. Guaranteed by characterization results.

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2. Measured from interrupt event to interrupt vector fetch
3. $t_{WU(WFI)} = 2 \times 1/f_{master} + 67 \times 1/f_{CPU}$
4. Configured by the REGAH bit in the CLK_ICKR register.
5. Configured by the AHALT bit in the FLASH_CR1 register.
6. Plus 1 LSI clock depending on synchronization.

Total current consumption and timing in forced reset state

Table 30. Total current consumption and timing in forced reset state

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$I_{DD(R)}$	Supply current in reset state(2)	V_{DD} = 5 V	400	-	µA
		V_{DD} = 3.3 V	300	-	
$t_{RESETBL}$	Reset pin release to vector fetch	-	-	150	µs

1. Guaranteed by design.
2. Characterized with all I/Os tied to V_{SS}.

Current consumption of on-chip peripherals

Subject to general operating conditions for V_{DD} and T_A.

HSI internal RC/f_{CPU}= f_{MASTER} = 16 MHz, V_{DD} = 5 V

Table 31. Peripheral current consumption

Symbol	Parameter	Typ	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)	210	µA
$I_{DD(TIM2)}$	TIM2 supply current(1)	130	
$I_{DD(TIM4)}$	TIM4 supply current(1)	50	
$I_{DD(UART1)}$	UART1 supply current (2)	120	
$I_{DD(SPI)}$	SPI supply current (2)	45	
$I_{DD(I2C)}$	I2C supply current(2)	65	
$I_{DD(ADC1)}$	ADC1 supply current when converting(3)	1000	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.
2. Data based on a differential IDD measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.
3. Data based on a differential IDD measurement between reset configuration and continuous A/D conversions. Not tested in production.

Current consumption curves

The following figures show typical current consumption measured with code executing in RAM.

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Figure 12. Typ $I_{DD(RUN)}$ vs. V_{DD} HSE user external clock, f_{CPU} = 16 MHz

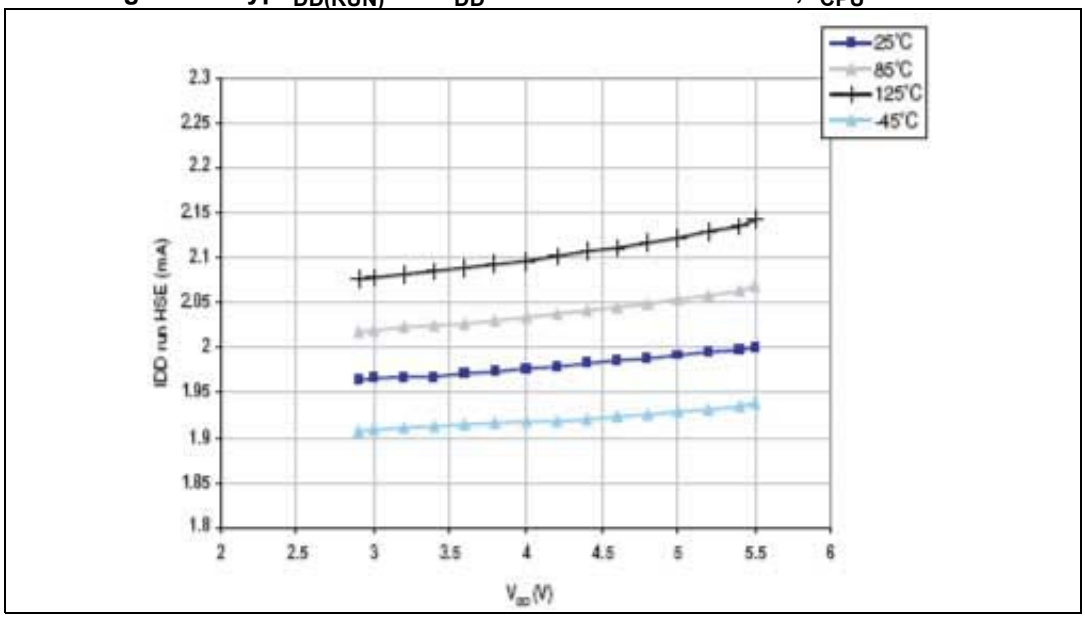
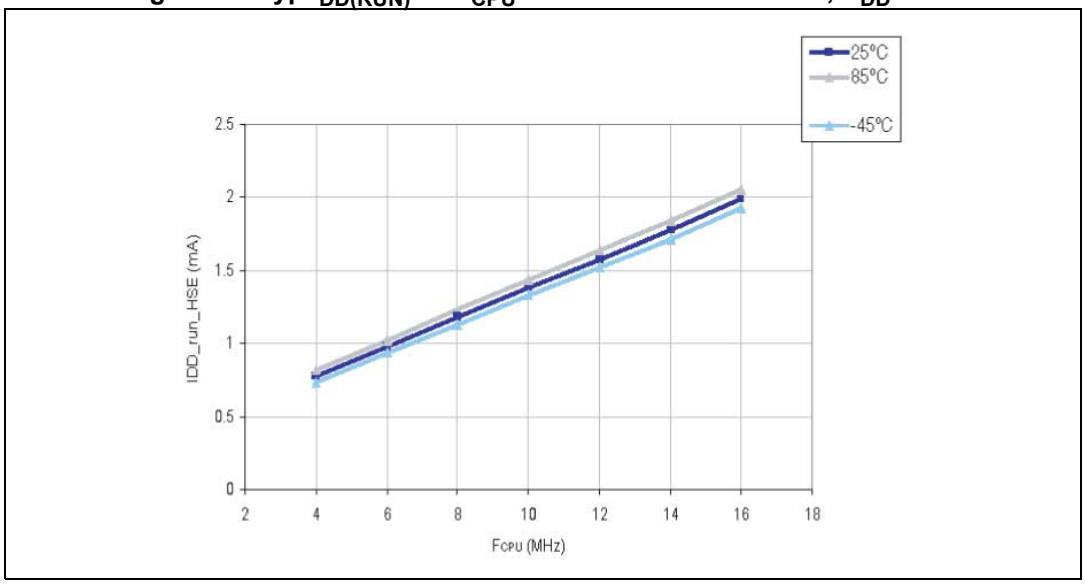


Figure 13. Typ $I_{DD(RUN)}$ vs. f_{CPU} HSE user external clock, V_{DD} = 5 V



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Figure 14. Typ $I_{DD(RUN)}$ vs. V_{DD} HSI RC osc, f_{CPU} = 16 MHz

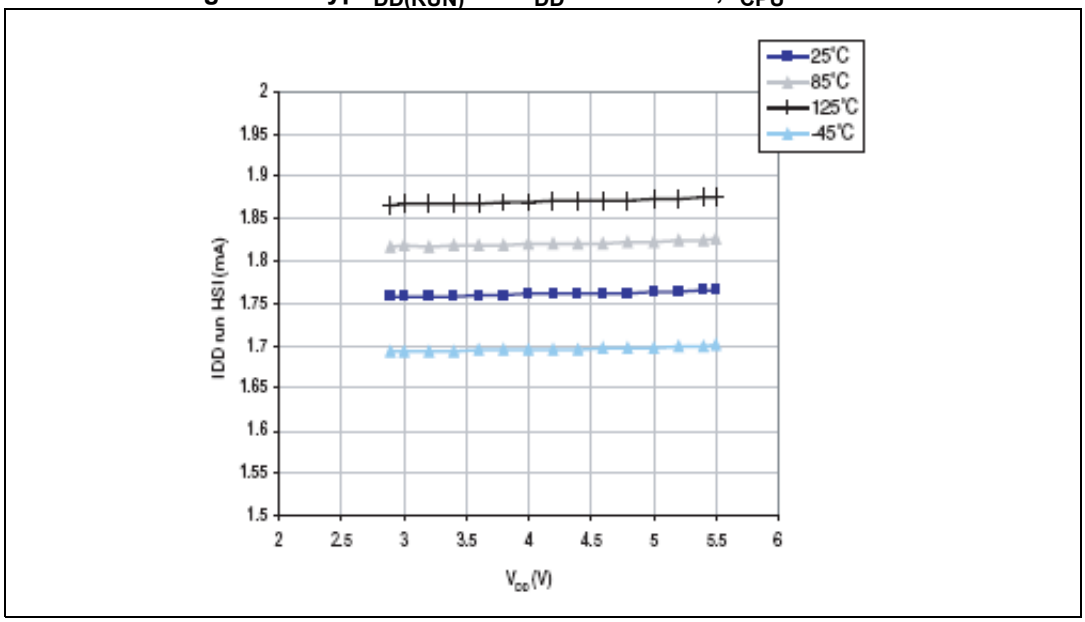
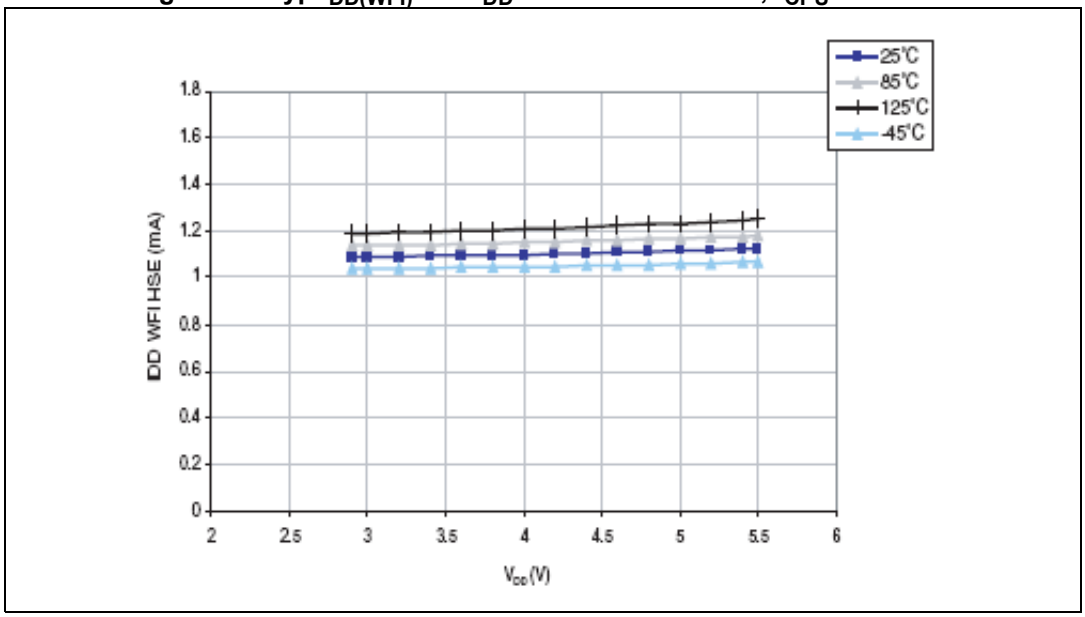


Figure 15. Typ $I_{DD(WFI)}$ vs. V_{DD} HSE external clock, f_{CPU} = 16 MHz



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Figure 16. Typ $I_{DD(WFI)}$ vs. f_{CPU} HSE external clock, V_{DD} = 5 V

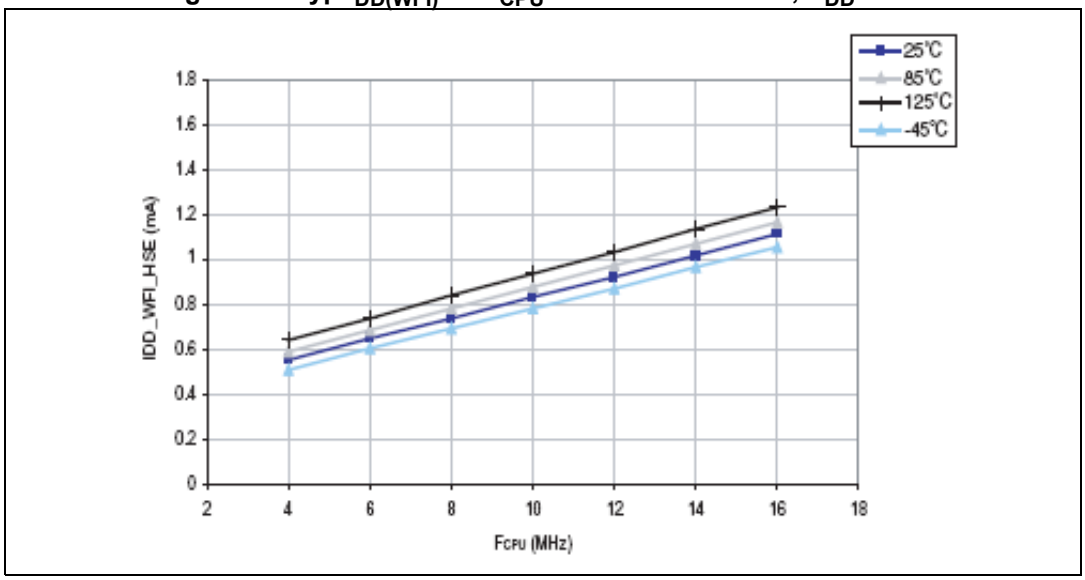
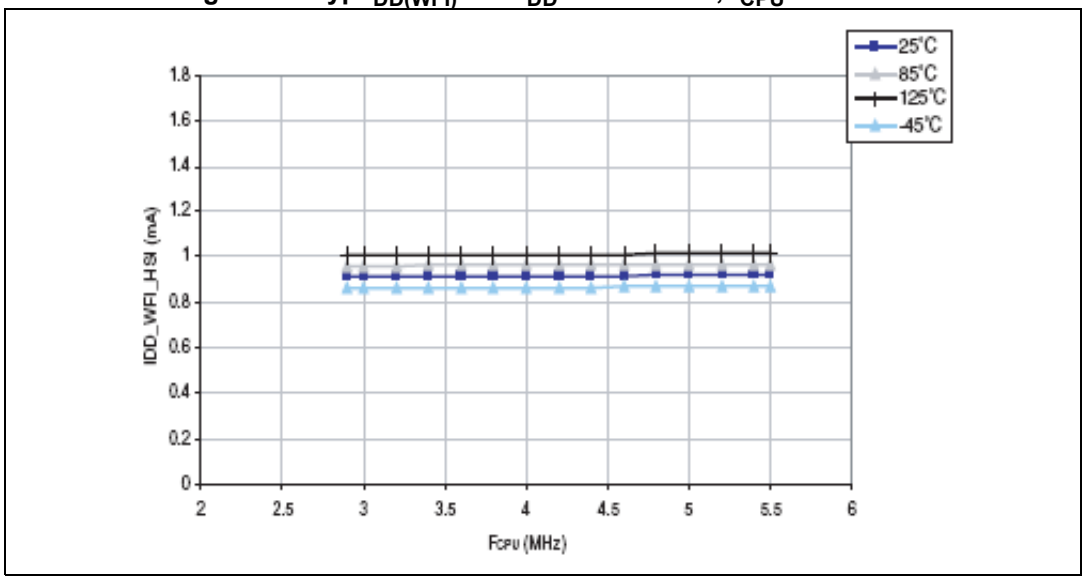


Figure 17. Typ $I_{DD(WFI)}$ vs. V_{DD} HSI RC osc., f_{CPU} = 16 MHz



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10.3.3 External clock sources and timing characteristics

HSE user external clock

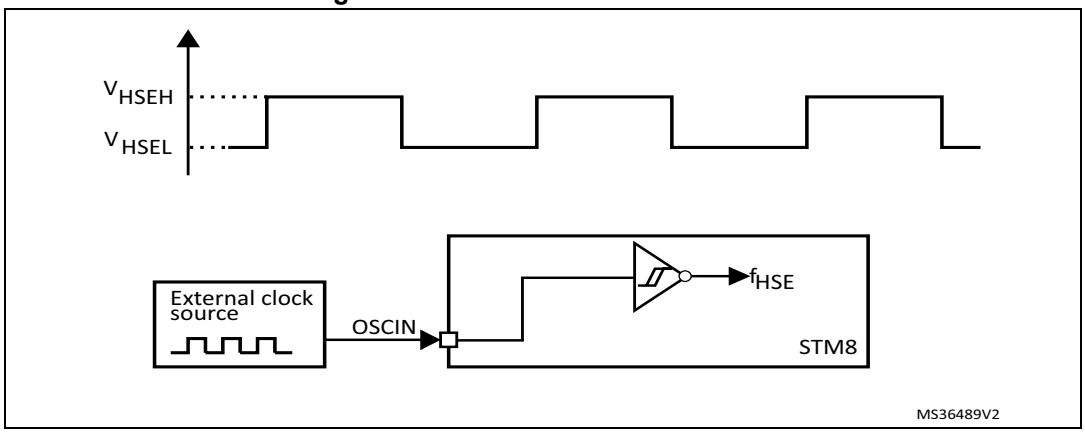
Subject to general operating conditions for V_{DD} and T_A.

Table 32. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	0	16	MHz
V_{HSEH}(1)	OSCIN input pin high level voltage	-	0.7 x V_{DD}	V_{DD} + 0.3 V	V
V_{HSEL}(1)	OSCIN input pin low level voltage	-	V_{SS}	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	+1	µA

1. Guaranteed by characterization results.

Figure 18. HSE external clock source



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HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

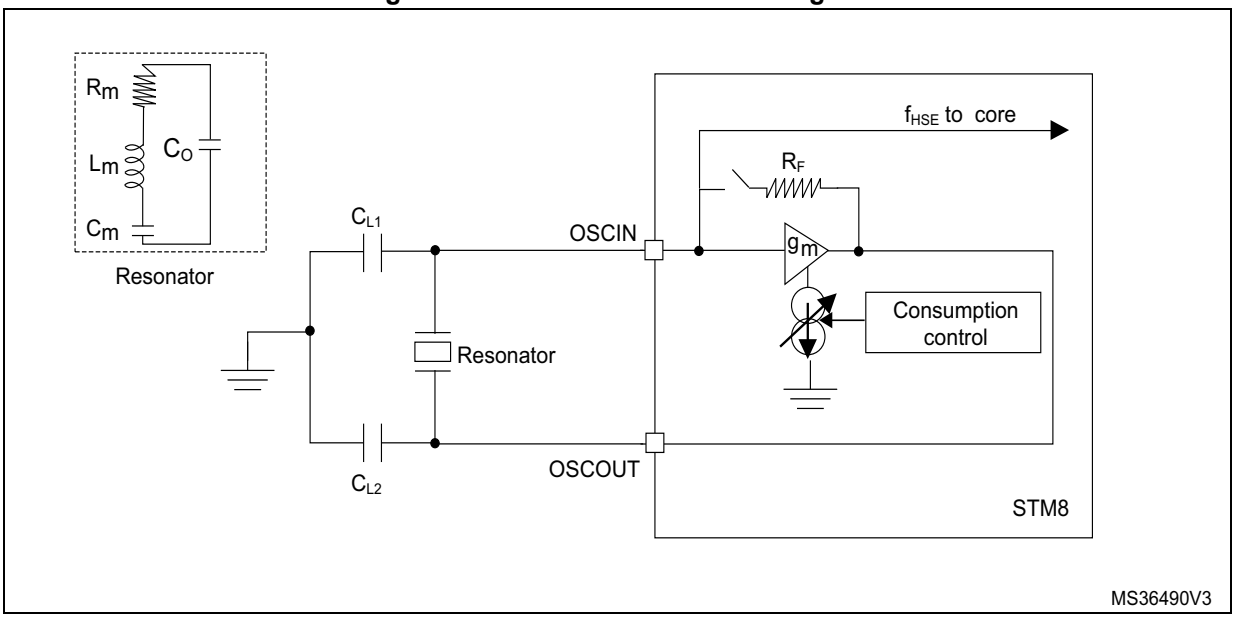
Table 33. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	External high speed oscillator frequency	-	1	-	16	MHz
R_F	Feedback resistor	-	-	220	-	kΩ
$C^{(1)}$	Recommended load capacitance(2)	-	-	-	20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF f_{OSC} = 16 MHz	-	-	6 (start up) 1.6 (stabilized)(3)	mA
		C = 10 pF f_{OSC} = 16 MHz	-	-	6 (start up) 1.2 (stabilized)(3)	
g_m	Oscillator transconductance	-	5	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	ms

1. C is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small Rm value. Refer to crystal manufacturer for more details
3. Guaranteed by characterization results.
4. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

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Figure 19. HSE oscillator circuit diagram



HSE oscillator critical g_m equation

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Notional resistance (see crystal specification)
L_m: Notional inductance (see crystal specification)
C_m: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
$C_{L1} = C_{L2} = C$: Grounded external capacitance
$g_m \gg g_{mcrit}$

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10.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A.

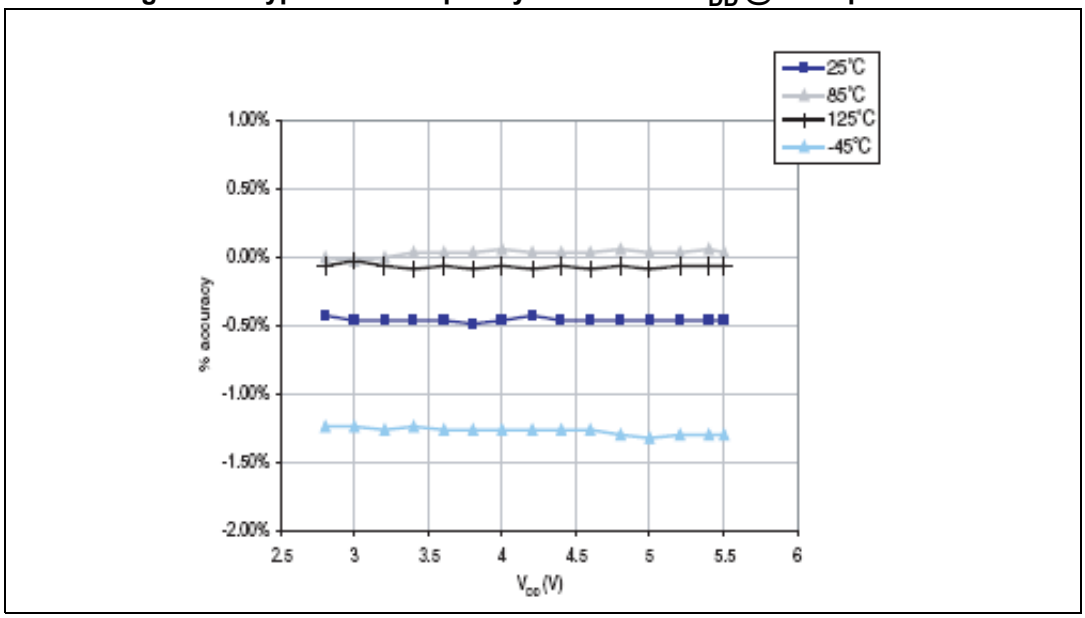
High speed internal RC oscillator (HSI)

Table 34. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HS}	Accuracy of HSI oscillator	User-trimmed with CLK_HSITRIMR register for given V_{DD} and T_A conditions(1)	-	-	1(2)	%
	HSI oscillator accuracy (factory calibrated)	V_{DD} = 5 V, T_A = 25 °C(3)	-1.0	-	1.0	
		V_{DD} = 5 V, -25°C ≤ T_A ≤ 85 °C	-2.0	-	2.0	
		2.95 V ≤ V_{DD} ≤ 5.5 V, -40°C ≤ T_A ≤ 125 °C	-3.0(3)	-	3.0(3)	
$t_{su(HSI)}$	HSI oscillator wakeup time including calibration	-	-	-	1.0(2)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	170	250(3)	µA

1. Refer to application note.
2. Guaranteed by design, not tested in production.
3. Guaranteed by characterization results.

Figure 20. Typical HSI frequency variation vs V_{DD} @ 4 temperatures



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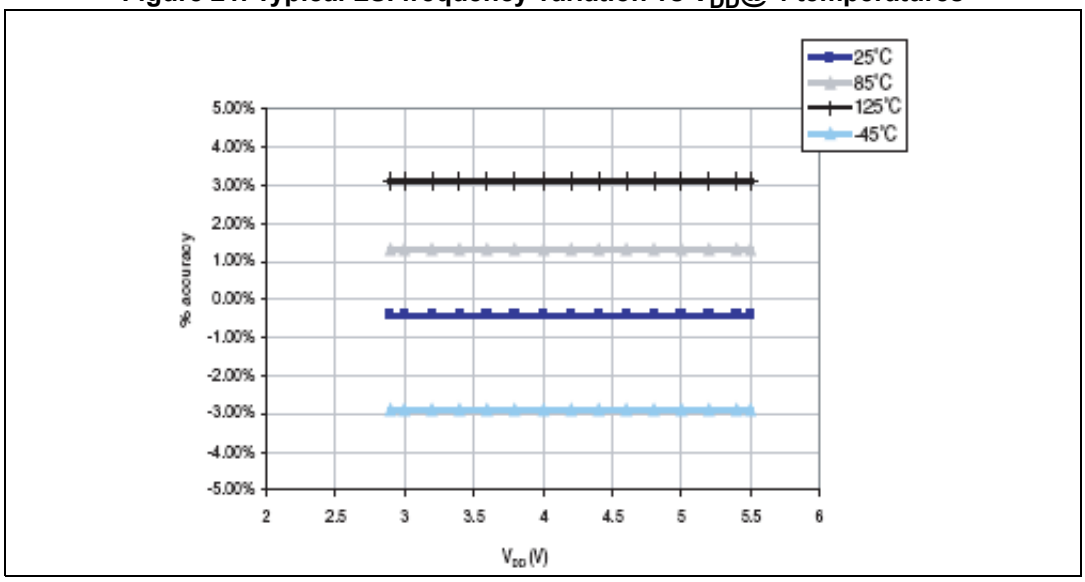
Low speed internal RC oscillator (LSI)

Subject to general operating conditions for V_{DD} and T_A.

Table 35. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	110	128	150	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	7	µs
IDD(LSI)	LSI oscillator power consumption	-	-	5	-	µA

Figure 21. Typical LSI frequency variation vs V_{DD}@ 4 temperatures



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10.3.5 Memory characteristics

RAM and hardware registers

Table 36. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Unit
V_{RM}	Data retention mode(1)	Halt mode (or reset)	V_{IT-max}(2)	V

1. Minimum supply voltage without losing data stored in RAM (in halt mode or under reset) or in hardware registers (only in halt mode). Guaranteed by design, not tested in production.
2. Refer to *Section 10.3: Operating conditions* for the value of V_{IT-max}.

Flash program memory/data EEPROM memory

Table 37. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, execution/write/erase)	f_{CPU}≤ 16 MHz	2.95	-	5.5	V
t_{prog}	Standard programming time (including erase) for byte/word/block (1 byte/4 byte/64 byte)	-	-	6	6.6	ms
	Fast programming time for 1 block (64 byte)	-	-	3	3.33	
t_{erase}	Erase time for 1 block (64 byte)	-	-	3	3.33	
N_{RW}	Erase/write cycles (program memory)(2)	T_A = +85 °C	100k	-	-	cycle
	Erase/write cycles (data memory)(2)	T_A = +125 °C	300k	1M	-	
t_{RET}	Data retention (program and data memory) after 10k erase/write cycles at T_A= +55 °C	T_{RET} = 55 °C	20	-	-	year
	Data retention (data memory) after 300k erase/write cycles at T_A= +125°C	T_{RET} = 85 °C	1	-	-	
I_{DD}	Supply current (Flash programming or erasing for 1 to 128 byte)	-	-	2	-	mA

1. Guaranteed by characterization results.
2. The physical granularity of the memory is 4 byte, so cycling is performed on 4 byte even when a write/erase operation addresses a single byte.

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10.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage, using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 38. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	V_{DD} = 5 V	-0.3 V	-	0.3 x V_{DD}	V
V_{IH}	Input high level voltage		0.7 x V_{DD}	-	V_{DD} + 0.3 V	
V_{hys}	Hysteresis(1)		-	700	-	mV
R_{pu}	Pull-up resistor	V_{DD} = 5 V, V_{IN} = V_{SS}	30	55	80	kΩ
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 50 pF	-	-	35(2)	ns
		Standard and high sink I/Os Load = 50 pF	-	-	125(2)	
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 20 pF	-	-	20(2)	ns
		Standard and high sink I/Os Load = 20 pF	-	-	50(2)	
I_{lkg}	Digital input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1(3)	µA
$I_{lkg\ ana}$	Analog input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±250(3)	nA
$I_{lkg(inj)}$	Leakage current in adjacent I/O	Injection current ±4 mA	-	-	±1(3)	µA

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.
2. Data guaranteed by design.
3. Guaranteed by characterization results

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Figure 22. Typical V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

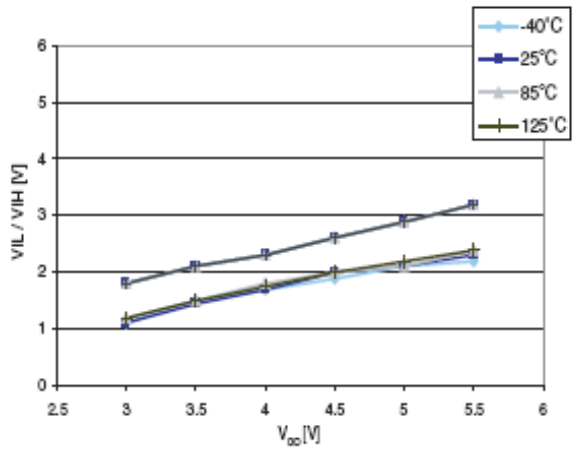


Figure 23. Typical pull-up current vs V_{DD} @ 4 temperatures

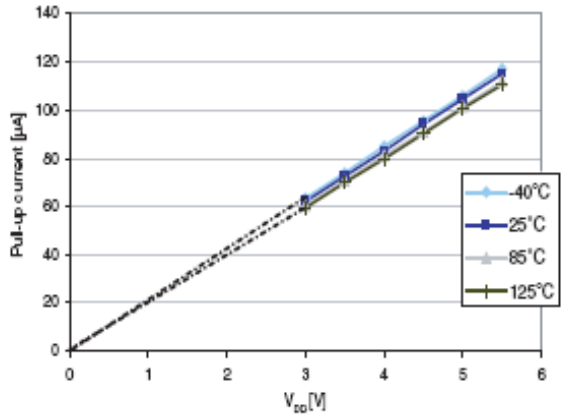


Figure 24. Typical pull-up resistance vs VDD @ 4 temperatures

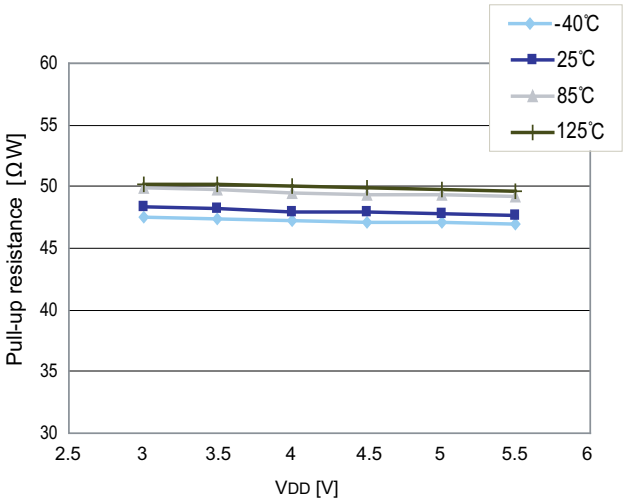


Table 39. Output driving current (standard ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	2.0	V
	Output low level with 4 pins sunk	I_{IO}= 4 mA, V_{DD} = 3.3 V	-	1.0(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO}= 10 mA, V_{DD} = 5 V	2.8	-	
	Output high level with 4 pins sourced	I_{IO}= 4 mA, V_{DD} = 3.3 V	2.1(1)	-	

1. Guaranteed by characterization results

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Table 40. Output driving current (true open drain ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 2 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	1.0	V
	Output low level with 2 pins sunk	I_{IO}= 10 mA, V_{DD} = 3.3 V	-	1.5(1)	
V_{OH}	Output high level with 2 pins sourced	I_{IO}= 10 mA, V_{DD} = 5 V	-	2.0(1)	

1. Guaranteed by characterization results

Table 41. Output driving current (high sink ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V	-	0.8	V
	Output low level with 4 pins sunk	I_{IO}= 10 mA, V_{DD} = 3.3 V	-	1.0(1)	
		I_{IO}= 20 mA, V_{DD} = 5 V	-	1.5(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO}= 10 mA, V_{DD} = 5 V	4.0	-	
	Output high level with 4 pins sourced	I_{IO}= 10 mA, V_{DD} = 3.3 V	2.1(1)	-	
		I_{IO}= 20 mA, V_{DD} = 5 V	3.3(1)	-	

1. Guaranteed by characterization results.

Figure 25. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports)

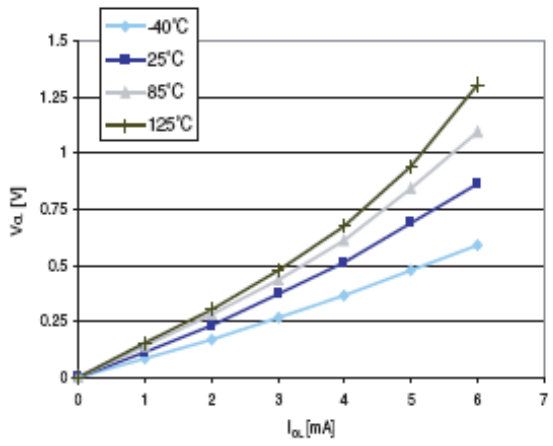
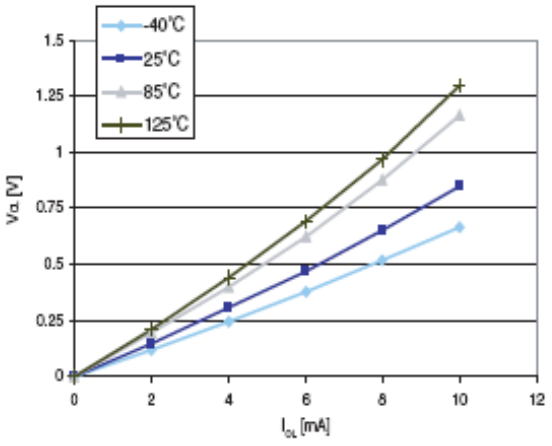


Figure 26. Typ. V_{OL} @ V_{DD} = 5.0 V (standard ports)



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Figure 27. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports)

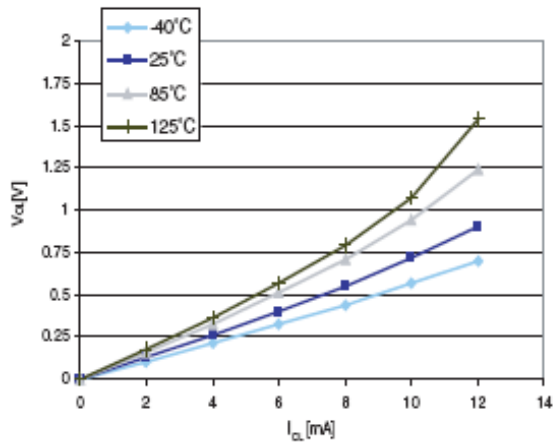


Figure 28. Typ. V_{OL} @ V_{DD} = 5.0 V (true open drain ports)

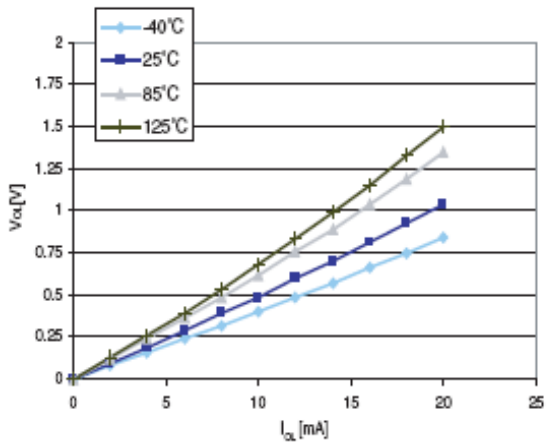


Figure 29. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports)

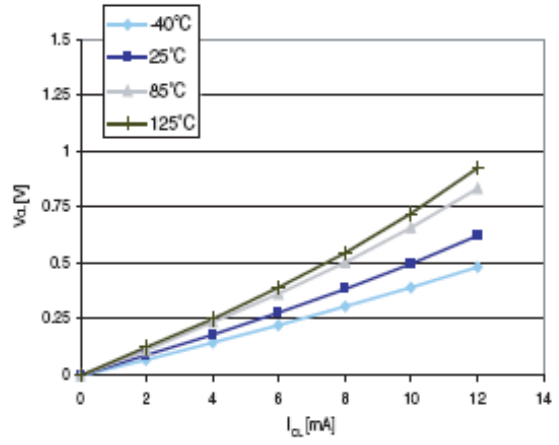
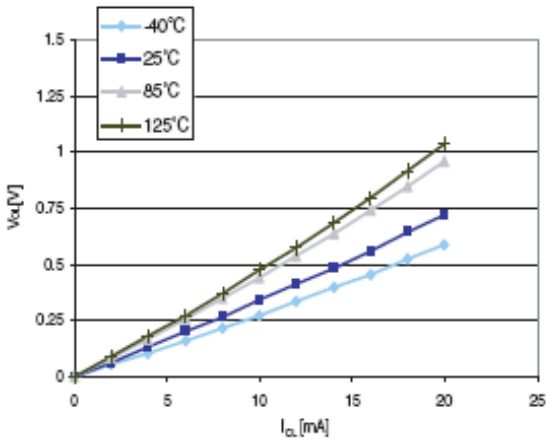


Figure 30. Typ. V_{OL} @ V_{DD} = 5.0 V (high sink ports)



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Figure 31. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports)

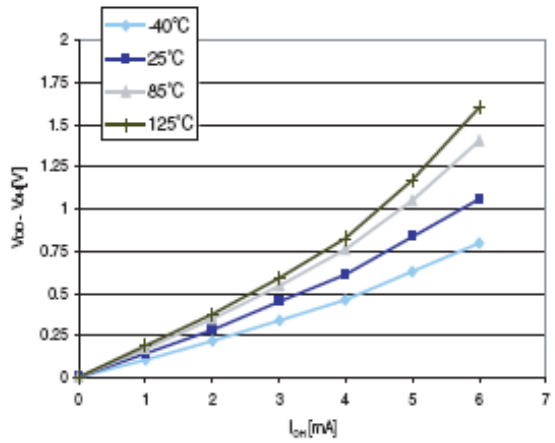


Figure 32. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (standard ports)

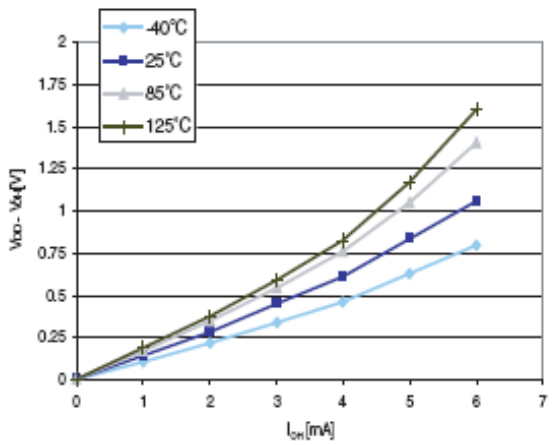


Figure 33. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports)

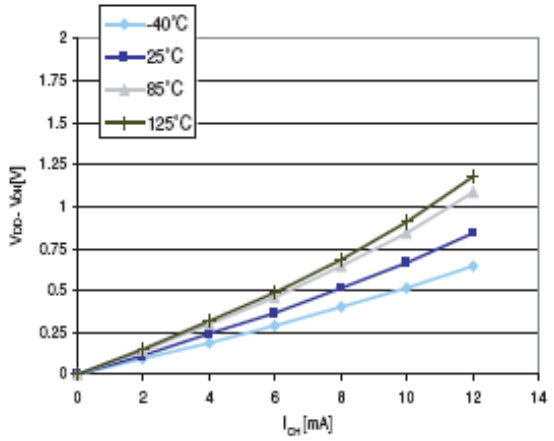
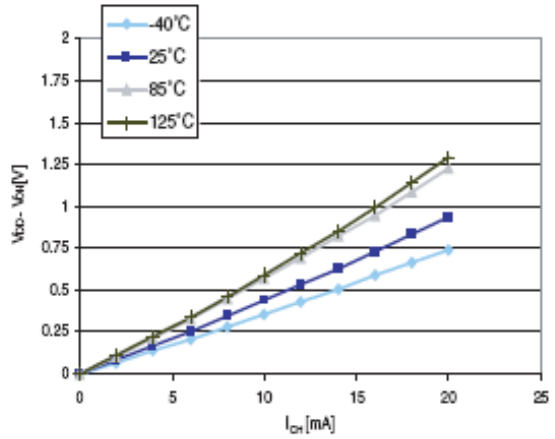


Figure 34. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (high sink ports)



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10.3.7 Reset pin characteristics

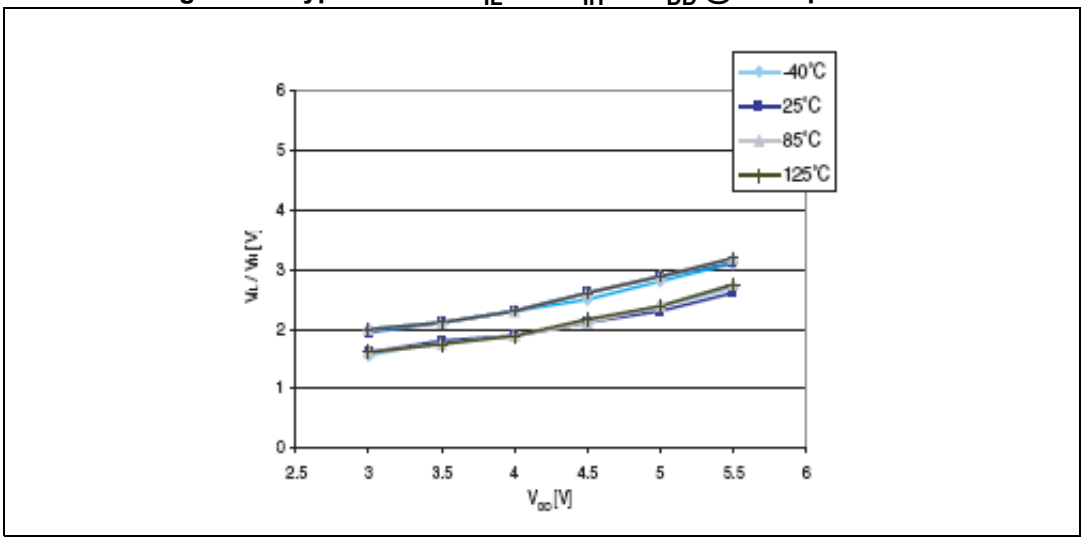
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 42. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage(1)	-	-0.3	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage(1)	I_{OL}= 2 mA	0.7 x V_{DD}	-	V_{DD}+ 0.3	
$V_{OL(NRST)}$	NRST output low level voltage(1)	I_{OL}= 3 mA	-	-	0.5	
$R_{PU(NRST)}$	NRST pull-up resistor(2)	-	30	55	80	kΩ
$t_{IFP(NRST)}$	NRST input filtered pulse(3)	-	-	-	75	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse(3)	-	500	-	-	
$t_{OP(NRST)}$	NRST output pulse(3)	-	20	-	-	µs

1. Guaranteed by characterization results.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.
3. Guaranteed by design.

Figure 35. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures



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Figure 36. Typical NRST pull-up resistance R_{PU} vs V_{DD} @ 4 temperatures

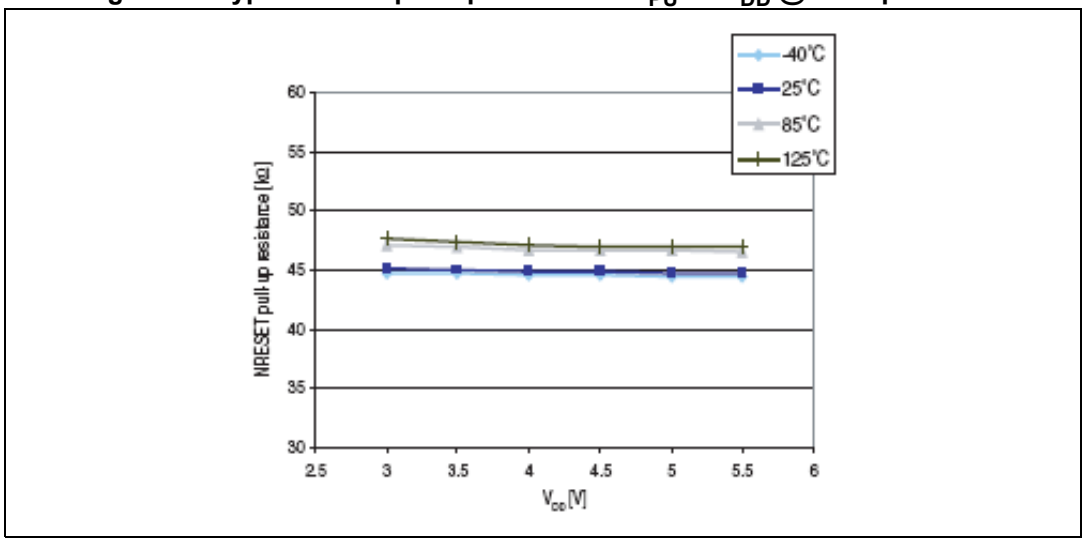
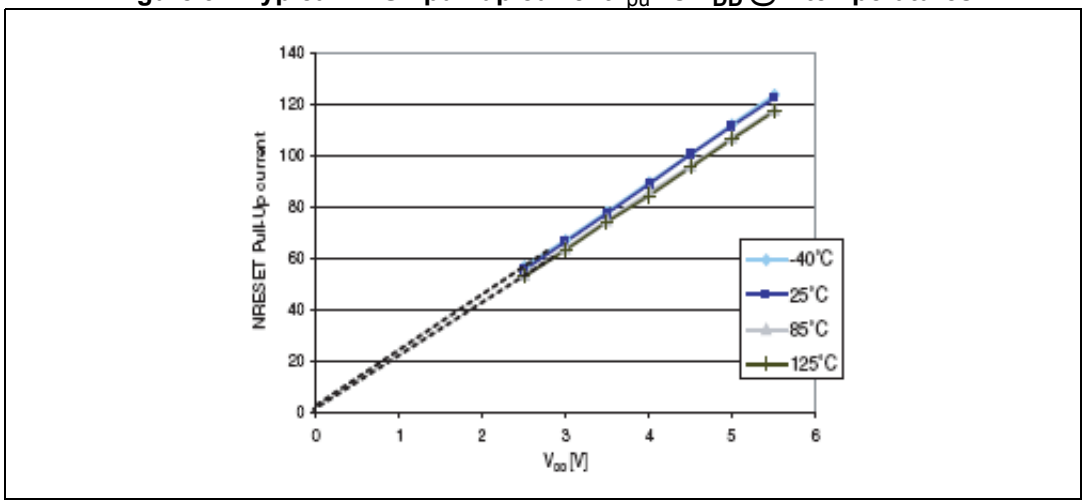


Figure 37. Typical NRST pull-up current I_{pu} vs V_{DD} @ 4 temperatures

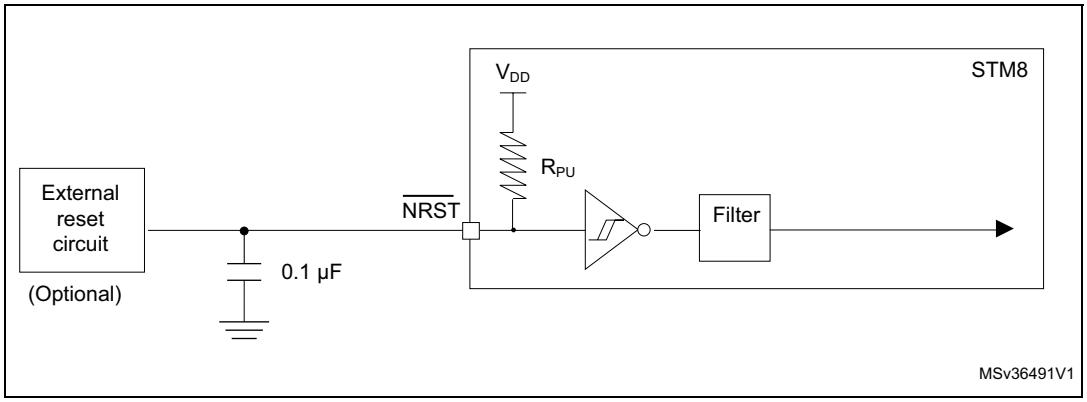


The reset network shown in *Figure 38* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below $V_{IL(NRST)}$ max (see *Table 42: NRST pin characteristics*), otherwise the reset is not taken into account internally.

For power consumption sensitive applications, the external reset capacitor value can be reduced to limit the charge/discharge current. If NRST signal is used to reset external circuitry, attention must be taken to the charge/discharge time of the external capacitor to fulfill the external devices reset timing conditions. Minimum recommended capacity is 100 nF.

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Figure 38. Recommended reset pin protection



10.3.8 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 43. SPI characteristics

Symbol	Parameter	Conditions(1)	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	8	MHz
		Slave mode	0	7	

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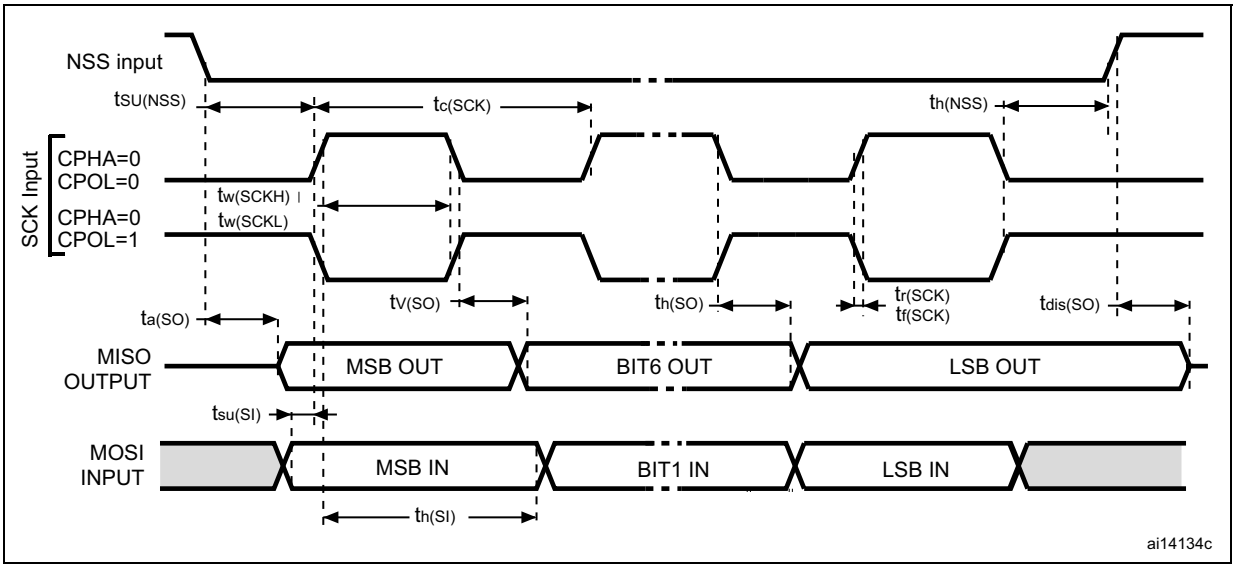
Table 43. SPI characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Max	Unit
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	25	ns
$t_{su(NSS)}$[2]	NSS setup time	Slave mode	4 * t_{MASTER}	-	
$t_{h(NSS)}$[2]	NSS hold time	Slave mode	70	-	
$t_{w(SCKH)}$[2] $t_{w(SCKL)}$[2]	SCK high and low time	Master mode	$t_{SCK}/2$ - 15	$t_{SCK}/2$ + 15	
$t_{su(MI)}$[2] $t_{su(SI)}$[2]	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}$[2] $t_{h(SI)}$[2]	Data input hold time	Master mode	7	-	
		Slave mode	10	-	
$t_{a(SO)}$[2][3]	Data output access time	Slave mode	-	3* t_{MASTER}	
$t_{dis(SO)}$[2][4]	Data output disable time	Slave mode	25	-	
$t_{v(SO)}$[2]	Data output valid time	Slave mode (after enable edge)	-	65	
$t_{v(MO)}$[2]	Data output valid time	Master mode (after enable edge)	-	30	
$t_{h(SO)}$[2]	Data output hold time	Slave mode (after enable edge)	27	-	
$t_{h(MO)}$[2]		Master mode (after enable edge)	11	-	

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

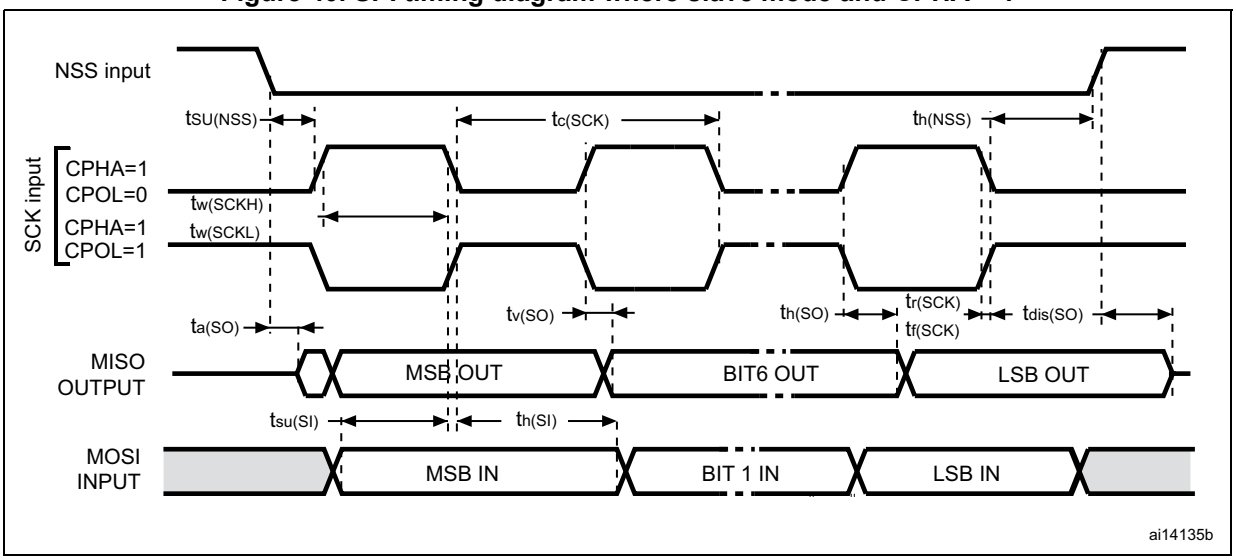
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Figure 39. SPI timing diagram where slave mode and CPHA = 0



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

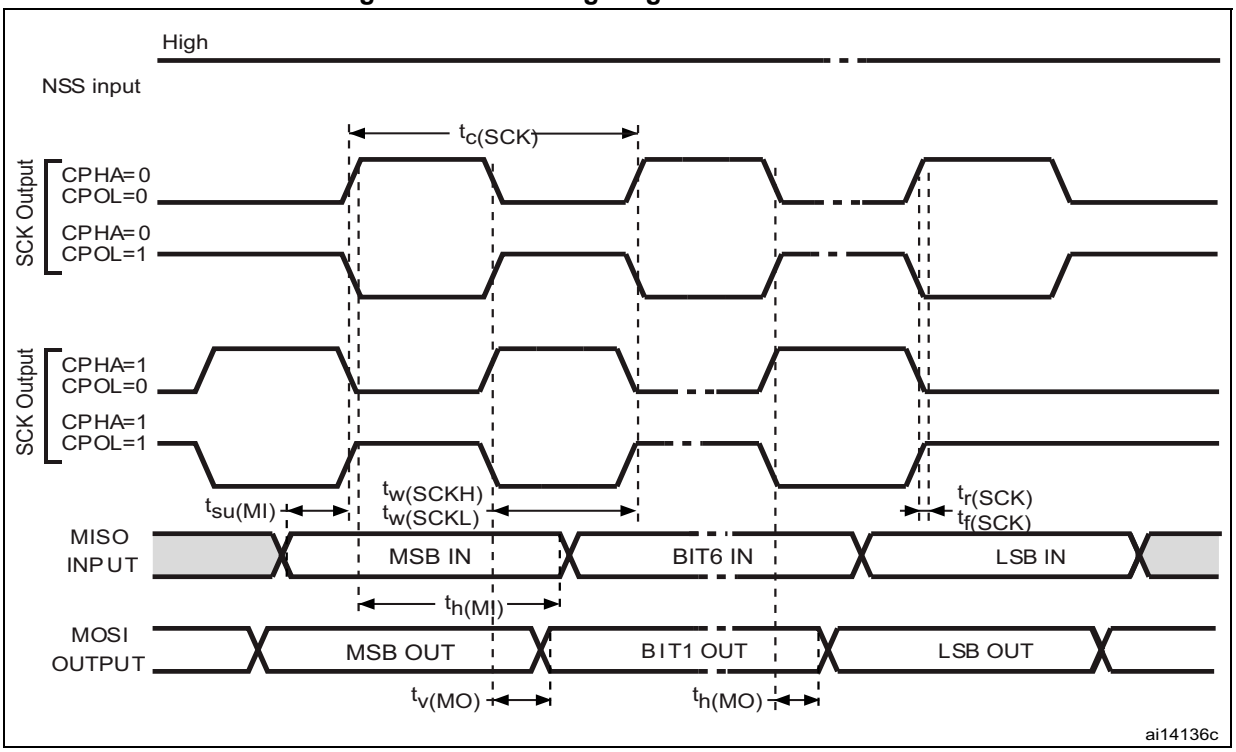
Figure 40. SPI timing diagram where slave mode and CPHA = 1



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

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Figure 41. SPI timing diagram - master mode



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

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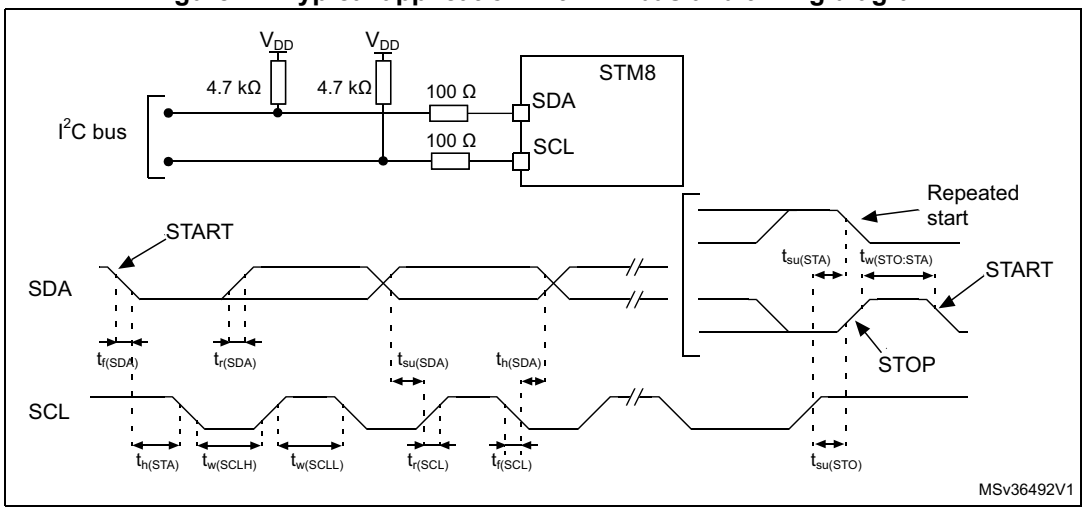
10.3.9 I²C interface characteristics

Table 44. I²C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	-	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time (V_{DD} = 3 to 5.5 V)	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time (V_{DD} = 3 to 5.5 V)	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{MASTER}, must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

Figure 42. Typical application with I²C bus and timing diagram



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10.3.10 10-bit ADC characteristics

Subject to general operating conditions for V_{DD}, f_{MASTER}, and T_A unless otherwise specified.

Table 45. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	V_{DD}= 2.95 to 5.5 V	1	-	4	MHz
		V_{DD}= 4.5 to 5.5 V	1	-	6	
V_{AIN}	Conversion voltage range(1)	-	V_{SS}	-	V_{DD}	V
C_{ADC}	Internal sample and hold capacitor	-	-	3	-	pF
t_S(1)	Minimum sampling time	f_{ADC} = 4 MHz	-	0.75	-	µs
		f_{ADC} = 6 MHz	-	0.5	-	
t_{STAB}	Wakeup time from standby	-	-	7.0	-	µs
t_{CONV}	Minimum total conversion time (including sampling time, 10-bit resolution)	f_{ADC} = 4 MHz	3.5			µs
		f_{ADC} = 6 MHz	2.33			µs
		-	14			$1/f_{ADC}$

1. During the sample time, the sampling capacitance, C_{AIN} (3 pF max), can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

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Table 46. ADC accuracy with R_{AIN}< 10 kΩ, V_{DD}= 5 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.6	3.5	LSB
		f_{ADC} = 4 MHz	2.2	4	
		f_{ADC} = 6 MHz	2.4	4.5	
$\|E_O\|$	Offset error(2)	f_{ADC} = 2 MHz	1.1	2.5	
		f_{ADC} = 4 MHz	1.5	3	
		f_{ADC} = 6 MHz	1.8	3	
$\|E_G\|$	Gain error(2)	f_{ADC} = 2 MHz	1.5	3	
		f_{ADC} = 4 MHz	2.1	3	
		f_{ADC} = 6 MHz	2.2	4	
$\|E_D\|$	Differential linearity error(2)	f_{ADC} = 2 MHz	0.7	1.5	
		f_{ADC} = 4 MHz	0.7	1.5	
		f_{ADC} = 6 MHz	0.7	1.5	
$\|E_L\|$	Integral linearity error(2)	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.8	2	
		f_{ADC} = 6 MHz	0.8	2	

1. Guaranteed by characterization results.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.

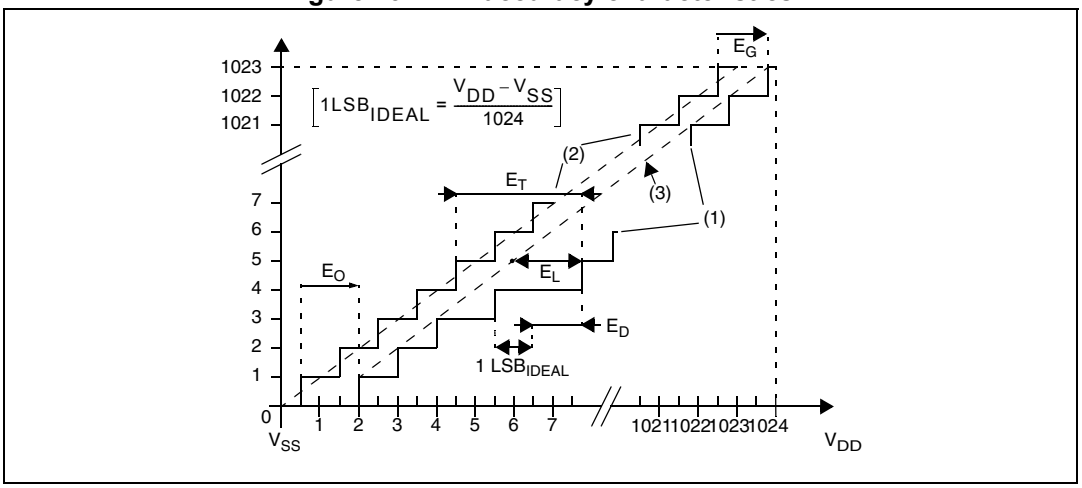
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Table 47. ADC accuracy with R_{AIN}< 10 kΩ, V_{DD}= 3.3 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.6	3.5	LSB
		f_{ADC} = 4 MHz	1.9	4	
$\|E_O\|$	Offset error(2)	f_{ADC} = 2 MHz	1	2.5	
		f_{ADC} = 4 MHz	1.5	2.5	
$\|E_G\|$	Gain error(2)	f_{ADC} = 2 MHz	1.3	3	
		f_{ADC} = 4 MHz	2	3	
$\|E_D\|$	Differential linearity error(2)	f_{ADC} = 2 MHz	0.7	1.0	
		f_{ADC} = 4 MHz	0.7	1.5	
$\|E_L\|$	Integral linearity error(2)	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.8	2	

1. Guaranteed by characterization results.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.

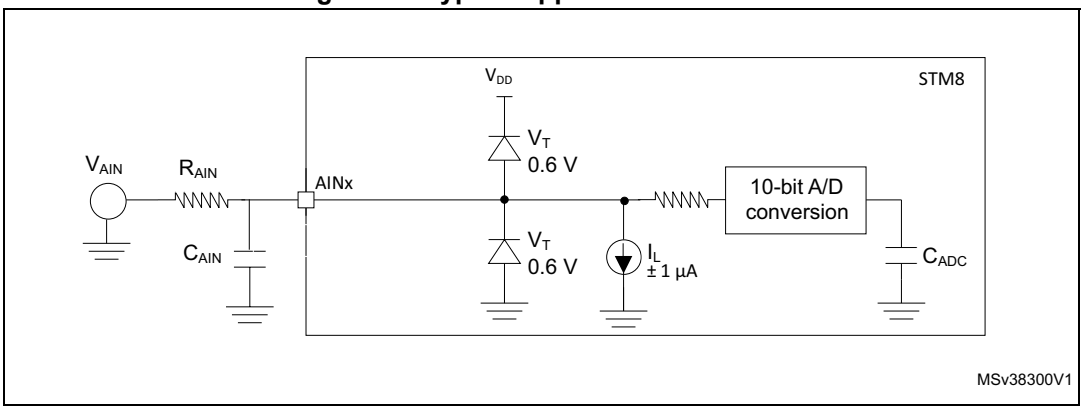
Figure 43. ADC accuracy characteristics



1. Example of an actual transfer curve
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: deviation between the first actual transition and the first ideal one.
   E_G = Gain error: deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

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Figure 44. Typical application with ADC



1. Legend: R_{AIN} = external resistance, C_{AIN} = capacitors, C_{samp} = internal sample and hold capacitor.

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10.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709 (EMC design guide for STM microcontrollers).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring. See application note AN1015 (Software techniques for improving microcontroller EMC performance).

Table 48. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 61000-4-2	2/B(1)
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 61000-4-4	4/A(1)

1. Data obtained with HSI clock configuration, after applying the hardware recommendations described in AN2860 (EMC guidelines for STM8S microcontrollers).

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Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC 61967-2 which specifies the board and the loading of each pin.

Table 49. EMI data

Symbol	Parameter	Conditions				Unit
		General conditions	Monitored frequency band	Max f_{CPU}(1)		
				16 MHz/ 8 MHz	16 MHz/ 16 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP32 package. Conforming to IEC 61967-2	0.1 MHz to 30 MHz	5	5	dBµV
			30 MHz to 130 MHz	4	5	
			130 MHz to 1 GHz	5	5	
	EMI level		EMI level	2.5	2.5	-

1. Guaranteed by characterization results.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD, DLU and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts x (n+1) supply pin). One model can be simulated: Human body model. This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 50. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to JESD22-A114	A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A= 25°C, conforming to SD22-C101 LQFP32 package	IV	1000	

1. Guaranteed by characterization results

Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin), and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

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This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 51. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A = 25 °C	A
		T_A = 85 °C	
		T_A = 125 °C	

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

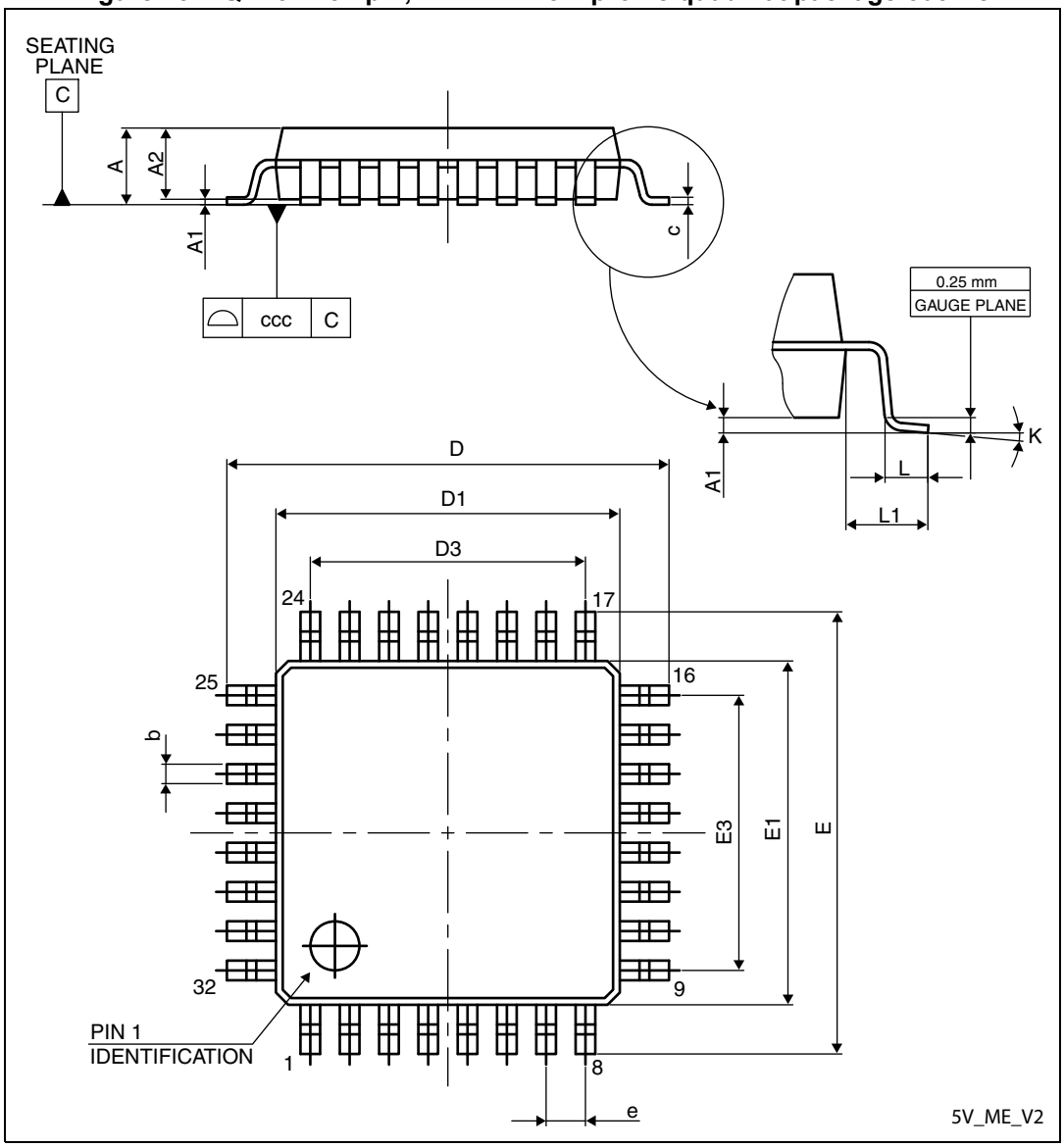
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11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

11.1 LQFP32 package information

Figure 45. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

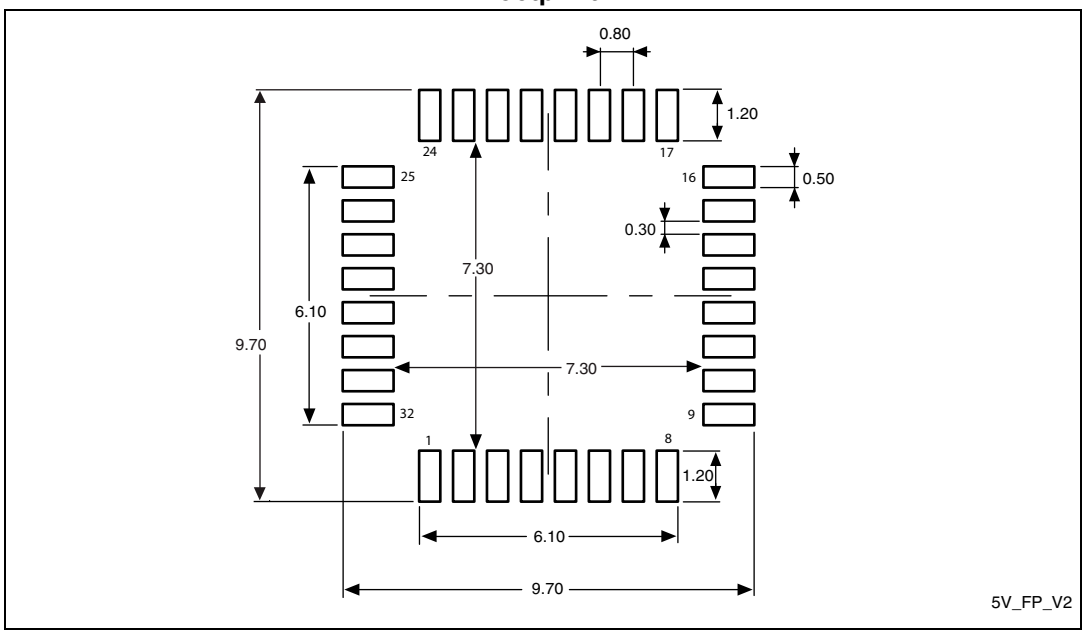
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Table 52. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 46. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

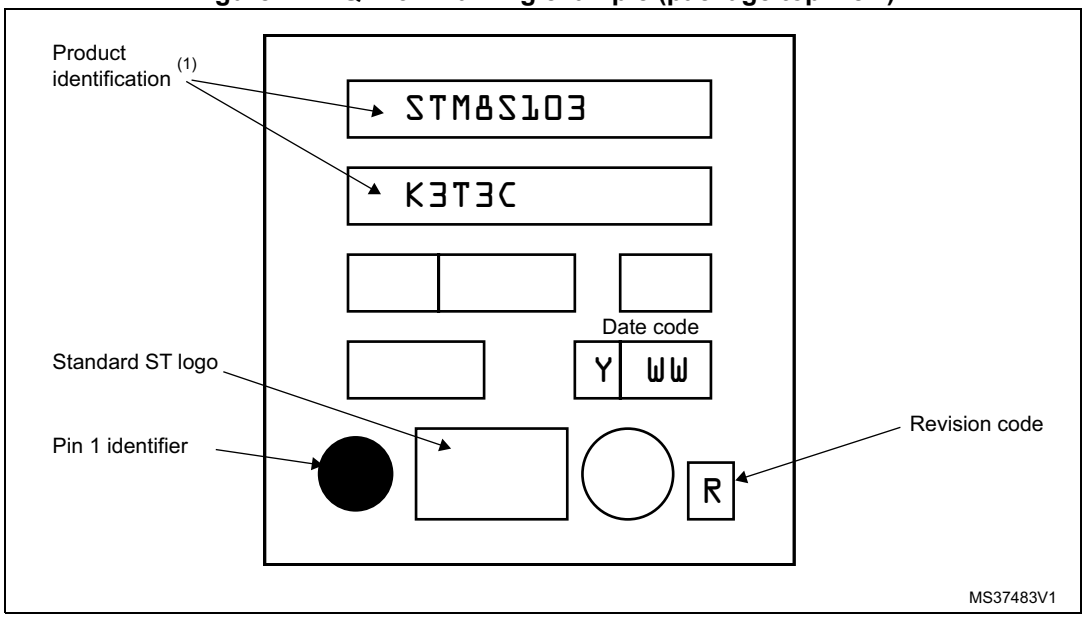
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Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 47. LQFP32 marking example (package top view)

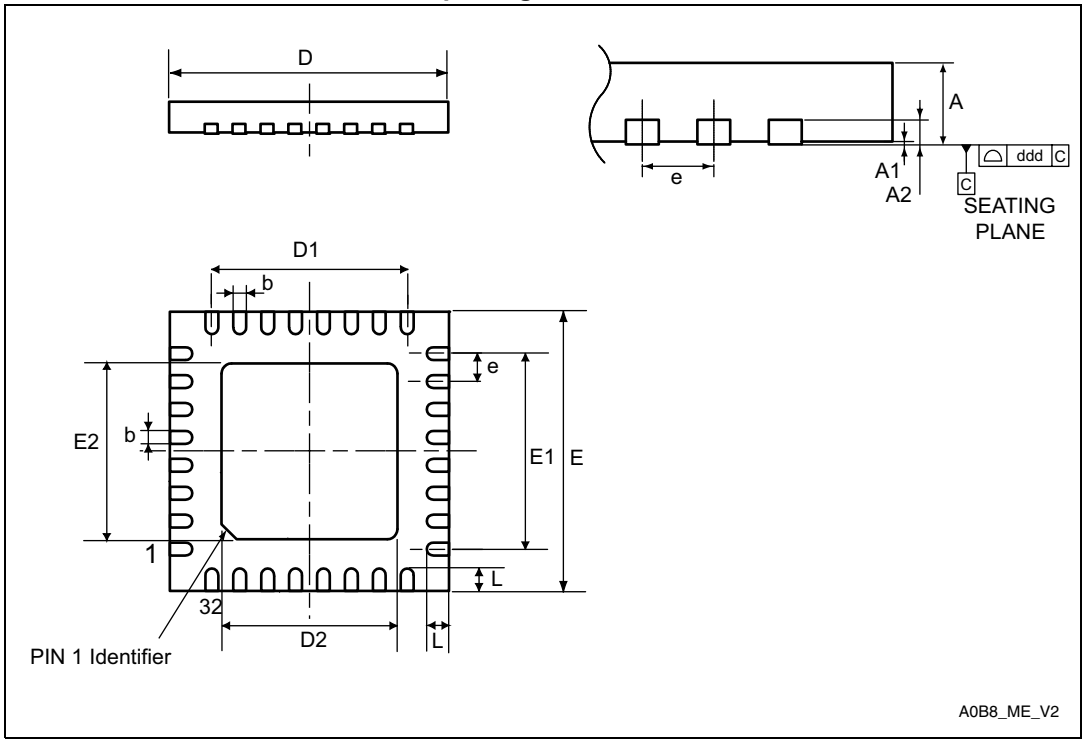


1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

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11.2 UFQFPN32 package information

Figure 48. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.
2. All leads/pads should be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this backside pad to PCB ground.
4. Dimensions are in millimeters.

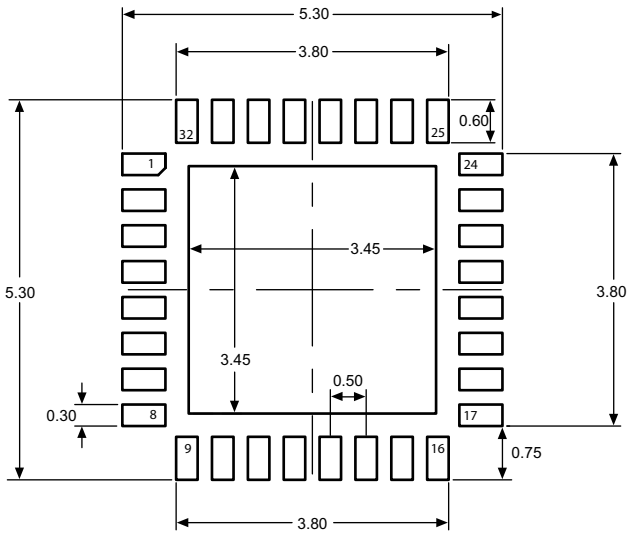
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Table 53. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 49. UFQFPN32 - 32-pin, 5 x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Section 11.7: UFQFPN recommended footprint shows the recommended footprints for UFQFPN with and without on-board emulation.

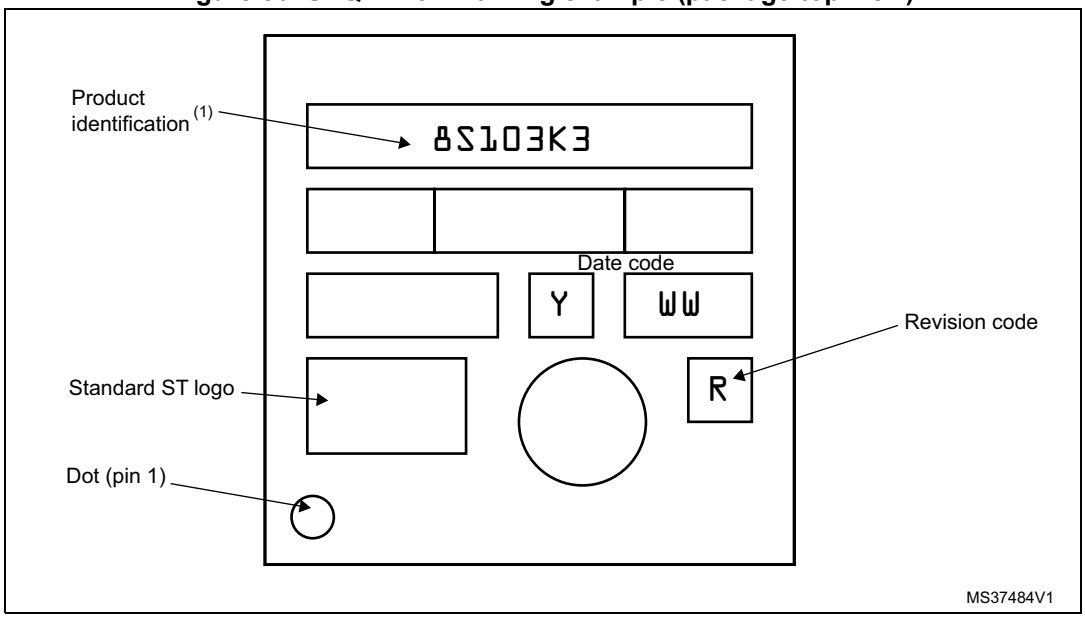
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Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 50. UFQFPN32 marking example (package top view)

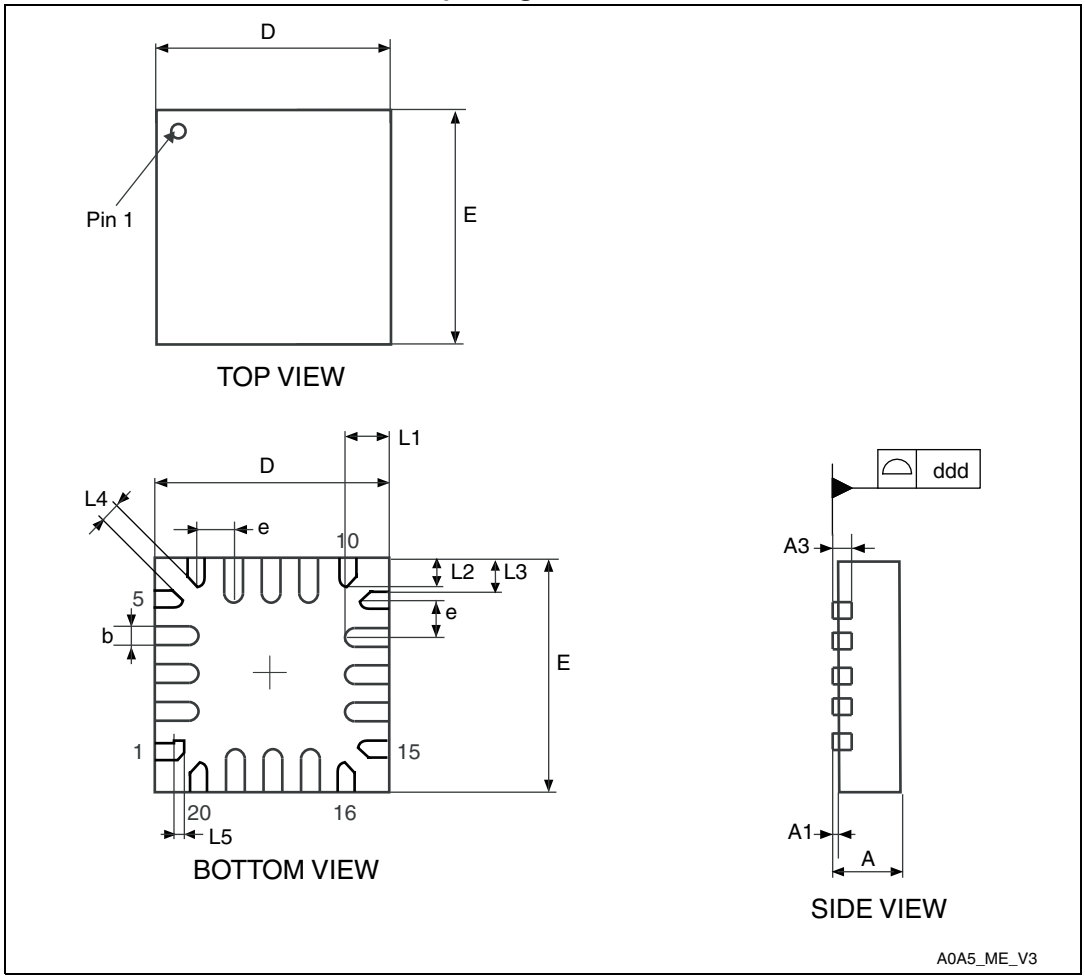


1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

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11.3 UFQFPN20 package information

Figure 51. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.

Table 54. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.060	-
D	2.900	3.000	3.100	0.1142	0.1181	0.1220
E	2.900	3.000	3.100	0.1142	0.1181	0.1220
L1	0.500	0.550	0.600	0.0197	0.0217	0.0236
L2	0.300	0.350	0.400	0.0118	0.0138	0.0157

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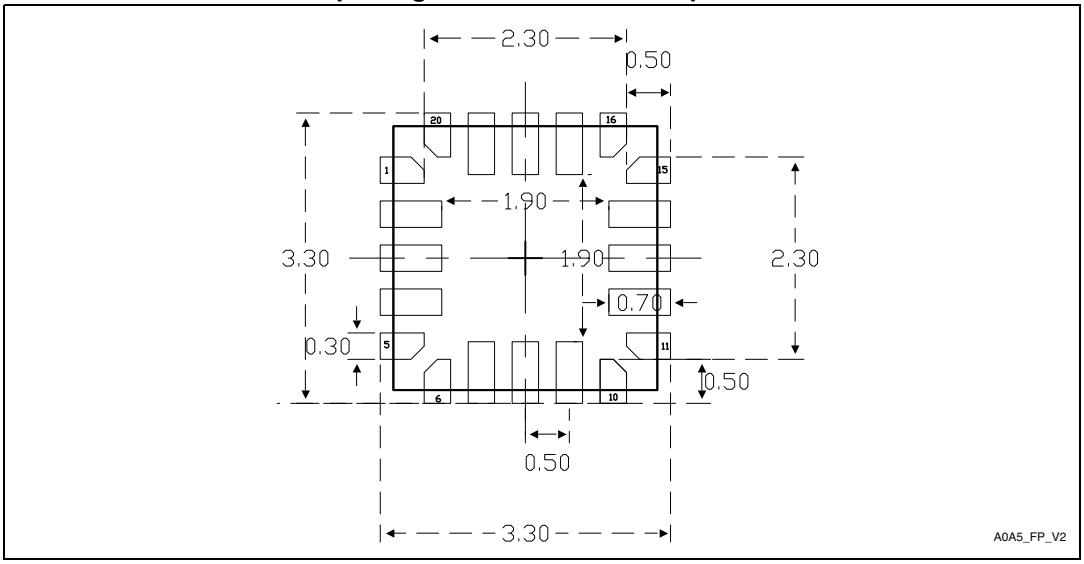
Table 54. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data (continued)

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
L3	-	0.375	-	-	0.0148	-
L4	-	0.200	-	-	0.0079	-
L5	-	0.150	-	-	0.0059	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits

Section 11.7: UFQFPN recommended footprint shows the recommended footprints for UFQFPN with and without on-board emulation.

Figure 52. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

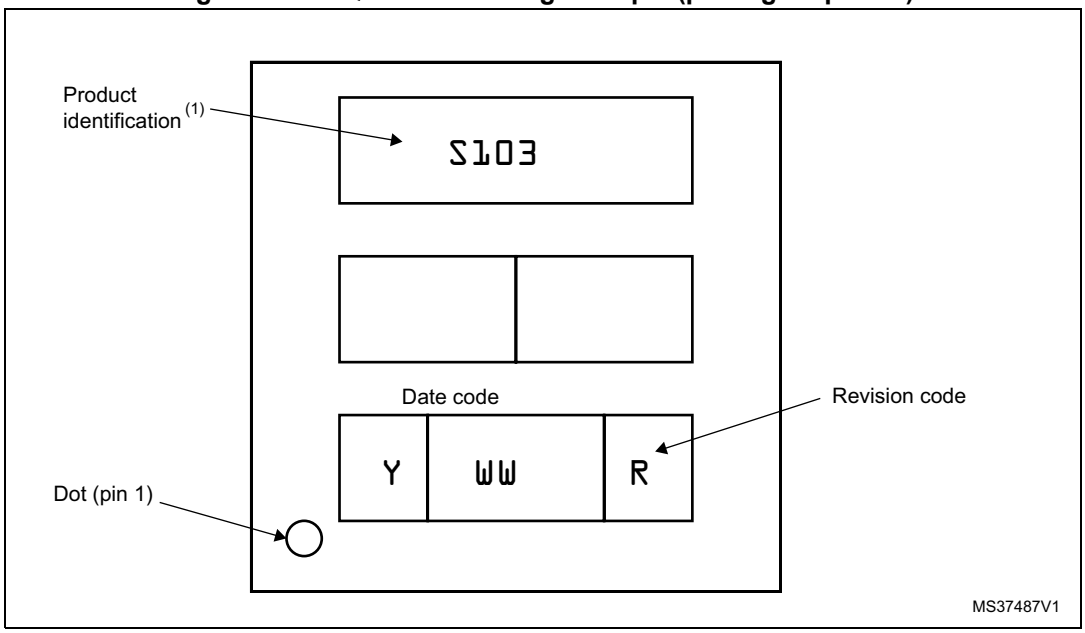
Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

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Figure 53. UFQFPN20 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

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11.4 SDIP32 package information

Figure 54. SDIP32 package outline

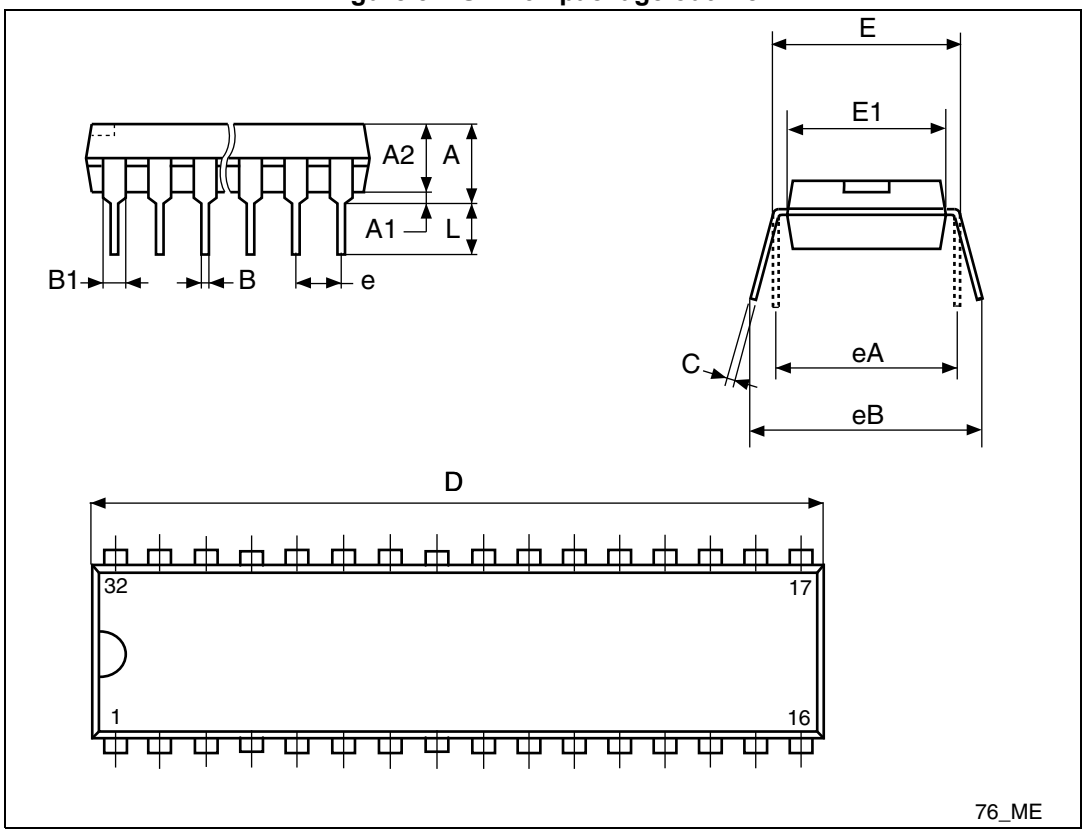


Table 55. SDIP32 package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	3.556	3.759	5.080	0.1400	0.1480	0.2000
A1	0.508	-	-	0.0200	-	-
A2	3.048	3.556	4.572	0.1200	0.1400	0.1800
B	0.356	0.457	0.584	0.0140	0.0180	0.0230
B1	0.762	1.016	1.397	0.0300	0.0400	0.0550
C	0.203	0.254	0.356	0.0079	0.0100	0.0140
D	27.430	27.940	28.450	1.0799	1.1000	1.1201
E	9.906	10.410	11.050	0.3900	0.4098	0.4350
E1	7.620	8.890	9.398	0.3000	0.3500	0.3700
e	-	1.778	-	-	0.0700	-
eA	-	10.160	-	-	0.4000	-

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Table 55. SDIP32 package mechanical data (continued)

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
eB	-	-	12.700	-	-	0.5000
L	2.540	3.048	3.810	0.1000	0.1200	0.1500

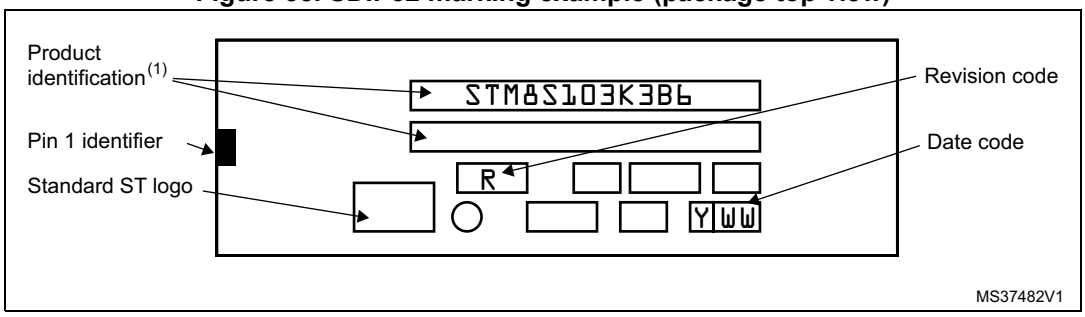
1. Values in inches are converted from mm and rounded to 4 decimal digits

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 55. SDIP32 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

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11.5 TSSOP20 package information

Figure 56. TSSOP20 package outline

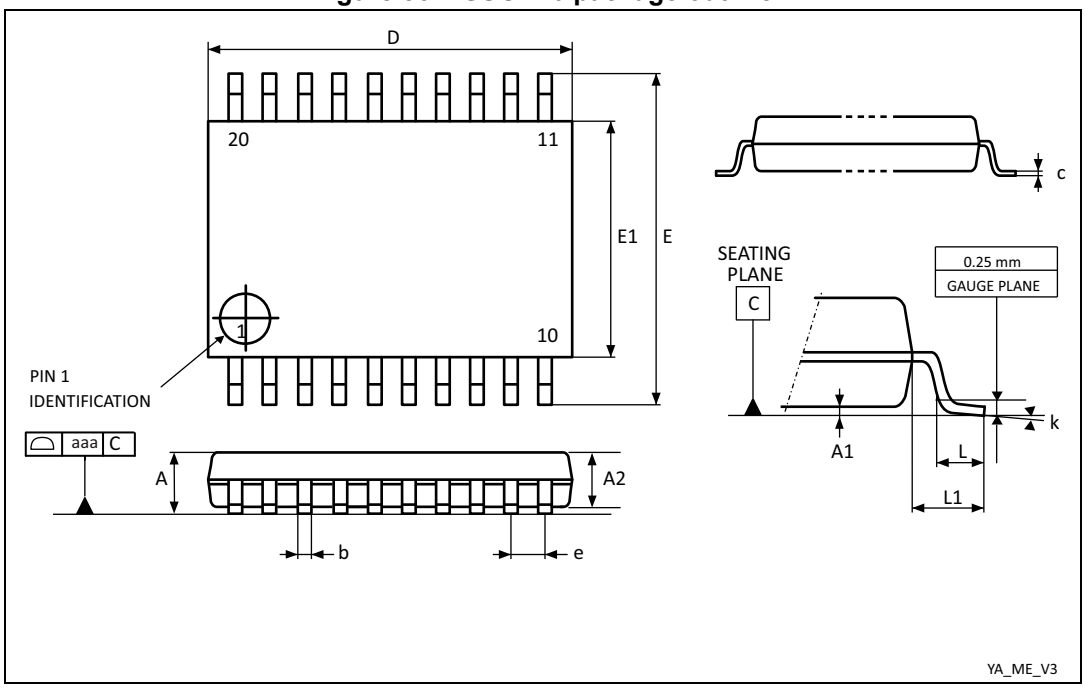


Table 56. TSSOP20 package mechanical data

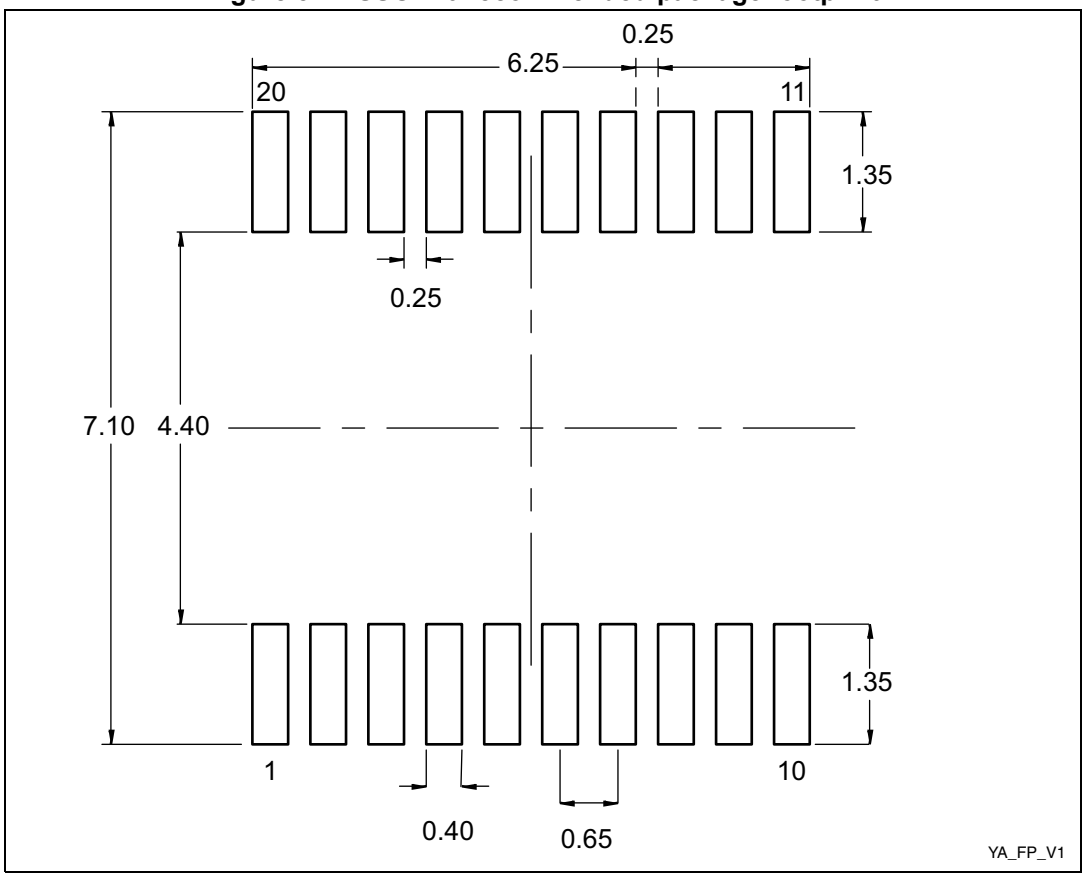
Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D[2]	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1[3]	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	-	8.0°	0.0°	-	8.0°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

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3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 57. TSSOP20 recommended package footprint



1. Dimensions are expressed in millimeters.

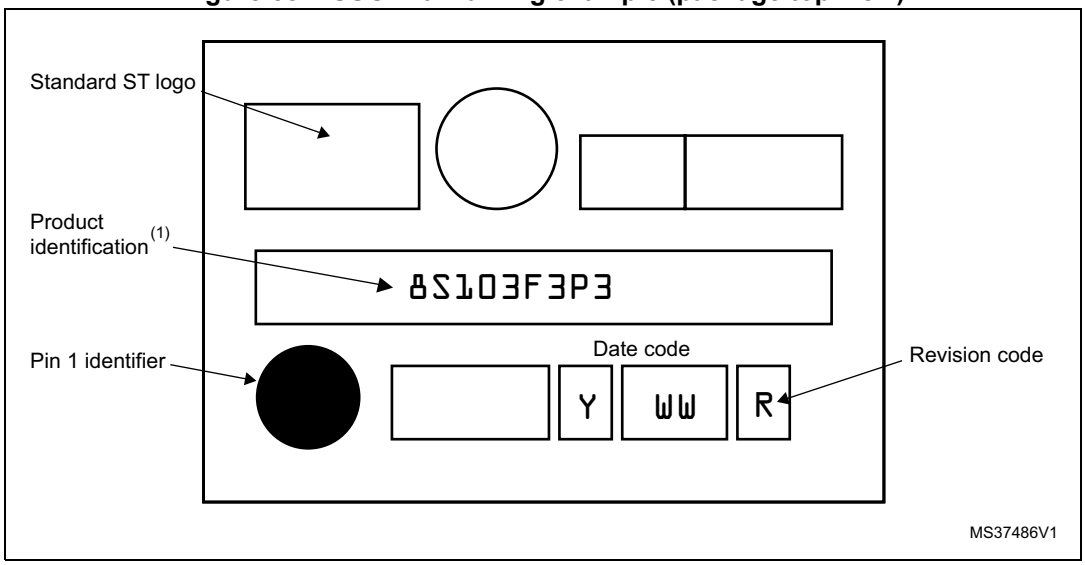
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Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 58. TSSOP20 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

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11.6 SO20 package information

Figure 59. SO20 package outline

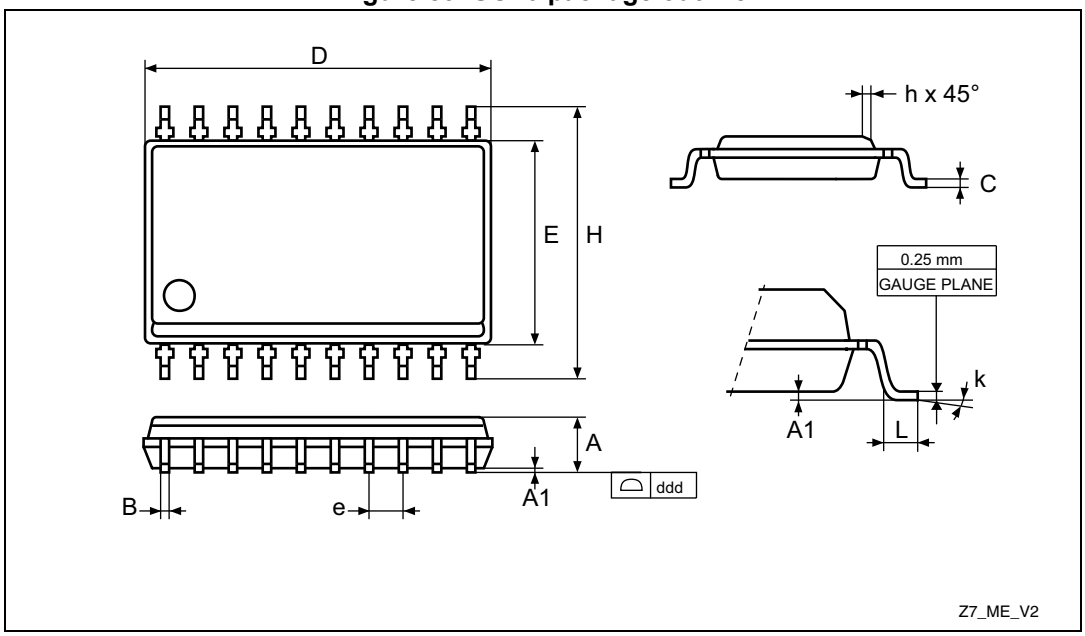


Table 57. SO20 mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	2.350	-	2.650	0.0925	-	0.1043
A1	0.100	-	0.300	0.0039	-	0.0118
B	0.330	-	0.510	0.013	-	0.0201
C	0.230	-	0.320	0.0091	-	0.0126
D	12.600	-	13.000	0.4961	-	0.5118
E	7.400	-	7.600	0.2913	-	0.2992
e	-	1.270	-	-	0.0500	-
H	10.000	-	10.650	0.3937	-	0.4193
h	0.250	-	0.750	0.0098	-	0.0295
L	0.400	-	1.270	0.0157	-	0.0500
k	0.0°	-	8.0°	0.0°	-	8.0°
ddd	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

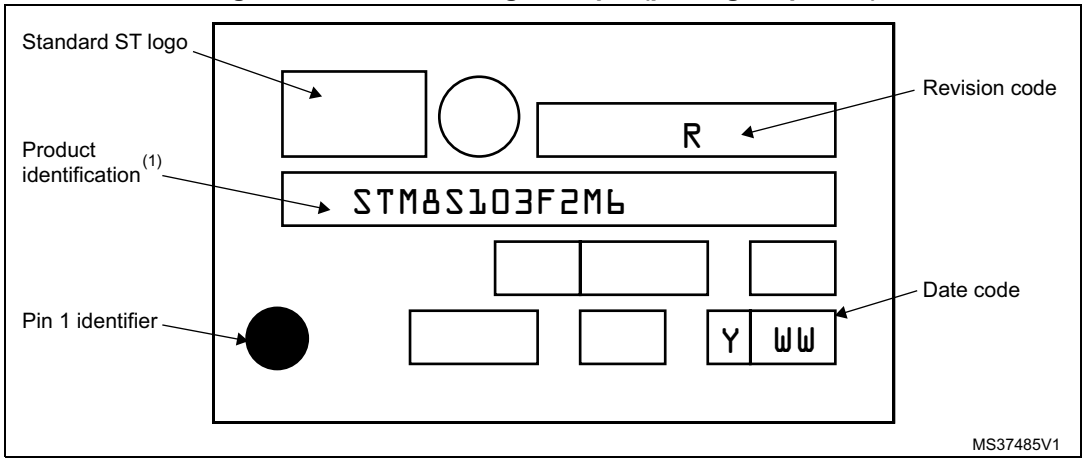
Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

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Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

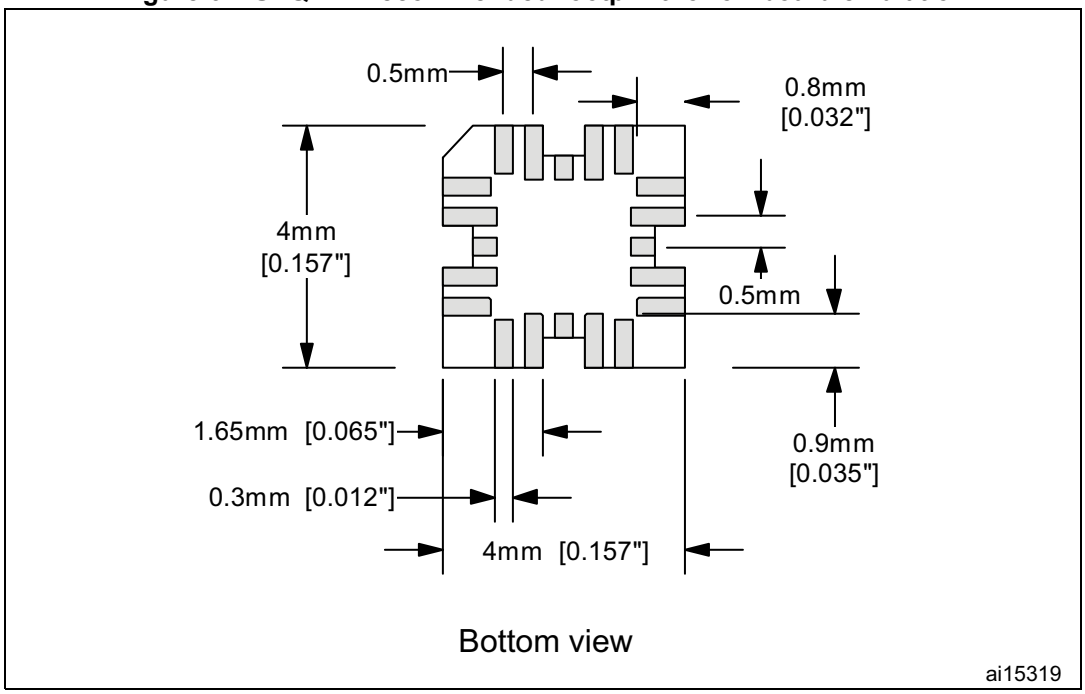
Figure 60. SO20 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

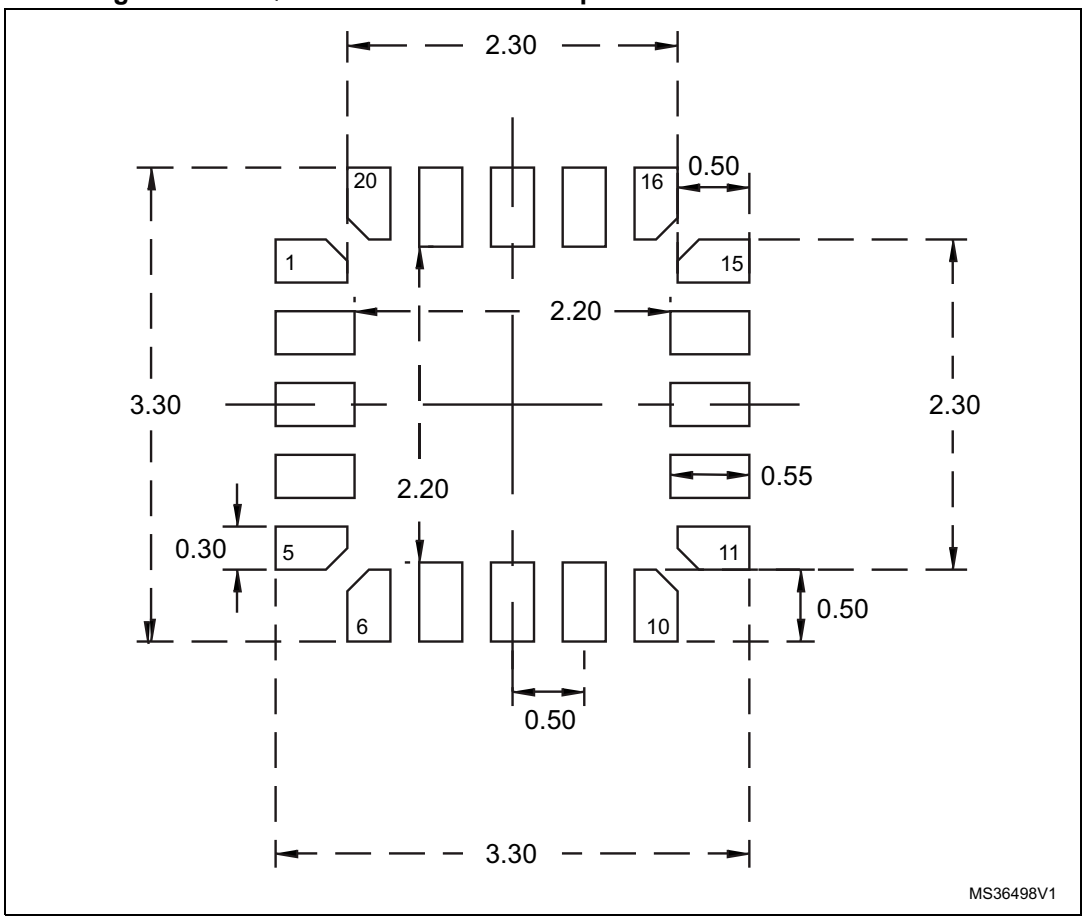
11.7 UFQFPN recommended footprint

Figure 61. UFQFPN recommended footprint for on-board emulation



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Figure 62. UFQFPN recommended footprint without on-board emulation



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12 Thermal characteristics

The maximum junction temperature (T_{Jmax}) of the device must never exceed the values specified in *Table 19: General operating conditions*, otherwise the functionality of the device cannot be guaranteed.

The maximum junction temperature T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 58. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient TSSOP20 - 4.4mm	84	°C/W
	Thermal resistance junction-ambient SO20W (300 mils)	91	
	Thermal resistance junction-ambient UFQFPN20 - 3 x 3 mm	90	
	Thermal resistance junction-ambient LQFP32 - 7 x 7 mm	60	
	Thermal resistance junction-ambient UFQFPN32 - 5 x 5 mm	38	
	Thermal resistance junction-ambient SDIP32 - 400 mils	60	

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

12.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

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12.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see *Section 13: Ordering information*).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax}= 75°C (measured according to JESD51-2), I_{DDmax} = 8 mA, V_{DD} = 5 V, maximum 20 I/Os used at the same time in output at low level with

I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 8 mA x 5 V= 400 mW

P_{IOmax} = 20 x 8 mA x 0.4 V = 64 mW

This gives: P_{INTmax} = 400 mW and P_{IOmax} 64 mW:

P_{Dmax} = 400 mW + 64 mW

Thus: P_{Dmax} = 464 mW.

Using the values obtained in *Table 58: Thermal characteristics on page 106* T_{Jmax} is calculated as follows:

For LQFP32 60 °C/W

T_{Jmax} = 75 °C + (60 °C/W x 464 mW) = 75 °C + 27.8 °C = 102.8 °C

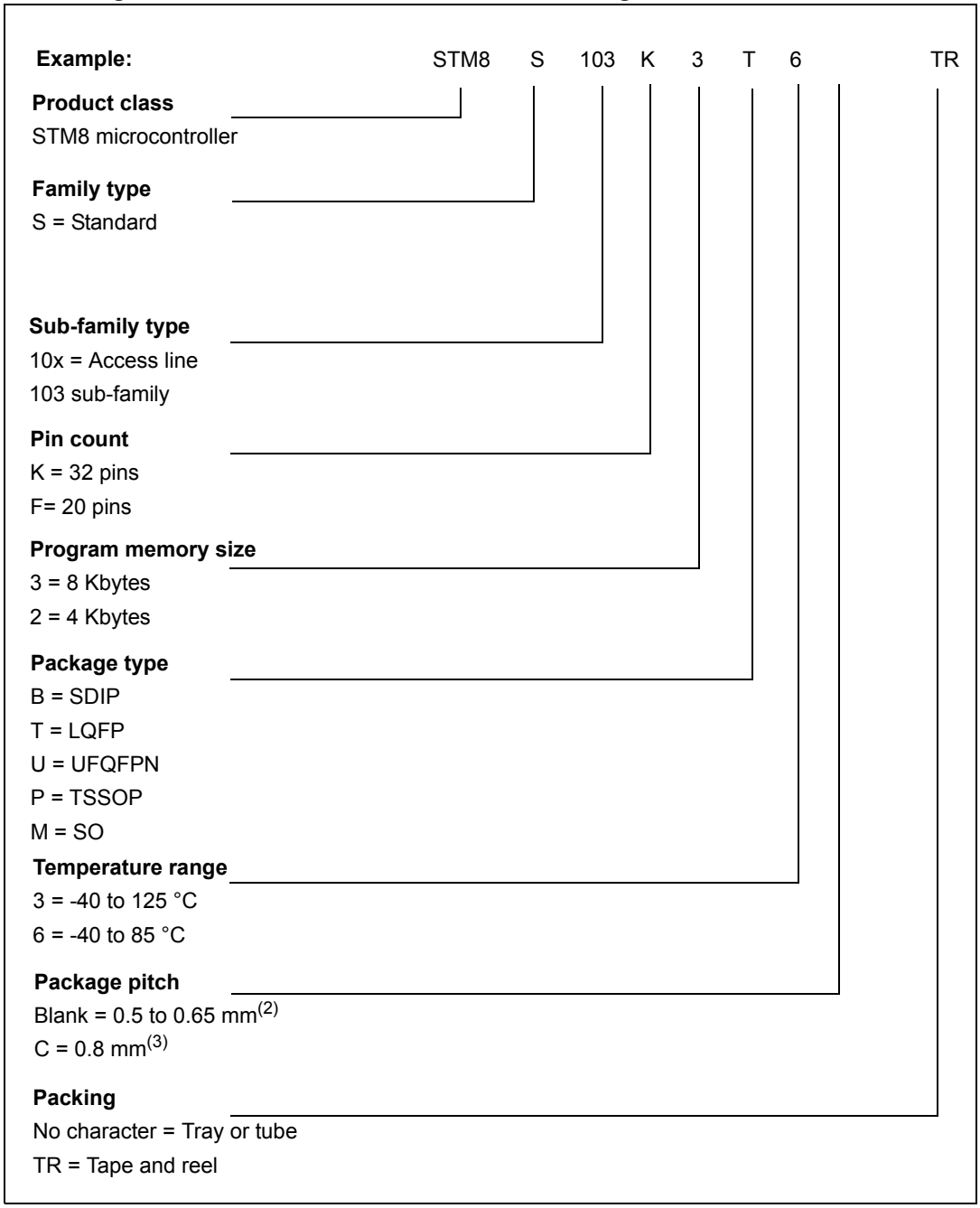
This is within the range of the suffix 6 version parts (-40 < T_J < 105 °C).

Parts must be ordered at least with the temperature range suffix 6.

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13 Ordering information

Figure 63. STM8S103F2/x3 access line ordering information scheme(1)



1. A dedicated ordering information scheme will be released if, in the future, memory programming service (FastROM) is required The letter “P” will be added after STM8S. Three unique letters identifying the customer application code will also be visible in the codification. Example: STM8SP103K3MACTR.
2. UFQFPN, TSSOP, and SO packages.
3. LQFP package.

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For a list of available options (for example memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.

13.1 STM8S103 FASTROM microcontroller option list

(last update: April 2010)

Customer	.....
Address	.....
Contact	.....
Phone number	.....
FASTROM code reference(1)	.....

1. The FASTROM code name is assigned by STMicroelectronics.

The preferable format for programing code is .hex (.s19 is accepted)

If data EEPROM programing is required, a separate file must be sent with the requested data.

Note: See the option byte section in the datasheet for authorized option byte combinations and a detailed explanation. Do not use more than one remapping option in the same port. It is forbidden to enable both AFR1 and AFR0.

Device type/memory size/package (check only one option)

FASTROM device	4 Kbyte	8 Kbyte
LQFP32	-	[ ] STM8S103K3
UFQFPN20	[ ] STM8S103F2	[ ] STM8S103F3
UFQFPN32	-	[ ] STM8S103K3
TSSOP20	[ ] STM8S103F2	[ ] STM8S103F3
SO20W	[ ] STM8S103F2	[ ] STM8S103F3

Conditioning (check only one option)

[ ] Tape and reel or [ ] Tray

Special marking (check only one option)

[ ] No [ ] Yes

Authorized characters are letters, digits, '.', '-', '/' and spaces only. Maximum character counts are:

UFQFPN20: 1 line of 4 characters max: “_ _ _ _”

UFQFPN32: 1 line of 7 characters max: “_ _ _ _ _ _ _”

LQFP32: 2 lines of 7 characters max: “_ _ _ _ _ _ _” and “_ _ _ _ _ _ _”

TSSOP20/SO20: 1 line of 10 characters max: “_ _ _ _ _ _ _ _ _ _”

Three characters are reserved for code identification.

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Temperature range

[ ] -40°C to +85°C or [ ] -40°C to +125°C

Padding value for unused program memory (check only one option)

[ ] 0xFF	Fixed value
[ ] 0x83	TRAP instruction code
[ ] 0x75	Illegal opcode (causes a reset when executed)

OTP0 memory readout protection (check only one option)

[ ] Disable or [ ] Enable

OTP1 user boot code area (UBC)

0x(_ _) fill in the hexadecimal value, referring to the datasheet and the binary format below:

UBC, bit0	[ ] 0: Reset [ ] 1: Set
UBC, bit1	[ ] 0: Reset [ ] 1: Set
UBC, bit2	[ ] 0: Reset [ ] 1: Set
UBC, bit3	[ ] 0: Reset [ ] 1: Set
UBC, bit4	[ ] 0: Reset [ ] 1: Set
UBC, bit5	[ ] 0: Reset [ ] 1: Set
UBC, bit6	[ ] 0: Reset [ ] 1: Set
UBC, bit7	[ ] 0: Reset [ ] 1: Set

OTP0 memory readout protection (check only one option)

[ ] Disable or [ ] Enable

OTP2 alternate function remapping for STM8S103K

Do not use more than one remapping option in the same port. It is forbidden to enable both AFR1 and AFR0.

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AFR0	Reserved
AFR1 (check only one option)	[ ] 1: Port A3 alternate function = SPI_NSS and port D2 alternate function = TIM2_CH3 [ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description
AFR2	Reserved
AFR3	Reserved
AFR4	Reserved
AFR5 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port D0 alternate function = CLK_CCO
AFR6 (check only one option)	[ ] 0: Remapping option inactive. Default alternate functions used. Refer to pinout description [ ] 1: Port D7 alternate function = TIM1_CH4
AFR7	Reserved

OPT3 watchdog

WWDG_HALT (check only one option)	[ ] 0: No reset generated on halt if WWDG active[[ ] 1: Reset generated on halt if WWDG active
WWDG_HW (check only one option)	[ ] 0: WWDG activated by software [ ] 1: WWDG activated by hardware
IWDG_HW (check only one option)	[ ] 0: IWDG activated by software [ ] 1: IWDG activated by hardware
LSI_EN (check only one option)	[ ] 0: LSI clock is not available as CPU clock source [ ] 1: LSI clock is available as CPU clock source
HSITRIM (check only one option)	[ ] 0: 3-bit trimming supported in CLK_HSITRIMR register [ ] 1: 4-bit trimming supported in CLK_HSITRIMR register

OPT4 watchdog

PRSC (check only one option)	[ ] for 16 MHz to 128 kHz prescaler [ ] for 8 MHz to 128 kHz prescaler [ ] for 4 MHz to 128 kHz prescaler
CKAWUSEL (check only one option)	[ ] LSI clock source selected for AWU [ ] HSE clock with prescaler selected as clock source for AWU
EXTCLK (check only one option)	[ ] External crystal connected to OSCIN/OSCOUT [ ] External signal on OSCIN

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OPT5 crystal oscillator stabilization HSECNT (check only one option)

[ ] 2048 HSE cycles

[ ] 128 HSE cycles

[ ] 8 HSE cycles

[ ] 0.5 HSE cycles

OTP6 is reserved

Comments:	.....
Supply operating range in the application:	.....
Notes:	.....
Date:	.....
Signature:	.....

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14 STM8 development tools

Development tools for the STM8 microcontrollers include the full-featured STice emulation system supported by a complete software tool package including C compiler, assembler and integrated development environment with high-level language debugger. In addition, the STM8 is to be supported by a complete range of tools including starter kits, evaluation boards and a low-cost in-circuit debugger/programmer.

14.1 Emulation and in-circuit debugging tools

The STice emulation system offers a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8 application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including profiling and coverage to help detect and eliminate bottlenecks in application execution and dead code when fine tuning an application.

In addition, STice offers in-circuit debugging and programming of STM8 microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows you to order exactly what you need to meet your development requirements and to adapt your emulation system to support existing and future ST microcontrollers.

14.1.1 STice key features

- Occurrence and time profiling and code coverage (new features),
- Advanced breakpoints with up to 4 levels of conditions,
- Data breakpoints,
- Program and data trace recording up to 128 KB records,
- Read/write on the fly of memory during emulation,
- In-circuit debugging/programming via SWIM protocol,
- 8-bit probe analyzer,
- 1 input and 2 output triggers,
- Power supply follower managing application voltages between 1.62 to 5.5 V,
- Modularity that allows you to specify the components you need to meet your development requirements and adapt to future requirements.
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.

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14.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8, which are available in a free version that outputs up to 16 Kbytes of code.

14.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8 Flash program memory, data EEPROM and option bytes. STVP also offers project mode for the saving of programming configurations and the automation of programming sequences.

14.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of user applications directly from an easy-to-use graphical interface.

Available toolchains include:

C compiler for STM8

Available in a free version that outputs up to 16 Kbytes of code. For more information, see www.cosmic-software.com.

STM8 assembler linker

Free assembly toolchain included in the STVD toolset, used to assemble and link the user application source code.

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14.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on the application board via the SWIM protocol. Additional tools include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for the STM8 programming.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

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15 Revision history

Table 59. Document revision history

Date	Revision	Changes
02-Mar-2009	1	Initial release.
10-Apr-2009	2	Added *Table 2: Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers*. Updated *Section 4.8: Auto wakeup counter*. Modified the description of PB4 and PB5 (removed X in PP column) and added footnote concerning HS I/Os in *Section 5.1: STM8S103K3 UFQFPN32/LQFP32/SDIP32 pinout and pin description* and *Section 5.2: STM8S103F2/F3 TSSOP20/SO20/UFQFPN20 pinout and pin description*. Removed TIM3 and UART from *Table 10: Interrupt mapping*. Updated VCAP specifications in *Section 10.3.1: VCAP external capacitor* Corrected the block size in *Table 37: Flash program memory/data EEPROM memory*t Updated *Section 10: Electrical characteristics*. Updated *Section 12: Thermal characteristics*.
10-Jun-1999	3	Document status changed from “preliminary data” to “datasheet”. Replaced WFQFPN20 package with UFQFPN package. Replaced ‘VFQFN’ with ‘VFQFPN’. Added bullet point on the unique identifier to *Features*. Updated *Section 4.8: Auto wakeup counter*. Updated wpu and PP status of PB5/12C_SDA and PB4/12C_SCL pins in *Section 5.1: STM8S103K3 UFQFPN32/LQFP32/SDIP32 pinout and pin description* and *Section 5.2: STM8S103F2/F3 TSSOP20/SO20/UFQFPN20 pinout and pin description*. Removed Table 7: Pin-to-pin comparison of pin 7 to 12 in 32-pin access line devices. Updated *Section 6.1: Memory map*. Updated reset status of port D CR1 register in *Table 7: I/O port hardware register map*. Updated alternate function remapping descriptions in *Table 13: STM8S103K3 alternate function remapping bits for 32-pin devices* and *Table 14: STM8S103Fx alternate function remapping bits for 20-pin devices*. Added *Section 9: Unique ID*. Updated *Section 10.3: Operating conditions*. Updated the caption of *Figure 20: Typical HSI frequency variation vs V_{DD} @ 4 temperatures*. Updated *Table 43: SPI characteristics* and added TBD occurrences. Added max values to *Table 46: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 5 V* and *Table 47: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 3.3 V*. Updated *Section 10.3.11: EMC characteristics*.

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Table 59. Document revision history

Date	Revision	Changes
16-Oct-1999	4	Replaced VFQFPN32 package by UFQFPN32 package. – *Section 4.5: Clock controller*: replaced TIM2 and TIM3 with reserved and TIM2 respectively in *Table 2: Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers* – *Total current consumption in halt mode*: changed the maximum current consumption limit at 125 °C (and VDD= 5 V) from 35 µA to 55 µA. – *Functional EMS (electromagnetic susceptibility)*: renamed ESD as FESD (functional); added name of AN1709; replaced EC 1000 with IEC 61000. – *Designing hardened software to avoid noise problems*: replaced IEC 1000 with IEC 61000, added title of AN1015, and added footnote to EMS data table. – *Electromagnetic interference (EMI)*: replaced J 1752/3 with IEC 61967-2 and updated data of the EMI data table. – *Section 12.2: Selecting the product temperature range*: changed the value of LQFP32 7x7 mm thermal resistance from 59 °C/W to 60 °C/W. Added *Section 13.1: STM8S103 FASTROM microcontroller option list*.
22-Apr-2010	5	Added VFQFPN32 and SO20 packages. Updated Px_IDR reset value in *Table 7: I/O port hardware register map*. – *Section 10.3: Operating conditions*: updated VCAP and ESR low limit, added ESL parameter, and Note 1 below *Table 19: General operating conditions* Updated ACCHSI in *Table 34: HSI oscillator characteristics*. Modified IDD(H)inand. Removed note 3 related to Accuracy of HSI oscillator. Updated maximum power dissipation in *Table 19: General operating conditions*. Updated *Section 12: Thermal characteristics* Replaced package pitch digit by VFQFPN/UFQFPN package digit in *Figure 63: STM8S103F2/x3 access line ordering information scheme*(1), and removed note 1.

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Table 59. Document revision history

Date	Revision	Changes
09-Sep-2010	6	Removed VFQFPN32 package. Removed internal reference voltage from *Section 4.13: Analog-to-digital converter (ADC1)*. Updated the reset state information in *Table 4: Legend/abbreviations for pin description tables* in *Section 5: Pinout and pin description*. Added footnote to PD1/SWIM pin in *Table 5: STM8S103K3 pin descriptions*. Updated pins 14 and 19 (TSSOP20/SO20) / pins 11 and 16 (UFQFPN20) in *Table 6: STM8S103F2 and STM8S103F3 pin descriptions*. Standardized all reset state values; updated the reset state values of the RST_SR, CLK_SWCR, CLK_HSITRIMR, CLK_SWIMCCR, IWDG_KR, and ADC_DRx registers in *Table 8: General hardware register map*. Updated AFR2 description of OPT 2 in *Table 14: STM8S103Fx alternate function remapping bits for 20-pin devices*s. Replaced 0.01 µF with 0.1 µf in *Figure 38: Recommended reset pin protection*. Added *Figure 42: Typical application with I^2C bus and timing diagram* and *Table 44: I^2C characteristics*. Updated footnote 1 in *Table 46: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 5 V* and *Table 47: ADC accuracy with R_{AIN}< 10 kΩ V_{DD}= 3.3 V*. Updated the Special marking section in *Section 13.1: STM8S103 FASTROM microcontroller option list*: Updated AFR2 description of OTP2 in *Table 14: STM8S103Fx alternate function remapping bits for 20-pin devices* Updated existing footnote and added three additional footnotes to *Table 53: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data*
12-Jul-2011	7	Updated the note related to true open-drain outputs in *Table 6: STM8S103F2 and STM8S103F3 pin descriptions* Removed CLK_CANCCR register from *Table 8: General hardware register map*. Added note for Px_IDR registers in *Table 7: I/O port hardware register map*. Added recommendation concerning NRST pin level, and power consumption sensitive applications, above *Figure 38: Recommended reset pin protection*. Removed typical HSI accuracy curve in *Section 10.3.4: Internal clock sources and timing characteristics*. Renamed package type 2 into package pitch and added pitch code “C” in *Figure 63: STM8S103F2/x3 access line ordering information scheme(1)* and added UFQFPN20 in *Section 13.1: STM8S103 FASTROM microcontroller option list*. Updated the disclaimer.

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Table 59. Document revision history

Date	Revision	Changes
04-Apr-2012	8	Updated notes related to V_{CAP} in *Table 19: General operating conditions*. Added values of t_R/t_F for 50 pF load capacitance, and updated note in *Table 38: I/O static characteristics*. Updated typical and maximum values of R_{PU} in *Table 38: I/O static characteristics* and *Table 42: NRST pin characteristics*. Changed SCK input to SCK output in *Section 10.3.8: SPI serial peripheral interface* Modified *Figure 51: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline* to add package top view.
26-Jun-2012	9	Added *Section 11.4: SDIP32 package information*.
04-Feb-2015	10	Updated *Section 11.5: TSSOP20 package information* and *Section 11.3: UFQFPN20 package information*.
10-Mar-2015	11	Updated: – *Table 34: HSI oscillator characteristics*: corrected HSI oscillator accuracy (factory calibrated) for V_{DD} = 5 V and T_A = 25 °C. – *Table 38: I/O static characteristics*: corrected the max. value for T_R/T_F, Fast I/Os, Load = 50 pF. Added: – *Figure 23: Typical pull-up current vs V_{DD} @ 4 temperatures*, – the rows for T_R/T_F, Fast I/Os, Load = 20 pF in *Table 38: I/O static characteristics*, – *Figure 47: LQFP32 marking example (package top view)*, – *Figure 50: UFQFPN32 marking example (package top view)*, – *Figure 53: UFQFPN20 marking example (package top view)*, – *Figure 55: SDIP32 marking example (package top view)*, – *Figure 58: TSSOP20 marking example (package top view)*, – *Figure 60: SO20 marking example (package top view)*.
26-Mar-2015	12	Corrected the values for “b” dimensions in *Table 53: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data*.

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Table 59. Document revision history

Date	Revision	Changes
03-Oct-2016	13	Updated: – Name of “LQFP32 package” to “LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package” on *Table 52: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data*, *Figure 45: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline* and *Figure 46: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint* – *Section 10.2: Absolute maximum ratings* – *Section 10.3.10: 10-bit ADC characteristics* – *Figure 40: SPI timing diagram where slave mode and CPHA = 1* – *Figure 41: SPI timing diagram - master mode* – *Figure 43: ADC accuracy characteristics* – *Figure 63: STM8S103F2/x3 access line ordering information scheme*(1): corrected package name from VFQFPN to UFQFPN – *Table 8: General hardware register map* – *Table 16: Voltage characteristics* – *Table 17: Current characteristics* – *Table 19: General operating conditions* – *Table 20: Operating conditions at power-up/power-down* – *Table 21: Total current consumption with code execution in run mode at V_{DD} = 5 V* – *Table 31: Peripheral current consumption* – *Table 49: EMI data* – Updated footnotes on *Table 18: Thermal characteristics*, *Table 38: I/O static characteristics*, *Table 43: SPI characteristics*, *Figure 45: LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline*, *Figure 48: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline*. – Updated all the “Device marking” sections on *Section 11: Package information*
13-Feb-2017	14	Updated: – *Section 10.2: Absolute maximum ratings* – *Section 11.3: UFQFPN20 package information* – *Table 5: STM8S103K3 pin descriptions* – *Table 6: STM8S103F2 and STM8S103F3 pin descriptions* – *Table 21: Total current consumption with code execution in run mode at V_{DD} = 5 V* – Footnotes in all tables of *Section 10: Electrical characteristics* Added: – *Figure 52: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint*

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