EPSON TOYOCOM

Application Manual

Real Time Clock Module

RX-4571SA

EPSON TOYOCOM CORPORATION

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com
微信扫码咨询客服

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深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
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Contents

1. Overview.....1

2. Block Diagram 1

3. Terminal description 2
3.1. Terminal connections..... 2
3.2. Pin Functions..... 2

4. External Dimensions / Marking Layout 3

5. Absolute Maximum Ratings 4

6. Recommended Operating Conditions.....4

7. Frequency Characteristics 4

8. Electrical Characteristics 5
8.1. DC characteristics..... 5
8.2. AC characteristics..... 6

9. Matters that demand special attention on use 7
9.1. VDD and CE timing..... 7
9.2. Migrating to backup, and returning 7
9.3. Restrictions on Access Operations During Power-on Initialization and Recovery from Backup 8

10.1. Reference information 9
10.1. Reference Data 9
10.2. External connection example..... 9

11. Application notes .....エラー! ブックマークが定義されていません。

12. Overview of Functions and Description of Registers 11
12.1. Overview of Functions..... 11
12.2. Register table..... 12

13. Description of Functions 13
13.1. Description of registers..... 13
13.2. Fixed-cycle Timer Interrupt Function..... 19
13.3. Alarm Interrupt Function..... 23
13.4. /IRQ "L" Interrupt Output When Interrupt Function Operates..... 26
13.5. FOUT function [clock output function]..... 27
13.6. Read/Write of data..... 29

LOW BACKUP VOLTAGE
SERIAL-INTERFACE REAL TIME CLOCK MODULE

RX – 4571 SA

- Built-in 32.768-kHz crystal resonator (with controlled frequency precision).
- Interface type : 3-wire serial interface
- Interface voltage range : 1.6 V to 5.5 V
- Voltage when during hold (timer hold) : 1.0 V to 5.5 V / Ta = +25 °C
- Current consumption during backup : 320 nA (Typ.) / 3 V
- 32.768-kHz output function with output control : C-MOS output With Control Pin
- Real-time clock function
  Clock/calendar function, auto leap year correction function, alarm interrupt function, etc.

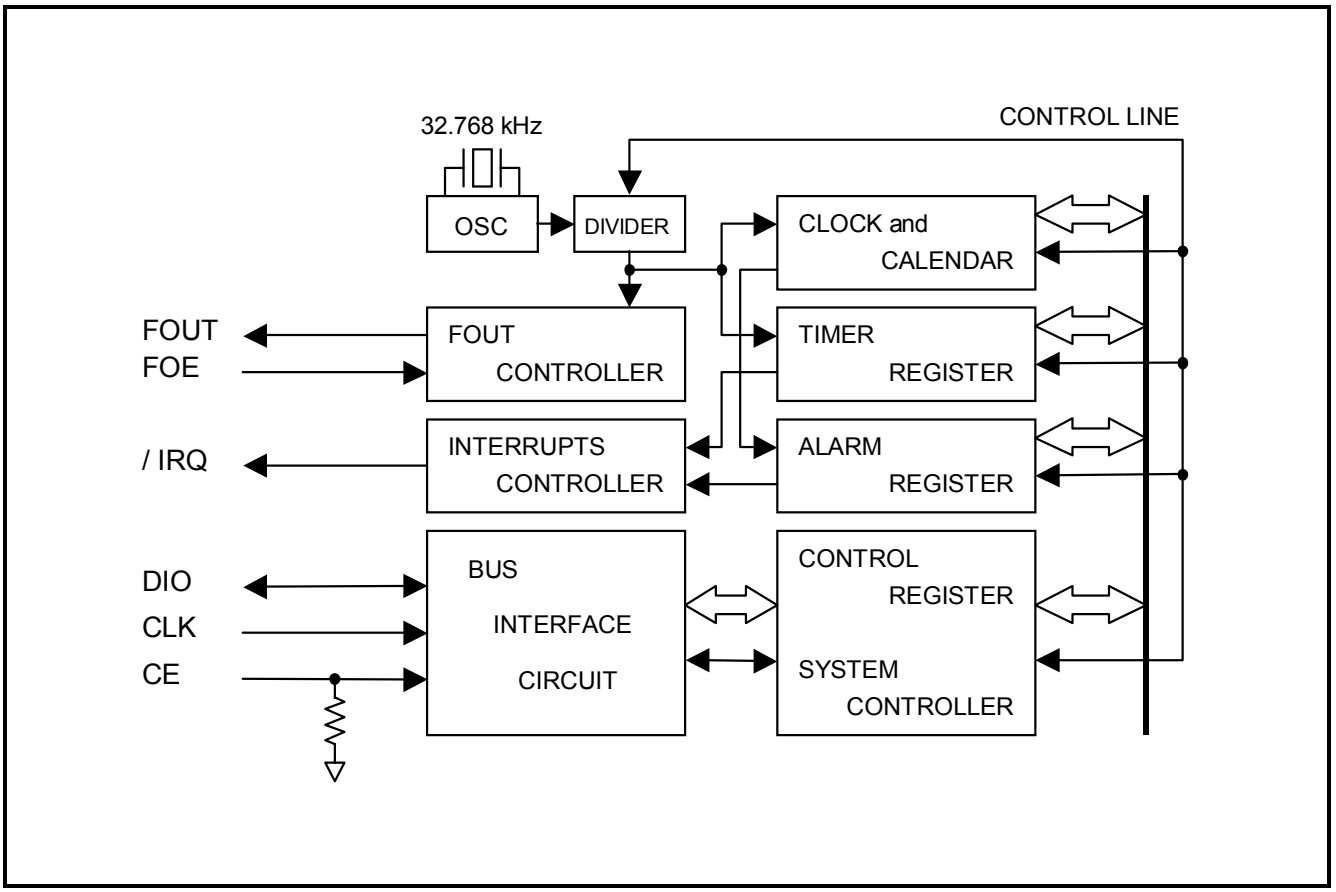
1. Overview

This module is a serial interface real time clock that has a built-in crystal unit.

The module offers many functions such as clock & calendar circuitry with automatic leap year adjustment (from seconds to year), alarm, and Timer interrupt. In addition, it can detect stopping of oscillation and time update.

All of these many functions are implemented in a thin, compact SOP package, which makes it suitable for various kinds of mobile telephones and other small electronic devices.

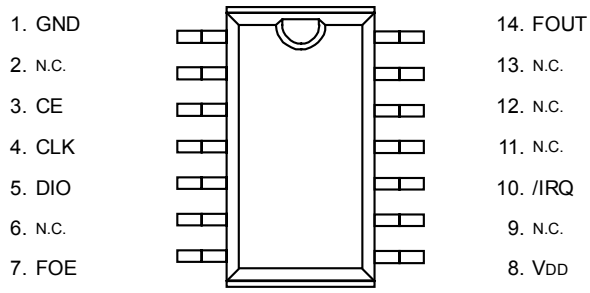
2. Block Diagram



3. Terminal description

3.1. Terminal connections

RX – 4571 SA



SOP – 14pin

3.2. Pin Functions

Signal name	I/O	Function
CE	Input	This is the chip enabled input pin. It has a built-in pull-down resistance. When both CE pin is at the "H" level, access to this RTC becomes possible.
CLK	Input	This is a shift clock input pin for serial data transmission. In the write mode, it takes in data from the DIO pin using the CLK signal rise edge. In the read mode, it outputs data from the DIO pin using the fall edge.
DIO	Bi-directional	This is a data input/output pin for serial data transmission. After the input rise of CE, by using the first 8-bit write data to set the write or read mode, this pin can be set as either input pin or output pin.
FOUT	Output	The FOUT pin is a clock output (C-MOS output) pin with control output. The FOE pin is an input pin used to control the output mode of the FOUT output pin. The FOE input pin can be used in combination with the FSEL1 bit and FSEL0 bit to select the output frequency from the FOUT output pin (32.768 kHz, 1024 Hz, or 1 Hz) or to stop output. When output is stopped, the CLKOUT output pin is at high impedance.
FOE	Input	∗ During the initial power-on (when power is applied from 0 V), if the FOE input pin is at high level (= H), the power-on reset function selects 32.768 kHz as the frequency.
/ IRQ	Output	This pin outputs alarm signals, fixed timer interrupt signals, and other interrupt signals at low level (= " L "). This pin is an open drain pin.
VDD	-	This pin connects to the plus side of the power.
GND	-	This pin connects to the minus side (ground) of the power.
N.C.	-	This pin is not connected internally. Be sure to connect using OPEN, or GND or VDD.

FOE pin input	FSEL1 bit	FSEL0 bit	FOUT pin output
X (Don't care)	0	0	32768 Hz Output (C-MOS output)
	0	1	1024 Hz Output (C-MOS output)
	1	0	1 Hz Output (C-MOS output)
" H "	1	1	32768 Hz Output (C-MOS output) ∗
" L "	1	1	OFF (high impedance)

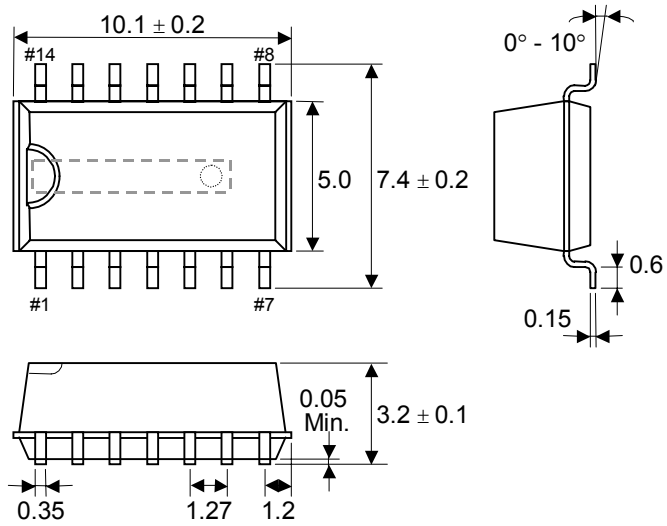
Note : Be sure to connect a bypass capacitor rated at least 0.1 µF between VDD and GND.

4. External Dimensions / Marking Layout

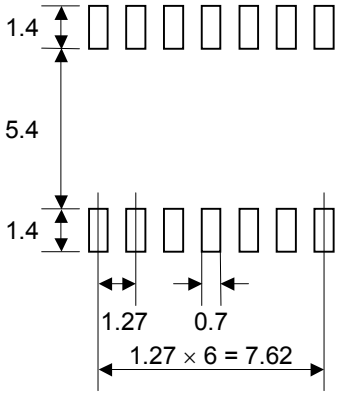
4.1. External Dimensions

RX – 4571 SA (SOP – 14 pin)

• External dimensions



• Recommended soldering pattern

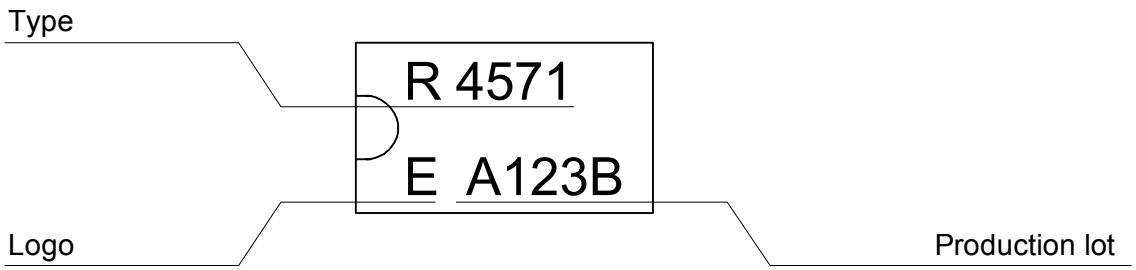


Unit : mm

∗ The cylinder of the crystal oscillator can be seen in this area (front), but it has no affect on the performance of the device.

4.2. Marking Layout

RX – 4571 SA (SOP – 14 pin)



∗ Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

5. Absolute Maximum Ratings

GND = 0 V

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	Between V_{DD} and GND	–0.3 to +6.5	V
Input voltage	VIN	CE, CLK, DIO, FOE pins	GND–0.3 to +6.5	V
Output voltage (1)	V_{OUT1}	DIO, FOUT pins	GND–0.3 to V_{DD}+0.3	V
Output voltage (2)	V_{OUT2}	/IRQ pin	GND–0.3 to +6.5	V
Storage temperature	T_{STG}	When stored separately, without packaging	–55 to +125	°C

6. Recommended Operating Conditions

GND = 0 V V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}	–	1.6	3.0	5.5	V
Clock supply voltage	V_{CLK}	Ta = +25 °C	1.0	3.0	5.5	V
		Ta = –40 °C to +85 °C	1.1.	3.0	5.5	V
Operating temperature	T_{OPR}	No condensation	–40	+25	+85	°C

7. Frequency Characteristics

GND = 0 V

Item	Symbol	Condition	Rating			Unit
Output frequency	fo		32.768 (Typ.)			kHz
Frequency/voltage characteristics	$\Delta f / f$	Ta = +25 °C V_{DD} = 3.0 V	5 ± 23 (*1)			$\times 10^{-6}$
Frequency/voltage characteristics	f / V	Ta = +25 °C V_{DD} = 2.0 V ~ 5.0 V	–2		+2	$\times 10^{-6}$ / V
Frequency/temperature characteristics	Top	Ta = –20 °C to +70 °C, V_{DD} = 3.0 V ; +25 °C reference	–120		+10	$\times 10^{-6}$
Oscillation start time	tSTA	Ta = +25 °C, V_{DD} = 1.6 V		0.5	1.0	s
		Ta = – 40 °C to +85 °C V_{DD} = 1.6 V			3.0	s
Aging	fa	Ta = +25 °C, V_{DD} = 3.0 V ; first year	–5		+5	$\times 10^{-6}$ / year

*1) This difference is 1 minute by 1 month. (excluding offset)

8. Electrical Characteristics

8.1. DC characteristics

8.1.1. DC characteristics (1)

* Unless otherwise specified, GND = 0 V , V_{DD} = 1.6 V to 5.5 V , Ta = –40 °C to +85 °C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption (1)	I_{DD1}	CE = OPEN (or GND) /IRQ = OFF FOUT ; output OFF (Hi - z)	V_{DD} = 5 V		0.40	1.00	μA
Current consumption (2)	I_{DD2}		V_{DD} = 3 V		0.32	0.95	
Current consumption (3)	I_{DD3}	CE = OPEN (or GND) /IRQ = OFF, FOE = V_{DD} FOUT; 32.768 kHz output ON , CL = 0 pF	V_{DD} = 5 V		3.5	6.0	μA
Current consumption (4)	I_{DD4}		V_{DD} = 3 V		2.0	3.5	
Current consumption (5)	I_{DD5}	CE = OPEN (or GND) /IRQ = OFF, FOE = V_{DD} FOUT; 32.768 kHz output ON , CL = 30 pF	V_{DD} = 5 V		8.0	14.0	μA
Current consumption (6)	I_{DD6}		V_{DD} = 3 V		5.0	8.5	
Input leakage current	I_{LK}	CE pin ; V_{IN} = GND CLK, FOE pins ; V_{IN} = V_{DD} or GND		–0.5		0.5	μA
Output leakage current	I_{OZ}	DATA, / IRQ, FOUT pins, V_{OUT} = V_{DD} or GND		–0.5		0.5	μA

8.1.2. DC characteristics (2)

* Unless otherwise specified, GND = 0 V , V_{DD} = 1.6 V to 5.5 V , Ta = –40 °C to +85 °C

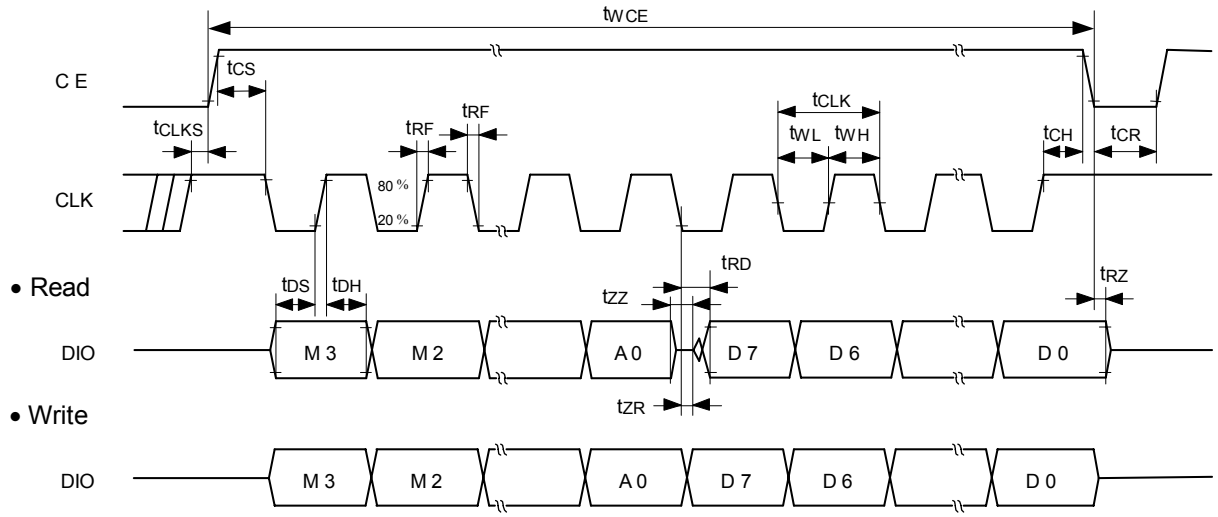
Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH1}	CE, CLK, FOE pins	V_{DD} = 1.6 V to 5.5 V	0.70 × V_{DD}		6.5	V
	V_{IH2}		V_{DD} = 5 V ± 10 %	0.75 × V_{DD}		6.5	V
	V_{IH3}	DIO pin	V_{DD} = 1.6 V to 5.5 V	0.70 × V_{DD}		V_{DD} + 0.3	V
	V_{IH4}		V_{DD} = 5 V ± 10 %	0.75 × V_{DD}		V_{DD} + 0.3	V
Low-level input voltage	V_{IL1}	CE, CLK, DATA, FOE pins		GND – 0.3		0.3 × V_{DD}	V
	V_{IL2}	CE, CLK, DATA, FOE pins (5 V ± 10 %)		GND – 0.3		0.25 × V_{DD}	V
High-level output voltage	V_{OH1}	DIO, FOUT pins	V_{DD} = 5 V, I_{OH} = –1 mA	4.5		5.0	V
	V_{OH2}		V_{DD} = 3 V, I_{OH} = –1 mA	2.2		3.0	
	V_{OH3}		V_{DD} = 3 V, I_{OH} = –100 μA	2.9		3.0	
Low-level output voltage	V_{OL1}	DIO, FOUT pins	V_{DD} = 5 V, I_{OL} = 1 mA	GND		GND+0.5	V
	V_{OL2}		V_{DD} = 3 V, I_{OL} = 1 mA	GND		GND+0.8	
	V_{OL3}		V_{DD} = 3 V, I_{OL} = 100 μA	GND		GND+0.1	
	V_{OL4}	/ IRQ pin	V_{DD} = 5 V, I_{OL} = 1 mA	GND		GND+0.25	V
	V_{OL5}		V_{DD} = 3 V, I_{OL} = 1 mA	GND		GND+0.4	
Input resistance (1)	R_{DWN1}	CE pin V_{IN} = V_{DD}	V_{DD} = 5 V	75	150	300	kΩ
Input resistance (2)	R_{DWN2}		V_{DD} = 3 V	150	300	600	kΩ

8.2. AC characteristics

* Unless otherwise specified, GND = 0 V , Ta = –40 °C to +85 °C

Item	Symbol	Condition	VDD = 3 V ± 10 %		VDD = 5 V ± 10 %		単位
			Min.	Max.	Min.	Max.	
CLK clock cycle	t_{CLK}		500		350		ns
CLK H pulse width	t_{WH}		250		175		ns
CLK L pulse width	t_{WL}		250		175		ns
CLK rise and fall time	t_{RF}			100		50	ns
CLK setup time	t_{CLKS}		50		25		ns
CE setup time	t_{CS}		200		150		ns
CE hold time	t_{CH}		200		100		ns
CE recovery time	t_{CR}		300		200		ns
CE enable time	t_{WCE}			0.95		0.95	s
Write data setup time	t_{DS}		100		50		ns
Write data hold time	t_{DH}		100		50		ns
Read data delay time	t_{RD}	C_L=50 pF		200		150	ns
DO output switching time	t_{ZR}			50		25	ns
DO output disable time	t_{RZ}	C_L=50 pF R_L=10 kΩ		200		100	ns
DI/DO conflict avoiding time	t_{ZZ}		0		0		ns

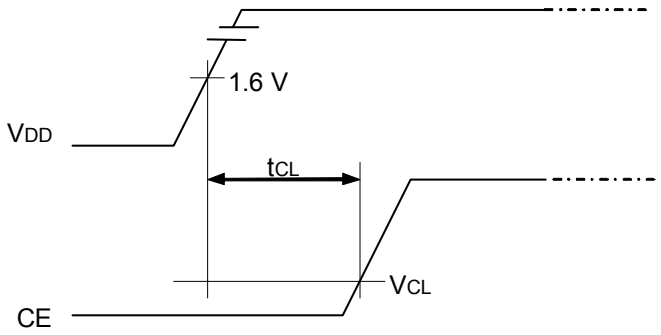
Timing chart



9. Matters that demand special attention on use

9.1. VDD and CE timing

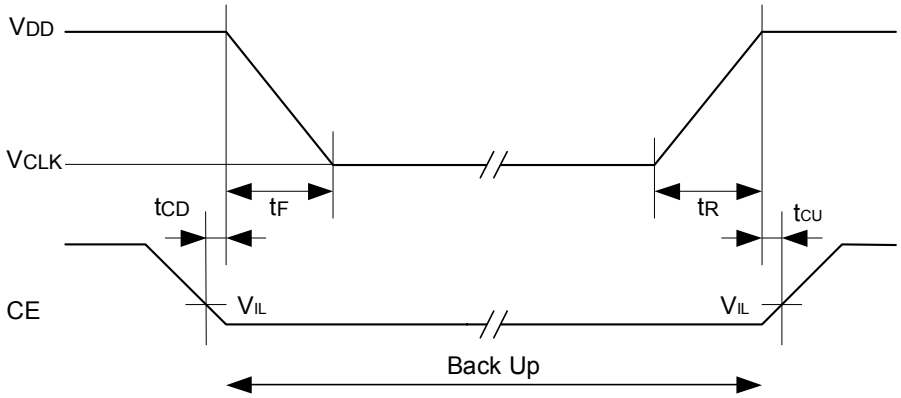
* When the power is turned to ON, use with CE = " L " (VCL[V] in the diagram) as illustrated in the following timing chart.



Item	Symbol	Remark	Specification	Unit
CE voltage when power is turned to ON	VCL	CE impressed voltage until VDD = 1.6 V	0.3 (Max.)	V
CE=VCL[V] time when power is turned to ON	tCL	Time to maintain CE=VCL[V] until VDD = 1.6 V	30 (Min.)	ms

9.2. Migrating to backup, and returning

* When migrating to backup, before switching the power source, make sure CE is definitely LOW and RTC is not selected



Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CE time before power drop	tCD	–	0			µs
Power drop time	tF	–	2			µs / V
Power rise time	tR	–	5			µs / V
CE time after power rise	tCU	–	0			µs

9.3. Restrictions on Access Operations During Power-on Initialization and Recovery from Backup

- Many of this product's operations are linked to the internal quartz oscillator's clock signal, so normal operation is not possible if there is no internal oscillation (= oscillation is stopped).

  Therefore, we recommend that the initial setting to be set during power-on initialization or backup and restore operations (i.e., when the power supply voltage is recovered after oscillation has stopped due to a voltage drop, etc.) should be "first start internal oscillation, then wait for the oscillation stabilization time (see tSTA standard) to elapse".

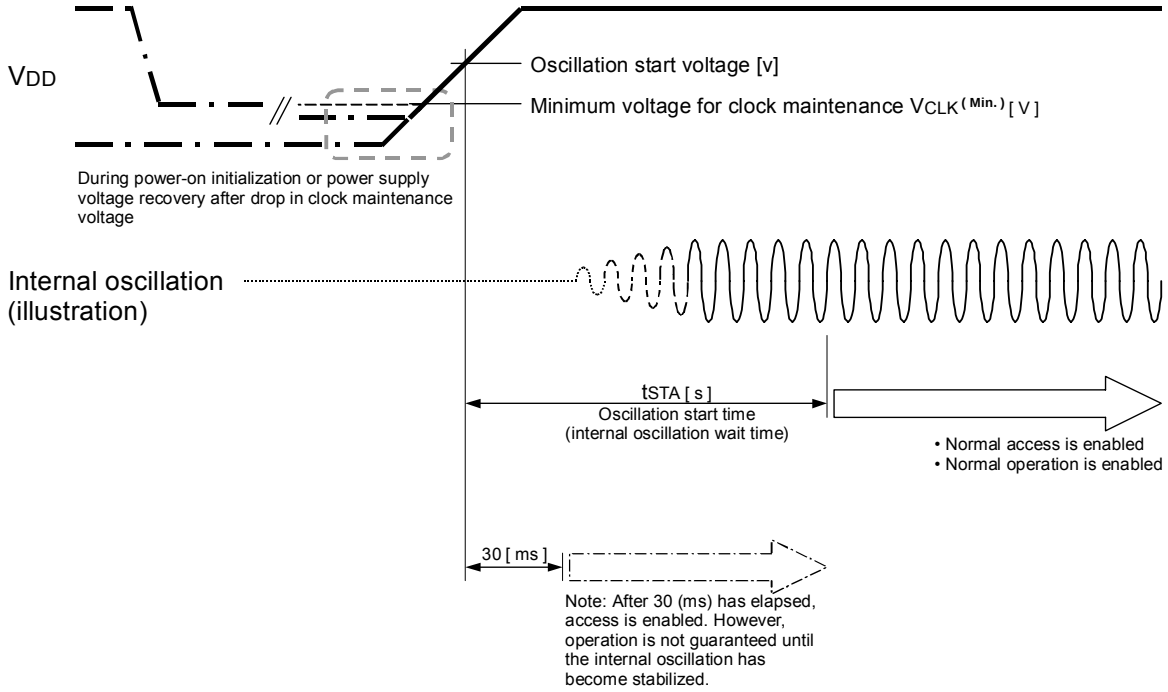
- Note the following caution points concerning access operations during power-on initialization or when restoring the power supply voltage from backup mode (hereafter referred to as "switching to the operating voltage").

  1) Before switching to the operating voltage, read the VLF-bit (which indicates the RTC error status).

  2) Initialization is required when the value read from the VLF-bit is "VLF = 1 (error status)".
  Before initializing in response to this VLF = "1" result, we recommend first waiting for the internal oscillation stabilization time (see the tSTA standard) to elapse.

Initialization is required when the status after reading a VLF-bit value of "1" is either of the following. (Status 1) During power-on initialization (Status 2) When the clock setting is invalid, such as due to a voltage drop during backup

∗ Access timing during power-on initialization and when recovering the power supply voltage after a drop in the voltage used to maintain the clock



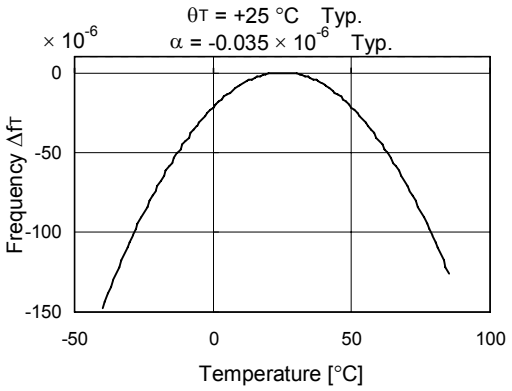
  3) When the read VLF-bit value is "VLF = 0 (normal status)", access is enabled without waiting for stabilization of oscillation.

Normal operation is enabled under the following two statuses when "0" is read as the VLF-bit value. (Status 1) When correct operation is enabled (except for settings errors while in use) (Status 2) When data is retained normally while switching to the operating voltage from backup mode

10.1. Reference information

10.1. Reference Data

(1) Example of frequency and temperature characteristics



[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

   $\Delta f_T = \alpha (\theta_T - \theta_X)^2$

   - Δf_T : Frequency deviation in any temperature
   - α [1 / °C^2] : Coefficient of secondary temperature (-0.035 ± 0.005) $\times 10^{-6}$ / °C^2
   - θ_T [°C] : Ultimate temperature ($+25 \pm 5$ °C)
   - θ_X [°C] : Any temperature

2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

   $\Delta f/f = \Delta f/fo + \Delta f_T + \Delta f_V$

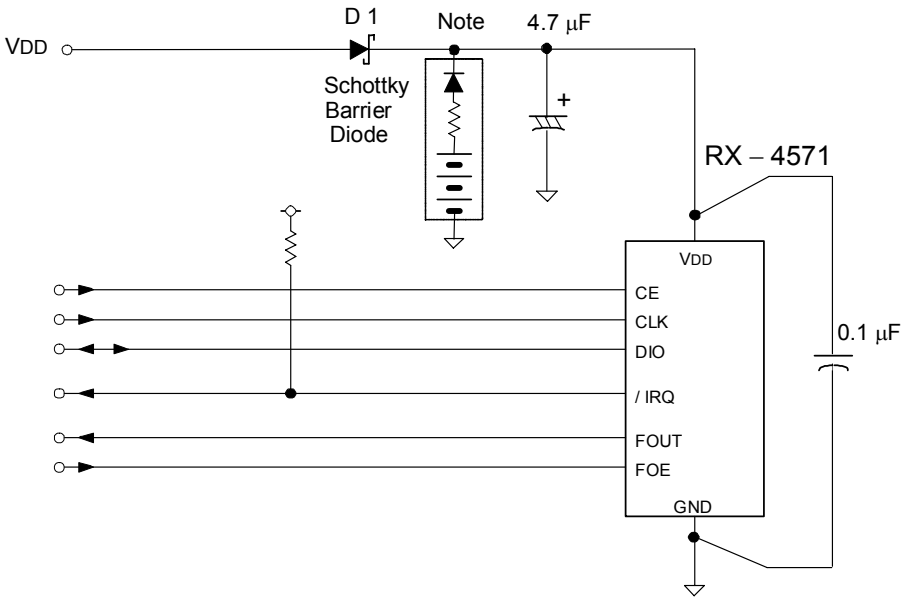
   - $\Delta f/f$: Clock accuracy (stable frequency) in any temperature and voltage.
   - $\Delta f/fo$: Frequency precision
   - Δf_T : Frequency deviation in any temperature.
   - Δf_V : Frequency deviation in any voltage.

3. How to find the date difference

   Date Difference = $\Delta f/f \times$ 86400(Sec)

   ∗ For example: $\Delta f/f = 11.574 \times 10^{-6}$ is an error of approximately 1 second/day.

10.2. External connection example



Note :

It uses the secondary battery or a lithium battery. When using the seconding battery, the diode is not required. When using the lithium battery, the diode is required. For detailed value on the resistance, please consult a battery maker.

11. Application notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 μF as close as possible to the power supply pins (between VDD and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.

* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to VDD or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

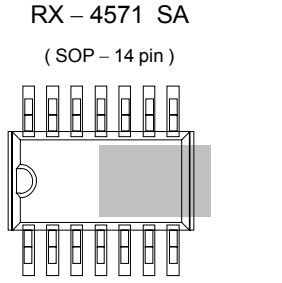
(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

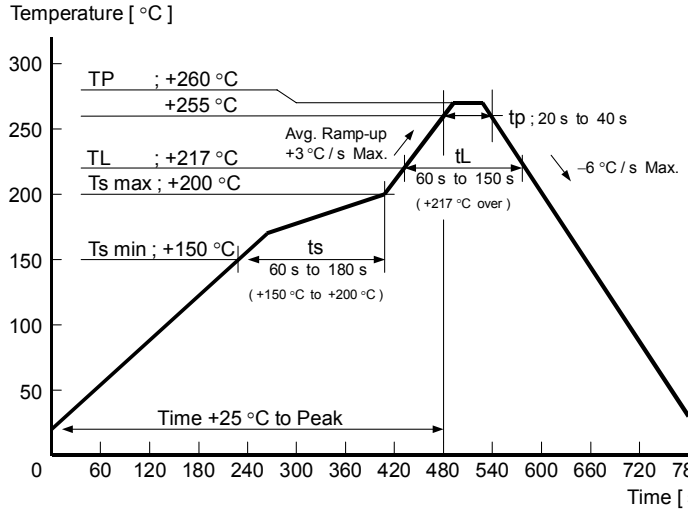
Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1 : Example GND Pattern



* The shaded part ( ) indicates where a GND pattern should be set without getting too close to a signal line

Fig. 2 : Reference profile for our evaluation of Soldering heat resistance.



12. Overview of Functions and Description of Registers

12.1. Overview of Functions

1) Clock functions

This function is used to set and read out month, day, hour, date, minute, second, and year (last two digits) data.
Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2099.
∗ For details, see "13.1. Description of Registers".

2) Fixed-cycle interrupt generation function

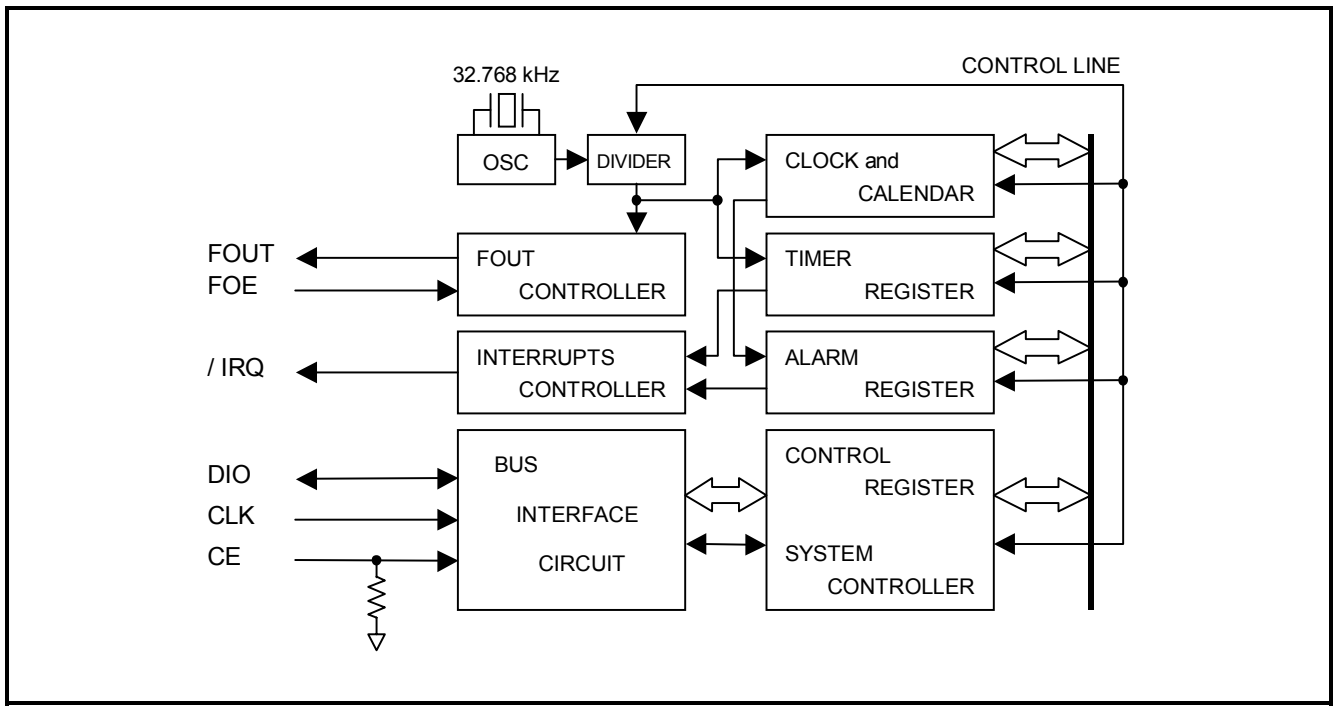
The fixed-cycle timer interrupt generation function generates an interrupt event periodically at any fixed cycle set between 244.14 μs and 4096 minutes.
When an interrupt event is generated, the /TIRQ pin goes to low level ("L") and "1" is set to the TF bit to report that an event has occurred..
This function can be selected from two types of operations (single-shot operations and repeated operations).
∗ For details, see "13.2. Fixed-cycle Interrupt Function". .

3) Alarm interrupt function

The alarm interrupt generation function generates interrupt events for alarm settings such as date, day, hour, and minute settings.
When an interrupt event occurs, the AF bit value is set to "1" and the /IRQ pin goes to low level to indicate that an event has occurred.
∗ For details, see "13.3. Alarm Interrupt Function".

4) Clock output function

A clock with the same frequency (32.768 kHz) as the built-in crystal resonator can be output from the FOUT pin (CMOS output).



12.2. Register table

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	note
0	SEC	○	40	20	10	8	4	2	1	∗3
1	MIN	○	40	20	10	8	4	2	1	∗3
2	HOUR	○	○	20	10	8	4	2	1	∗3
3	WEEK	○	6	5	4	3	2	1	0	∗3
4	DAY	○	○	20	10	8	4	2	1	∗3
5	MONTH	○	○	○	10	8	4	2	1	∗3
6	YEAR	80	40	20	10	8	4	2	1	
7	RAM	•	•	•	•	•	•	•	•	∗4
8	MIN Alarm	AE	40	20	10	8	4	2	1	
9	HOUR Alarm	AE	•	20	10	8	4	2	1	∗4
A	DAY Alarm	AE	6	5	4	3	2	1	0	∗4
	DAY Alarm		•	20	10	8	4	2	1	
B	Timer Counter 0	128	64	32	16	8	4	2	1	–
C	Timer Counter 1	•	•	•	•	2048	1024	512	256	∗4
D	Extension Register	***TEST1***	WADA	○	TE	FSEL1	FSEL0	TSEL1	TSEL0	∗1, ∗3
E	Flag Register	***TEST2***	○	○	TF	AF	○	VLF	***RSV***	∗1, ∗3, ∗5
F	Control Register	***TEST3***	○	○	TIE	AIE	○	STOP	○	∗3

Note During the initial power-on (from 0 V) and if the value of the VLF bit is "1" when the VLF bit is read, be sure to initialize all registers before using them.
When doing this, be careful to avoid setting incorrect data as the date or time, as timed operations cannot be guaranteed if incorrect date or time data has been set.

∗1. During the initial power-on (from 0 V), the power-on reset function sets "1" to the VLF bit.
∗ Since the value of other registers is undefined at this time, be sure to reset all registers before using them.

∗2. The ***TEST1***, ***TEST2***, ***TEST3*** bits are Epson Toyocom test bits.
∗ Be sure to write "0" by initializing before using the clock module. Afterward, be sure to set "0" when writing.
∗ The four ***TEST**** bits are undefined when read. Those bits should be masked after being read.

∗3. The ' ○ ' mark indicates a write-prohibited bit, which returns a "0" when read.

∗4. The ' • ' mark indicates a read/write-accessible RAM bit for any data.

∗5. The ***RSV*** bit are Epson Toyocom test bits.
∗ Be sure to write "0" by initializing before using the clock module. Afterward, be sure to set "0" when writing.
∗ The four ***RSV*** bits are undefined when read. Those bits should be masked after being read.

13. Description of Functions

13.1. Description of registers

13.1.1. Clock counter (Reg - 0[h] ~ 2[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	SEC	○	40	20	10	8	4	2	1
1	MIN	○	40	20	10	8	4	2	1
2	HOUR	○	○	20	10	8	4	2	1

- The clock counter counts seconds, minutes, and hours.
- The data format is BCD format. For example, when the "seconds" register value is "0101 1001" it indicates 59 seconds.

∗ Note with caution that writing non-existent time data may interfere with normal operation of the clock counter.

1) Second counter (Reg - 0[h])

This counter counts seconds.
Count values are updated as: 00 seconds, 01 second, 02 to 59 seconds, 00 seconds, 01 second, etc. in that order. When writing is performed to this registor, Internal-count-down-chain less than one second is cleared to 0.

2) Minute counter (Reg - 1[h])

This counter counts minutes.
Count values are updated as: 00 minutes, 01 minute, 02 to 59 minutes, 00 minutes, 01 minute, etc. in that order.

3) Hour counter (Reg - 2[h])

This counter counts hours.
Count values are updated as: 00 hours, 01 hour, 02 to 23 hours, 00 hours, 01 hour, etc. in that order.

13.1.2. . Day counter (Reg - 3[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
3	WEEK	○	6	5	4	3	2	1	0

- The day (of the week) is indicated by 7 bits, bit 0 to bit 6.
  The day data values are counted as: Day 01h → Day 02h → Day 04h → Day 08h → Day 10h → Day 20h → Day 40h → Day 01h → Day 02h, etc.
- The correspondence between days and count values is shown below.

[WEEK]	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Day	Data [h]
Write / Read	0	0	0	0	0	0	0	**1**	Sunday	01 h
	0	0	0	0	0	0	**1**	0	Monday	02 h
	0	0	0	0	0	**1**	0	0	Tuesday	04 h
	0	0	0	0	**1**	0	0	0	Wednesday	08 h
	0	0	0	**1**	0	0	0	0	Thursday	10 h
	0	0	**1**	0	0	0	0	0	Friday	20 h
	0	**1**	0	0	0	0	0	0	Saturday	40 h
Write prohibit	∗ Do not set "1" to more than one day at the same time. Also, note with caution that any setting other than the seven shown above should not be made as it may interfere with normal operation.								–	–

13.1.3. Calendar counter (Reg - 04[h] ~ 06[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
4	DAY	○	○	20	10	8	4	2	1
5	MONTH	○	○	○	10	8	4	2	1
6	YEAR	80	40	20	10	8	4	2	1

- The auto calendar function updates all dates, months, and years from January 1, 2001 to December 31, 2099.
- The data format is BCD format. For example, a date register value of "0011 0001" indicates the 31st.

∗ Note with caution that writing non-existent date data may interfere with normal operation of the calendar counter.

1) [DAY] register (Reg – 04 [h])

- This is the date counter.
  Updating of this counter varies depending on the month.

∗ A leap year is set whenever the year value is a multiple of four (such as 04, 08, 12, 88, 92, or 96). In February of a leap year, the counter counts dates from "01," "02," "03," to "28," "29," "01," etc.

DAY	Month	Date update pattern
Write/Read	1, 3, 5, 7, 8, 10, or 12	01, 02, 03 ~ 30, 31, 01 ~
	4, 6, 9, or 11	01, 02, 03 ~ 30, 01, 02 ~
	February in normal year	01, 02, 03 ~ 28, 01, 02 ~
	February in leap year	01, 02, 03 ~ 28, 29, 01 ~

2) [MONTH] register (Reg – 05 [h])

- This is the month counter.
  It is updated in annual cycles of regularly ordered months (January, February, March, etc.).

3) [YEAR] register (Reg – 06 [h])

- This is the year counter.
  It is updated in 100-year cycles of regularly ordered years (00, 01, 02 to 99, etc.).
- Any year that is a multiple of four (04, 08, 12, 88, 92, 96, etc.) is handled as a leap year.

13.1.4. RAM register (Reg - 7[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
7	RAM	•	•	•	•	•	•	•	•

- This RAM register is read/write accessible for any data in the range from 00 h to FF h.

13.1.5. Alarm registers (Reg - 8[h] ~ A[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
8	MIN Alarm	AE	40	20	10	8	4	2	1
9	HOUR Alarm	AE	•	20	10	8	4	2	1
A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1

- The alarm interrupt function is used, along with the AE, AF, and WADA bits, to set alarms for specified date, day, hour, and minute values.
- When the settings in the above alarm registers and the WADA bit match the current time, the /IRQ pin goes to low level and "1" is set to the AF bit to report that and alarm interrupt event has occurred.

* For details, see "13.3. Alarm Interrupt Function".

13.1.6. Timer setting and Timer counter register (Reg - C[h] ~ D[h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
B	Timer Setup	128	64	32	16	8	4	2	1
C	Timer Counter	•	•	•	•	2048	1024	512	256

- This register is used to set the default (preset) value for the counter. Any count value from 1 (001 h) to 4095 (FFFh) can be set
- To use the fixed-cycle timer interrupt function, the TE, TF, TIE, TSEL0, and TSEL1 bits are set and used.
- When this down counter's count value changes from 001h to 000h, when TF bit = "1", or when the /IRQ pin is at low level ("L"), it indicates that a fixed-cycle timer interrupt event has occurred.

* When the fixed-cycle timer interrupt function is not being used, the fixed-cycle timer control register (Reg – B to C) can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

* For details, see "13.2. Fixed-cycle Timer Interrupt Function ".

13.1.7. Extension Register (Reg – D [h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
D	Extension Register	***TEST1***	WADA	○	TE	FSEL1	FSEL0	TSEL1	TSEL0

- This register is used to specify the target for the alarm function or time update interrupt function and to select or set operations such as fixed-cycle timer operations.

1) ***TEST1*** bit

This bits is the manufacturer's test bit.
Always leave this bit value as "0" except when testing.
Be careful to avoid writing to this bit when writing "1" to other bits in this register.

∗ The three ***TEST*** bits are undefined when read. Those bits should be masked after being read.

2) WADA bit (Week Alarm / Day Alarm Select)

This bit is used to specify either WEEK or DAY as the target of the alarm interrupt function.
Writing a "1" to this bit specifies DAY as the comparison object for the alarm interrupt function.
Writing a "0" to this bit specifies WEEK as the comparison object for the alarm interrupt function.

3) TE bit (Timer Enable)

This bit is used to control operation of the fixed-cycle timer interrupt function.
When "1" is written to this bit, the fixed-cycle timer interrupt function starts operating.
When "0" is written to this bit, the fixed-cycle timer interrupt function stops operating.
∗ For details, see "13.2. Fixed-cycle Timer Interrupt Function ".

4) FSEL1, FSEL0 bits (Frequency Select 1, 0)

A combination of the FSEL1 and FSEL0 bits is used to select the frequency to be output.
The choice is possible by a combination of FSEL-bits and FOE-pin, select the frequency of clock output or inhibit the clock output.

5) TSEL1,TSEL0 bits (Timer Select 1, 0)

These bits specify the fixed-cycle timer interrupt function's countdown period (source clock).
Four different periods can be selected via combinations of these two bit values.
∗ For details, see "13.2. Fixed-cycle Timer Interrupt Function ".

13.1.8. Flag Register (Reg – 0E [h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
E	Flag Register	***TEST2***	○	○	TF	AF	○	VLF	***RSV***

- This is a flag register that indicates circumstantial results, such as the state of power supply, the generated state of various interrupt events, the reliability of internal data, and the like.

1) ***TEST2***, ***RSV*** bit

Those bits are the manufacturer's test bit.
Always leave this bit value as "0" except when testing.
Be careful to avoid writing to this bit when writing "1" to other bits in this register.

∗ The three ***TEST*** bits are undefined when read. Those bits should be masked after being read.

2) TF bit (Timer Flag)

This flag bit holds the result of the detection of a fixed-cycle timer interrupt event.
If a fixed-cycle timer interrupt event is generated, this bit shifts from "0" to "1."

∗ For details, see "13.2. Fixed-cycle Timer Interrupt Function".

3) AF bit (Alarm Flag)

This is a flag bit that retains the result when an alarm interrupt event has been detected.
When an alarm interrupt event occurs, this bit's value changes from "0" to "1".

∗ For details, see "13.4. Alarm Interrupt Function".

4) VLF bit (Voltage Low Flag)

This flag bit indicates the retained status of clock operations or internal data. Its value changes from "0" to "1" when data loss occurs, such as due to a supply voltage drop. Once this flag bit's value is "1", its value is retained until a "0" is written to it.
During the initial power-on (from 0 V) and if the value of the VLF bit is "1" when the VLF bit is read, be sure to initialize all registers before using them.

VLF	Data	Description
Write	0	The VLF is cleared to 0, and waiting for next low voltage detection.
	1	It is impossible to write in 1 to VLF.
Read	0	RTC register data are valid.
	1	RTC register data are invalid. Should be initialized of all register data. VLF is maintained till it is cleared by zero.

13.1.9. Control Register (Reg – 0F [h])

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
F	Control Register	***TEST3***	○	○	TIE	AIE	○	STOP	○

- This is a flag register that indicates circumstantial results, such as the state of power supply, the generated state of various interrupt events, the reliability of internal data, and the like.

1) ***TEST3*** bit

This bits is the manufacturer's test bit.
Always leave this bit value as "0" except when testing.
Be careful to avoid writing to this bit when writing "1" to other bits in this register.

∗ The three ***TEST*** bits are undefined when read. Those bits should be masked after being read.

2) TIE bit (Timer Interrupt Enable)

This bit sets the operation of the /IRQ interrupt signal when a fixed-cycle interrupt event has occurred (the TF bit value changes from "0" to "1").
When a "1" is written to this bit, occurrence of an interrupt event causes a low-level interrupt signal to be output from /IRQ pin.
Writing "0" to this bit prohibits low-level output from the /IRQ pin.

∗ For details, see "13.2. Fixed-cycle Timer Interrupt Function ".

3) AIE bit (Alarm Interrupt Enable)

This bit sets the operation of the /IRQ interrupt signal when an alarm interrupt event has occurred (the AF bit value changes from "0" to "1").
When a "1" is written to this bit, occurrence of an interrupt event causes a low-level interrupt signal to be output from /IRQ pin.
Writing "0" to this bit prohibits low-level output from the /IRQ pin.

∗ For details, see "13.4. Alarm Interrupt Function".

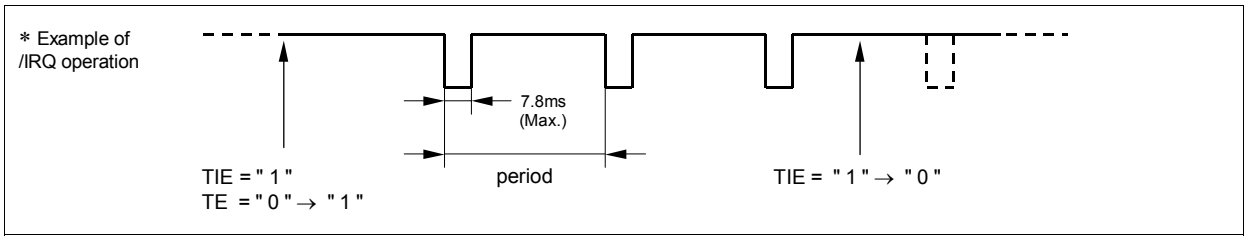
4) STOP bit

This bit is used to stop functions related to the RTC's internal counter operations.
Writing a "1" to this bit stops the counter operations.
Writing a "0" to this bit cancels stop status (restarts counter operations).

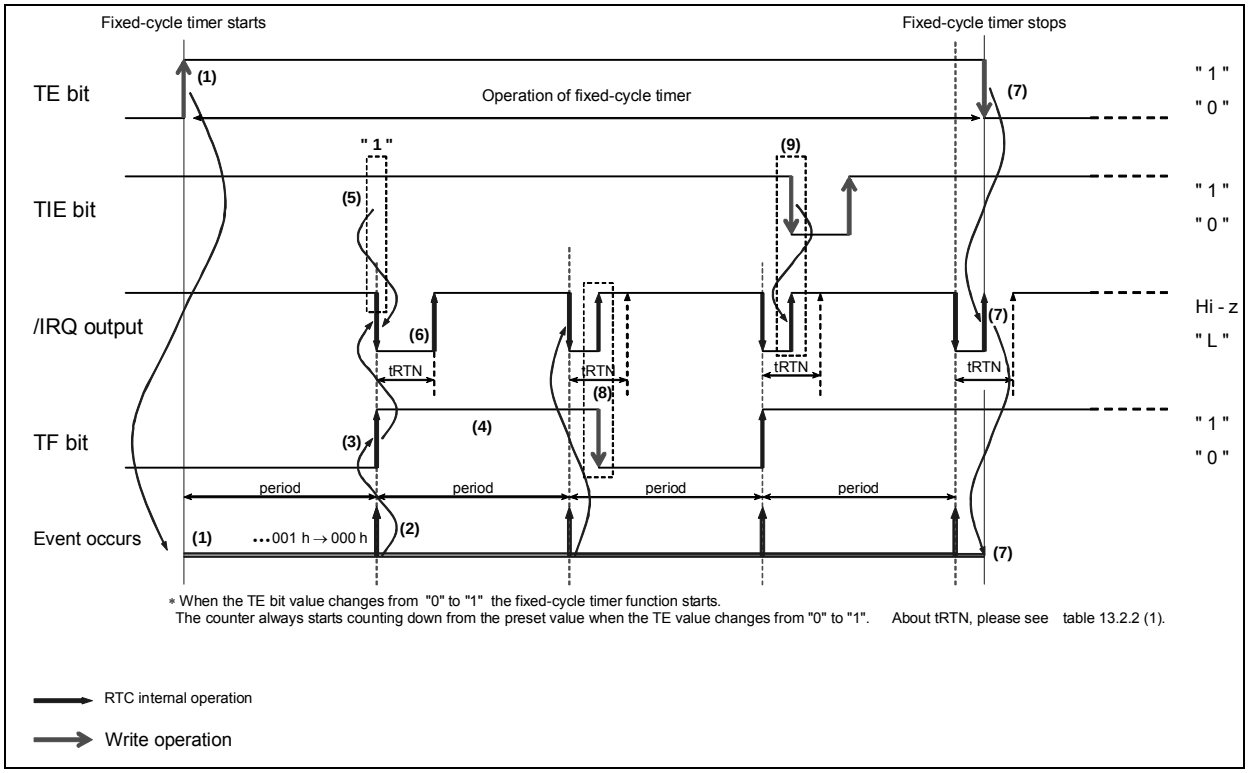
∗ For optimum performance, do not use this bit for functions other than the clock and calendar functions.

13.2. Fixed-cycle Timer Interrupt Function

The fixed-cycle timer interrupt generation function generates an interrupt event periodically at any fixed cycle set between 244.14 μs and 4095 minutes.
When an interrupt event is generated, the /IRQ pin goes to low level and "1" is set to the TF bit to report that an event has occurred. (However, when a fixed-cycle timer interrupt event has been generated low-level output from the /IRQ pin occurs only when the value of the control register's TIE bit is "1". Up to 7.8 ms after the interrupt occurs, the /IRQ status is automatically cleared (/IRQ status changes from low-level to Hi-Z).



13.2.1. Diagram of fixed-cycle timer interrupt function



(1) When a "1" is written to the TE bit, the fixed-cycle timer countdown starts from the preset value.

(2) A fixed-cycle timer interrupt event starts a countdown based on the countdown period (source clock). When the count value changes from 001h to 000h, an interrupt event occurs.
∗ After the interrupt event that occurs when the count value changes from 001h to 000h, the counter automatically reloads the preset value and again starts to count down. (Repeated operation)

(3) When a fixed-cycle timer interrupt event occurs, "1" is set to the TF bit.

(4) When the TF bit = "1" its value is retained until it is cleared to zero.

(5) If the TIE bit = "1" when a fixed-cycle timer interrupt occurs, /IRQ pin output goes low.
∗ If the TIE bit = "0" when a fixed-cycle timer interrupt occurs, /IRQ pin output remains Hi-Z.

(6) Output from the /IRQ pin remains low during the tRTN period following each event, after which it is automatically cleared to Hi-Z status.
∗ /IRQ is again set low when the next interrupt event occurs.

(7) When a "0" is written to the TE bit, the fixed-cycle timer function is stopped and the /IRQ pin is set to Hi-Z status.

(8) When /IRQ = low, the /IRQ pin status changes from low to Hi-Z as soon as the TF bit value changes from "1" to "0".

(9) When /IRQ = low, the /IRQ pin status changes from low to Hi-Z as soon as the TIE bit value changes from "1" to "0".

13.2.2. Related registers for function of fixed-cycle timer interrupt function

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
B	Timer Counter 0	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
C	Timer Counter 1	•	•	•	•	**2048**	**1024**	**512**	**256**
D	Extension Register	***TEST1***	WADA	○	**TE**	FSEL1	FSEL0	TSEL1	TSEL0
E	Flag Register	***TEST2***	○	○	**TF**	AF	○	VLF	***RSV***
F	Control Register	***TEST3***	○	○	**TIE**	AIE	○	STOP	○

∗ Before entering operation settings, we recommend first clearing the TE bit to "0" and then clearing the TF and TIE bits to "0" in that order, so that all control-related bits are zero-cleared (= set to operation stop mode) to prevent hardware interrupts from occurring inadvertently while entering settings.
∗ When the fixed-cycle timer interrupt function is not being used, the fixed-cycle timer control register (Reg – 0B to 0C) can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

1) TSEL1, TESL0 bits (Timer Select 1, 0)

The combination of these two bits is used to set the countdown period (source clock) for the fixed-cycle timer interrupt function (four settings can be made).

TSEL1, 0	TSEL1 (bit 1)	TSEL0 (bit 0)	Source clock	Auto reset time tRTN	Effects of STOP and RESET bits
W / R	0	0	4096 Hz /Once per 244.14 μs	122 μs	–
	0	1	64 Hz /Once per 15.625 ms	7.813 ms	∗ Does not operate when the STOP bit or RESET bit value is "1".
	1	0	1 Hz /Once per second	7.813 ms	
	1	1	1/60 Hz /Once per minute	7.813 ms	

∗1) The /IRQ pin's auto reset time (tRTN) varies as shown above according to the source clock setting.
∗2) An interrupt that occurs when the source clock is in 1 Hz mode is not linked to the internal clock.
∗3) An interrupt that occurs when the source clock is in 1/60 Hz mode is linked to the internal clock's "minute" update operation.

2) Down counter for fixed-cycle timer (Timer Counter 1, 0)

This register is used to set the default (preset) value for the counter. Any count value from 1 (001 h) to 4095 (FFFh) can be set. The counter counts down based on the source clock's period, and when the count value changes from 001h to 000h, the TF bit value becomes "1".
The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value.
Be sure to write "0" to the TE bit before writing the preset value. If a value is written while TE = "1" the first subsequent event will not be generated correctly.

Address 0C Timer Counter 1								Address 0B Timer Counter 0							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
•	•	•	•	2048	1024	512	256	128	64	32	16	8	4	2	1

∗ When TE=1, read out data of timer counter is default(Preset) value.
And when TE=0, read out data of timer counter is just counting value.
But , when access to timer counter data, counting value is not held.
Therefore, for example, perform twice read access to obtain right data, and a way to adopt the case that two data accorded is necessary.
You can use timer registers as RAM, when you do not use timer functions.
In this case, clear the TE and TIE, should stop the timer interrupt function.

3) TE bit (Timer Enable)

When TE bit is "0", the default (preset) can be checked by reading this register.

TE	Data	Description
Write / Read	0	Stops fixed-cycle timer interrupt function. * Clearing this bit to zero does not enable the /IRQ low output status to be cleared (to Hi-Z).
	1	Starts fixed-cycle timer interrupt function. * The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value.

4) TF bit (Timer Flag)

This is a flag bit that retains the result when a fixed-cycle timer interrupt event is detected.

If it was already cleared to zero, this value changes from "0" to "1" when an event occurs, and the new value is retained.

TF	Data	Description
Write	0	The TF bit is cleared to zero to prepare for the next status detection * Clearing this bit to zero does not enable the /IRQ low output status to be cleared (to Hi-Z).
	1	This bit is invalid after a "1" has been written to it.
Read	0	Fixed-cycle timer interrupt events are not detected.
	1	Fixed-cycle timer interrupt events are detected. (Result is retained until this bit is cleared to zero.)

5) TIE bit (Timer Interrupt Enable)

This bit is used to control output of interrupt signals from the /IRQ pin when a fixed-cycle timer interrupt event has occurred.

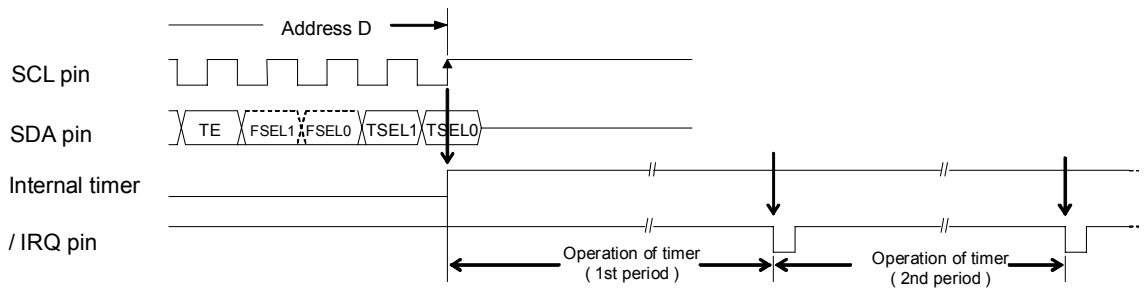
When a "1" is written to this bit, occurrence of an interrupt event causes a low-level interrupt signal to be output from /IRQ pin.

When a "0" is written to this bit, output from the /IRQ pin is prohibited (disabled).

TIE	Data	Description
Write / Read	0	1) When a fixed-cycle timer interrupt event occurs, an interrupt signal is not generated or is canceled (/IRQ status remains Hi-Z). 2) When a fixed-cycle timer interrupt event occurs, the interrupt signal is canceled (/IRQ status changes from low to Hi-Z). * Even when the TIE bit value is "0" another interrupt event may change the /IRQ status to low (or may hold /IRQ = "L").
	1	When a fixed-cycle timer interrupt event occurs, an interrupt signal is generated (/IRQ status changes from Hi-Z to low).

13.2.3. Fixed-cycle timer start timing

Counting down of the fixed-cycle timer value starts at the falling edge of the CLK signal that occurs when the TE value is changed from "0" to "1" (after bit 0 is transferred).



13.2.4. Fixed-cycle timer interrupt interval (example)

The combination of the source clock settings (settings in TSEL1 and TSEL0) and fixed-cycle timer countdown setting (Reg–B to Reg-C setting) sets the fixed-cycle timer interrupt interval, as shown in the following examples.

Timer Counter setting	Source clock			
	4096 Hz TSEL1,0 0 , 0	64 Hz TSEL1,0 0 , 1	1 Hz TSEL1,0 1 , 0	1/60 Hz TSEL1,0 1 , 1
0	–	–	–	–
1	244.14 μs	15.625 ms	1 s	1 min
2	488.28 μs	31.25 ms	2 s	2 min
⋮	⋮	⋮	⋮	⋮
41	10.010 ms	640.63 ms	41 s	41 min
82	20.020 ms	1.281 s	82 s	82 min
128	31.250 ms	2.000 s	128 s	128 min
192	46.875 ms	3.000 s	192 s	192 min
205	50.049 ms	3.203 s	205 s	205 min
320	78.125 ms	5.000 s	320 s	320 min
410	100.10 ms	6.406 s	410 s	410 min
640	156.25 ms	10.000 s	640 s	640 min
820	200.20 ms	12.813 s	820 s	820 min
1229	300.05 ms	19.203 s	1229 s	1229 min
1280	312.50 ms	20.000 s	1280 s	1280 min
1920	468.75 ms	30.000 s	1920 s	1920 min
2048	500.00 ms	32.000 s	2048 s	2048 min
2560	625.00 ms	40.000 s	2560 s	2560 min
3200	0.7813 s	50.000 s	3200 s	3200 min
3840	0.9375 s	60.000 s	3840 s	3840 min
⋮	⋮	⋮	⋮	⋮
4095	0.9998 s	63.984 s	4095 s	4095 min

- Fixed-cycle timer interrupt time error and fixed-cycle timer interrupt interval time

  A fixed-cycle timer interrupt time error is an error in the selected source clock's $^{+0}/_{-1}$ interval time. Accordingly, the fixed-cycle timer interrupt's interval (one cycle) falls within the following range in relation to the set time.

  Fixed-cycle timer interrupt's interval

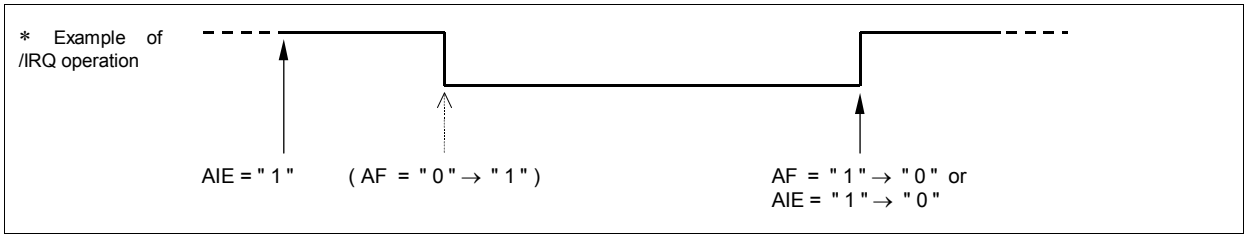
  (Fixed-cycle timer interrupt's set time(∗) – source clock interval) to (fixed-cycle timer interrupt set time)

  ∗) Fixed-cycle timer interrupt's set time = Source clock setting × Countdown timer setting for fixed-cycle timer

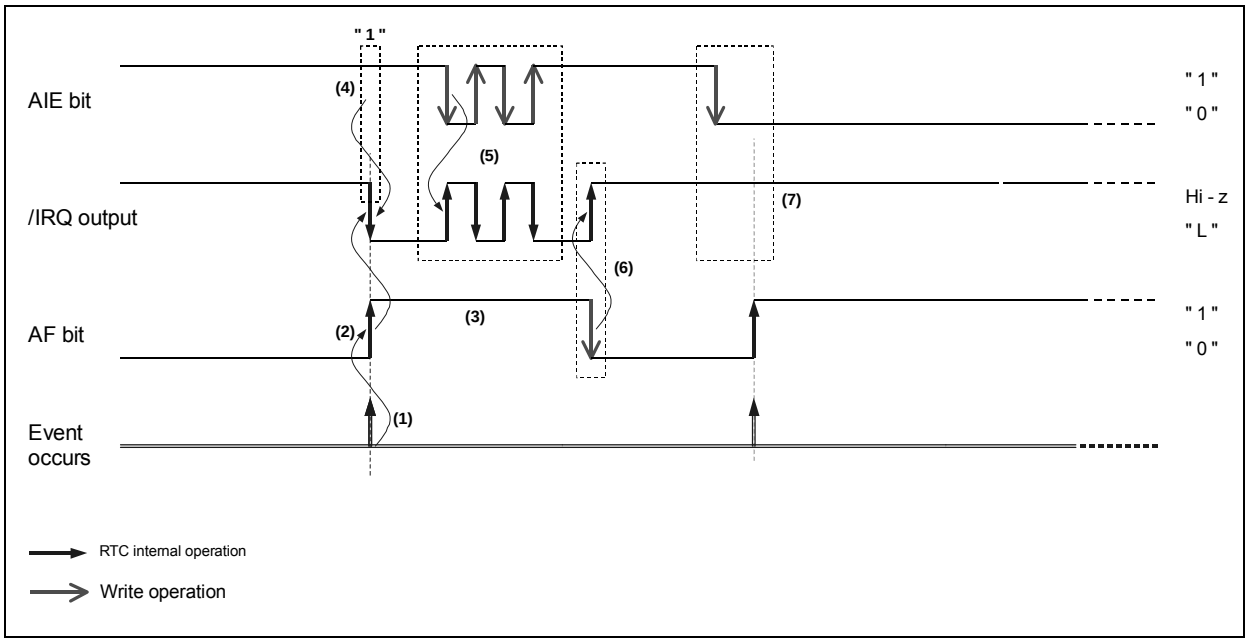
  ∗ The time actually set to the timer is adjusted by adding the time described above to the communication time for the serial data transfer clock used for the setting.

13.3. Alarm Interrupt Function

The alarm interrupt generation function generates interrupt events for alarm settings such as date, day, hour, and minute settings.
When an interrupt event occurs, the AF bit value is set to "1" and the /IRQ pin goes to low level to indicate that an event has occurred.



13.3.1. Diagram of alarm interrupt function



(1) The hour, minute, date or day when an alarm interrupt event is to occur is set in advance along with the WADA bit, and when the setting matches the current time an interrupt event occurs.
(Note) Even if the current date/time is used as the setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).

(2) When a time update interrupt event occurs, the AF bit values becomes "1".

(3) When the AF bit = "1", its value is retained until it is cleared to zero.

(4) If AIE = "1" when an alarm interrupt occurs, the /IRQ pin output goes low.
∗ When an alarm interrupt event occurs, /IRQ pin output goes low, and this status is then held until it is cleared via the AF bit or AIE bit.

(5) If the AIE value is changed from "1" to "0" while /IRQ is low, the /IRQ status immediately changes from low to Hi-Z. After the alarm interrupt occurs and before the AF bit value is cleared to zero, the /IRQ status can be controlled via the AIE bit.

(6) If the AF bit value is changed from "1" to "0" while /IRQ is low, the /IRQ status immediately changes from low to Hi-Z.

(7) If the AIE bit value is "0" when an alarm interrupt occurs, the /IRQ pin status remains Hi-Z.

13.3.2. Related registers for Alarm interrupt functions.

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	MIN	○	40	20	10	8	4	2	1
2	HOUR	○	○	20	10	8	4	2	1
3	WEEK	○	6	5	4	3	2	1	0
4	DAY	○	○	20	10	8	4	2	1
8	MIN Alarm	**AE**	40	20	10	8	4	2	1
9	HOUR Alarm	**AE**	•	20	10	8	4	2	1
A	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
D	Extension Register	*TEST1*	**WADA**	○	TE	FSEL1	FSEL0	TSEL1	TSEL0
E	Flag Register	*TEST2*	○	○	TF	**AF**	○	VLF	*RSV*
F	Control Register	*TEST3*	○	○	TIE	**AIE**	○	STOP	○

∗ Before entering settings for operations, we recommend writing a "0" to the AIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the STOP bit or RESET bit value is "1" alarm interrupt events do not occur.

∗ When the alarm interrupt function is not being used, the Alarm registers (Reg - 08h to 0Ah) can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.

∗ When the AIE bit value is "1" and the Alarm registers (Reg - 08h to 0Ah) is being used as a RAM register, /IRQ may be changed to low level unintentionally.

1) WADA bit (Week Alarm / Day Alarm Select)

The alarm interrupt function uses either "Day" or "Week" as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

WADA	Data	Description
Write / Read	0	Sets WEEK as target of alarm function (DAY setting is ignored)
	1	Sets DAY as target of alarm function (WEEK setting is ignored)

2) Alarm registers (Reg – 8[h] to A[h])

The hour, minute, date or day when an alarm interrupt event will occur is set using this register and the WADA bit.

In the WEEK alarm /Day alarm register (Reg - A), the setting selected via the WADA bit determines whether WEEK alarm data or DAY alarm data will be set. If WEEK has been selected via the WADA bit, multiple days can be set (such as Monday, Wednesday, Friday, Saturday).

When the settings made in the alarm registers and the WADA bit match the current time, the AF bit value is changed to "1". At that time, if the AIE bit value has already been set to "1", the /IRQ pin goes low.

∗1) The register that "1" was set to "AE" bit, doesn't compare alarm.
(Example) Write 80h (AE = "1") to the WEEK Alarm /DAY Alarm register (Reg - A):
Only the hour and minute settings are used as alarm comparison targets. The week and date settings are not used as alarm comparison targets.
As a result, alarm occurs if only an hour and minute accords with alarm data.

∗2) If all three AE bit values are "1" the week/date settings are ignored and an alarm interrupt event will occur once per minute.

3) AF bit (Alarm Flag)

When this flag bit value is already set to "0", occurrence of an alarm interrupt event changes it to "1". When this flag bit value is "1", its value is retained until a "0" is written to it.

AF	Data	Description
Write	0	The AF bit is cleared to zero to prepare for the next status detection * Clearing this bit to zero enables /IRQ low output to be canceled (/IRQ remains Hi-Z) when an alarm interrupt event has occurred.
	1	This bit is invalid after a "1" has been written to it.
Read	0	Alarm interrupt events are not detected.
	1	Alarm interrupt events are detected. (Result is retained until this bit is cleared to zero.)

4) AIE bit (Alarm Interrupt Enable)

When an alarm interrupt event occurs (when the AF bit value changes from "0" to "1"), this bit's value specifies whether an interrupt signal is generated (/IRQ status changes from Hi-Z to low) or is not generated (/IRQ status remains Hi-Z).

AIE	Data	Description
Write / Read	0	1) When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/IRQ status remains Hi-Z). 2) When an alarm interrupt event occurs, the interrupt signal is canceled (/IRQ status changes from low to Hi-Z). * Even when the AIE bit value is "0" another interrupt event may change the /IRQ status to low (or may hold /IRQ = "L").
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/IRQ status changes from Hi-Z to low). * When an alarm interrupt event occurs, low-level output from the /IRQ pin occurs only when the AIE bit value is "1". This value is retained (not automatically cleared) until the AF bit is cleared to zero.

13.4.3. Examples of alarm settings

1) Example of alarm settings when "Day" has been specified (and WADA bit = "0")

Day is specified WADA bit = "0"	Reg – A bit 7 AE	bit 6 S	bit 5 F	bit 4 T	bit 3 W	bit 2 T	bit 1 M	bit 0 S	Reg - 9 HOUR Alarm	Reg - 8 MIN Alarm
Monday through Friday, at 7:00 AM * Minute value is ignored	0	0	1	1	1	1	1	0	07 h	AE bit = 1
Every Saturday and Sunday, for 30 minutes each hour * Hour value is ignored	0	1	0	0	0	0	0	1	AE bit = 1	30 h
Every day, at 6:59 AM	0	1	1	1	1	1	1	1	18 h	59 h
	1	X	X	X	X	X	X	X		

X: Don't care

2) Example of alarm settings when "Day" has been specified (and WADA bit = "1")

Day is specified WADA bit = "1"	Reg - A bit 7 AE	bit 6 •	bit 5 20	bit 4 10	bit 3 08	bit 2 04	bit 1 02	bit 0 01	Reg - 9 HOUR Alarm	Reg - 8 MIN Alarm
First of each month, at 7:00 AM * Minute value is ignored	0	0	0	0	0	0	0	1	07 h	AE bit = 1
15th of each month, for 30 minutes each hour * Hour value is ignored	0	0	0	1	0	1	0	1	AE bit = 1	30 h
Every day, at 6:59 PM	1	X	X	X	X	X	X	X	18 h	59 h

X: Don't care

13.4. /IRQ "L" Interrupt Output When Interrupt Function Operates

1) Setting interrupt events to occur in response to /IRQ "L" interrupt output

The /IRQ interrupt output pin is shared as the output pin for two kinds of interrupt events: events related to the fixed-cycle timer interrupt function and events related to the alarm interrupt function.

When an interrupt occurs (when /IRQ is at low level ("L")), read the TF and AF flags to determine which type of interrupt event occurred (which flag value changed to "1").

2) How to prevent /IRQ pin from going to low level ("L")

To prevent the /IRQ pin from going to low level ("L"), clear all TIE and AIE bits to zero.
To detect when an interrupt event has occurred without having to set the /IRQ pin to low level, monitor the TF and AF flag bit values to see if the target interrupt event has occurred (i.e., to see if either flag bit value changes from "0" to "1").

13.5. FOUT function [clock output function]

The clock signal (with precision equal to that of the on-chip crystal osillator) can be output (as C-MOS output) via the FOUT pin.

13.5.1. FOUT control register.

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
D	Extension Register	***TEST1***	WADA	○	TE	**FSEL1**	**FSEL0**	TSEL1	TSEL0

By a combination of FSEL and FOE, an FOUT terminal outputs 32768Hz and 1024Hz and 1Hz and can stop the output.

13.5.2. FOUT function table.

FOE pin input	FSEL1 bit	FSEL0 bit	FOUT pin output	
X (Don't care)	0	0	32768 Hz Output (C-MOS output)	
	0	1	1024 Hz Output (C-MOS output)	
	1	0	1 Hz Output (C-MOS output)	
" H "	1	1	32768 Hz Output (C-MOS output)	∗1
" L "	1	1	OFF (high impedance)	∗2

∗1 At initial power-on , in case of FOE input is high, 32768Hz is selected automatically by power-on-reset-function.

∗2 The combination to disable the FOUT output is FOE=Low and FSEL=FSEL1 = ″1″ only.
Other combinations output any frequency from FOUT terminal.

∗3 When control about ON and OFF of the output from FOUT by only FSEL, should FOE=L.

FOE pin input	**FSEL1 bit**	**FSEL0 bit**	FOUT pin output	
" L "	**0**	**0**	32768 Hz Output (C-MOS output)	
	0	**1**	1024 Hz Output (C-MOS output)	
	1	**0**	1 Hz Output (C-MOS output)	
	1	**1**	32768 Hz Output (C-MOS output)	∗1

∗4 When control about ON and OFF of the output from FOUT by only by FOE terminal, should FSEL0=FSEL1=″0″.
Note: The control frequency is 32768Hz only.

FSEL1 bit	FSEL0 bit	**FOE pin input**	FOUT pin output
1	1	**" H "**	32768 Hz Output (C-MOS output)
		" L "	OFF (high impedance)

At initial power-on, FSEL0 and FSEL1 are set to ″1″ by power-on-reset function.

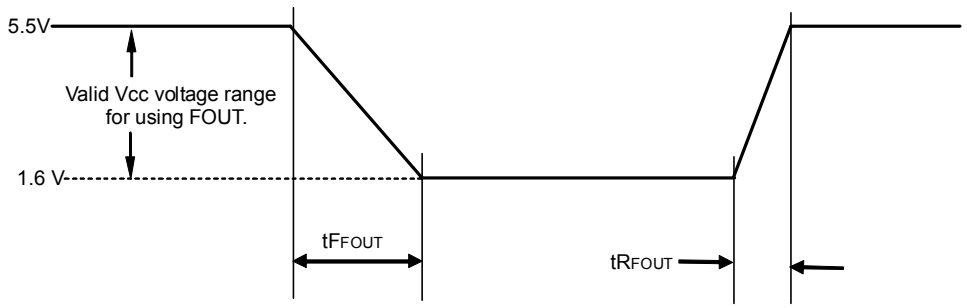
13.5.3. Attention of FOUT function.

Note 1
Valid voltage range for FOUT function is 1.6V to 5.5V. (Please see operating voltage.)

Note 2
A disappearance of the FOUT output when the voltage sharply went up and down.

For example, Vcc voltage of the RTC is come and go between Main power and backup battery.
The clock output from FOUT disappears then during several miliseconds when a sharp voltage change happens.
Please check that there is not a problem by this characteristic on your system.

An reference example of a power up and down timing without affect to FOUT.



tFFOUT Please make speed to descend of a power supply voltage loose than 4ms/V.
tRFOUT Please make speed to rise of a power supply voltage loose than one ms/V.

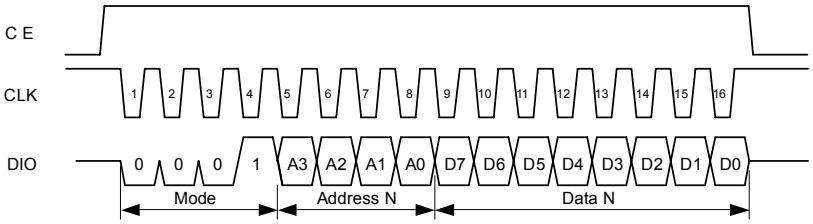
Note 3
The effect of STOP bit to FOUT functions.
When STOP = "1", 32768Hz and 1024Hz output is possible.
But 1Hz output is disabled.

13.6. Read/Write of data

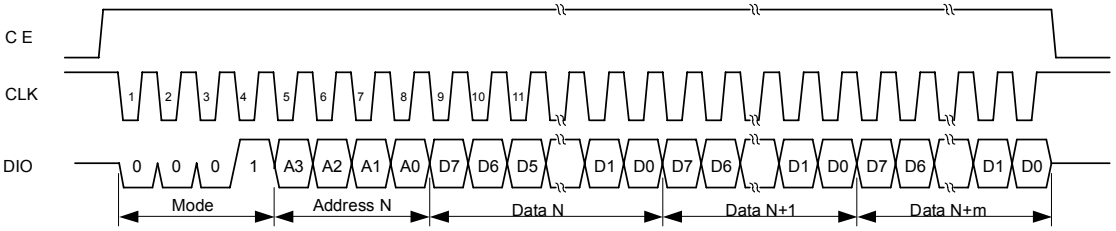
For both read and write, first set up chip condition to CE="H", then specify the 4-bits address, and finally read or write in 8-bits units.
Both read and write use MSB-first. In continuous operation, objected address is auto incremented.
Auto incrementing of the address is cyclic, so address "F" is followed by address "0".

13.6.1. Write of data

1) One-shot writing



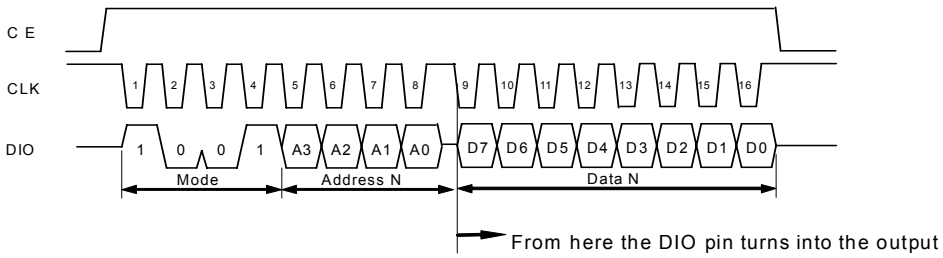
2) Continuous writing



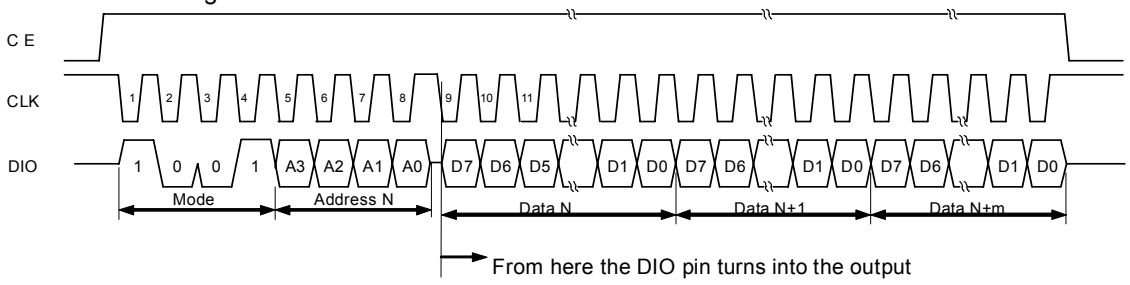
*When writing data, the data needs to be entered in 8-bits units.
If the input of data in 8-bits unit is not completed before CE input falls, the 8-bits data will not be written properly at the time CE input falls.

13.6.2. Read of data

1) One-shot reading



2) Continuous reading



13.6.3. Write/Read mode setting code for each bank

Mode	設定コード
Write	1 [h]
Read	9 [h]

*In the mode setting code, if a value other than those listed is used, the subsequent data will be ignored and the DIO pin remains in the Hi-z state.

EPSON TOYOCOM

Application Manual

AMERICA

EPSON ELECTRONICS AMERICA, INC.

HEADQUARTER 2580 Orchard Parkway, San Jose, CA 95131, U.S.A.
Phone: (1)800-228-3964 (Toll free) : (1)408-922-0200 (Main)
Fax: (1)408-922-0238
http://www.eea.epson.com

Atlanta Office One Crown Center 1895 Phoenix Blvd. Suite 348 Atlanta,GA 30349
Phone: (1)800-228-3964 (Toll free) : (1)770-907-7667 (Main)

Boston Office 301Edgewater Place, Ste. 120, Wakefield, MA 01880, U.S.A.
Phone: (1)800-922-7667 (Toll free) : (1)781-246-3600 (Main)
Fax: (1)781-246-5443

Chicago Office 1827 Walden Office Square. Suite 450 Schaumburg, IL 60173
Phone: (1)847-925-8350
Fax: (1)847 925-8965

El Segundo Office 1960 E. Grand Ave., 2nd Floor, El Segundo, CA 90245, U.S.A.
Phone: (1)800-249-7730 (Toll free) : (1)310-955-5300 (Main)
Fax: (1)310-955-5400

EUROPE

EPSON EUROPE ELECTRONICS GmbH

HEADQUARTER Riesstrasse 15, 80992 Munich, Germany
Phone: (49)-(0)89-14005-0 Fax: (49)-(0)89-14005-110
http://www.epson-electronics.de

ASIA

EPSON (CHINA) CO., LTD.
7F, Jinbao Building No.89 Jinbao Street Dongcheng District, Beijing, China, 100005
Phone: (86) 10-8522-1199 Fax: (86) 10-8522-1120
http://www.epson.com.cn

Shinghai Branch High-Tech Building,900 Yishan Road Shanghai 200233,China
Phone: (86) 21-5423-5577 Fax: (86) 21-5423-4677

EPSON HONG KONG LTD.
20/F., Harbour Centre, 25 Harbour Road, Wanchai,Hong kong
Phone: (852) 2585-4600 Fax: (852) 2827-2152
http://www.epson.com.hk

EPSON ELECTRONIC TECHNOLOGY DEVELOPMENT (SHENZHEN)CO., LTD.
12/F, Dawning Mansion,#12 Keji South Road, Hi-Tech Park,Shenzhen, China
Phone: (86) 755-26993828 Fax: (86) 755-26993838

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
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Phone: (886) 2-8786-6688 Fax: (886)2-8786-6660
http://www.epson.com.tw

EPSON SINGAPORE PTE. LTD.
No 1 HarbourFront Place, #03-02 HarbourFront Tower One, Singapore 098633.
Phone: (65)- 6586-5500 Fax: (65) 6271-3182
http://www.epson.com.sg

SEIKO EPSON CORPORATION KOREA Office
50F, KLI 63 Building,60 Yoido-dong, Youngdeungpo-Ku, Seoul, 150-763, Korea
Phone: (82) 2-784-6027 Fax: (82) 2-767-3677
http://www.epson-device.co.kr

Gumi Branch Office 2F, Grand Bldg,457-4, Songjeong-dong Gumi-City,Gyongsangbuk-Do,
730-090, Korea
Phone: (82) 54-454-6027 Fax: (82) 54-454-6093

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深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com