Application manual

Real Time Clock Module

RA8804CE

Product name	Product number
RA8804CE XA	X1B000381A00100
RA8804CE XB	X1B000381A00200

EPSON

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com
微信扫码咨询客服

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ETM60E Revision History

Rev. No.	Date	Page	Description
01	30.Apr.2018		Release
02	27.Jun.2018	17	5) RESET bit] It explained detailed function of RESET. 4) RESET bit
		47	8.15. Figure of 32kHz-TCXO was updated. SCL and SDA connects to GND. " 32.768 kHz DTCXO Connection "
03	19.Nov.2021	All	Document contents and format was update to same as RX8804CE. Ex. Some block diagram etc.
		30	As for time of auto release of timer interruption, Symbol name was update to tRTN2 from tRTN. *"TSEL1, TSEL0 bit"*
		33	Wakeup Timer Timing chart was optimized. "8.3.5. Wakeup Timer Interrupt Timing Chart"
		34 35	Optimized explanation of the Time-Update interruption. 8.7. Time Update Interrupt Function *"Timing chart of Time update interruption"*
		34	As for time of auto release of Time update interruption, Symbol name was updated to tRTN1 from tRTN. "USEL (Update Interrupt Select) bit"
		48	Note is added the Metal pad of package. 9.1.External Dimensions
04	26.Feb.2025	All	The link to index was added to all footer.
		42	Software reset command has been release. 8.10.1. Software Reset Procedure
		30	TSTP bit typo was corrected. 2) TSTP (Timer STOP) bit TSTP = 1: Timer stopped. TSTP = 0: Timer continued.
05	30.Jun.2025	2	・Revised notes regarding use of this manual. ・Addition of disclaimer information.

Note, Past page numbers may have changed due to new revision work.

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INDEX

NOTICE 2
ETM60E Revision History 3
Software reset command has been release. 3
8.10.1. Software Reset Procedure 3
INDEX 4
Overview 6
2. Block Diagram 6
3. Terminal Description 7
3.1. Terminal Connections 7
3.2. Pin Functions 7
4. Absolute Maximum Ratings 8
5. Recommended Operating Conditions 8
6. Frequency Characteristics 8
7. Electrical Characteristics 9
7.1. DC Characteristics 9
7.2. AC Characteristics 10
7.3. Reference Characteristics 11
7.3.1 Temperature Compensation and Consumption Current 11
7.3.2 IDD vs TC Characteristics for Reference 11
7.3.3 Reference characteristic of I^2C-Bus active current. 11
8. Use Methods 12
8.1. Description of Registers 12
8.1.1. Write / Read and Bank Select 12
8.1.2. Register Table (Basic time and calendar register) 12
8.1.3. Register Table (Time stamp, EVIN, SOUT, Timer) 13
8.1.4. Quick Reference 13
8.1.5 Initial Value of Registers 13
8.2. Details of Registers 14
8.2.1. Clock Counter (SEC - YEAR) 14
8.2.2. Alarm Registers 15
8.2.3. Wakeup Timer Control Registers 16
8.2.4. Control Registers, Flag Registers 16
8.2.5. SOUT Control Register 18
8.2.6. Time Stamp Data Event Controller Register 19
8.3. SOUT Function 22
8.3.1. Various Function of SOUT 22
8.3.2. SOUT Function Program ex.1 22
8.4. EVIN Interrupt and Time Stamp Function 24
8.4.1. Time Stamp Program ex. 24
8.4.2. Timing Chart of EVIN Time Stamping 25
8.4.3. /INT pin Operation when an Interrupt Occurs. 25
8.5. Alarm Interrupt Function 26
8.5.1. Alarm Interrupt Function 26
8.5.2. Alarm Interrupt Function Register 26
8.5.3. Examples of Alarm Settings 27
8.5.4. Alarm Interrupt Timing Chart 28
8.5.5. /INT pin Operation when an Interrupt Occurs. 29
8.6. Wakeup Timer Interrupt Function 29
8.6.1. Wakeup Timer Interrupt Function 29
8.6.2. Wakeup Timer Interruption Registers. 29
8.6.3. Wakeup Timer Start Timing 31
8.3.4. Wakeup Timer Interrupt Interval (example) 32
8.3.5. Wakeup Timer Interrupt Timing Chart 33
8.7. Time Update Interrupt Function 34
8.7.1. Time Update Interrupt Function 34
8.7.2. Related Registers for Time Update Interrupt Functions 34
8.7.3. Time Update Interrupt Function Timing Chart 35
8.8. Temperature Compensation Function 36
8.8.1. Temperature Compensation Function 36
8.8.2. Related Registers for Temperature Compensation Function 36
8.9. Reading / Writing Data via the I^2C-Bus Interface 37

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8.9.1. Overview of I²C-Bus 37
8.9.2. System Configuration 37
8.9.3. Starting and stopping I²C-Bus communications 38
8.9.4. Data Transfers and Acknowledge Responses during I²C-Bus Communications 39
8.9.5. Slave Address 40
8.9.6. I²C-Bus Protocol 41
8.10. Backup and Recovery 42
8.10.1. Software Reset Procedure 42
8.11. About Access at the Time of Backup Return and Initial Power Supply 43
8.12. Flow Chart 44
8.13. Connection with Typical Microcontroller 47
8.14. When Used as a Clock Source (32.768 kHz DTCXO) 47
9. External Dimensions / Marking Layout 48
9.1. External Dimensions 48
9.2. Marking Layout 48
10.Application Notes 49
11.Figures 50
12.Tables 50

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RA8804CE

- Built-in 32.768 kHz DTCXO
- Interface Type : I²C-Bus (Up to 400 kHz)
- Low current consumption at backup : 350 nA / 3.0 V Typ.
- Wide time-keeping voltage range : 1.5 V to 5.5 V
- Wide interface voltage range : 1.6 V to 5.5 V
- SOUT can output self monitoring status, voltage down etc. : SOUT can output programmed H / L level also.
- Time stamp function of Seconds from Year : One time recorded by trigger of EVIN.
- EVIN is equipped for time stamp trigger : It has connectable pull up resistor
- Alarm interrupt function : Combination of Day, Date, Hour, Minute, and AE bit
- Wakeup timer interrupt function : Auto repeated 244.14 µs to 32 years
- Time update interrupt function : Every second or every minute
- Temperature compensated 32.768 kHz or other output : Available output enable control
- Auto correction of leap years : In 60 seconds, revision of a leap second is possible.
- AEC-Q100 compliant for automotive applications

Overview

This module is an I²C-Bus interface-compliant real-time clock which includes a 32.768 kHz DTCXO. In addition to providing a calendar (year, month, date, day, hour, minute, second) function and a clock counter function, this module provides an abundance of other functions including an alarm function, wakeup timer function, time update interrupt function, 32.768 kHz output function, Time stamp function with EVIN-pin trigger, and. Programmable output function to SOUT-pin of interrupt Flags or self monitoring Flags.

The devices in this module are fabricated via a CMOS process for low current consumption, which enables long-term battery back-up.

2. Block Diagram

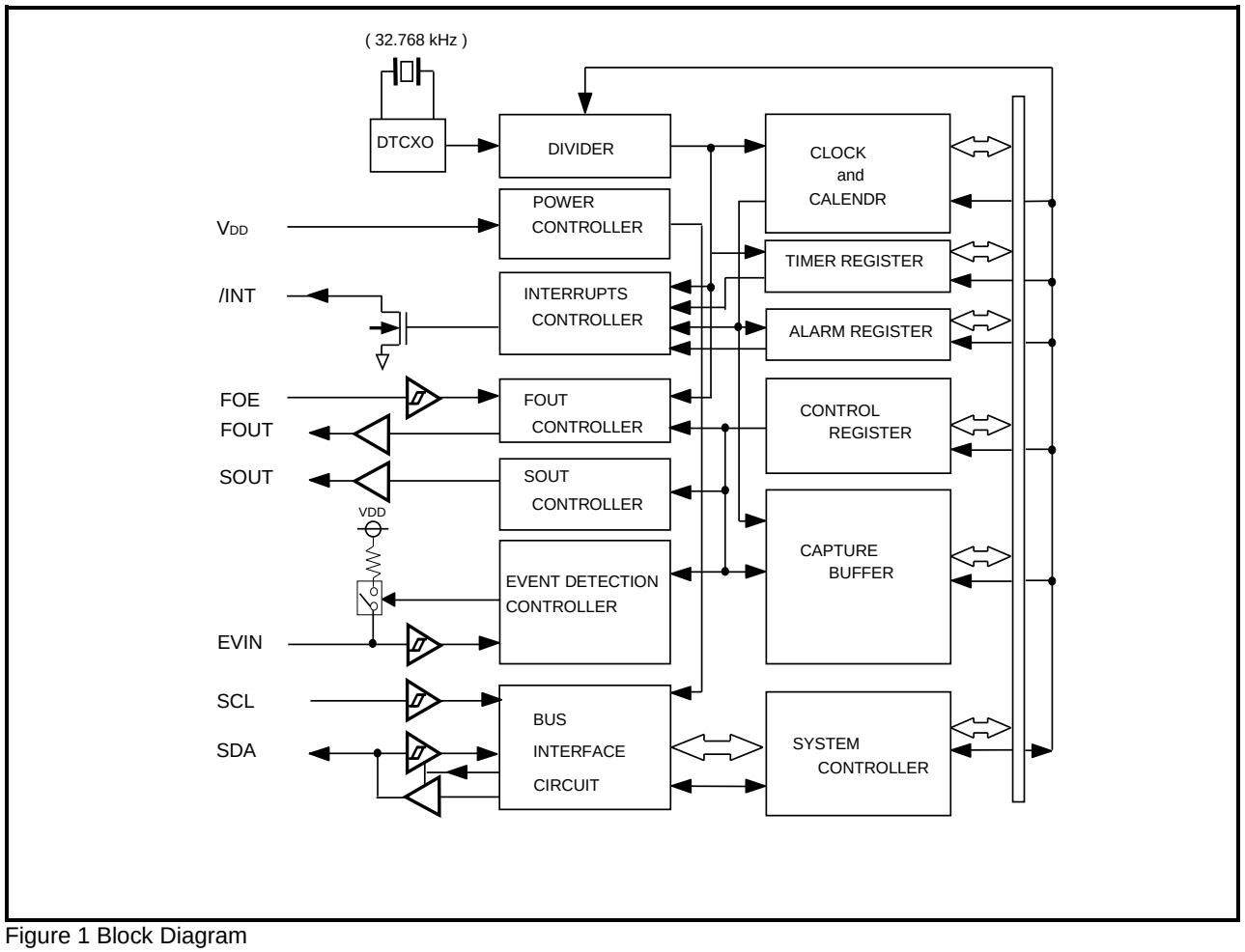


Figure 1 Block Diagram

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3. Terminal Description

3.1. Terminal Connections

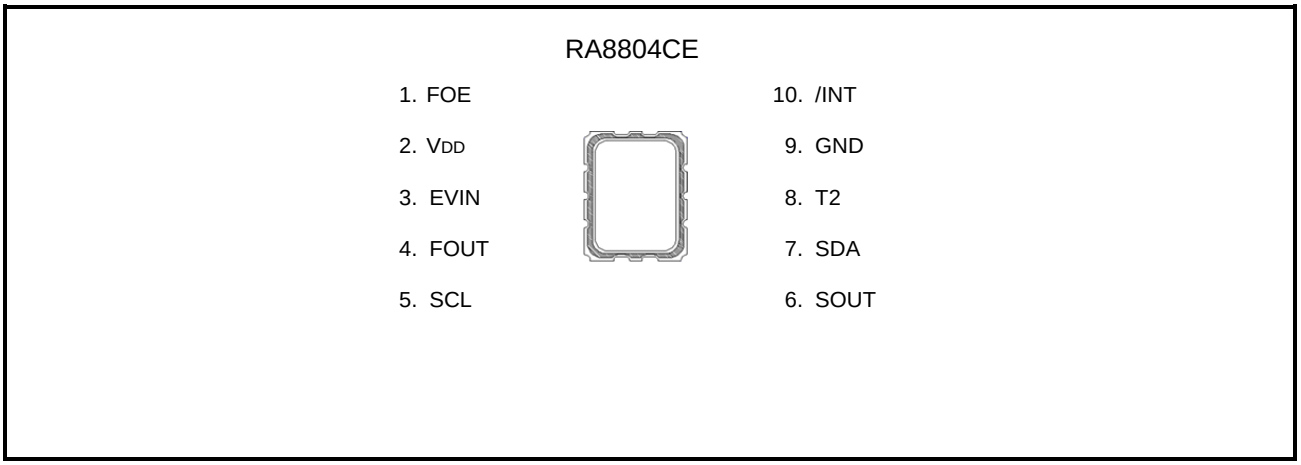


Figure 2 Pin Layout

3.2. Pin Functions

Table 1 Pin Functions

Signal name	I/O	Function
SDA	I/O	This pin's signal is used for input and output of address, data, and ACK bits, synchronized with the serial clock used for I^2C-Bus communications Since the SDA pin is an N-ch open drain pin during output, be sure to connect a suitable pull-up resistance relative to the signal line capacity
SCL	Input	This is the serial clock input pin for I^2C-Bus communications.
FOUT	Output	This is the CMOS output pin with output control provided via the FOE pin. When FOE = "H" (high level), this pin outputs a 32.768 kHz signal. (depend on FSEL bit) When output is stopped, the FOUT pin = Hi-Z (high impedance)
FOE	Input	This is an input pin used to control the output mode of the FOUT pin When this pin's level is high, the FOUT pin is in output mode. When it is low, output via the FOUT pin is stopped
/INT	Output	This pin is used to output alarm signals, timer signals, time update signals, and other signals. This pin is an open drain pin
EVIN	Input	Trigger input terminal for time stamps. Pull-up resistor selectable by register setting
SOUT	Output	SOUT is push-pull for the inside state output SOUT outputs state of a specified flag bit or programmed logical 1 or 0
VDD	–	This pin is connected to a positive power supply
GND	–	This pin is connected to a ground
T2	–	Use only for testing in the factory (Do not connect externally)

Note: Be sure to connect a bypass capacitor rated at least 0.1 μF between VDD and GND.

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4. Absolute Maximum Ratings

Table 2 Absolute Maximum Rating

GND = 0 V

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	Between V_{DD} and GND	−0.3 to +6.5	V
Input voltage (1)	V_{IN1}	FOE, SCL, SDA, EVIN pins	GND −0.3 to +6.5	V
Input voltage (2)	V_{IN2}	EVIN pin	GND −0.3 to V_{DD} +0.3	V
Output voltage (1)	V_{OUT1}	FOUT and SOUT pins	GND −0.3 to V_{DD} +0.3	V
Output voltage (2)	V_{OUT2}	SDA and /INT pins	GND −0.3 to +6.5	V
Storage temperature	T_{STG}	When stored separately, without packaging	−55 to +125	°C

5. Recommended Operating Conditions

Table 3 Recommended Operating Conditions

GND = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{ACC}	Between V_{DD} and GND	1.6	3.0	5.5	V
Temp. compensation voltage	V_{TEM}	–	1.5	3.0	5.5	V
Clock supply voltage	V_{CLK}	–	1.5	3.0	5.5	V
Operating temperature	Ta	No condensation	−40	+25	+105	°C

* To apply Min. value of V_{ACC} and V_{CLK}, the V_{DD} needs to be supplied with more than 1.5 V at least for the oscillation to stabilize (oscillation start time tSTA).
* The Min. value of V_{CLK} is the Min. voltage required to retain the time counting function. it is however necessary to maintain V_{TEM} till the oscillation of the oscillator has stabilized (oscillation start time tSTA).
* The temperature compensation stops working below Min. value of V_{TEM}.

6. Frequency Characteristics

Table 4 Frequency Characteristics

GND = 0 V

Item	Symbol	Condition		Rating	Unit
Frequency stability	Δf/f	XA	Ta = 0 to +50 °C, V_{DD} = 3.0 V Ta = -40 to +85 °C, V_{DD} = 3.0 V Ta = -85 to +105 °C, V_{DD} = 3.0 V	±1.9 *1 ±3.4 *2 ±8.0 *3	× 10^{-6}
		XB	Ta = 0 to +50 °C, V_{DD} = 3.0 V Ta = -40 to +85 °C, V_{DD} = 3.0 V Ta = -85 to +105 °C, V_{DD} = 3.0 V	±3.8 *4 ±5.0 *5 ±8.0 *3	
Frequency/voltage characteristics	f/V	Ta= +25 °C, V_{DD}=1.5 V to 5.5 V		±1.0 Max.	× 10^{-6} / V
FOUT Symmetry	SYM	50% V_{DD} level, +25 °C, V_{DD} = 1.5 V to 5.5 V		50 ± 10	%
Oscillation start time	tSTA	Ta = +25 °C, V_{DD} = 1.5 V ~ 5.5 V Ta = -40 to +85 °C, V_{DD} = 1.6 V to 5.5 V		1.0 Max. 3.0 Max.	s
Aging	fa	Ta = +25 °C, V_{DD} = 3.0 V, first year		±3 Max.	× 10^{-6} / year
Reflow	fref	260 °C Max. 2 times		±3 Max. *6	× 10^{-6}

*1 5 s error per a month.
*2 9 s error per a month.
*3 21 s error per a month.
*4 10 s error per a month.
*5 13.2 s error per a month.
*6 The result that it was measured at 25 °C, 24 hours after processing of reflow soldering.

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7. Electrical Characteristics

7.1. DC Characteristics

Table 5 DC Characteristics

*Unless otherwise specified, GND = 0 V, V_{DD} = 1.5 V to 5.5 V, Ta = –40 °C to +105 °C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Average Current consumption (1)	I_{DD1}	fSCL = 0 Hz, /INT = Hi-Z, FOUT is stopped Temp compensation interval 2.0 s	V_{DD} = 5 V		0.40	1.6	µA
Average Current consumption (2)	I_{DD2}		V_{DD} = 3 V		0.35	1.5	
Average Current consumption (3)	I_{DD3}	fSCL = 0 Hz, /INT = Hi-Z, FOUT outputs 32 kHz, CL = 0 pF Temp compensation interval 2.0 s	V_{DD} = 5 V		1.1	3.1	
Average Current consumption (4)	I_{DD4}		V_{DD} = 3 V		1.0	3.0	
Average Current consumption (5)	I_{DD5}	fSCL = 0 Hz, /INT = Hi-Z, FOUT outputs 32 kHz, CL = 30 pF Temp compensation interval 2.0 s	V_{DD} = 5 V		6.1	8.1	
Average Current consumption (6)	I_{DD6}		V_{DD} = 3 V		4.0	6.0	
Average Current consumption (7)	I_{DD7}	fSCL = 0 Hz, /INT = Hi-Z, FOUT is stopped Temp compensation is stopped.	V_{DD} = 5 V		0.38	1.55	
Average Current consumption (8)	I_{DD8}		V_{DD} = 3 V		0.33	1.45	
Peak Current consumption (1)	I_{DD9}	fSCL = 0 Hz, /INT = V_{DD}, FOUT is stopped Temp compensation ON (peak)	V_{DD} = 5 V		55	100	
Peak Current consumption (2)	I_{DD10}		V_{DD} = 3 V		50	95	
High-level input voltage	V_{IH1}	SCL, SDA, FOE		0.8 × V_{DD}		5.5	V
	V_{IH2}	EVIN		0.8 × V_{DD}		V_{DD}	
Low-level input voltage	V_{IL}	SCL, SDA, FOE, EVIN		GND – 0.3		0.2 × V_{DD}	
High-level output voltage	V_{OH1}	FOUT, SOUT	V_{DD} = 5 V, I_{OH} = –1 mA	4.5		5.0	
	V_{OH2}		V_{DD} = 3 V, I_{OH} = –1 mA	2.2		3.0	
	V_{OH3}		V_{DD} = 3 V, I_{OH} = –100 µA	2.9		3.0	
Low-level output voltage	V_{OL1}	FOUT, SOUT	V_{DD} = 5 V, I_{OL} = 1 mA	GND		GND + 0.5	
	V_{OL2}		V_{DD} = 3 V, I_{OL} = 1 mA	GND		GND + 0.8	
	V_{OL3}		V_{DD} = 3 V, I_{OL} = 100 µA	GND		GND + 0.1	
	V_{OL4}	/INT	V_{DD} = 5 V, I_{OL} = 1 mA	GND		GND + 0.25	
	V_{OL5}		V_{DD} = 3 V, I_{OL} = 1 mA	GND		GND + 0.4	
	V_{OL6}	SDA	V_{DD} ≥ 2 V, I_{OL} = 3 mA	GND		GND + 0.4	
Input leakage current	I_{LK}	INPUT pins, VIN = V_{DD} or GND		–0.5		0.5	µA
Output leakage current	I_{OZ}	Output pins, output voltage = V_{DD} or GND		–0.5		0.5	
Pull-up Resistor	R_{EVIN}	EVIN		125	500	2000	kΩ
Detection voltage of VDET	V_{DET}	V_{DD}		1.41	1.45	1.49	V
Detection voltage of VLF	V_{LOW}	V_{DD}		0.9	1.0	1.2	

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7.2. AC Characteristics

Table 6 AC Characteristics

* Unless otherwise specified, GND = 0 V , V_{DD} = 1.6 V to 5.5 V , Ta = –40 °C to +105 °C

Item	Symbol	Condition	SCL = 100 kHz Standard Mode		SCL = 400 kHz Fast Mode		Unit
			Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	–	–	100	–	400	kHz
Start condition setup time	$t_{SU;STA}$	–	4.7	–	0.6	–	µs
Start condition hold time	$t_{HD;STA}$	–	4.0	–	0.6	–	µs
Data setup time	$t_{SU;DAT}$	–	250	–	100	–	ns
Data hold time	$t_{HD;DAT}$	–	0	–	0	–	ns
Stop condition setup time	$t_{SU;STO}$	–	4.0	–	0.6	–	µs
Bus idle time between start condition and stop condition	t_{BUF}	–	4.7	–	1.3	–	µs
Time when SCL = ”L”	t_{LOW}	–	4.7	–	1.3	–	µs
Time when SCL = “H”	t_{HIGH}	–	4.0	–	0.6	–	µs
Rise time for SCL and SDA	t_r	–	–	1.0	–	0.3	µs
Fall time for SCL and SDA	t_f	–	–	0.3	–	0.3	µs
Allowable spike time on bus	t_{SP}	–	–	50	–	50	ns

Timing chart

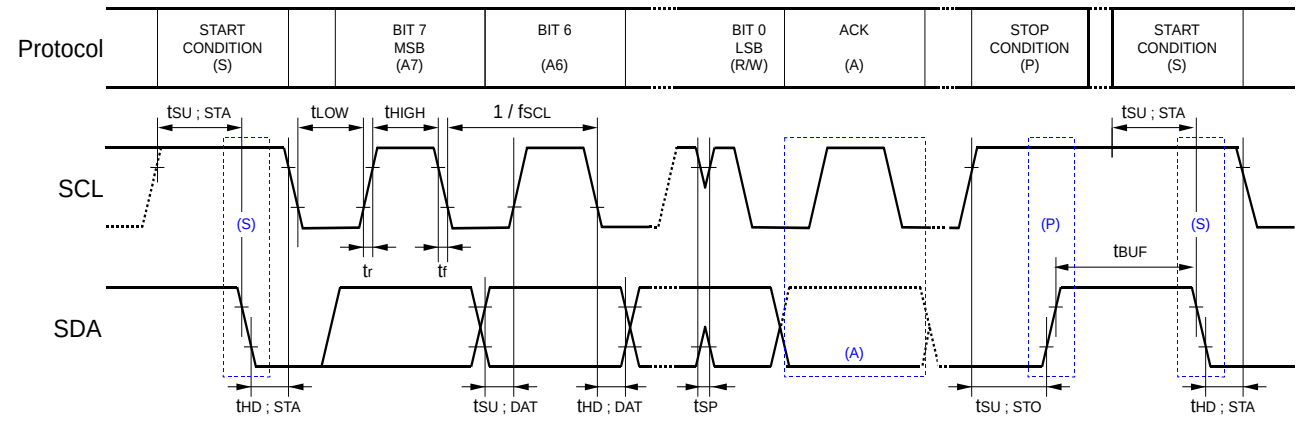


Figure 3 I²C-Bus Timing Chart

Note

1. As for the communication time of I²C-Bus, completion of less than 1 second is recommended. If such communication requires 1 second (Max.) or longer, the I²C-Bus interface is reset by the internal bus timeout function. When bus-time-out occur, SDA is released to Hi-Z input mode.
2. But readout data of a clock is stable anytime, and there isn’t contradiction. And it does not occur that data of a clock delay even if access time is prolonged.

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7.3. Reference Characteristics

7.3.1 Temperature Compensation and Consumption Current

The current consumption of RA8804CE increases at a timing of a temperature compensation.
As for this peak current consumption, it occurs in about 0.7ms.
I_{DD1}, I_{DD2} is the average current consumption at temperature compensation in 2 seconds cycle.

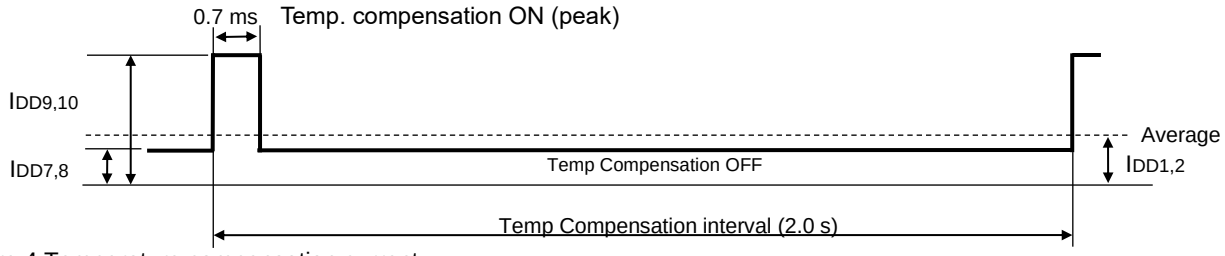


Figure 4 Temperature compensation current

7.3.2 I_{DD} vs TC Characteristics for Reference

Table 7 Average Current consumption I_{DD1}, I_{DD2}

Temp. compensation interval TC Unit s	I_{DD1} Typ. (V_{DD} = 5.0 V) Unit µA	I_{DD2} Typ. (V_{DD} = 3.0 V) Unit µA
0.5	0.46	0.40
2	0.38	0.35
10	0.38	0.33
30	0.38	0.33

7.3.3 Reference characteristic of I²C-Bus active current.

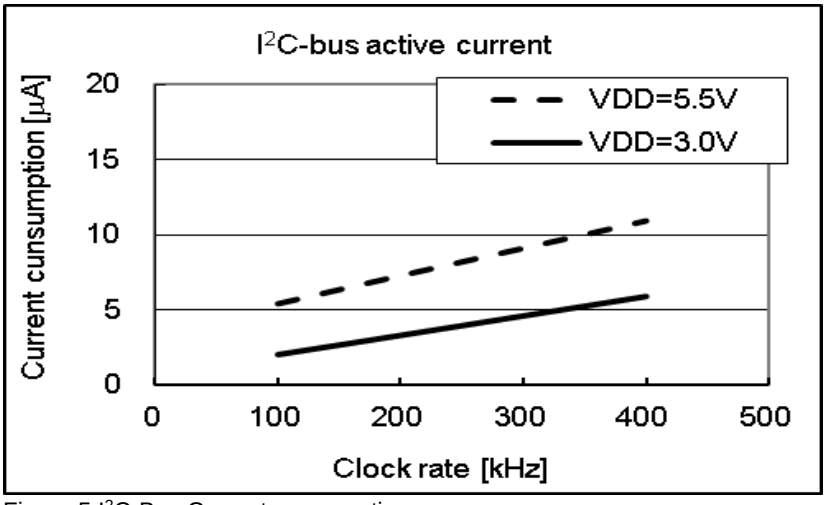


Figure 5 I²C-Bus Current consumption

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8. Use Methods

8.1. Description of Registers

8.1.1. Write / Read and Bank Select

Address 00h to 0Fh: Basic time and calendar register. It compatible with RX8803 and RX8900
Address 10h to 1Fh: Extension register
Access to more than address 20h is possible, but there is some control register for quality inspection.
Address is incremented automatically in lower 4 bits address.
Upper 4bits address are fixed. (00, ..., 0E, 0F, 00, 01), (10, ..., 1E, 1F, 10, 11)

Table 8 Register Division (00h ~ 0Fh)

	Basic register	Time stamp register	Access is prohibited
Address (8bit)	0Fh from 00h	1Fh from 10h	FFh from 20h

8.1.2. Register Table (Basic time and calendar register)

Table 9 Register Table (00h ~ 0Fh)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Init	Write
00	SEC	○	40	20	10	8	4	2	1		√
01	MIN	○	40	20	10	8	4	2	1		√
02	HOUR	○	○	20	10	8	4	2	1		√
03	WEEK	○	6	5	4	3	2	1	0		√
04	DAY	○	○	20	10	8	4	2	1		√
05	MONTH	○	○	○	10	8	4	2	1		√
06	YEAR	80	40	20	10	8	4	2	1		√
07	RAM	•	•	•	•	•	•	•	•		√
08	MIN Alarm	AE	40	20	10	8	4	2	1		√
09	HOUR Alarm	AE	•	20	10	8	4	2	1		√
0A	WEEK Alarm	AE	6	5	4	3	2	1	0		√
	DAY Alarm		•	20	10	8	4	2	1		
0B	Timer Counter 0	128	64	32	16	8	4	2	1		√
0C	Timer Counter 1	32768	16384	8132	4096	2048	1024	512	256		√
0D	Control1	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	02h	√
0E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	00h	√ *
0F	Control2	CSEL1	CSEL0	UIE	TIE	AIE	○	○	RESET	40h	√

○ Writing is avoided. Read value is 0, always. • It can read and write. √ is available. – avoid.
"Init" shows value of after power-on Reset. Unit is Hex.
*Note Refer to Flag Registers

Note After the initial power-up (from 0 V) or in case the VLF bit returns "1" , make sure to initialize all registers, before using the RTC.
Be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the data or time data is incorrect.

- Only a 0 can be written to the UF, TF, AF, VLF, VDET and EF bit.
  The EVMON bit is read only bit.
- Any bit marked with "○" should be used with a value of "0" after initialization.
- Any bit marked with "•" is a RAM bit that can be used to read or write any data.
- The TEST bit is used by the manufacturer for testing. Be sure to set "0" for this bit when writing.
- If an alarm function is not used, registers 08h-0Ah can be used as RAM. (AIE: "0")
- Reading register value of address 0Bh-0Ch and 1Fh is pre-set data.
  If a timer function is not used, register of 0Bh-0Ch and 1Fh can be used as RAM. (TE, TIE: "0")

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8.1.3. Register Table (Time stamp, EVIN, SOUT, Timer)

Table 10 Register Table (10h ~ 1Fh)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Init	Write
10	Time stamp SEC	○	40	20	10	8	4	2	1	00h	–
11	Time stamp MIN	○	40	20	10	8	4	2	1	00h	–
12	Time stamp HOUR	○	○	20	10	8	4	2	1	00h	–
13	Time stamp WEEK	○	6	5	4	3	2	1	0	00h	–
14	Time stamp DAY	○	○	20	10	8	4	2	1	00h	–
15	Time stamp MONTH	TSVLF	TSVDET	○	10	8	4	2	1	00h	–
16	Time stamp YEAR	80	40	20	10	8	4	2	1	00h	–
17	EVIN set	ECP	EHL	EPU	RCE	EIE	○	ET1	ET0	00h	√
18	EVIN det	EF	○	○	○	EVMON	○	○	○	00h	√
19	SOUT set1	SOE7	SOE6	SOE5	SOE4	SOE3	SOE2	SOE1	SOE0	00h	√
1A	SOUT set2	DCE	DC	○	○	SRV	FS2	FS1	FS0	00h	√
1B	Timer set	TSTP	TRES	○	○	○	○	○	○	00h	√
1C	Timer0	128	64	32	16	8	4	2	1	00h	–
1D	Timer1	32768	16384	8192	4096	2048	1024	512	256	00h	–
1E	Timer2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	00h	–
1F	Timer counter 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	00h	√

○ Writing is avoided. Read value is 0, always. • It can read and write. √ is available. – avoid.
"Init" shows value of after power-on Reset. Unit is Hex.

8.1.4. Quick Reference

Table 11 Quick Reference

Update interrupt selection		Default
USEL = 0	Every updates of seconds.	√
USEL = 1	Every updates of minutes.	
Output Frequency selection		
FSEL1, FSEL0 = 00	32.768 kHz	√
FSEL1, FSEL0 = 01	1024 Hz	
FSEL1, FSEL0 = 10	1 Hz	
FSEL1, FSEL0 = 11	32.768 kHz	
Timer source clock selection		
TSEL1, TSEL0 = 00	4096 Hz	
TSEL1, TSEL0 = 01	64 Hz	
TSEL1, TSEL0 = 10	1Hz. Not updates of seconds.	√
TSEL1, TSEL0 = 11	Every minute update	
Temperature compensation selection		
CSEL1, CSEL0 = 00	0.5 s	
CSEL1, CSEL0 = 01	2.0 s	√
CSEL1, CSEL0 = 10	10 s	
CSEL1, CSEL0 = 11	30 s	

8.1.5 Initial Value of Registers

Table 12 Registers Initial Value

	Registers' Initial value after power on reset
Initial Value	Register
1	TSEL1, VLF, VDET, CSEL0
0	TEST, WADA, USEL, TE, FSEL1, FSEL0, TSEL0, UF, TF, AF, EF, CSEL1, UIE, TIE, AIE, RESET, TSVLF, TSVDET, ECP, EHL, EPU, RCE, EIE, ET1, ET0, EVMON, SOE0 ~ SOE7, DCE, DC, SRV, FS0 ~ FS2, TRES, TSTP, All bits of address1Ch,1Dh,1Eh and 1Fh

All other register values are undefined, so be sure to perform a reset before using the module.

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8.2. Details of Registers

8.2.1. Clock Counter (SEC - YEAR)

·The data format is BCD format. For example, when the “seconds” register value is “0101 1001” it indicates 59 seconds.

24hours system is available.

Table 13 Clock, Calendar Register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00	SEC	O	40	20	10	8	4	2	1
01	MIN	O	40	20	10	8	4	2	1
02	HOUR	O	O	20	10	8	4	2	1
03	WEEK	O	6	5	4	3	2	1	0
04	DAY	O	O	20	10	8	4	2	1
05	MONTH	O	O	O	10	8	4	2	1
06	YEAR	80	40	20	10	8	4	2	1

1) SEC register

This second register counts from “00” to “01”, “02”, and up to 59 seconds, after 59 it starts again from 00 second.
When written any data to SEC register, less than a SEC counter (512 Hz from 2 Hz) is cleared to zero.
Thus, the time accuracy becomes 0 s to 30.5 μs. * (refer to Figure 6)
If highly precise time synchronization is needed, RESET bit setting to 1 is most suitable operation.
When 60 seconds were written to SEC register, it returns to 00 second in next update. This special update is the same as plus-adjustment of Leap second. This behavior is useful in the adjustments of Leap second.

2) MIN register

This minute register counts from “00” to “01”, “02”, and up to 59 minutes, after 59 it starts again from 00 minute.

3) HOUR register

This 24 hours register counts from “00” hour to “01”, “02”, “23”, ”00”, ”01”. “o” indicates write-protected bits. Zero is always read from these bits.

4) WEEK register

This WEEK register consists of 7bit shift registers.
The data values are counted as follows: Day 01h → Day 02h → Day 04h → Day 08h → Day 10h → Day 20h → Day 40h → Day 01h → Day 02h
The correspondence between days and count values is shown below.

Table 14 WEEK Register

WEEK	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Day of week	Data h
Write / Read	0	0	0	0	0	0	0	**1**	Sunday	01h
	0	0	0	0	0	0	**1**	0	Monday	02h
	0	0	0	0	0	**1**	0	0	Tuesday	04h
	0	0	0	0	**1**	0	0	0	Wednesday	08h
	0	0	0	**1**	0	0	0	0	Thursday	10h
	0	0	**1**	0	0	0	0	0	Friday	20h
	0	**1**	0	0	0	0	0	0	Saturday	40h
Write prohibit	* Do NOT set “1” more than one day at the same time. Also, note with caution that any setting other than the seven shown above should not be made as it may interfere with normal operation.								–	–

5) DAY Register

The updating of DAY register varies according to the month setting.
A leap year is set whenever the year value is a multiple of four (such as 04, 08, 12, 88, 92, or 96).
In February of a leap year, the counter counts dates from “01”, “02”, “03”, to “28”, “29”, “01”.

Table 15 DAY Register

DAY	Month	Date update pattern
Write / Read	1, 3, 5, 7, 8, 10, or 12	01, 02, 03 ~ 30, 31, 01 ~
	4, 6, 9, or 11	01, 02, 03 ~ 30, 01, 02 ~
	February in common year	01, 02, 03 ~ 28, 01, 02 ~
	February in leap year	01, 02, 03 ~ 28, 29, 01 ~

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3) MONTH register

This MONTH register counts from 01 (January), 02 (February), and up to 12 (December), then starts again since 01 (January).

4) YEAR register

This YEAR register counts from 00, 01, 02 and up to 99, then starts again since 00.
Any year multiple of four (04, 08, 12, 88, 92, 96, etc.) works as a leap year.

< Definition of leap years >

Leap year: year divisible by 4, year divisible by 400
Ex. 2000, 2004, 2008, 2012, 2096, 2400, 2800
Common year: year indivisible by 4, year divisible by 100
Ex. 2001, 2002, 2003, 2005, 2099, 2100, 2200, 2300, 2500

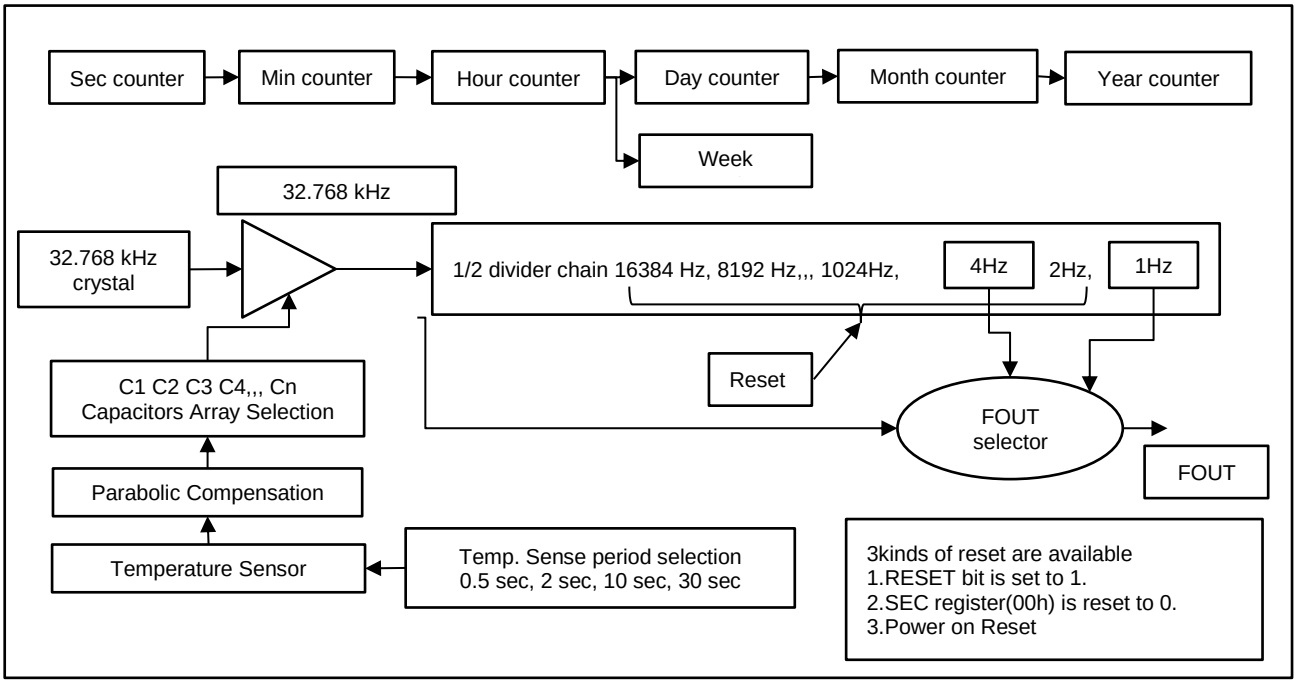


Figure 6 Internal clock distribution diagram

8.2.2. Alarm Registers

Table 16 Alarm registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
08	MIN Alarm	**AE**	**40**	**20**	**10**	**8**	**4**	**2**	**1**
09	HOUR Alarm	**AE**	•	**20**	**10**	**8**	**4**	**2**	**1**
0A	WEEK Alarm	**AE**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	DAY Alarm		•	**20**	**10**	**8**	**4**	**2**	**1**
0D	Control1	TEST	**WADA**	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E	Flag Register	○	○	UF	TF	**AF**	○	VLF	VDET
0F	Control2	CSEL1	CSEL0	UIE	TIE	**AIE**	○	○	RESET

The alarm interrupt function is used, along with the AEI, AF, and WADA bits, to set alarms for specified date, day, hour, and minute values

When the settings in the above alarm registers and the WADA bit match the current time, the /INT pin goes to low level and “1” is set to the AF bit to report that an alarm interruption has occurred

Please refer to Alarm Interrupt Function

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8.2.3. Wakeup Timer Control Registers

Table 17 Wakeup Timer Control Registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
0B	Timer Counter 0	128	64	32	16	8	4	2	1	√	√
0C	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256	√	√
1B	Timer set	TSTP	TRES	○	○	○	○	○	○	√	√
1C	Timer0	128	64	32	16	8	4	2	1	√	
1D	Timer1	32768	16384	8192	4096	2048	1024	512	256	√	
1E	Timer2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	√	
1F	Timer Counter 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	√	√

These registers are used to set the preset countdown value for the wakeup timer interrupt function.
The **TE, TF, TIE, and TSEL0 / 1 bits** are also used to set the wakeup timer interrupt function.
When the value in the above wakeup timer control register just changes from 01h to 00h, the /INT pin goes to low level and “1” is set to the TF bit to report that a wakeup timer interrupt event has occurred.
Please refer to Wakeup timer Control function

8.2.4. Control Registers, Flag Registers

Table 18 Control Register, Flag Register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0D	Control1	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
	(Default)	(0)	(0)	(0)	(0)	(0)	(0)	(1)	(0)
0E	Flag register	○	○	UF	TF	AF	○	VLF	VDET
	(Default)	(0)	(0)	(0)	(0)	(0)	(0)	(1)	(1)
0F	Control2	CSEL1	CSEL0	UIE	TIE	AIE	○	○	RESET
	(Default)	(0)	(1)	(0)	(0)	(0)	(0)	(0)	(0)

- The default value is loaded after powering up from 0 V, automatically.
- TEST must be always cleared by a zero.
- This register is used to specify the target for the alarm function or time update interrupt function and to select or set operations such as wakeup timer operations.

1) TEST bit

This is the manufacturer's test bit. Its value should always be “0”.
Be careful to avoid writing “1” to this bit when writing to other bits.

Table 19 Test bit

TEST	Data	Description
Write	0	TEST bit is cleared to 0
	1	Setting prohibited (manufacturer's test bit)
Read	0	TEST bit has been cleared to 0
	1	TEST bit has been set to 1. It be must clear to 0

2) VLF (Voltage Low Flag) bit

This flag bit indicates the history of clock operations due to low voltage.
Its value change from “0” to “1” indicates a possibility of data loss or time data error, and all the data of registers should be initialized.
Once this flag bit's value is “1”, its value is retained until a “0” is written to it.
After powering up from 0 V, make sure to set this bit's value to “1”.
Please refer to 8.10. Backup and Recovery.

Table 20 VLF bit

VLF	Data	Description
Write	0	The VLF bit is cleared to 0 to prepare for the next status detection
	1	VLF bit value doesn't affect by writes 1.
Read	0	No supply voltage drops occurred
	1	Low voltage has been detected, so data loss might have occurred, and time information and other bits setup value might be wrong All registers should be initialized

3) VDET (Voltage Detection Flag) bit

This flag bit indicates the history of the voltage for temperature compensation circuit.
Its value changes from “0” to “1” indicates that the temperature compensation function has stopped operation due to a supply voltage drop. Once this flag bit's value is 1, its value is retained until a 0 is written to it.
After powering up from 0 V, make sure to set this bit's value to “1”. Please confirm table in 8.11. Backup and Recovery.

Table 21 VDET bit

VDET	Data	Description
Write	0	The VDET bit is cleared to 0 to prepare for the next low voltage detection
	1	VDET data remains even it was 0 or 1. To retain the data, please write 1
Read	0	Temperature compensation is normal
	1	Temperature compensation has been stopped

4) RESET bit

When highly precise synchronization of both time, timer is necessary, use RESET.

Table 22 RESET bit

RESET	Data	Description
Write	0	Writing 0 is invalid
	1	Writing 1 resets 16384 Hz ~2 Hz of 32.768 kHz counter (Refer to Figure 6)
Read	0	The read value of RESET is 0, always writes 0, it is invalid
	1	writes 1, it executes reset of count-down-chain from 32.768kHz

The detailed function of RESET.

For example.
S is start condition. P is stop condition.

[Write access to RESET-bit.]

S---Slave address(w)---ACK1---0Fh---ACK2---01h---ACK3---P.

RESET executes and it keeps between P from ACK3.
After P, RESET bit clears automatically.
reset area of circuit are the count-down-chain of 2 Hz from 16 kHz, are cleared.
As for next update timing of a Seconds counter from RESET.
That range is 1000 ms-30.5 μs from just 1000 ms.
RESET affects time update interruption, alarm, FOUT and timer.
But it doesn't affect 32 kHz output.

Note:
RESET is released by the reception of a START or RE-START condition before receiving a STOP condition.
The Single write access is recommended for precise RESET.
Unnecessary use of RESET will be the cause of delay error of time.

5) USEL (Update Interrupt Select) bit

This bit is used to define if the RTC should output a “second update” or “minute update” interrupt, allowing to synchronize external clocks with the time registers of the RTC.

Please refer to 8.6. Time Update Interrupt Function

6) TSEL0, 1 (Timer Select 0, 1) bits

The combination of these two bits is used to set the countdown period (source clock) for the wakeup timer interrupt function (four settings can be made).

Please refer to 8.3. Wakeup Timer Function

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7) FSEL0, 1 (FOUT frequency Select 0, 1) bits
The combination of these two bits is used to set the FOUT frequency.
Note: All frequencies are temperature compensated!

Table 23 FSEL bit

FSEL0,1	FSEL1 (bit 3)	FSEL0 (bit 2)	FOUT frequency
Write / Read	0	0	32.768 kHz Output Default
	0	1	1024 Hz Output
	1	0	1 Hz Output
	1	1	32.768 kHz Output

8) CSEL0, 1 (Compensation interval Select 0, 1) bits
The combination of these two bits is used to set the temperature compensation interval.
Please refer to 8.9. Temperature Compensation Function

9) AF (Alarm Flag) bit
If set to “0” beforehand, this flag bit's value changes from “0” to “1” when an alarm interrupt event has occurred. Once this flag bit's value is “1”, its value is retained until a “0” is written to it.
Please refer to 8.5. Alarm Interrupt Function.

10) TF (Timer Flag) bit
If set to “0” beforehand, this flag bit's value changes from “0” to “1” when a wakeup timer interrupt event has occurred. Once this flag bit's value is “1”, its value is retained until a “0” is written to it.
Please refer to 8.6. Wakeup Timer Interrupt Function.

11) UF (Update Flag) bit
If set to “0” beforehand, this flag bit's value changes from “0” to “1” when a time update interrupt event has occurred. Once this flag bit's value is “1”, its value is retained until a “0” is written to it.
Please refer to 8.7. Time Update Interrupt Function.

12) AIE, TIE, UIE (Alarm, Wakeup Timer, Update Interrupt Enable) bit
In case of Alarm or Wakeup Timer or Update occurs AIE, TIE, UIE bit controls /INT output.
When a “1” is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) .
When a “0” is written to this bit, no interrupt signal is generated.
Please refer to each function.

Table 24 AIE, TIE, UIE bit

Function	condition	Flag	/INT interrupt control
Alarm	Alarm time hit	AF	AIE
Wakeup Timer	Timer Count down to 0	TF	TIE
Update	Minute or Second update	UF	UIE

8.2.5. SOUT Control Register

Table 25 SOUT Control Register

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Read	Write
19	SOUT set1	SOE7	SOE6	SOE5	SOE4	SOE3	SOE2	SOE1	SOE0	√	√
1A	SOUT set0	DCE	DC	○	○	SRV	FS2	FS1	FS0	√	√

1) SOUT set1 register (19h)
By setting 69h =01101001b into SOUT set1 SOUT function becomes activated.
Other data than 69h makes SOUT function non active. Then SOUT becomes Hi-Z.

2) DCE bit ((Direct Control Enable), DC bit (Direct Control)
In case of DCE=1, DC bit Value is outputted at SOUT.
In case of DCE=0, register value Flag value is outputted at SOUT.

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Table 26 DCE, DC bit

DCE	DC	SOUT output
0	0	Flag value decided by SRV, FS2, FS1, FS0
0	1	
1	0	SOUT = Low, SRV bit is ignored
1	1	SOUT = High, SRV bit is ignored

3) SRV bit (SOUT Reverse)
SOUT output reverse.
Each Flag register is high active. In case of SRV = 1, IT becomes low active.

Table 27 SRV bit

SRV	SOUT Output
0	Flag Value
1	Inverse value of Flag Value

4) FS0,1,2 bit
Flag selection bits. SOUT set1 should be active.

Table 28 FS bit

DCE	FS2	FS1	FS0	Selected Flag	SOUT	
					SRV = 1	SRV = 0
0	0	0	0	TF	Inversion of TF	TF
0	0	0	1	AF	Inversion of AF	AF
0	0	1	0	UF	Inversion of UF	UF
0	1	1	1	EF	Inversion of EF	EF
0	1	0	0	VDET	Inversion of VDET	VDET
0	1	0	1	VLF	Inversion of VLF	VLF
0	Other value than above combination			----	Low	
1	----			----	DC	

Selected Flag register value by FS2,1, 0 is outputted at SOUT.
Output data is inversed by SRV bit.
Other FS2, 1, 0 combination makes SOUT low.
By this function RTC module inner status ex. VLF is outputted to external controller device.

8.2.6. Time Stamp Data Event Controller Register

Table 29 Time Stamp Data Event Control

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
10	Time stamp SEC	○	40	20	10	8	4	2	1	√	–
11	Time stamp MIN	○	40	20	10	8	4	2	1	√	–
12	Time stamp HOUR	○	○	20	10	8	4	2	1	√	–
13	Time stamp WEEK	○	6	5	4	3	2	1	0	√	–
14	Time stamp DAY	○	○	20	10	8	4	2	1	√	–
15	Time stamp MONTH	TSVLF	TSVDET	○	10	8	4	2	1	√	–
16	Time stamp YEAR	80	40	20	10	8	4	2	1	√	–
17	EVIN set	ECP	EHL	EPU	RCE	EIE	○	ET1	ET0	√	√
18	EVIN det	EF	○	○	○	EVMON	○	○	○	√	√

√ is available. – is not available.

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1) Time stamp SEC ~ YEAR
In case of trigger input detection from EVIN terminal, Clock and calendar data are recorded in Time stamp SEC ~ YEAR.

2) TSVLF, TSVDET bit (Time stamp VLF, Time stamp VDET)
In case of trigger input detection from EVIN terminal, VLF bit is recorded to TSVLF, VDET bit to TSVDET.

3) ECP bit (Event capture Enable)
ECP enables Time Stamp function.

Table 30 ECP bit

ECP	Data	Function
Write / Read	0	Time stamp is disabled
	1	Time stamp is enabled Time stamp data are overwritten by latest time stamp data

4) EHL bit (EVIN pin, High / Low detection select)
Selection bit of EVIN Voltage level.

Table 31 EHL bit

EHL	Data	Function
Write / Read	0	EVIN pin detects active Low level
	1	EVIN pin detects active High level

5) EPU bit (Enable Pull-up register)
EPU enables Pull-up-resistor of EVIN input terminal.

Table 32 EPU bit

EPU	Data	Function
Write / Read	0	Pull-up resistor is disabled
	1	Pull-up resistor is enabled

6) RCE bit (Repeat Capture Enable)
RCE enables repeated times stamp capture.

Table 33 RCE bit

RCE	Data	Function
Write / Read	0	After time stamp, ECP bit is cleared to 0 automatically and Time stamp is not executed, till ECP is set to 1 again
	1	Repeated Time stamp is enabled After a Time stamp execution, ECP is not cleared to 0 Time stamp is executed in every event detection and overwrites to Timestamp register

7) EF bit (Event trigger Flag)
History bit of EVIN trigger.

Table 34 EF bit

EF	Data	Function
Write	0	/INT Low output is cleared to Hi-Z
	1	The value of EF bit remains even EF = 0 or EF = 1 To keep the EF bit value, please write 1 to EF bit
Read	0	There is no EVIN detection history
	1	There is EVIN detection history

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8) ET1, ET0 bit (Event input debounce Time set)
Selection of debounce filtering cycle time.

Table 35 ET bit

ET0, 1	ET1	ET0	Filtering Cycle Time
Write / Read	0	0	No filtered * Default
	0	1	3.9 ms
	1	0	15.6 ms
	1	1	125 ms

*In case of no filtering, larger than 60 μs active input is detected.

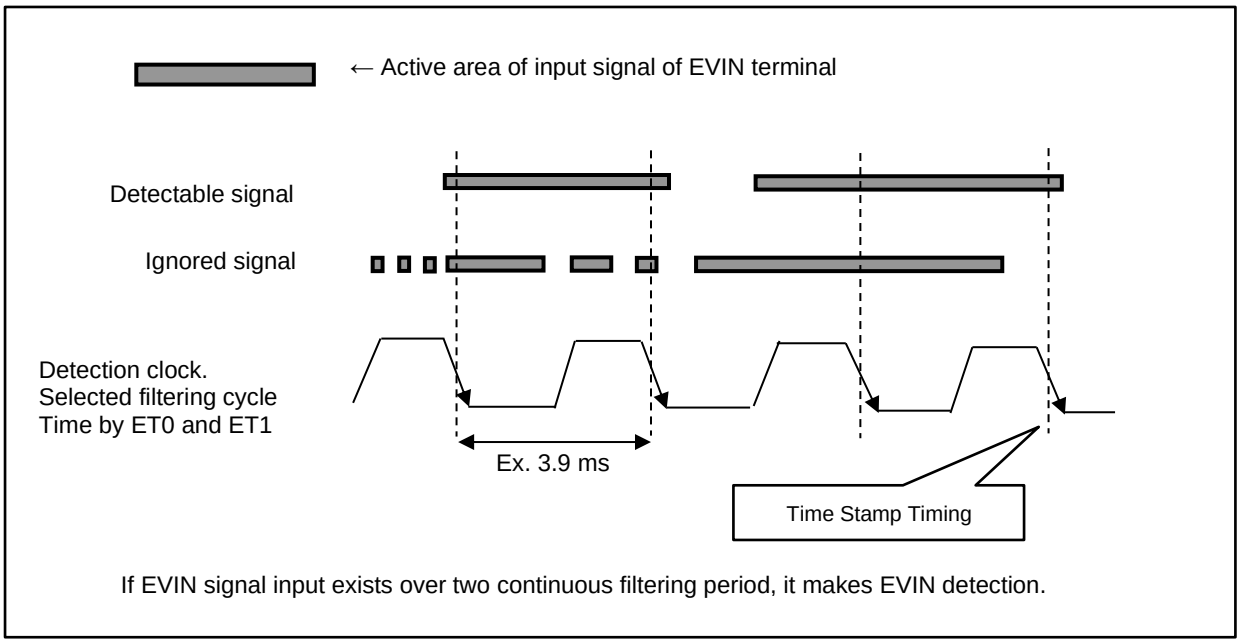


Figure 7 EVIN Debounce Function

9) EIE bit (EVIN Interrupt Enable)
/INT Interrupt Enable / Disable selection bit.

Table 36 EIE bit

EIE	Data	Description
Write / Read	0	1) In case of EVIN interrupt event, no interrupt signal is generated. /INT status remains Hi-Z 2) In case of EVIN interrupt event, /INT low signal is canceled. /INT status changes from low to Hi-Z Even the EIE bit value is "0" another interrupt event may change the /INT status to low (or may hold /INT = "L") *
	1	In case of EVIN interrupt event, interrupt signal is generated. /INT status changes from Hi-Z to low There is no auto reset function like Wakeup timer interrupt and Update interrupt function

*/INT low active signal is generated OR logic of Wakeup timer, Alarm, Update and EVIN interrupt.

10) EVMON (EVIN Monitor) bit
EVMON can read the EVIN input level.
Writing operation is ignored.

Table 37 EVMON bit

EVMON	Data	Function
Write / Read	0	The input level of EVIN is LOW
	1	The input level of EVIN is HIGH

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8.3. SOUT Function

8.3.1. Various Function of SOUT

1) The flag value selected by FS bit can be outputted at SOUT pin. See SOUT Function program ex.1
   By this function RTC inner self monitoring flag VDET, VLF are outputted at SOUT pin despite /INT pin.
   Even user system sleep period, RTC can monitor inner status.
2) By setting DC bit, user can control SOUT pin output. See SOUT Function program ex.2.
   By this function RTC SOUT pin can drive external device ex. LED.

8.3.2. SOUT Function Program ex.1

In case of V_{DD} voltage drop SOUT pin outputs Low level. Signal.
Timing chart SOUT Function program is described step 1~ 7.

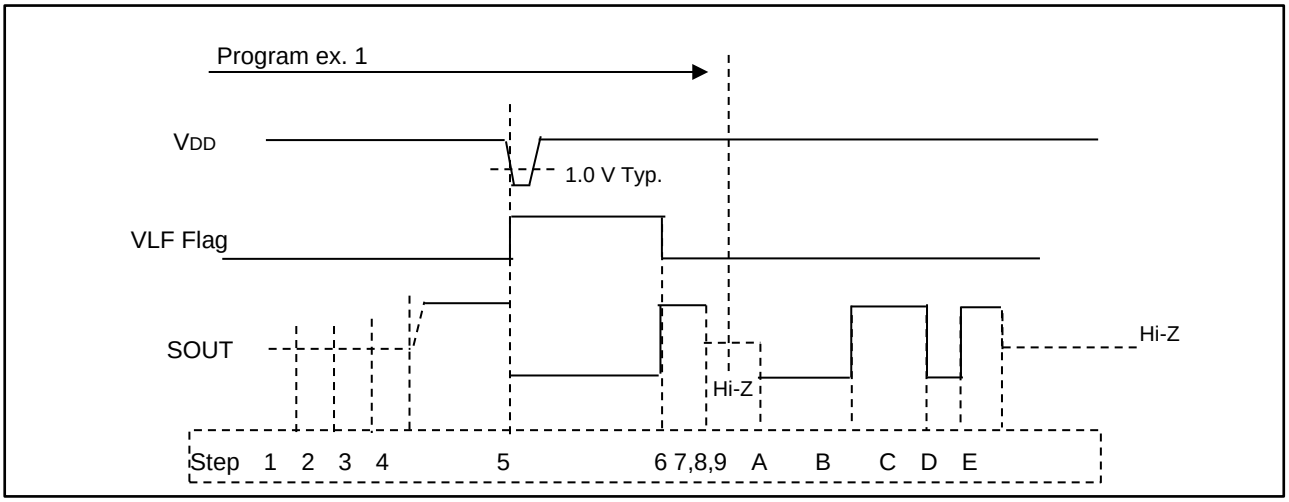


Figure 8 SOUT Function Program ex.1

STEP 1	operation		Disabling SOUT function							
	Command Example		WriteRA8804(19h,00h)							
	Target Address	19h	SOE7	SOE6	SOE5	SOE4	SOE3	SOE2	SOE1	SOE0
	Write Data	00h	0	0	0	0	0	0	0	0

STEP 2	operation		Clearing VLF bit. Retaining UF, TF, AF, VDET bit							
	Command Example		WriteRA8804(0Eh,39h)							
	Target Address	0Eh	0	0	UF	TF	AF	0	VLF	VDET
	Write Data	39h	0	0	1	1	1	0	0	1

STEP 3	operation		VLF is outputted to SOUT pin as low active							
	Command Example		WriteRA8804(1Ah,0Dh)							
	Target Address	1Ah	DCE	DC	0	0	SRV	FS2	FS1	FS0
	Write Data	0Dh	0	0	0	0	1	1	0	1

STEP 4	operation		Enabling SOUT function							
	Command Example		WriteRA8804(19h,69h)							
	Target Address	19h	SOE7	SOE6	SOE5	SOE4	SOE3	SOE2	SOE1	SOE0
	Write Data	69h	0	1	1	0	1	0	0	1

STEP 5	Low level is outputted at SOUT pin when V_{DD} low is detected

STEP 6	operation		SOUT pin is switched to High level when VLF is cleared to 0							
	Command Example		WriteRA8804(0Eh,39h)							
	Target Address	0Eh	0	0	UF	TF	AF	0	VLF	VDET
	Write Data	39h	0	0	1	1	1	0	0	1

STEP 7	operation		Disabling SOUT function							
	Command Example		WriteRA8804(19h,00h)							
	Target Address	19h	SOE7	SOE6	SOE5	SOE4	SOE3	SOE2	SOE1	SOE0
	Write Data	00h	0	0	0	0	0	0	0	0

8.3.3. SOUT Function Program ex.2

By setting DC bit, SOUT pin can control status like a general OUT put port.

Timing chart SOUT Function program are described step 9 ~ E.

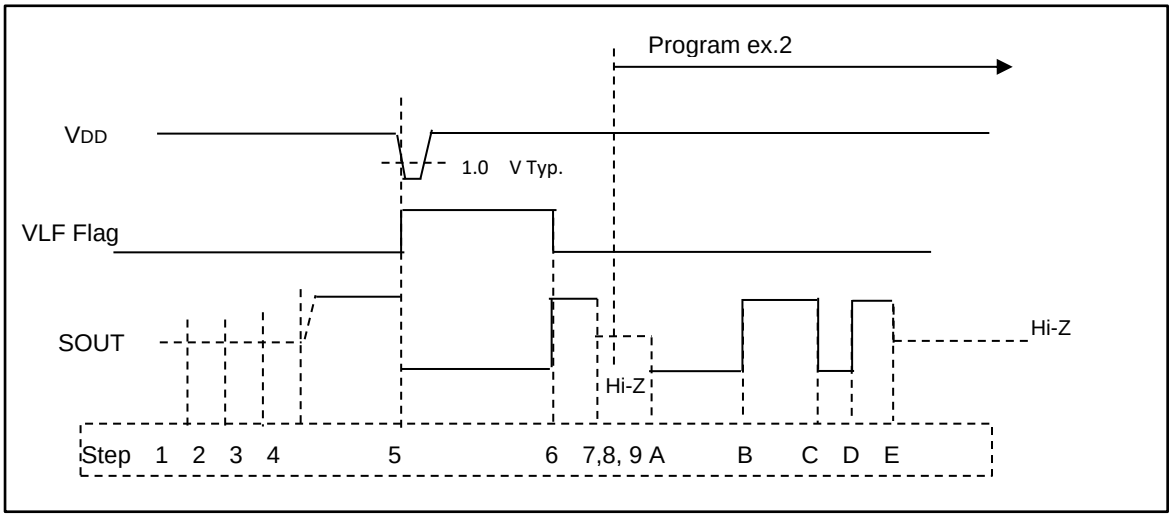


Figure 9 SOUT function Program ex.2

STEP 8	operation		Disabling SOUT function							
	Command Example		WriteRA8804(19h,00h)							
	Target Address	19h	SOE7	SOE6	SOE5	SOE4	SOE3	SOE2	SOE1	SOE0
	Write Data	00h	0	0	0	0	0	0	0	0

STEP 9	operation		Enabling SOUT control by setting DCE bit to 1							
	Command Example		WriteRA8804(1Ah,80h)							
	Target Address	1Ah	DCE	DC	0	0	SRV	FS2	FS1	FS0
	Write Data	80h	1	0	0	0	0	0	0	0

STEP A	operation		Enabling SOUT function							
	Command Example		WriteRA8804(19h,69h)							
	Target Address	19h	SOE7	SOE6	SOE5	SOE4	SOE3	SOE2	SOE1	SOE0
	Write Data	69h	0	1	1	0	1	0	0	1

STEP B	operation		Outputting High level at SOUT pin							
	Command Example		WriteRA8804(1Ah,C0h)							
	Target Address	1Ah	DCE	DC	0	0	SRV	FS2	FS1	FS0
	Write Data	C0h	1	1	0	0	0	0	0	0

STEP C	operation		Outputting High level at SOUT pin							
	Command Example		WriteRA8804(1Ah,80h)							
	Target Address	1Ah	DCE	DC	0	0	SRV	FS2	FS1	FS0
	Write Data	80h	1	0	0	0	0	0	0	0

STEP D	operation		Outputting High level at SOUT pin							
	Command Example		WriteRA8804(1Ah,C0h)							
	Target Address	1Ah	DCE	DC	0	0	SRV	FS2	FS1	FS0
	Write Data	C0h	1	1	0	0	0	0	0	0

STEP E	operation		Disabling SOUT function							
	Command Example		WriteRA8804(19h,00h)							
	Target Address	19h	SOE7	SOE6	SOE5	SOE4	SOE3	SOE2	SOE1	SOE0
	Write Data	00h	0	0	0	0	0	0	0	0

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8.4. EVIN Interrupt and Time Stamp Function

At the EVIN input timing, the time data, VDET and VLF date are stored to registers.
An application ex. User can obtain the timing information ex. System error timing and analyses.

8.4.1. Time Stamp Program ex.

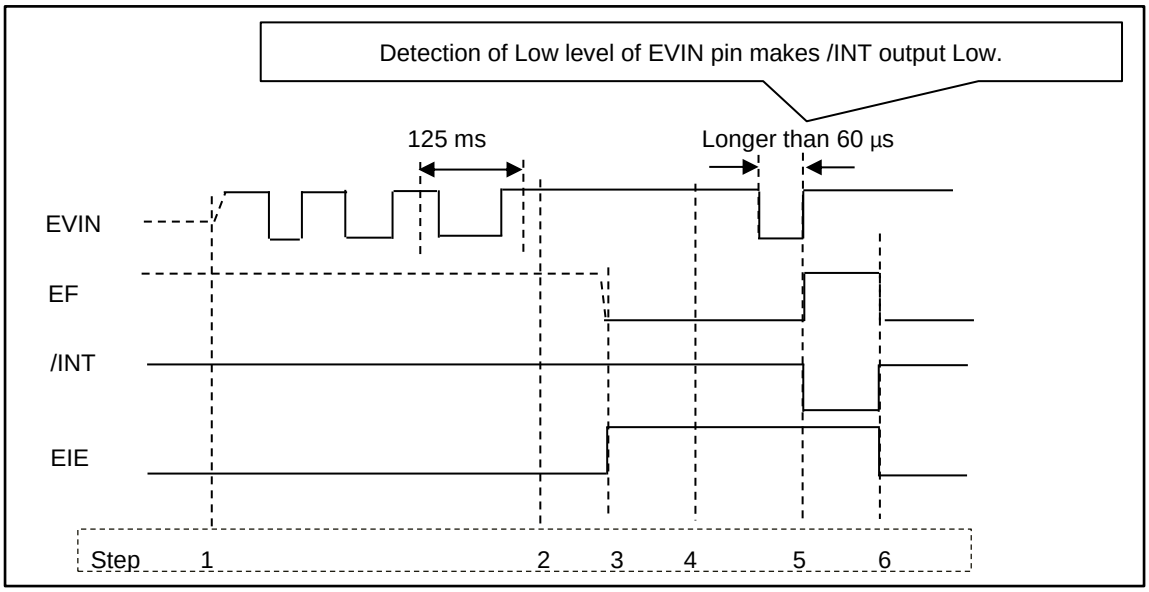


Figure 10 Time Stamp Program ex.

STEP1	operation		EVIN setting after disabling EVIN interrupt							
	Command Example		WriteRA8804(17h,23h)							
	Target Address	17h	ECP	EHL	EPU	RCE	EIE	0	ET1	ET0
	Write Data	23h	0	0	1	0	0	0	1	1

STEP2	operation		Disabling other interrupts							
	Command Example		WriteRA8804(0Fh,40h)							
	Target Address	0Fh	CSEL1	CSEL0	UIE	TIE	AIE	0	0	Reset
	Write Data	40h	0	1	0	0	0	0	0	

STEP3	operation		Clearing EF bit							
	Command Example		WriteRA8804(18h,00h)							
	Target Address	18h	EF	0	0	0	EVMON	0	0	0
	Write Data	00h	0	0	0	0	0	0	0	0

STEP4	operation		Enabling EVIN interrupt							
	Command Example		WriteRA8804(17h,A8h)							
	Target Address	17h	ECP	EHL	EPU	RCE	EIE	0	ET1	ET0
	Write Data	A8h	1	0	1	0	1	0	0	0

STEP5	Time data, VLF, VDET data is stored to registers when longer than 60 us signal is inputted to EVIN

STEP6	INIT returns to Hi-Z when either EF or EIE is cleared to 0

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8.4.2. Timing Chart of EVIN Time Stamping

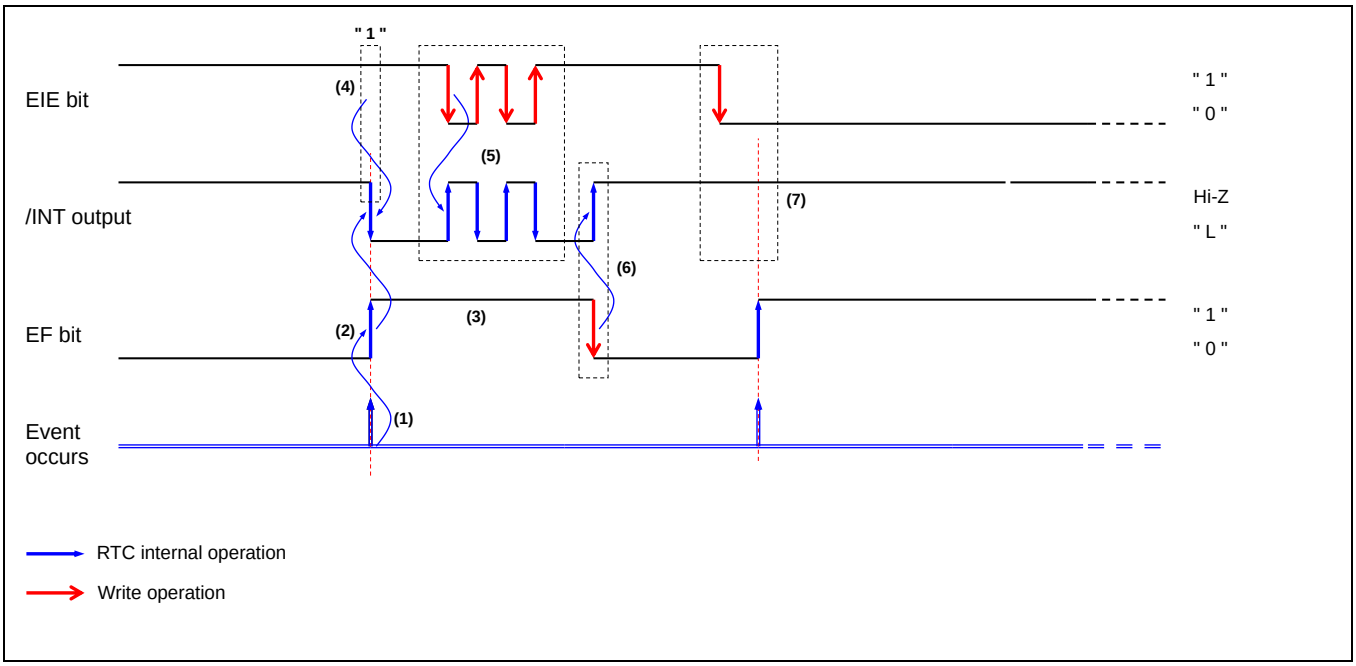


Figure 11 EVIN Timing Chart

(1) An EVIN interrupt event occurred.
(2) At the same time, EF bit value becomes “1”.

(3) When the EF bit = “1”, its value is retained until it is cleared to zero.

(4) If EIE = “1” when an EVIN interrupt occurs, the /INT pin output goes low.
∗ When an EVIN interrupt event occurs, /INT pin output goes low, and this status is then held until it is cleared via the EF bit or EIE bit.

(5) If the EIE value is changed from “1” to “0” while /INT is low, the /INT status immediately changes from low to Hi-Z. After the EVIN interrupt occurs and during the EF bit value is 1, the /INT status can be controlled via the EIE bit.

(6) If the EF bit value is changed from “1” to “0” while /INT is low, the /INT status immediately changes from low to Hi-Z.

(7) If the EIE bit value is “0” when an EVIN interrupt occurs, the /INT pin status remains Hi-Z.

8.4.3. /INT pin Operation when an Interrupt Occurs.

1) How to identify events when the interrupt output occurs
/INT output pin is common output terminal of interrupt events of four types Wakeup timer, alarm, time update and EVIN interrupt.
When an interrupt occurs, please read the TF, AF, UF and EF flag to confirm which types of events occurred.
2) Processing method in case of no using /INT output.
1. Please keep /INT pin open.
2. Please set “0” to TIE, AIE, UIE and EIE bits and do poling TF, AF, UF and EF.

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8.5. Alarm Interrupt Function

8.5.1. Alarm Interrupt Function

The alarm interrupt function generates interrupt events at the matching time of alarm day, hour, and minute settings.

When an interrupt event occurs, the AF bit value is set to “1” and the /INT pin goes to low level to indicate that an event has occurred.

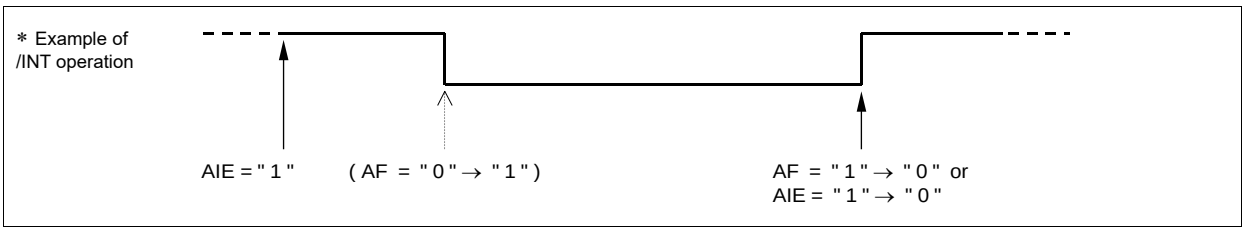


Figure 12 Alarm Function

8.5.2. Alarm Interrupt Function Register

Table 38 Alarm Interrupt Function Register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
08	MIN Alarm	**AE**	40	20	10	8	4	2	1
09	HOUR Alarm	**AE**	•	20	10	8	4	2	1
0A	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
0D	Control1	TEST	**WADA**	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E	Flag Register	O	O	UF	TF	**AF**	O	VLF	VDET
0F	Control 2	CSEL1	CSEL0	UIE	TIE	**AIE**	O	O	RESET

∗1) o indicates write-protected bits. A zero is always read from these bits.

∗2) Bits marked with • are RAM bits that can contain any value and are read/write-accessible.

∗ Before entering settings for operations, it is recommended that writing “0” to the AIE bit to prevent unexpected hardware interrupts.

∗ When the RESET bit value is “1” alarm interrupt events do not occur.

∗ When the alarm interrupt function is not used, the Alarm registers (Reg – 08h to 0Ah) can be used as a RAM register. In such cases, be sure to write “0” to the AIE bit.

∗ When the AIE bit value is “1” and the Alarm registers (Reg – 08h to 0Ah) is being used as a RAM register, /INT may be changed to low level unintentionally.

1) Alarm registers

The minute, hour, day and date when an alarm interrupt event is set using this register and the WADA bit.

In the WEEK alarm /Day alarm register (Reg – 0Ah), the setting selected via the WADA bit determines whether WEEK alarm data or DAY alarm data will be set. If WEEK has been selected via the WADA bit, multiple days can be set (such as Monday, Wednesday, Friday, Saturday).

- Unwanted alarm term is decided by setting respective AE bit =”1”. If AE is set to “1”, this alarm term becomes inactive.
  Ex. WEEK Alarm / DAY Alarm (0Ah) = 80h (AE=”1”) hour, minute, second alarm active week, day alarm inactive
- Setting all AE bit “1” makes every one second alarm exceptionally. The result is reflected in AF bit.
- Alarm event does not occur even user set alarm time to current time. Coming next time matching (alarm time = current time) can occur the event.

2) WADA (Week Alarm /Day Alarm) bit

The alarm interrupt function uses either” Day” or “Week” as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

Table 39 WADA bit

WADA	Data	Description
Write / Read	0	Sets WEEK as target of alarm function Register 0Ah is compared with register 03h (DAY setting is ignored)
	1	Sets DAY as target of alarm function Register 0Ah is compared with register 04h (WEEK setting is ignored)

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3) AF (Alarm Flag) bit

When this flag bit value is already set to “0”, occurrence of an alarm interrupt event changes it to “1”. When this flag bit value is “1”, its value is retained until a “0” is written to it.

Table 40 AF bit AF bit

AF	Data	Description
Write	0	The AF bit is cleared to zero to prepare for the next status detection * Clearing this bit to zero enables /INT low output to be canceled (/INT remains Hi-Z) when an alarm interrupt event has occurred
	1	AF bit is retained even AF is 0 or 1. To retain AF bit, user can write 1.
Read	0	Alarm interrupt events are not detected.
	1	Alarm interrupt events are detected. (Result is retained until this bit is cleared to 0)

4) AIE (Alarm Interrupt Enable) bit

When an alarm interrupt event occurs (when the AF bit value changes from “0” to “1”), this bit's value specifies whether an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

Table 41 AIE bit

AIE	Data	Description
Write / Read	0	1) When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z). 2) When an alarm interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z). Even when the AIE bit value is “0” another interrupt event may change the /INT status to low (or may hold /INT = ”L”)
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). When an alarm interrupt event occurs, low-level output from the /INT pin occurs only when the AIE bit value is “1”. This value is retained (not automatically cleared) until the AF bit is cleared to zero

8.5.3. Examples of Alarm Settings

1) Example of alarm settings when Day has been specified (and WADA bit = 0)

Table 42 Alarm Setting ex.1

Day is specified WADA bit = 0	Reg – A								Reg - 9	Reg - 8
	bit 7 AE	bit 6 S	bit 5 F	bit 4 T	bit 3 W	bit 2 T	bit 1 M	bit 0 S	HOUR Alarm	MIN Alarm
Monday through Friday, at 7:00 AM ∗ Minute value is ignored	0	0	1	1	1	1	1	0	07h	AE = 1
Every Saturday and Sunday, for 30 minutes each hour ∗ Hour value is ignored	0	1	0	0	0	0	0	1	AE = 1	30h
Every day, at 6:59 AM	0 1	1 X	1 X	1 X	1 X	1 X	1 X	1 X	18h	59h

X: Don't care

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2) Example of Alarm Settings when Day has been Specified (and WADA bit = ”1”)

Table 43 Alarm Setting ex.2

Day is specified WADA bit = 1	Reg - A								Reg - 9	Reg - 8
	bit 7 AE	bit 6 •	bit 5 20	bit 4 10	bit 3 08	bit 2 04	bit 1 02	bit 0 01	HOUR Alarm	MIN Alarm
First of each month, at 7:00 AM ∗ Minute value is ignored	0	0	0	0	0	0	0	1	0 h	AE = 1
15th of each month, for 30 minutes each hour ∗ Hour value is ignored	0	0	0	1	0	1	0	1	AE = 1	30h
Every day, at 6:59 PM	1	X	X	X	X	X	X	X	18h	59h

X: Don't care

8.5.4. Alarm Interrupt Timing Chart

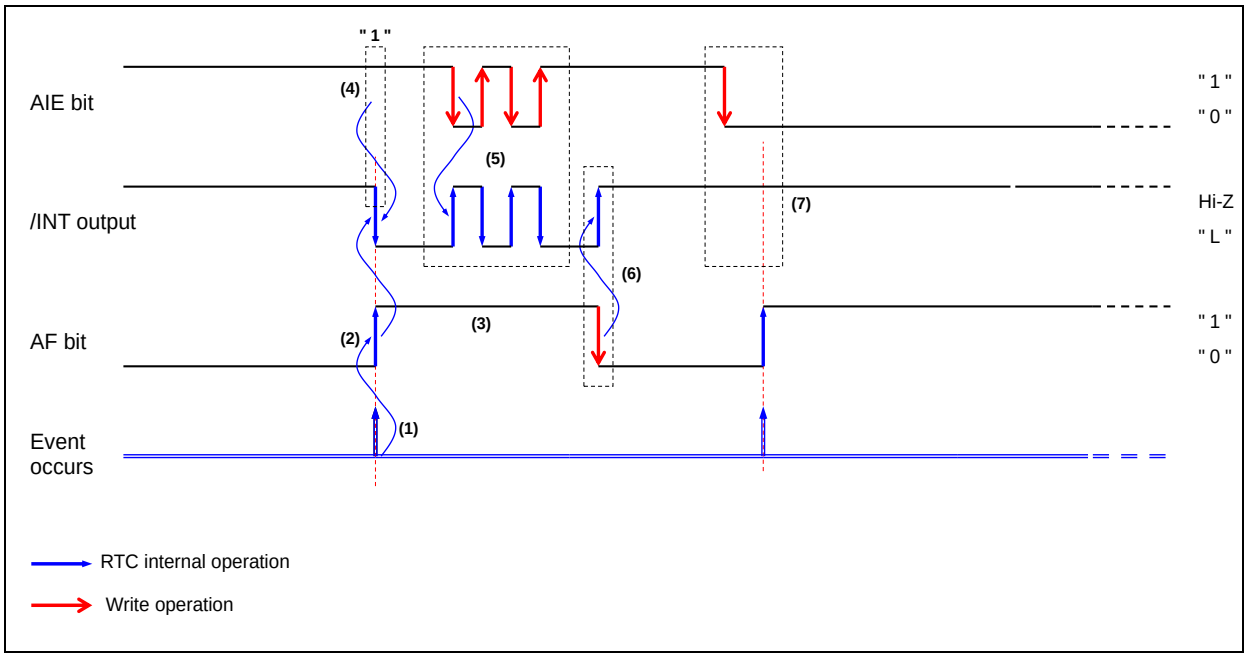


Figure 13 Alarm Timing Chart

(1) The minute, hour, day and date, when an alarm interrupt event is supposed to occur has to be set in advance, along with the WADA bit (Note) Even if the current date/time is used as the setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).

(2) When a time update interrupt event occurs, the AF bit values becomes “1”.

(3) When the AF bit = 1, its value is retained until it is cleared to zero.

(4) If AIE = 1 when an alarm interrupt occurs, the /INT pin output goes low.
∗ When an alarm interrupt event occurs, /INT pin output goes low, and this status is then held until it is cleared via the AF bit or AIE bit.

(5) If the AIE value is changed from “1” to “0” while /INT is low, the /INT status immediately changes from low to Hi-Z. After the alarm interrupt occurs and before the AF bit value is cleared to zero, the /INT status can be controlled via the AIE bit.

(6) If the AF bit value is changed from “1” to “0” while /INT is low, the /INT status immediately changes from low to Hi-Z.

(7) When the AIE bit value is “0”, and an alarm interrupt occurs, the /INT pin stay Hi-Z.

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8.5.5. /INT pin Operation when an Interrupt Occurs.

1) How to identify events when the interrupt output occurs
/INT output pin is common output terminal of interrupt events of four types Wakeup timer, alarm, time update and EVIN interrupt.
When an interrupt occurs, please read the TF, AF, UF and EF flag to confirm which types of events occurred.

2) Processing method in case of no using /INT output.
Please keep /INT pin open.
Please set “0” to TIE, AIE, UIE and EIE bits and do poling TF, AF, UF and EF.

8.6. Wakeup Timer Interrupt Function

8.6.1. Wakeup Timer Interrupt Function

The wakeup timer interrupt generation function generates an interrupt event periodically at any wakeup set between 244.14 μs and 32 years.
When an interrupt event is generated, the /INT pin goes to low level and “1” is set to the TF bit to report that an event has occurred. However, when a wakeup timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is “1”. Time of TRTN2 after the interrupt occurs, the /INT status is automatically cleared. /INT status changes from low-level to Hi-Z.

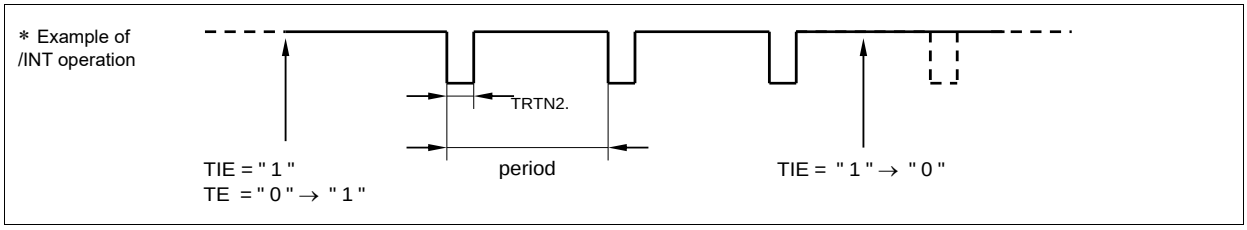


Figure 14 Wakeup Timer Function

8.6.2. Wakeup Timer Interruption Registers.

The wakeup timer interrupt generation function generates an interrupt event periodically at any wakeup set between 244.14 s and 16777215 minutes.

Table 44 Wakeup Timer Register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
0B	Timer Counter 0	128	64	32	16	8	4	2	1	√	√
0C	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256	√	√
0D	Control1	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	√	√
0E	Flag Register	O	O	UF	TF	AF	O	VLF	VDET	√	Clear only
0F	Control2	CSEL1	CSEL0	UIE	TIE	AIE	O	O	RESET	√	√
1B	Timer set	TSTP	TRES	O	O	O	O	O	O	√	√
1C	Timer 0	128	64	32	16	8	4	2	1	√	-
1D	Timer 1	32768	16384	8192	4096	2048	1024	512	256	√	-
1E	Timer 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	√	-
1F	Timer Counter 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536	√	√

- Timer Counter 0, 1, 2 are preset value of timer.
- Timer 0, 1, 2 are current count value of timer.
- Before entering settings for operations, it is recommended writing a “0” to the TE and TIE bits to prevent unexpected hardware interrupts.
- When the RESET bit value is “1” the time update interrupt function does not operate.
- When the wakeup timer interrupt function is not using, the wakeup timer counter0, 1, 2 (0Bh, 0Ch, 1Fh), these can be used as a RAM register. In such cases, stop the wakeup timer function by writing “0” to the TE and TIE bits.
- When writes 00h to all timer counter, Timer countdown are stop, and new Timer interruption are inhibited.

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1) TSEL0, 1bits (Timer Select 0, 1)

The combination of these two bits is used to set the countdown period source clock for the wakeup timer interrupt function (four settings can be made).

Table 45 TESL bit

TSEL0,1	TSEL1 (bit 1)	TSEL0 (bit 0)	Source clock / cycle time	Auto reset time tRTN2
Write / Read	0	0	4096 Hz / Once per 244.14 μs	122 μs
	0	1	64 Hz / Once per 15.625 ms	7.813 ms
	1	0	Default 1Hz	7.813 ms
	1	1	1/60 Hz "Minute" update / Once per minute	7.813 ms

1. tRTN2 is different with a source clock in automatic release time. TF is not cleared automatically.
2. Source clock of 1 Hz does not synchronize to update of a Seconds counter. It is a 1 Hz clock for Wakeup Timer.
3. Source clock 1/60 Hz synchronize in update of a Minutes counter.
4. A preset value, it is loaded with the first source clock of a timer counter after having set TE.
5. Therefore, two periods of source clocks are needed at the maximum till the first countdown starts after TE="1".

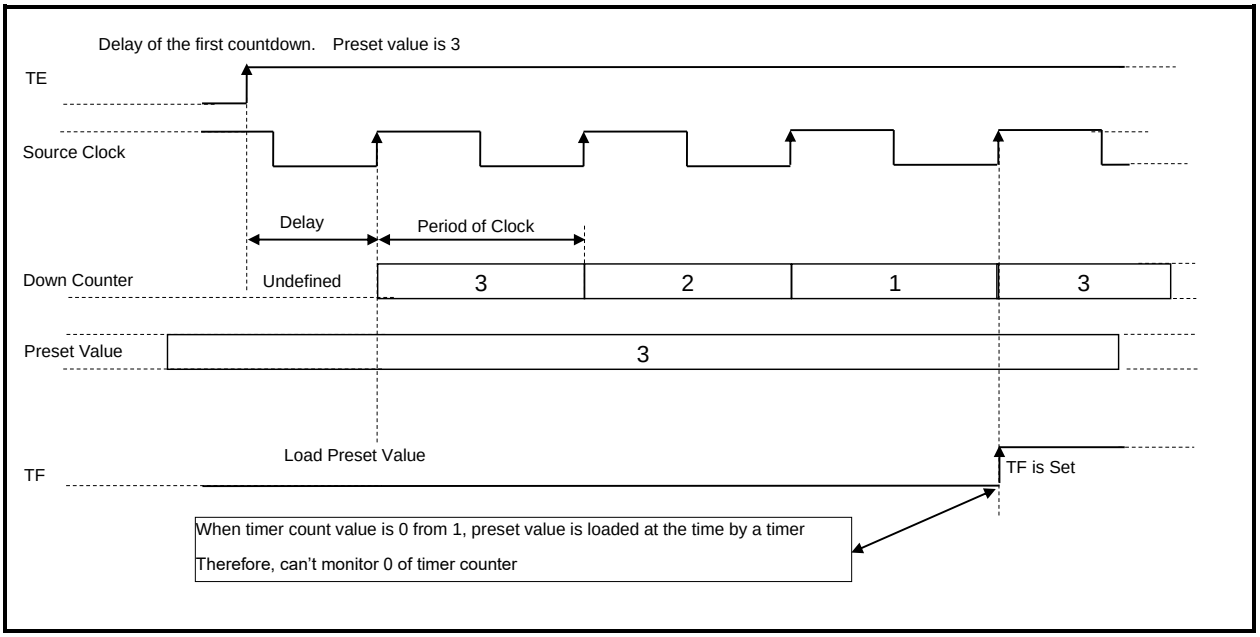


Figure 15 Wakeup Timer Count Down Timing Chart

2) TSTP (Timer STOP) bit

This bit controls the temporarily stopped of Timer Counter.

Table 46 TSTP bit

TSTP	Data	Description
Write / Read	1	The timer count down is stopped. The counter data is not cleared.
	0	The timer Count down is continued.

3) TRES (Timer Reset) bit

This bit can be employed like Watch Dog Timer function.

Table 47 TRES bit

TRES	Data	Description
Write / Read	1	Preset value is loaded to all Timer Counters
	0	The Timer Counter is not affected

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4) TE (Timer Enable) bit
This bit controls the start/stop setting for the wakeup timer interrupt function.

Table 48 TE bit

TE	Data	Description
Write / Read	0	Preset value loaded to all Timer counter, and count-down stops
	1	Starts wakeup timer countdown * The countdown that starts when the TE bit value changes from 0 to 1 always begins from the preset value

5) TF (Timer Flag) bit
If set to 0 beforehand, this flag bit's value changes from “0” to “1” when a wakeup timer interrupt event has occurred. Once this flag bit's value is “1”, its value is retained until a “0” is written to it.

Table 49 TF bit

TF	Data	Description
Write	0	The TF bit is cleared to zero to prepare for the next status detection * Clearing this bit to zero does not enable the /INT low output status to be cleared (to Hi-Z).
	1	Invalid (writing a 1 will be ignored)!
Read	0	Wakeup timer interrupt events are not detected.
	1	Wakeup timer interrupt events are detected. (Result is retained until this bit is cleared to zero.)

6) TIE (Timer Interrupt Enable) bit
When a wakeup timer interrupt event occurs (when the TF bit value changes from “0” to “1”), this bit's value specifies whether an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

Table 50 TIE bit

TIE	Data	Description
Write / Read	0	1) When a wakeup timer interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z) 2) When a wakeup timer interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z) * Even when the TIE bit value is “0” another interrupt event may change the /INT status to low (or may hold /INT = L)
	1	When a wakeup timer interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low) * When a wakeup timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is 1. Earliest 7.813 ms the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi-Z).

8.6.3. Wakeup Timer Start Timing

Counting down of the wakeup timer value starts at the rising edge of the SCL signal that occurs when the TE value is changed from 0 to “1” (after bit “0” is transferred).

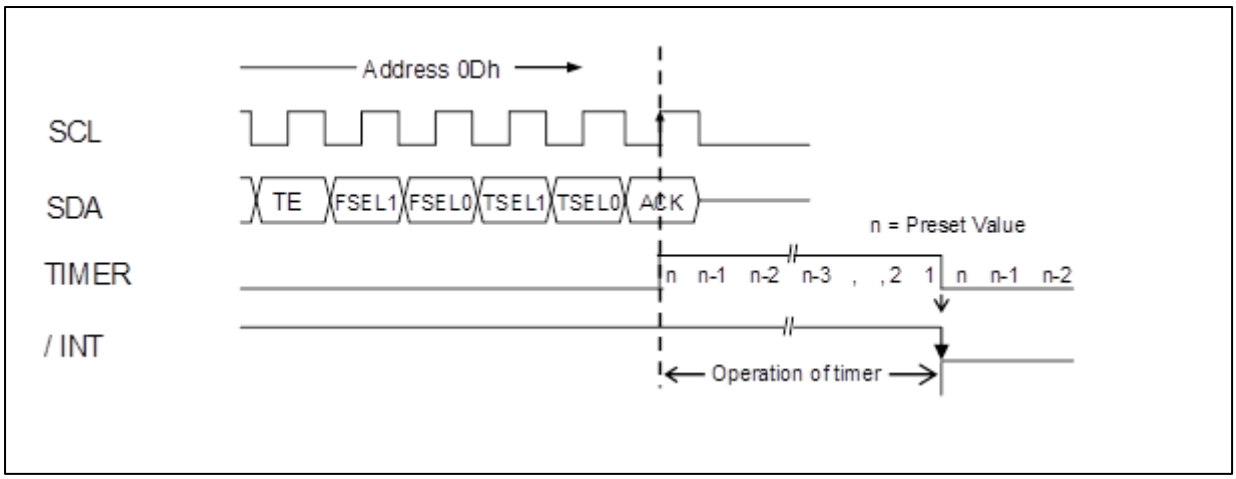


Figure 16 Wakeup Timer Start Sequence

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8.6.4. Wakeup Timer Interrupt Interval (example)

Table 51 Wakeup Timer Interrupt Interval

Preset Value	Source clock			
	4096 Hz TSEL1,0 = 0,0	64 Hz TSEL1,0 = 0,1	"Second" update TSEL1,0 = 1,0	"Minute" update TSEL1,0 = 1,1
0	–	–	–	–
1	244.14 μs	15.625 ms	1 s	1 min
2	488.28 μs	31.25 ms	2 s	2 min
⋮	⋮	⋮	⋮	⋮
41	10.010 ms	640.63 ms	41 s	41 min
82	20.020 ms	1.281 s	82 s	82 min
128	31.250 ms	2.000 s	128 s	128 min
192	46.875 ms	3.000 s	192 s	192 min
205	50.049 ms	3.203 s	205 s	205 min
320	78.125 ms	5.000 s	320 s	320 min
410	100.10 ms	6.406 s	410 s	410 min
640	156.25 ms	10.000 s	640 s	640 min
820	200.20 ms	12.813 s	820 s	820 min
1229	300.05 ms	19.203 s	1229 s	1229 min
1280	312.50 ms	20.000 s	1280 s	1280 min
1920	468.75 ms	30.000 s	1920 s	1920 min
2048	500.00 ms	32.000 s	2048 s	2048 min
2560	625.00 ms	40.000 s	2560 s	2560 min
3200	0.7813 s	50.000 s	3200 s	3200 min
3840	0.9375 s	60.000 s	3840 s	3840 min
4095	0.9998 s	63.984 s	4095 s	4095 min
⋮	⋮	⋮	⋮	⋮
16777215	4096 s	3 days,49 min.4 s	194 days	32 years

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8.6.5. Wakeup Timer Interrupt Timing Chart

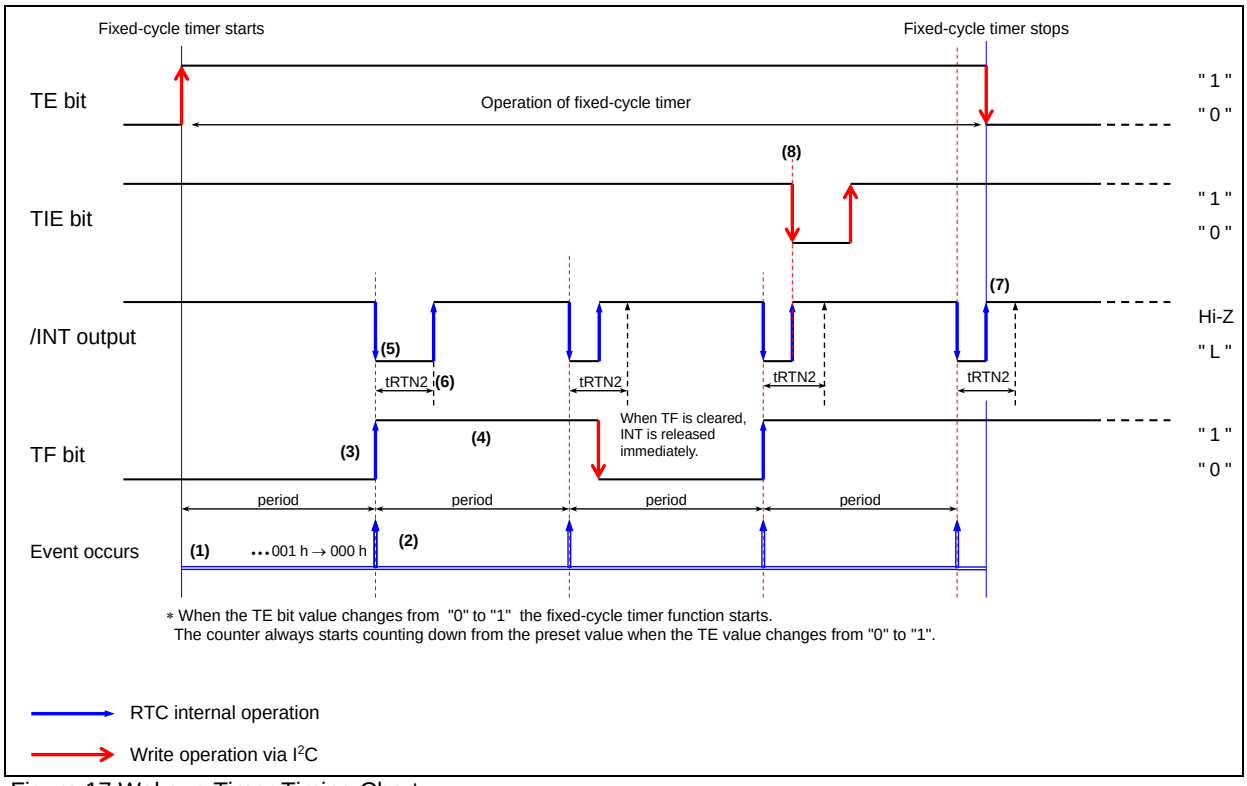


Figure 17 Wakeup Timer Timing Chart

(1) When a “1” is written to the TE bit, the wakeup timer is loaded preset value, at first source clock.

(2) A wakeup timer interrupt event starts a countdown based on the countdown period (source clock). When the count value changes from 001 to 000, an interrupt event occurs. After the interrupt event occurs, the counter automatically reloads the preset value and again starts to count down. (Repeated interruption)

(2) When a wakeup timer interrupt event occurs, TF is set to "1".

(3) When the TF bit = 1 its value is retained until it is cleared to zero.

(4) If the TIE bit = 1 when a wakeup timer interrupt occurs, /INT pin output goes low.

(6) Output from the /INT pin remains low during the tRTN2 period following each event, after which it is automatically released to Hi-Z status.
When the next interrupt event occurs, /INT is asserted to Low again.

(7) When a 0 is written to the TE bit, the wakeup timer function is stopped and the /INT pin is set to Hi-Z status and the wakeup timer function is stopped.

(8) When /INT is low, the /INT pin status changes from Low to Hi-Z as soon as the TIE bit value changes from 1 to 0.

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8.7. Time Update Interrupt Function

8.7.1. Time Update Interrupt Function

The time update interrupt function generates interrupt events at one-second or one-minute intervals, according to the timing of the internal clock.

When an interrupt event occurs, the UF bit value set to 1, and the /INT pin is asserted to Low level to indicate that an event has occurred. This LOW output is automatically released after tRTN1.

8.7.2. Related Registers for Time Update Interrupt Functions

Table 52 Update Interrupt Function Register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0D	Control 1	TEST	WADA	**USEL**	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E	Flag Register	○	○	**UF**	TF	AF	○	VLF	VDET
0F	Control 2	CSEL1	CSEL0	**UIE**	TIE	AIE	○	○	RESET

∗) o indicates write-protected bits. A zero is always read from these bits.

∗ Before entering settings for operations, we recommend writing a “0” to the UIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the RESET bit value is 1 time update interrupt events do not occur.

∗ Although the time update interrupt function cannot be fully stopped, if “0” is written to the UIE bit, the time update interrupt function can be prevented from changing the /INT pin status to low.

1) USEL (Update Interrupt Select) bit

This bit is used to select "second" update or "minute" update as the timing for generation of time update interrupt events.

Table 53 USEL bit

USEL	Data	update interrupts	Auto release time tRTN1
Write / Read	0	second update ∗ Default	500 ms
	1	minute update	15.625 ms

2) UF (Update Flag) bit

Once it has been set to "0", this flag bit value changes from "0" to "1" when a time update interrupt event occurs. When this flag bit = "1" its value is retained until a "0" is written to it.

Table 54 UF bit

UF	Data	Description
Write	0	The UF bit is cleared to zero to prepare for the next detection. In time update interruption, INT is released immediately.
	1	Invalid (writing a 1 will be ignored)!
Read	0	Time update interrupt events are not detected
	1	Time update interrupt events are detected (The result is retained until UF is cleared to zero)

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3) UIE (Update Interrupt Enable) bit
UIE selects whether to enables an this interrupt signal to /INT pin, or disable it.

Table 55 UIE bit

UIE	Data	Description
Write / Read	0	1) Does not generate an interrupt signal when a time update interrupt event occurs. 2) Cancels interrupt signal triggered by time update interrupt event. /INT is released from low to Hi-Z. Even when the UIE bit value is “0” another interrupt event may change the /INT status to low or may hold /INT = L.
	1	When a time update interrupt event occurs, an interrupt signal is generated /INT status changes from Hi-Z to Low. After tRTN1, the /INT status is automatically released.

8.7.3. Time Update Interrupt Function Timing Chart

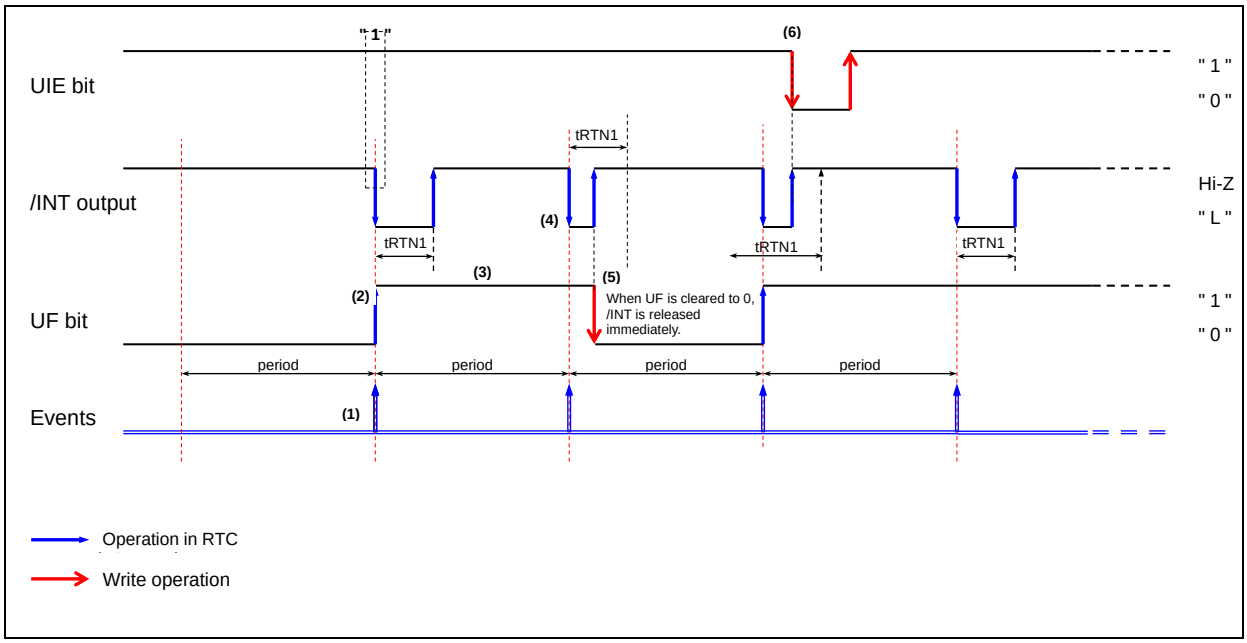


Figure 18 Update Interrupt Timing Chart

(1) A time update interrupt event occurs when the internal clock's value matches either the Seconds updates or the Minutes updates. The USEL specification determines whether it is the Seconds updates or the Minutes updates that must be matched.

(2) When a time update interrupt event occurs, the UF is set to “1”.

(3) When the UF bit value is “1” its value is retained until it is cleared to zero.

(4) When a time update interrupt occurs, /INT pin output is low if UIE = ”1”.

(5) Each time an event occurs, /INT pin output is low only up to the tRTN1 after which it is automatically cleared to Hi-Z. But, When UF is cleared to 0, /INT is released immediately.

(6) When /INT = Low, the /INT pin status changes from Low to Hi-Z as soon as the UIE bit value changes from “1” to ”0”.

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8.8. Temperature Compensation Function

8.8.1. Temperature Compensation Function

During the production process of the RTC, we are programming the individual characteristics of the built-in crystal into the non-volatile memory of the RTC. The build-in temperature sensor measures the actual temperature of the module and compensates the oscillation frequency of the crystal oscillator using the stored compensation data. This way not only the time information is temperature compensated, but as well the FOUT signal, even when outputting 32.768 kHz. This function works in the supply voltage range VTEM.

8.8.2. Related Registers for Temperature Compensation Function

Table 56 Temperature Compensation Register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0F	Control 2	**CSEL1**	**CSEL0**	UIE	TIE	AIE	O	O	RESET

1) CSEL1, CSEL0 (Compensation Interval Select 1, 0) bit
This bit sets an interval of a temperature compensation operation.
Current consumption decreases when increasing the Compensation Interval by means CSEL1, 0. CSEL1, 0 is set at the time of initial power-up to (“0”, “1”).

Table 57 CSEL bit

CSEL0,1	CSEL1	CSEL0	Compensation interval
Write / Read	0	0	0.5 s
	0	1	2.0 s Default
	1	0	10 s
	1	1	30 s

Even if the power supply voltage falls below V_{TEM} and a VDET bit is set to “1”, the temperature compensation operation is performed again if the supply voltage raises above V_{TEM}.

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8.9. Reading / Writing Data via the I²C-Bus Interface

8.9.1. Overview of I²C-Bus

The I²C-Bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data transfer signals, acknowledge signals, and so on.

Both the SCL and SDA signals are held at high level whenever communications are not being performed.
The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level.

During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is output while the SCL line is at high level.
The I²C-Bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse.

8.9.2. System Configuration

All ports connected to the I²C-Bus must be either open drain or open collector ports to enable “AND-connections” to multiple devices.
SCL and SDA are both connected to the VDD line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).

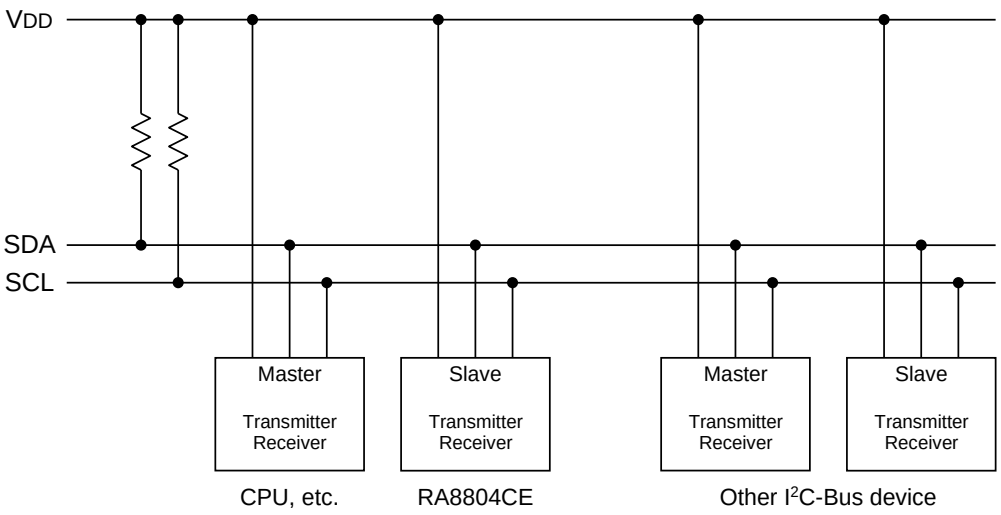


Figure 19 I²C-Bus Connection

Any device that controls the data transmission and data reception is defined as a “Master”.
And any device that is controlled by a master device is defined as a “Slave”.
The device transmitting data is defined as a “Transmitter” and the device receiving data is defined as a “receiver”

In the case of this RTC module, controllers such as a CPU are defined as master devices and the RTC module is defined as a slave device. When a device is used for both transmitting and receiving data, it is defined as either a transmitter or receiver depending on these conditions.

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8.9.3. Starting and stopping I²C-Bus communications

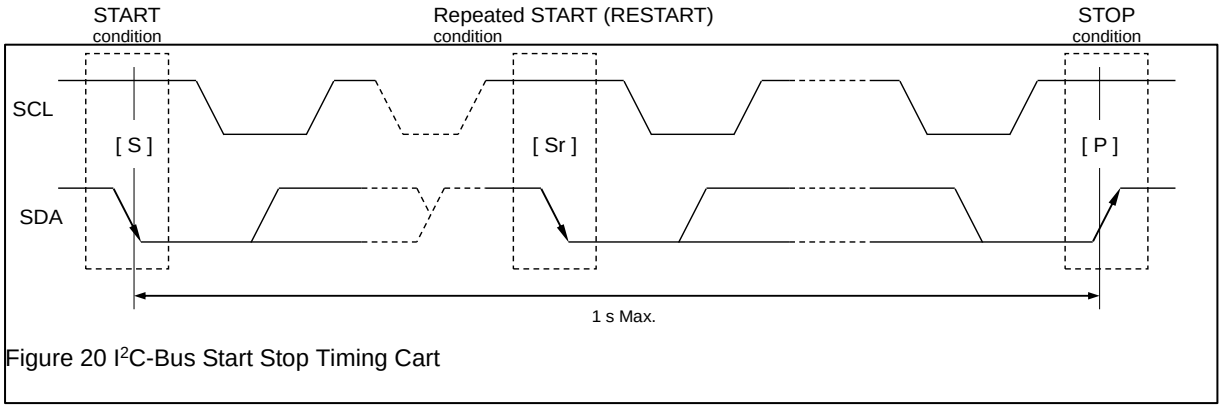


Figure 20 I²C-Bus Start Stop Timing Cart

1) START condition, repeated START condition, and STOP condition

(1) START condition
The SDA level changes from high to low while SCL is at high level.

(2) STOP condition
This condition regulates how communications on the I²C-Bus are terminated. The SDA level changes from low to high while SCL is at high level.

(3) Repeated START condition (RESTART condition)
In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

2) Caution points

1) The master device always controls the START, RESTART, and STOP conditions for communications.

2) The master device does not impose any restrictions on the timing by which STOP conditions affect transmissions, so communications can be forcibly stopped at any time while in progress. (However, this is only when this RTC module is in receiver mode (data reception mode = SDA released).

3) When communicating with this RTC module, the series of operations from transmitting the START condition to transmitting the STOP condition should occur within 1 second. (A RESTART condition may be sent between a START condition and STOP condition, but even in such cases the series of operations from transmitting the START condition to transmitting the STOP condition should still occur within 1 second.)

If this series of operations requires 1 second or longer, the I²C-Bus interface will be automatically cleared and set to standby mode by this RTC module's bus timeout function. Note with caution that both write and read operations are invalid for communications that occur during or after this auto clearing operation. (When the read operation is invalid, all data that is read has a value of “1”).
Restarting of communications begins with transfer of the START condition again

∗4) When communicating with this RTC module, wait at least 1.3 µs (see the tBUF rule) between transferring a STOP condition (to stop communications) and transferring the next START condition (to start the next round of communications).

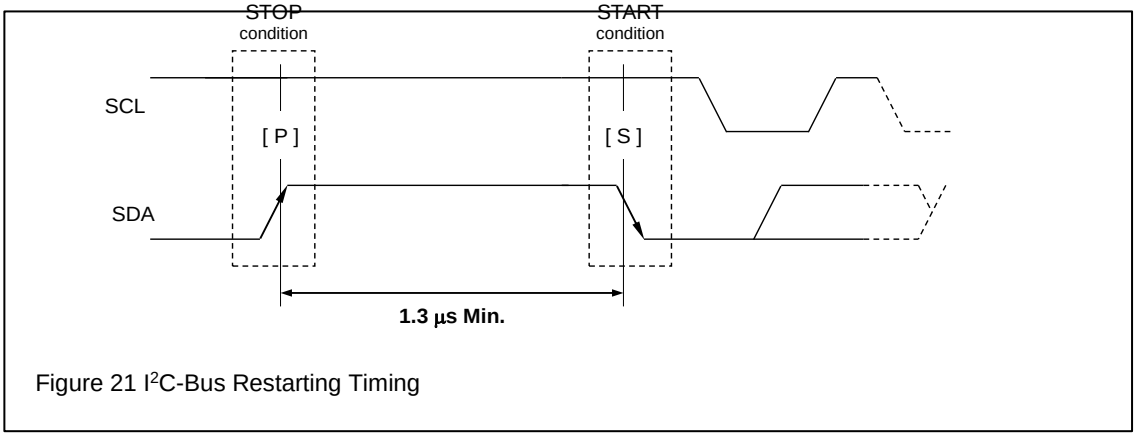


Figure 21 I²C-Bus Restarting Timing

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8.9.4. Data Transfers and Acknowledge Responses during I²C-Bus Communications

1) Data transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition. (However, the transfer time must be no longer than 1 second)

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level. The receiver (receiving side) receives data while the SCL line is at high level.

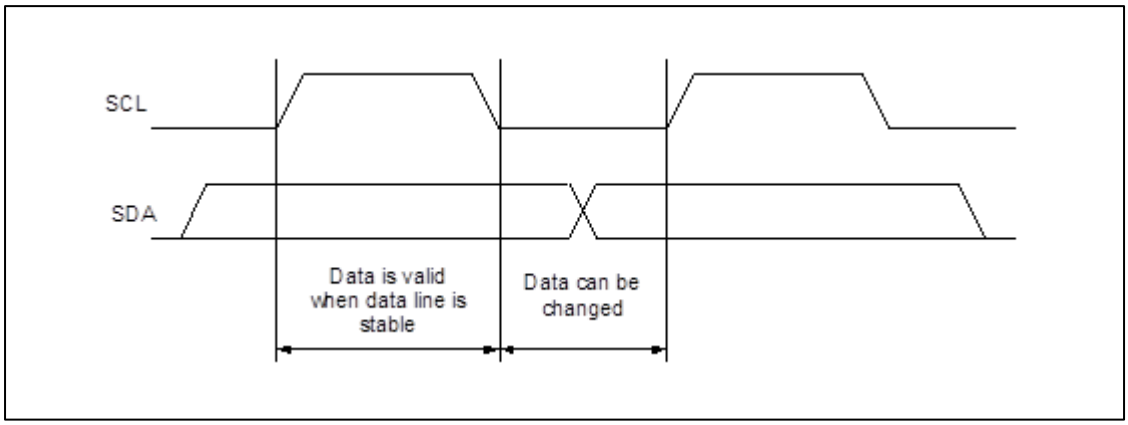


Figure 22 I²C-Bus SDA, SCL

* Note with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

2) Data acknowledge response (ACK signal)

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.

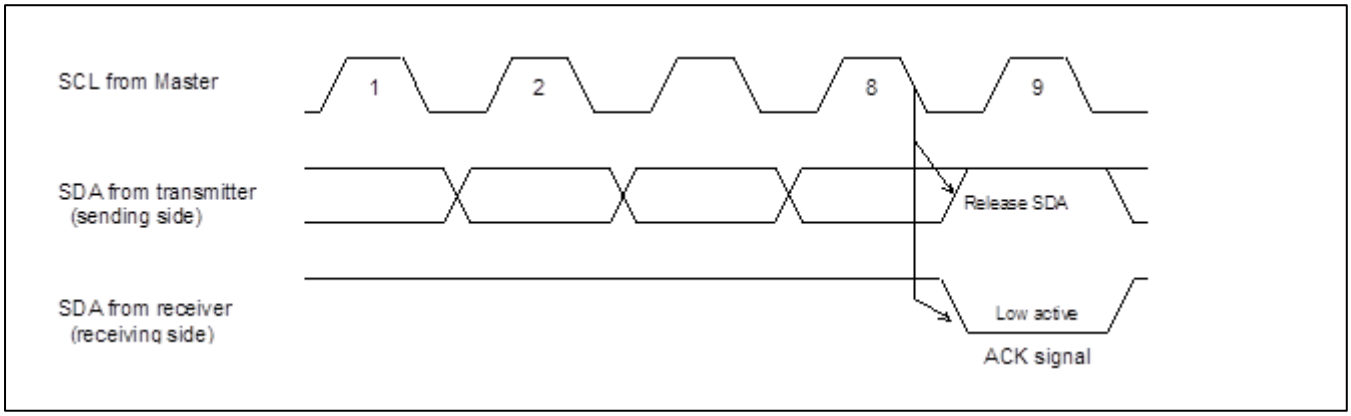


Figure 23 I²C-Bus Acknowledge Signal

After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.
When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

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8.9.5. Slave Address

The I²C-Bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.
All communications begin with transmitting the [START condition] + [slave address (+ R/W specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.

Slave addresses have a fixed length of 7 bits. This RTC's slave address is [0110 010*].
An R/W bit ("*" above) is added to each 7-bit slave address during 8-bit transfers.

Table 58 I²C-Bus Slave Address

	Transfer data	Slave address							R / W bit
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	65h	0	1	1	0	0	1	0	1
Write	64h								0

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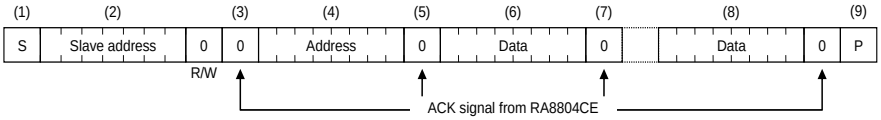
8.9.6. I²C-Bus Protocol

In the following sequence descriptions, it is assumed that the CPU is the master and the RA8804CE is the slave.

a. Address specification write sequence

Since the RA8804CE includes an address auto increment function, once the initial address has been specified, the RA8804CE increments (by one byte) the receive address each time data is transferred.

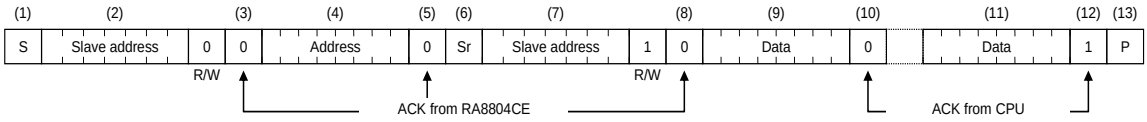
(1) CPU transfers start condition [S].
(2) CPU transmits the RA8804CE's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RA8804CE.
(4) CPU transmits write address to RA8804CE.
(5) Check for ACK signal from RA8804CE.
(6) CPU transfers write data to the address specified at (4) above.
(7) Check for ACK signal from RA8804CE.
(8) Repeat (6) and (7) if necessary. Addresses are automatically incremented.
(9) CPU transfers stop condition [P].



b. Address specification read sequence

After using write mode to write the address to be read, set read mode to read the actual data.

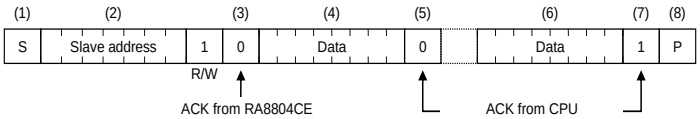
(1) CPU transfers start condition [S].
(2) CPU transmits the RA8804CE's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RA8804CE.
(4) CPU transfers address for reading from RA8804CE.
(5) Check for ACK signal from RA8804CE.
(6) CPU transfers RESTART condition [Sr] (in which case, CPU does not transfer a STOP condition [P]).
(7) CPU transfers RA8804CE's slave address with the R/W bit set to read mode.
(8) Check for ACK signal from RA8804CE (from this point on, the CPU is the receiver and the RA8804CE is the transmitter).
(9) Data from address specified at (4) above is output by the RA8804CE.
(10) CPU transfers ACK signal to RA8804CE.
(11) Repeat (9) and (10) if necessary. Read addresses are automatically incremented.
(12) CPU transfers ACK signal for “1”.
(13) CPU transfers stop condition [P].



c. Read sequence when address is not specified

Once read mode has been initially set, data can be read immediately. In such cases, the address for each read operation is the previously accessed address + 1.

(1) CPU transfers start condition [S].
(2) CPU transmits the RA8804CE's slave address with the R/W bit set to read mode.
(3) Check for ACK signal from RA8804CE (from this point on, the CPU is the receiver and the RA8804CE is the transmitter).
(4) Data is output from the RA8804CE to the address following the end of the previously accessed address.
(5) CPU transfers ACK signal to RA8804CE.
(6) Repeat (4) and (5) if necessary. Read addresses are automatically incremented in the RA8804CE.
(7) CPU transfers ACK signal for “1”.
(8) CPU transfers stop condition [P].



d. The address auto increment in Read / Write.

(1) In Basic time and calendar resister.
Address - - - - - - - 08 - 09 - 0A - 0B - 0C - 0D - 0E - 0F - 00 - 01 - 02 - -
(2) In Extension resister
Address - - - - - - - 18 - 19 - 1A - 1B - 1C - 1D - 1E - 1F - 10 - 11 - 12 - -

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8.10. Backup and Recovery

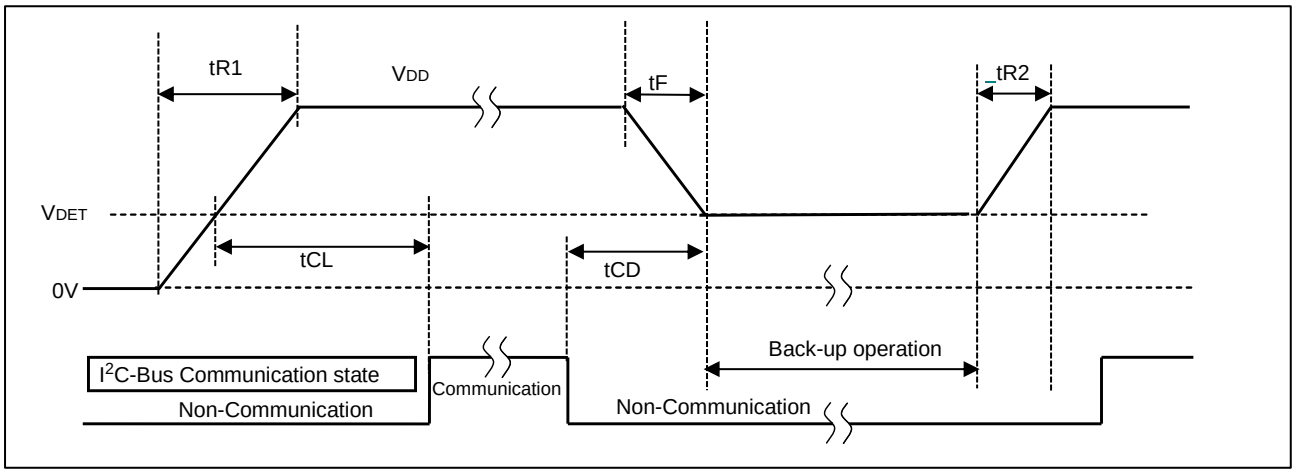


Figure 24 V_{DD} Sequence

RTC circuit is sensitive and supply voltage should be stabilized to avoid negative impact on the clock accuracy or other functions.
tR1 spec is need for a proper power-on reset, and VDD need start from less than 0.2V.
Therefore, In RTC cold start, recommended keep VDD = GND more than about 10 seconds for a proper power-on reset.
When these condition is difficulty, Power-on-reset can be performed using a software command.
When out of spec tR2 or tF, it have possibility of momentary missing clock output from FOUT. But crystal oscillation is not stops.

Table 59 V_{DD} sequence characteristics

Item	symbol	Condition	Min.	Typ.	Max.	Unit
Power supply rise time1	tR1	V_{DD} = V_{SS} ~ 5.5 V	1		10	ms / V
Access wait time (after initial power on)	tCL	After V_{DD} = V_{DET}	30			ms
Power supply fall time	tF	V_{DD} = 5.5 V ~ V_{DET}	100			µs / V
Power supply rise time	tR2	V_{DD} = V_{DET} ~ 5.5 V	15			µs / V
Setup time from finish of I^2C-Bus	tCD	Before V_{DD} = V_{DET}	0			µs

8.10.1. Software Reset Procedure

If it is difficult to ensure conditions such as tR1 above or if the power supply environment is unstable, a power-on reset can be performed using a software command.
Soft ware Reset can be performed at any time.
This software reset does not affect the stored date and time data.
But, sub-second counters are cleared to zero.
As a result, frequent software resets may cause the time to be delayed.
In addition, the reset sets the VLF and VDET detection bits to 1, and initial values are loaded into each control bit.
Please be sure setup the optimal initial value for each of system again.
The following procedure operates the registers for device inspection. The detailed inspection function is confidential.
Please perform STEP 5 to STEP 8 promptly.

Table 60 Software Reset Step

STEP	R/W	Address	Write Data		
1				V_{DD} ON	
2				Need wait time more than 30ms.	
3	Read	0x07		Perform read access to address 0x07 according to the sequence in "b. Address specification read sequence". Do not need judge the ACK and readout data.	
4	Read	0x0D		Perform read access to address 0x0D according to the sequence in "b. Address specification read sequence". Do not need judge the ACK and readout data.	
5	Write	0x0F	0x00		
6	Write	0x0D	0x80		
7	Write	0xCB	0x6C	Inspection register	
8	Write	0xCF	0x01	Inspection register	
9				After wait time more than 5ms, Reset complete.	

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8.11. About Access at the Time of Backup Return and Initial Power Supply

Because most of RTC registers are synchronized with the oscillation clock of the built-in crystal oscillator, the RTC does not work normally without the integrated oscillator having stabilized. Please initialize the RTC at the time the power supply voltage returns (VLF = 1) after the oscillation has stabilized (after oscillation start time tSTA).

If intending to access the RTC after the main supply voltage returns, please note following points:

Please begin to read VLF-bit first.
If VLF-bit returns “1”, please initialize all registers. Please perform initial setting only tSTA (oscillation start time), when the built-in oscillation is stable.
Access is prohibited about 30 ms, from the VCLK voltage. VCLK (clock supply voltage (V_{DD} > 1.5 V).
If VLF-bit returns “0”, access is possible without waiting time.
Before the internal crystal oscillator has stabilized (tSTA), no clock operation is possible, and time is not counted.

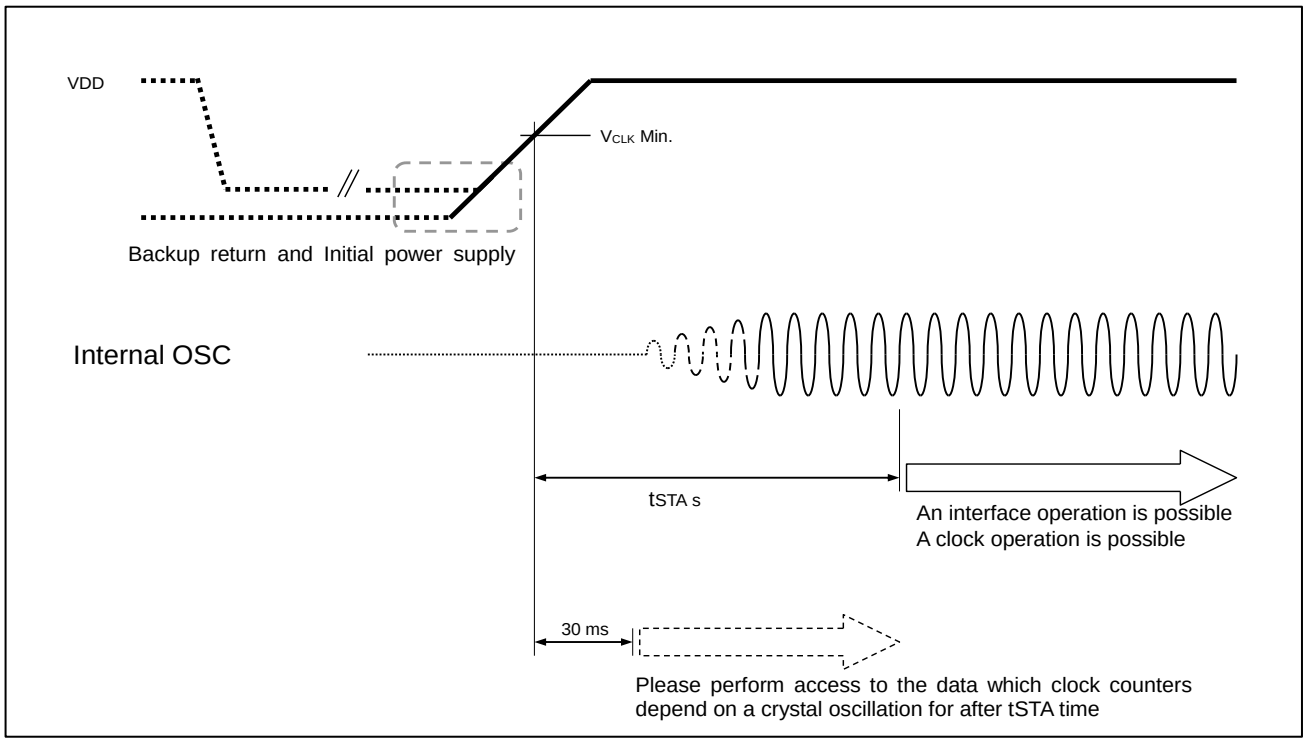


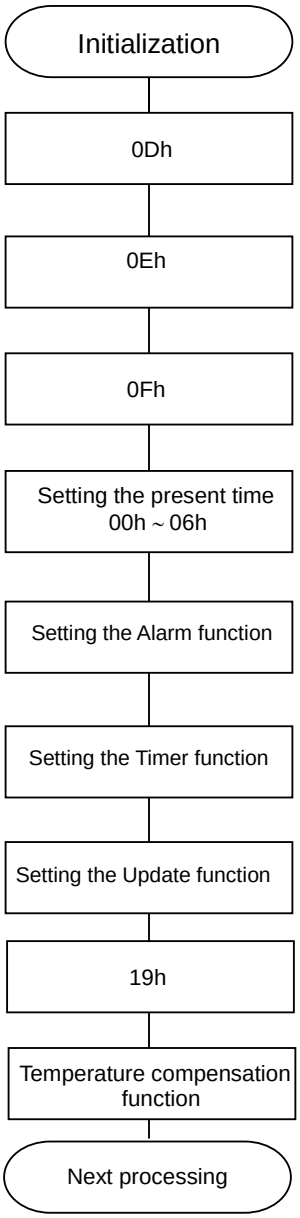
Figure 25 Power ON and restore from backup sequence

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8.12. Flow Chart

The following flow-chart is one example, but it is not necessarily applicable for every use-case and not necessarily the most effective process for individual applications.

1) An example of the initialization



- Cleart TE bit to “0”. Clear TEST bit to “0”
- Setup FSEL1, 0 bit optionally

- Clear VDET, VLF bit to “0”

- Set AIE, TIE, UIE bit to “0 " to prevent unprepared interruption output

- Set the present time
  * Setting the present time concerned, please refer to item of [Clock and calendar writing]

- Set the Alarm interrupt function
  When the alarm interrupt function is not being used, the Alarm registers can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit

- Set the fixed-cycle Timer function
  When the fixed-cycle timer function is not being used, the Timer Counter register can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits

- Set the Update interrupt function

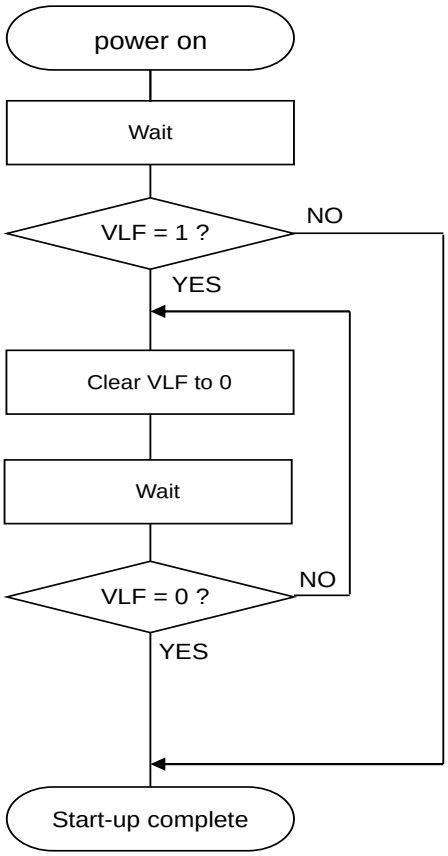
- Writes 00h. Disable output of SOUT

- Set the interval of a temperature compensation operation

Figure 26 Flow ex. 1

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2) Method of initialization after starting of internal oscillation (VLF stays “0”)

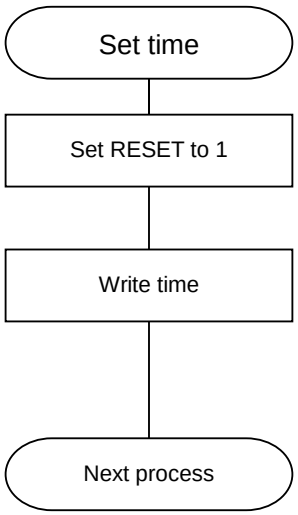


- Wait time of 30 ms is necessary at least
- Whether it is a return from the state of the backup is confirmed
- When an internal oscillation starts, 0 writing of VLF is approved
- Please set waiting time depending on load of a system optionally

Figure 27 Flow ex. 2

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3) The setting of the clock and calendar

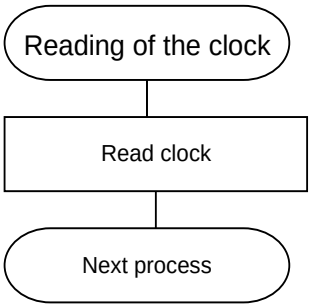


- Set RESET bit to 1 to prevent timer update in time setting

- Write information of [year / month /date [day of the week] hour: minute: second] which is necessary to set (or reset)
  In case of initialization, please initialize all data
- Please complete access within 1 seconds

Figure 28 Flow ex. 3

4) The reading of the clock and calendar



- Please complete access within 1 second

- At the time of a communication start, the Clock & Calendar data are fixed (hold the carry operation), and it is automatically revised at the time of the communication end

- The access to a clock calendar recommends to have access to continuation by an auto increment function

Figure 29 Flow ex. 4

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8.13. Connection with Typical Microcontroller

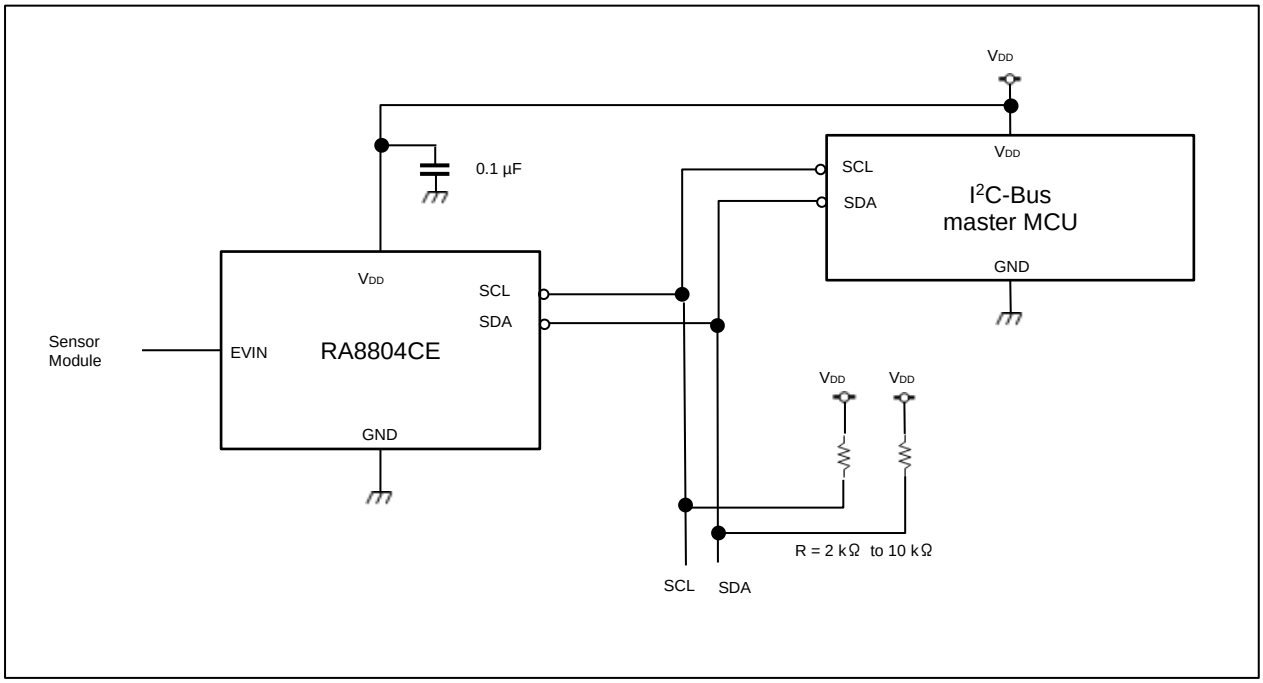


Figure 30 Circuit Diagram

8.14. When Used as a Clock Source (32.768 kHz DTCXO)

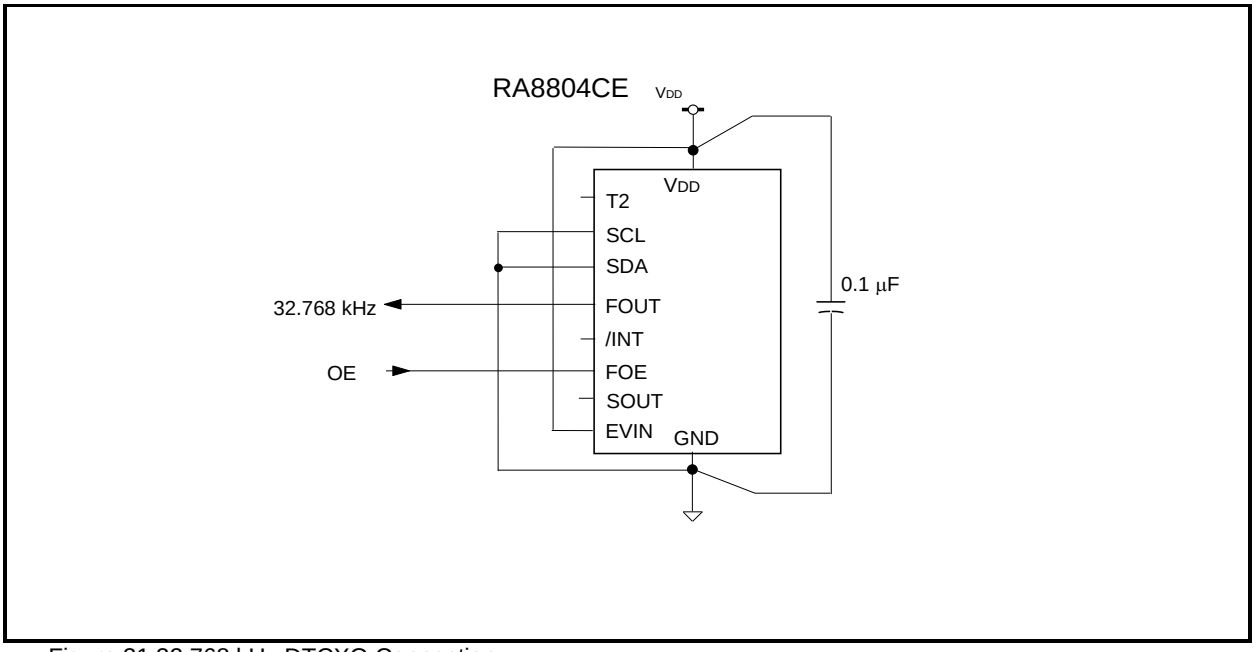
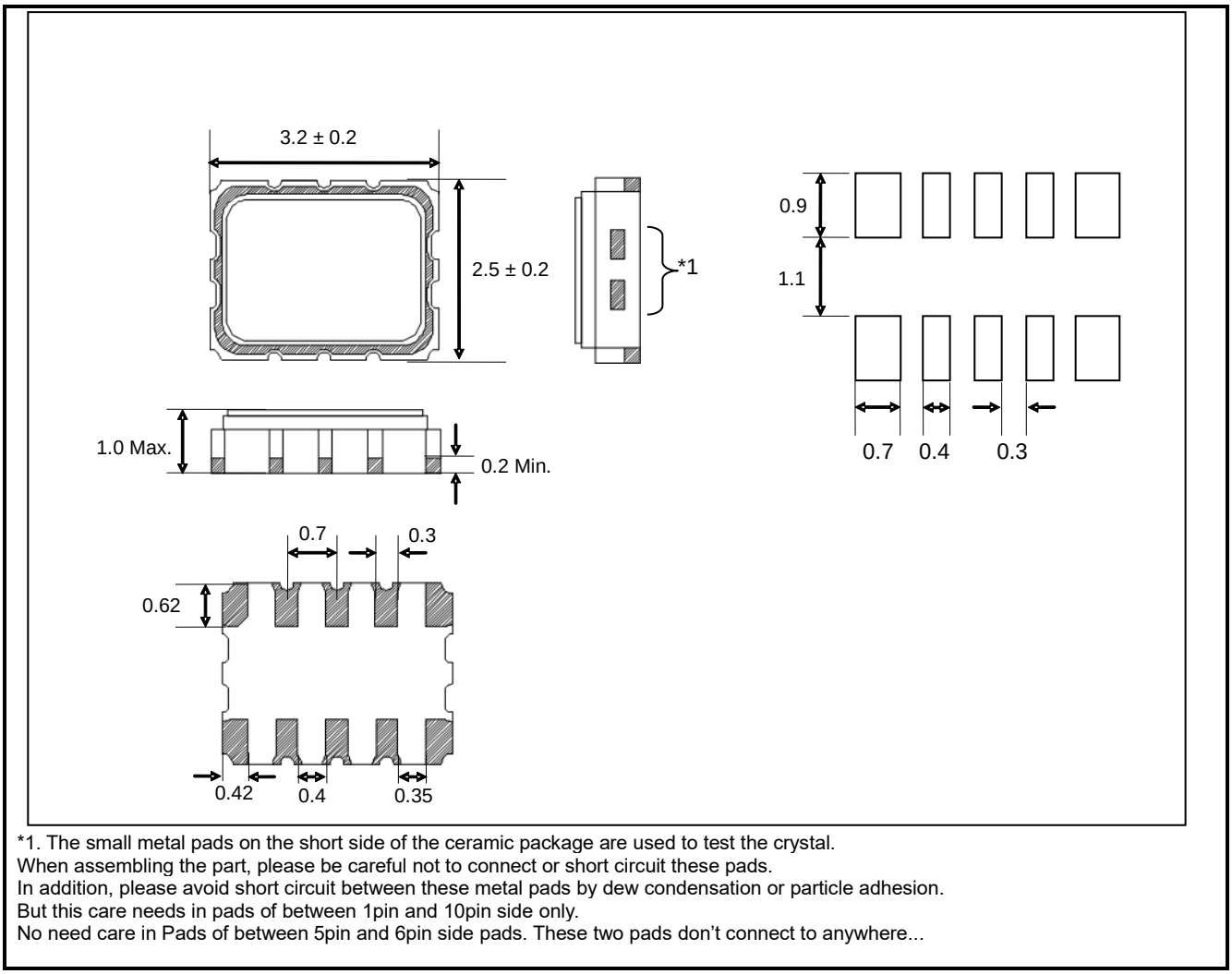


Figure 31 32.768 kHz DTCXO Connection

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9. External Dimensions / Marking Layout

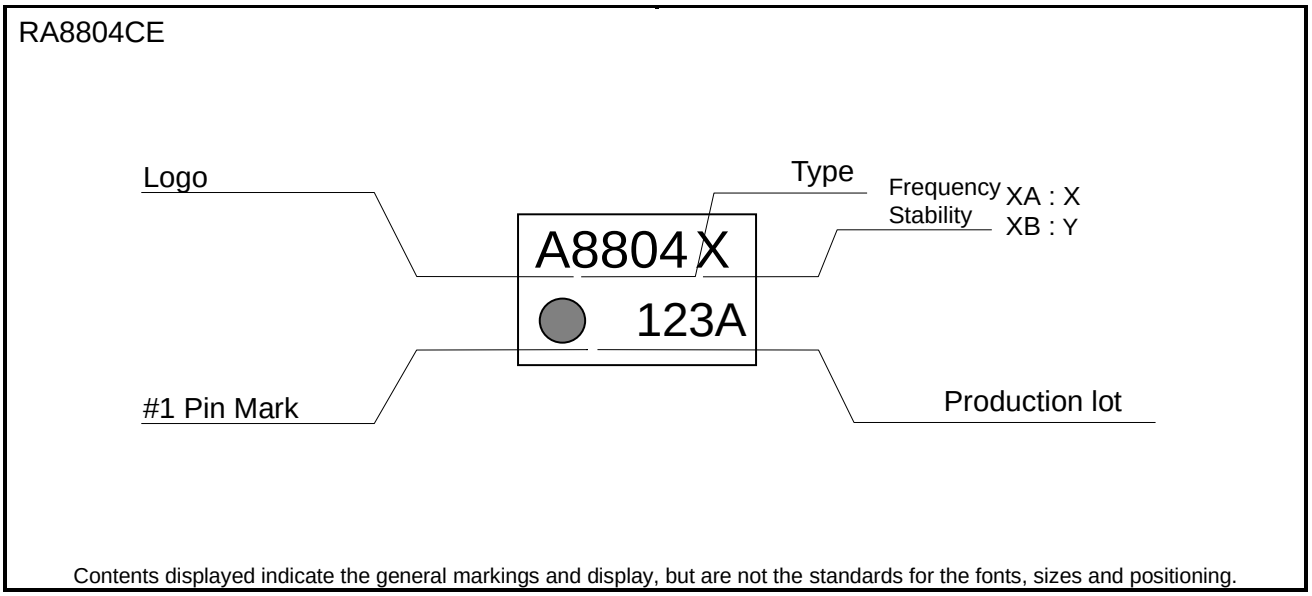
9.1. External Dimensions



*1. The small metal pads on the short side of the ceramic package are used to test the crystal.
When assembling the part, please be careful not to connect or short circuit these pads.
In addition, please avoid short circuit between these metal pads by dew condensation or particle adhesion.
But this care needs in pads of between 1pin and 10pin side only.
No need care in Pads of between 5pin and 6pin side pads. These two pads don't connect to anywhere...

Figure 32 Package Dimension

9.2. Marking Layout



Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

Figure 33 Marking

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10.Application Notes

1) Notes on handling

This module uses a CMOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity
While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise
If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 μF as close as possible to the power supply pins (between V_{DD} and GND). Also, avoid placing any device that generates high level of electronic noise near this module.
* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins
When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin and can impair the functioning of the device. Therefore, please apply the voltage level close to V_{DD} or GND.

(4) Handling of unused pins
Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, please apply the voltage level close to V_{DD} or GND.
But these pins must be the disposals that followed specification of pin exposition when it was specified N.C or open by pin exposition.

2) Notes on packaging

(1) Soldering heat resistance.
If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded, and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.
* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Mounting equipment
While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning
Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation
This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins
Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

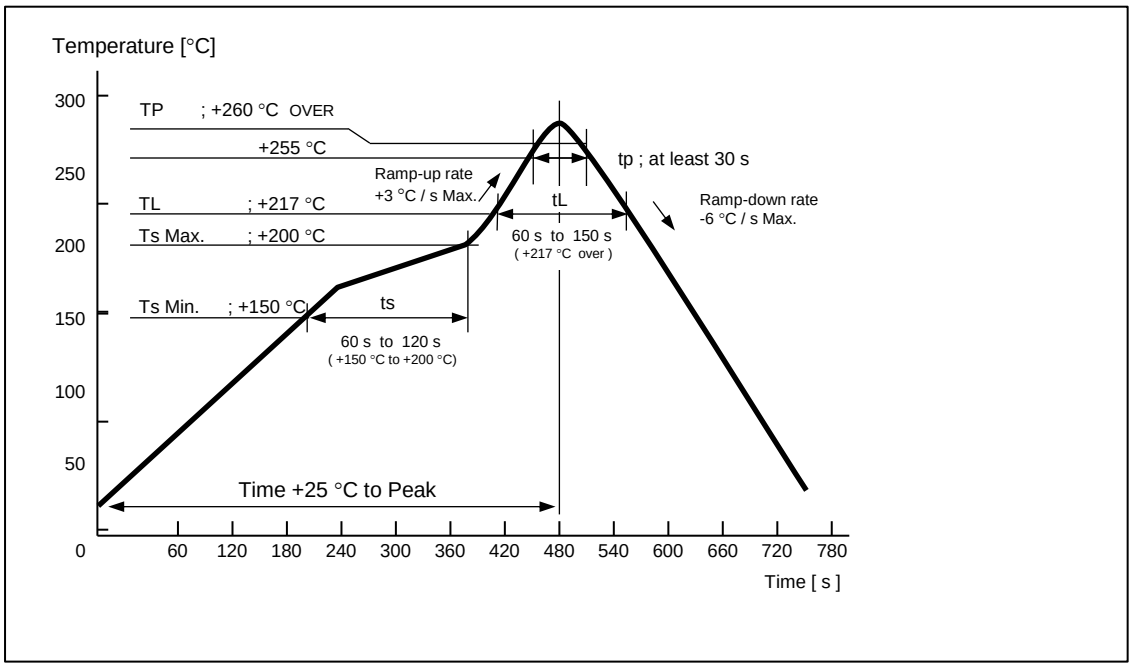


Figure 34 Soldering Profile

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11.Figures

Figure 1 Block Diagram 6
Figure 2 Pin Layout 7
Figure 3 I²C-Bus Timing Chart 10
Figure 4 Temperature compensation current 11
Figure 5 I²C-Bus Current consumption 11
Figure 6 Internal clock distribution diagram 15
Figure 7 EVIN Debounce Function 21
Figure 9 SOUT Function Program ex.1 22
Figure 9 SOUT function Program ex.2 23
Figure 10 Time Stamp Program ex. 24
Figure 11 EVIN Timing Chart 25
Figure 12 Alarm Function 26
Figure 13 Alarm Timing Chart 28
Figure 14 Wakeup Timer Function 29
Figure 16 Wakeup Timer Count Down Timing Chart 30
Figure 16 Wakeup Timer Start Sequence 31
Figure 17 Wakeup Timer Timing Chart 33
Figure 18 Update Interrupt Timing Chart 35
Figure 19 I²C-Bus Connection 37
Figure 20 I²C-Bus Start Stop Timing Cart 38
Figure 22 I²C-Bus Restarting Timing 38
Figure 22 I²C-Bus SDA, SCL 39
Figure 23 I²C-Bus Acknowledge Signal 39
Figure 24 V_{DD} Sequence 42
Figure 25 Power ON and restore from backup sequence 43
Figure 26 Flow ex. 1 44
Figure 27 Flow ex. 2 45
Figure 28 Flow ex. 3 46
Figure 29 Flow ex. 4 46
Figure 30 Circuit Diagram 47
Figure 31 32.768 kHz DTCXO Connection 47
Figure 32 Package Dimension 48
Figure 33 Marking 48
Figure 34 Soldering Profile 49

12.Tables

TRES bit typo was corrected. Table 47 TRES bit 3
Table 1 Pin Functions 7
Table 2 Absolute Maximum Rating 8
Table 3 Recommended Operating Conditions 8
Table 4 Frequency Characteristics 8
Table 5 DC Characteristics 9
Table 6 AC Characteristics 10
Table 7 Average Current consumption IDD1, IDD2 11
Table 8 Register Division (00h ~ 0Fh) 12
Table 9 Register Table (00h ~ 0Fh) 12
Table 10 Register Table (10h ~ 1Fh) 13
Table 11 Quick Reference 13
Table 12 Registers Initial Value 13
Table 13 Clock, Calendar Register 14
Table 14 WEEK Register 14
Table 15 DAY Register 14
Table 16 Alarm registers 15
Table 17 Wakeup Timer Control Registers 16
Table 18 Control Register, Flag Register 16
Table 19 Test bit 16
Table 20 VLF bit 16
Table 21 VDET bit 17
Table 22 RESET bit 17
Table 23 FSEL bit 18
Table 24 AIE, TIE, UIE bit 18
Table 25 SOUT Control Register 18
Table 26 DCE, DC bit 19
Table 27 SRV bit 19
Table 28 FS bit 19
Table 29 Time Stamp Data Event Control 19
Table 30 ECP bit 20
Table 31 EHL bit 20

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Table 32 EPU bit 20
Table 33 RCE bit 20
Table 34 EF bit 20
Table 35 ET bit 21
Table 36 EIE bit 21
Table 37 EVMON bit 21
Table 38 Alarm Interrupt Function Register 26
Table 39 WADA bit 26
Table 40 AF bit AF bit 27
Table 41 AIE bit 27
Table 42 Alarm Setting ex.1 27
Table 43 Alarm Setting ex.2 28
Table 44 Wakeup Timer Register 29
Table 45 TESL bit 30
Table 46 TSTP bit 30
Table 47 TRES bit 30
Table 48 TE bit 31
Table 49 TF bit 31
Table 50 TIE bit 31
Table 51 Wakeup Timer Interrupt Interval 32
Table 52 Update Interrupt Function Register 34
Table 53 USEL bit 34
Table 54 UF bit 34
Table 55 UIE bit 35
Table 56 Temperature Compensation Register 36
Table 57 CSEL bit 36
Table 58 I^2C-Bus Slave Address 40
Table 59 VDD sequence characteristics 42
Table 60 Software Reset Step 42

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