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Application Manual

Real Time Clock Module

RA4803SA

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Contents

1. Overview....1

2. Block Diagram....1

3. Terminal description....2
3.1. Terminal connections....2
3.2. Pin Functions....2

4. Absolute Maximum Ratings....3

5. Recommended Operating Conditions....3

6. Frequency Characteristics....3

7. Electrical Characteristics....4
7.1. DC characteristics....4
7.2. AC Characteristics....5

8. Use Methods....6
8.1. Description of Registers....6
8.1.1. Write / Read and Bank Select....6
8.1.2. Register table (Bank1)....6
8.1.3. Register table (Bank2)....7
8.1.4. Register table (Bank3)....7
8.2. Details of Registers....8
8.2.1. Clock counter (1/100S, SEC - HOUR)....8
8.2.2. Calendar counter (WEEK - YEAR)....9
8.2.3. Alarm registers....10
8.2.4. Fixed-cycle timer control registers....10
8.2.5. Extension register....10
8.2.6. Flag register....11
8.2.7. Control register....12
8.2.8. OSC Offset Contorol (Reg -C / Bank 3)....14
8.2.9. Capture Buffer / Event control (Bank 3)....15
8.3. Fixed-cycle Timer Interrupt Function....16
8.3.1. Diagram of fixed-cycle timer interrupt function....16
8.3.2. Related registers for function of time update interrupts....17
8.3.3. Fixed-cycle timer interrupt interval (example)....18
8.3.4. Fixed-cycle timer start timing....18
8.4. Time Update Interrupt Function....19
8.4.1. Time update interrupt function diagram....19
8.4.2. Related registers for time update interrupt functions.....20
8.5. Alarm Interrupt Function....21
8.4.1. Diagram of alarm interrupt function....21
8.5.2. Related registers....22
8.5.2. Examples of alarm settings....23
8.6. Read/Write of data....24
8.6.1. Write of data....24
8.6.2. Read of data....24
8.7. VDD and CE timing....25
8.8. Backup and Recovery....25
8.9 Connection with Typical Microcontroller....26
8.10 When used as a clock source (32 kHz-TCXO)....26
8.11. Note about read-out method of a 1/100s register....27

9. External Dimensions / Marking Layout....28

10. Application notes....29

For automotive Serial Interface Real-time Clock Module

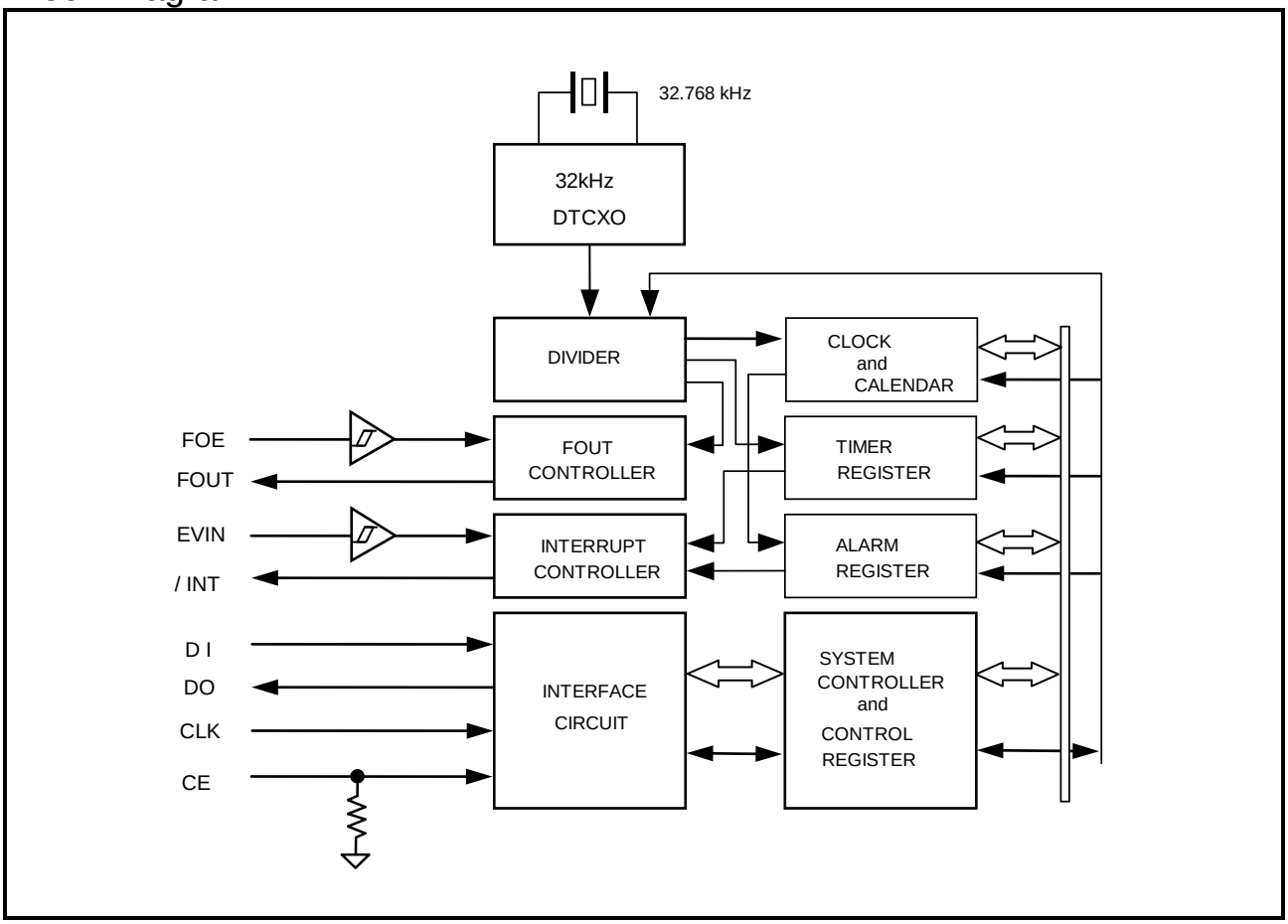
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- Features built-in 32.768 kHz DTCXO, High Stability.
- Serial interface in 4 lines form
- Alarm interrupt function for day, date, hour, and minute settings
- Fixed-cycle timer interrupt function
- Time update interrupt function (Seconds, minutes)
- 32.768 kHz output with OE function (FOE and FOUT pins)
- Auto correction of leap years (from 2000 to 2099)
- Wide interface voltage range: 1.6 V to 5.5 V
- Wide time-keeping voltage range: 1.6 V to 5.5 V
- Low current consumption: 0.75μA / 3 V (Typ.)

1. Overview

This module is an serial interface real-time clock which includes a 32.768 kHz DTCXO.
In addition to providing a calendar (year, month, date, day, hour, minute, second) function and a clock counter function, this module provides an abundance of other functions including an alarm function, fixed-cycle timer function, time update interrupt function, and 32.768 kHz output function.
The devices in this module are fabricated via a C-MOS process for low current consumption, which enables long-term battery back-up.
All of these many functions are implemented in SOP-14 pin package.

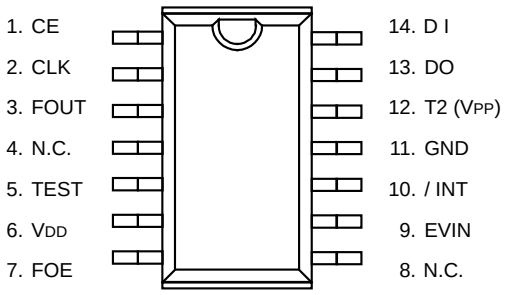
2. Block Diagram



3. Terminal description

3.1. Terminal connections

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SOP – 14pin

3.2. Pin Functions

Signal name	I/O	Function
CE	Input	This is the chip enabled input pin. It has a built-in pull-down resistance. When the CE pin is at the "H" level, access to this RTC becomes possible. Also, when the chip is not selected, the DO pin is at the high impedance level, and the CLK and DI pins would not accept input.
CLK	Input	This is the shift clock input pin for serial data transfer. In the write mode, it takes in data from the DI pin using the CLK signal rise edge. In the read mode, it outputs data from the DO pin using the fall edge.
D I	Input	This is the data input pin for serial data transfer.
DO	Output	This is the data output pin for serial data transfer.
FOUT	Output	This is the C-MOS output pin with output control provided via the FOE pin. When FOE = "H" (high level), this pin outputs a 32.768 kHz signal. When output is stopped, the FOUT pin = "Hi-Z"(high impedance).
FOE	Input	This is an input pin used to control the output mode of the FOUT pin. When this pin's level is high, the FOUT pin is in output mode. When it is low, output via the FOUT pin is stopped.
/ INT	Output	This pins is used to output alarm signals, timer signals, time update signals, and other signals. This pin is an open drain pin.
EVIN	Input	External event input pin.
VDD	–	This pin is connected to a positive power supply.
GND	–	This pin is connected to a ground.
TEST	Input	Use by the manufacture for testing. (Do not connect externally.)
T2(VPP)	–	Use by the manufacture for testing. (Do not connect externally.)
N.C.	–	This pin is not connected to the internal IC. Leave N.C. pins open or connect them to GND or VDD.

Note: Be sure to connect a bypass capacitor rated at least 0.1 µF between VDD and GND.

4. Absolute Maximum Ratings

GND = 0 V

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	Between V_{DD} and GND	−0.3 to +6.5	V
Input voltage	V_{IN1}	CE, CLK, DI, FOE, EVIN pin	−0.3 to +6.5	V
Output voltage (1)	V_{OUT1}	DO, FOUT pin	GND−0.3 to V_{DD}+0.3	V
Output voltage (2)	V_{OUT2}	/INT pins	GND−0.3 to +6.5	V
Storage temperature	T_{STG}	When stored separately, without packaging	−55 to +125	°C

5. Recommended Operating Conditions

GND = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}	Interface voltage	1.6	3.0	5.5	V
Temp. compensation voltage	V_{TEM}	Temperature compensation voltage	2.2	3.0	5.5	V
Clock supply voltage	V_{CLK}	−	1.6	3.0	5.5	V
Operating temperature	T_{OPR}	No condensation	−40	+25	+85	°C

6. Frequency Characteristics

GND = 0 V

Item	Symbol	Condition		Rating	Unit
Frequency stability	Δ f / f	U A	Ta= 0 to +50 °C, V_{DD}=3.0 V Ta=−40 to +85 °C, V_{DD}=3.0 V	± 1.9 (*1) ± 3.4 (*2)	× 10^{-6}
		U B	Ta= 0 to +50 °C, V_{DD}=3.0 V Ta=−40 to +85 °C, V_{DD}=3.0 V	± 3.8 (*3) ± 5.0 (*4)	
		U C	Ta= 0 to +50 °C, V_{DD}=3.0 V Ta=−30 to +70 °C, V_{DD}=3.0 V	± 3.8 (*3) ± 5.0 (*4)	
		A A	Ta= +25 °C, V_{DD}=3.0 V	+5± 5.0 (*5)	
Frequency/voltage characteristics	f / V	Ta= +25 °C, V_{DD}=2.2 V to 5.5 V		± 1.0 Max.	× 10^{-6} / V
Oscillation start time	tSTA	Ta= +25 °C, V_{DD}=1.6 V Ta=−40 to +85 °C, V_{DD}=1.6 V to 5.5 V		1.0 Max. 3.0 Max.	s
Aging	fa	Ta= +25 °C, V_{DD}=3.0 V, first year		± 3 Max.	× 10^{-6} / year

*1) Equivalent to 5 seconds of month deviation. *2) Equivalent to 9 seconds of month deviation.
*3) Equivalent to 10 seconds of month deviation. *4) *5) Equivalent to 13 seconds of month deviation. (excluding offset)

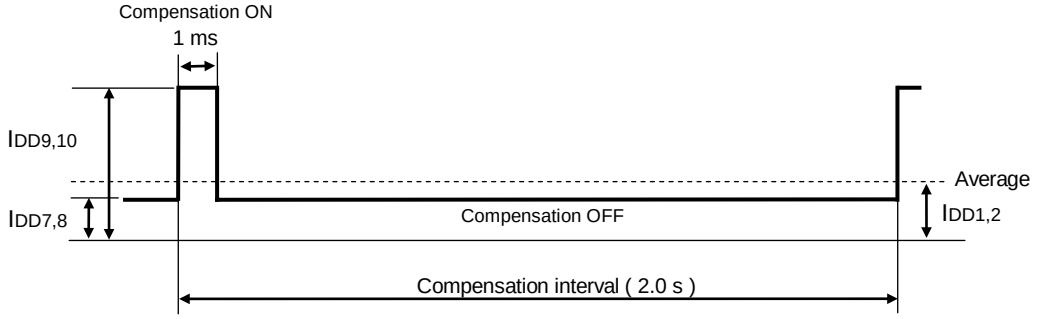
7. Electrical Characteristics

7.1. DC characteristics

*Unless otherwise specified, GND = 0 V , V_{DD} = 1.6 V to 5.5 V , Ta = –40 °C to +85 °C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption (1)	I_{DD1}	CE = GND, /INT = V_{DD} FOE = GND FOUT : output OFF (High Z) Compensation interval 2.0 s	V_{DD} =5 V		0.75	3.4	µA
Current consumption (2)	I_{DD2}		V_{DD}=3 V		0.75	2.1	
Current consumption (3)	I_{DD3}	CE = GND, /INT, FOE = V_{DD} FOUT : 32 kHz, CL = 0 pF Compensation interval 2.0 s	V_{DD}=5 V		2.0	7.5	µA
Current consumption (4)	I_{DD4}		V_{DD}=3 V		1.5	5.0	
Current consumption (5)	I_{DD5}	CE = GND, /INT, FOE = V_{DD} FOUT: 32 kHz, CL = 30 pF Compensation interval 2.0 s	V_{DD}=5 V		7.0	20.0	µA
Current consumption (6)	I_{DD6}		V_{DD}=3 V		4.5	12.0	
Current consumption (7)	I_{DD7}	CE = GND, /INT, FOE = GND FOUT : output OFF (High Z) Compensation OFF	V_{DD}=5 V		0.7	2.95	µA
Current consumption (8)	I_{DD8}		V_{DD}=3 V		0.7	1.85	
Current consumption (9)	I_{DD9}	CE = GND, /INT, FOE = GND FOUT : output OFF (High Z) Compensation ON (peak)	V_{DD}=5 V		120	900	µA
Current consumption (10)	I_{DD10}		V_{DD}=3 V		115	350	
High-level input voltage	V_{IH}	CE, DI, CLK, FOE, EVIN pins		0.8 × V_{DD}		5.5	V
Low-level input voltage	V_{IL}	CE, DI, CLK, FOE, EVIN pins		GND – 0.3		0.2 × V_{DD}	V
High-level output voltage	V_{OH1}	FOUT, DO pins	V_{DD}=5 V, I_{OH}=–1 mA	4.5		5.0	V
	V_{OH2}		V_{DD}=3 V, I_{OH}=–1 mA	2.2		3.0	
	V_{OH3}		V_{DD}=3 V, I_{OH}=–100 µA	2.9		3.0	
Low-level output voltage	V_{OL1}	FOUT, DO pins	V_{DD}=5 V, I_{OL}=1 mA	GND		GND+0.5	V
	V_{OL2}		V_{DD}=3 V, I_{OL}=1 mA	GND		GND+0.8	
	V_{OL3}		V_{DD}=3 V, I_{OL}=100 µA	GND		GND+0.1	
	V_{OL4}	/INT pin	V_{DD}=5 V, I_{OL}=1 mA	GND		GND+0.25	V
	V_{OL5}		V_{DD}=3 V, I_{OL}=1 mA	GND		GND+0.4	
Input leakage current	I_{LK}	CE, DI, CLK, FOE pins, V_{IN} = V_{DD} or GND		–0.5		0.5	µA
Output leakage current	I_{OZ}	/INT, DO, FOUT pins, V_{OUT} = V_{DD} or GND		–0.5		0.5	µA
Input resistance	R_{DWN}	CE pin	V_{DD}=5 V	75	150	300	kΩ
			V_{DD}=3 V	150	300	600	

- Temperature compensation and consumption current

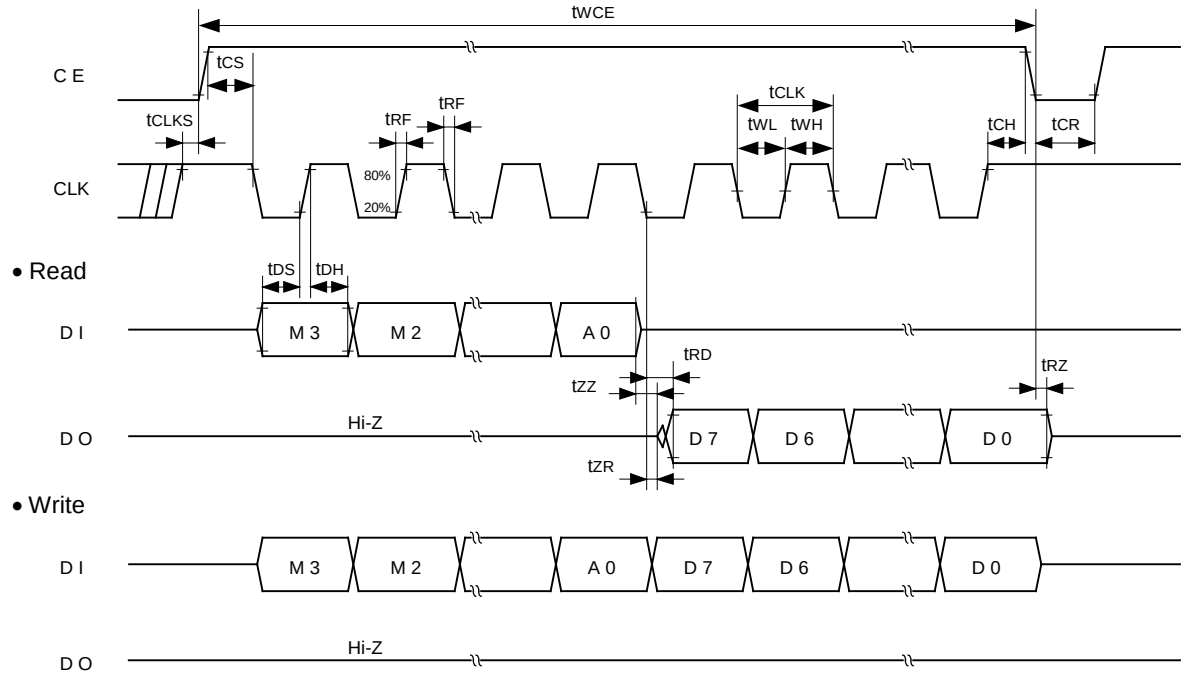


7.2. AC Characteristics

* Unless otherwise specified, GND = 0 V , Ta = –40 °C to +85 °C

Item	Symbol	Condition	2.4V ≤ V_{DD} < 4.5V		4.5V ≤ V_{DD} ≤ 5.5V		Unit
			Min.	Max.	Min.	Max.	
CLK clock cycle	t_{CLK}		500		350		ns
CLK H pulse width	t_{WH}		220		155		ns
CLK L pulse width	t_{WL}		220		155		ns
CLK rise and fall time	t_{RF}			60		40	ns
CLK setup time	t_{CLKS}		50		25		ns
CE setup time	t_{CS}		200		150		ns
CE hold time	t_{CH}		200		150		ns
CE recovery time	t_{CR}		300		200		ns
CE enable time	t_{WCE}			0.95		0.95	s
Write data setup time	t_{DS}		100		50		ns
Write data hold time	t_{DH}		100		50		ns
Read data delay time	t_{RD}	C_L=50 pF		200		150	ns
DO output switching time	t_{ZR}			50		20	ns
DO output disable time	t_{RZ}	C_L=50 pF R_L=10 kΩ		200		150	ns
DI/DO conflict avoiding time	t_{ZZ}		0		0		ns
FOUT duty	tw / t	50% V_{DD} level	40	60	40	60	%

Timing chart



∗ If DI and DO pins are wired-OR connected to make it to 3 lines form, secure tzz to avoid bus conflict.

8. Use Methods

8.1. Description of Registers

8.1.1. Write / Read and Bank Select

R/W and Register bank are specified by the four bits mode setting code.

Bank1: Basic time and calendar register.
Bank2: Extension register① … Adds 1/100s Counter.
Bank3: Extension register② … Capture buffer and Event control registers.

Mode	Bank 1	Bank 2	Bank 3
Read	9 h	A h	B h
Write	1 h	2 h	3 h

The register of the same name of Bank1 and Bank2 is the same register.

8.1.2. Register table (Bank1)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
0	SEC	○	40	20	10	8	4	2	1	P	P
1	MIN	○	40	20	10	8	4	2	1	P	P
2	HOUR	○	○	20	10	8	4	2	1	P	P
3	WEEK	○	6	5	4	3	2	1	0	P	P
4	DAY	○	○	20	10	8	4	2	1	P	P
5	MONTH	○	○	○	10	8	4	2	1	P	P
6	YEAR	80	40	20	10	8	4	2	1	P	P
7	RAM	•	•	•	•	•	•	•	•	P	P
8	MIN Alarm	AE	40	20	10	8	4	2	1	P	P
9	HOUR Alarm	AE	•	20	10	8	4	2	1	P	P
A	WEEK Alarm	AE	6	5	4	3	2	1	0	P	P
	DAY Alarm		•	20	10	8	4	2	1		
B	Timer Counter 0	128	64	32	16	8	4	2	1	P	P
C	Timer Counter 1	•	•	•	•	2048	1024	512	256	P	P
D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	P	P
E	Flag Register	○	○	UF	TF	AF	EVF	VLF	VDET	P	P
F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	EIE	○	RESET	P	P

P : Possible , I : Impossible

Note When after the initial power-up or when the result of read out the VLF bit is "1" , initialize all registers, before using the module.
Be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the data or time data is incorrect.

∗1) During the initial power-up, the TEST bit is reset to "0" and the VLF bit is set to "1".
∗ At this point, all other register values are undefined, so be sure to perform a reset before using the module.

∗2) Only a "0" can be written to the UF, TF, AF, VLF, or VDET bit.

∗3) Any bit marked with "○" should be used with a value of "0" after initialization.

∗4) Any bit marked with "•" is a RAM bit that can be used to read or write any data.

∗5) The TEST bit is used by the manufacturer for testing. Be sure to set "0" for this bit when writing.

8.1.3. Register table (Bank2)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
0	1/100 S	80	40	20	10	8	4	2	1	P	I
1	SEC	○	40	20	10	8	4	2	1	P	P
2	MIN	○	40	20	10	8	4	2	1	P	P
3	HOUR	○	○	20	10	8	4	2	1	P	P
4	WEEK	○	6	5	4	3	2	1	0	P	P
5	DAY	○	○	20	10	8	4	2	1	P	P
6	MONTH	○	○	○	10	8	4	2	1	P	P
7	YEAR	80	40	20	10	8	4	2	1	P	P
8	MIN Alarm	AE	40	20	10	8	4	2	1	P	P
9	HOUR Alarm	AE	•	20	10	8	4	2	1	P	P
A	WEEK Alarm	AE	6	5	4	3	2	1	0	P	P
	DAY Alarm		•	20	10	8	4	2	1		
B	Timer Counter 0	128	64	32	16	8	4	2	1	P	P
C	Timer Counter 1	•	•	•	•	2048	1024	512	256	P	P
D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	P	P
E	Flag Register	○	○	UF	TF	AF	EVF	VLF	VDET	P	P
F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	EIE	○	RESET	P	P

1/100S Reg. is cleared to "00" by writing in the SEC Reg. or RESET bit and the ERST bit operation.

8.1.4. Register table (Bank3)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
0	1/100 S CP	80	40	20	10	8	4	2	1	P	I
1	SEC CP	○	40	20	10	8	4	2	1	P	I
2	–	–	–	–	–	–	–	–	–	–	–
3	–	–	–	–	–	–	–	–	–	–	–
4	–	–	–	–	–	–	–	–	–	–	–
5	–	–	–	–	–	–	–	–	–	–	–
6	–	–	–	–	–	–	–	–	–	–	–
7	–	–	–	–	–	–	–	–	–	–	–
8	–	–	–	–	–	–	–	–	–	–	–
9	–	–	–	–	–	–	–	–	–	–	–
A	–	–	–	–	–	–	–	–	–	–	–
B	–	–	–	–	–	–	–	–	–	–	–
C	OSC Offset	○	○	○	○	OFS3	OFS2	OFS1	OFS0	P	P
D	–	–	–	–	–	–	–	–	–	–	–
E	–	–	–	–	–	–	–	–	–	–	–
F	Event Control	ECP	EHL	ET1	ET0	○	○	○	ERST	P	P

When an initial power on, frequency offset is ±0 selected by "0000".

8.2. Details of Registers

It explains each register based on Bank2.

8.2.1. Clock counter (1/100S, SEC - HOUR)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	1/100 S	80	40	20	10	8	4	2	1
1	SEC	○	40	20	10	8	4	2	1
2	MIN	○	40	20	10	8	4	2	1
3	HOUR	○	○	20	10	8	4	2	1

*) "o" indicates write-protected bits. A zero is always read from these bits.

- The clock counter counts 1/100s, seconds, minutes, and hours.
- The data format is BCD format. For example, when the "seconds" register value is "0101 1001" it indicates 59 seconds.

* Note with caution that writing non-existent time data may interfere with normal operation of the clock counter.

1) 1/100 Second counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	1/100 S	80	40	20	10	8	4	2	1

- This second counter counts from "00" to "01," "02," and up to 99/100 seconds, after which it starts again from 00 seconds.

2) Second counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	SEC	○	40	20	10	8	4	2	1

- This second counter counts from "00" to "01," "02," and up to 59 seconds, after which it starts again from 00 seconds.

3) Minute counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
2	MIN	○	40	20	10	8	4	2	1

- This minute counter counts from "00" to "01," "02," and up to 59 minutes, after which it starts again from 00 minutes.

4) Hour counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
3	HOUR	○	○	20	10	8	4	2	1

- This hour counter counts from "00" hours to "01," "02," and up to 23 hours, after which it starts again from 00 hours.

8.2.2. Calendar counter (WEEK - YEAR)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
4	WEEK	○	6	5	4	3	2	1	0

*) "o" indicates write-protected bits. A zero is always read from these bits.

1) Day of the WEEK counter

- The day (of the week) is indicated by 7 bits, bit 0 to bit 6.
  The day data values are counted as: Day 01h → Day 02h → Day 04h → Day 08h → Day 10h → Day 20h → Day 40h → Day 01h → Day 02h, etc.
- The correspondence between days and count values is shown below.

WEEK	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Day	Data [h]
Write/Read	0	0	0	0	0	0	0	**1**	Sunday	01 h
	0	0	0	0	0	0	**1**	0	Monday	02 h
	0	0	0	0	0	**1**	0	0	Tuesday	04 h
	0	0	0	0	**1**	0	0	0	Wednesday	08 h
	0	0	0	**1**	0	0	0	0	Thursday	10 h
	0	0	**1**	0	0	0	0	0	Friday	20 h
	0	**1**	0	0	0	0	0	0	Saturday	40 h
Write prohibit	* Do not set "1" to more than one day at the same time. Also, note with caution that any setting other than the seven shown above should not be made as it may interfere with normal operation.								–	–

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
5	DAY	○	○	20	10	8	4	2	1
6	MONTH	○	○	○	10	8	4	2	1
7	YEAR	80	40	20	10	8	4	2	1

*) "o" indicates write-protected bits. A zero is always read from these bits.

- The auto calendar function updates all dates, months, and years from January 1, 2001 to December 31, 2099.
- The data format is BCD format. For example, a date register value of "0011 0001" indicates the 31st.

* Note with caution that writing non-existent date data may interfere with normal operation of the calendar counter.

2) Date counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
4	DAY	○	○	20	10	8	4	2	1

- The updating of dates by the date counter varies according to the month setting.

* A leap year is set whenever the year value is a multiple of four (such as 04, 08, 12, 88, 92, or 96). In February of a leap year, the counter counts dates from "01," "02," "03," to "28," "29," "01," etc.

DAY	Month	Date update pattern
Write/Read	1, 3, 5, 7, 8, 10, or 12	01, 02, 03 ~ 30, 31, 01 ~
	4, 6, 9, or 11	01, 02, 03 ~ 30, 01, 02 ~
	February in normal year	01, 02, 03 ~ 28, 01, 02 ~
	February in leap year	01, 02, 03 ~ 28, 29, 01 ~

3) Month counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
5	MONTH	○	○	○	10	8	4	2	1

- The month counter counts from 01 (January), 02 (February), and up to 12 (December), then starts again at 01 (January).

4) Year counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
6	YEAR	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1

- The year counter counts from 00, 01, 02 and up to 99, then starts again at 00.
- Any year that is a multiple of four (04, 08, 12, 88, 92, 96, etc.) is handled as a leap year.

8.2.3. Alarm registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
8	MIN Alarm	AE	40	20	10	8	4	2	1
9	HOUR Alarm	AE	•	20	10	8	4	2	1
A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1

- The alarm interrupt function is used, along with the AEI, AF, and WADA bits, to set alarms for specified date, day, hour, and minute values.
- When the settings in the above alarm registers and the WADA bit match the current time, the /INT pin goes to low level and "1" is set to the AF bit to report that and alarm interrupt event has occurred.

8.2.4. Fixed-cycle timer control registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
B	Timer Counter 0	128	64	32	16	8	4	2	1
C	Timer Counter 1	•	•	•	•	2048	1024	512	256

- These registers are used to set the preset countdown value for the fixed-cycle timer interrupt function. The TE, TF, TIE, and TSEL0/1 bits are also used to set the fixed-cycle timer interrupt function.
- When the value in the above fixed-cycle timer control register changes from 001h to 000h, the /INT pin goes to low level and "1" is set to the TF bit to report that a fixed-cycle timer interrupt event has occurred.

8.2.5. Extension register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
D	Extension Register (Default)	TEST (0)	WADA (–)	USEL (–)	TE (–)	FSEL1 (0)	FSEL0 (0)	TSEL1 (–)	TSEL0 (–)

∗1) The default value is the value that is read (or is set internally) after powering up from 0 V.

∗2) "o" indicates write-protected bits. A zero is always read from these bits.

∗3) "–" indicates a default value is undefined.

- This register is used to specify the target for the alarm function or time update interrupt function and to select or set operations such as fixed-cycle timer operations.

1) TEST bit

This is the manufacturer's test bit. Its value should always be "0".
Be careful to avoid writing a "1" to this bit when writing to other bits.

TEST	Data	Description
Write/Read	0	Normal operation mode ∗ Default
	1	Setting prohibited (manufacturer's test bit)

2) WADA (Week Alarm/Day Alarm) bit

This bit is used to specify either WEEK or DAY as the target of the alarm interrupt function.
Writing a "1" to this bit specifies DAY as the comparison obLCct for the alarm interrupt function.
Writing a "0" to this bit specifies WEEK as the comparison obLCct for the alarm interrupt function.

3) USEL (Update Interrupt Select) bit

This bit is used to specify either "second update" or "minute update" as the update generation timing of the time update interrupt function.

USEL	Data	update interrupts	Auto reset time tRTN
Write/Read	0	second update ∗ Default	500 ms
	1	minute update	7.813 ms

4) TE (Timer Enable) bit

This bit controls the start/stop setting for the fixed-cycle timer interrupt function.
Writing a "1" to this bit specifies starting of the fixed-cycle timer interrupt function (a countdown starts from a preset value).
Writing a "0" to this bit specifies stopping of the fixed-cycle timer interrupt function.

5) FSEL0,1 (FOUT frequency Select 0, 1) bits
The combination of these two bits is used to set the FOUT frequency.

FSEL0,1	FSEL1 (bit 3)	FSEL0 (bit 2)	FOUT frequency
Write/Read	0	0	32768 Hz Output ∗ Default
	0	1	1024 Hz Output
	1	0	1 Hz Output
	1	1	32768 Hz Output

6) TSEL0,1 (Timer Select 0, 1) bits
The combination of these two bits is used to set the countdown period (source clock) for the fixed-cycle timer interrupt function (four settings can be made).

TSEL0,1	TSEL1 (bit 1)	TSEL0 (bit 0)	Source clock
Write/Read	0	0	4096 Hz / Once per 244.14 μs
	0	1	64 Hz / Once per 15.625 ms
	1	0	"Second" update / Once per second
	1	1	"Minute" update / Once per minute

8.2.6. Flag register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
E	Flag register (Default)	○ (0)	○ (0)	UF (–)	TF (–)	AF (–)	EVF (0)	VLF (1)	VDET (1)

∗1) The default value is the value that is read (or is set internally) after powering up from 0 V.
∗2) "o" indicates write-protected bits. A zero is always read from these bits.
∗3) "–" indicates a default value is undefined.

- This register is used to detect the occurrence of various interrupt events and reliability problems in internal data.

1) UF (Update Flag) bit
If set to "0" beforehand, this flag bit's value changes from "0" to 1" when a time update interrupt event has occurred. Once this flag bit's value is "1", its value is retained until a "0" is written to it.
∗ For details, see "8.4. Time Update Interrupt Function".

2) TF (Timer Flag) bit
If set to "0" beforehand, this flag bit's value changes from "0" to 1" when a fixed-cycle timer interrupt event has occurred. Once this flag bit's value is "1", its value is retained until a "0" is written to it.
∗ For details, see "8.3. Fixed-cycle Timer Interrupt Function".

3) AF (Alarm Flag) bit
If set to "0" beforehand, this flag bit's value changes from "0" to 1" when an alarm interrupt event has occurred. Once this flag bit's value is "1", its value is retained until a "0" is written to it.
∗ For details, see "8.5. Alarm Interrupt Function".

4) EVF (Event Flag) bit
If set to "0" beforehand, this flag bit's value changes from "0" to 1" when a event input interrupt has occurred. Once this flag bit's value is "1", its value is retained until a "0" is written to it.

5) VLF (Voltage Low Flag) bit
This flag bit indicates the retained status of clock operations or internal data. Its value changes from "0" to "1" when data loss occurs, such as due to a supply voltage drop. Once this flag bit's value is "1", its value is retained until a "0" is written to it.
When after powering up from 0 V this bit's value is "1" .

VLF	Data	Description
Write	0	The VLF bit is cleared to zero to prepare for the next status detection.
	1	This bit is invalid after a "1" has been written to it.
Read	0	Data loss is not detected.
	1	Data loss is detected. All registers must be initialized. (This setting is retained until a "zero" is written to this bit.)

5) VDET (Voltage Detection Flag) bit

This flag bit indicates the status of temperature compensation. Its value changes from "0" to "1" when stop the temperature compensation, such as due to a supply voltage drop. Once this flag bit's value is "1", its value is retained until a "0" is written to it.

When after powering up from 0 V this bit's value is "1".

VDET	Data	Description
Write	0	The VDET bit is cleared to zero to prepare for the next low voltage detection.
	1	The write access of "1" to this bit is invalid.
Read	0	Temperature compensation is normal.
	1	Temperature compensation is stop detected.

8.2.7. Control register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
F	Control Register (Default)	CSEL1 (0)	CSEL0 (1)	UIE (–)	TIE (–)	AIE (–)	EIE (0)	○ (0)	RESET (–)

∗1) The default value is the value that is read (or is set internally) after powering up from 0 V.

∗2) "o" indicates write-protected bits. A zero is always read from these bits.

∗3) "–" indicates no default value has been defined.

- This register is used to control interrupt event output from the /INT pin and the stop/start status of clock and calendar operations.

1) CSEL0,1 (Compensation interval Select 0, 1) bits

The combination of these two bits is used to set the temperature compensation interval.

CSEL0,1	CSEL1 (bit 7)	CSEL0 (bit 6)	Compensation interval	
Write/Read	0	0	0.5 s	
	0	1	2.0 s	∗ Default
	1	0	10 s	
	1	1	30 s	

2) UIE (Update Interrupt Enable) bit

When a time update interrupt event is generated (when the UF bit value changes from "0" to "1"), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.

When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

UIE	Data	Function
Write/Read	0	When a time update interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status changes from low to Hi-Z).
	1	When a time update interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). * When a time update interrupt event occurs, low-level output from the /INT pin occurs only when the value of the control register's UIE bit is "1". This /INT status is automatically cleared (/INT status changes from low to Hi-Z) 7.8 ms after the interrupt occurs.

2) TIE (Timer Interrupt Enable) bit

When a fixed-cycle timer interrupt event occurs (when the TF bit value changes from "0" to "1"), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.

When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

TIE	Data	Function
Write/Read	0	When a fixed-cycle timer interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status changes from low to Hi-Z).
	1	When a fixed-cycle timer interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). * When a fixed-cycle timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is "1". Up to 7.8 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi-Z).

3) AIE (Alarm Interrupt Enable) bit

When an alarm timer interrupt event occurs (when the AF bit value changes from "0" to "1"), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.

When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

AIE	Data	Function
Write/Read	0	When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status changes from low to Hi-Z).
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). * When an alarm interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's AIE bit is "1". This setting is retained until the AF bit value is cleared to zero. (No automatic cancellation)

* For details, see "8.5. Alarm Interrupt Function".

[Caution]

(1) The /INT pin is a shared interrupt output pin for three types of interrupts. It outputs the OR'ed result of these interrupt outputs. When an interrupt has occurred (when the /INT pin is at low level), the UF, TF, read AF flags to determine which flag has a value of "1" (this indicates which type of interrupt event has occurred).

(2) To keep the /INT pin from changing to low level, write "0" to the UIE, TIE, and AIE bits. To check whether an event has occurred without outputting any interrupts via the /INT pin, use software to monitor the value of the UF, TF, and AF interrupt flags.

4) EIE (Event Interrupt Enable) bit

When a Event input is generated (when the EVF bit value changes from "0" to "1"), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z). When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.

When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

5) RESET bit

When this bit is set to "1", values (less than seconds) of the counter in the Clock & Calendar circuitry is reset, and the clock also stops.

After "1" is written to this bit, this can be released by setting CE to "L".

8.2.8. OSC Offset Contorol (Reg -C / Bank 3)

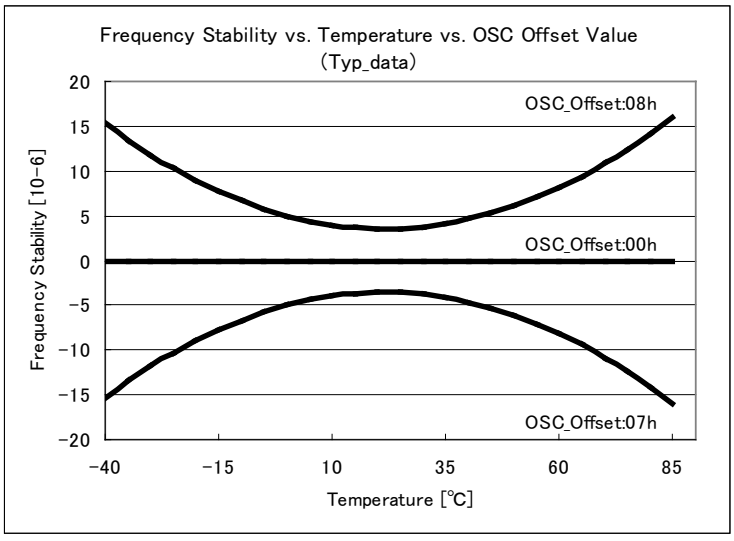
Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
C	OSC Offset	○	○	○	○	OFS3	OFS2	OFS1	OFS0

1) OFS bits (OFS3-OFS0)

The offset adjustment is done to the oscillation frequency.

OFS3	OFS2	OFS1	OFS0	Adjust value (x 10^{-6}) RA4803SA
0	0	0	0	± 0.0
0	0	0	1	−0.6
0	0	1	0	−1.2
0	0	1	1	−1.8
0	1	0	0	−2.4
0	1	0	1	−3.0
0	1	1	0	−3.6
0	1	1	1	−4.2
1	0	0	0	+4.8
1	0	0	1	+4.2
1	0	1	0	+3.6
1	0	1	1	+3.0
1	1	0	0	+2.4
1	1	0	1	+1.8
1	1	1	0	+1.2
1	1	1	1	+0.6

*The OFS register affects the frequency stability. Please refer to a lower graph.
Please be careful if you offset and adjust it.
The offset function is effective for frequency adjustment at the normal temperature.



8.2.9. Capture Buffer / Event control (Bank 3)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	1/100 S CP	80	40	20	10	8	4	2	1
1	SEC CP	○	40	20	10	8	4	2	1
F	Event Control	ECP	EHL	ET1	ET0	○	○	○	ERST

It is a register that sets it concerning the event detection.

1) ECP bit (Event Capture enable)

It is specified whether to do the second and 1/100S data to the capture buffer in capture when the event is detected.

ECP	Operation
0	Capture doesn't operate
1	Capture operation

2) EHL bit (High/Low detection select)

The disregard level of the event input is specified.

The event is detected by maintaining the level specified by the EHL bit longer than the chattering removal cycle.

EHL	Operation
0	"L" level detect
1	"H" level detect

3) ET1,ET0 bits (Event chattering Time Set)

The removal cycle of the chattering removal function is set.

・Chattering removal cycle

ET1	ET0	Cycle
0	0	not provided
0	1	3.9 ms
1	0	15.6 ms
1	1	125 ms

4) ERST bit

When this bit is made "1", the counter of the Clock&Calendar circuit (counter for 16KHz to 2Hz and 1/100 seconds) at less than second is reset synchronizing with the external event detection.

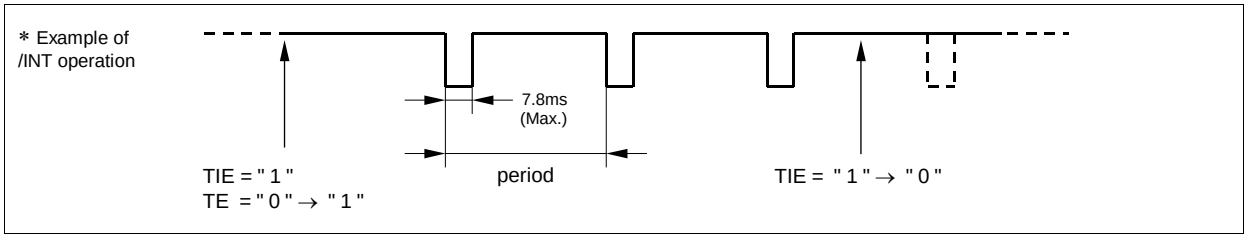
ALL "0" is cleared to CP and the CP register of the second at the same time for 1/100 seconds.

Timing continues until the event is generated after "1" is written in the ERST bit.
The counter at less than second when an external event is detected is reset, and the ERST bit is cleared.
Moreover, it is also possible to assume this reset action to be invalid by doing "0" writing directly to the ERST bit before the event is generated.

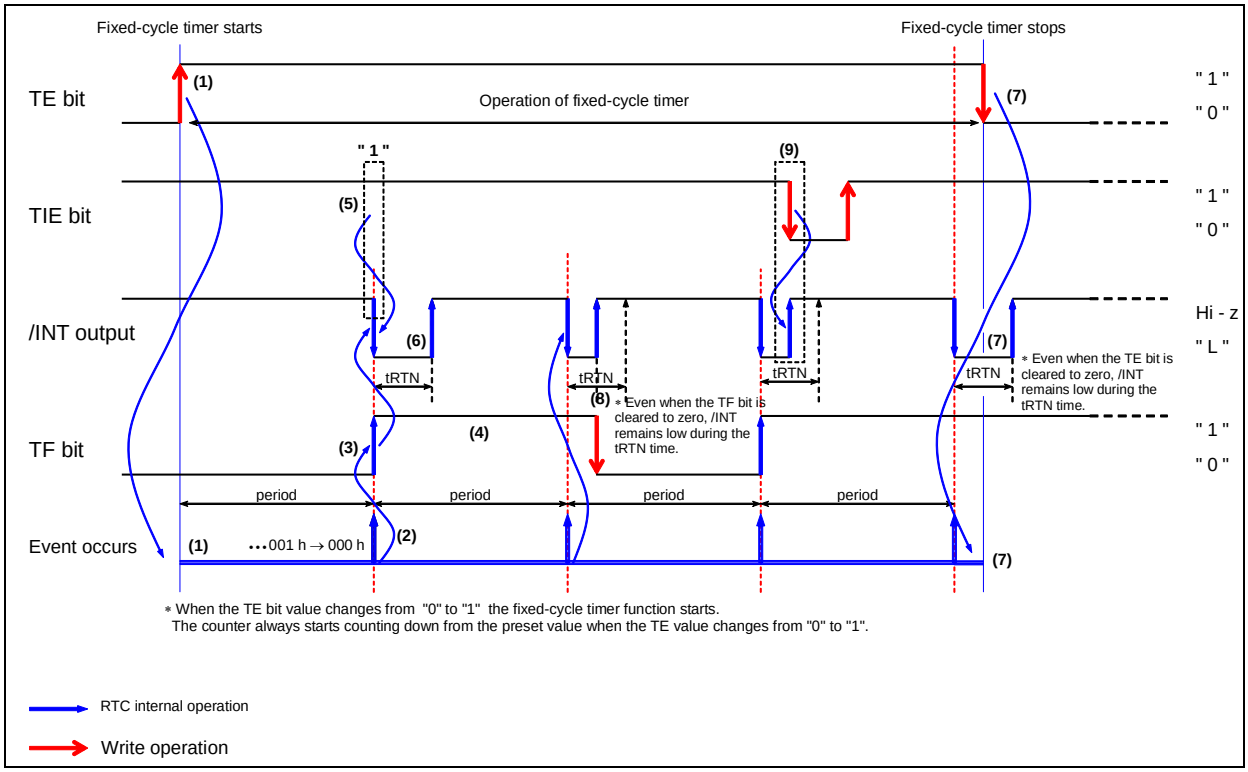
When the highly accurate time suiting is done, this bit is used.
The time for the counter at less than second to be reset influences the operation of the alarm, the fixed cycle timer, and the update interrupt of time, etc.

8.3. Fixed-cycle Timer Interrupt Function

The fixed-cycle timer interrupt generation function generates an interrupt event periodically at any fixed cycle set between 244.14 μs and 4095 minutes.
When an interrupt event is generated, the /INT pin goes to low level and "1" is set to the TF bit to report that an event has occurred. (However, when a fixed-cycle timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is "1". Up to 7.8 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low-level to Hi-Z).



8.3.1. Diagram of fixed-cycle timer interrupt function



(1) When a "1" is written to the TE bit, the fixed-cycle timer countdown starts from the preset value.

(2) A fixed-cycle timer interrupt event starts a countdown based on the countdown period (source clock). When the count value changes from 001h to 000h, an interrupt event occurs.
∗ After the interrupt event that occurs when the count value changes from 001h to 000h, the counter automatically reloads the preset value and again starts to count down. (Repeated operation)

(3) When a fixed-cycle timer interrupt event occurs, "1" is written to the TF bit.

(4) When the TF bit = "1" its value is retained until it is cleared to zero.

(5) If the TIE bit = "1" when a fixed-cycle timer interrupt occurs, /INT pin output goes low.
∗ If the TIE bit = "0" when a fixed-cycle timer interrupt occurs, /INT pin output remains Hi-Z.

(6) Output from the /INT pin remains low during the tRTN period following each event, after which it is automatically cleared to Hi-Z status.
∗ /INT is again set low when the next interrupt event occurs.

(7) When a "0" is written to the TE bit, the fixed-cycle timer function is stopped and the /INT pin is set to Hi-Z status.
∗ When /INT = low, the fixed-cycle timer function is stopped. The tRTN period is the maximum amount of time before the /INT pin status changes from low to Hi-Z.

(8) When /INT = low, the /INT pin status changes from low to Hi-Z as soon as the TF bit value changes from "1" to "0".

(9) When /INT = low, the /INT pin status changes from low to Hi-Z as soon as the TIE bit value changes from "1" to "0".

8.3.2. Related registers for function of time update interrupts.

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
B	Timer Counter 0	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
C	Timer Counter 1	•	•	•	•	**2048**	**1024**	**512**	**256**
D	Extension Register	TEST	WADA	USEL	**TE**	FSEL1	FSEL0	**TSEL1**	**TSEL0**
E	Flag Register	○	○	UF	**TF**	AF	EVF	VLF	VDET
F	Control Register	CSEL1	CSEL0	UIE	**TIE**	AIE	EIE	○	RESET

∗1) "o" indicates write-protected bits. A zero is always read from these bits.

∗2) Bits marked with "•" are RAM bits that can contain any value and are read/write-accessible.

∗ Before entering settings for operations, we recommend writing a "0" to the TE and TIE bits to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the RESET bit value is "1" the time update interrupt function operates only partially.
(Operation continues if the source clock setting is 4096 Hz. Otherwise, operation is stopped.)

∗ When the fixed-cycle timer interrupt function is not being used, the fixed-cycle timer control register (Reg – B to C) can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

1) TSEL0,1 bits (Timer Select 0, 1)
The combination of these two bits is used to set the countdown period (source clock) for the fixed-cycle timer interrupt function (four settings can be made).

TSEL0,1	TSEL1 (bit 1)	TSEL0 (bit 0)	Source clock	Auto reset time tRTN	Effects of RESET bits
Write/Read	0	0	4096 Hz / Once per 244.14 μs	122 μs	–
	0	1	64 Hz / Once per 15.625 ms	7.8125 ms	∗ Does not operate when the RESET bit value is "1".
	1	0	"Second" update / Once per second	7.8125 ms	
	1	1	"Minute" update / Once per minute	7.8125 ms	

∗1) The /INT pin's auto reset time (tRTN) varies as shown above according to the source clock setting.
∗2) When the source clock has been set to "second update" or "minute update", the timing of both countdown and interrupts is coordinated with the clock update timing.

2) Fixed-cycle Timer Control register (Reg - B to C)
This register is used to set the default (preset) value for the counter. Any count value from 1 (001 h) to 4095 (FFFh) can be set. The counter counts down based on the source clock's period, and when the count value changes from 001h to 000h, the TF bit value becomes "1".
The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value. Be sure to write "0" to the TE bit before writing the preset value. If a value is written while TE = "1" the first subsequent event will not be generated correctly.

Address C Timer Counter 1								Address B Timer Counter 0							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
•	•	•	•	2048	1024	512	256	128	64	32	16	8	4	2	1

3) TE (Timer Enable) bit
This bit controls the start/stop setting for the fixed-cycle timer interrupt function.

TE	Data	Description
Write/Read	0	Stops fixed-cycle timer interrupt function.
	1	Starts fixed-cycle timer interrupt function. ∗ The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value.

4) TF (Timer Flag) bit
If set to "0" beforehand, this flag bit's value changes from "0" to 1" when a fixed-cycle timer interrupt event has occurred. Once this flag bit's value is "1", its value is retained until a "0" is written to it.

TF	Data	Description
Write	0	The TF bit is cleared to zero to prepare for the next status detection ∗ Clearing this bit to zero enables /INT low output to be canceled (/INT remains Hi-Z) when timer interrupt event has occurred.
	1	This bit is invalid after a "1" has been written to it.
Read	0	Fixed-cycle timer interrupt events are not detected.
	1	Fixed-cycle timer interrupt events are detected. (Result is retained until this bit is cleared to zero.)

5) TIE (Timer Interrupt Enable) bit
When a fixed-cycle timer interrupt event occurs (when the TF bit value changes from "0" to "1"), this bit's value specifies whether an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

TIE	Data	Description
Write/Read	0	1) When a fixed-cycle timer interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z). 2) When a fixed-cycle timer interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z). * Even when the TIE bit value is "0" another interrupt event may change the /INT status to low (or may hold /INT = "L").
	1	When a fixed-cycle timer interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). * When a fixed-cycle timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is "1". Up to 7.8 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi-Z).

8.3.3. Fixed-cycle timer interrupt interval (example)

Timer Counter setting	Source clock			
	4096 Hz TSEL1,0 = 0,0	64 Hz TSEL1,0 = 0,1	"Second" update TSEL1,0 = 1,0	"Minute" update TSEL1,0 = 1,1
0	–	–	–	–
1	244.14 μs	15.625 ms	1 s	1 min
2	488.28 μs	31.25 ms	2 s	2 min
⋮	⋮	⋮	⋮	⋮
41	10.010 ms	640.63 ms	41 s	41 min
205	50.049 ms	3.203 s	205 s	205 min
410	100.10 ms	6.406 s	410 s	410 min
2048	500.00 ms	32.000 s	2048 s	2048 min
⋮	⋮	⋮	⋮	⋮
4095	0.9998 s	63.984 s	4095 s	4095 min

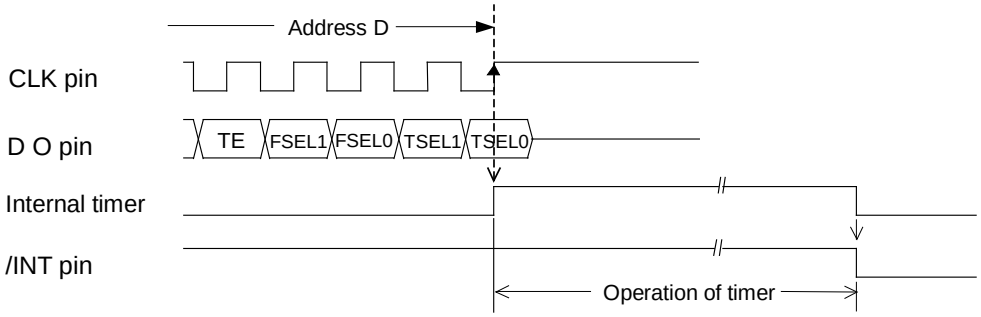
- Time error in fixed-cycle timer
  A time error in the fixed-cycle timer will produce a positive or negative time period error in the selected source clock. The fixed-cycle timer's time is within the following range relative to the time setting.

(Fixed-cycle timer's time setting (*) – source clock period) to (timer's time setting)
*) The timer's time setting = source clock period × timer counter's division value.

* The time actually set to the timer is adjusted by adding the time described above to the communication time for the serial data transfer clock used for the setting.

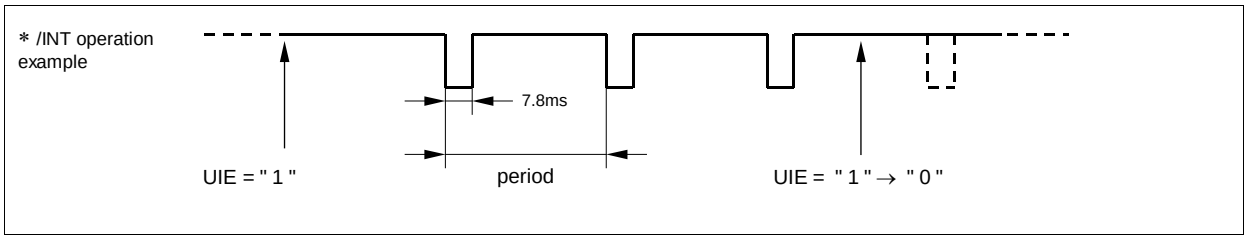
8.3.4. Fixed-cycle timer start timing

Counting down of the fixed-cycle timer value starts at the rising edge of the CLK signal that occurs when the TE value is changed from "0" to "1" (after bit 0 is transferred).

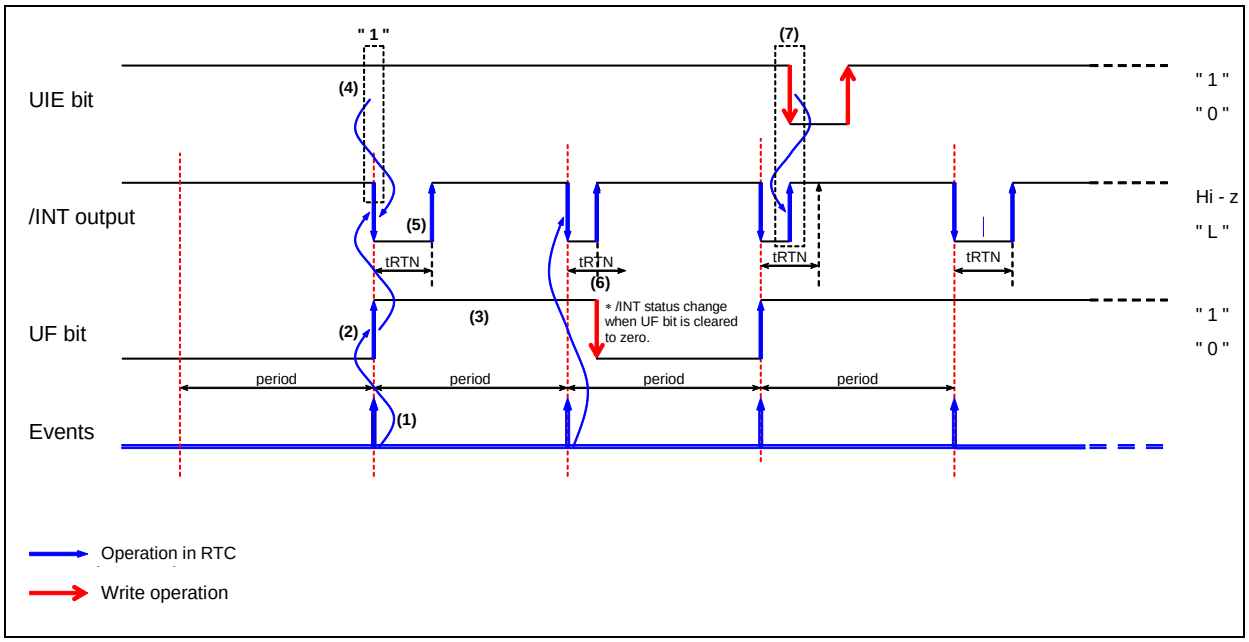


8.4. Time Update Interrupt Function

The time update interrupt function generates interrupt events at one-second or one-minute intervals, according to the timing of the internal clock.
When an interrupt event occurs, the UF bit value becomes "1" and the /INT pin goes to low level to indicate that an event has occurred. (However, when a fixed-cycle timer interrupt event has been generated, low-level output from the /INT pin occurs only when the value of the control register's UIE bit is "1". This /INT status is automatically cleared (/INT status changes from low level to Hi-Z) 7.8 ms (fixed value) after the interrupt occurs.



8.4.1. Time update interrupt function diagram



(1) A time update interrupt event occurs when the internal clock's value matches either the second update time or the minute update time. The USEL bit's specification determines whether it is the second update time or the minute update time that must be matched.

(2) When a time update interrupt event occurs, the UF bit value becomes "1".

(3) When the UF bit value is "1" its value is retained until it is cleared to zero.

(4) When a time update interrupt occurs, /INT pin output is low if UIE = "1".
∗ If UIE = "0" when a timer update interrupt occurs, the /INT pin status remains Hi-Z.

(5) Each time an event occurs, /INT pin output is low only up to the tRTN time (which is fixed as 7.1825 ms for time update interrupts) after which it is automatically cleared to Hi-Z.
∗ /INT pin output goes low again when the next interrupt event occurs.

(6) When /INT = low, the /INT pin status changes from low to Hi-Z as soon as the UF bit value changes from "1" to "0".

(7) When /INT = low, the /INT pin status changes from low to Hi-Z as soon as the UIE bit value changes from "1" to "0".

8.4.2. Related registers for time update interrupt functions.

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
D	Extension Register	TEST	WADA	**USEL**	TE	FSEL1	FSEL0	TSEL1	TSEL0
E	Flag Register	○	○	**UF**	TF	AF	EVF	VLF	VDET
F	Control Register	CSEL1	CSEL0	**UIE**	TIE	AIE	EIE	○	RESET

*) "o" indicates write-protected bits. A zero is always read from these bits.

* Before entering settings for operations, we recommend writing a "0" to the UIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

* When the RESET bit value is "1" time update interrupt events do not occur.

* Although the time update interrupt function cannot be fully stopped, if "0" is written to the UIE bit, the time update interrupt function can be prevented from changing the /INT pin status to low.

1) USEL (Update Interrupt Select) bit
This bit is used to select "second" update or "minute" update as the timing for generation of time update interrupt events.

USEL	Data	Description
Write/Read	0	Selects "second update" (once per second) as the timing for generation of interrupt events
	1	Selects "minute update" (once per minute) as the timing for generation of interrupt events

2) UF (Update Flag) bit
Once it has been set to "0", this flag bit value changes from "0" to "1" when a time update interrupt event occurs. When this flag bit = "1" its value is retained until a "0" is written to it.

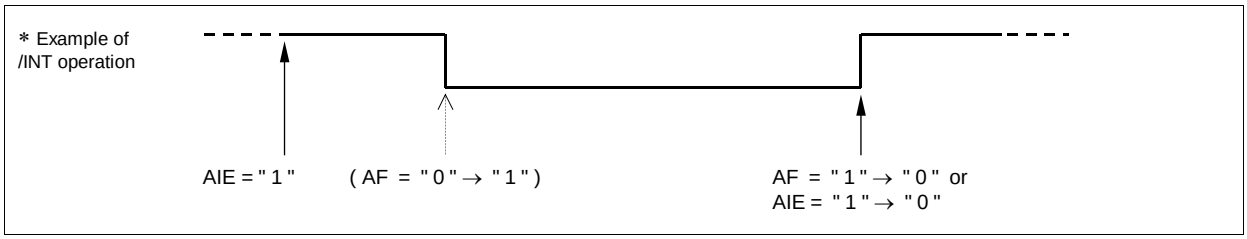
UF	Data	Description
Write	0	The UF bit is cleared to zero to prepare for the next status detection * Clearing this bit to zero does not enable the /INT low output status to be cleared (to Hi-Z).
	1	This bit is invalid after a "1" has been written to it.
Read	0	Time update interrupt events are not detected.
	1	Time update interrupt events are detected. (The result is retained until this bit is cleared to zero.)

3) UIE (Update Interrupt Enable) bit
When a time update interrupt event occurs (UF bit value changes from "0" to "1"), this bit selects whether to generate an interrupt signal (/INT status changes from Hi-Z to low) or to not generate it (/INT status remains Hi-Z).

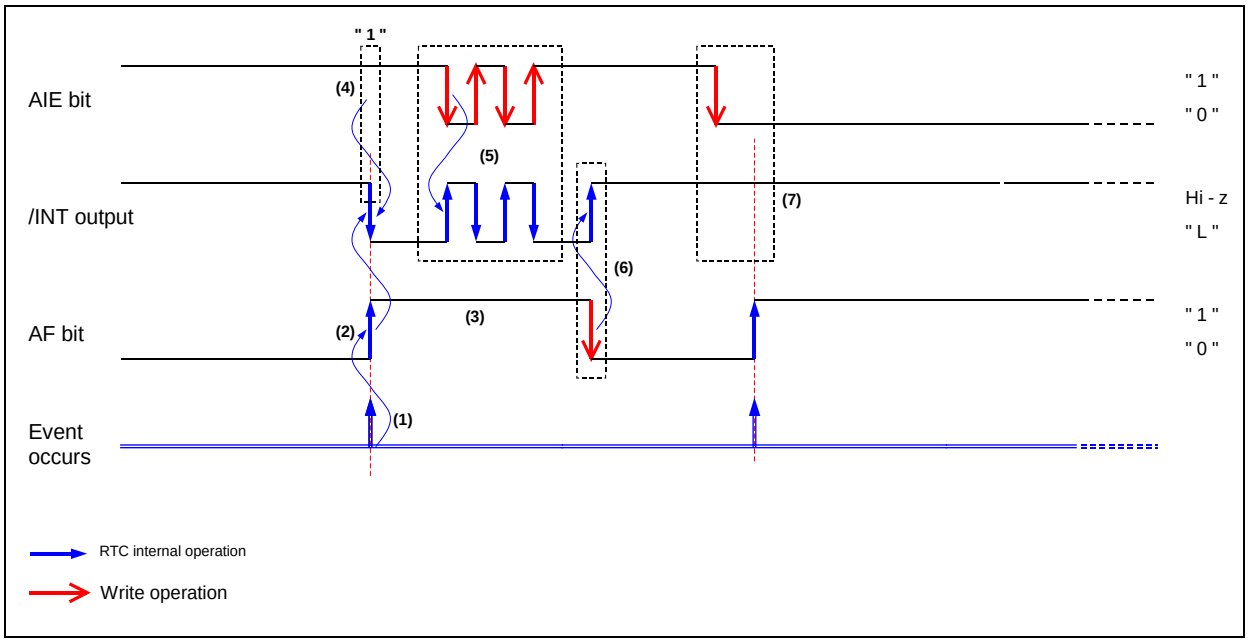
UIE	Data	Description
Write/Read	0	1) Does not generate an interrupt signal when a time update interrupt event occurs (/INT remains Hi-Z) 2) Cancels interrupt signal triggered by time update interrupt event (/INT changes from low to Hi-Z). * Even when the UIE bit value is "0" another interrupt event may change the /INT status to low (or may hold /INT = "L").
	1	When a time update interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). * When a time update interrupt event occurs, low-level output from the /INT pin occurs only when the UIE bit value is "1". Up to 7.8 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi-Z).

8.5. Alarm Interrupt Function

The alarm interrupt generation function generates interrupt events for alarm settings such as date, day, hour, and minute settings.
When an interrupt event occurs, the AF bit value is set to "1" and the /INT pin goes to low level to indicate that an event has occurred.



8.4.1. Diagram of alarm interrupt function



(1) The hour, minute, date or day when an alarm interrupt event is to occur is set in advance along with the WADA bit, and when the setting matches the current time an interrupt event occurs.
(Note) Even if the current date/time is used as the setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).

(2) When a time update interrupt event occurs, the AF bit values becomes "1".

(3) When the AF bit = "1", its value is retained until it is cleared to zero.

(4) If AIE = "1" when an alarm interrupt occurs, the /INT pin output goes low.
* When an alarm interrupt event occurs, /INT pin output goes low, and this status is then held until it is cleared via the AF bit or AIE bit.

(5) If the AIE value is changed from "1" to "0" while /INT is low, the /INT status immediately changes from low to Hi-Z. After the alarm interrupt occurs and before the AF bit value is cleared to zero, the /INT status can be controlled via the AIE bit.

(6) If the AF bit value is changed from "1" to "0" while /INT is low, the /INT status immediately changes from low to Hi-Z.

(7) If the AIE bit value is "0" when an alarm interrupt occurs, the /INT pin status remains Hi-Z.

8.5.2. Related registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	MIN	○	40	20	10	8	4	2	1
2	HOUR	○	○	20	10	8	4	2	1
3	WEEK	○	6	5	4	3	2	1	0
4	DAY	○	○	20	10	8	4	2	1
8	MIN Alarm	**AE**	40	20	10	8	4	2	1
9	HOUR Alarm	**AE**	•	20	10	8	4	2	1
A	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
E	Flag Register	○	○	UF	TF	**AF**	EVF	VLF	VDET
F	Control Register	CSEL1	CSEL0	UIE	TIE	**AIE**	EIE	○	RESET

∗1) "o" indicates write-protected bits. A zero is always read from these bits.

∗2) Bits marked with "•" are RAM bits that can contain any value and are read/write-accessible.

∗ Before entering settings for operations, we recommend writing a "0" to the AIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the RESET bit value is "1" alarm interrupt events do not occur.

∗ When the alarm interrupt function is not being used, the Alarm registers (Reg - 8 to A) can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.

∗ When the AIE bit value is "1" and the Alarm registers (Reg - 8 to A) is being used as a RAM register, /INT may be changed to low level unintentionally.

1) WADA (Week Alarm /Day Alarm) bit

The alarm interrupt function uses either "Day" or "Week" as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

WADA	Data	Description
Write/Read	0	Sets WEEK as target of alarm function (DAY setting is ignored)
	1	Sets DAY as target of alarm function (WEEK setting is ignored)

2) Alarm registers (Reg - 8 to A)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
8	MIN Alarm	AE	40	20	10	8	4	2	1
9	HOUR Alarm	AE	•	20	10	8	4	2	1
A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1

The hour, minute, date or day when an alarm interrupt event will occur is set using this register and the WADA bit.

In the WEEK alarm /Day alarm register (Reg - A), the setting selected via the WADA bit determines whether WEEK alarm data or DAY alarm data will be set. If WEEK has been selected via the WADA bit, multiple days can be set (such as Monday, Wednesday, Friday, Saturday).

When the settings made in the alarm registers and the WADA bit match the current time, the AF bit value is changed to "1". At that time, if the AIE bit value has already been set to "1", the /INT pin goes low.

∗1) The register that "1" was set to "AE" bit, doesn't compare alarm.
(Example) Write 80h (AE = "1") to the WEEK Alarm /DAY Alarm register (Reg - A):
Only the hour and minute settings are used as alarm comparison targets. The week and date settings are not used as alarm comparison targets.
As a result, alarm occurs if only an hour and minute accords with alarm data.

∗2) If all three AE bit values are "1" the week/date settings are ignored and an alarm interrupt event will occur once per minute.

3) AF (Alarm Flag) bit

When this flag bit value is already set to "0", occurrence of an alarm interrupt event changes it to "1". When this flag bit value is "1", its value is retained until a "0" is written to it.

AF	Data	Description
Write	0	The AF bit is cleared to zero to prepare for the next status detection * Clearing this bit to zero enables /INT low output to be canceled (/INT remains Hi-Z) when an alarm interrupt event has occurred.
	1	This bit is invalid after a "1" has been written to it.
Read	0	Alarm interrupt events are not detected.
	1	Alarm interrupt events are detected. (Result is retained until this bit is cleared to zero.)

4) AIE (Alarm Interrupt Enable) bit

When an alarm interrupt event occurs (when the AF bit value changes from "0" to "1"), this bit's value specifies whether an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

AIE	Data	Description
Write/Read	0	1) When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z). 2) When an alarm interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z). * Even when the AIE bit value is "0" another interrupt event may change the /INT status to low (or may hold /INT = "L").
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). * When an alarm interrupt event occurs, low-level output from the /INT pin occurs only when the AIE bit value is "1". This value is retained (not automatically cleared) until the AF bit is cleared to zero.

8.5.2. Examples of alarm settings

1) Example of alarm settings when "Day" has been specified (and WADA bit = "0")

Day is specified WADA bit = "0"	Reg – A bit 7 AE	bit 6 S	bit 5 F	bit 4 T	bit 3 W	bit 2 T	bit 1 M	bit 0 S	Reg - 9 HOUR Alarm	Reg - 8 MIN Alarm
Monday through Friday, at 7:00 AM * Minute value is ignored	0	0	1	1	1	1	1	0	07 h	80 h to FF h
Every Saturday and Sunday, for 30 minutes each hour * Hour value is ignored	0	1	0	0	0	0	0	1	80 h to FF h	30 h
Every day, at 6:59 AM	0	1	1	1	1	1	1	1	18 h	59 h
	1	X	X	X	X	X	X	X		

X: Don't care

2) Example of alarm settings when "Day" has been specified (and WADA bit = "1")

Day is specified WADA bit = "1"	Reg - A bit 7 AE	bit 6 •	bit 5 20	bit 4 10	bit 3 08	bit 2 04	bit 1 02	bit 0 01	Reg - 9 HOUR Alarm	Reg - 8 MIN Alarm
First of each month, at 7:00 AM * Minute value is ignored	0	0	0	0	0	0	0	1	07 h	80 h to FF h
15th of each month, for 30 minutes each hour * Hour value is ignored	0	0	0	1	0	1	0	1	80 h to FF h	30 h
Every day, at 6:59 PM	1	X	X	X	X	X	X	X	18 h	59 h

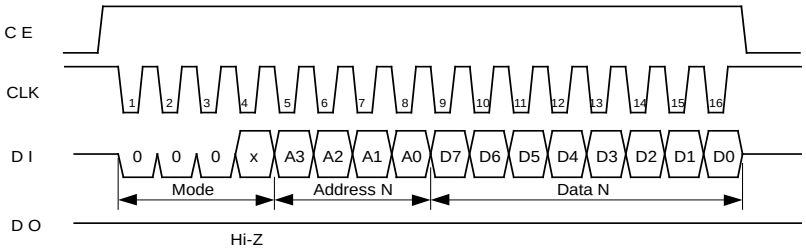
X: Don't care

8.6. Read/Write of data

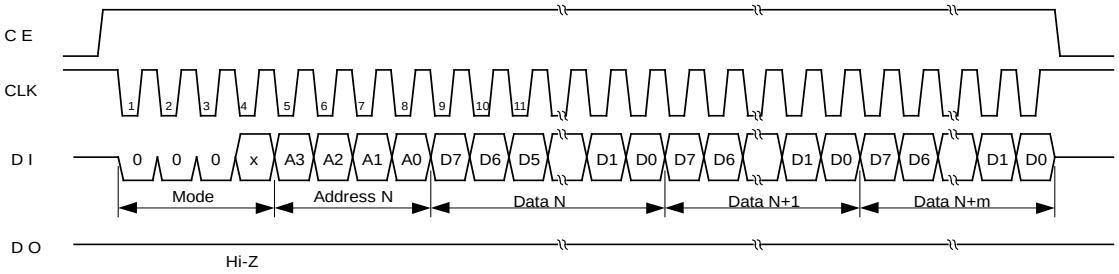
For both read and write, first set up chip condition (internally CE="H") to CE="H" , then specify the 4-bits address, and finally read or write in 8-bits units. Both read and write use MSB-first. In continuous operation, objected address is auto incremented. Auto incrementing of the address is cyclic, so address "F" is followed by address "0".

8.6.1. Write of data

1) One-shot writing



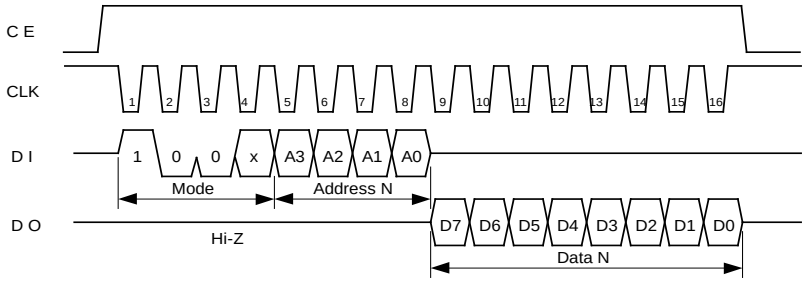
2) Continuous writing



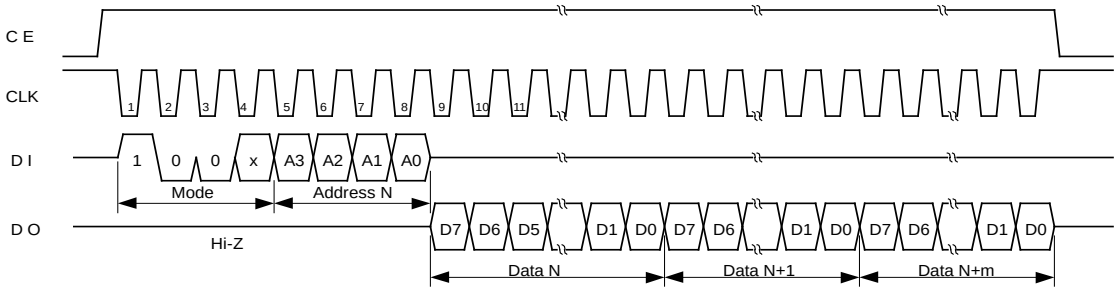
*When writing data, the data needs to be entered in 8-bits units.
If the input of data in 8-bits unit is not completed before CE input falls, the 8-bits data will not be written properly at the time CE input falls.

8.6.2. Read of data

1) One-shot reading

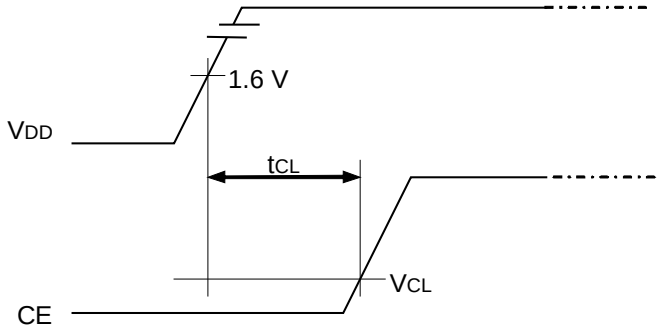


2) Continuous reading



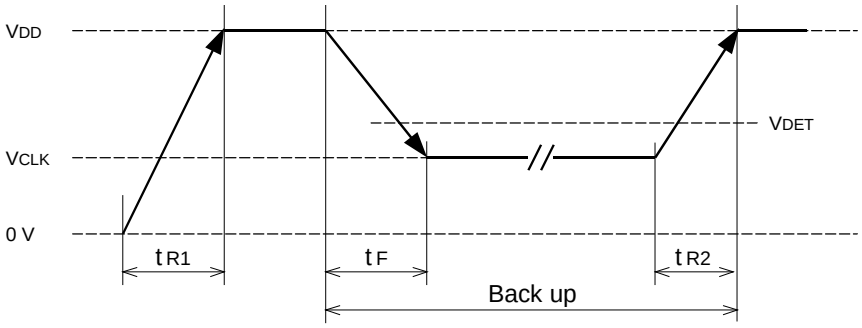
8.7. VDD and CE timing

* When the power is turned to ON, use with CE = " L " (VCL[V] in the diagram) as illustrated in the following timing chart.



Item	Symbol	Remark	Specification	Unit
CE voltage when power is turned to ON	VCL	CE impressed voltage until VDD = 1.6 V	0.3 (Max.)	V
CE=VCL[V] time when power is turned to ON	tCL	Time to maintain CE=VCL[V] until VDD = 1.6 V	30 (Min.)	ms

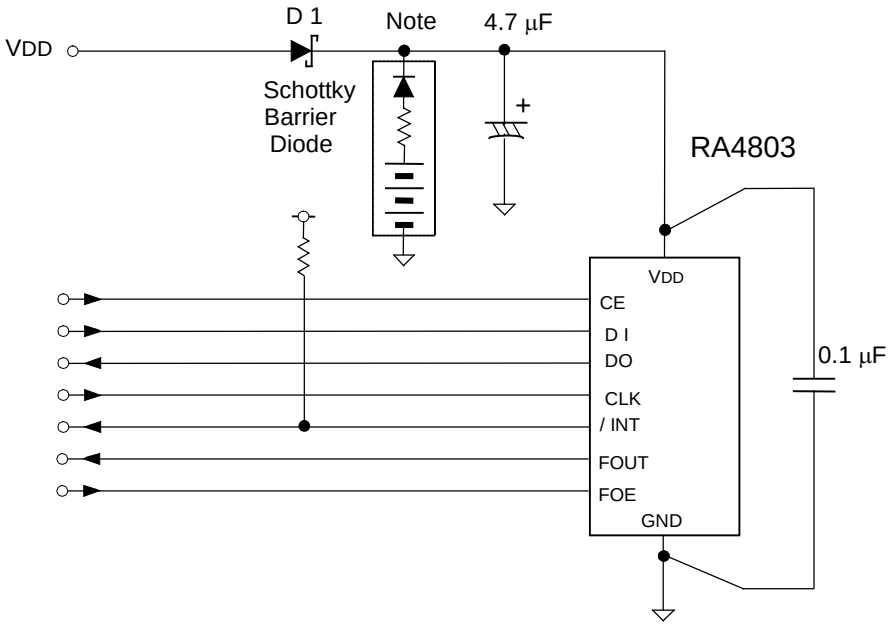
8.8. Backup and Recovery



Item	Symbol	Condition	Min.	Typ.	Max.	Unit.
Power supply detection voltage (1)	VDET	–			2.2	V
Power supply detection voltage (2)	VLOW	–			1.6	V
Power supply drop time	tF	–	2			µs /V
Initial power-up time	tR1	–			10	ms /V
Clock maintenance power-up time	tR2	1.6V → VDD ≤ 3.6V	5			µs /V
		1.6V → VDD > 3.6V	15			µs /V

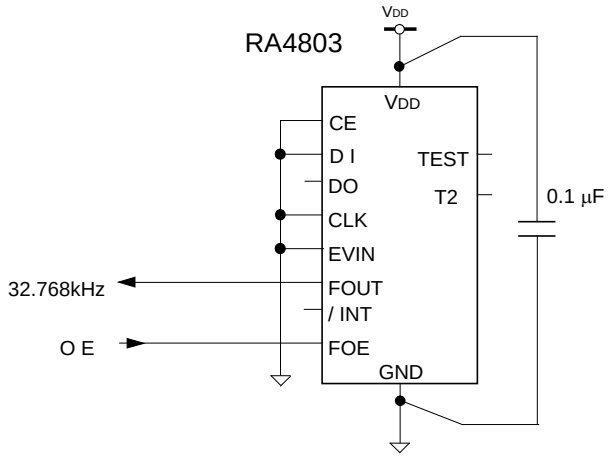
Please control a power supply in the above agreement so that normalcy operates a detect circuit of power supply injection.
Please start a power supply at 0V by all means.
Before power supply change operation and a shift to backup state ,please set a CE terminal at a Low level

8.9 Connection with Typical Microcontroller



Note : When using the seconding battery, the diode is not required.
When using the primary battery, the diode is required.
For detailed value on the resistance, please consult a battery maker.

8.10 When used as a clock source (32 kHz-TCXO)



8.11. Note about read-out method of a 1/100s register

RA-4803 is equipped with a 1/100s register.
As for 1/100 counters, it is worked in very fast clock than second.
Therefore, as for the count operation of each, behavior in a chip access hold facility (P.8 reference) operation is different.
When using a 1/100s register, be careful as follows.
Behavior, when access hold function worked.
When communication to a clock counter of an RTC started, by access hold facility, update in the time can stop hold automatically.
However, as for 1/100 second counters, data cannot stop hold, and count is continued.
As for 1/100 value, it is examined data by IC circuit, and it is captured to 1/100s register.

Therefore, there is case lost continuity of data in 1/100 second data and time data when 1/100 second digits are captured just after a second updates.

This phenomenon occurs in restrictive timing, but internal Time and date are correct and internal updates are correct.

A lag of a readout result is -1 second at the maximum.

Read-out method of 1/100 second digits to prevent mismatching of the time
Method 1
Method to read two times of 1/100 second digits
Step1:
please read 1/100 second digits and time data, and stored those.
Step2:
Please read only 1/100 second digits again.
Please complete Step2 within 10ms from Step1.
Step3:
If two 1/100 second digits are same values, please advance next.
When two values are different, please return to Step1.
Note
Between Step2 and Step1, please put CE=LOW by all means.

Method 2
Method to use an interruption flag of the fixed period interrupt function.

Step1
Please clear USEL bit of address Dh in a zero.
It is update interruption of sec.

Please clear UF bit of address Eh in a zero.
Step3:
Please read time data and 1/100 data.

Please read UF bit.

Step5:
Please adopt the data that I read in case of UF=0.
Please cancel the data that I read in case of UF=1.
Step6:
When it is executed again, return to Step2.

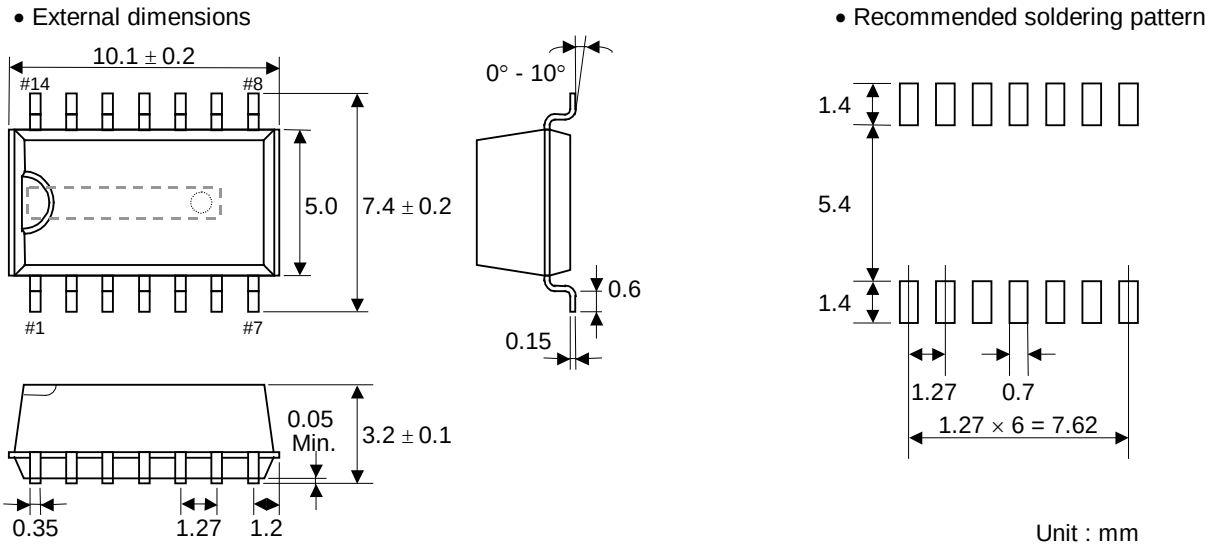
When second is updated, a UF bit is set to 1.
Therefore it must be executed Step2 and 4 within one second.
Please complete Step4 within 1sec from Step2.
(recommendation,:, lower than 10ms)
Please divide Step3 and Step4 by CE=LOW.

9. External Dimensions / Marking Layout

9.1. RA4803 SA

9.1.1. External dimensions

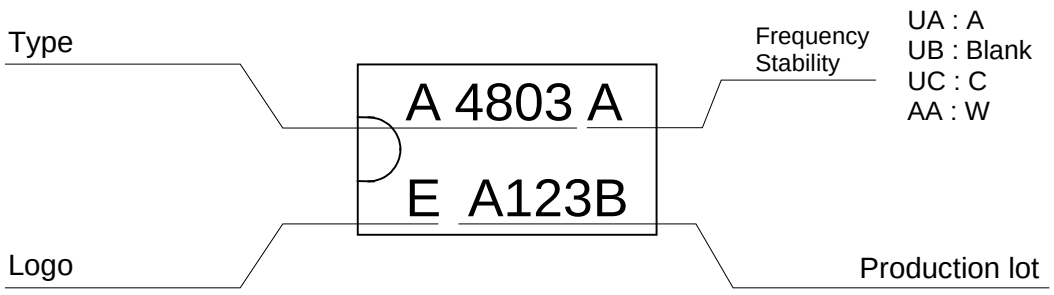
RA4803SA (SOP – 14pin)



∗ The cylinder of the crystal oscillator can be seen in this area (front), but it has no affect on the performance of the device.

9.1.2. Marking layout

RA4803 SA (SOP – 14pin)



∗ Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

10. Application notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 μF as close as possible to the power supply pins (between VDD and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.

* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to VDD or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

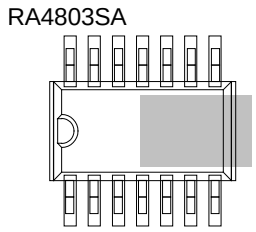
(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

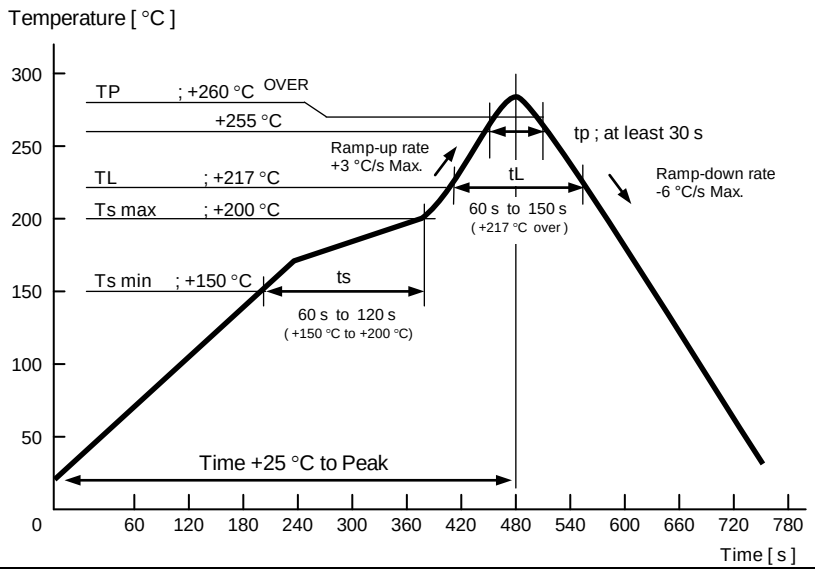
Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1 : Example GND Pattern



* The shaded part ( ) indicates where a GND pattern should be set without getting too close to a signal line

Fig. 2 : Reference profile for our evaluation of Soldering heat resistance.



Application Manual

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