BGA24 NAND Specification

1Gb (128M x 8), 3.3v, with ECC controller build-in NAND flash

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Revision History:

Rev.	Date	Changes	Remark
V0.0	2016/08/16	Initial version	Preliminary
V0.1	2016/09/25	Update ID table	Preliminary
V0.2	2017/02/26	Update ID table on page 21; Correct a Part number; definition typo on page4	Preliminary
V0.3	2017/12/11	Change company name “Paragon” to “XTX”.	Revise
V0.4	2017/07/22	Overall reviewing and updating	Revise
V0.5	2019/12/04	Correct the unclear description	Revise
V0.6	2023/11/01	Add RoHS, MSL and Reflow Soldering Profile Correct the unclear description about flash ID	Revise

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General Description

The PN27G01B is a single 3.3v 1Gbit NAND Electrically Erasable and Programmable Read-Only Memory (NAND E2PROM) organized as (2048 + 64) bytes × 64 pages × 1024 blocks. The device has a 2112-byte static registers which allow program and read data to be transferred between the register and the memory cell array in 2112-byte increments. The Erase operation is implemented in a single block unit (128 Kbytes + 4 Kbytes: 2112 bytes × 64 pages).

The PN27G01B is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

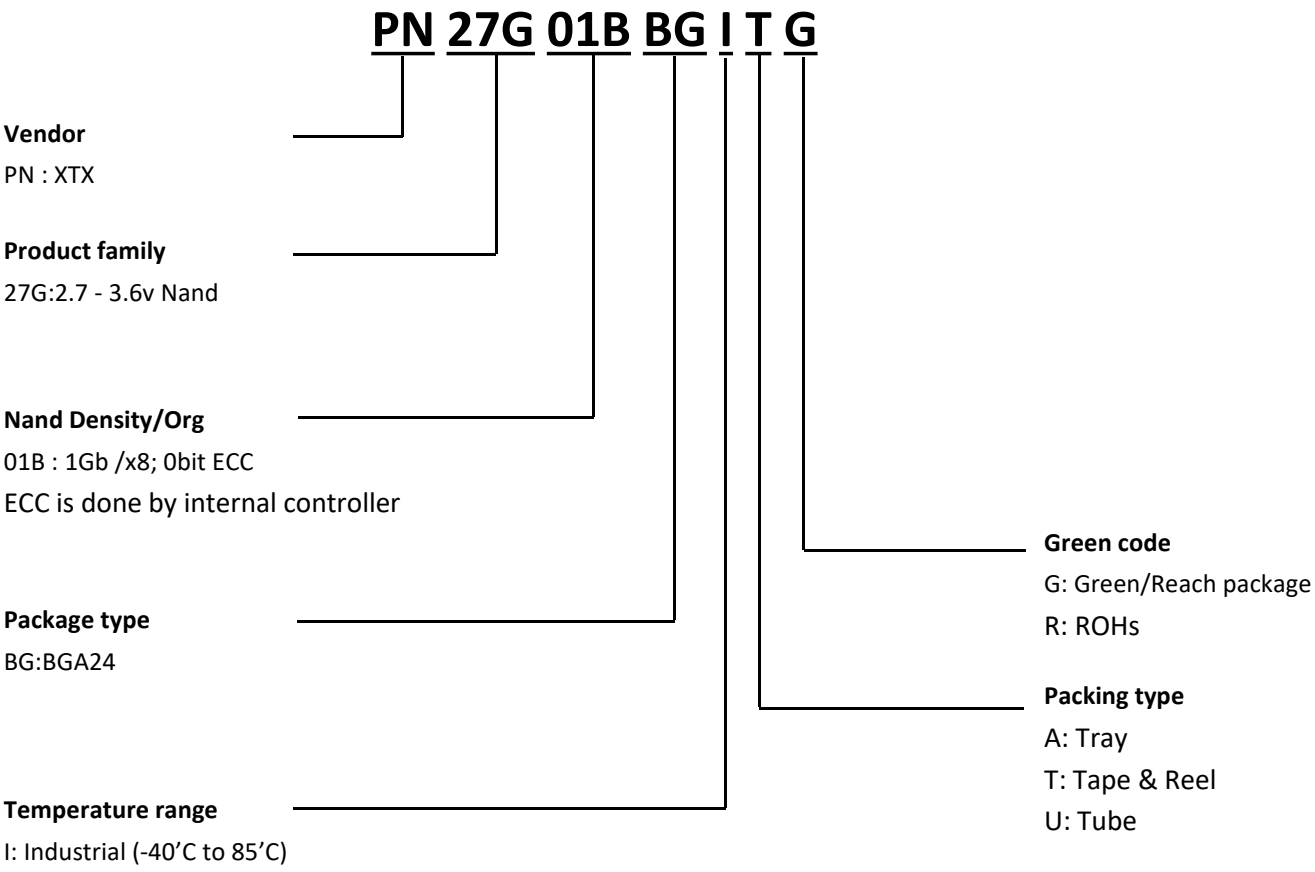
The PN27G01B has ECC logic on the chip and 8bit read errors for each 528Bytes can be corrected internally.

Features

- **Single Level per Cell (SLC) Technology**
- **ECC requirement: 0 bit/528Bytes, with build-in ECC controller to implement 8bit/528Bytes internally**
- **Power Supply Voltage**
  Voltage range: 2.7V ~ 3.6V
- **Organization**
  Page size: x8 (2048 + 64) bytes; 64- bytes spare area
  Block size: x8 (128k + 4k) bytes
  1004 block(min) ~ 1024 block(max)
- **Modes**
  Read, Reset, Auto Page Program, Auto Block Erase, Status Read, Page Copy, ECC Status Read
- **Access time**
  Cell array to register: 40μs (typ)
  Serial Read Cycle: 25 ns (min) (CL=50pF)
- **Program/Erase time**
  Auto Page Program: 330 μs /page (typ.)
  Auto Block Erase: 3.5 ms /block(typ.)
- **Reliability**
  10 Year Data retention (Typ)
- **Moisture Sensitivity Level: MSL3**
- **Package**
  BGA24 (6x8mm)
  All Packages are RoHS Compliant and Halogen-free

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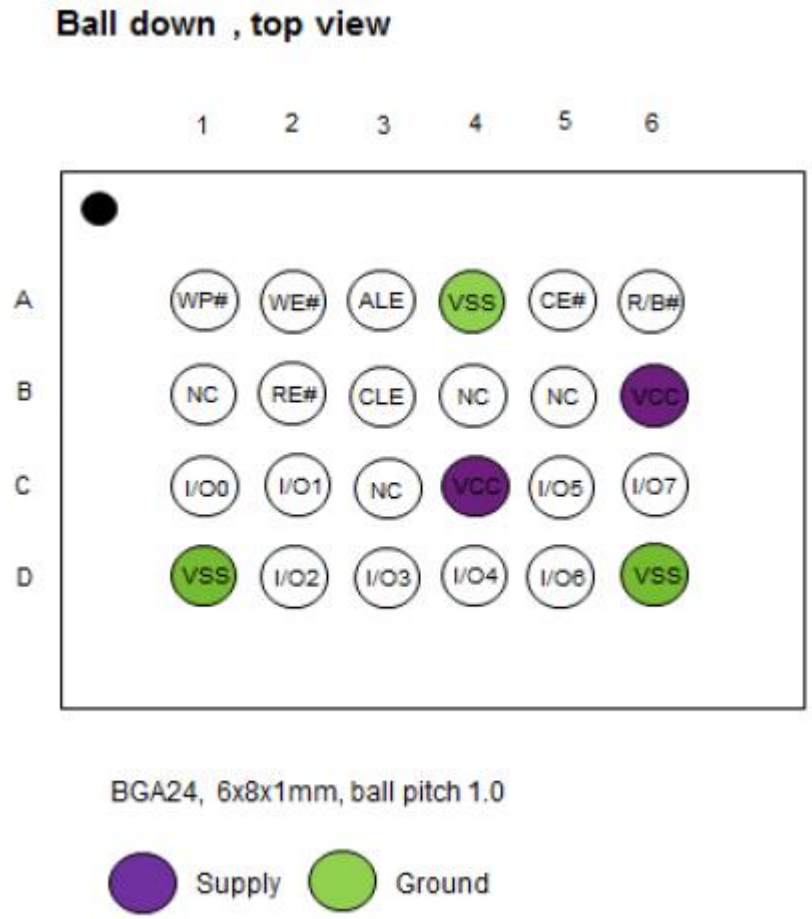
Part number description



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Pin Assignments

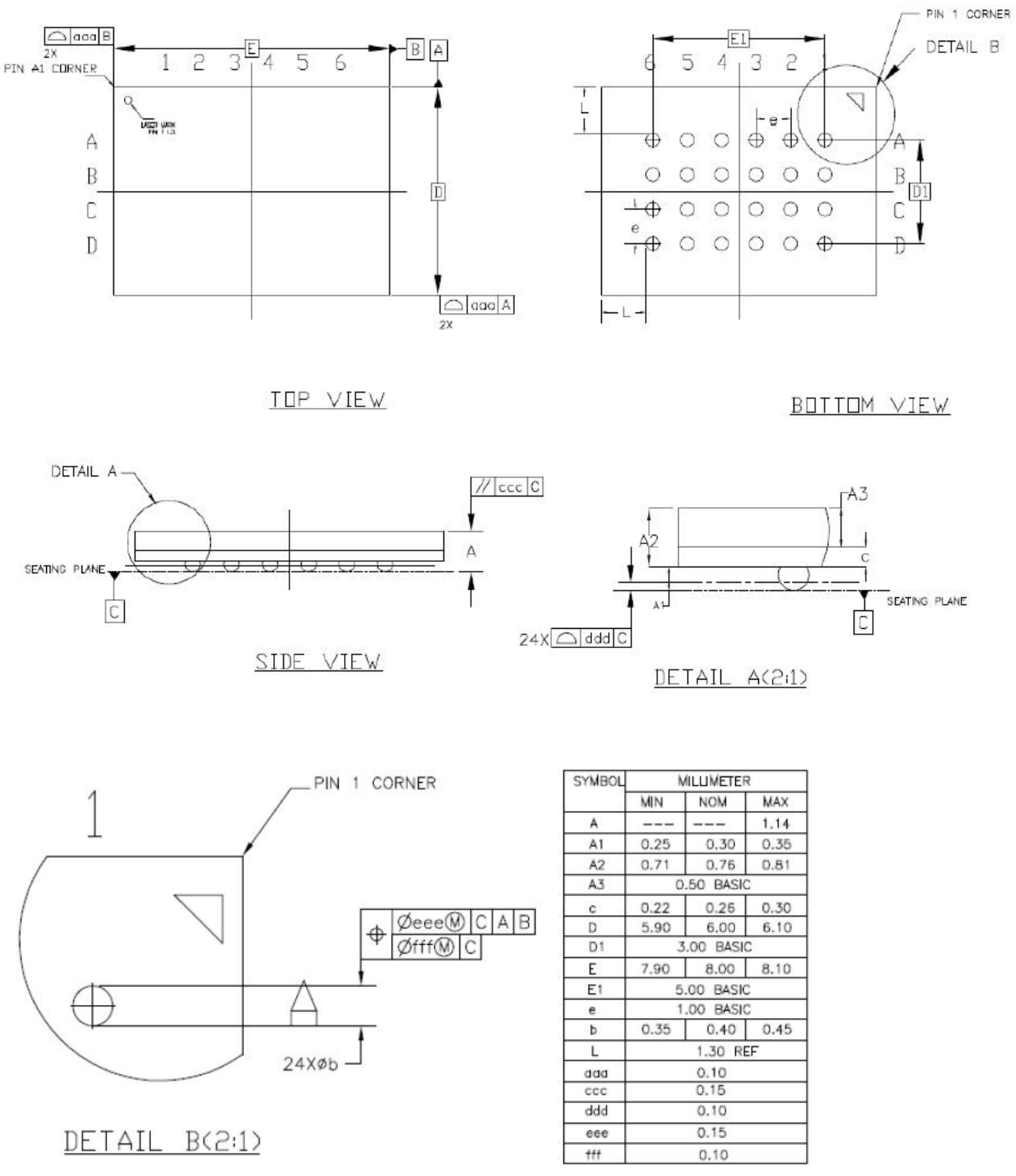
BGA24



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Package Dimension

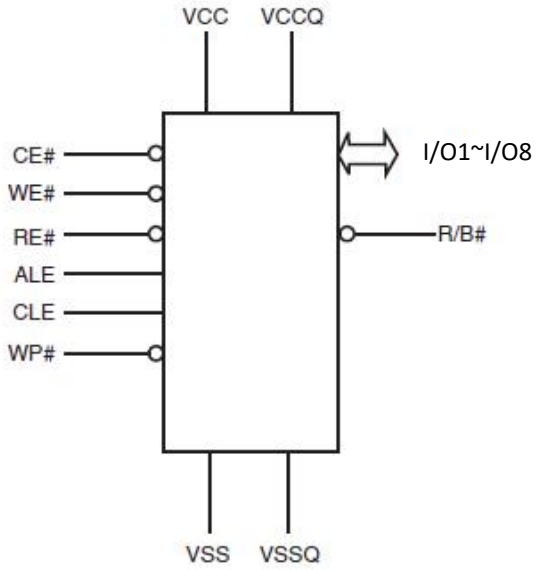
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SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.14
A1	0.25	0.30	0.35
A2	0.71	0.76	0.81
A3	0.50 BASIC		
c	0.22	0.26	0.30
D	5.90	6.00	6.10
D1	3.00 BASIC		
E	7.90	8.00	8.10
E1	5.00 BASIC		
e	1.00 BASIC		
b	0.35	0.40	0.45
L	1.30 REF		
aaa	0.10		
ccc	0.15		
ddd	0.10		
eee	0.15		
fff	0.10		

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Logic Diagram



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Pin Description

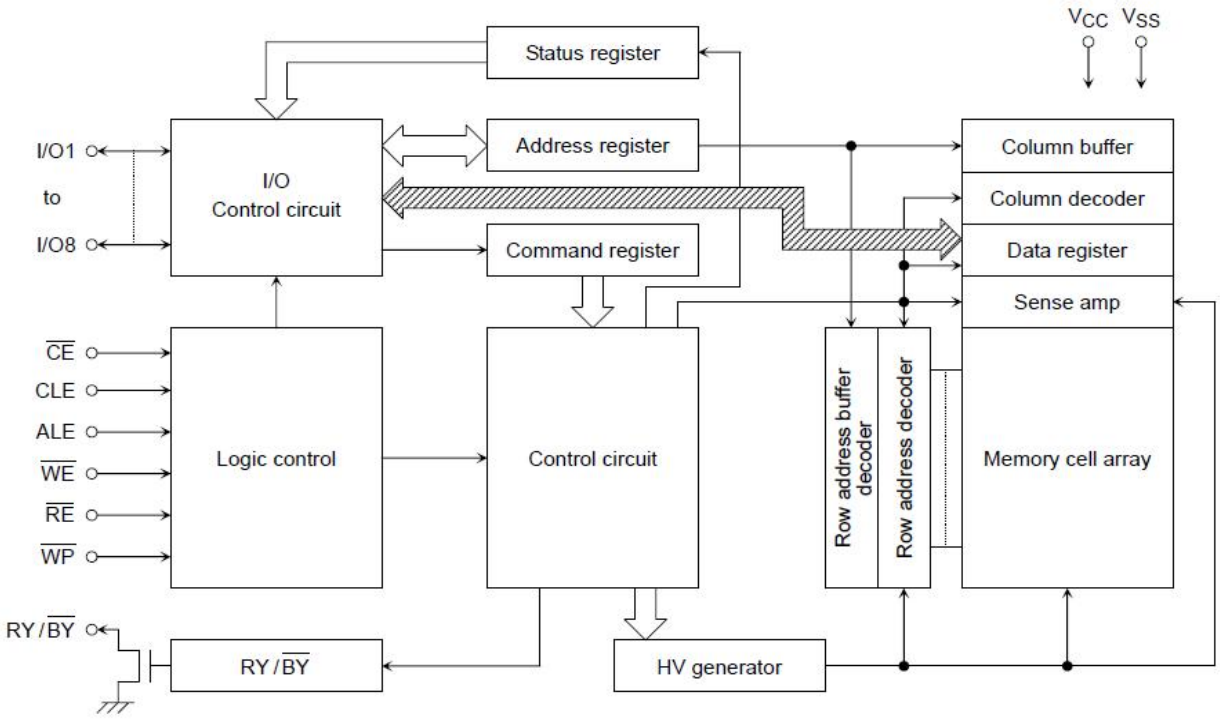
Pin Name	Description
I/O1 - I/O8 (x8)	**Inputs/Outputs**. The I/O pins are used for command input, address input, data input, and data output. The I/O pins float to High-Z when the device is deselected or the outputs are disabled.
CLE	**Command Latch Enable.** This input activates the latching of the I/O inputs inside the Command Register on the rising edge of Write Enable (WE#).
ALE	**Address Latch Enable.** This input activates the latching of the I/O inputs inside the Address Register on the rising edge of Write Enable (WE#).
CE#	**Chip Enable.** This input controls the selection of the device. When the device is not busy CE# low selects the memory.
WE#	**Write Enable.** This input latches Command, Address and Data. The I/O inputs are latched on the rising edge of WE#.
RE#	**Read Enable.** The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE# which also increments the internal column address counter by one.
WP#	**Write Protect.** The WP# pin, when low, provides hardware protection against undesired data modification (program / erase).
R/B#	**Ready Busy**. The Ready/Busy output is an Open Drain pin that signals the state of the memory.
VCC	**Supply Voltage**. The VCC supplies the power for all the operations (Read, Program, Erase). An internal lock circuit prevents the insertion of Commands when VCC is less than VLKO.
VSS	**Ground.**
NC	**Not Connected.**

Notes:

1. *A 0.1 µF capacitor should be connected between the VCC Supply Voltage pin and the VSS Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.*

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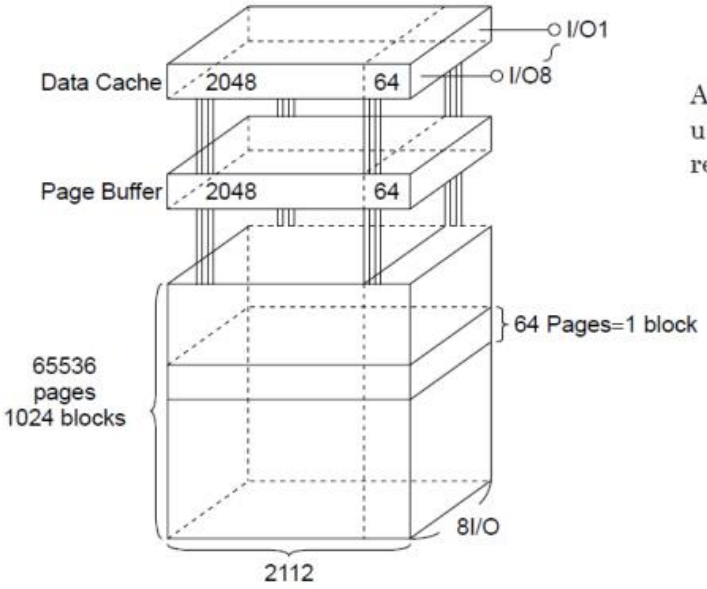
Block Diagram



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Array Organization

The Program operation works on page units while the Erase operation works on block units.



A page consists of 2112 bytes in which 2048 bytes are used for main memory storage and 64 bytes are for redundancy or for other uses.

1 page = 2112bytes

1 block = 2112 bytes × 64 pages = (128K + 4K) bytes

Capacity = 2112 bytes × 64pages × 1024 blocks

Addressing

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second cycle	L	L	L	L	CA11	CA10	CA9	CA8
Third cycle	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth cycle	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8

CA0 to CA11: Column address

PA0 to PA15: Page address

PA6 to PA15: Block address

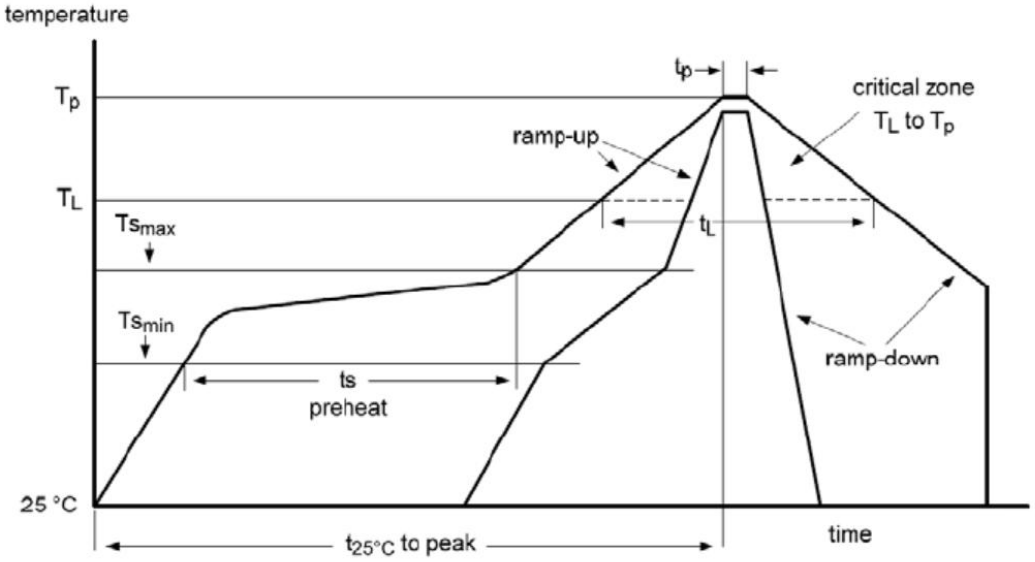
PA0 to PA5: NAND address in block

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Absolute Maximum Ratings

SYMBOL	RATING	VALUE	UNIT
V_{CC}	Power Supply Voltage	−0.6 to 4.6	V
V_{IN}	Input Voltage	−0.6 to 4.6	V
$V_{I/O}$	Input /Output Voltage	−0.6 to V_{CC} + 0.3 (≤ 4.6 V)	V
P_D	Power Dissipation	0.3	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Storage Temperature	−55 to 150	°C
T_{OPR}	Operating Temperature	-40 to 85	°C

Reflow Soldering Profile



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Capacitance *(Ta = 25°C, f = 1 MHz)

SYMB0L	PARAMETER	CONDITION	MIN	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	—	10	pF
C_{OUT}	Output	V_{OUT} = 0 V	—	10	pF

* This parameter is periodically sampled and is not tested for every device.

Valid Blocks

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	1004	—	1024	Blocks

NOTE: The device occasionally contains unusable blocks. Refer to Application Note (13) toward the end of this document.

The first block (Block 0) is guaranteed to be a valid block at the time of shipment.

The specification for the minimum number of valid blocks is applicable over lifetime The number of valid blocks is on the basis of single plane operations, and this may be decreased with two plane operations.

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Recommended DC Operating Conditions

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply Voltage	2.7	—	3.6	V
V_{IH}	High Level input Voltage	Vcc x 0.8	—	V_{CC} + 0.3	V
V_{IL}	Low Level Input Voltage	−0.3*	—	Vcc x 0.2	V

* −2 V (pulse width lower than 20 ns)

DC Characteristics (Ta = -40 to 85℃, VCC = 2.7 to 3.6V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	—	—	±10	μA
I_{CCO1}	Serial Read Current	CE# = V_{IL}, I_{OUT} = 0 mA, tcycle = 25	—	—	30	mA
I_{CCO2}	Programming Current	—	—	—	30	mA
I_{CCO3}	Erasing Current	—	—	—	30	mA
I_{CCS}	Standby Current	CE# = V_{CC}−0.2 V, WP# = 0 V/V_{CC}	—	—	50	μA
V_{OH}	High Level Output Voltage	I_{OH} = −0.1 mA	Vcc – 0.2	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 0.1 mA	—	—	0.2	V
I_{OL} (RY/BY)	Output current of RY/BY pin	V_{OL} = 0.2 V	—	4	—	mA

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AC CHARACTERISTICS AND RECOMMENDED OPERATING

(Ta = -40 to 85℃, V_{CC} = 2.7 to 3.6V)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{CLS}	CLE Setup Time	12	—	ns
t_{CLH}	CLE Hold Time	5	—	ns
t_{CS}	CE# Setup Time	20	—	ns
t_{CH}	CE# Hold Time	5	—	ns
t_{WP}	Write Pulse Width	12	—	ns
t_{ALS}	ALE Setup Time	12	—	ns
t_{ALH}	ALE Hold Time	5	—	ns
t_{DS}	Data Setup Time	12	—	ns
t_{DH}	Data Hold Time	5	—	ns
t_{WC}	Write Cycle Time	25	—	ns
t_{WH}	WE# High Hold Time	10	—	ns
t_{WW}	WP# High to WE# Low	100	—	ns
t_{RR}	Ready to RE# Falling Edge	20	—	ns
t_{RW}	Ready to WE# Falling Edge	20	—	ns
t_{RP}	Read Pulse Width	12	—	ns
t_{RC}	Read Cycle Time	25	—	ns
t_{REA}	RE# Access Time	—	20	ns
t_{CEA}	CE# Access Time	—	25	ns
t_{CLR}	CLE Low to RE# Low	10	—	ns
t_{AR}	ALE Low to RE# Low	10	—	ns
t_{RHOH}	RE# High to Output Hold Time	25	—	ns
t_{RLOH}	RE# Low to Output Hold Time	5	—	ns
t_{RHZ}	RE# High to Output High Impedance	—	60	ns
t_{CHZ}	CE# High to Output High Impedance	—	20	ns
t_{CSD}	CE# High to ALE or CLE Don't Care	0	—	ns
t_{REH}	RE# High Hold Time	10	—	ns
t_{IR}	Output-High-impedance-to- RE# Falling Edge	0	—	ns
t_{RHW}	RE# High to WE# Low	30	—	ns
t_{WHC}	WE# High to CE# Low	30	—	ns
t_{WHR}	WE# High to RE# Low	60	—	ns
t_{WB}	WE# High to Busy	—	100	ns
t_{RST}	Device Reset Time (Ready/Read/Program/Erase)	—	5/5/10/500	μs

*1: tCLS and tALS can not be shorter than tWP

*2: tCS should be longer than tWP + 8ns.

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AC Test Conditions

PARAMETER	CONDITION
	V_{CC}: 2.7 to 3.6V
Input level	V_{CC} – 0.2 V, 0.2 V
Input pulse rise and fall time	3 ns
Input comparison level	Vcc / 2
Output data comparison level	Vcc / 2
Output load	C_L (50 pF) + 1 TTL

Note: Busy to ready time depends on the pull-up resistor tied to the RY/BY# pin.

Programming and Erasing Characteristics

(Ta = -40 to 85℃, V_{CC} = 2.7 to 3.6V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Average Programming Time (single page)	—	330	700	μs	
N	Number of Partial Program Cycles in the Same Page	—	—	4		(1)
t_{BERASE}	Block Erasing Time	—	3.5	10	ms	
tR	Memory Cell Array to Starting Address (Single Page)	—	40	120	us	

(1) Refer to Application Note (12) toward the end of this document.

Data Output

When tREH is long, output buffers are disabled by /RE=High, and the hold time of data output depend on tRHOH (25ns MIN). On this condition, waveforms look like normal serial read mode.

When tREH is short, output buffers are not disabled by /RE=High, and the hold time of data output depend on tRLOH (5ns MIN). On this condition, output buffers are disabled by the rising edge of CLE, ALE, /CE or falling edge of /WE, and waveforms look like Extended Data Output Mode.

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Mode Selection

The operation modes such as Program, Erase, Read and Reset are controlled by command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, /CE , /WE , /RE and /WP signals as shown in Table 2.

Table 2. Logic Table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$ *1
Command Input	H	L	L	⌐└⌐	H	*
Data Input	L	L	L	⌐└⌐	H	H
Address input	L	H	L	⌐└⌐	H	*
Serial Data Output	L	L	L	H	⌐└⌐	*
During Program (Busy)	*	*	*	*	*	H
During Erase (Busy)	*	*	*	*	*	H
During Read (Busy)	*	*	H	*	*	*
	*	*	L	H (*2)	H (*2)	*
Program, Erase Inhibit	*	*	*	*	*	L
Standby	*	*	H	*	*	0 V/V_{CC}

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

1. **1: Refer to Application Note (10) toward the end of this document regarding the $\overline{WP}$ signal when Program or Erase Inhibit*
2. **2 :If $\overline{CE}$ is low during read busy, $\overline{WE}$ and $\overline{RE}$ must be held High to avoid unintended command/address input to the device or read to device. Reset or Status Read command can be input during Read Busy.*

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Table 3. Command table (HEX)

	First Cycle	Second Cycle	Acceptable while Busy
Serial Data Input	80	—	
Read	00	30	
Column Address Change in Serial Data Output	05	E0	
Auto Page Program	80	10	
Column Address Change in Serial Data Input	85	—	
Read for Copy-back without Data Out	00	35	
Copy-back program without Data Out	85	10	
Auto Block Erase	60	D0	
ID Read	90	—	
Status Read	70	—	°
ECC status read	7A	—	
Reset	FF	—	°

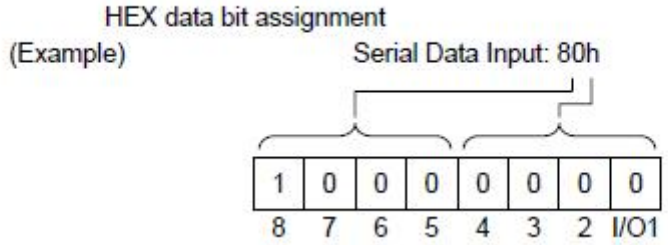


Table 4. Read mode operation states

	CLE	ALE	CE	WE	RE	I/O1 to I/O8	Power
Output select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active

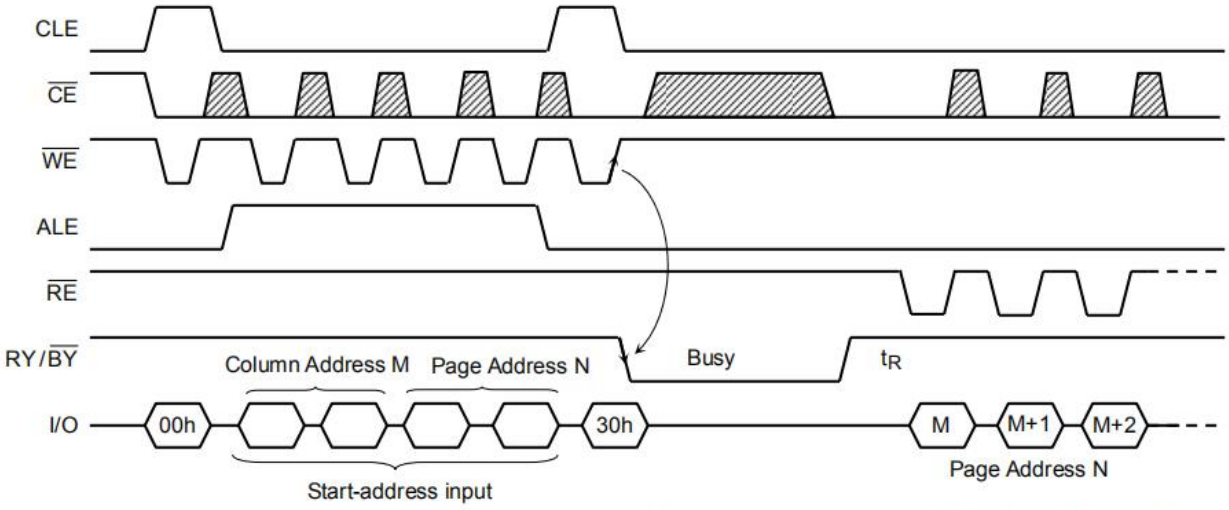
H: V_{IH}, L: V_{IL}

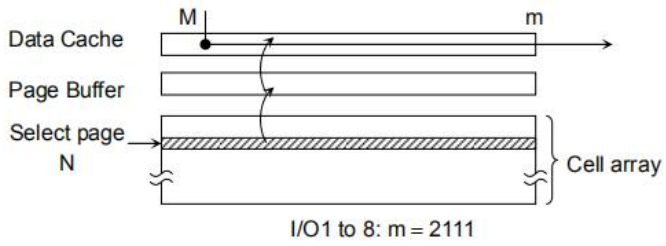
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Device Operation

Read Mode

Read mode is set when the "00h" and “30h” commands are issued to the Command register. Between the two commands, a start address for the Read mode needs to be issued. After initial power on sequence, “00h” command is latched into the internal command register. Therefore read operation after power on sequence is executed by the setting of only five address cycles and “30h” command. Refer to the figures below for the sequence and the block diagram (Refer to the detailed timing chart.).



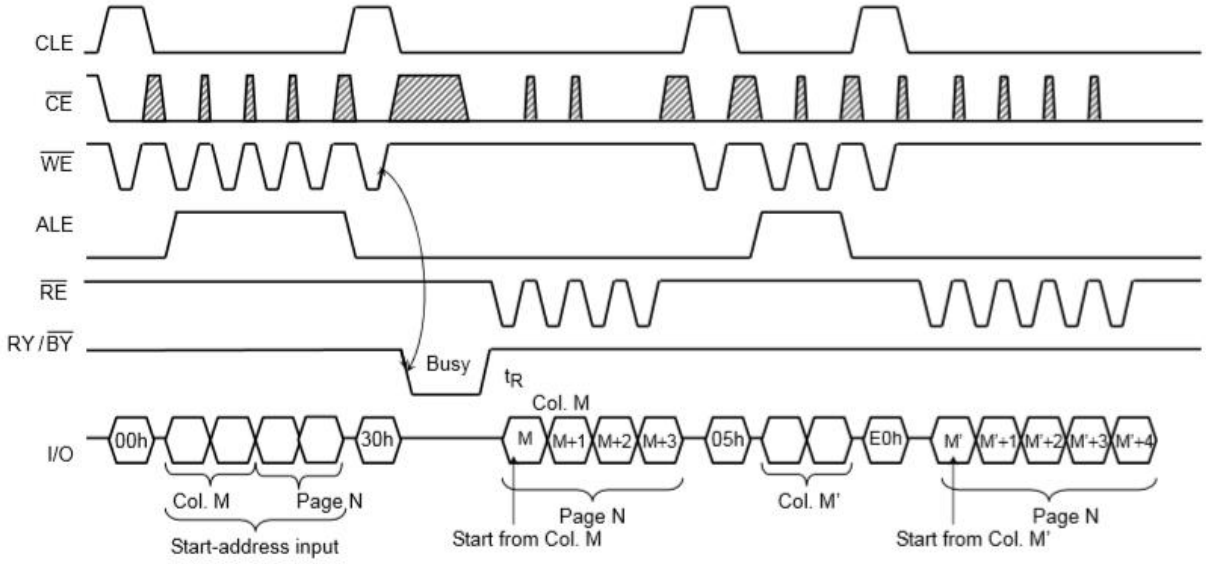


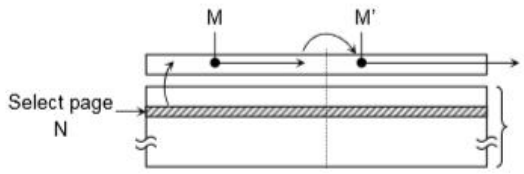
A data transfer operation from the cell array to the Data Cache via Page Buffer starts on the rising edge of $\overline{WE}$ in the 30h command input cycle (after the address information has been latched). The device will be in the Busy state during this transfer period.

After the transfer period, the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start address designated in the address input cycle.

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Random Column Address Change in Read Cycle





During the serial data output from the register, the column address can be changed by inputting a new column address using the 05h and E0h commands. The data is read out in serial starting at the new column address. Random Column Address Change operation can be done multiple times within the same page.

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ECC & Sector definition for ECC

Internal ECC logic generates Error Correction Code during busy time in program operation. The ECC logic manages 9bit error detection and 8bit error correction in each 528Bytes of main data and spare data. A section of main field (512Bytes) and spare field (16Bytes) are paired for ECC. During read, the device executes ECC of itself. Once read operation is executed, Read Status Command (70h) can be issued to check the read status. The read status remains until other valid commands are executed.

To use ECC function, below limitation must be considered.

- A sector is the minimum unit for program operation and the number of program per page must not exceed 4.

2KByte Page Assignment

1st Main	2nd Main	3rd Main	4th Main	1st Spare	2nd Spare	3rd Spare	4th Spare
512B	512B	512B	512B	16B	16B	16B	16B

Note) Internal ECC manages all data of Main area and Spare area

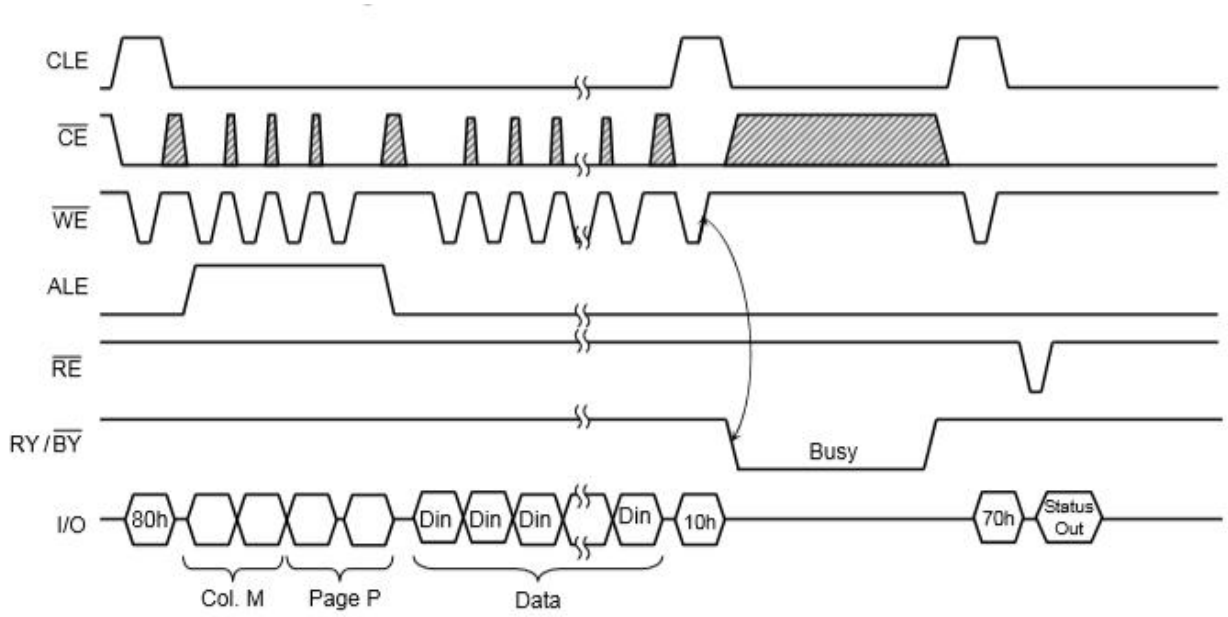
Definition of 528Byte Sector

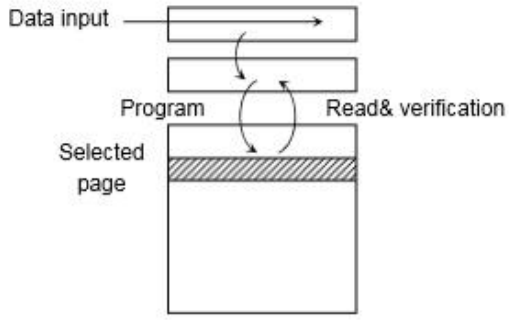
Sector	**Column Address (Byte)**	
	Main Field	**Spare Field**
1st Sector	0 ~ 511	2,048 ~ 2,063
2nd Sector	512 ~ 1,023	2,064 ~ 2,079
3rd Sector	1,024 ~ 1,535	2,080 ~ 2,095
4th Sector	1,536 ~ 2,047	2,096 ~ 2,111

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Auto Page Program Operation

The device carries out an Automatic Page Program operation when it receives a "10h" Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)





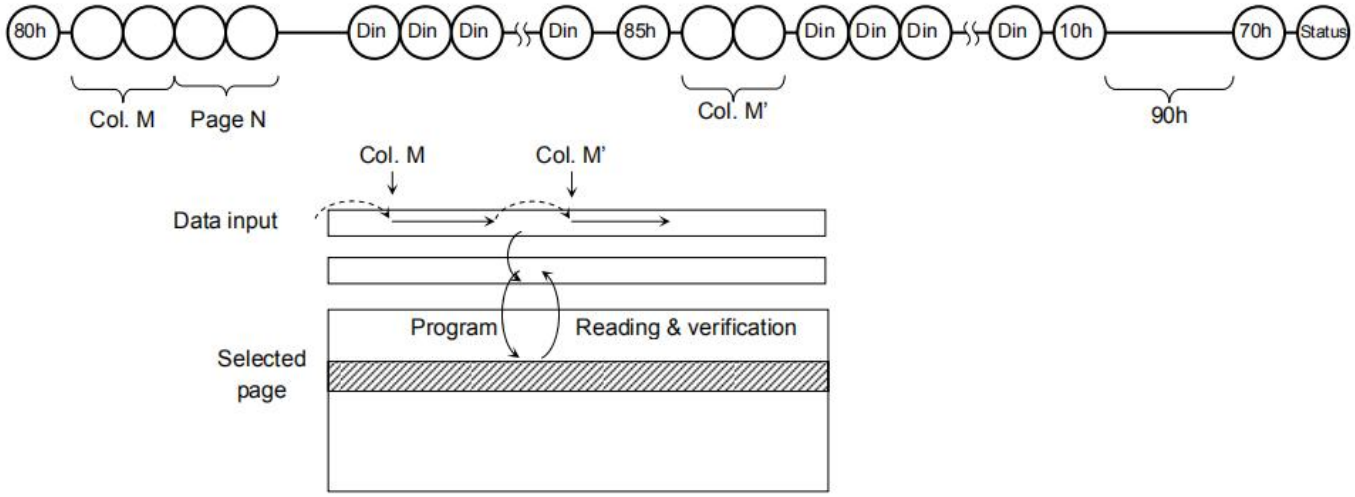
The data is transferred (programmed) from the Data Cache via the Page Buffer to the selected page on the rising edge of $\overline{WE}$ following input of the "10h" command. After programming, the programmed data is transferred back to the Page Buffer to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

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Random Column Address Change in Auto Page Program Operation

The column address can be changed by the 85h command during the data input sequence of the Auto Page Program operation.

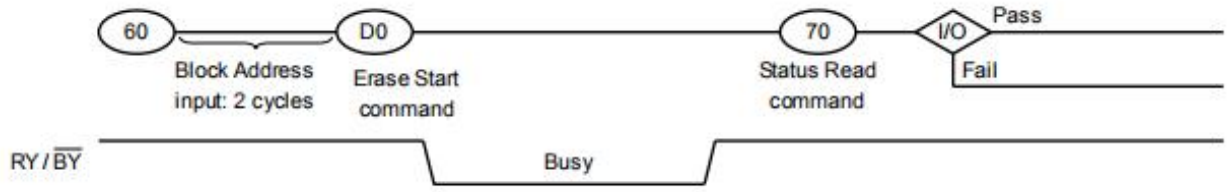
Two address input cycles after the 85h command are recognized as a new column address for the data input. After the new data is input to the new column address, the 10h command initiates the actual data program into the selected page automatically. The Random Column Address Change operation can be repeated multiple times within the same page.



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Auto Block Erase

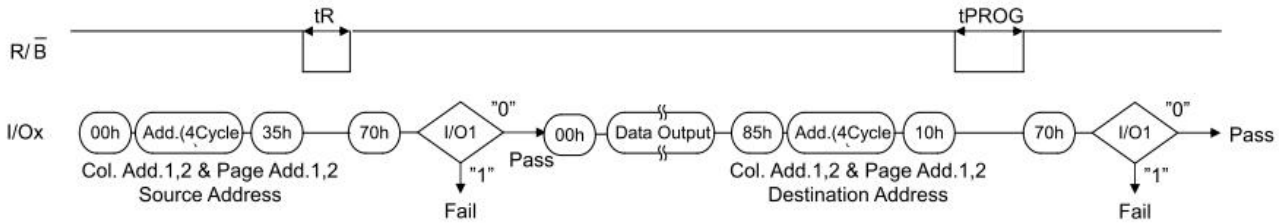
The Auto Block Erase operation starts on the rising edge of WE# after the Erase Start command “D0h” which follows the Erase Setup command “60h”. This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



READ FOR COPY-BACK WITH DATA OUTPUT TIMING GUIDE

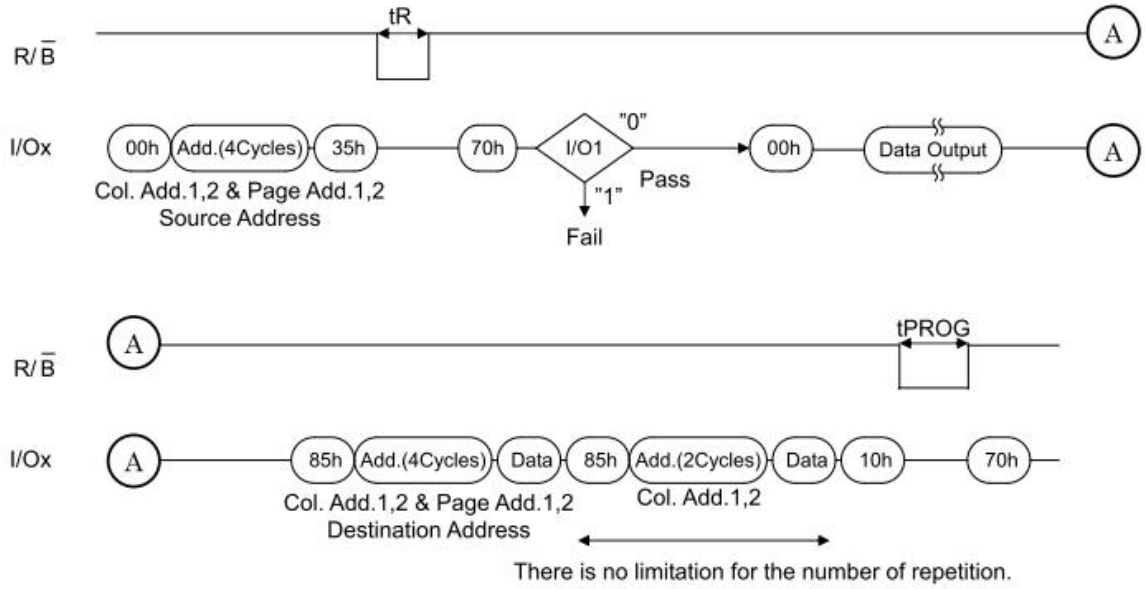
Copy-Back operation is a sequence execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with “35h” command and the address of source page moves the whole 2112 bytes data into the internal data buffer. Bit errors are checked by sequential reading the data or by reading the status in read after read busy time(tR) to check if uncorrectable error occurs. In the case where there is no bit error or no uncorrectable error, the data don’t need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the BY / RY# output, or the Status Bit (I/O7) of the Status Register. When the Copy-Back Program is complete, the Write Status Bit (I/O1) may be checked. The command register remains in Read Status command mode until another valid command is written to the command register. During copy-Back program, data modification is possible using random data input command (85h) as shown below.

Page Copy-Back Program Operation



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Page Copy-Back Program Operation with Random Data Input



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ID Read

The device contains ID codes which can be used to identify the device type, the manufacturer, and features of the device. The ID codes can be read out under the following timing conditions:

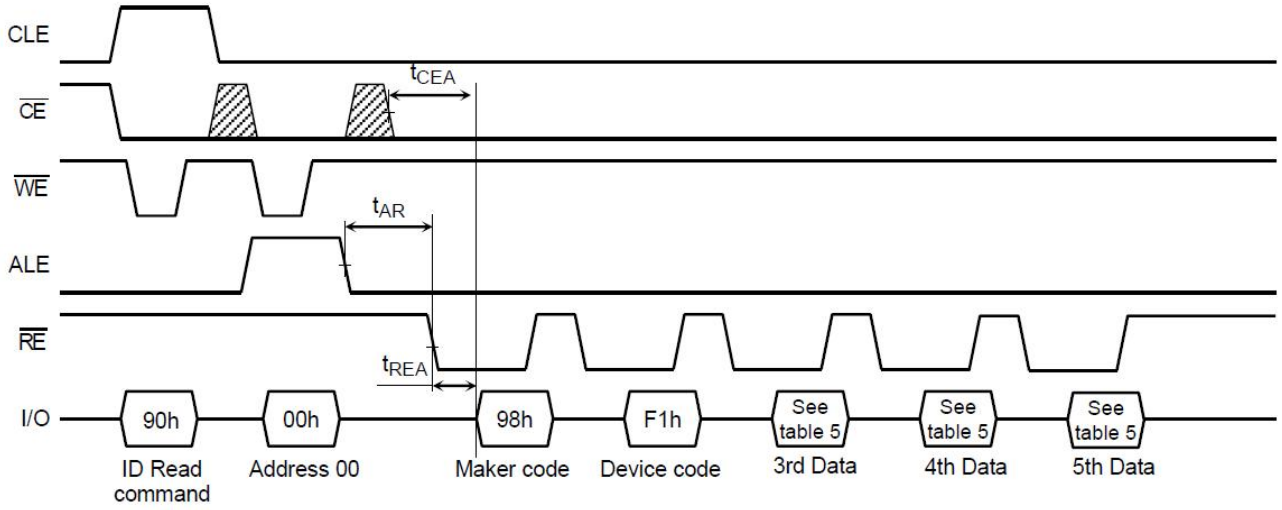


Table 5. Code table

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
1st Data	Maker Code	1	0	0	1	1	0	0	0	98h
2nd Data	Device Code	1	1	1	1	0	0	0	1	F1h
3rd Data	Chip Number, Cell Type	1	0	0	0	0	0	0	0	80h
4th Data	Page Size, Block Size	0	0	0	1	0	1	0	1	15h
5th Data	Plane Number	1	1	1	1	0	0	1	0	F2h

3rd Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 level cell					0	0		
	4 level cell					0	1		
	8 level cell					1	0		
	16 level cell					1	1		
Reserved		1	0	0	0				

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4th Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Page Size (without redundant area)	1 KB							0	0
	2 KB							0	1
	4 KB							1	0
	8 KB							1	1
Block Size (without redundant area)	64 KB			0	0				
	128 KB			0	1				
	256 KB			1	0				
	512 KB			1	1				
I/O Width	x8		0						
	x16		1						
Reserved		0				0	1		

5th Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Plane Number	1 Plane					0	0		
	2 Plane					0	1		
	4 Plane					1	0		
	8 Plane					1	1		
ECC engine on chip	With ECC engine	1							
Reserved			1	1	1			1	0

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Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass /fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port using RE# after a “70h” command input. The Status Read can also be used during a Read operation to find out the Ready/Busy status.

The resulting information is outlined in Table 6.

Table 6. Status output table

	Definition	Page Program	Block Erase	Read
I/O1	Chip Status Pass: 0 Fail: 1	Pass/Fail	Pass/Fail	Pass/Fail(Uncorrectable)
I/O2	Not Used	Invalid	Invalid	Invalid
I/O3	Not Used	0	0	0
I/O4	Chip Read status Normal or uncorrectable: 0 Recommended to rewrite: 1	0	0	Normal or uncorrectable/ Recommended to rewrite
I/O5	Not Used	0	0	0
I/O6	Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
I/O7	Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
I/O8	Write Protect Not Protected: 1 Protected: 0	Write Protect	Write Protect	Write Protect

The Pass/Fail status on I/O1 is only valid during a Program/Erase operation when the device is in the Ready state.

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ECC Status Read

The ECC Status Read function is used to monitor the Error Correction Status.

Internal ECC circuit works for the NAND Flash main and spare areas. The number of errors in the sector can be confirmed by this ECC Status Read command during read operation.

8	7	6	5	4	3	2	I/O1
Sector Information				ECC Status			

ECC Status

I/O4 to I/O1	ECC Status
0000	No Error
0001	1bit error(Correctable)
0010	2bit error(Correctable)
0011	3bit error(Correctable)
0100	4bit error(Correctable)
0101	5bit error(Correctable)
0110	6bit error(Correctable)
0111	7bit error(Correctable)
1000	8bit error(Correctable)
1111	Uncorrectable Error

Sector Information

I/O8 to I/O5	Sector Information
0000	1st Sector (Main and Spare area)
0001	2nd Sector (Main and Spare area)
0010	3rd Sector (Main and Spare area)
0011	4th Sector (Main and Spare area)
Other	Reserved

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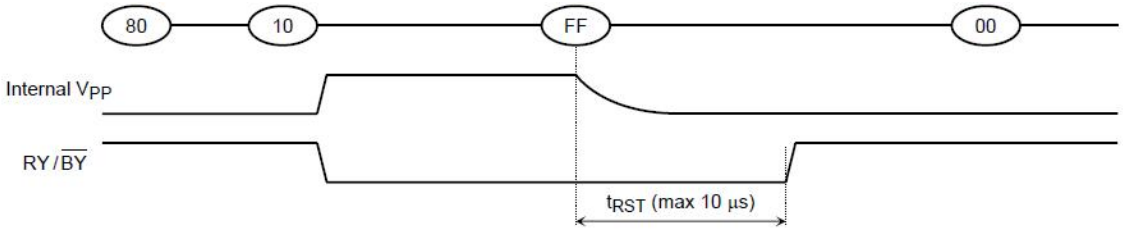
Reset

The Reset mode stops all operations. For example, in case of a Program or Erase operation, the internally generated voltage is discharged to 0 volt and the device enters the Wait state.

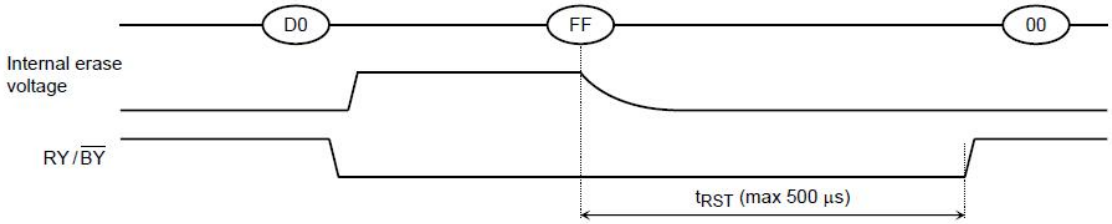
Reset during a Cache Program/Page Copy may not just stop the most recent page program but it may also stop the previous program to a page depending on when the FF reset is input.

The response to a “FFh” Reset command input during the various device operations is as follows:

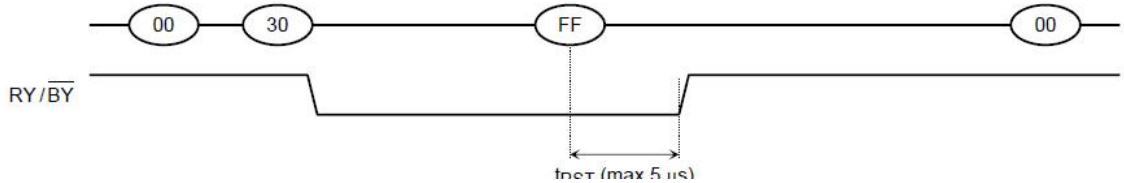
When a Reset (FFh) command is input during programming



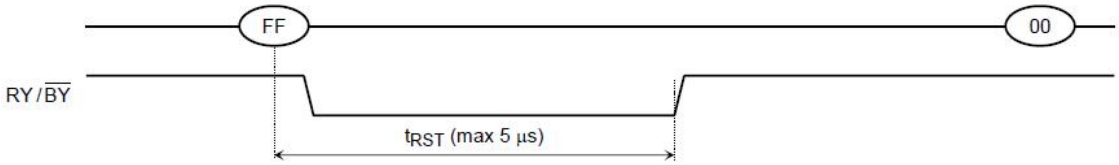
When a Reset (FFh) command is input during erasing



When a Reset (FFh) command is input during Read operation

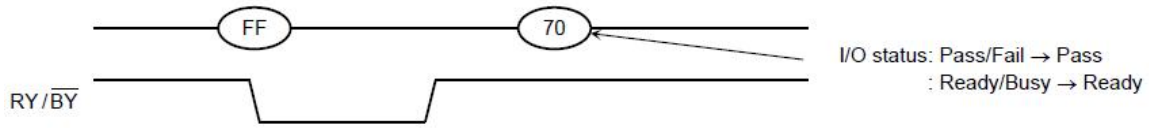


When a Reset (FFh) command is input during Ready

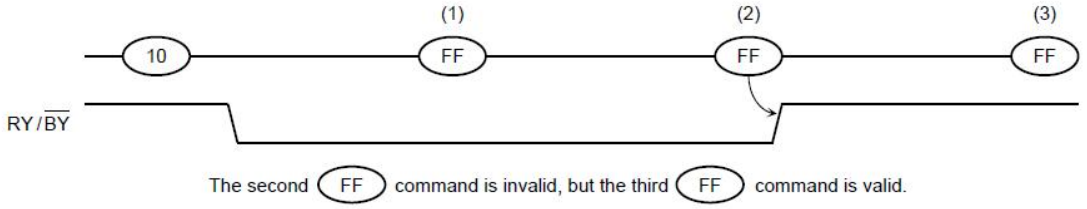


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When a Status Read command (70h) is input after a Reset



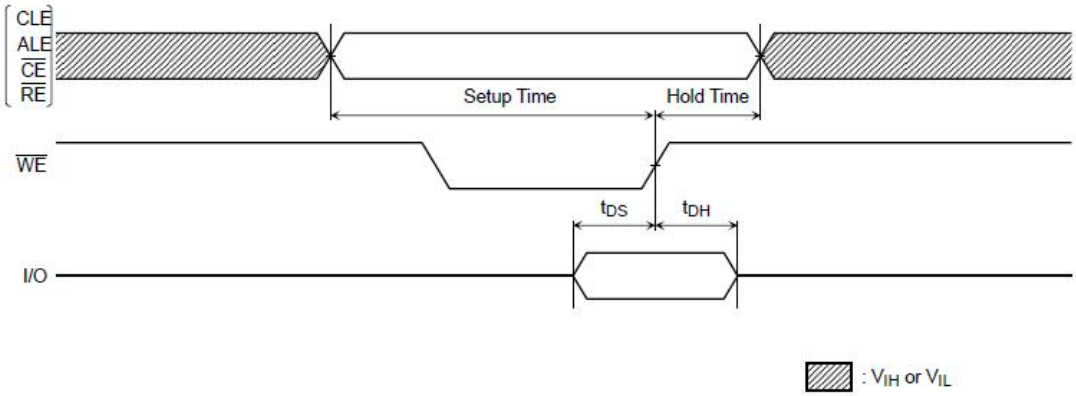
When two or more Reset commands are input in succession



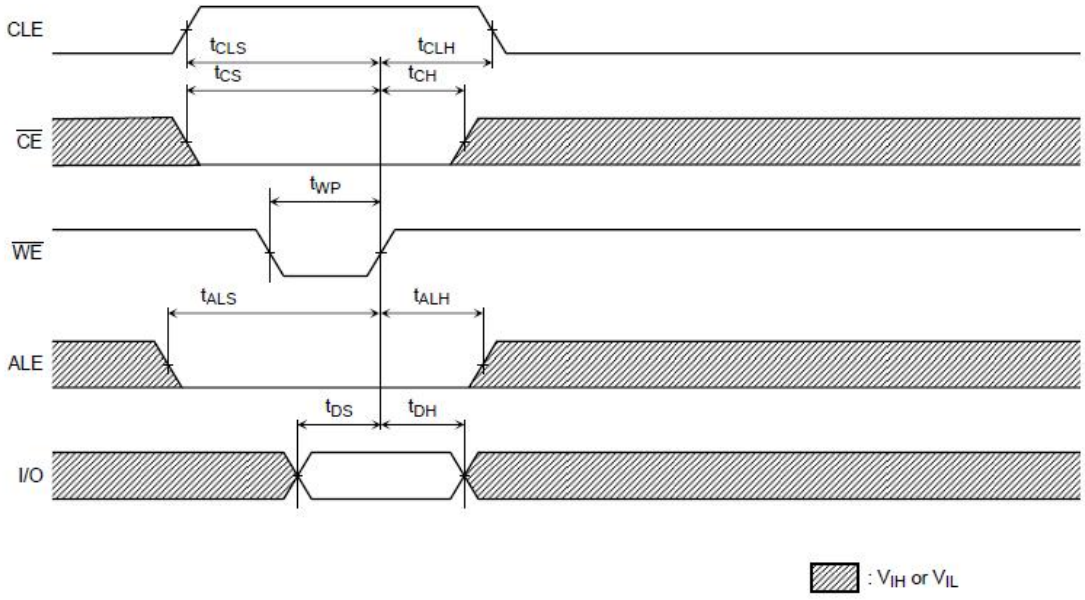
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Timing Diagrams

Latch Timing Diagram for Command/Address/Data

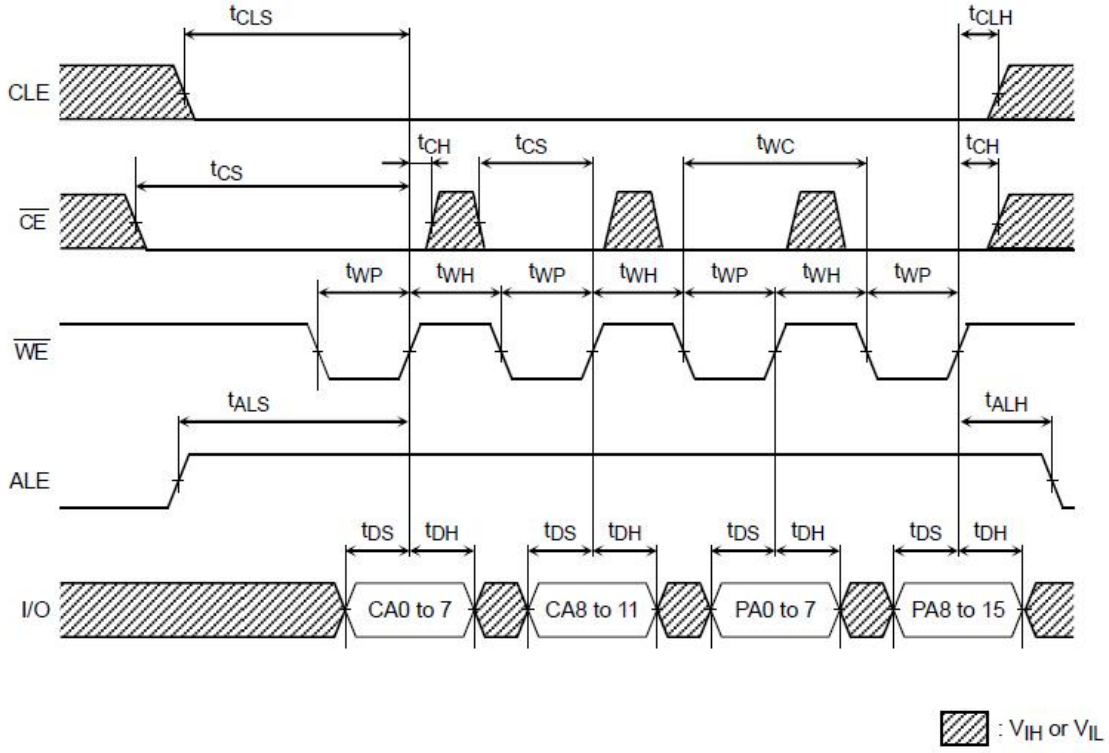


Command Input Cycle Timing Diagram

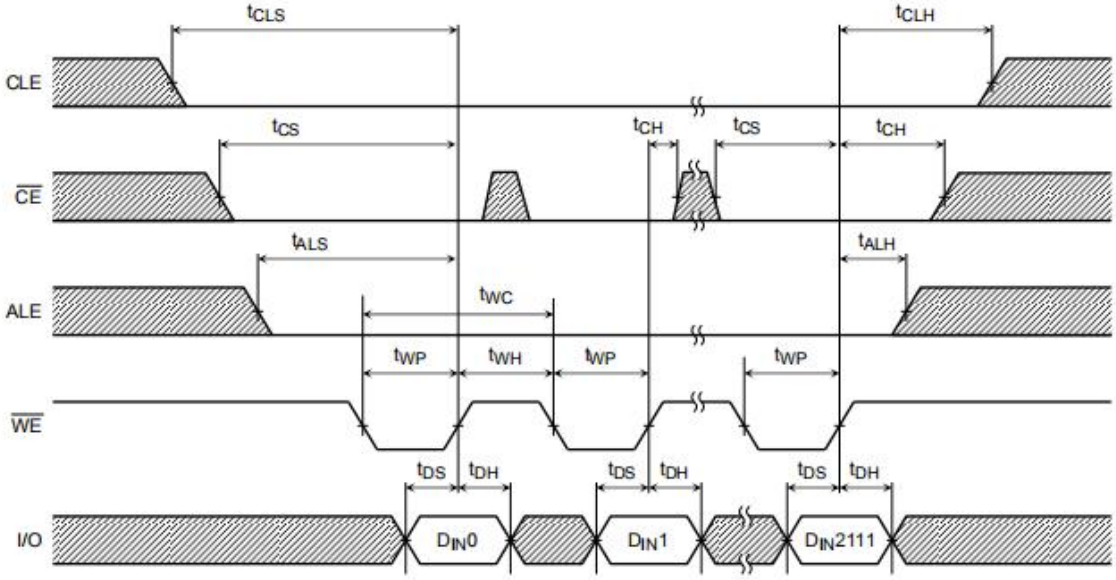


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Address Input Cycle Timing Diagram

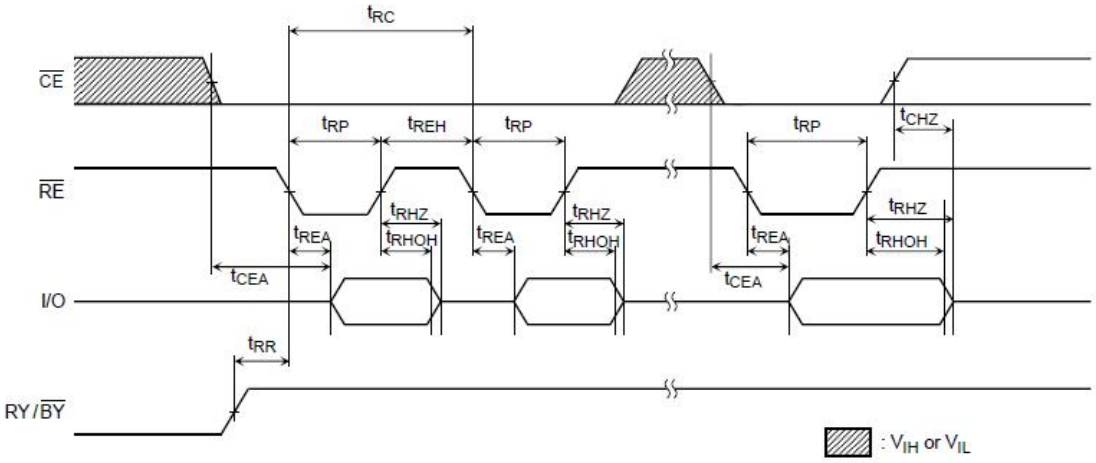


Data Input Cycle Timing Diagram

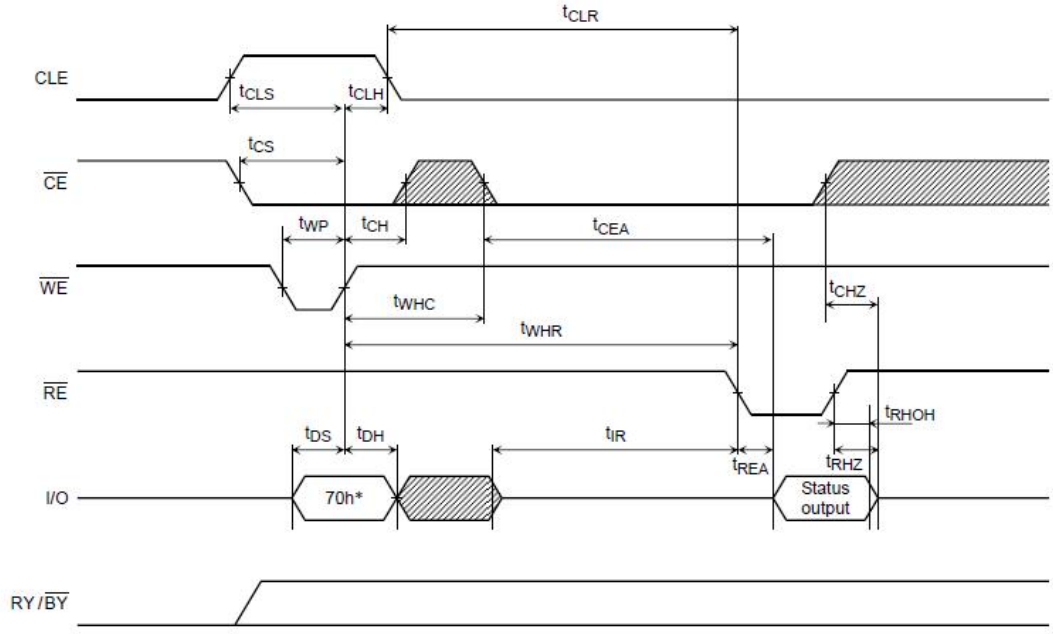


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Serial Read Cycle Timing Diagram



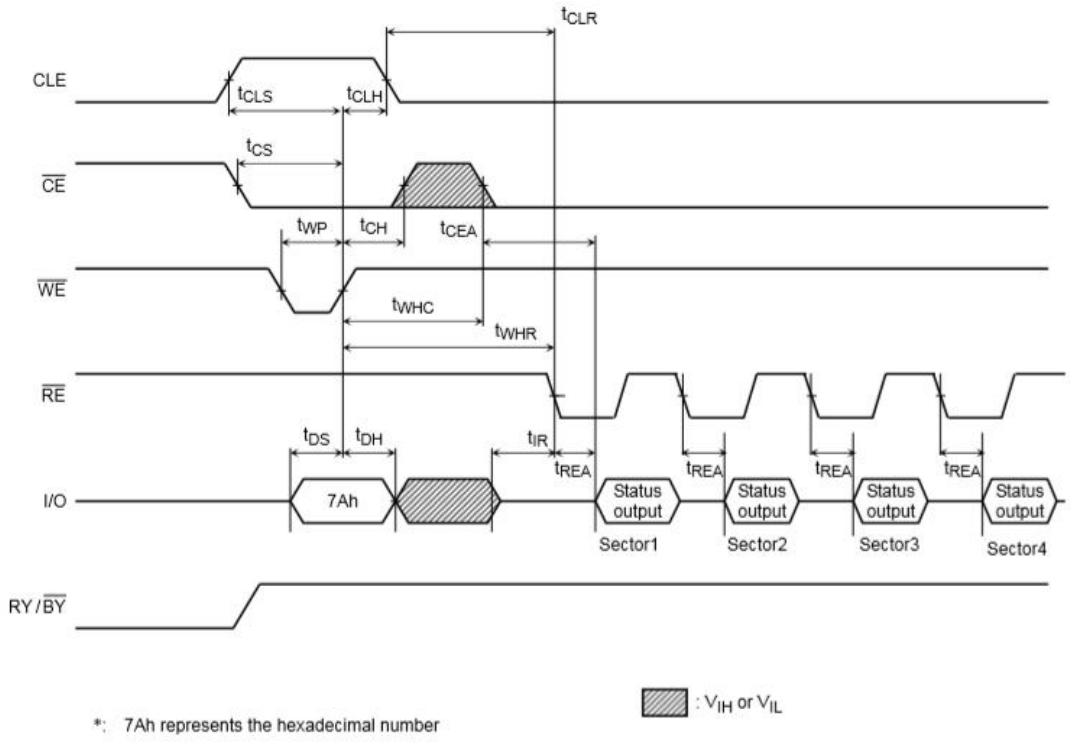
Status Read Cycle Timing Diagram



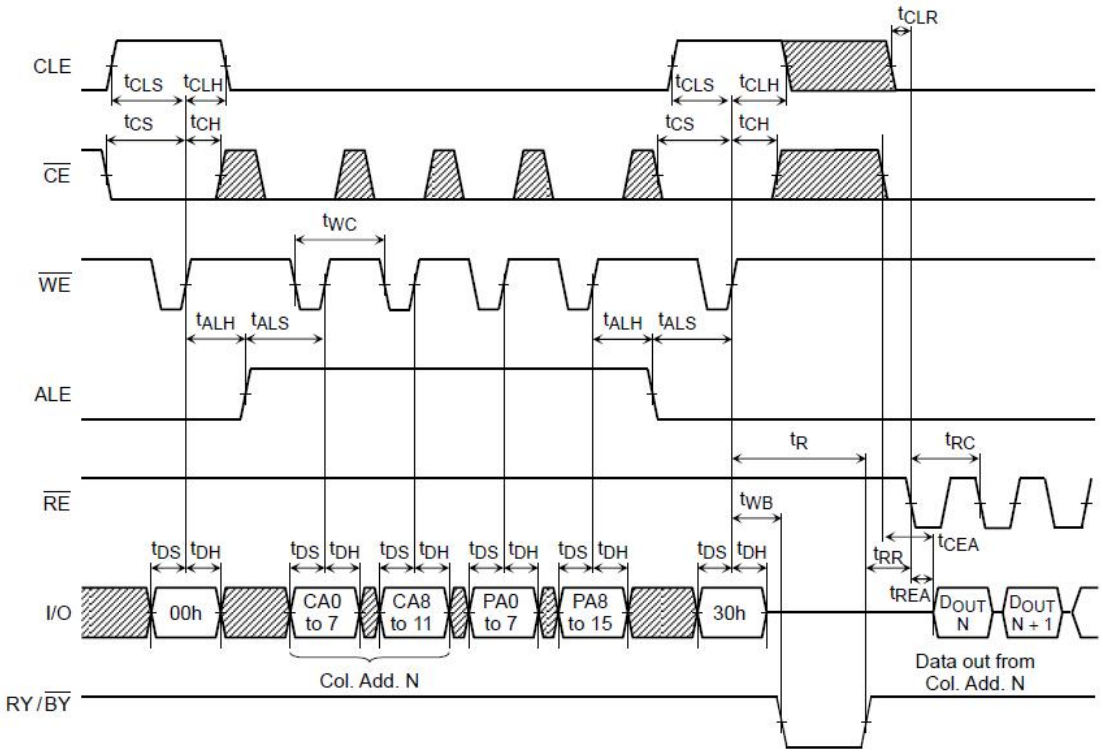
*: 70h represents the hexadecimal number

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ECC Status Read Cycle Timing Diagram

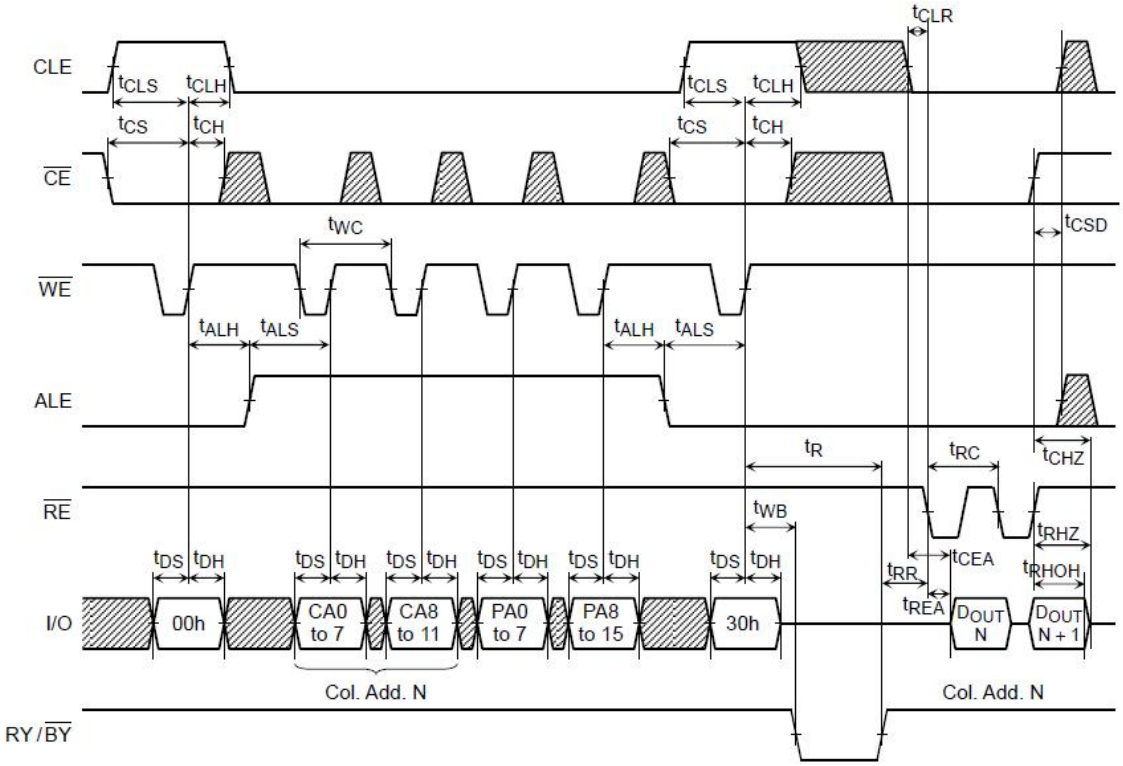


Read Cycle Timing Diagram



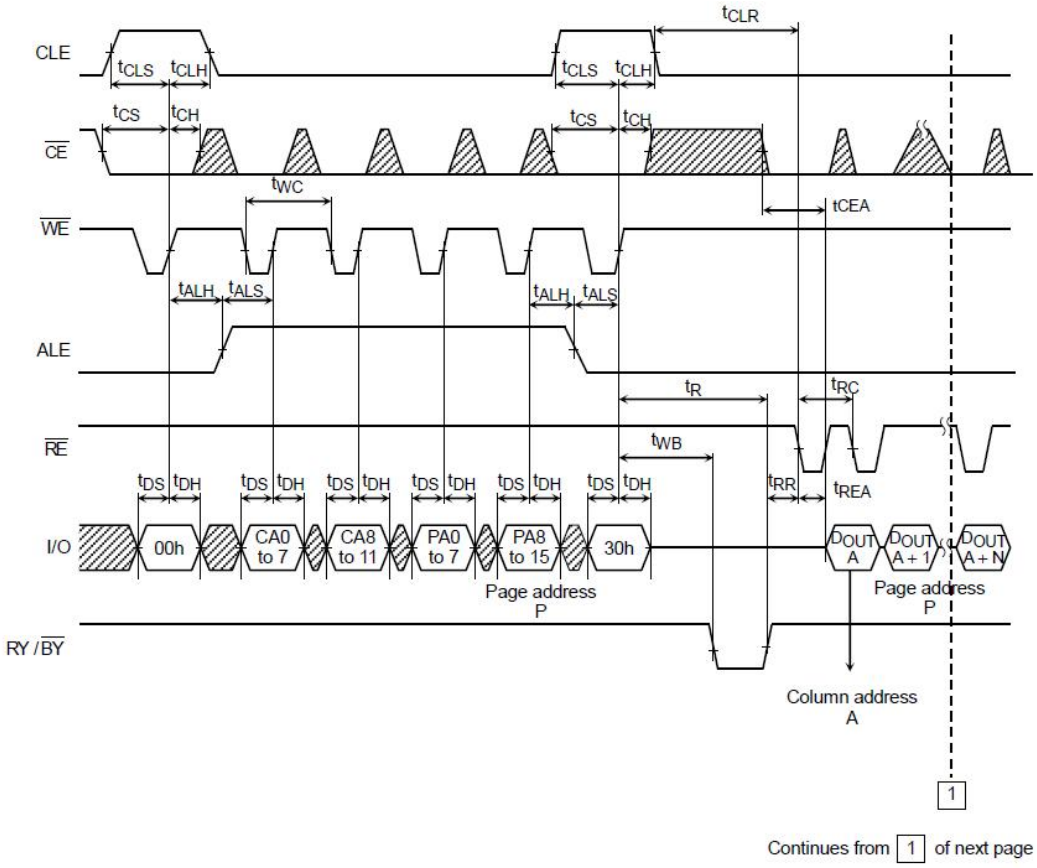
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Read Cycle Timing Diagram: When Interrupted by /CE



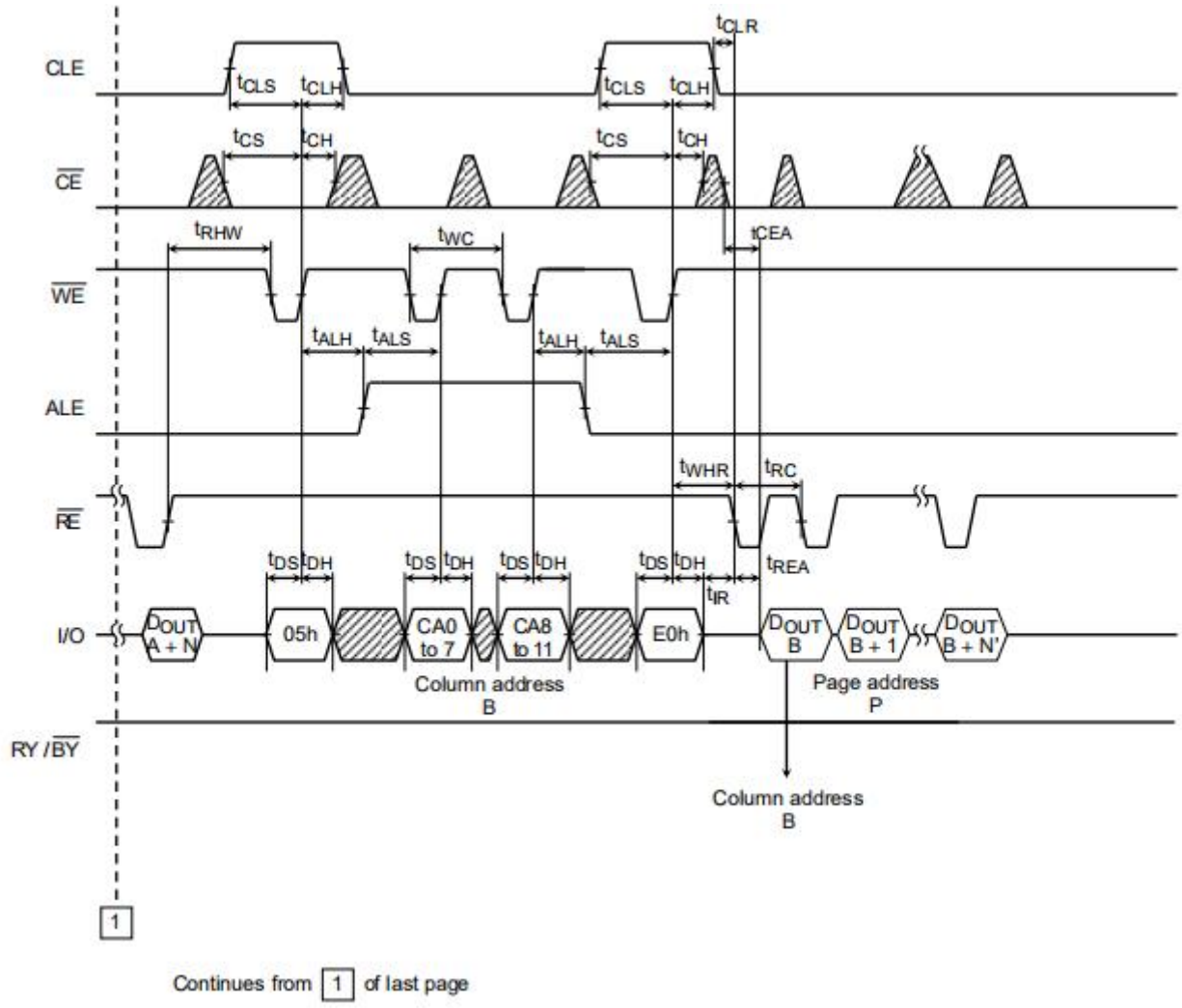
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Column Address Change in Read Cycle Timing Diagram (1/2)



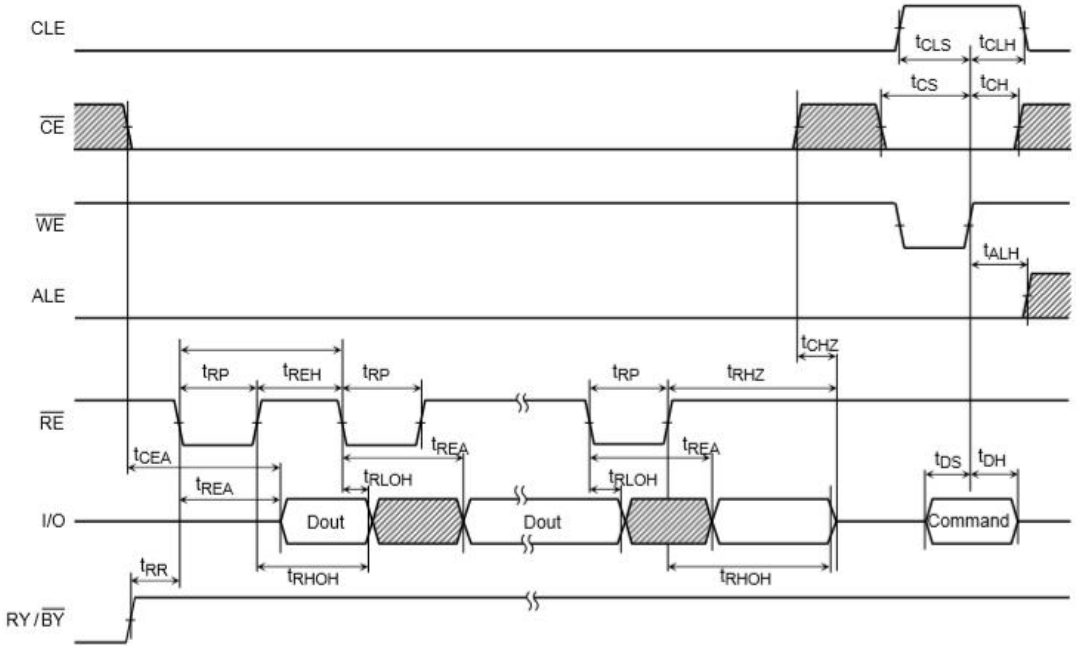
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Column Address Change in Read Cycle Timing Diagram (2/2)

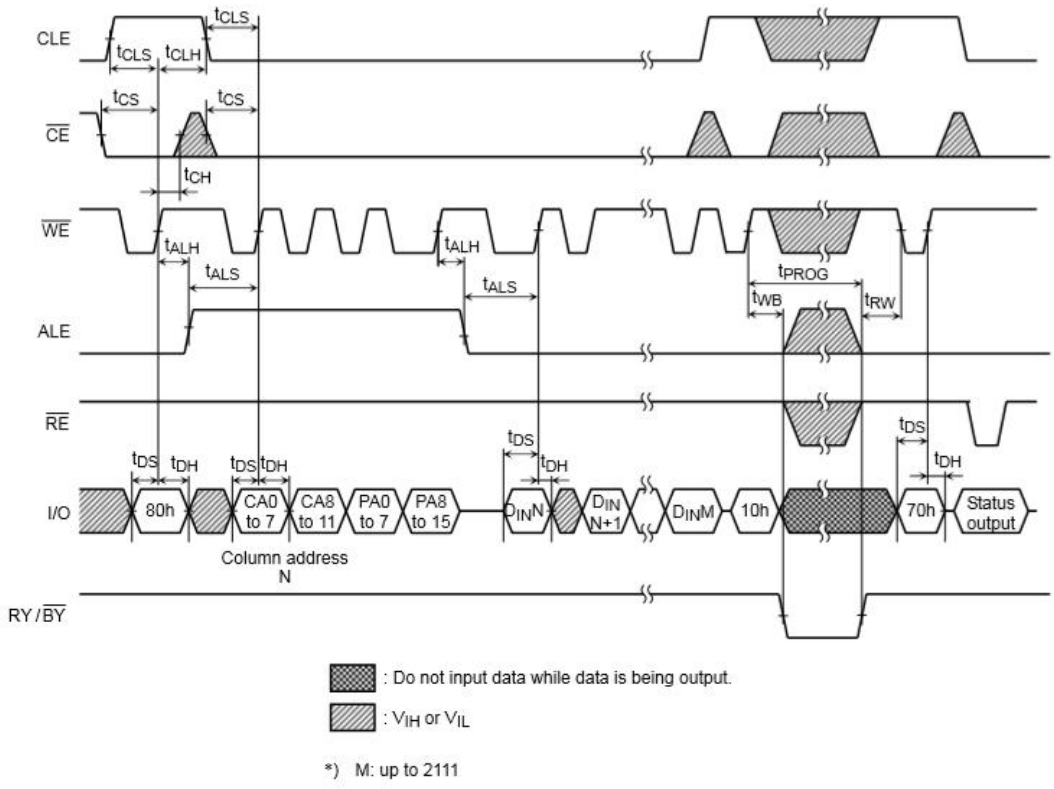


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Data Output Timing Diagram

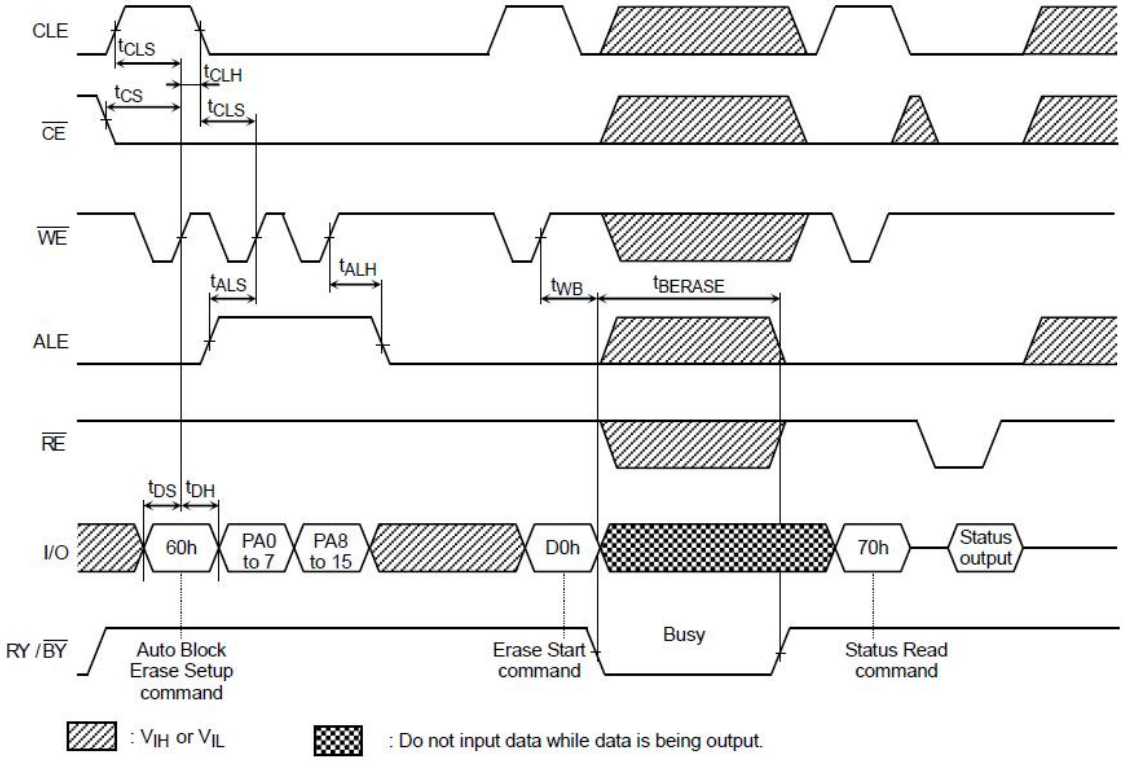


Auto-Program Operation Timing Diagram

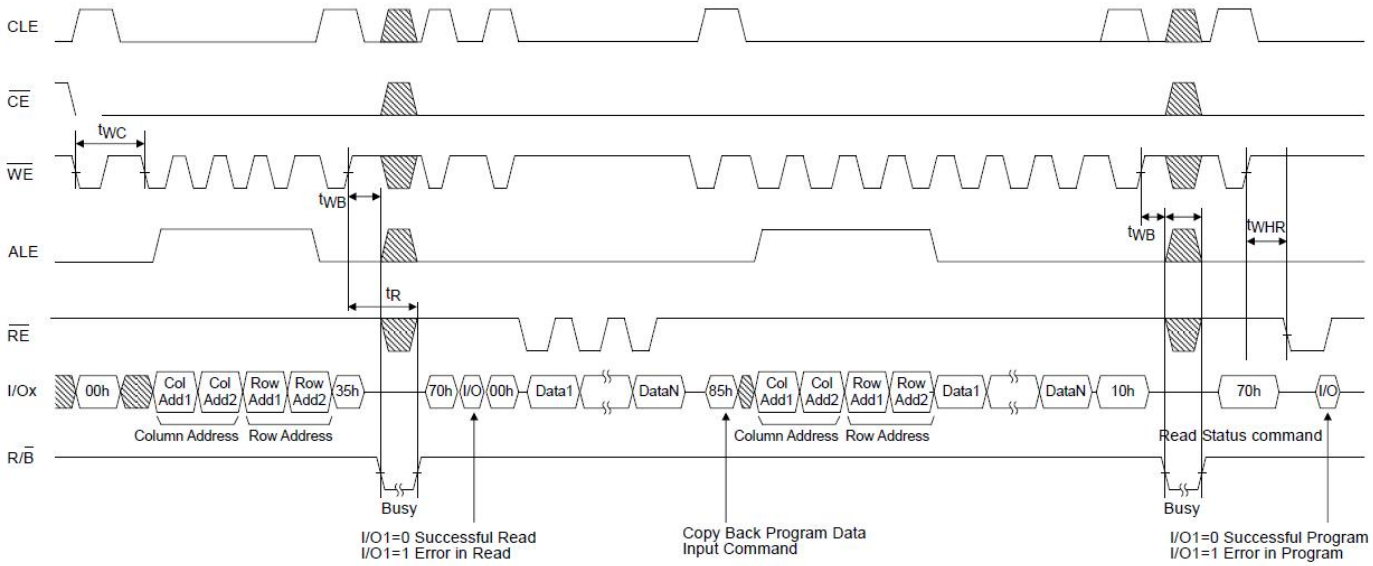


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Auto Block Erase Timing Diagram

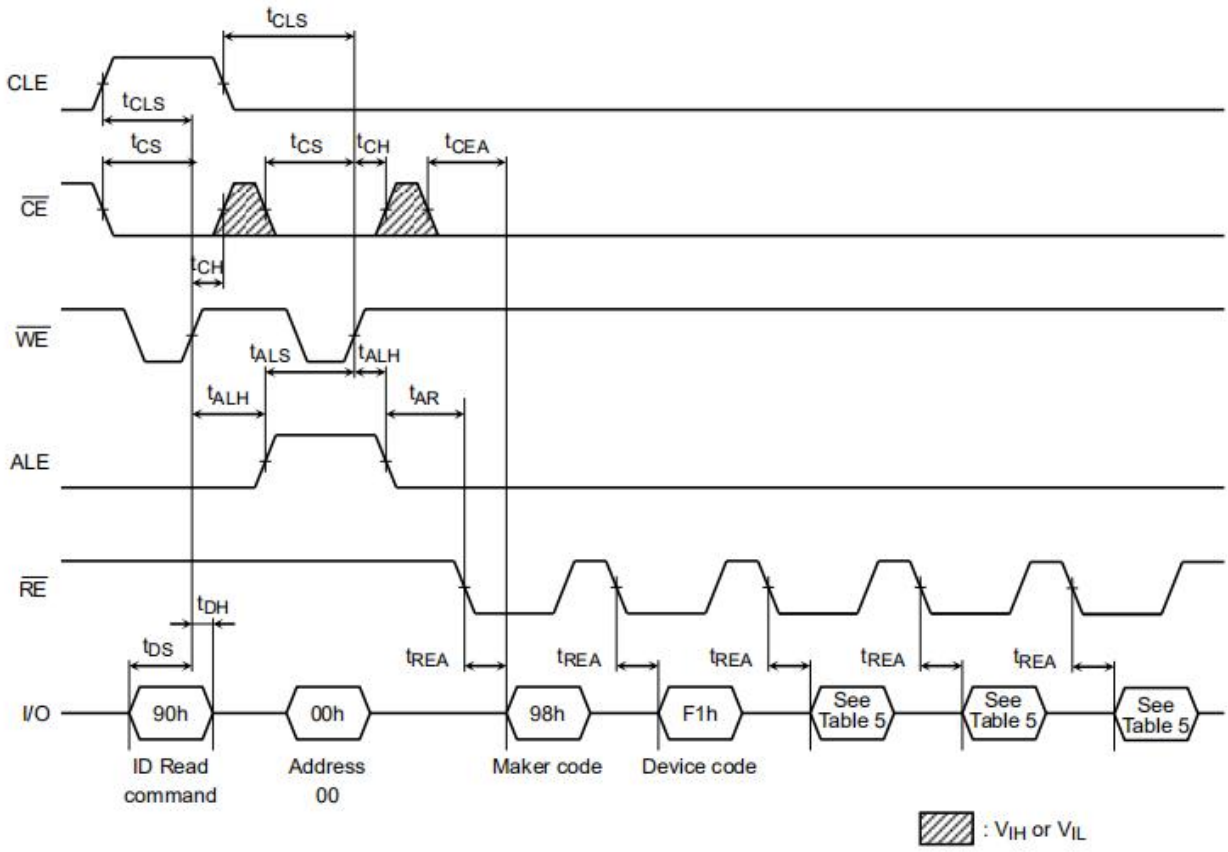


Copy back program with random data input



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ID Read Operation Timing Diagram



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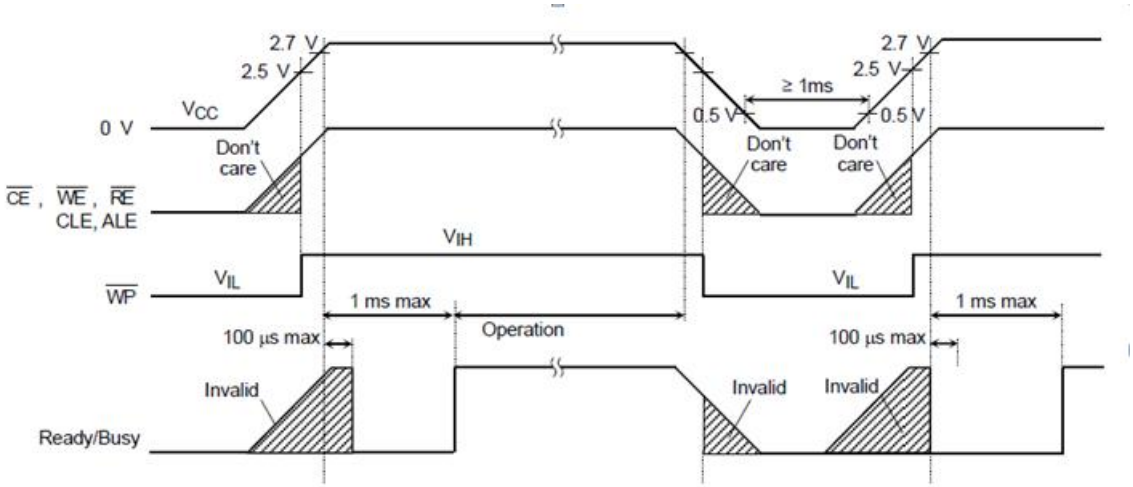
Application Notes and Comments

(1) Power-on/off sequence:

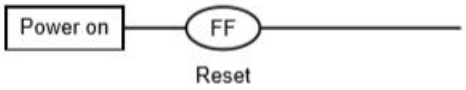
The timing sequence shown in the figure below is necessary for the power-on/off sequence.

The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. During the initialization the device Ready/Busy signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are FFh or 70h.

The WP signal is useful for protecting against data corruption at power-on/off.



(2)Power-on Reset The following sequence is necessary because some input signals may not be stable at power-on.



(3) Prohibition of unspecified commands

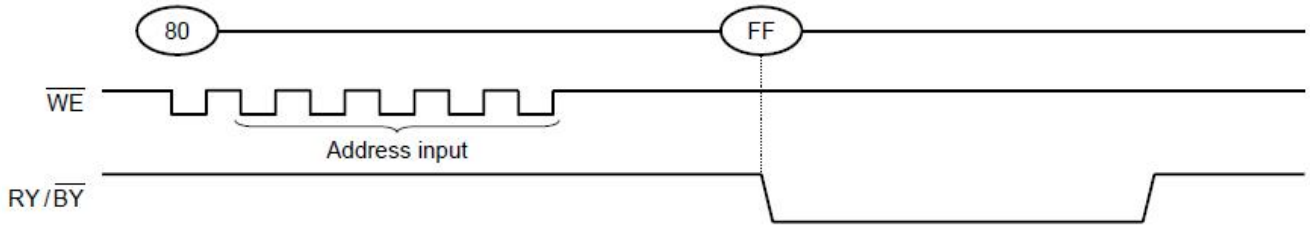
The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

(4) Restriction of commands while in the Busy state

During the Busy state, do not input any command except 70h and FFh.

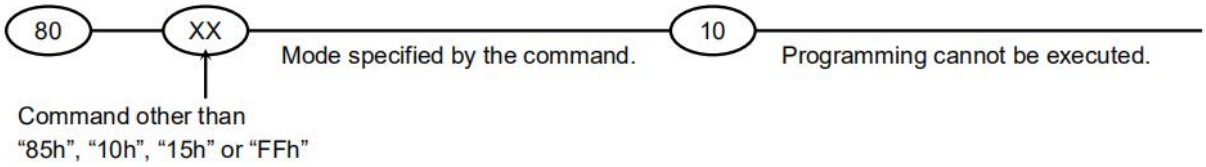
(5) Acceptable commands after Serial Input command “80h”

Once the Serial Input command “80h” has been input, do not input any command other than the Column Address Change in Serial Data Input command “85h”, Auto Program command “10h”, Auto Program with Data Cache Command “15h”, or the Reset command “FFh”.



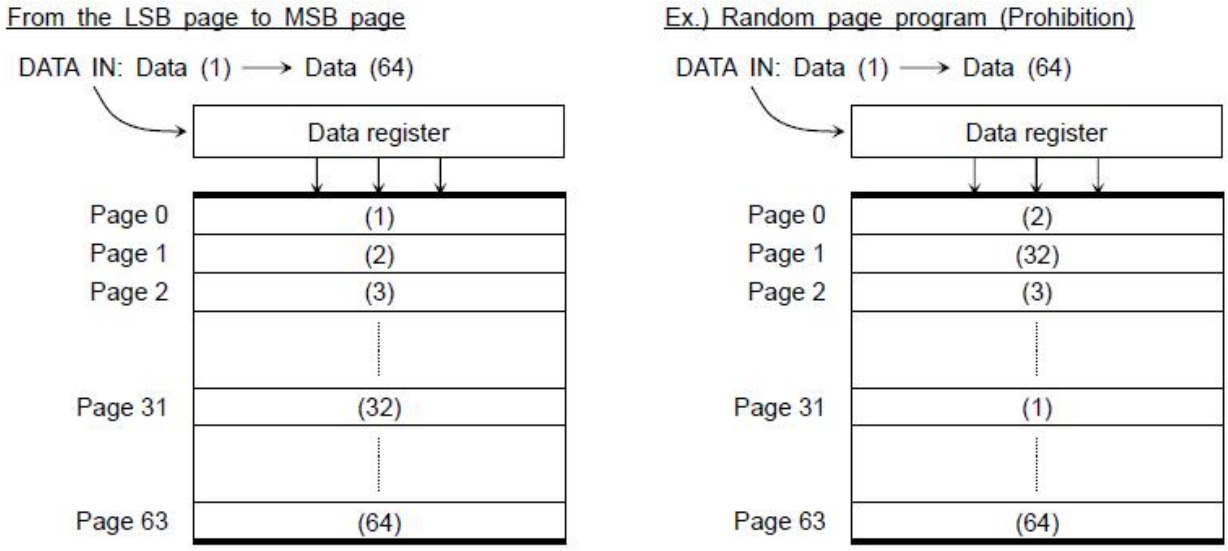
If a command other than “85h” , “10h” , “15h” or “FFh” is input, the Program operation is not performed and the device operation is set to the mode which the input command specifies.

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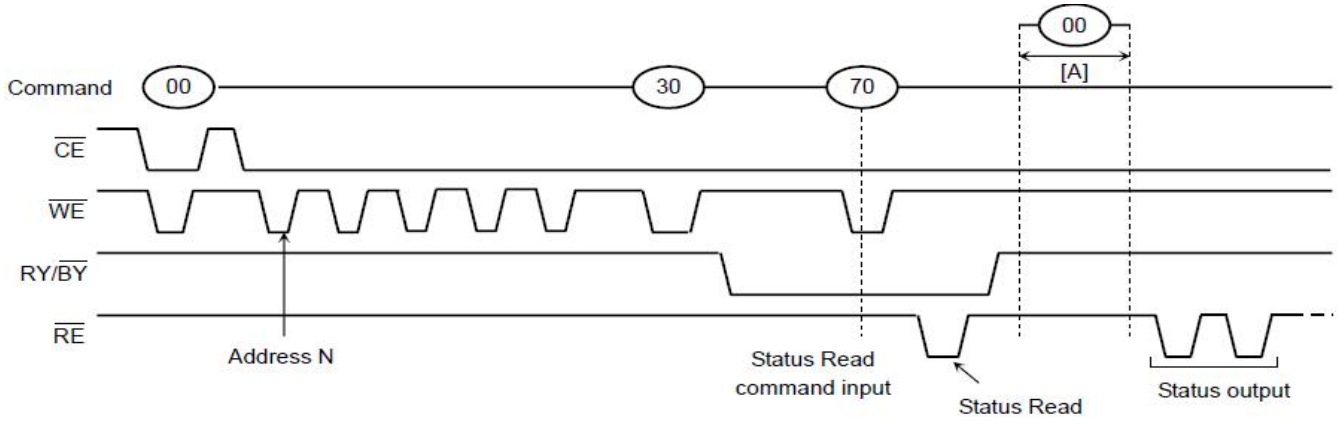


⑹ Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.



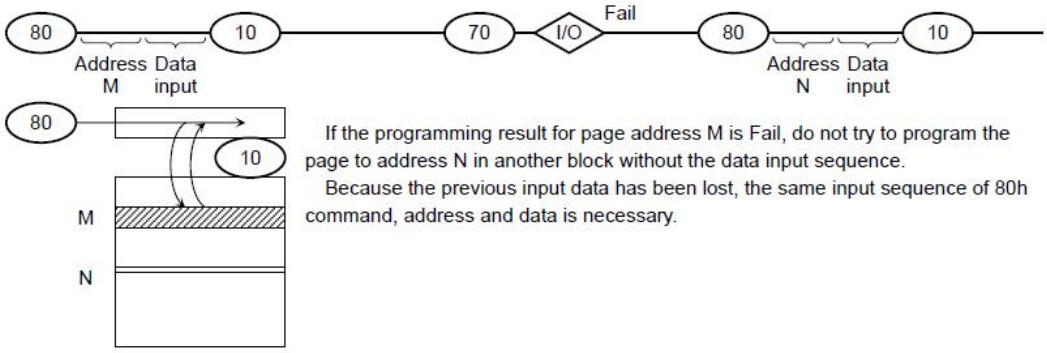
⑺ Status Read during a Read operation



The device status can be read out by inputting the Status Read command “70h” in Read mode. Once the device has been set to Status Read mode by a “70h” command, the device will not return to Read mode unless the Read command “00h” is inputted during [A]. If the Read command “00h” is inputted during [A], Status Read mode is reset, and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary

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⑧ Auto programming failure

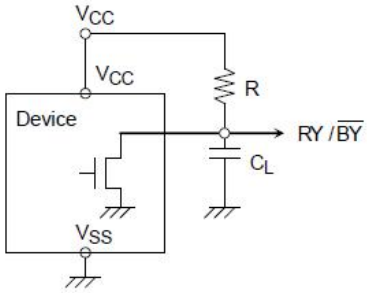


If the programming result for page address M is Fail, do not try to program the page to address N in another block without the data input sequence.

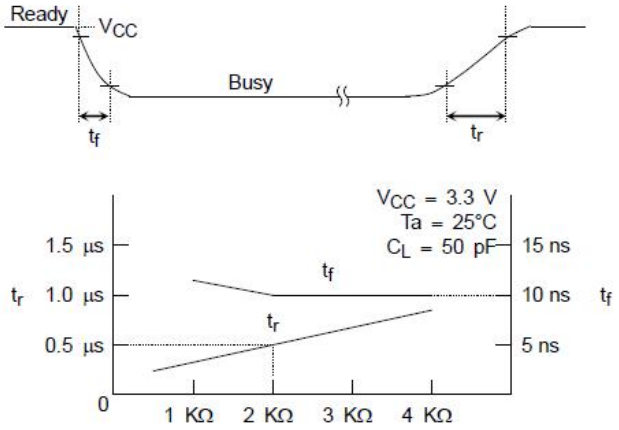
Because the previous input data has been lost, the same input sequence of 80h command, address and data is necessary.

⑨ RY / BY# : termination for the Ready/Busy pin (RY / BY#)

A pull-up resistor needs to be used for termination because the RY / BY# buffer consists of an open drain circuit.



This data may vary from device to device.
We recommend that you use this data as a reference when selecting a resistor value.

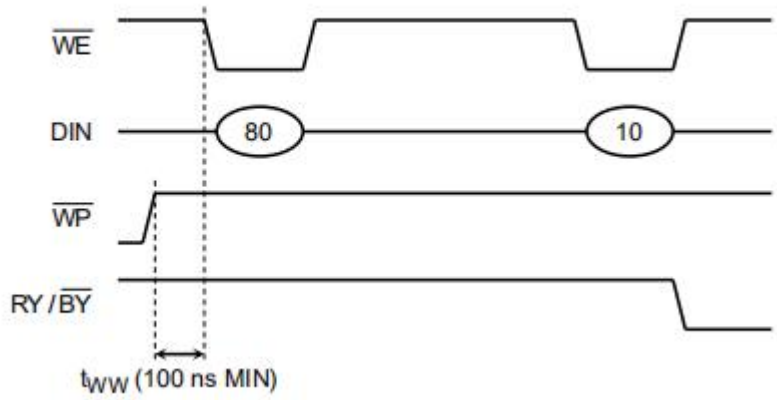


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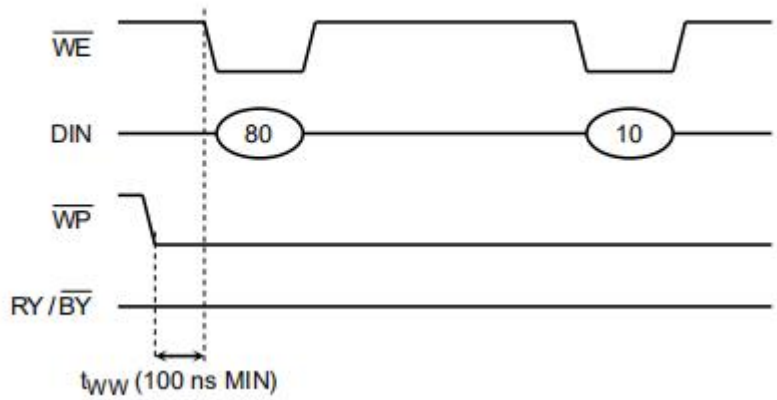
(10) Note regarding the WP# signal

The Erase and Program operations are automatically reset when WP# goes Low. The operations are enabled and disabled as follows:

Enable Programming

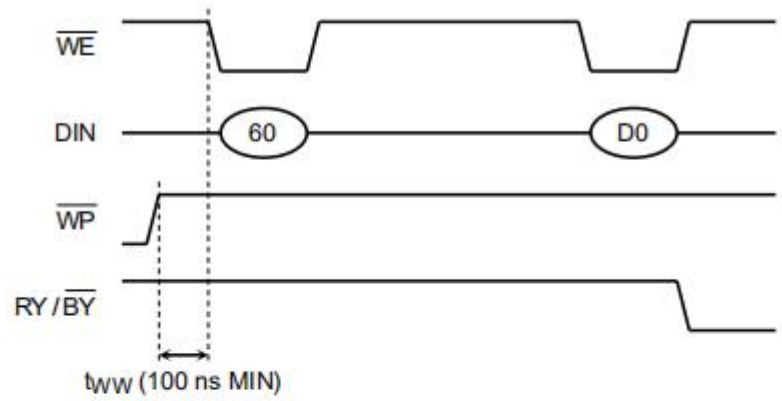


Disable Programming

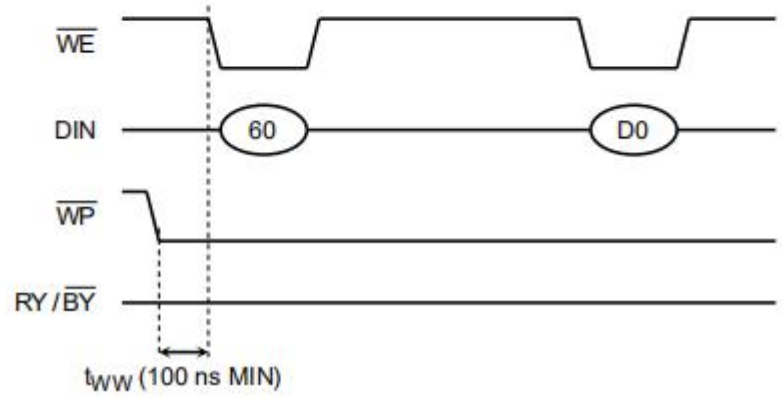


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Enable Erasing



Disable Erasing

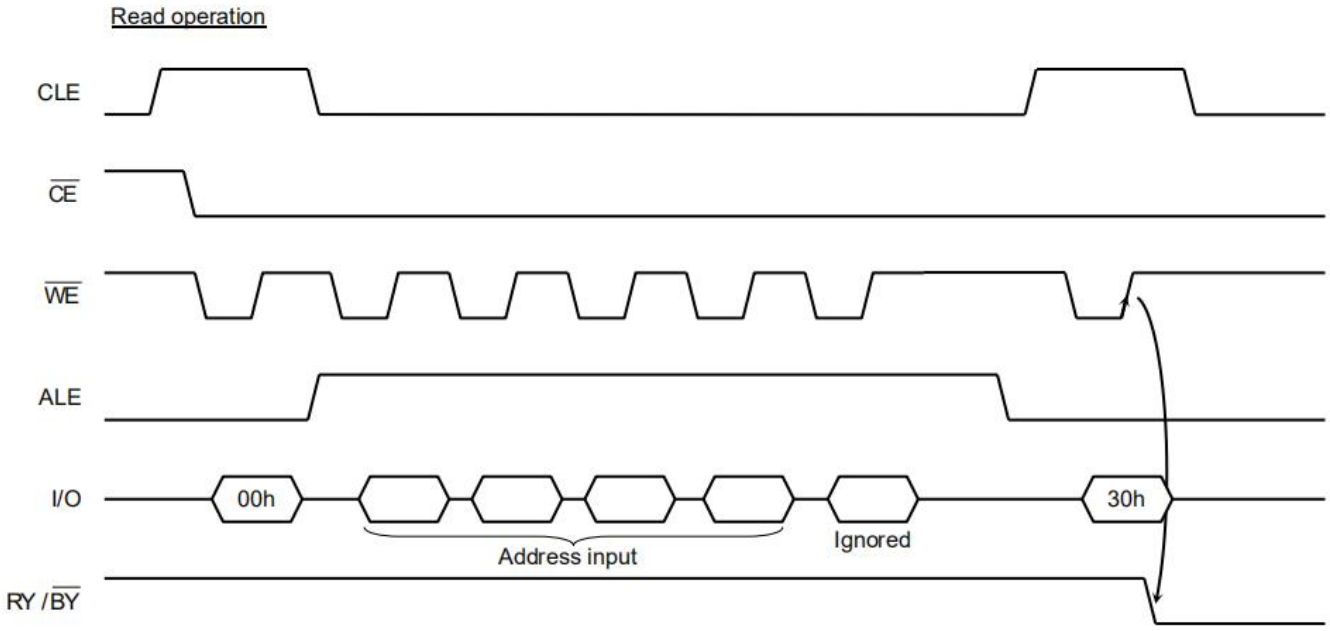


(11) When five address cycles are input

Although the device may read in a fifth address, it is ignored inside the chip.

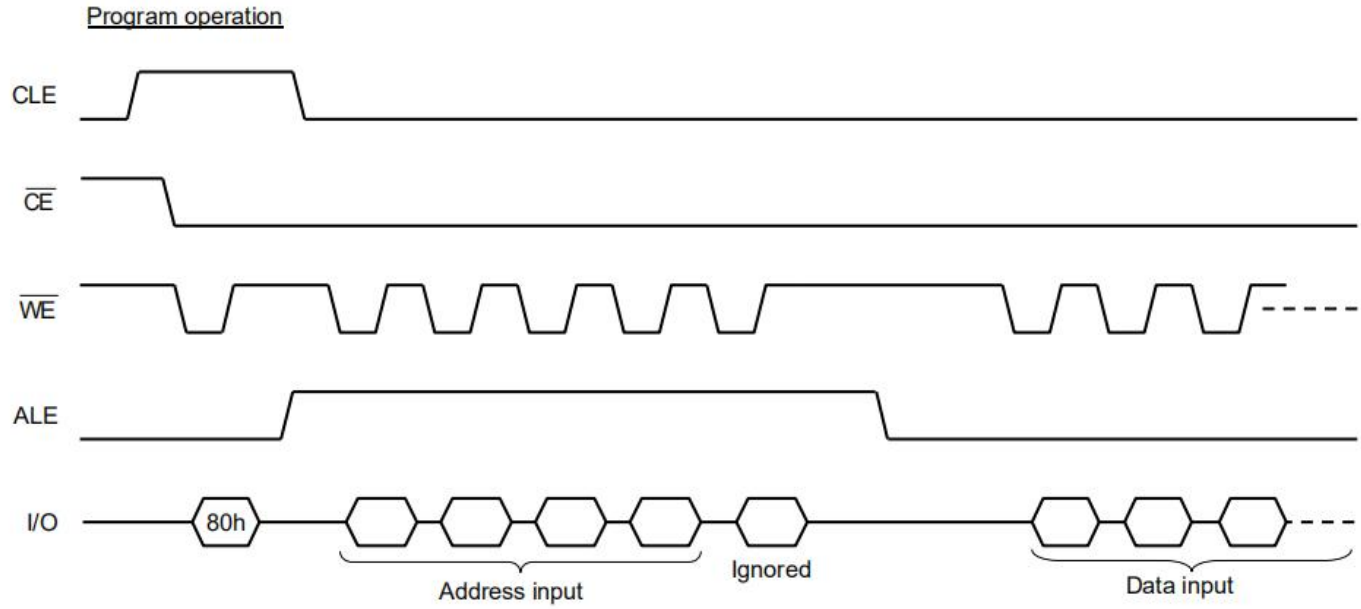
Read operation

Read operation



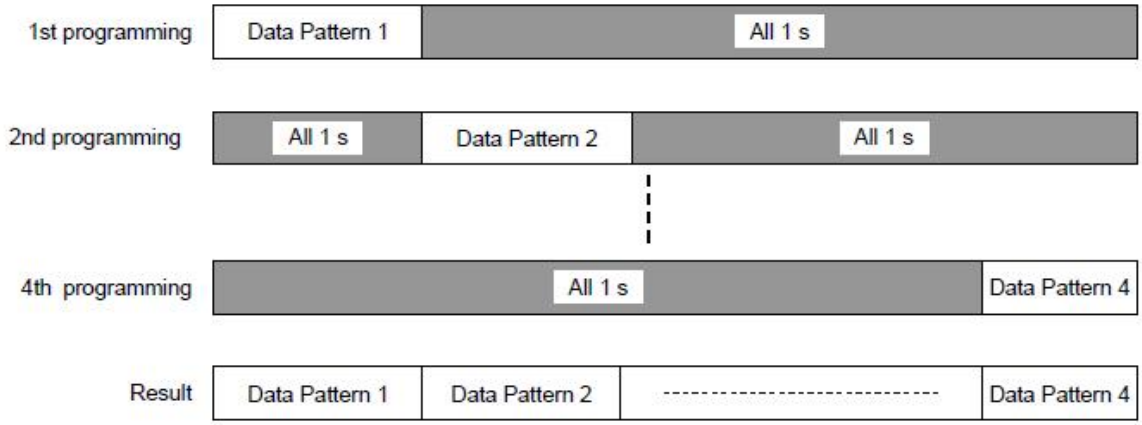
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Program operation



(12) Several programming cycles on the same page (Partial Page Program)

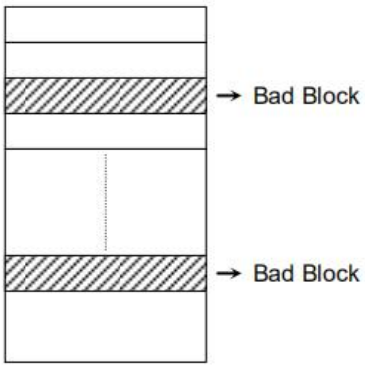
Each segment can be programmed individually as follows:



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(13) Invalid blocks (bad blocks)

The device occasionally contains unusable blocks. Therefore, the following issues must be recognized:



Please do not perform an erase operation to bad blocks. It may be impossible to recover the bad block information if the information is erased.

Check if the device has any bad blocks after installation into the system. Refer to the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

A bad block does not affect the performance of good blocks because it is isolated from the bit lines by select gates.

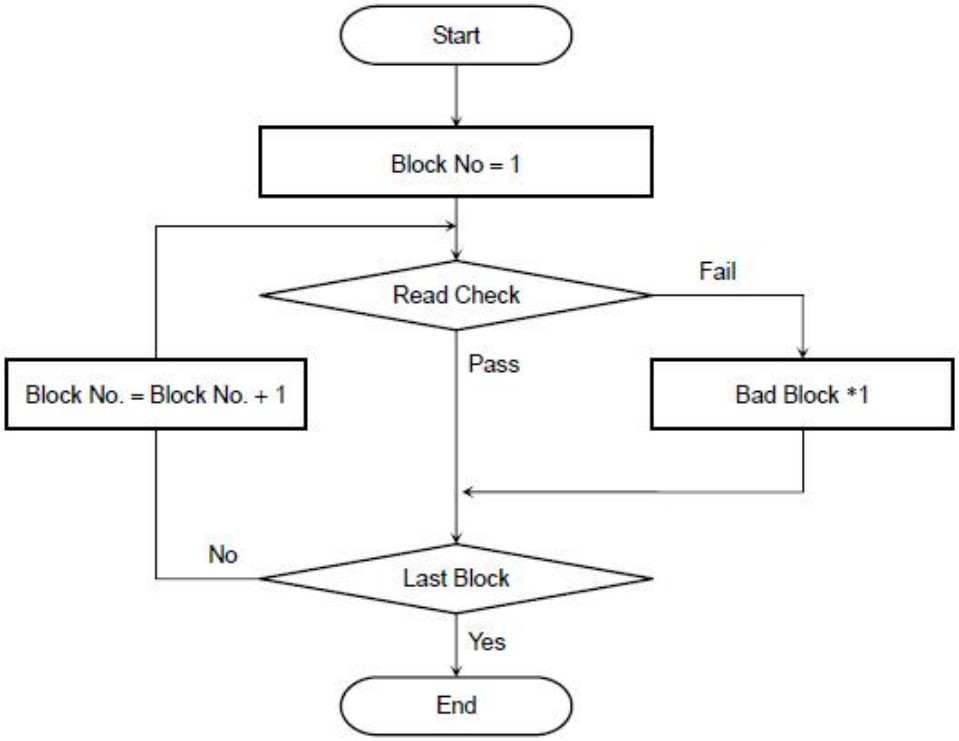
The number of valid blocks over the device lifetime is as follows:

	MIN	TYP.	MAX	UNIT
Valid (Good) Block Number	1004	—	1024	Block

Bad Block Test Flow

Regarding invalid blocks, bad block mark is in whole pages.

Please read one column of any page in each block. If the data of the column is 00(Hex), define the block as a bad block.



*1: No erase operation is allowed to detected bad blocks

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(14) Failure phenomena for Program and Erase operations

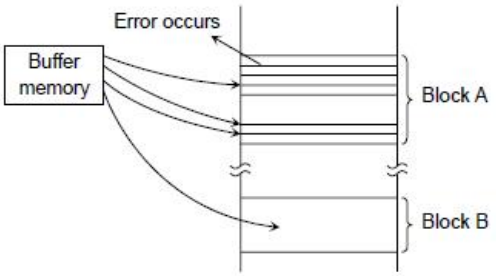
The device may fail during a Program or Erase operation.

The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Read	9bit Failure(uncorrectable error)	Uncorrectable ECC error

- ECC: Error Correction Code. 8 bit correction per 528 Bytes is executed in a device.
- Block Replacement

Program



When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using another appropriate scheme).

Erase

When an error occurs during an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

(15) Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.

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