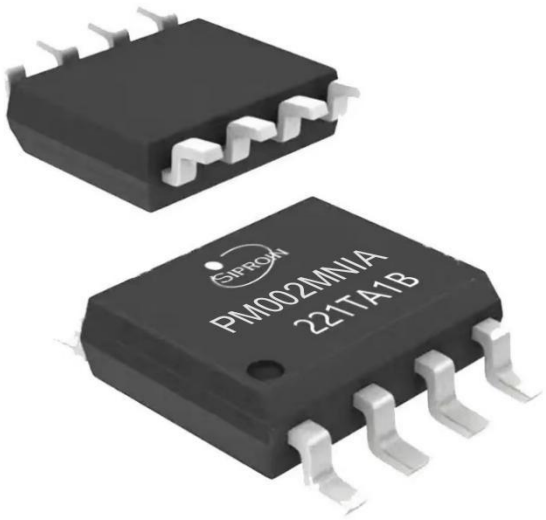
STT-MRAM Datasheet

PM002MNIA



Version:1.34

Jan. 2026

Shanghai Siproin Microelectronics

http://www.siproin.com

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扫码查规格书

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1 Features

The PM002M is Mbit of SPI/QPI (serial/quad parallel interface) MRAM device. This device is configurable as 1 bit I/O separate or 4 bits I/O common interface. The PM002M has MRAM technology in memory array. The data in the memory array will be sustained with data retention greater than 20 years.

Density

- 2Mbit

Fast SPI interface

- Up to 50MHz clock frequency @SPI SDR
- Up to 50MHz clock frequency @QPI SDR
- Support standard SPI, Quad SPI mode
- Write no delay
- Support SPI mode0 and mode3

Single voltage operation

- Typical Voltage：3.3V　Vcc=2.7V~3.6V

Data protection

- Software protection mode with BP0,BP1 in mode register#1

Power consumption

- Sleep current 2uA (Typical value)
- Standby current 2mA (Typical value)
- Active current 4.3mA (Typical value @SPI 50MHz)

Reliability

- Data retention >20years @85℃
- P/E cycle up to 10^8

Package

- SOP8_150MIL

Temperature range

- Junction temperature: -40℃~85℃

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2 Pin Information

2.1 SOP8

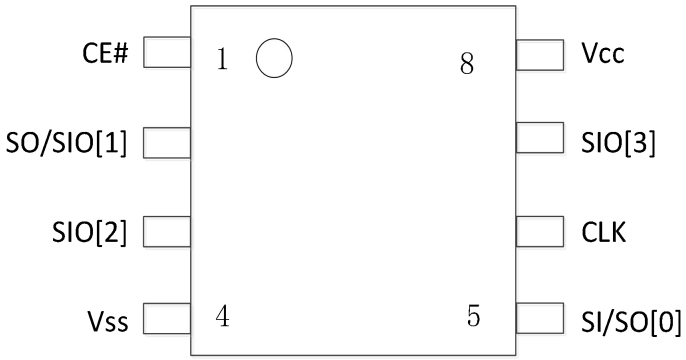


Figure 1: Package Information

3 Pin Description

Table1: Pin Description

Symbol	Signal Type	SPI Mode	QPI Mode
CE#	Input	Chip select signal,Active low.When CE input is high ,Memory will be in standby state	
SO/SIO[1]	I/O	Serial output	I/O[1]
SIO[2]	I/O	I/O[2]*	I/O[2]
Vss	Ground	Core Supply Ground	
SI/SO[0]	I/O	Serial intput	I/O[0]
CLK	Input	Clock Signal	
SIO[3]	I/O	I/O[3]*	I/O[3]
Vcc	Power	Core Power Supply	

*Fast read Quad access and Quad write access in SPI Mode use SIO[2] and SIO[3]；
Recommend to pull down Vcc or to GND if no use of SIO[2] and SIO[3] in SPI Mode;

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4 Operation Flow

According SPI protocol, the first 8 bits of DI is COMMAND (op_code), which define which operation the memory will do. The following 24bits (3 bytes) are address phase, which defined the memory array row address and column address. According current array density, PM002M use 17 of 24 address to feed in memory address, and left spare MSB bit with '0'.

Every command sequence starts with a one-byte command code. Depending on the command, this might be followed by 3-byte (24-bit) address plus dummy cycles and data byte(s).

All commands, addresses, and dummy bits are shifted in of the PM002M device with the most significant bit first. The data bits are also shifted in or out of the PM002M with the most significant bit.

The figure below explains relation between internal memory array organization and external I/O. This device has 16 internal I/O plates. Once memory read or write operation starts, these 16 internal I/O plates works parallelly. Because of this internal memory plates organization, the minimum burst access for read or write operation becomes 2 Bytes access.

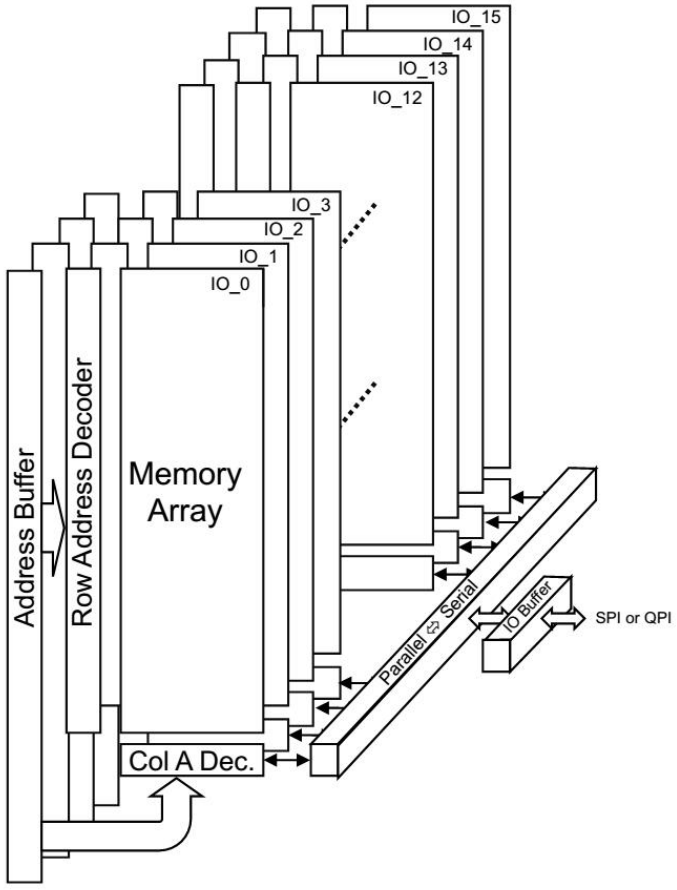


Figure 2: Operation Flow

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5 SPI mode commands

Table 2: SPI Mode Commands

Command	SPI Mode						
	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7
Number of Clocks	8	8(or 2)	8(or 2)	8(or 2)	8(or 2)	8(or 2)	8(or 2)
Mode Register Write	B1H	A23-A16	A16-A8	A7-A0	Value#n		
Mode Register Read	B5H	A23-A16	A16-A8	A7-A0	Value#n		
Write	02H	A23-A16	A16-A8	A7-A0	D15-D8	D7-D0	
Quad Write	38H	A23-A16	A16-A8	A7-A0	D15-D8	D7-D0	
Read	03H	A23-A16	A16-A8	A7-A0	Dummy(0~12)	D15-D8	D7-D0
Quad Read	EBH	A23-A16	A16-A8	A7-A0	Dummy(0~12)	D15-D8	D7-D0
Write Enable	06H						
Write Disable	04H						
Entry To Deep PowerDown	B9H						
Exit From Deep PowerDown	ABH						
Read Unique ID Register	9FH	0H	0H	0H	16 Bytes		
Enter QPI Mode	35H						
Reset Enable	66H						
Reset	99H						

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5.1 Control Command Operation

Control command include WriteEnable,WriteDisable,Entry To Sleep,Exit From Sleep,

Enter QPI Mode. For example Enter QPI Mode:

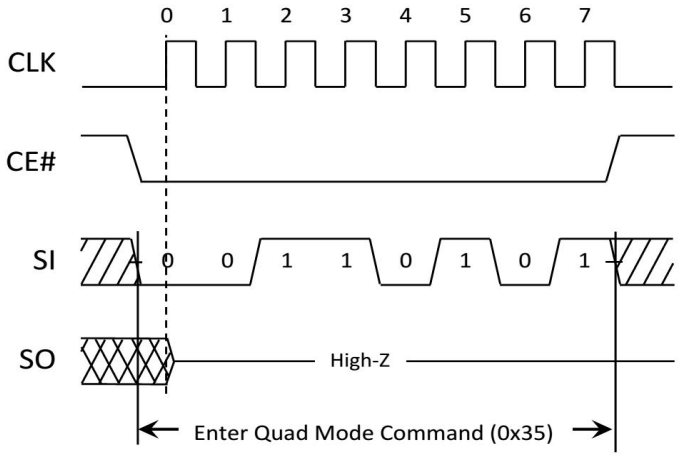


Figure 3: Enter QPI Command Timing

5.2 Reset Operation

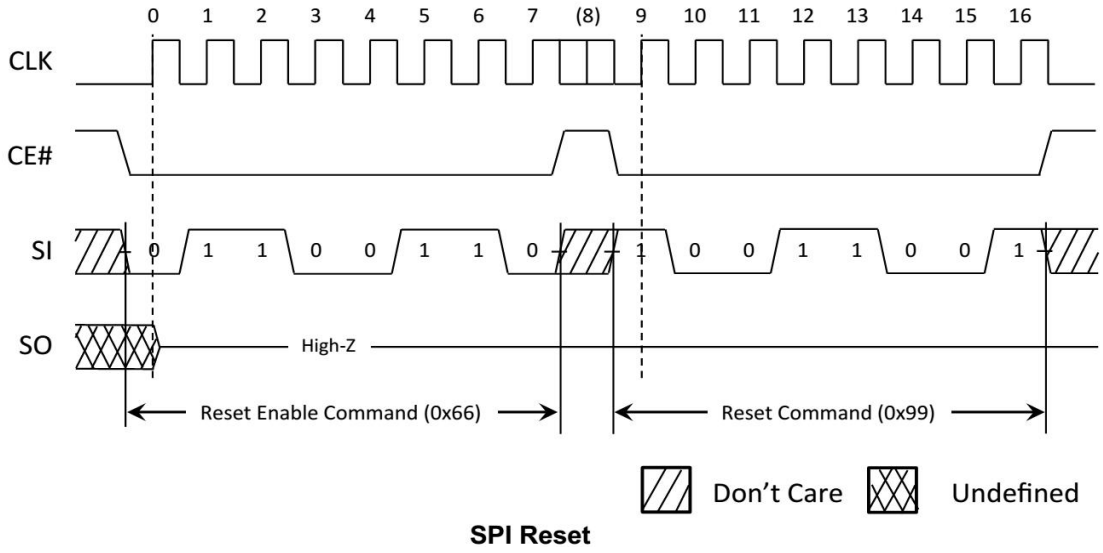


Figure 4: SPI Reset Operation Timing

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5.3 Mode Register Write Command Timing

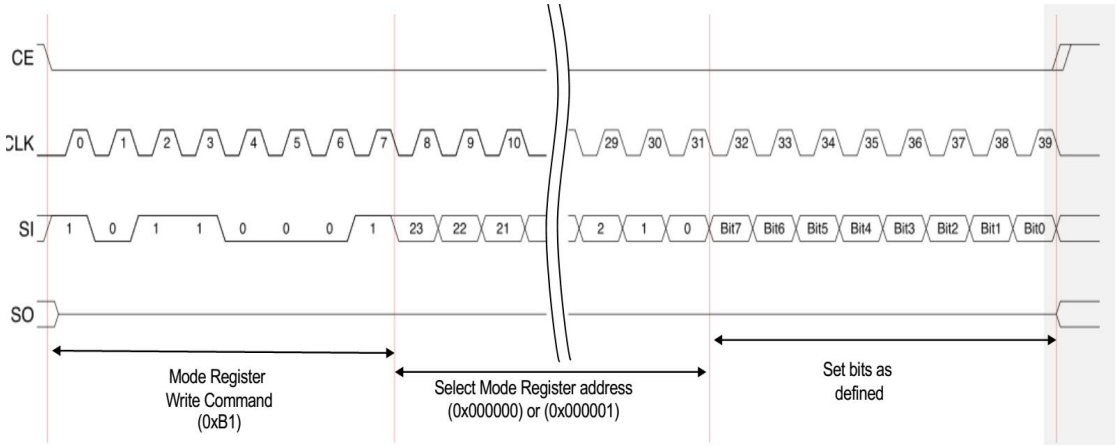


Figure 5: SPI Mode Register Write Command Timing

5.4 Mode Register Read Command Timing

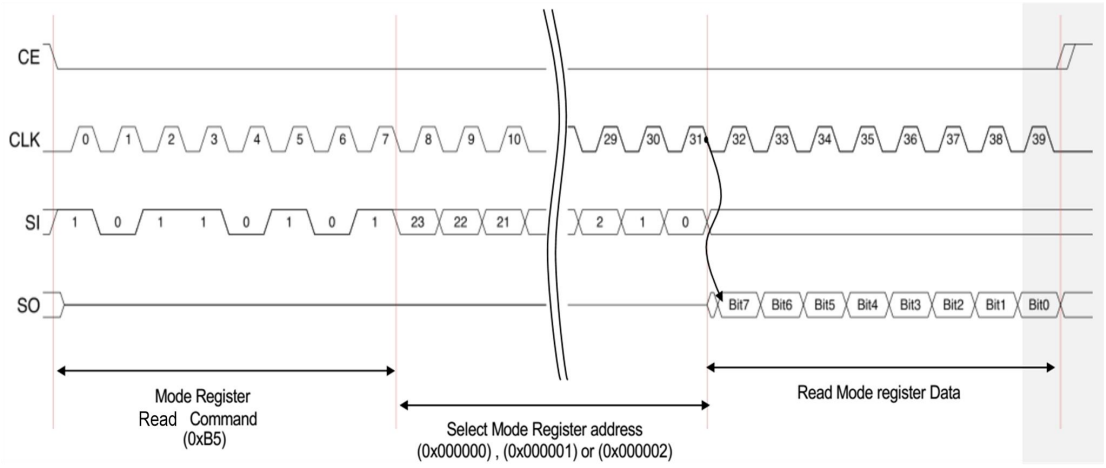


Figure 6: SPI Mode Register Read Command Timing

5.5 SPI Write Command Timing

The first byte(Bit7~Bit0) means IO_15~IO_8, the followed byte(Bit7~Bit0) means IO_7~IO_0 .

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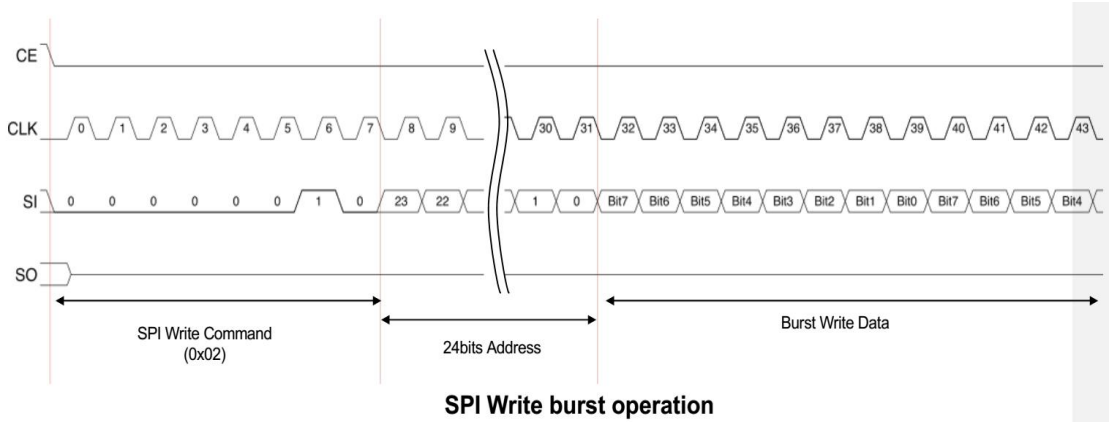


Figure 7: SPI Write Command Timing

5.6 SPI Read Command Timing

The first byte(Bit7~Bit0) means IO_15~IO_8, the followed byte(Bit7~Bit0) means IO_7~IO_0 .

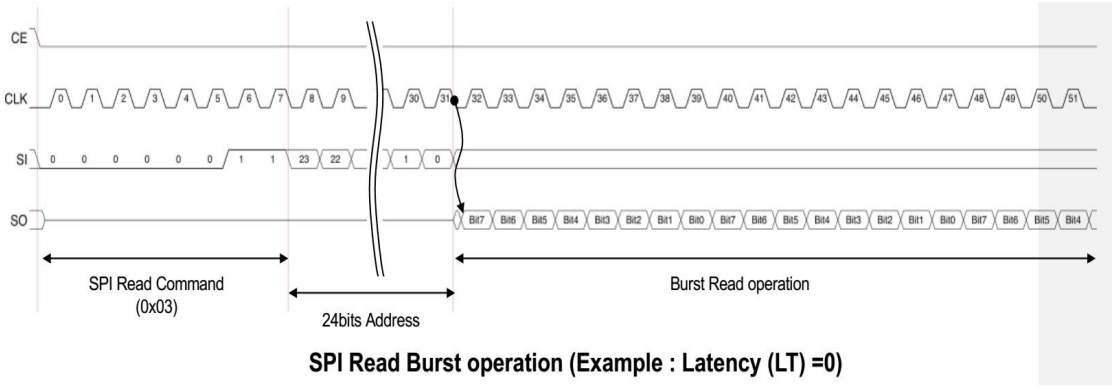


Figure 8: SPI Read Command Timing (Example: Latency(LT)=0)

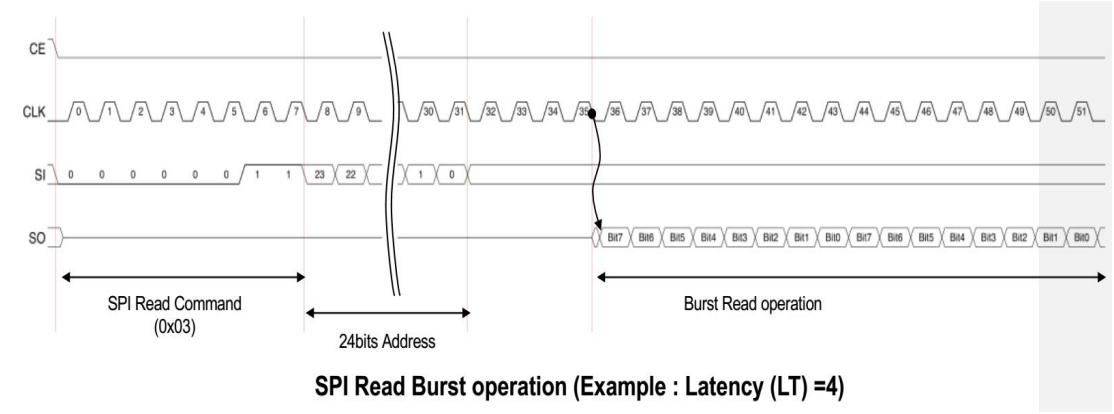


Figure 9: SPI Read Command Timing (Example: Latency(LT)=4)

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5.7 SPI QuadWrite Command Timing

The first byte(Bit7~Bit0) means IO_15~IO_8, the followed byte(Bit7~Bit0) means IO_7~IO_0 .

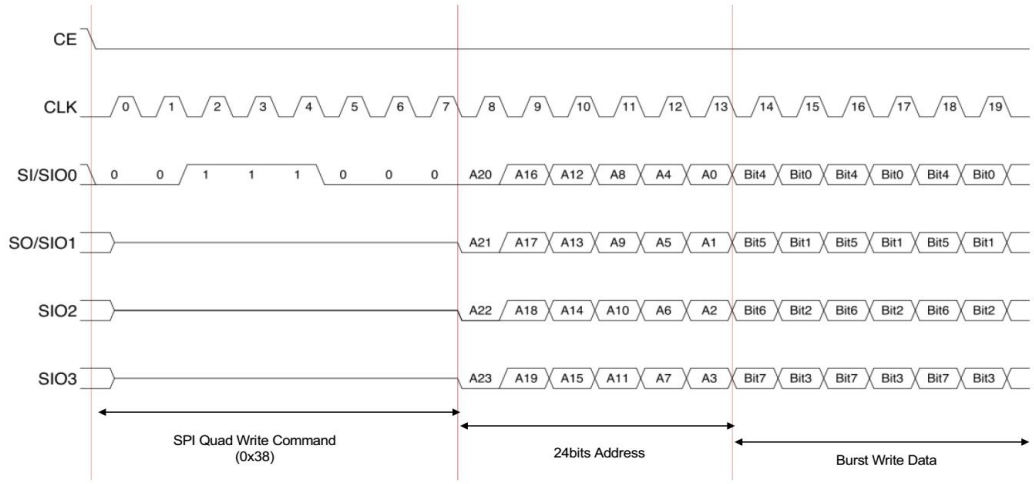


Figure 10: SPI QuadWrite Command Timing

5.8 SPI QuadRead Command Timing

The first byte(Bit7~Bit0) means IO_15~IO_8, the followed byte(Bit7~Bit0) means IO_7~IO_0 .

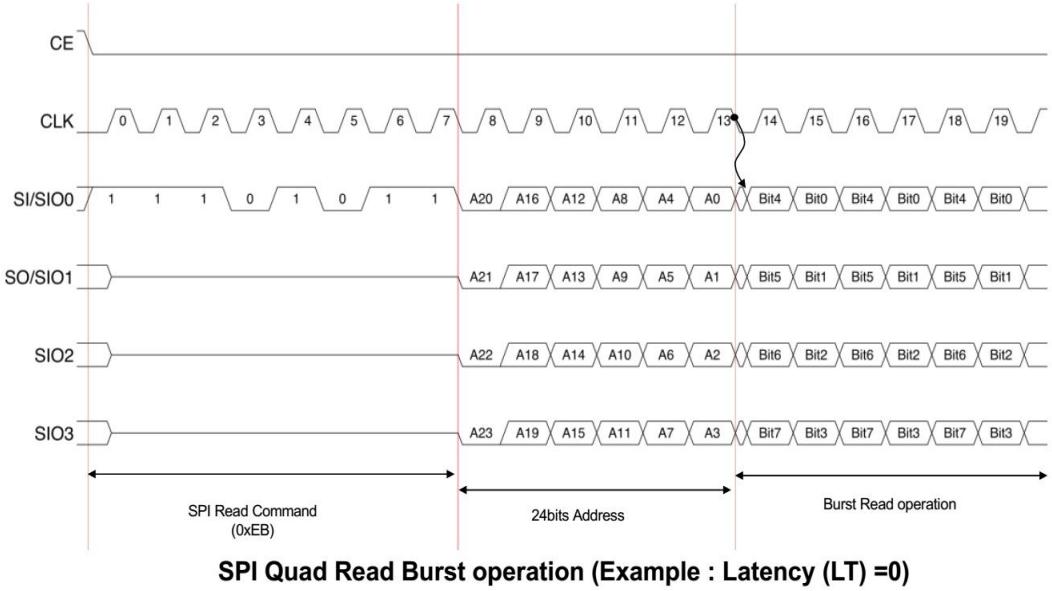


Figure 11: SPI QuadRead Command Timing (Example: Latency(LT)=0)

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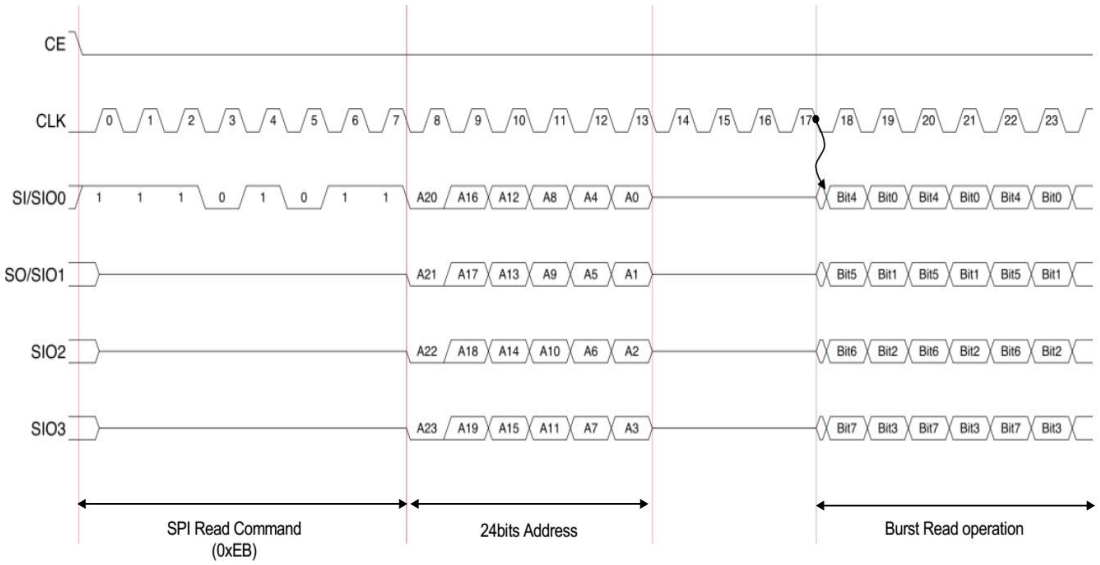


Figure 12: SPI QuadRead Command Timing (Example: Latency(LT)=4)

5.9 SPI Unique ID Operation

The two bytes are used for Manufacture ID (0x29, 0x55) and the two bytes can be read by SPI instruction.

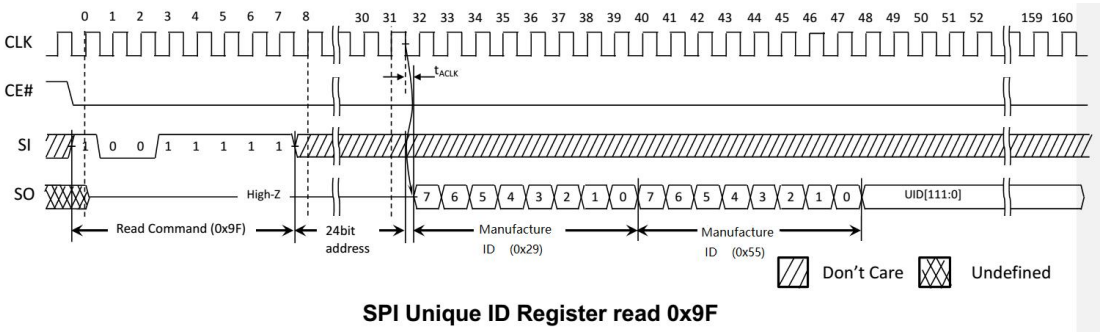


Figure 13: SPI Unique ID Read Command Timing

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6 QPI mode commands

Table 3: QPI Mode Commands

Command	QPI Mode						
	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7
Number of Clocks	2	2	2	2	2	2	2
Mode Register Write	B1H	A23-A16	A16-A8	A7-A0	Value#n		
Mode Register Read	B5H	A23-A16	A16-A8	A7-A0	Dummy(2)	Value#n	
Write	02H	A23-A16	A16-A8	A7-A0	D15-D8	D7-D0	
Read	03H	A23-A16	A16-A8	A7-A0	Dummy(0~12)	D15-D8	D7-D0
Write Enable	06H						
Write Disable	04H						
Entry To Deep PowerDown	B9H						
Exit From Deep PowerDown	ABH						
Read Unique ID Register	9FH	0H	0H	0H	16 Bytes		
Exit QPI Mode	F5H						
Reset Enable	66H						
Reset	99H						

At power up, QPI mode is disabled.

6.1 Control Command Operation

Control command include Write Enable,Write Disable,Entry To Sleep,Exit From Sleep,

Exit QPI Mode. For example Exit QPI Mode:

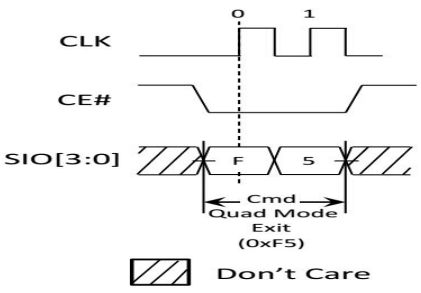


Figure 14: Exit QPI Command Timing

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6.2 Reset Operation

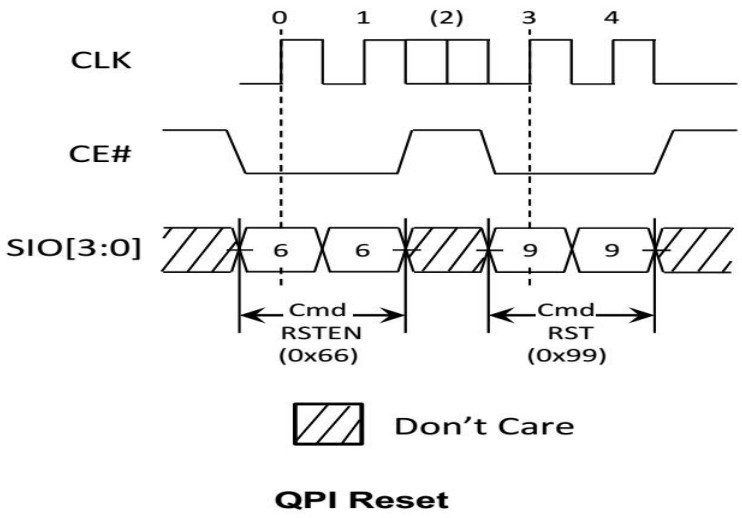


Figure 15: QPI Reset Operation Timing

6.3 Mode Register Write Command Timing

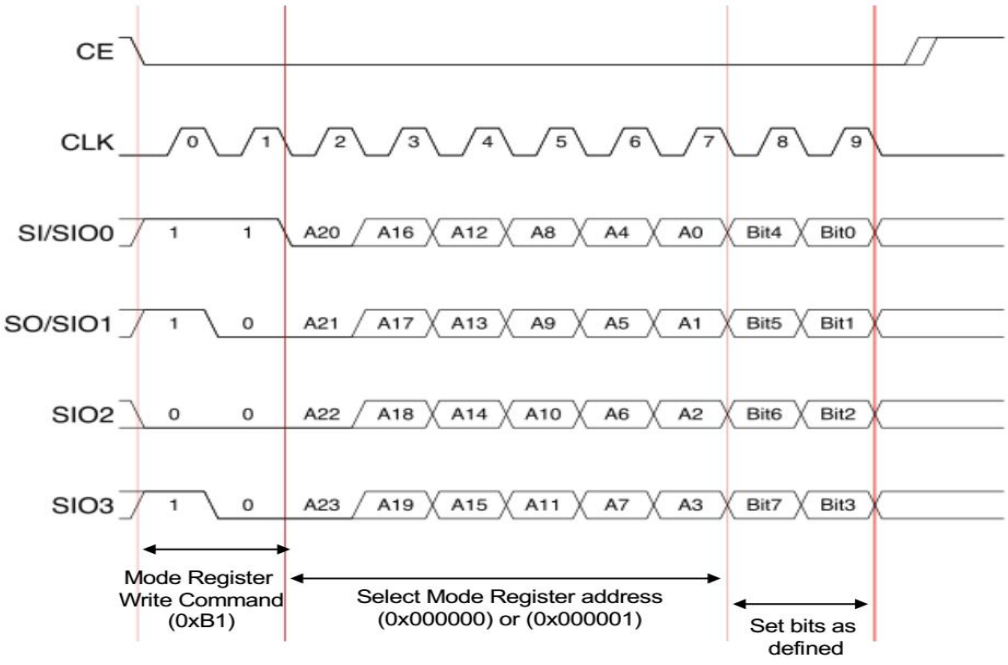


Figure 16: QPI Mode Register Write Command Timing

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6.4 Mode Register Read Command Timing

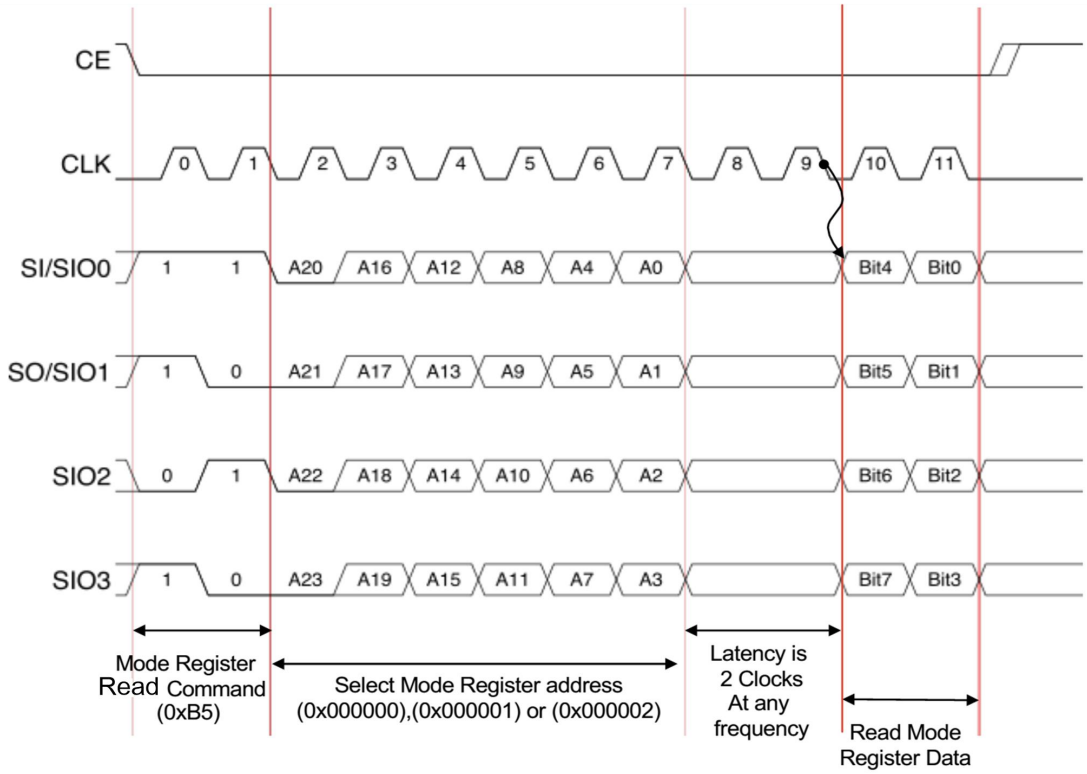


Figure 17: QPI Mode Register Read Command Timing

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6.5 QPI Write Command Timing

The first byte(Bit7~Bit0) means IO_15~IO_8, the followed byte(Bit7~Bit0) means IO_7~IO_0 .

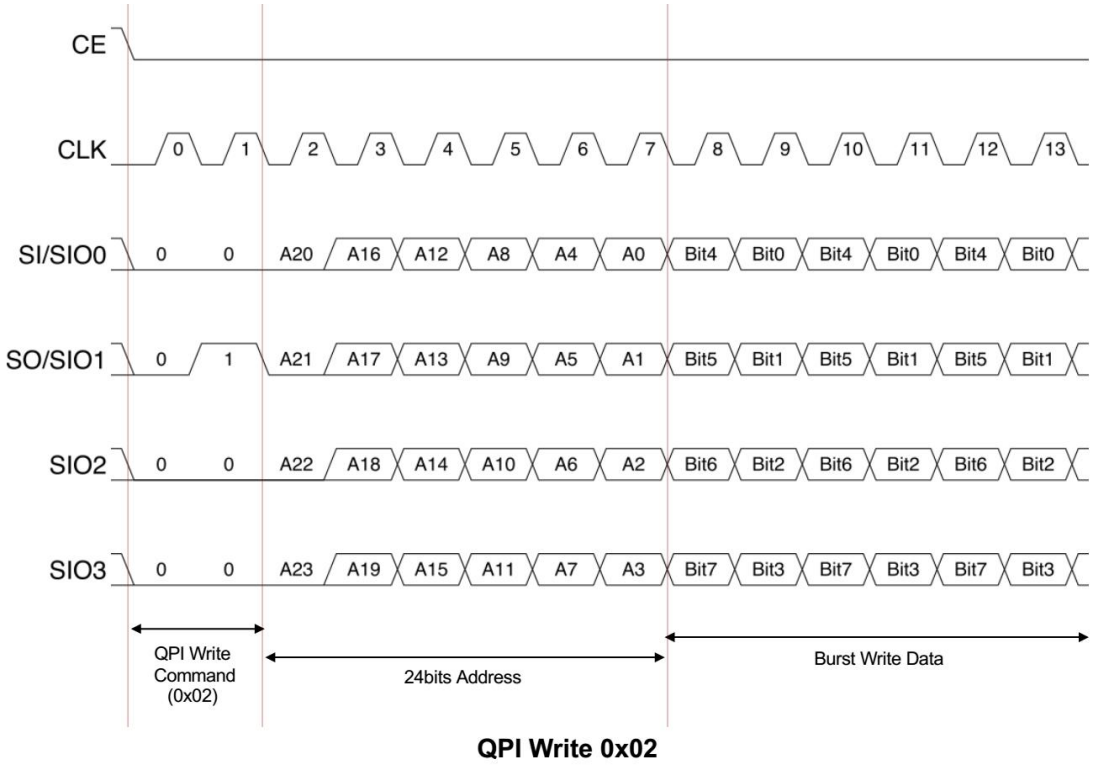


Figure 18: QPI Write Command Timing

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6.6 QPI Read Command Timing

The first byte(Bit7~Bit0) means IO_15~IO_8, the followed byte(Bit7~Bit0) means IO_7~IO_0 .

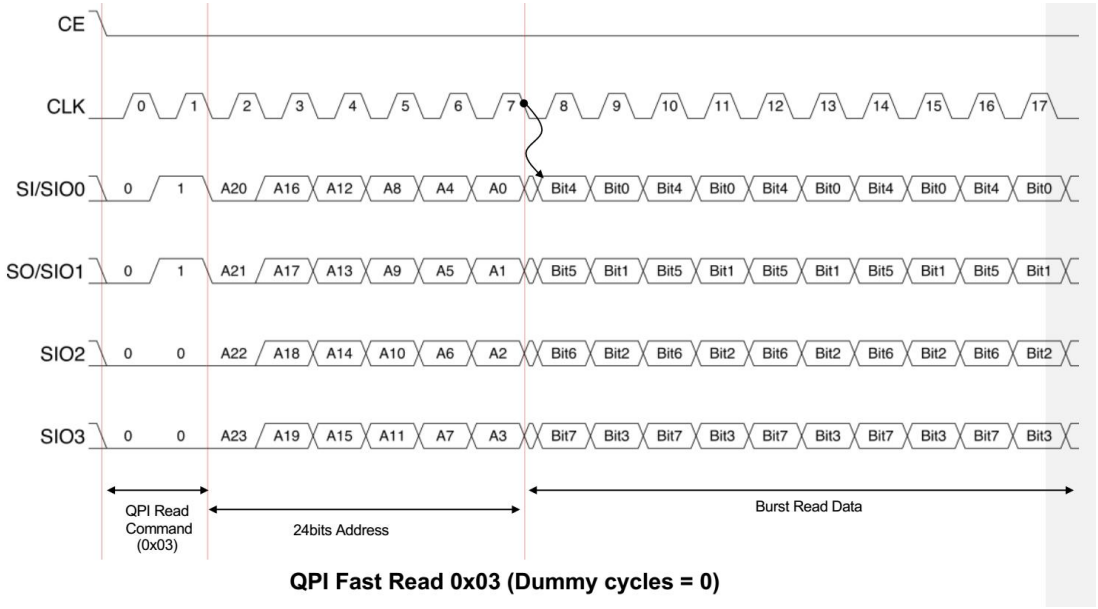


Figure 19: QPI Read Command Timing (Example: Dummy cycles=0)

6.7 QPI Unique ID Operation

The two bytes are used for Manufacture ID (0x29, 0x55) and the two bytes can be read by SPI instruction.

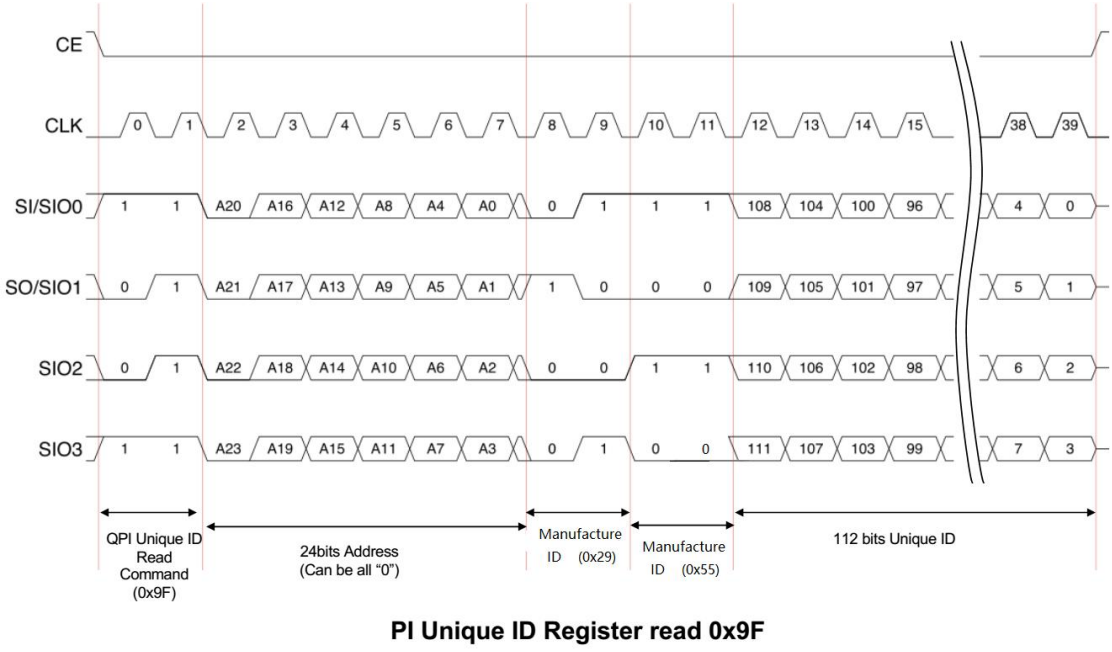


Figure 20: QPI Unique ID Read Command Timing

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7 Mode Register Definition

For PM002M chip, three Mode Registers are provided, that are, MR1, MR2,MR3. Each register is accessed by MRWR and MRRD commands combined with 3-Bytes Register Address and 1-Byte Value respectively.

Table 4: Mode Register Definition

	Address	Feature Data Bits Definition								Note
		7	6	5	4	3	2	1	0	
MR#1	0x0000	MRWD	--	--	--	BP1	BP0	WEC	--	RW
MR#2	0x0001	--	--	--	LT1	LT0	--	--	--	RW
MR#3	0x0002	--	D1	D0	REV1	REV0	--	--	--	R

7.1 Mode Register#1 (MR#1)

This register defines Write protection function. When this device will be used as partial nonvolatile memory. There are protected area and unprotected area which aredefined by BP1(Bit3) and BP0 (Bit2). The combination of MRWD(Bit7) and WEC(Bit1) defines how write protection applies to those protected area, unprotected area and Mode Register.

Table 5: Write Protection Combination

WEC	MRWD	Protected area	Unprotected area	Mode Register	Note
0	0	Writable	Writable	Writable	Default
0	1	Protected	Writable	Protected	
1	0	Protected	Writable	Writable	
1	1	Protected	Protected	Protected	

Table 6: Protected and unprotected area

BP1	BP0	Protected area	Unprotected area	Note
0	0	None	ALL	Default
0	1	Upper 1/4	Lower 3/4	
1	0	Upper 1/2	Lower 1/2	
1	1	ALL	None	

Note : Lower half is h[00FFFF]~h[000000], and Higher half is h[01FFFF]~h[010000]
Lower 1/4 means h[007FFF]~h[000000]. Lower 3/4 means h[017FFF]~h[000000]

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7.2 Mode Register#2 (MR#2)

MR#2 defines Read operation. Especially, the latency (number of dummy cycles) between the end of read address input to the first data output in Bit4 and Bit3.

The default value of other RFU bits in MR#2 are “0”.

Table 7: Read Latency definition

LT1	LT0	Number of Dummy Clock	Max Clock Frequency (SPI Mode)	Max Clock Frequency (QPI Mode)	Note
0	0	0	50Mhz	50Mhz	Default
0	1	4	50Mhz	50Mhz	
1	0	8	50Mhz	50Mhz	
1	1	12	50Mhz	50Mhz	

7.3 Mode Register#3 (MR#3)

MR#3 defines density of the products and revision of the products.

D1 and D0 bits in Bit6 and 5 in MR#3 define memory density of this device. Bit4 and 3 in MR#3 define revision of the device. The default value of other RFU bits in MR#3 are “0”.

Table 8: Density Bits

D1	D0	Density	Note
0	0	2Mbit	Default
0	1	RFU	
1	0	RFU	
1	1	RFU	

Table 9: Revision

Rev1	Rev0	Revision	Note
0	0	0	Default

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8 Power Mode

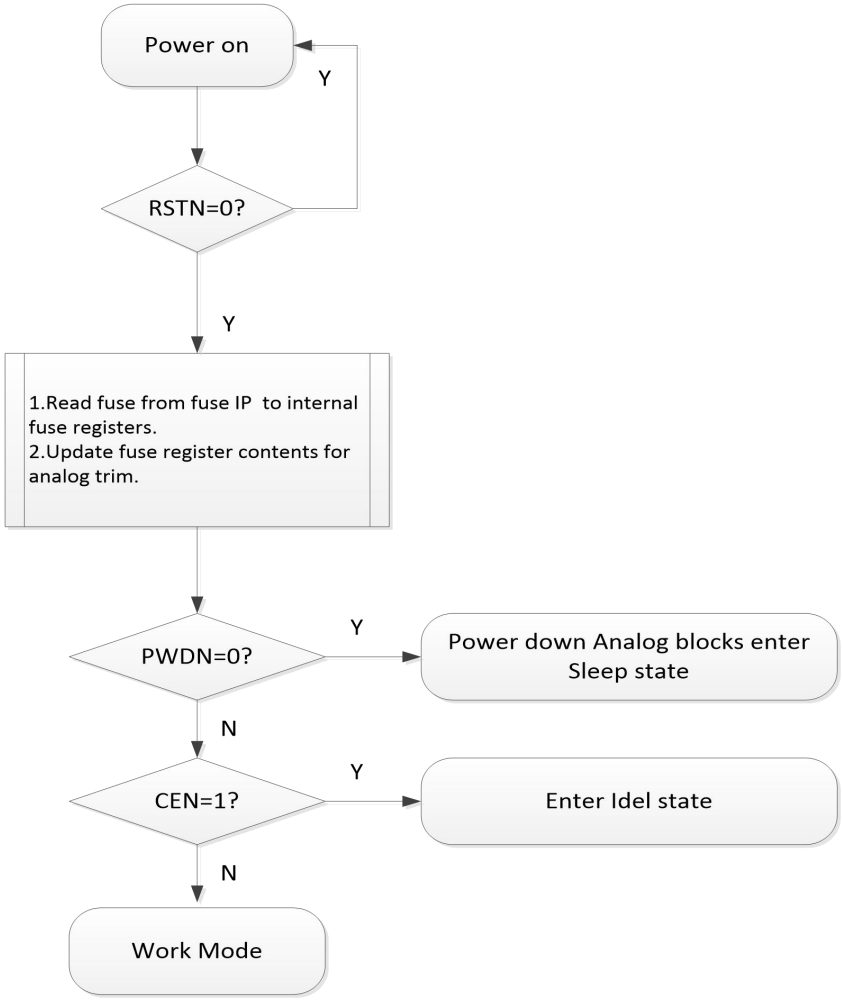
This device provides four kind of low power mode, Read, Write, Standby, Sleep.

During normal work mode, there are read and write. when CE# high, the arrays enter into the Standby mode, which internal regular are still on, but the device cannot receive the command and the data in SI/SO will be not available. When host issue EntryToSleep command, the device will enter into the Sleep mode, in this situation, the internal logic and voltage regular will be off, when host issue the ExitFromSleep command, the device will execute the wake-up sequence to the Standby mode.

This device has four states, that is power-on sequence, normal work mode, sleep mode and wake-up sequence

8.1 Power-on

When powering on, the power-on sequence begins, it is composed of three stage as below:



Analog block active

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Fuse-recall

During this stage, the device internal logic loads the fuse bits form EFUSE to trim registers..

Analog block ready

In Fuse-recall stage, the analog blocks' trim bits are updated by fuse registers, and it takes some times to stable..

8.2 Sleep

Sleep is a low power mode. During this mode, all internal regulators were closed to saving the power consumption. Host can issue command EntryTo Sleep to make device enter into this stage.

8.3 Wake-up

Wake-up make the internal analog blocks active It doesn't need do initialization like fuse-recall, only need analog modules stable stage.

9 Input/Output Timing

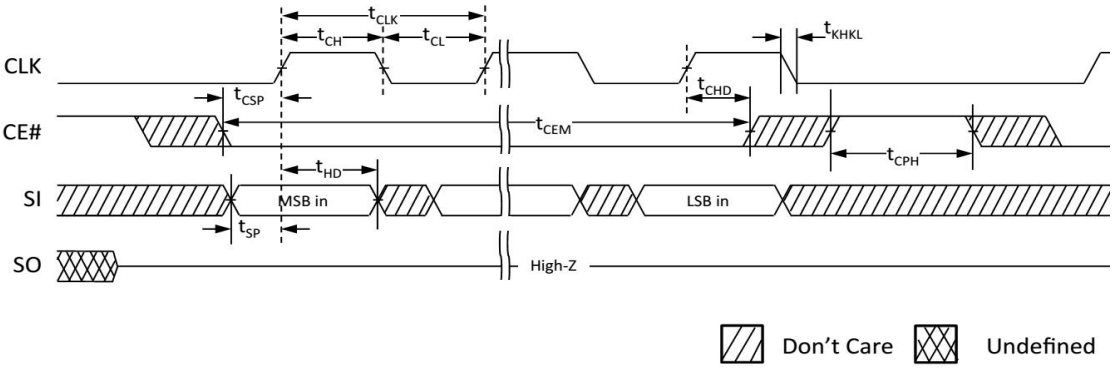


Figure 22: Input Timing

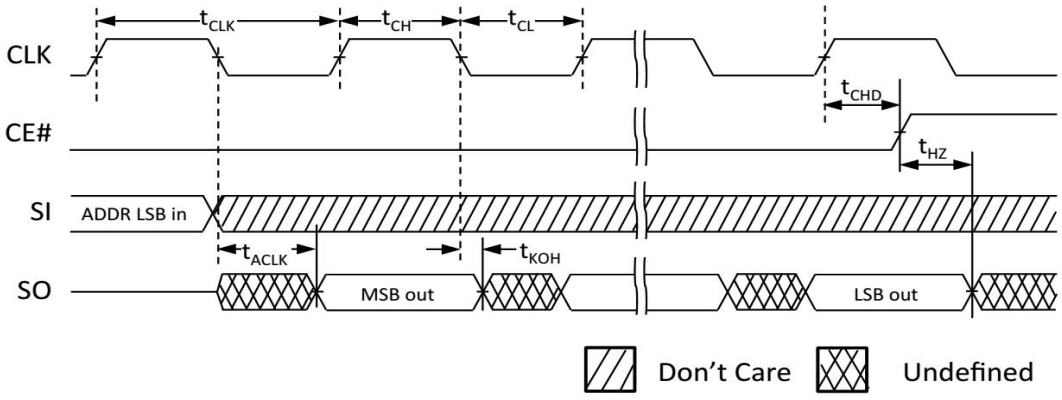


Figure 23: Output Timing

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10 Electrical Specifications

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 10: Electrical Specifications

Symbol	Parameter	Conditions	Value	Unit
Vcc	Supply Voltage		-0.5 to 4	V
Vin	Voltage on any pin		-0.5 to Vcc	V
Iout	Output current per pin		±4	mA
Tbias	Temperature under bias	Commercial Grade	-40 to 85	℃
Tstg	Storage Temperature		-55 to 125	℃
Tlead	Lead temperature during solder(3mins max)(note1)		260	℃
Hmax_write	Maximum magnetic field during write	Write	4,000	A/m
Hmax_read	Maximum magnetic field during read or standby	Read or Standby	40,000	A/m
Hmax_poweroff	Maximum magnetic field during power off	Power off	40,000	A/m

*Note1:We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed

WARNING:Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, magnetic etc.) in excess of absolute maximum ratings. Do not exceed these ratings.Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.

11 DC/AC characteristic

This section presents the DC and AC characteristics of the device. The values for the DC and AC parameters indicated in the following tables are derived from tests under the operating and measurement conditions also indicated in the relevant tables. Designers should be aware that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

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11.1 Operating Conditions

Table 11: Operating Conditions

Symbol	Parameter	Min	Max	Unit
Vcc	Voltage Supply	2.7	3.6	V
Tax	Operating Temperature(commercial)	-40	85	℃

11.2 DC Characteristics

Table 12: DC Characteristics

Symbol	Parameter	Test Conditions		Min	Typ.	Max	Uni
I_{LI}	Input leakage current					±1	μA
I_{LO}	Output Leakage current					±1	μA
I_{SLP}	Sleep Current				2	13	uA
I_{SBY}	Standby current				2	2.7	mA
I_{CC}	Active Current	SPI Write/Read	CLK = 1MHz		2.25		mA
			CLK = 10MHz		2.5		mA
			CLK = 20MHz		3	4.8	mA
			CLK = 50MHz		4.3	6.9	mA
		QPI Write/Read	CLK = 1MHz		2.5		mA
			CLK = 10MHz		4		mA
			CLK = 20MHz		5	7	mA
			CLK = 50MHz		7	9	mA
V_{IL}	Input low voltage			-0.3		0.8	V
V_{IH}	Input high voltage			2.0		Vcc+0.3	V
V_{OL}	Output low voltage	I_{OL} = 4mA				0.4	V
V_{OH}	Output high voltage	I_{OH} = -4mA		2.4			V

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11.3 Pin Capacitance

Table 13: Pin Capacitance

Symbol	Parameter	Typical	Max	Unit
Cp*	VCC/VSS power external capacitance		10	uF
C_{IN}	Control input capacitance	-	8	pF
C_{IO}	IO capacitance	-	12	pF
C_{LOAD}	Load capacitance	-	32	pF

*Note: The external capacitor Cp at the Vcc/Vss is recommended ≤10μF; If Cp > 10μF, reading datas may be unstable when Vcc return to the normal operating voltage from power down. In this case, for the datas are read reliably, suggest to operate the highest address to write ID(0x29, 0x55) data within the specified working voltage range, and then confirm this ID data before operating on the chip. If the ID data is wrong, need to send 0xB9 (sleep) and 0xAB (wake-up),so the chip will be read reliably; Otherwise, when power up and down frequently, the hardware circuit ensures that the chip starting voltage is lower than Vs (0.3V), when Vcc up from down.

11.4 AC Characteristics

Table 14: AC Characteristics

Symbol	Parameter	50Mhz		Unit
		Min	Max	
tCLK	CLK period	20		ns
tCH/tCL	Clock high/low width	1.5		ns
tKHKL	CLK rise or fall time		1.5	ns
tCPH	CE# High between subsequent burst	20		ns
tCSP	CE# Setup time to CLK rising edge	3		ns
tCHD	CE# Hold time from CLK rising edge	50		ns
tSP	Setup time to active CLK edge	2		ns
tHD	Hold time from active CLK edge	2		ns
tHZ	Chip disable to DQ output high-Z		6	ns
tACLK	CLK to output delay	8	10	ns

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tKOH	Data hold time from clock falling edge	1.5		ns
tRST	Reset recovery time after Operation command	150		us
tESLP	Sleep entry time from Sleep command		40	us
tRSLP	Recovery time from Sleep exit command	1		ms

11.5 Power Up Timing

To provide protection for data during initial power up, power loss or brownout, when ever V_{cc} falls below VCC（min）the device cannot be selected (CE# is restricted from going low) and the device is inhibited from Read or Write operations.

Power Up Delay Time

During initial power up or when recovering from brownout or power loss, a power up delay time (tPU) must be added from their specified minimum voltages (Vcc(min)) to normal operations may commence.This time is required to insure that the device internal voltages have stabilized.

tPU is measured from the time that Vcc have reached their specified minimum voltages. and the device will finish fuse-recall and analog blocks are stable to work.

Table 15: Power-Up Initial Voltages and Delay Timing

Symbol	Parameter	Min	Typ	Max	Unit
Vs	Chip Starting Voltage	-	-	0.3	V
t PU	Power Up delay time	1.5	-	-	ms
T R	Reset Power Up Time	-	4	150	us

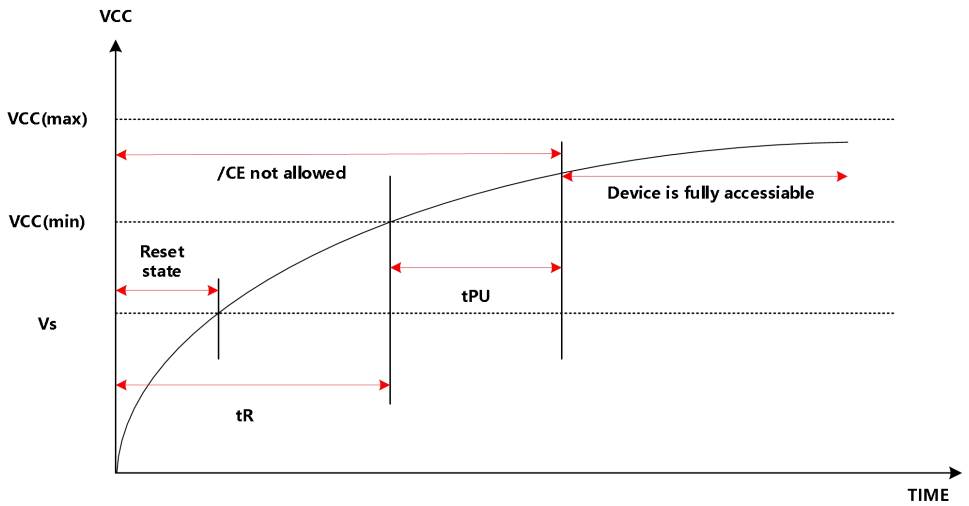


Figure 24: Power-Up Timing and Voltage Levels

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In some cases, because the voltage stays within the protection voltage range after power failure, the circuit is in the protection state, and there is no reset to reset the circuit and it enters the normal state, resulting in the phenomenon that it cannot operate normally.

In order to avoid entering the protection state and not being able to operate normally, the following suggestions are put forward:

(1) The external capacitance of VCC/VSS is recommended not to be greater than 10 μ F to ensure that the chip can be powered on and off quickly.

(2) Ensure that the minimum voltage of the power supply is lower than the starting voltage of the chip protection 0.3V when the power fails on the circuit to avoid the chip entering the protection state.

(3) Add the power-on review program to determine whether the chip starts normally by reading whether the data at a specific position is a specific value.

(4) Write data after reflow soldering is completed to avoid data loss caused by high temperature.

Power-On and Power-Off Application Scheme Recommendations

Increase the measures of fast power on and off, so that when the chip is powered off, it can quickly discharge to 0V, and when the chip is powered on, it can quickly power on to the working voltage, so that it can avoid opening the self-protection module and reduce the failure probability.

The test data show that, from 0V to 3.3V within 150us, the successful reset can be guaranteed.

● **Method 1**

The power supply can be turned off for the chip, and the power supply of the chip can be turned off in time when the voltage drops, such as the H7211 enabled LDO, which can make the VCC rise and fall quickly by controlling the enable foot.

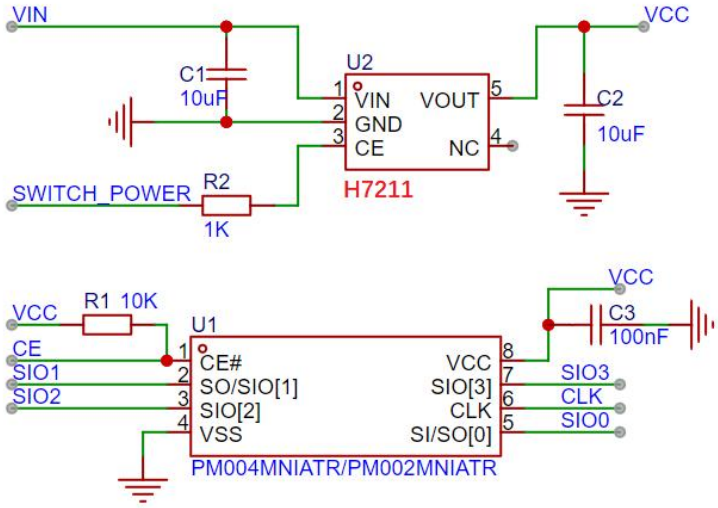


Figure 25: Schematic diagram of the LDO control

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(1) H7211 power on the chip: when the system is stable, turn off the H7211 output for a period of time to ensure that the VCC is reduced to 0V, and turn on the H7211 power output to make the chip rise from 0V to the working voltage. When powering on, the waiting time is set in the software to 2ms (= capacitor charging time +tPU, due to the difference of LDO output capacitance, the specific time is subject to the actual test), and then the normal read and write operation is carried out.

(2) H7211 power off to the chip: when the system power down, SWITCH_POWER is low, turn off H7211 power output; At the same time, it is also necessary to ensure that pins SIO0, SIO1, SIO2, SIO3, CE, CLK are also low to avoid leakage of these pins and the voltage of the VCC terminal cannot be discharged to 0V.

In the event of uncontrolled power loss, Step 1 may be performed alone, provided that all MRAM chip pins are discharged to 0 V.

- **Method 2**

The power supply at the VCC end of the P-MOS switch chip is adopted, and the reference schematic diagram is as follows (see Figure 26). SWITCH_POWER is the enable pin that controls the output of P-MOS. The actual output (VCC) voltage of P-MOS must be within the normal operating voltage range of the chip (2.7V~3.6V). The pressure difference from the input (VIN) to the output (VCC) is about 0.1V to 0.2V.

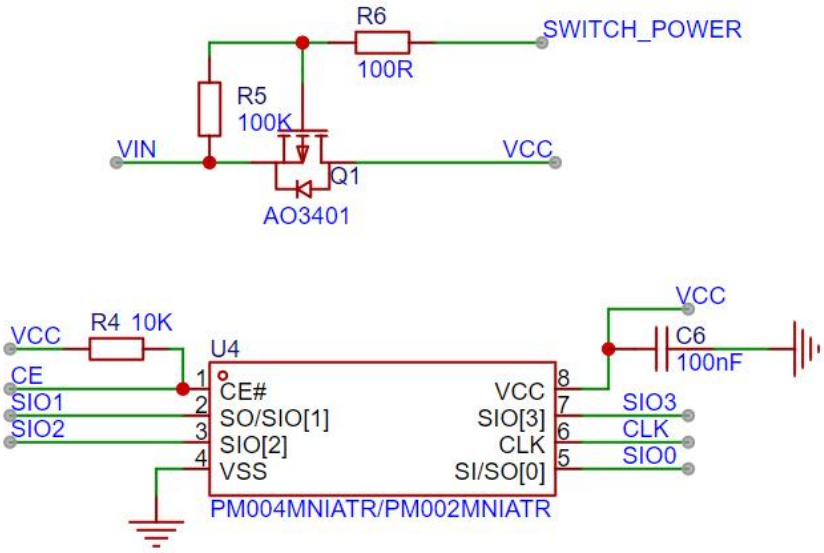


Figure 26 Schematic diagram of P-MOS control

(1) P-MOS power on the chip: when the system is powered on and stabilized, make SWITCH_POWER low, open the P-MOS power output, and make the chip rise from 0V to the working voltage. When powering on, the waiting time is set in the software to be about 2ms (= capacitor charging time +tPU, due to the difference of P-MOS output capacitance, the specific time is subject to the actual test), and then the normal read and write operation is carried out.

(2) Powering Off the Chip via P-MOS: During system power loss, set SWITCH_POWER to a high

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level to disable the P-MOS power output. Simultaneously, ensure that all pins SIO0, SIO1, SIO2, SIO3, CE, and CLK are held at a low level to prevent leakage current from preventing the VCC voltage from discharging to 0 V. In software, configure a delay of approximately 2 ms (equal to the capacitor discharge time; due to variations in the output capacitance of the P-MOS, the exact duration should be determined by actual testing) to ensure the VCC voltage of the chip is fully discharged to 0 V.

Recommended Work Flow:

1. After system power-on, the MCU shall control either an LDO or MOSFET to rapidly power up the MRAM. If the pre-power state of the MRAM voltage is uncertain, first de-energize the MRAM via the LDO or MOSFET for a brief duration , then reapply power.

2. Read the ID.

If the ID 0x29, 0x55 is successfully retrieved， insert a 1 ms delay, and then transmit instruction 0xB9.

Insert a 1 ms delay, and then transmit instruction 0xAB. Insert a 1 ms delay, and then proceed to subsequent operations.

3. Detect whether the content at a specific location of the MRAM meets the requirements.

If the content of the address 0x0000 is read whether it is 0x1234, if not, it is written to 0x1234 and read again, if it is read to 0x1234, it can be operated normally.

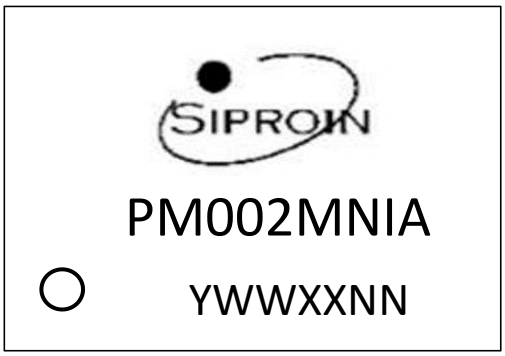
If read directly or after writing is still not 0x1234, start failed, so reenter step 1.

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12 Order Information

Orderable Device	Density	Typical voltage	Interface	Package Type	Op Temp(℃)	Package Qty
PM002MNIATU	2Mbit	3.3V	SPI/QPI	SOP8_150mil	-40 to 85	100/Tube
PM002MNIATR	2Mbit	3.3V	SPI/QPI	SOP8_150mil	-40 to 85	2500/Reel
PM002MNIATR	2Mbit	3.3V	SPI/QPI	SOP8_150mil	-40 to 85	4000/Reel

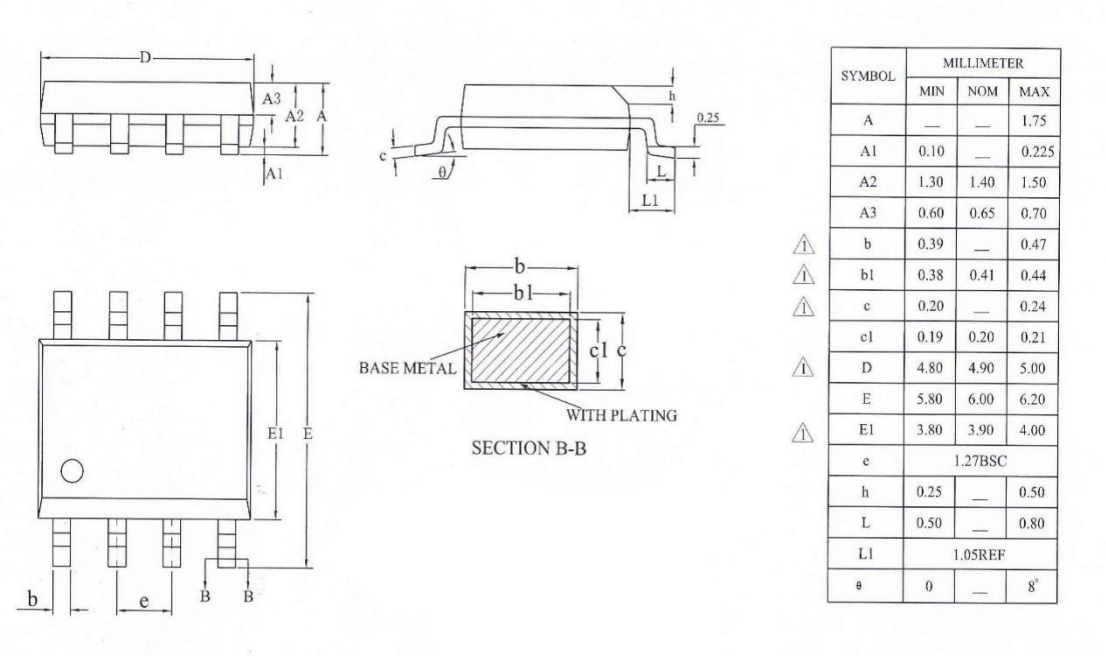
Top Side Marking



Type: PM002MNI Version： A
Y: Year WW:Week

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13 Package Outline Drawing



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 25: Package Outline for SOP8 150MIL

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Document Revision History

Version	Date	Author	Brief Description of Changes
V1.0	2022-05-05	Ding	Define Max Frequency，modify Feature/DC/AC, parameter, cancel ddr read/write timing
V1.1	2022-05-24	Ding	modify Electrical Specifications, modify Note on Use, modify Package description
V1.2	2022-08-22	Justin	modify Vin description in Table10, Delete Vccq description in Table11, modify Table15 and Figure24
V1.3	2022-11-01	Justin	Modify ID(0x29, 0x55) description in Chapter 5.9 and Chapter 5.9,Modify Hmax_read description in Table10, define tRST in Table14,modify Chapter 11.3, modifyChapter 11.5
V1.31	2023-07-19	Zhao	Delete tERSLP description in Table14 ,Modify the Operation Timing in Figure 13 and Figure 20.
V1.32	2025-07-16	Yang	Add the Reset Power Up Time parameter in 11.5 Power Up Timing.
V1.33	2025-07-24	Yang	Update and modify Order Information.
V1.34	2026-1-5	Yang	Add the Power-On and Power-Off Application Scheme Recommendations in 11.5 Power Up Timing.

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