P25T22H/12H

Ultra Low Power, 2M/1M-bit

Serial Standard and Dual I/O Flash Memory Datasheet

May. 18, 2021

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Performance Highlight

- *Wide Supply Range from 2.3 to 3.6V for Read, Erase and Program*
- *Ultra Low Power consumption for Read, Erase and Program*
- *X1, X2 Multi I/O Support*
- *High reliability with 100K cycling and 20 Year-retention*



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1 Overview

General

- **Single 2.3V to 3.60V supply**
- **Industrial Temperature Range -40C to 85C**
- **Serial Peripheral Interface (SPI) Compatible: Mode 0 and Mode 3**
- **Single, Dual IO mode**
  - 2M/1M x 1 bit
  - 1M/512K x 2 bits
- **Flexible Architecture for Code and Data Storage**
  - Uniform 256-byte Page Program
  - Uniform 256-byte Page Erase
  - Uniform 4K-byte Sector Erase
  - Uniform 32K/64K-byte Block Erase
  - Full Chip Erase
- **Hardware Controlled Locking of Protected Sectors by WP Pin**
- **128 bit unique ID for each device**
- **Fast Program and Erase Speed**
  - 2ms Page program time
  - 8ms Page erase time
  - 8ms 4K-byte sector erase time
  - 8ms 32K-byte block erase time
  - 8ms 64K-byte block erase time
- **JEDEC Standard Manufacturer and Device ID Read Methodology**
- **Ultra Low Power Consumption**
  - 0.2uA Typical Deep Power Down current @3.0V
  - 9uA Typical Standby current @3.0V
  - 0.8mA Active Read current at 33MHz
  - 2.0mA Active Program or Erase current
- **High Reliability**
  - 100,000 Program / Erase Cycles
  - 20-year Data Retention
- **Industry Standard Green Package Options**
  - 8-pin SOP (150mil/208mil)/TSSOP
  - 8-land USON (3x2x0.55mm)
  - KGD for SiP

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2 Description

The P25T22H/12H is a serial interface Flash memory device designed for use in a wide variety of high-volume consumer based applications in which program code is shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the device, with its page erase granularity it is ideal for data storage as well, eliminating the need for additional data storage devices.

The erase block sizes of the device have been optimized to meet the needs of today's code and data storage applications. By optimizing the size of the erase blocks, the memory space can be used much more efficiently. Because certain code modules and data storage segments must reside by themselves in their own erase regions, the wasted and unused memory space that occurs with large sectored and large block erase Flash memory devices can be greatly reduced. This increased memory space efficiency allows additional code routines and data storage segments to be added while still maintaining the same overall device density.

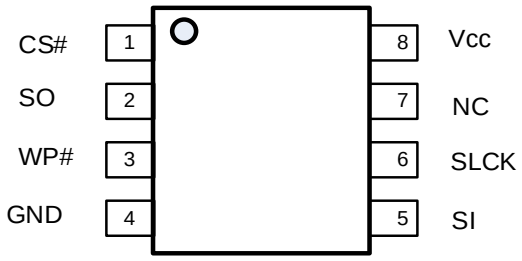
Specifically designed for use in many different systems, the device supports read, program, and erase operations with a wide supply voltage range of 2.3V to 3.6V. No separate voltage is required for programming and erasing.

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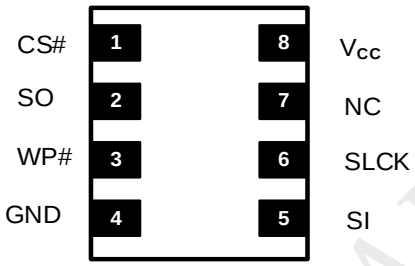
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3 Pin Definition

3.1 Pin Configurations



8-PIN SOP (150mil/208mil) and TSSOP



8-Land USON (2x3mm)

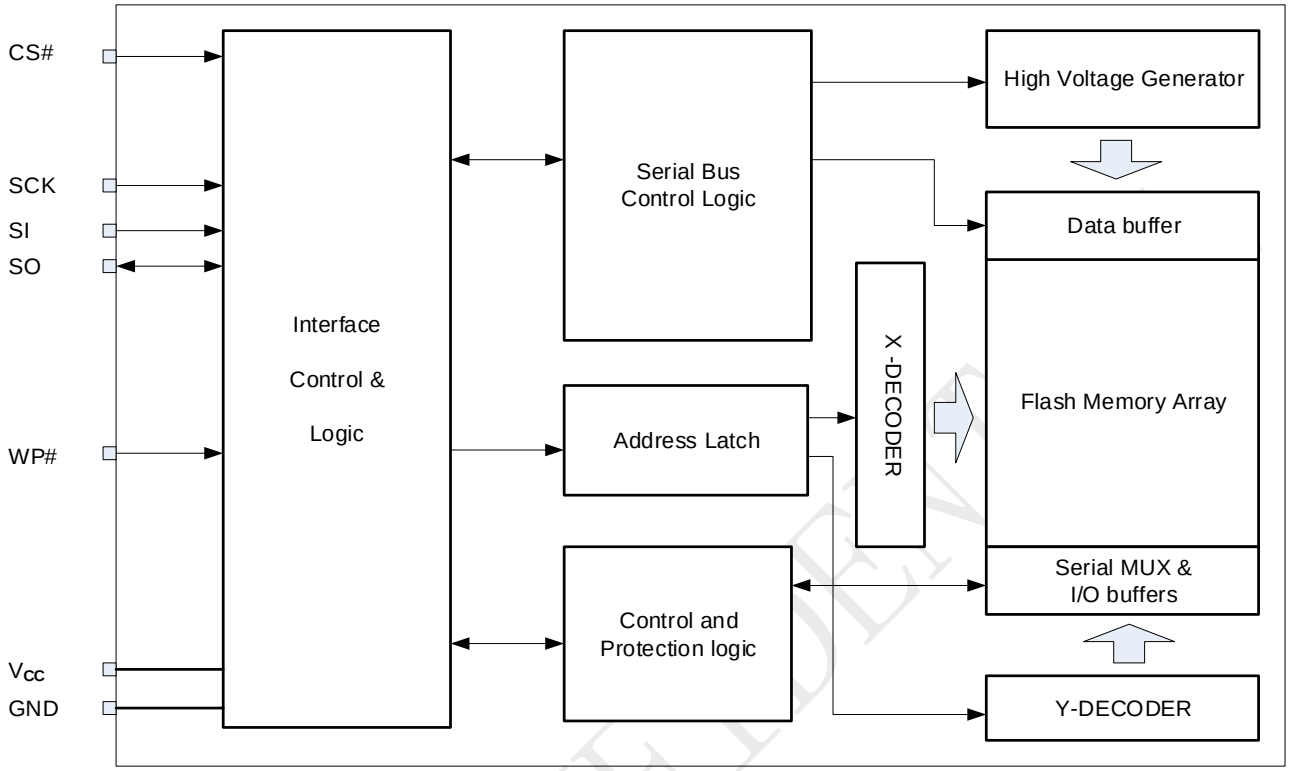
3.2 Pin Descriptions

No.	Symbol	Extension	Remarks
1	CS#		Chip select
2	SO	SIO1	Serial data output for 1 x I/O Serial data input and output for 2 x I/O read mode
3	WP#	-	Write protection active low
4	GND	-	Ground of the device
5	SI	SIO0	Serial data input for 1x I/O Serial data input and output for 2 x I/O read mode
6	SCLK	-	Serial interface clock input
7	NC	-	Not connected
8	Vcc	-	Power supply of the device

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4 Block Diagram



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5 Electrical Specifications

5.1 Absolute Maximum Ratings

- Storage Temperature .....-65°C to +150°C
- Operation Temperature .....-40°C to +85°C
- Maximum Operation Voltage..... 4.0V
- Voltage on Any Pin with respect to Ground.....-0.6V to + 4.1V
- DC Output Current .....5.0 mA

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Pin Capacitance[1]

Symbol	Parameter	Max.	Units	Test Condition
C_{OUT}	Output Capacitance	8	pF	V_{OUT}=GND
C_{IN}	Input Capacitance	6	pF	V_{IN}=GND

Note:

1. Test Conditions: T_A= 25°C, F = 1MHz, Vcc = 3.0V.

Figure 5-1Maximum Overshoot Waveform



Figure 5-2 Input Test Waveforms and Measurement Level

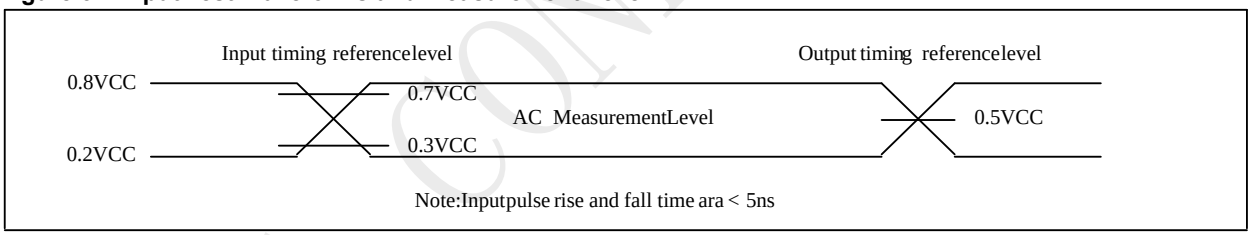
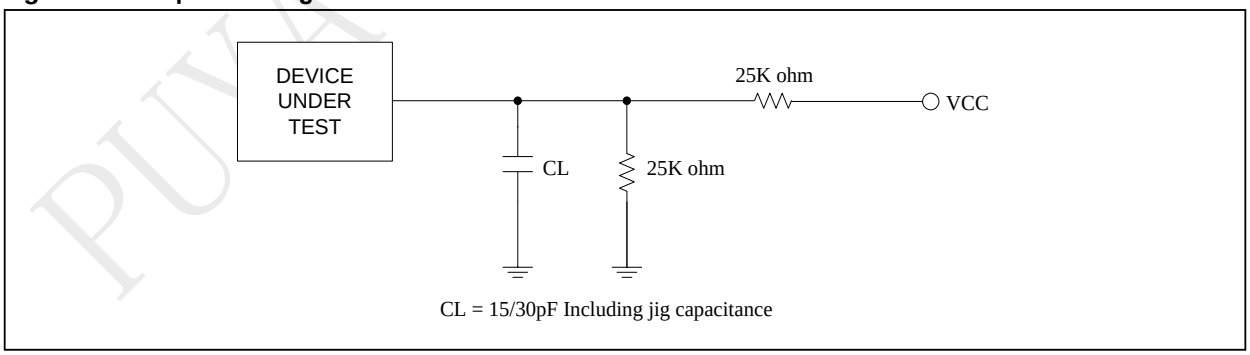


Figure 5-3 Output Loading



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5.2 DC Characteristics

Table 5-2 DC parameters(Ta=-40°C to +85°C)

Sym.	Parameter	Conditions	2.3V to 3.6V			Units
			Min.	Typ.	Max.	
I_{DPD}	Deep power down current	CS#=Vcc, all other inputs at 0V or Vcc		0.2	2	uA
I_{SB}	Standby current	CS#, WP#=VIH all inputs at CMOS levels		12	20	uA
I_{CC1}	Low power read current (03h)	f=1MHz; IOUT=0mA		0.5	1.0	mA
		f=33MHz; IOUT=0mA		0.8	1.5	mA
I_{CC2}	Read current (0Bh)	f=50MHz; IOUT=0mA		1.0	2.0	mA
		f=85MHz; IOUT=0mA		1.5	2.5	mA
I_{CC3}	Program current	CS#=Vcc		2.0	3.0	mA
I_{CC4}	Erase current	CS#=Vcc		2.0	3.0	mA
I_{LI}	Input load current	All inputs at CMOS level			1.0	uA
I_{LO}	Output leakage	All inputs at CMOS level			1.0	uA
V_{IL}	Input low voltage				0.3Vcc	V
V_{IH}	Input high voltage		0.7Vcc			V
V_{OL}	Output low voltage	IOL=100uA			0.2	V
V_{OH}	Output high voltage	IOH=-100uA	Vcc-0.2			V

Note:

1. Typical values measured at 3.0V @ 25°C for 2.3V to 3.6V.

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5.3 AC Characteristics

Table 5-3 AC parameters(Ta=-40°C to +85°C)

Symbol	Alt.	Parameter	2.3V~3.6V			
			min	typ	max	Unit
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE32K, BE, CE, DP, RES, WREN, WRDI, RDID, RDSR, RDCR, WRSR, WRCR, RUID			104	MHz
fRSCLK	fR	Clock Frequency for READ instruction			40	MHz
fTSCLK	fT	Clock Frequency for DREAD instructions and 2READ instructions with 8 dummy CLK			104	MHz
	fQ	Clock Frequency for 2READ instructions with 4 dummy CLK			104	MHz
tCH(1)	tCLH	Clock High Time for READ instruction	9.0			ns
		Clock High Time	4.5			ns
tCL(1)	tCLL	Clock Low Time for READ instruction	9.0			ns
		Clock Low Time (fSCLK) 45% x (1fSCLK)	4.5			ns
tCLCH(4)		Clock Rise Time (peak to peak)	0.1			v/ns
tCHCL(4)		Clock Fall Time (peak to peak)	0.1			v/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)	5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)	5			ns
tDVCH	tDSU	Data In Setup Time	2			ns
tCHDX	tDH	Data In Hold Time	3			ns
tCHSH		CS# Active Hold Time (relative to SCLK)	5			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)	5			ns
tSHSL	tCSH	CS# Deselect Time From Read to next Read	20			ns
		CS# Deselect Time From Write, Erase, Program to Read Status Register	30			ns
tSHQZ(7)	tDIS	Output Disable Time			6	ns
tCLQV	tV	Clock Low to Output Valid Loading 30pF			7	ns
		Clock Low to Output Valid Loading 15pF			6	ns
tCLQX	tHO	Output Hold Time	0			ns
tWHSL(3)		Write Protect Setup Time	20			ns
tSHWL(3)		Write Protect Hold Time	100			ns
tDP		CS# High to Deep Power-down Mode			3	us
tRES1		CS# High To Standby Mode Without Electronic Signature Read			8	us
tRES2		CS# High To Standby Mode With Electronic Signature Read			8	us
tW		Write Status Register Cycle Time		8	12	ms
tReady		Reset recovery time (for erase/program operation except WRSR)	30			us
		Reset recovery time (for WRSR operation)		8	12	ms

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5.4 AC Characteristics for Program and Erase

Table 5-4 AC parameters for program and erase(Ta=-40°C to +85°C)

Sym.	Parameter	2.3V to 3.6V			Units
		Min.	Typ.	Max.	
t_{PP}	Page program time (up to 256 bytes)		2	3	ms
t_{PE}	Page erase time		8	20	ms
t_{SE}	Sector erase time		8	20	ms
t_{BE1}	Block erase time for 32K bytes		8	20	ms
t_{BE2}	Block erase time for 64K bytes		8	20	ms
t_{CE}	Chip erase time		8	20	ms

Note:

1. tCH + tCL must be greater than or equal to 1/ Frequency.
2. Typical values given for TA=25°C. Not 100% tested.
3. Only applicable as a constraint for a WRSR instruction.
4. The value guaranteed by characterization, not 100% tested in production.

Figure 5-4 Serial Input Timing

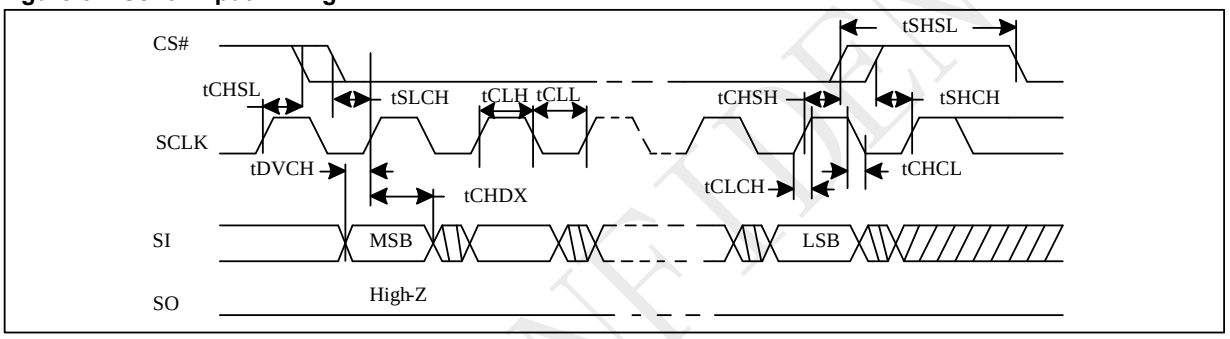


Figure 5-5 Output Timing

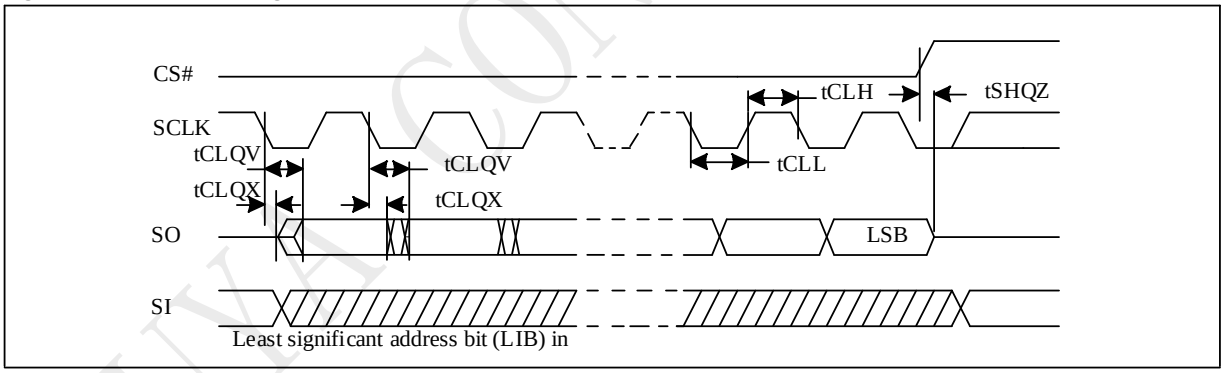
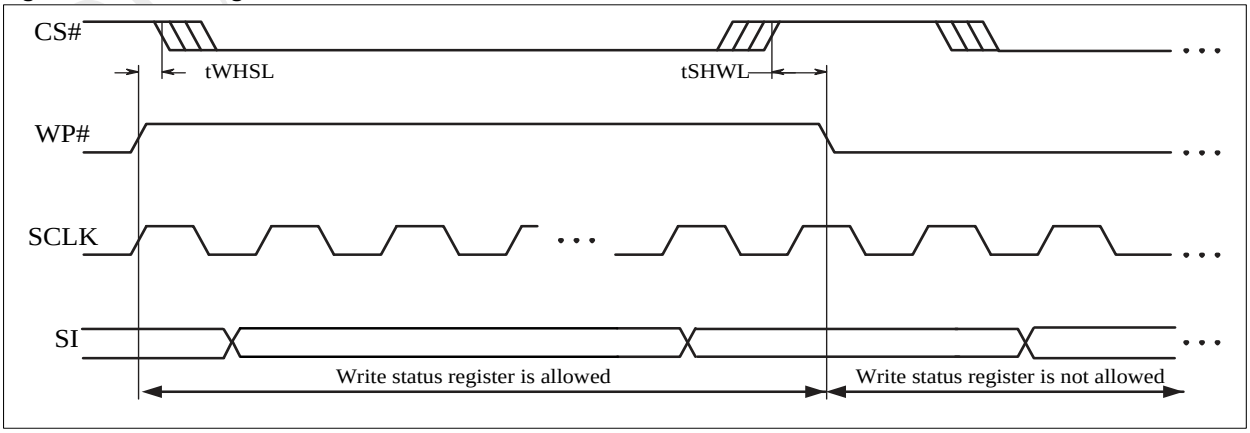


Figure 5-7 WP Timing



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5.5 Operation Conditions

At Device Power-Up and Power-Down

AC timing illustrated in "Figure AC Timing at Device Power-Up" and "Figure Power-Down Sequence" are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 5-8 AC Timing at Device Power-Up

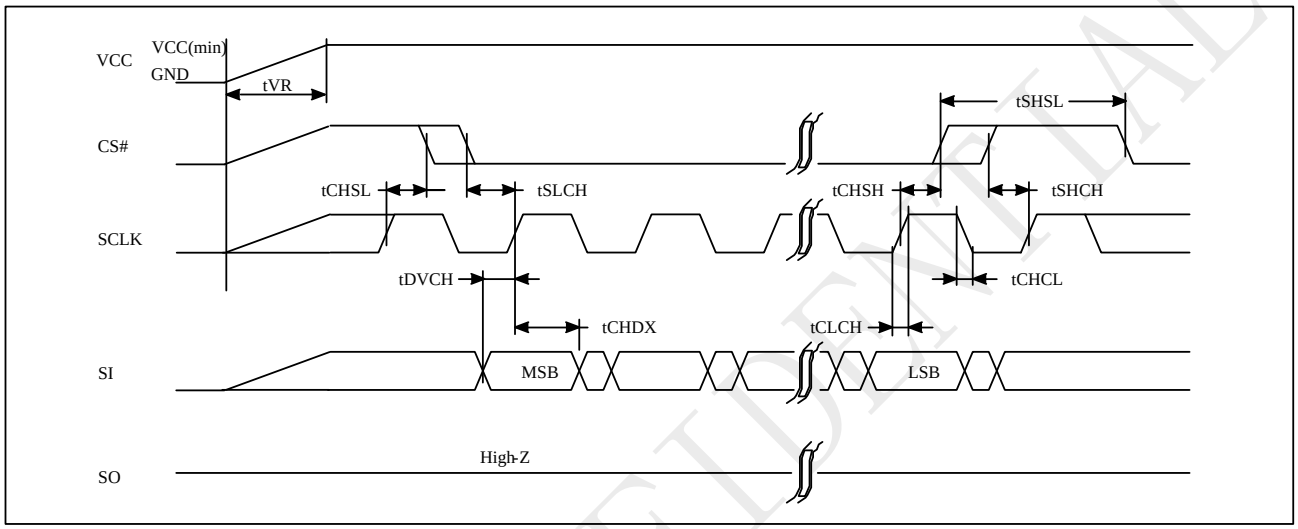
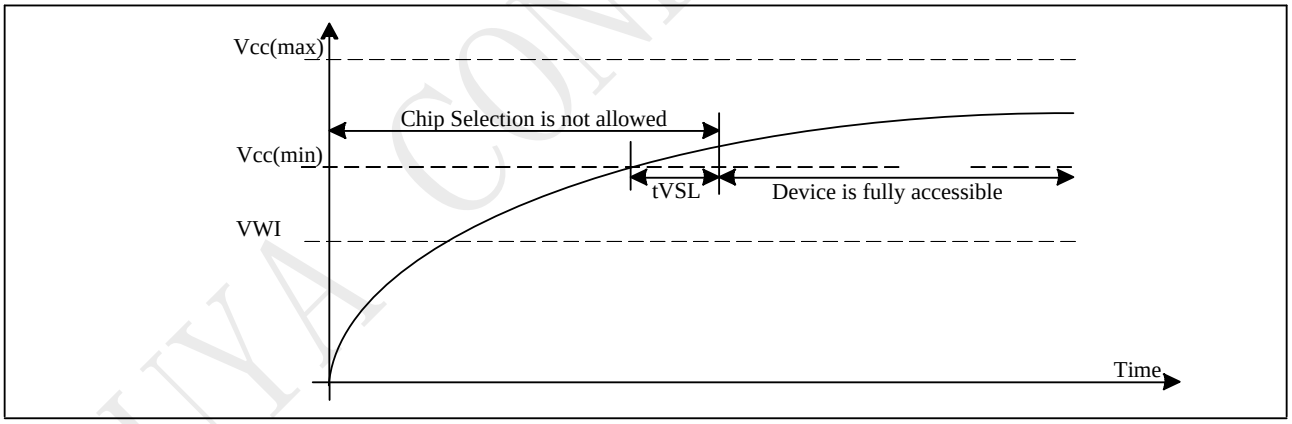


Figure 5-9 Power-up Timing



Power Up/Down and Voltage Drop

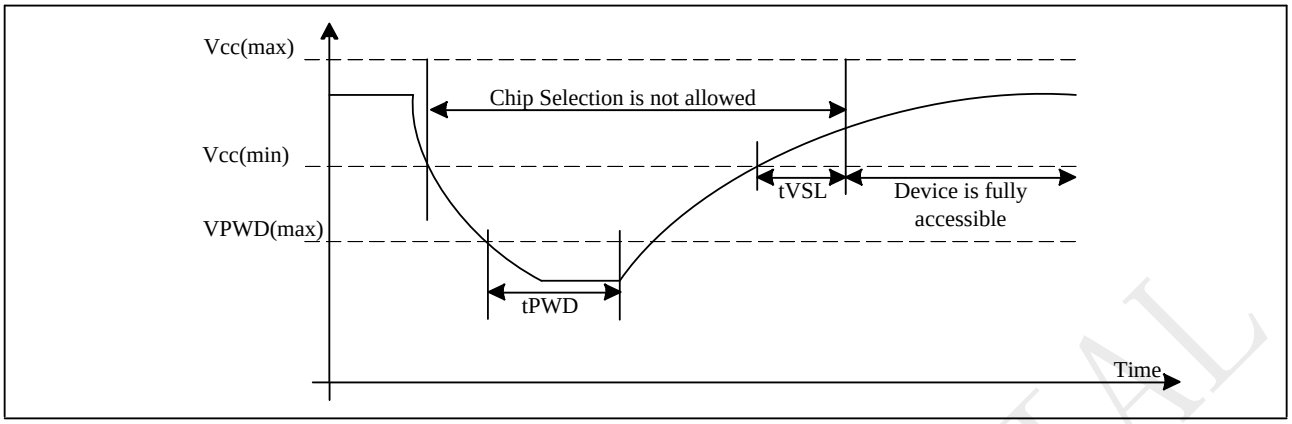
For Power-down to Power-up operation, the VCC of flash device must below VPWD for at least tPWD timing.

Please check the table below for more detail.

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Figure 5-10Power down-up Timing



Symbol	Parameter	min	max	unit
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		1	V
tPWD	The minimum duration for ensuring initialization will occur	300		us
tVSL	VCC(min.) to device operation	150		us
tVR	VCC Rise Time	1	500000	us/V
VWI	Write Inhibit Voltage	1.45	1.55	V

Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

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6 Data Protection

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

• Power-on reset: to avoid sudden power switch by system power supply transition, the power-on reset may protect the Flash.
• Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
• Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before issuing other commands to change data.
• Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits define the section of the memory array that can be read but not change.
• Hardware Protection Mode: WP# going low to protected the BP0~BP4bits and SRP bits
• Deep Power-Down Mode: By entering deep power down mode, the flash device is under protected from writing all commands except the Release form Deep Power-Down Mode command.

Table 6-1. Protected Area Sizes
P25T22H Protected Area Sizes

Status bit					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
0	x	x	0	0	NONE	NONE	NONE	NONE
0	0	x	0	1	3	030000H-03FFFFH	64KB	Upper 1/4
0	0	x	1	0	2 and 3	020000H-03FFFFH	128KB	Upper 1/2
0	1	x	0	1	0	000000H-00FFFFH	64KB	Lower 1/4
0	1	x	1	0	0 and 1	000000H-01FFFFH	128KB	Lower 1/2
0	x	x	1	1	0 to 3	000000H-03FFFFH	256KB	ALL
1	x	0	0	0	NONE	NONE	NONE	NONE
1	0	0	0	1	3	03F000H-03FFFFH	4KB	Upper 1/64
1	0	0	1	0	3	03E000H-03FFFFH	8KB	Upper 1/32
1	0	0	1	1	3	03C000H-03FFFFH	16KB	Upper 1/16
1	0	1	0	x	3	038000H-03FFFFH	32KB	Upper 1/8
1	0	1	1	0	3	038000H-03FFFFH	32KB	Upper 1/8
1	1	0	0	1	0	000000H-000FFFH	4KB	Lower 1/64
1	1	0	1	0	0	000000H-001FFFH	8KB	Lower 1/32
1	1	0	1	1	0	000000H-003FFFH	16KB	Lower 1/16
1	1	1	0	x	0	000000H-007FFFH	32KB	Lower 1/8
1	1	1	1	0	0	000000H-007FFFH	32KB	Lower 1/8
1	x	1	1	1	0 to 3	000000H-03FFFFH	256KB	ALL

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P25T12H Protected Area Sizes

Status bit					Memory Content			
BP4	**BP3**	**BP2**	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
0	x	x	0	0	NONE	NONE	NONE	NONE
0	0	x	0	1	1	010000H-01FFFFH	64KB	Upper 1/2
0	1	x	0	1	0	000000H-00FFFFH	64KB	Lower 1/2
0	x	x	1	x	0 to 1	000000H-01FFFFH	128KB	ALL
1	x	0	0	0	NONE	NONE	NONE	NONE
1	0	0	0	1	1	01F000H-01FFFFH	4KB	Upper 1/32
1	0	0	1	0	1	01E000H-01FFFFH	8KB	Upper 1/16
1	0	0	1	1	1	01C000H-01FFFFH	16KB	Upper 1/8
1	0	1	0	x	1	018000H-01FFFFH	32KB	Upper 1/4
1	0	1	1	0	1	018000H-01FFFFH	32KB	Upper 1/4
1	1	0	0	1	0	000000H-000FFFH	4KB	Lower 1/32
1	1	0	1	0	0	000000H-001FFFH	8KB	Lower 1/16
1	1	0	1	1	0	000000H-003FFFH	16KB	Lower 1/8
1	1	1	0	x	0	000000H-007FFFH	32KB	Lower 1/4
1	1	1	1	0	0	000000H-007FFFH	32KB	Lower 1/4
1	x	1	1	1	0 to 1	000000H-01FFFFH	128KB	ALL

Note:

1. X=don’t care

2. If any erase or program command specifies a memory that contains protected data portion, this command will be ignored.

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7 Memory Address Mapping

The memory array can be erased in three levels of granularity including a full chip erase. The size of the erase blocks is optimized for both code and data storage applications, allowing both code and data segments to reside in their own erase regions.

P25T22H Memory Organization

Block64K	Block32K	Sector	Address Range	
3	7-6	63	03F000H	03FFFFH
		……	……	……
		48	030000H	030FFFH
2	5-4	47	02F000H	02FFFFH
		……	……	……
		32	020000H	020FFFH
1	3-2	31	01F000H	01FFFFH
		……	……	……
		16	010000H	010FFFH
0	1-0	15	00F000H	00FFFFH
		……	……	……
		0	000000H	000FFFH

P25T12H Memory Organization

Block64K	Block32K	Sector	Address Range	
1	3-2	31	01F000H	01FFFFH
		……	……	……
		16	010000H	010FFFH
0	1-0	15	00F000H	00FFFFH
		……	……	……
		0	000000H	000FFFH

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8 Device Operation

Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

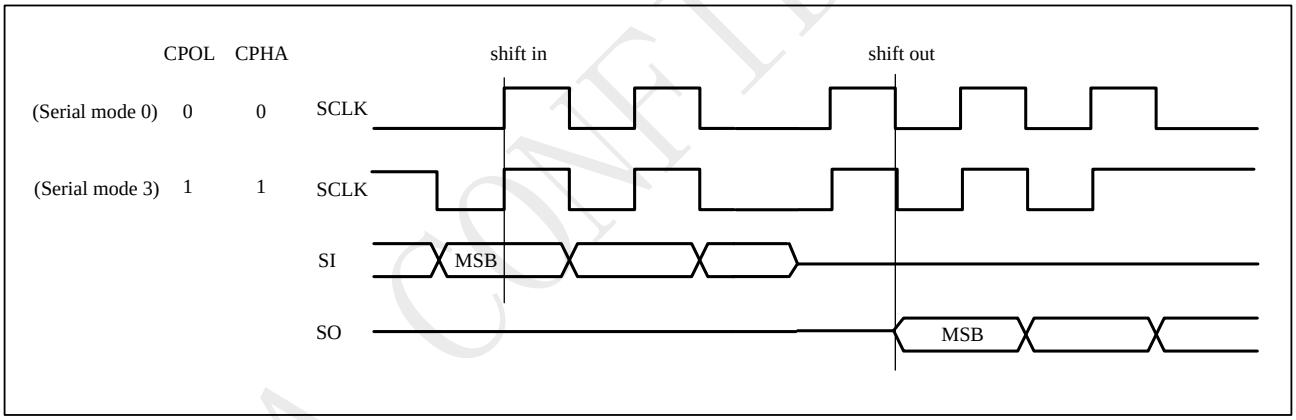
When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this LSI should be High-Z. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.

Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of serial peripheral interface mode 0 and mode 3 is shown as Figure 8-1.

For the following instructions: RDID, RDSR, READ, FAST_READ, DREAD, 2READ, RES, REMS, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, WRCR, PE, SE, BE32K, BE, CE, PP, DP, RSTEN, RST, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 8-1 Serial Peripheral Interface Modes Supported



Note:

CPOL indicates clock polarity of serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which serial mode is supported.

Standard SPI

The P25T22H/12H features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The P25T22H/12H supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast Read” (3BH and BBH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

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9 Commands

9.1 Commands listing

Figure 10-1 Command set

Commands	Abbr.	Code	ADR Bytes	DMY Bytes	Data Bytes	Function description
Read						
Read Array (fast)	FREAD	0Bh	3	1	1+	n bytes read out until CS# goes high
Read Array (low power)	READ	03h	3	0	1+	n bytes read out until CS# goes high
Read Dual Output	DREAD	3Bh	3	1	1+	n bytes read out by Dual output
Read 2x I/O	2READ	BBh	3	1	1+	n bytes read out by 2 x I/O
Program and Erase						
Page Erase	PE	81h	3	0	0	erase selected page
Sector Erase (4K bytes)	SE	20h	3	0	0	erase selected sector
Block Erase (32K bytes)	BE32	52h	3	0	0	erase selected 32K block
Block Erase (64K bytes)	BE64	D8h	3	0	0	erase selected 64K block
Chip Erase	CE	60h	0	0	0	erase whole chip
		C7h	0	0	0	erase whole chip
Page Program	PP	02h	3	0	1+	program selected page
Protection						
Write Enable	WREN	06h	0	0	0	sets the (WEL) write enable latch bit
Write Disable	WRDI	04h	0	0	0	resets the (WEL) write enable latch bit
Volatile SR Write Enable	VWREN	50h	0	0	0	Write enable for volatile status register
Status Register						
Read Status Register -0	RDSR	05h	0	0	1	read out status register
Read Configure Register	RDCR	15h	0	0	1	Read out configure register
Write Status Register	WRSR	01h	0	0	1	Write data to status/configuration registers
Write Configure Register	WRCR	11h	0	0	1	Write data to configuration register

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Command set (Cont'd)

Commands	Abbr.	Code	ADR Bytes	DMY Bytes	Data Bytes	Function
Other Commands						
Reset Enable	RSTEN	66h	0	0	0	Enable reset
Reset	RST	99h	0	0	0	Reset
Read Manufacturer/device ID	RDID	9Fh	0	0	1 to 3	output JEDEC ID: 1-byte manufacturer ID & 2-byte device ID
Read Manufacture ID	REMS	90h	3		1+	Read manufacturer ID/device ID data
Deep Power-down	DP	B9h	0	0	0	enters deep power-down mode
Release Deep Power-down/Read Electronic ID	RDP/RES	ABh	3	0	1	Read electronic ID data
Read unique ID	RUID	4Bh		4	1+	Read unique ID

NOTE:

1. Dual Output data

IO0 = (D6, D4, D2, D0)

IO1 = (D7, D5, D3, D1)

2. Dual Input Address

IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0

IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1

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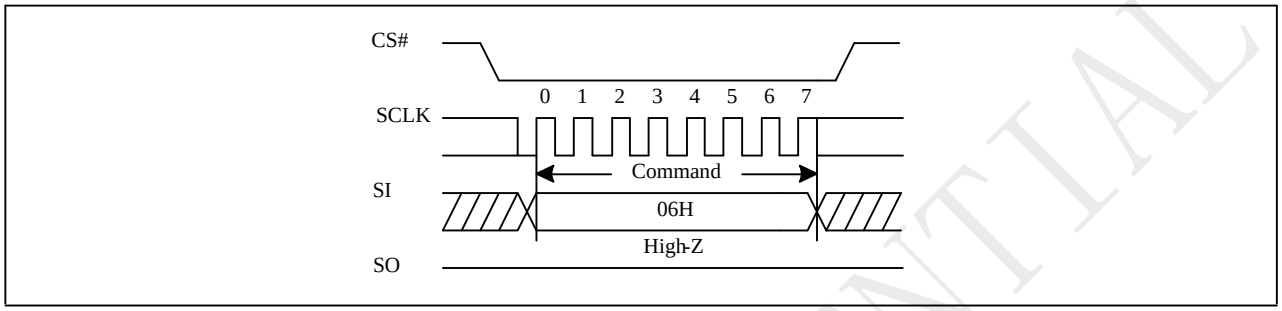
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9.2 Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, PE,SE, BE32K,BE, CE, and WRSR which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→ sending WREN instruction code→ CS# goes high.

Figure 10-2 Write Enable (WREN) Sequence (Command 06)



9.3 Write Disable (WRDI)

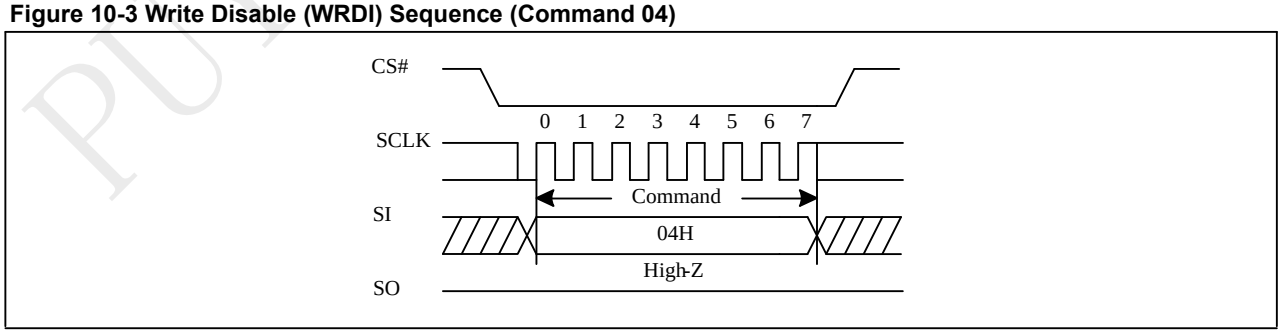
The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→ sending WRDI instruction code→ CS# goes high.

The WEL bit is reset by following situations:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Page Erase (PE) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE32K,BE) instruction completion
- Chip Erase (CE) instruction completion
- Reset (RST) instruction completion

Figure 10-3 Write Disable (WRDI) Sequence (Command 04)



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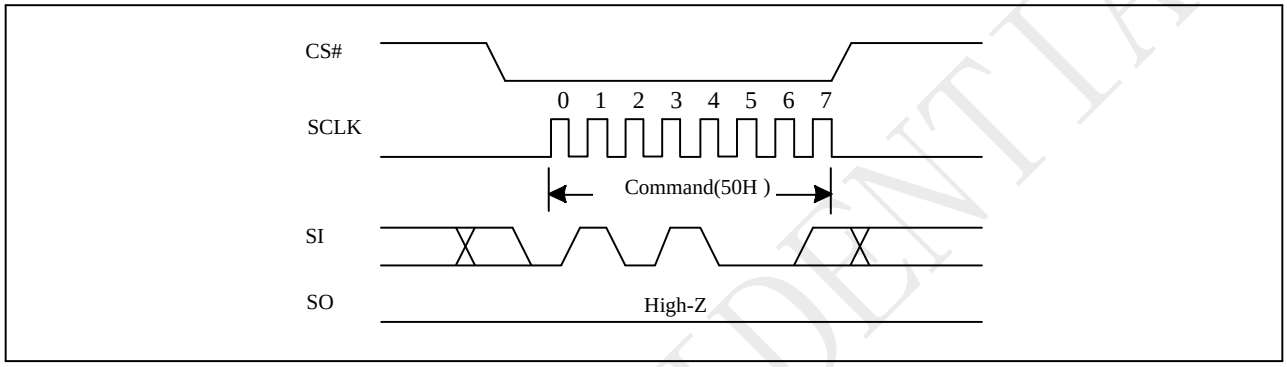
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9.4 Write Enable for Volatile Status Register

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

The sequence of issuing Write Enable for Volatile Status Register instruction is: CS# goes low→ sending Write Enable for Volatile Status Register instruction code→ CS# goes high.

Figure 10-4 Write Enable for Volatile Status Register Sequence (Command 50)

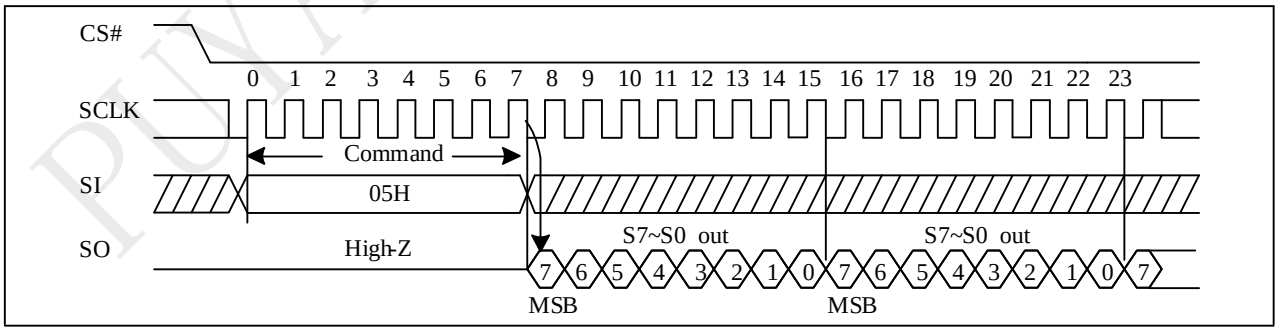


9.5 Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO. The SIO[3:1] are "don't care".

Figure 10-5 Read Status Register (RDSR) Sequence (Command 05)



Status Register

S7	S6	S5	S4	S3	S2	S1	S0
SRP	BP4	BP3	BP2	BP1	BP0	WEL	WIP

The definition of the status register bits is as below:

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WIP bit.

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP4, BP3, BP2, BP1, BP0 bits.

The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table “Protected Area Sizes”).becomes protected against Page Program (PP), Page Erase (PE), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed, only if the Block Protect (BP4, BP3, BP2, BP1and BP0) are set to “None protected”.

SRP bits.

The Status Register Protect (SRP) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection

SRP	WP#	Status Register	Description
0	x	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1.(Default)
1	0	Hardware Protected	WP#=0,the Status Register locked and can not be written to.
1	1	Hardware Unprotected	WP#=1,the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.

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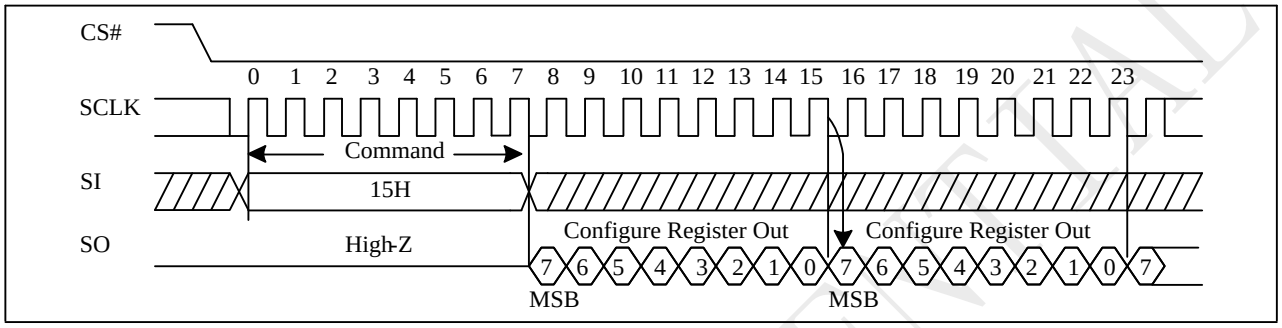
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9.6 Read Configure Register (RDCR)

The RDCR instruction is for reading Configure Register Bits. The Read Configure Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDCR instruction is: CS# goes low→ sending RDCR instruction code→ Configure Register data out on SO. The SIO[3:1] are "don't care".

Figure 10-6 Read Status Register (RDCR) Sequence (Command 15)



Configure Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DC	DRV1	DRV0	Reserved	Reserved	Reserved	Reserved	Reserved

DC bit

The Dummy Cycle (DC) bit can be used to configure the number of dummy clocks for “SPI 2 X IO Read (BBH)” command.

Table Dummy Cycle Table

SPI command	DC	Number of dummy
BBH	0(default)	4
	1	8

DRV1 & DRV0 bit.

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

Note: DRV1,DRV0 does not change the output driver strength with ordering option "D"

DRV1,DRV0	Drive Strength
0,0(default)	75%
0,1	100%
1,0	150%
1,1	50%

Reserved bit.

When write status register, the data of reserved bit must keep to "0".

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9.7 Write Status Register (WRSR)

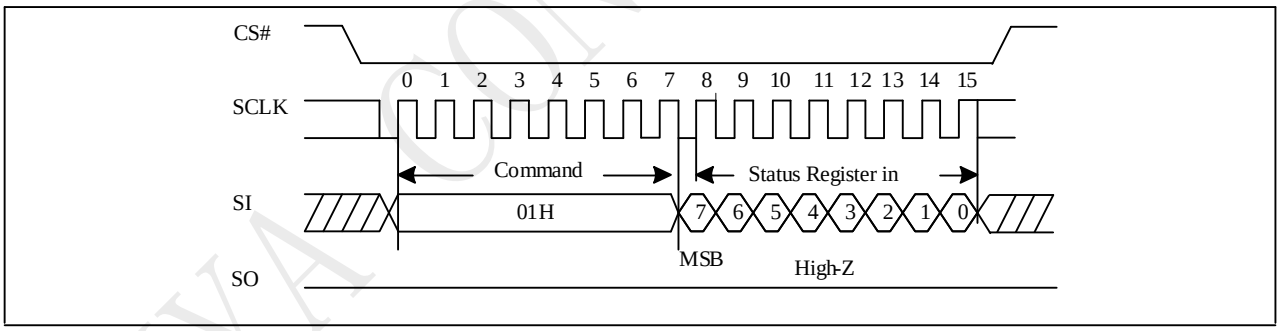
The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL). CS# must be driven high after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table1. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP) bits in accordance with the Write Protect (WP#) signal. The SRP bits and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register command is not executed once the Hardware Protected Mode is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→CS# goes high.

The CS# must go high exactly at the 8 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 10-8Write Status Register (WRSR) Sequence (Command 01)



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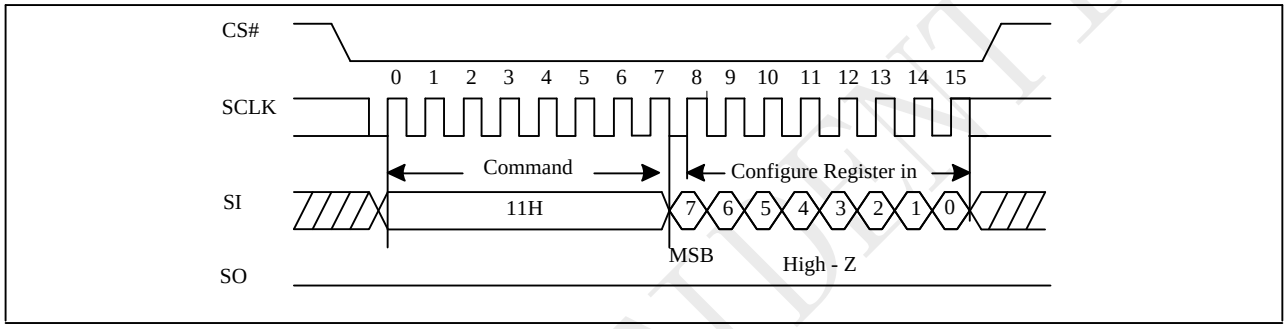
9.8 Write Configure Register (WRCR)

The Write Configure Register (WRCR) command allows new values to be written to the Configure Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch .

The sequence of issuing WRCR instruction is: CS# goes low→ sending WRCR instruction code→ Configure Register data on SI→CS# goes high.

The CS# must go high exactly at the 8 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Configure Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 10-9Write Configure Register (WRCR) Sequence (Command 11)

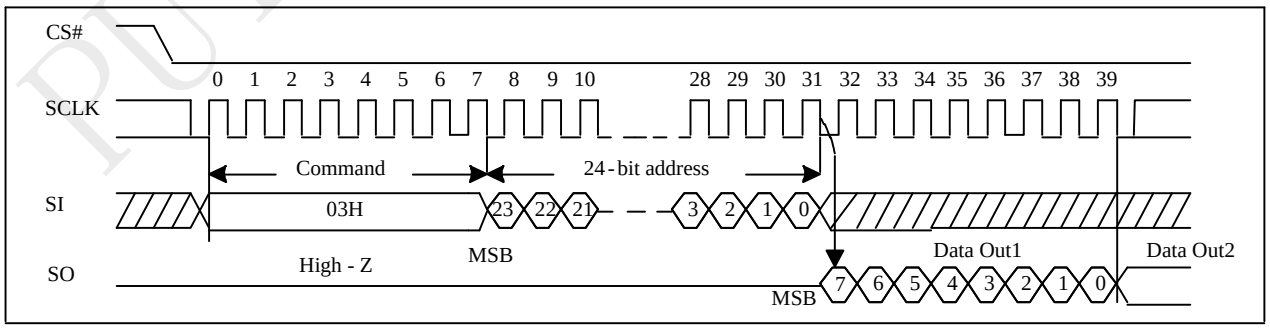


9.9 Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→ sending READ instruction code→ 3-byte address on SI→ data out on SO→ to end READ operation can use CS# to high at any time during data out.

Figure 10-10 Read Data Bytes (READ) Sequence (Command 03)



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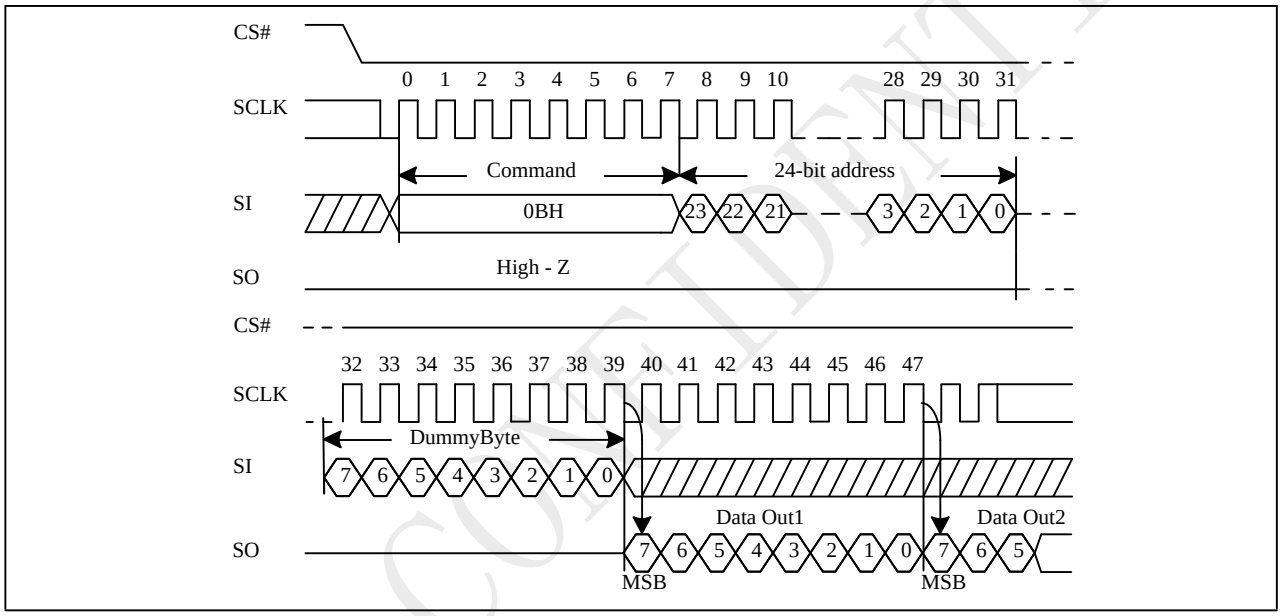
9.10 Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code→3-byte address on SI→ 1-dummy byte address on SI→data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 10-11 Read at Higher Speed (FAST_READ) Sequence (Command 0B)



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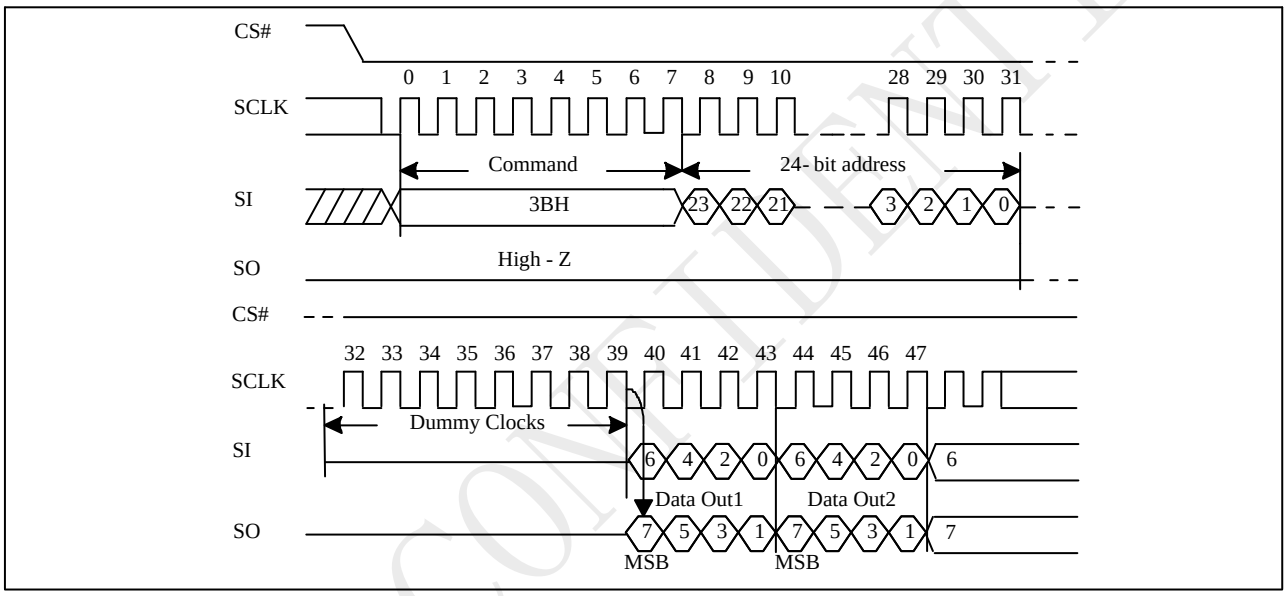
9.11 Dual Read Mode (DREAD)

The DREAD instruction enable double throughput of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing DREAD instruction is: CS# goes low → sending DREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SIO1 & SIO0 → to end DREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 10-12 Dual Read Mode Sequence (Command 3B)



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9.12 2 X IO Read Mode (2READ)

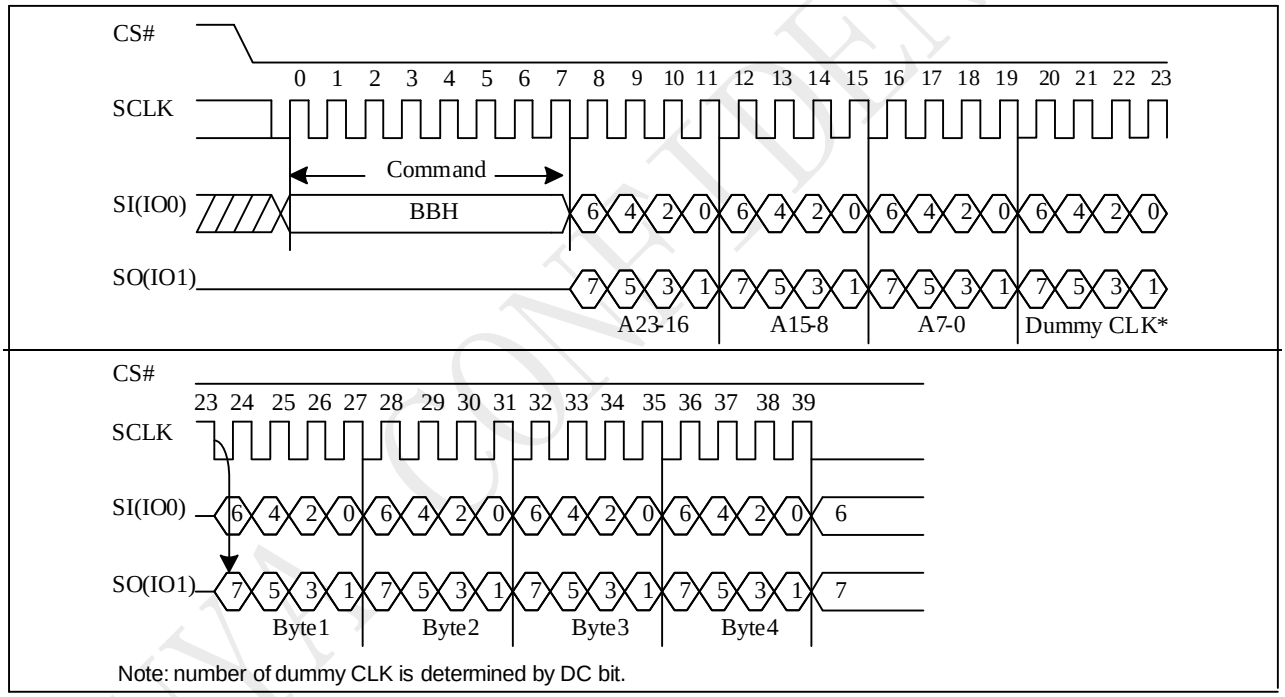
The 2READ instruction enables Double Transfer Rate of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached.

Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→ sending 2READ instruction→ 24-bit address interleave on SIO1 & SIO0→ 8-bit dummy cycle on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without anyimpact on the Program/Erase/Write Status Register current cycle.

Figure 10-13 2 X IO Read Mode Sequence (Command BB)



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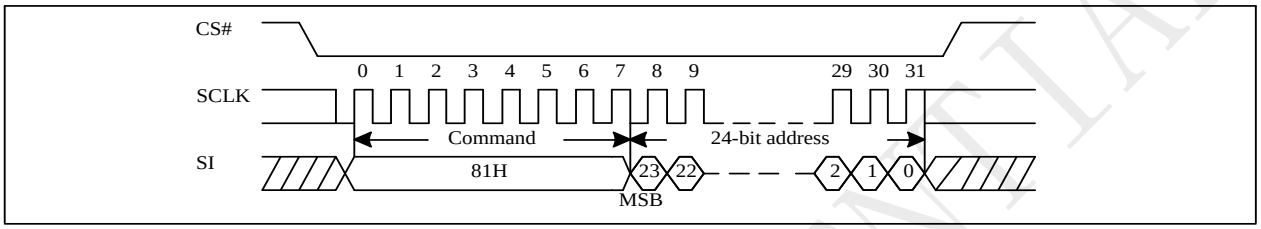
9.13 Page Erase (PE)

The Page Erase (PE) instruction is for erasing the data of the chosen Page to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Erase (PE).

To perform a Page Erase with the standard page size (256 bytes), an opcode of 81h must be clocked into the device followed by three address bytes comprised of 2 page address bytes that specify the page in the main memory to be erased, and 1 dummy byte.

ThesequenceofissuingPEinstructionis:CS#goeslow→sendingPEinstructioncode→3-byteaddressonSI→ CS# goes high.

Figure 10-15 Page Erase Sequence (Command 81)



9.14 Sector Erase (SE)

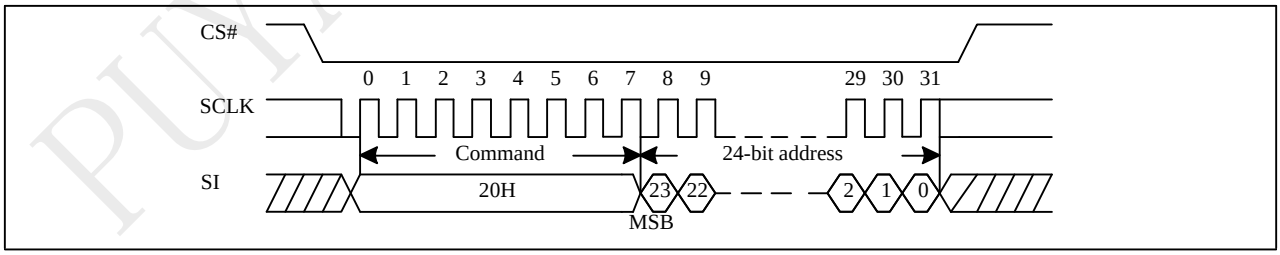
The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low → sending SE instruction code→ 3-byte address on SI → CS# goes high.

The SIO[3:1] are don't care.

Figure 10-16 Sector Erase (SE) Sequence (Command 20)



The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the sector is protected by BP4, BP3, BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the sector.

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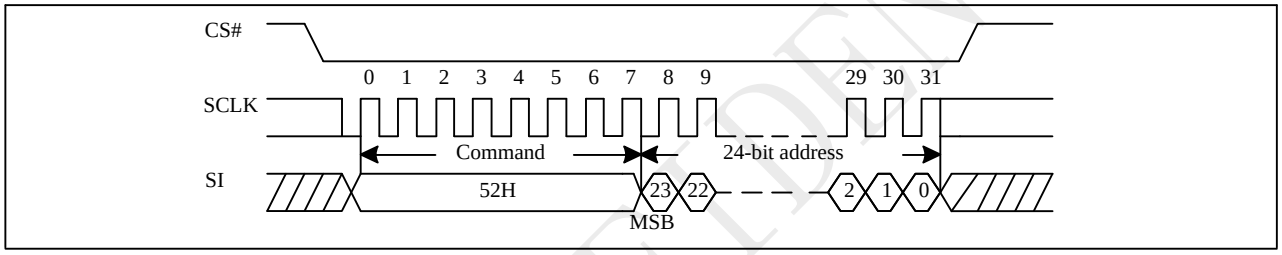
9.15 Block Erase (BE32K)

The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block is a valid address for Block Erase (BE32K) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte has been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE32K instruction is: CS# goes low → sending BE32K instruction code → 3-byte address on SI → CS# goes high. The SIO[3:1] are don't care.

The self-timed Block Erase Cycle time (tBE32K) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE32K timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP4, BP3, BP2, BP1,BP0 bits, the array data will be protected (no change) and the WEL bit still be reset.

Figure 10-17 Block Erase 32K(BE32K) Sequence (Command 52)



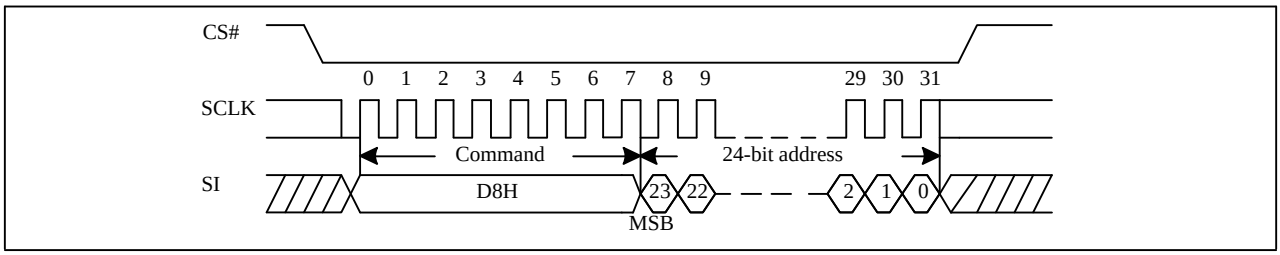
9.16 Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low→ sending BE instruction code→ 3-byte address on SI→CS# goes high. The SIO[3:1] are "don't care".

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Block Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP4, BP3, BP2, BP1, BP0 bits, the Block Erase (BE) instruction will not be executed on the block.

Figure 10-18 Block Erase (BE) Sequence (Command D8)



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9.17 Chip Erase (CE)

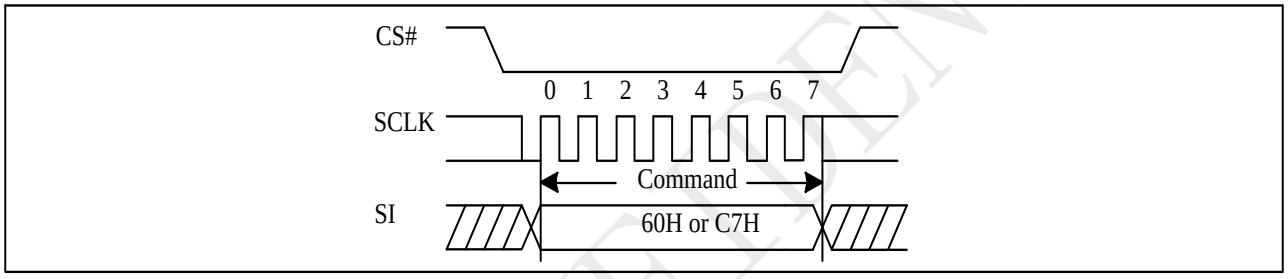
The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→ sending CE instruction code→ CS# goes high.

The SIO[3:1] are "don't care".

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Chip Erase cycle is in progress. The WIP sets 1 during the tCE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by BP4,BP3, BP2, BP1, BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when all Block Protect(BP4, BP3, BP2, BP1, BP0) are set to “None protected”.

Figure 10-19 Chip Erase (CE) Sequence (Command 60 or C7)



9.18 Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. If the entire 256 data bytes are going to be programmed, A7-A0 (The eight least significant address bits) should be set to 0. If the eight least significant address bits (A7-A0) are not all 0, all transmitted data going beyond the end of the current page are programmed from the start address of the same page (from the address A7-A0 are all 0). If more than 256 bytes are sent to the device, the data of the last 256-byte is programmed at the request page and previous data will be disregarded. If less than 256 bytes are sent to the device, the data is programmed at the requested address of the page.

For the very best performance, programming should be done in full pages of 256 bytes aligned on 256 byte boundaries with each Page being programmed only once. Using the Page Program (PP) command to load an entire page, within the page boundary, will save overall programming time versus loading less than a page into the program buffer.

It is possible to program from one byte up to a page size in each Page programming operation. Please refer to the P25T serial flash application note for multiple byte program operation within one page.

The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→ 3-byte address on SI→ at least 1-byte data on SI→ CS# goes high.

The CS# must be kept low during the whole Page Program cycle; The CS# must go high exactly at the byte

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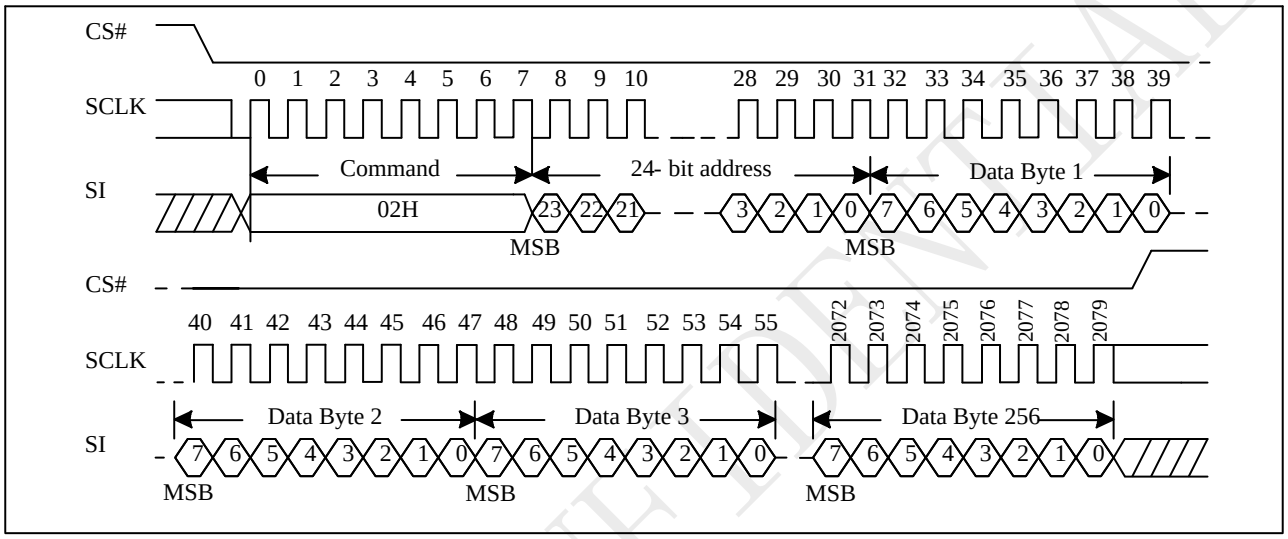
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boundary (the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP4, BP3, BP2, BP1, BP0 bits, the Page Program (PP) instruction will not be executed.

The SIO[3:1] are "don't care".

Figure 10-20 Page Program (PP) Sequence (Command 02)



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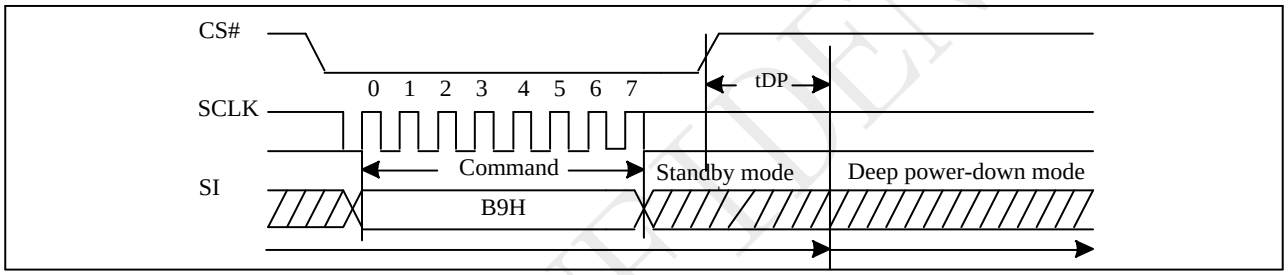
9.19 Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (to entering the Deep Power-down mode), the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When CS# goes high, it's only in standby mode not deep power-down mode. It's different from Standby mode.

The sequence of issuing DP instruction is: CS# goes low→ sending DP instruction code→ CS# goes high.

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction. (RES instruction to allow the ID been read out). When Power- down, the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For RDP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not be executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode and reducing the current to ISB2.

Figure 10-25 Deep Power-down (DP) Sequence (Command B9)



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9.20 Release form Deep Power-Down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven high, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and Chip Select (CS#) must remain High for at least tRES2(max). Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/ write cycle in progress.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2 (max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

The RDP instruction is for releasing from Deep Power-Down Mode.

Figure 10-26 Read Electronic Signature (RES) Sequence (Command AB)

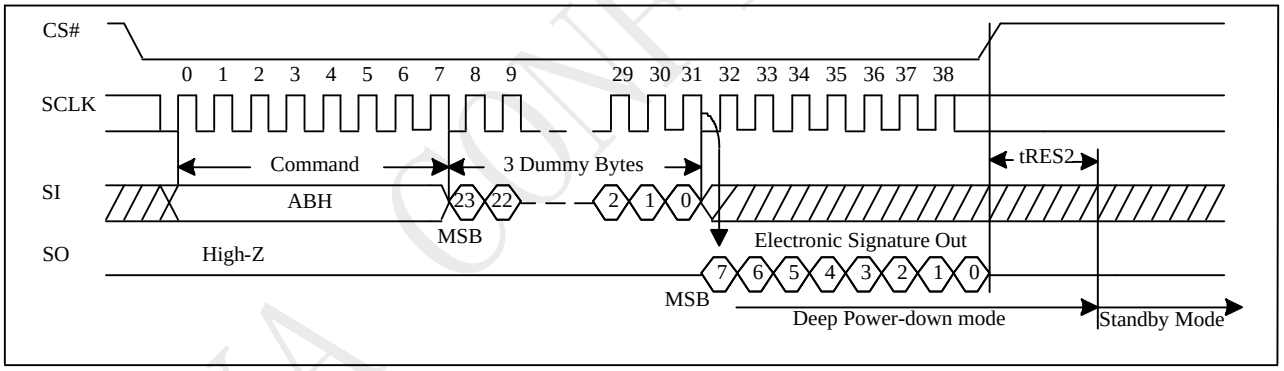
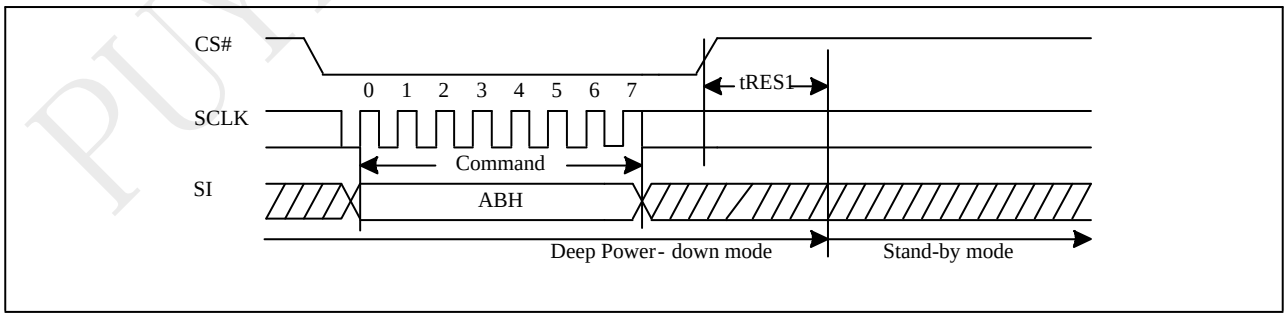


Figure 10-26a Release from Deep Power-down (RDP) Sequence (Command AB)



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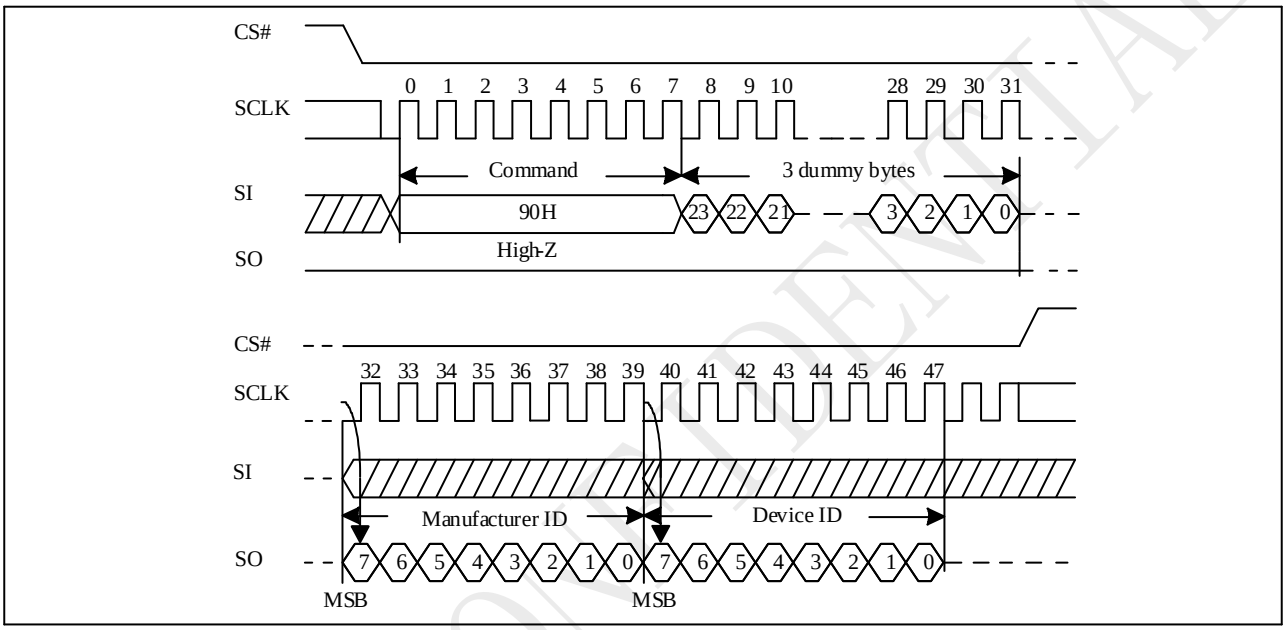
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9.21 Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction returns both the JEDEC assigned manufacturer ID and the device ID. The Device ID values are listed in "Table ID Definitions".

The REMS instruction is initiated by driving the CS# pin low and sending the instruction code "90h" followed by three dummy bytes. After which the manufacturer ID for PUYA (85h) and the device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first. While CS# is low, the manufacturer and device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 10-27 Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90)



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9.22 Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The PUYA Manufacturer ID and Device ID are list as “as "Table ID Definitions”.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code → 24-bits ID data out on SO→ to end RDID operation can use CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 10-29 Read Identification (RDID) Sequence (Command 9F)

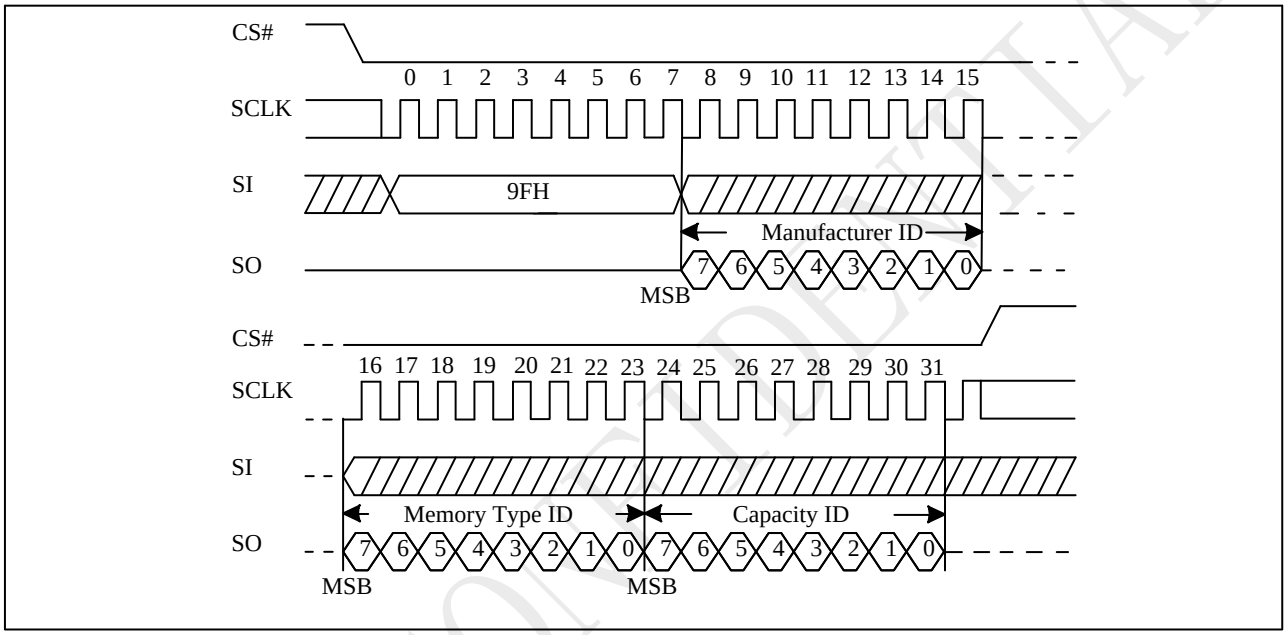


Table ID Definitions

P25T22H	RDID command	manufacturer ID	memory type	memory density
		85	44	12
	RES command	electronic ID		
		11		
	REMS command	manufacturer ID		device ID
		85		11
P25T12H	RDID command	manufacturer ID	memory type	memory density
		85	44	11
	RES command	electronic ID		
		10		
	REMS command	manufacturer ID		device ID
		85		10

9.23 No Operation (NOP)

The "No Operation" command is only able to terminate the Reset Enable (RSTEN) command and will not affect any other command.

The SIO[3:1] are don't care.

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9.24 Software Reset (RSTEN/RST)

The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command and Reset (RST) command. It returns the device to a standby mode. All the volatile bits and settings will be cleared then, which makes the device return to the default status as power on.

To execute Reset command (RST), the Reset-Enable (RSTEN) command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the Reset-Enable will be invalid.

The SIO[3:1] are "don't care".

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged or lost.

Figure 10-33 Software Reset Recovery

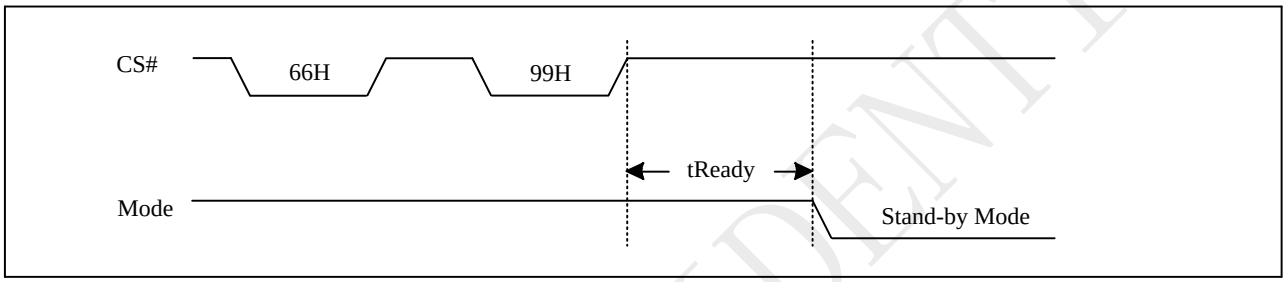
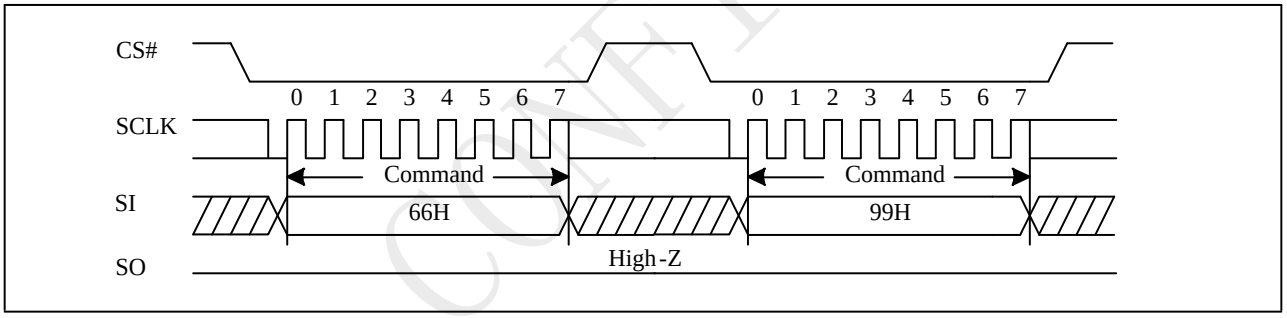


Figure 10-33a Reset Sequence



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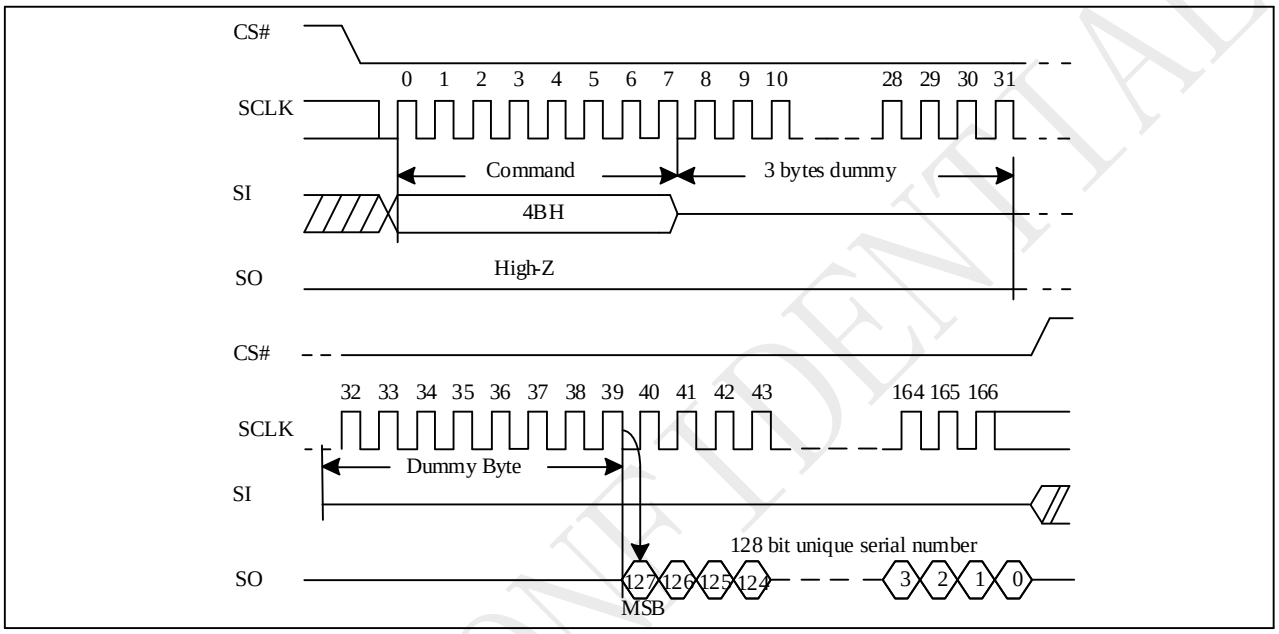
9.25 Read Unique ID(RUID)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each P25Txx device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low →sending Read Unique ID command →Dummy Byte1 →Dummy Byte2 →Dummy Byte3 →Dummy Byte4→128bit Unique ID Out →CS# goes high.

The command sequence is show below.

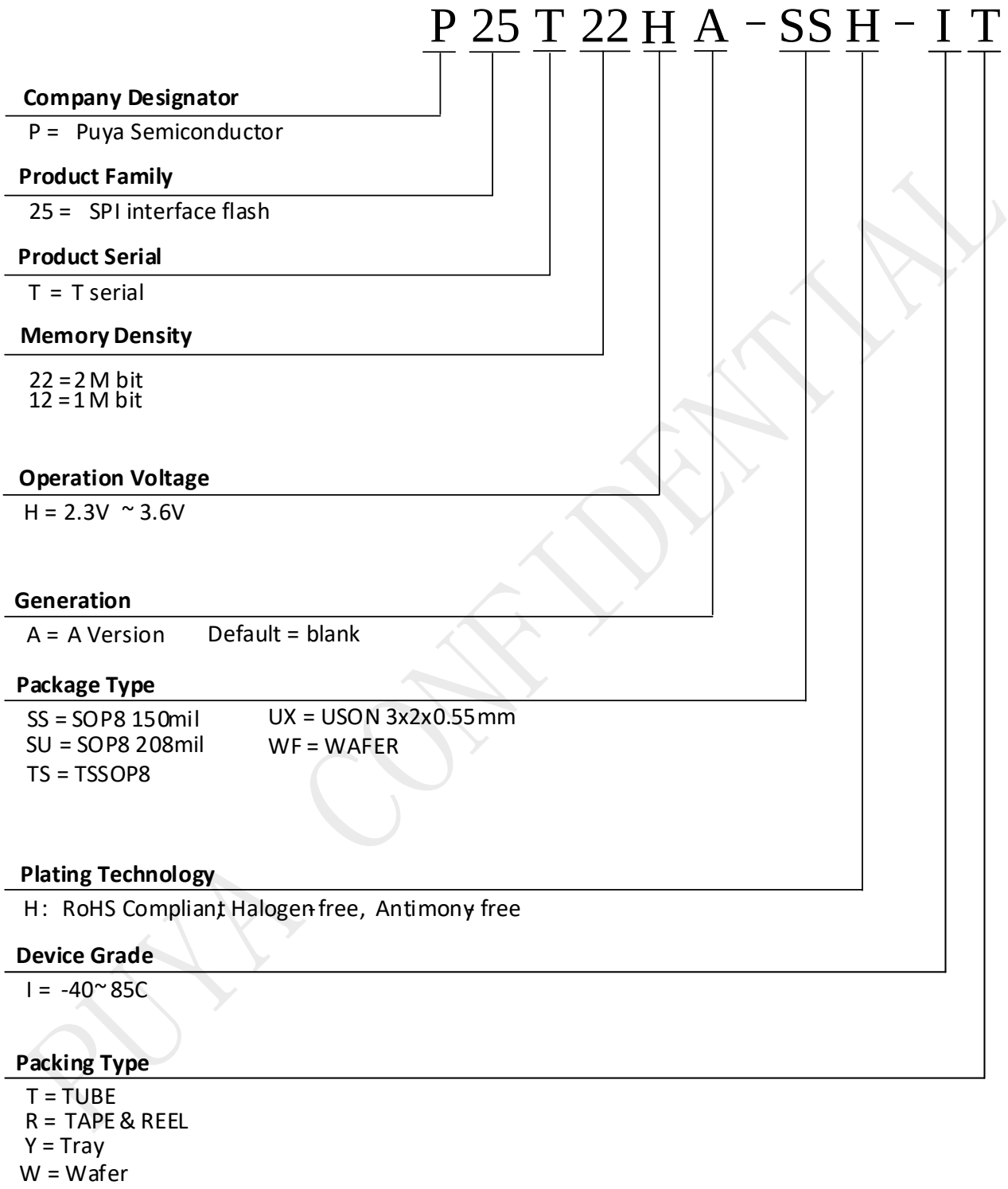
Figure 10-34 Read Unique ID (RUID) Sequence (Command 4B)



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10 Ordering Information



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11 Valid Part Numbers and Top Marking

The following table provides the valid part numbers for the P25T22H/12H Flash Memory. Please contact PUYA for specific availability by density and package type. PUYA Flash memories use a 14-digit Product Number for ordering.

2M bit Flash Valid Part Number

Package Type	Product Number	Density	Top Side Marking	Temp.	Packing Type
SS SOP8 150mil	P25T22H-SSH-IT	2M-bit	P25T22H xxxxxxx	85C	Tube
SS SOP8 150mil	P25T22H-SSH-IR	2M-bit	P25T22H xxxxxxx	85C	Reel
SU SOP8 208mil	P25T22H-SUH-IT	2M-bit	P25T22H xxxxxxx	85C	Tube
SU SOP8 208mil	P25T22H-SUH-IR	2M-bit	P25T22H xxxxxxx	85C	Reel
TS TSSOP8	P25T22H-TSH-IT	2M-bit	P25T22H xxxxxxx	85C	Tube
TS TSSOP8	P25T22H-TSH-IR	2M-bit	P25T22H xxxxxxx	85C	Reel
UX USON8 3x2x0.55mm	P25T22H-UXH-IR	2M-bit	PT22 HXXX	85C	Reel

1M bit Flash Valid Part Number

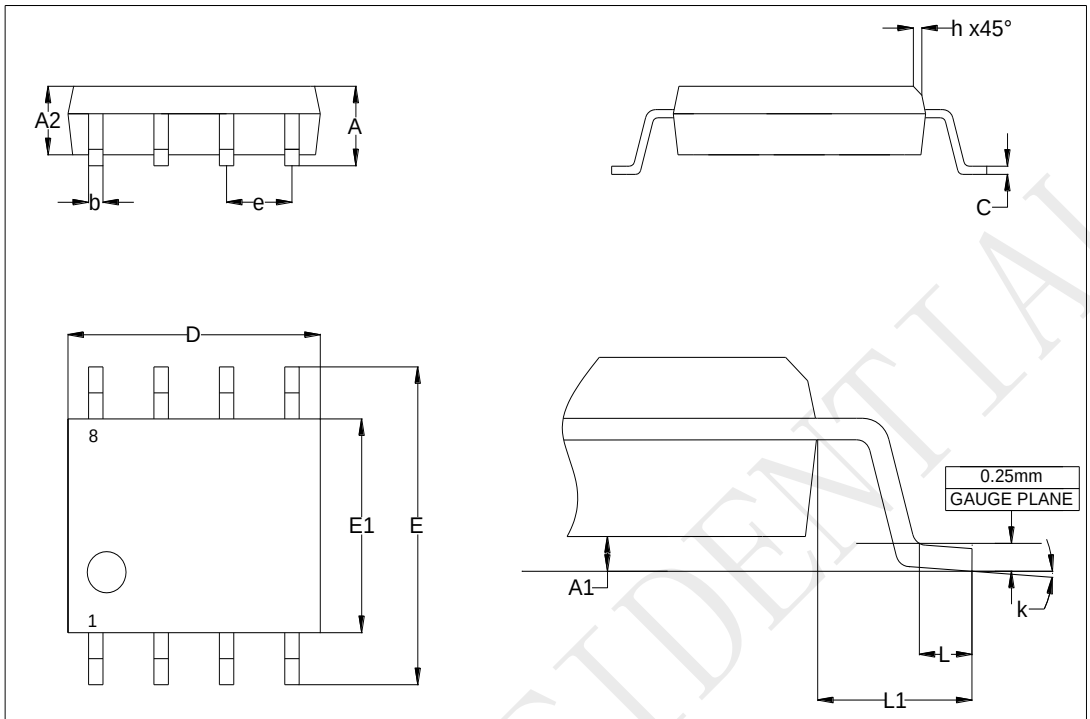
Package Type	Product Number	Density	Top Side Marking	Temp.	Packing Type
SS SOP8 150mil	P25T12H-SSH-IT	1M-bit	P25T12H xxxxxxx	85C	Tube
SS SOP8 150mil	P25T12H-SSH-IR	1M-bit	P25T12H xxxxxxx	85C	Reel

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12 Package Information

12.1 8-Lead SOP(150mil)



Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.750
A1	0.100	-	0.250
A2	1.250	-	-
b	0.280	-	0.480
c	0.170	-	0.230
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
e	-	1.270	-
h	0.250	-	0.500
k	0°	-	8°
L	0.400	-	1.270
L1	-	1.040	-

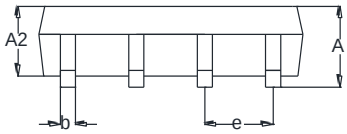
Note：1. Dimensions are not to scale

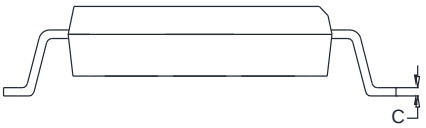
	TITLE	DRAWING NO.	REV
PUYA	8-lead SOP	SP-8	A

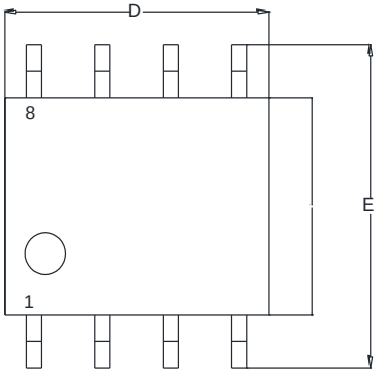
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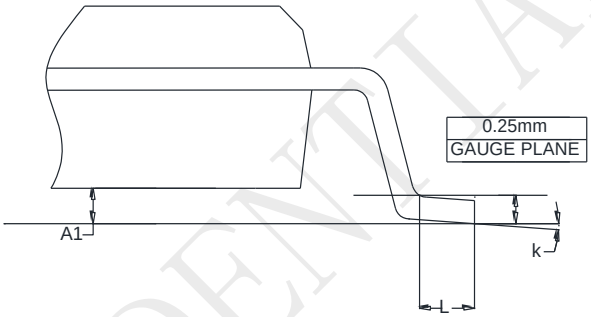
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12.2 8-Lead SOP(208mil)









Common Dimensions

(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	2.150
A1	0.050	-	0.250
A2	1.700	-	1.900
b	0.350	-	0.500
c	0.100	-	0.250
D	5.130	-	5.330
E	7.700		8.100
E1	5.180		5.380
e	-	1.270	-
k	0°	-	8°
L	0.500	-	0.850

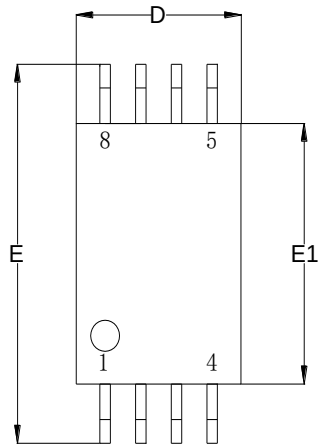
Note：1. Dimensions are not to scale

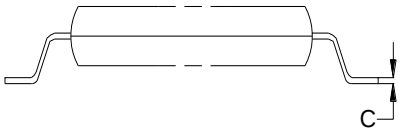
	TITLE	DRAWING NO.	REV
PUYA	8-lead SOP(208mil)	SP-8	A

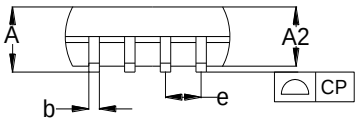
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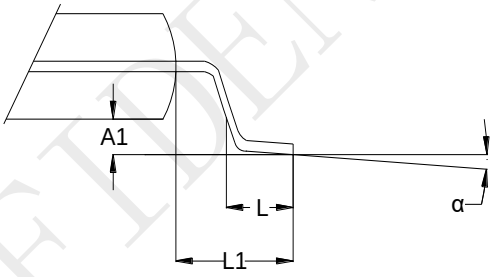
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12.3 8-Lead TSSOP









Common Dimensions

(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	1.000	1.050
b	0.190	-	0.300
c	0.090	-	0.200
CP	-	-	0.100
D	2.900	3.000	3.100
e	-	0.650	-
E	6.200	6.400	6.600
E1	4.300	4.400	4.500
L	0.450	0.600	0.750
L1	-	1.000	
α	0°	-	8°

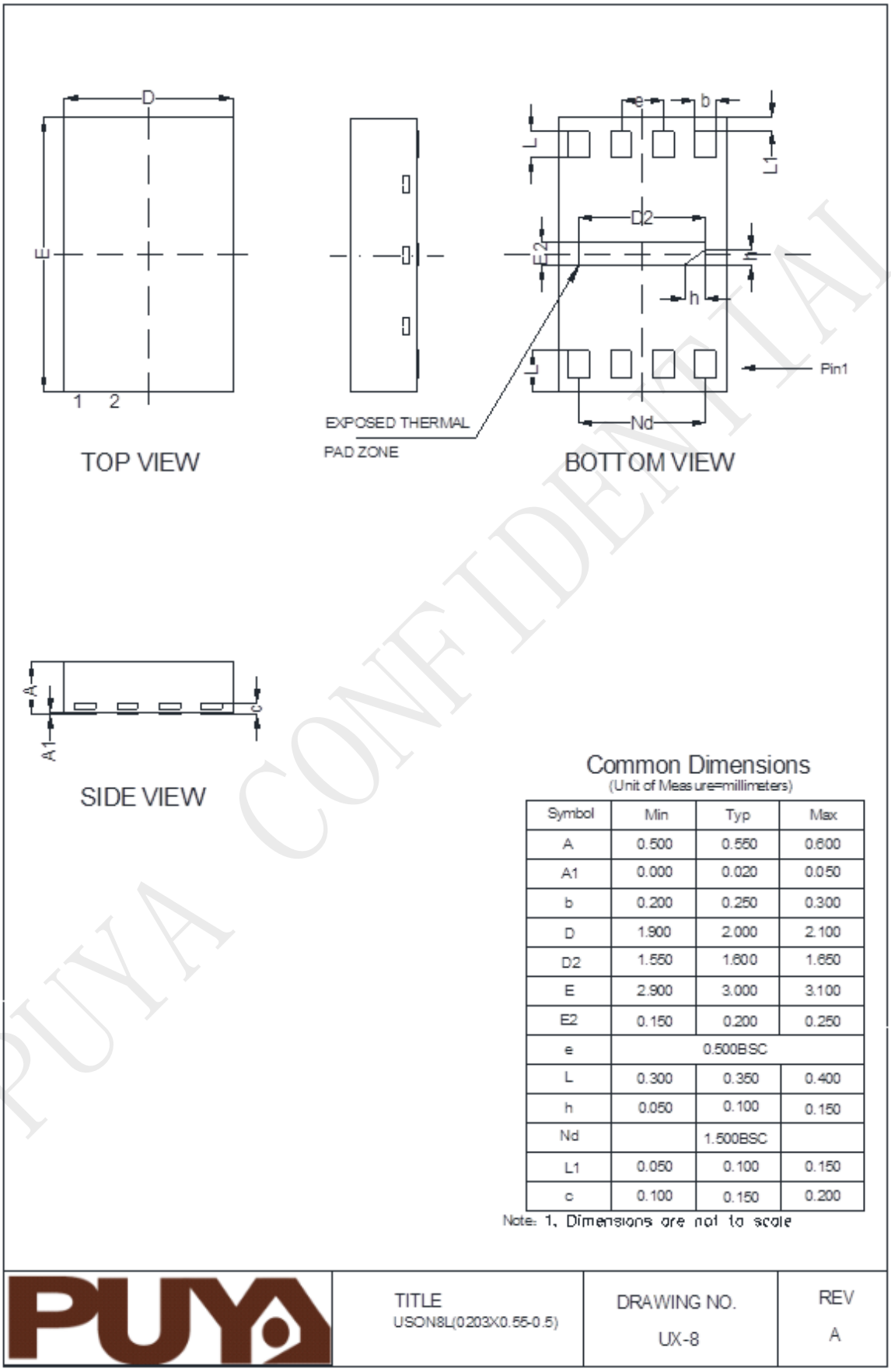
Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	8-lead TSSOP	TS-8	A

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12.4 8-land USON (3x2x0.55mm)



Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.500	0.550	0.600
A1	0.000	0.020	0.050
b	0.200	0.250	0.300
D	1.900	2.000	2.100
D2	1.550	1.600	1.650
E	2.900	3.000	3.100
E2	0.150	0.200	0.250
e		0.500BSC	
L	0.300	0.350	0.400
h	0.050	0.100	0.150
Nd		1.500BSC	
L1	0.050	0.100	0.150
c	0.100	0.150	0.200

Note: 1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	USON8L(0203X0.55-0.5)	UX-8	A

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13 Revision History

Rev.	Date	Description	Note
V1.0	2021-02-03	Initial release	-
V1.1	2021-05-18	Add USON 3x2x0.55mm POD Delete 512K configuration information	-

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