P24C64C

I²C-Compatible Serial E²PROM

Datasheet V2.3

General Description

The P24C64C is I²C-compatible Serial EEPROM (Electrically Erasable Programmable Memory) device. It contains a memory array of 64 Kbits (8 Kbytes), which is organized in 32 bytes per page.

Features

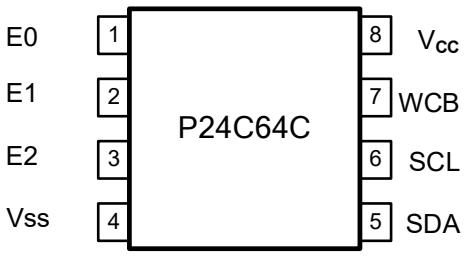
- Single Supply Voltage and High Speed Mode
  - Minimum operating voltage down to 1.7 V
  - 400 kHz/1 MHz clock from 1.7 V to 5.5 V
- Low power CMOS technology
  - Read current 0.2 mA (400 kHz, typical)
  - Write current 0.6 mA (400 kHz, typical)
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Sequential & Random Read Features
- 32 bytes Page Write Modes, Partial Page Writes Allowed
- Write protect of the whole memory array
- Additional Write Lockable Page
- Additional 128 bits Serial Number
- Self-timed Write Cycle (5 ms maximum)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - HBM: 6 kV
  - Latch up Capability: +/- 200 mA (25 C)
- Package: PDIP8, SOP8(150mil), MSOP8, TSSOP8, UDFN8, SOT23-5 and WLCSP4

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1. Pin Configuration

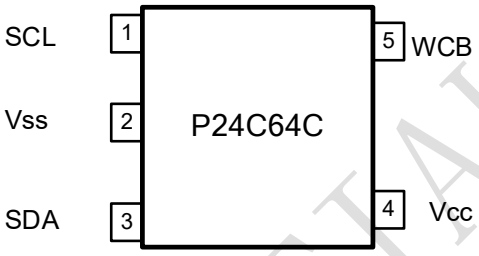
1.1 Pin Configuration

Figure 1-1 Pin Configuration



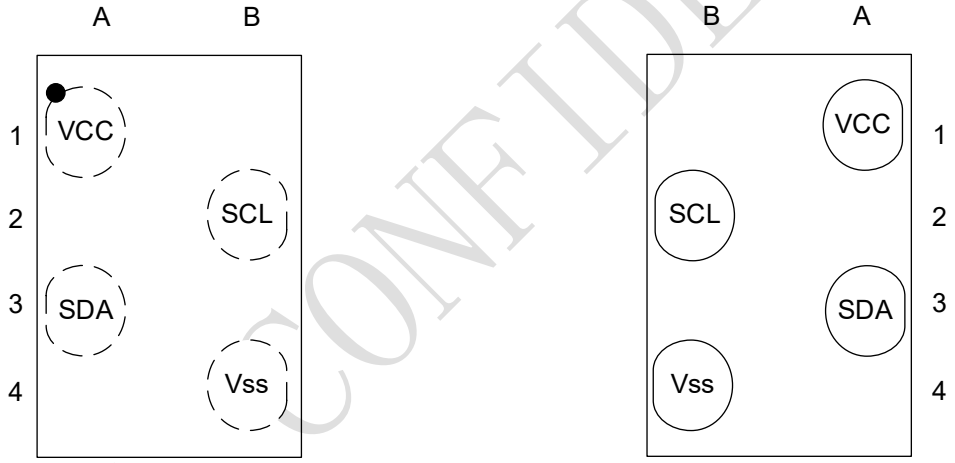
PDIP8/SOP8(150mil)/MSOP8/TSSOP8/UDFN8

TOP VIEW



SOT23-5

BOTTOM VIEW



WLCSP4 (Ball Pitch 320um*320um)

1.2 Pin Definition

Table 1-1 Pin Definition

Pin	Name	Type	Description
1	E0	Input	Slave Address Setting
2	E1	Input	Slave Address Setting
3	E2	Input	Slave Address Setting
4	Vss	Ground	Ground
5	SDA	I/O	Serial Data Input and Serial Data Output
6	SCL	Input	Serial Clock Input
7	WCB	Input	Write Control, Low Enable Write
8	V_{cc}	Power	Power

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Table 1-2 Pin Definition

Pin	Name	Type	Description
A1	V_{CC}	Power	Power
A3	SDA	I/O	Serial Data Input and Serial Data Output
B2	SCL	Input	Serial Clock Input
B4	Vss	Ground	Ground

1.3 Pin Descriptions

Serial Clock (SCL): The SCL input is used to positive-edge clock data in and negative-edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wired-OR'ed with any number of other open-drain or open-collector devices.

Device Addresses (E2, E1, E0): The E2, E1, and E0 pins are device address inputs. Typically, the E2, E1, and E0 pins are for hardware addressing and a total of 8 devices can be connected on a single bus system. If these pins are left floating, the E2, E1, and E0 pins will be internally pulled down to Vss.

Write Control (WCB): The Write Control input, when WCB is connected directly to V_{CC}, all write operations to the memory are inhibited. When connected to Vss, allows normal write operations. If the pin is left floating, the WCB pin will be internally pulled down to Vss.

Supply Voltage (V_{CC}): V_{CC} is the supply voltage.

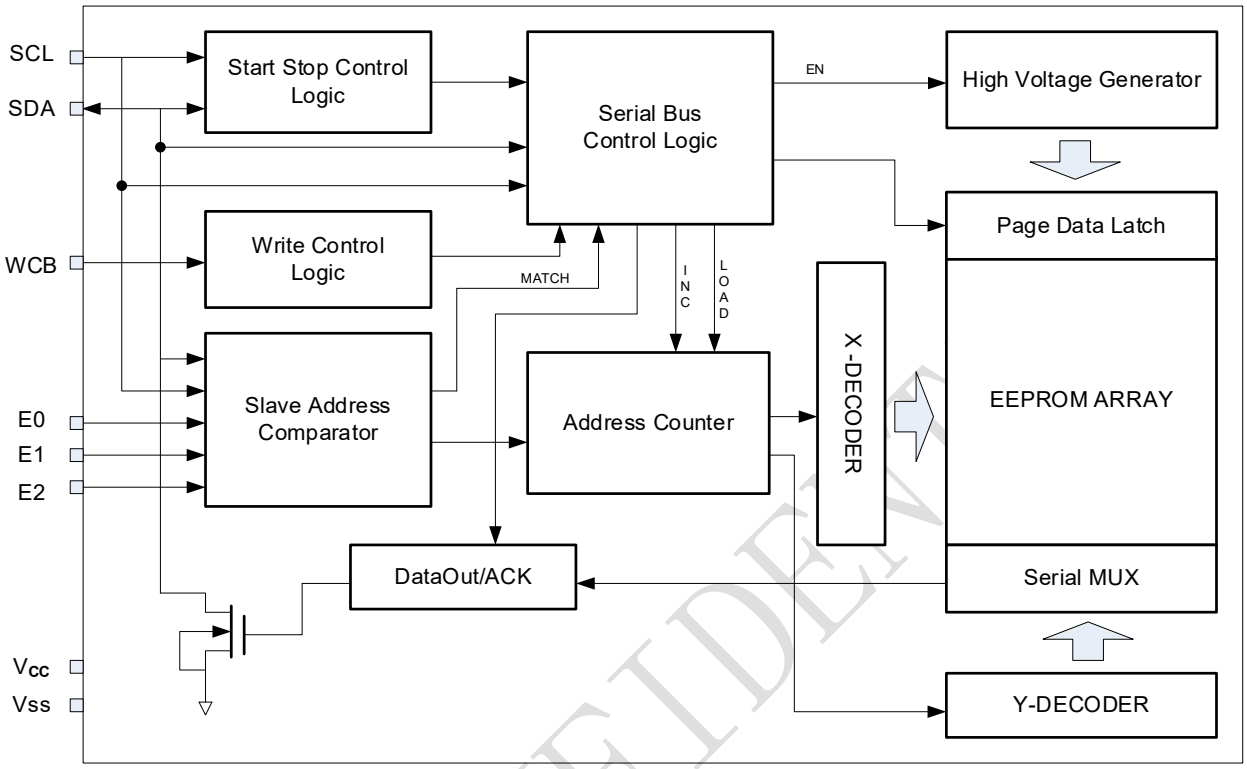
Ground (Vss): Vss is the reference for the V_{CC} supply voltage.

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2. Block Diagram

Figure 2-1 Block Diagram



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3. Electrical Characteristics

Table 3-1 Absolute Maximum Ratings [1]

Symbol	Parameter	Min.	Max.	Units
T_{STG}	Storage Temperature	-65	150	°C
T_A	Ambient operating temperature	-40	125	°C
V_{CC}	Supply Voltage	-0.5	6.5	V
V_{IO}	Input or output range	-0.5	6.5	V
I_{OL}	DC output current (SDA=0)	-	5	mA

Note: [1] Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3-2 Pin Capacitance [1]

Symbol	Parameter	Max.	Units	Test Condition
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$= Vss
C_{IN}	Input Capacitance (E0, E1, E2, WCB, SCL)	6	pF	V_{IN}= Vss

Note: [1] Test Conditions: T_A = 25°C, f_{SCL} = 1MHz, Vcc = 5.0V.

Table 3-3 DC Characteristics （Unless otherwise specified, V_{CC} = 1.7V to 5.5V, T_A = –40°C to 125°C）

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{CC}	Supply Voltage	1.7	-	5.5	V	
		1.8	-	5.5	V	
		2.5	-	5.5	V	
Isb	Standby Current	-	0.5	1.0	uA	Vcc = 3.3V, T_A = 85°C
		-	0.7	3.0	uA	Vcc = 5.5V, T_A = 85°C
		-	-	6.0	uA	Vcc = 5.5V, T_A = 105°C
		-	-	10.0	uA	Vcc = 5.5V, T_A = 125°C
I_{CC1}	Supply Current(Read)	-	0.2	0.4	mA	Vcc=5.5V，f_{SCL} = 400KHz
I_{CC2} [1]	Supply Current(Write)	-	0.6	1.0	mA	Vcc=5.5V，f_{SCL} = 400KHz
I_{LI}	Input Leakage Current	-	0.10	1.0	μA	V_{IN} = V_{CC} or Vss
I_{LO}	Output Leakage Current	-	0.05	1.0	μA	V_{OUT} = V_{CC} or Vss
V_{IL}	Input Low Level	–0.5	-	0.3V_{CC}	V	
V_{IH}	Input High Level	0.7V_{CC}	-	V_{CC}+0.5	V	
V_{OL1}	Output Low Level V_{CC} = 1.7V (SDA)	-	-	0.2	V	I_{OL} = 0.15 mA
V_{OL2}	Output Low Level V_{CC} = 3.0V (SDA)	-	-	0.4	V	I_{OL} = 2.1 mA

Note: [1] Characterized values, not tested in product.

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Table 3-4 100kHz AC Characteristics（Unless otherwise specified, V_{CC} = 1.7V to 5.5V, T_A = –40°C to 125°C, C_L=100pF, Test Conditions are listed in Notes [2] ）

Symbol	Parameter	1.7≤V_{CC}≤5.5			Units
		Min.	Typ.	Max.	
f_{SCL}	Clock Frequency, SCL	-	-	100	kHz
t_{LOW}	Clock Pulse Width Low	4.7	-	-	μs
t_{HIGH}	Clock Pulse Width High	4	-	-	μs
t_{AA}	Clock Low to Data Out Valid	0.05	-	3.45	μs
t_I	Noise Suppression Time	-	-	0.1	μs
tBUF	Time the bus must be free before a new transmission can start	4.7	-	-	μs
$t_{HD.STA}$	Start Hold Time	4	-	-	μs
$t_{SU.STA}$	Start Setup Time	4.7	-	-	μs
$t_{HD.DAT}$	Data In Hold Time	0	-	-	μs
$t_{SU.DAT}$	Data In Setup Time	0.25	-	-	μs
t_R	Inputs Rise Time[1]	-	-	1	μs
t_F	Inputs Fall Time[1]	-	-	0.3	μs
$t_{SU.STO}$	Stop Setup Time	4	-	-	μs
t_{DH}	Data Out Hold Time	0.05	-	-	μs
$t_{SU.WCB}$	WCB pin Setup Time	4	-	-	μs
$t_{HD.WCB}$	WCB pin Hold Time	4	-	-	μs
t_{WR}	Write Cycle Time	-	-	5	ms

Notes: [1] This parameter is ensured by characterization not 100% tested

Table 3-5 400kHz&1Mhz AC Characteristics（Unless otherwise specified, V_{CC} = 1.7V to 5.5V, T_A = –40°C to 125°C, C_L=100pF, Test Conditions are listed in Notes [2] ）

Symbol	Parameter	1.7≤V_{CC}≤5.5			1.7≤V_{CC}≤5.5			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Clock Frequency, SCL	-	-	400	-	-	1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3	-	-	0.4	-	-	μs
t_{HIGH}	Clock Pulse Width High	0.6	-	-	0.4	-	-	μs
t_{AA}	Clock Low to Data Out Valid	0.05	-	0.9	0.05	-	0.55	μs
t_I	Noise Suppression Time	-	-	0.1	-	-	0.05	μs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3	-	-	0.5	-	-	μs
$t_{HD.STA}$	Start Hold Time	0.6	-	-	0.25	-	-	μs
$t_{SU.STA}$	Start Setup Time	0.6	-	-	0.25	-	-	μs
$t_{HD.DAT}$	Data In Hold Time	0	-	-	0	-	-	μs
$t_{SU.DAT}$	Data In Setup Time	0.1	-	-	0.1	-	-	μs
t_R	Inputs Rise Time[1]	-	-	0.3	-	-	0.3	μs
t_F	Inputs Fall Time[1]	-	-	0.3	-	-	0.1	μs
$t_{SU.STO}$	Stop Setup Time	0.6	-	-	0.25	-	-	μs
t_{DH}	Data Out Hold Time	0.05	-	-	0.05	-	-	μs
$t_{SU.WCB}$	WCB pin Setup Time	1.2	-	-	0.6	-	-	μs

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Symbol	Parameter	1.7≤V_{CC}≤5.5			1.7≤V_{CC}≤5.5			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_{HD.WCB}$	WCB pin Hold Time	1.2	-	-	0.6	-	-	μs
t_{WR}	Write Cycle Time	-	-	5	-	-	5	ms

Note: [1] This parameter is ensured by characterization not 100% tested

[2] AC measurement conditions:

- R_L (connects to V_{CC}): 1.3k (2.5V, 5.5V), 10k (1.7V)
- Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}
- Input rise and fall times: ≤50ns
- Input and output timing reference voltages: 0.5V_{CC}

Table 3-6 Reliability Characteristic [1]

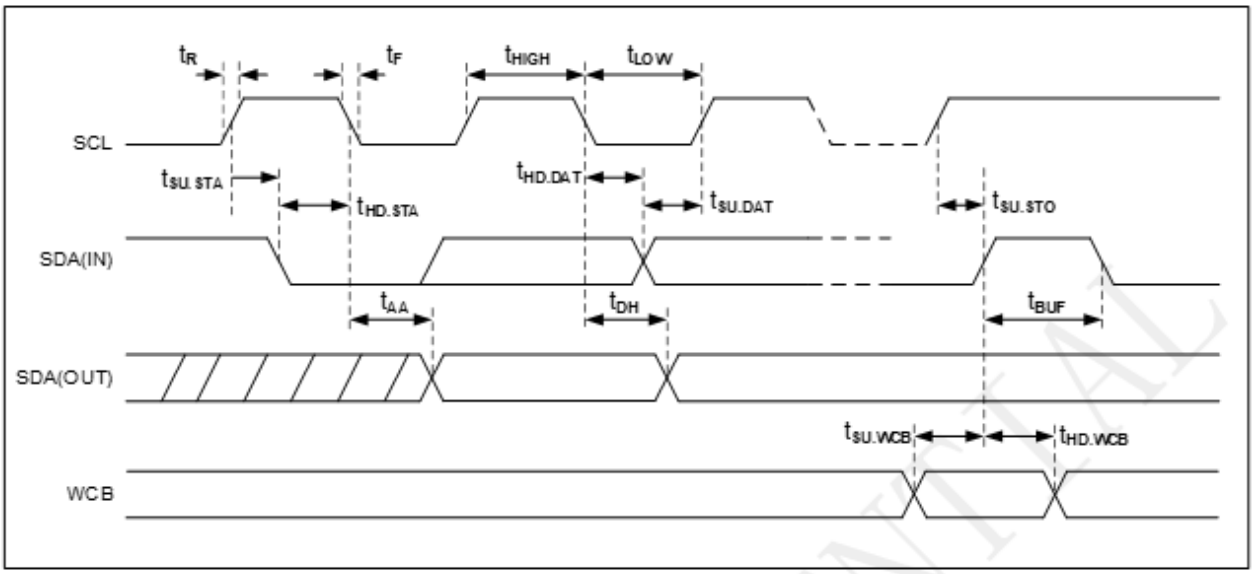
Symbol	Parameter	Min.	Typ.	Max.	Unit
EDR[2]	Endurance	1,000,000			Write cycles
DRET[3]	Data retention	100			Years

Note: [1] This parameter is ensured by characterization not 100% tested

[2] Under the condition: 25°C, 3.3V, Page mode

[3] Test condition: T_A = 55°C

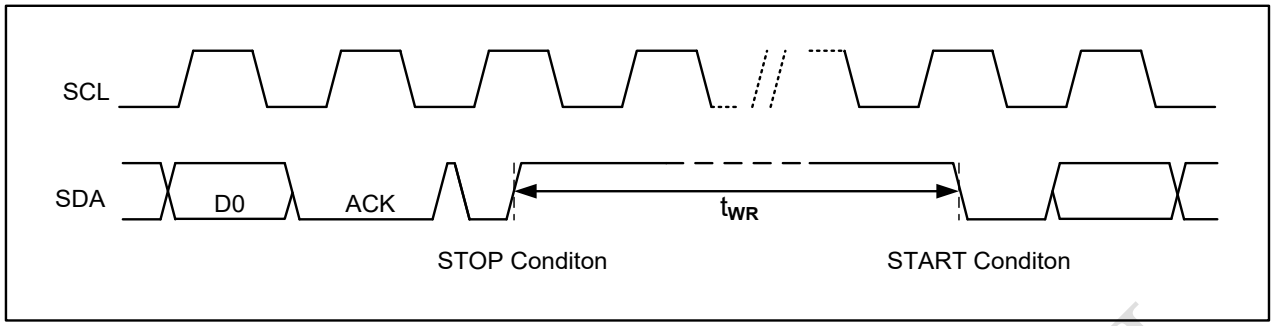
Figure 3-1 Bus Timing



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Figure 3-2 Write Cycle Timing



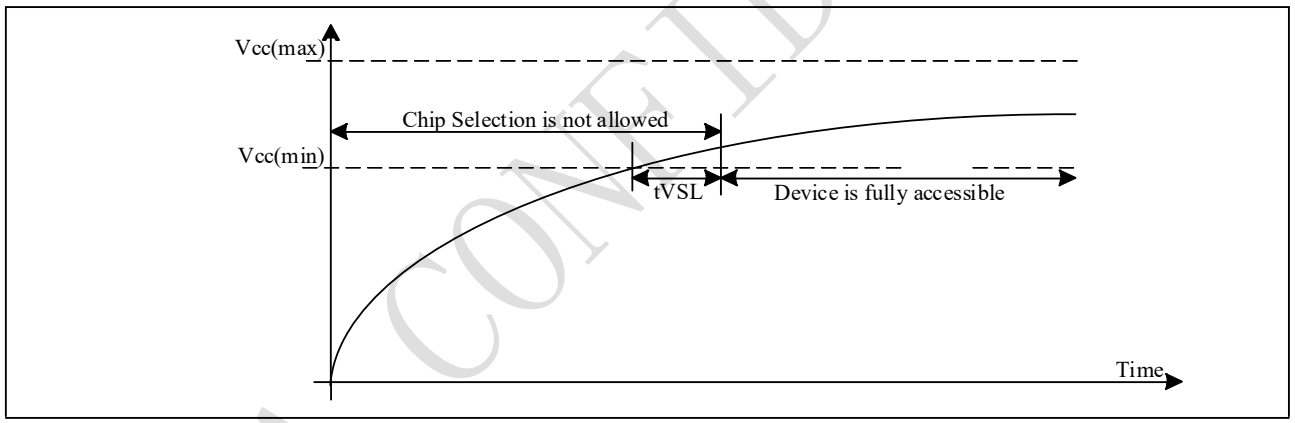
Note: [1] The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Device Power-Up

The EEPROM has a built-in power-on-reset circuit that initializes itself at the same time during power-on. Unsuccessful initialization may cause a malfunction. To operate the power-on-reset circuit normally, the following conditions must be satisfied to raise the power supply voltage.

When initialization is successfully completed by the power-on-reset circuit, the EEPROM enters the standby status. tVSL is the time required to initialize the EEPROM. No instructions are accepted during this time.

Figure 3-3 Power up Timing



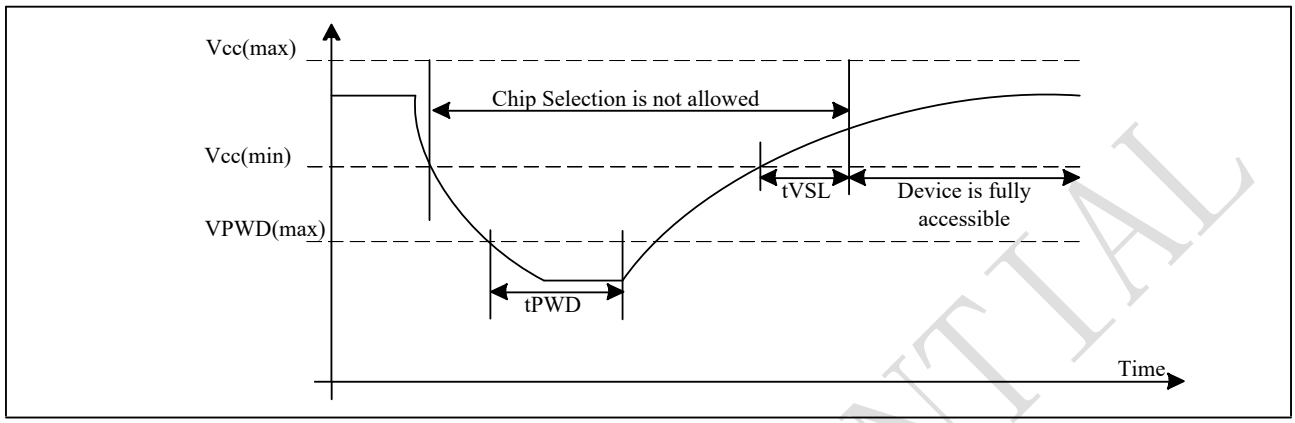
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Power Up/Down and Voltage Drop

For Power-down to Power-up operation, the VCC of EEPROM device must below VPWD for at least tPWD timing. Please check the table below for more detail.

Figure 3-4 Power down-up Timing



Symbol	Parameter	min	max	unit
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		0.7	V
tPWD	The minimum duration for ensuring initialization will occur	300		us
tVSL	VCC(min.) to device operation	70		us
tVR	VCC Rise Time	1	500000	us/V

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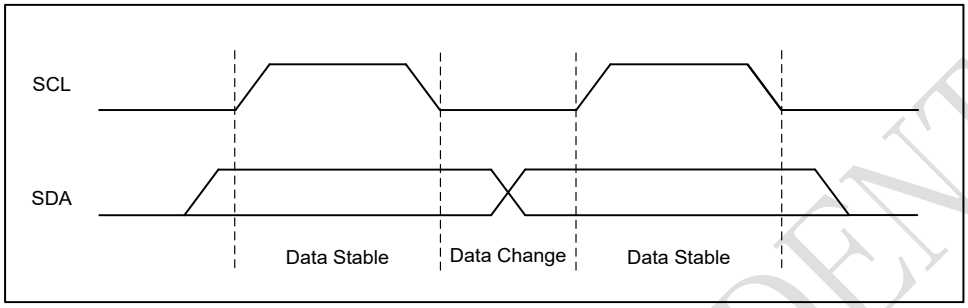
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4. Device Operation

4.1 Data Input

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 4-1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

Figure 4-1 Data Validity



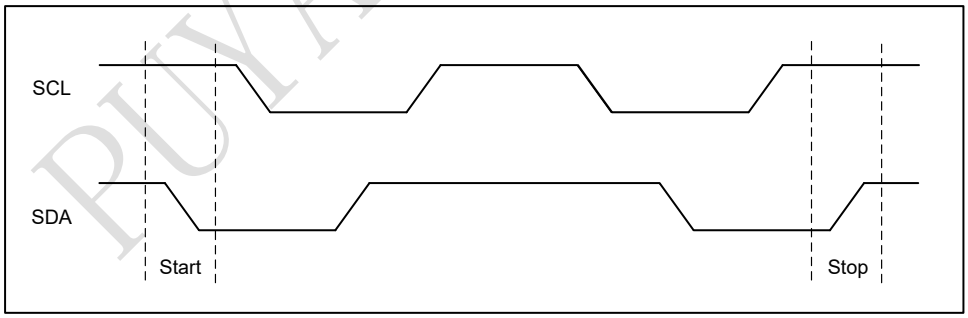
4.2 Start Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 4-2).

4.3 Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the P24C64C in a standby mode (see Figure 4-2).

Figure 4-2 Start and Stop Definition



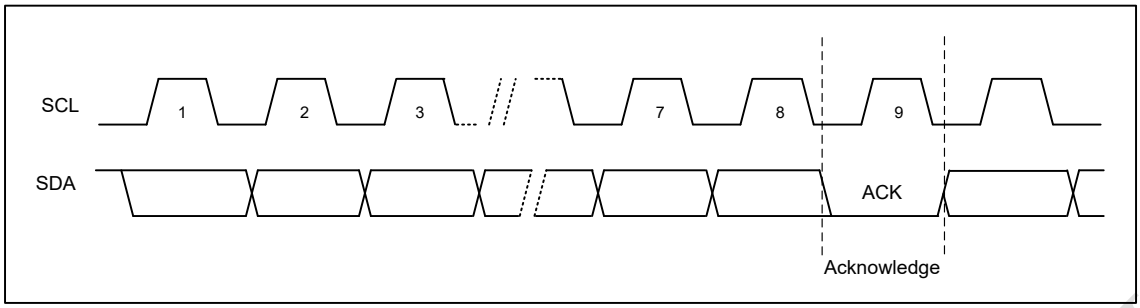
4.4 Acknowledge (ACK)

All addresses and data words are serially transmitted to and from the P24C64C in 8-bit words. The P24C64C sends a “0” to acknowledge that it has received each word. This happens during the ninth clock cycle.

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Figure 4-3 Output Acknowledge



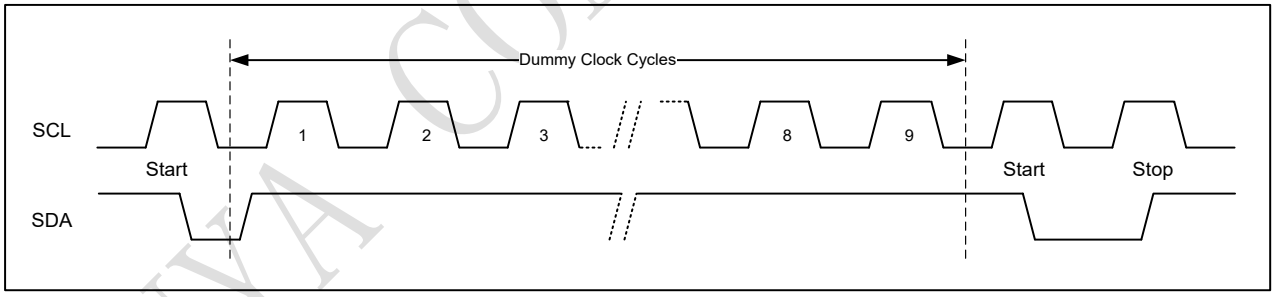
4.5 Standby Mode

The P24C64C features a low-power standby mode which is enabled: (a) after a fresh power up, (b) after receiving a STOP bit in read mode, and (c) after completing a self-time internal programming operation

4.6 Soft Reset

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps: (a) Create a start condition, (b) Clock nine cycles, and (c) create another start bit followed by stop bit condition, as shown below. The device is ready for the next communication after the above steps have been completed.

Figure 4-4 Soft Reset



4.7 Device Addressing

The P24C64C requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see table below). The device address word consists of a mandatory one-zero sequence for the first four most-significant bits, as shown.

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Table 4-1 Device Address

Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal Area	1	0	1	0	E2	E1	E0	R/W
ID Page	1	0	1	1	E2	E1	E0	R/W
ID LOCK Bit	1	0	1	1	E2	E1	E0	R/W
Serial Number	1	0	1	1	E2	E1	E0	1

Table 4-2 First Word Address

Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal Area	X	X	X	A12	A11	A10	A9	A8
ID Page	X	X	X	X	0	0	X	X
ID LOCK Bit	X	X	X	X	X	1	X	X
Serial Number	X	X	X	X	1	0	X	X

Table 4-3 Second Word Address

Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal Area	A7	A6	A5	A4	A3	A2	A1	A0
ID Page	X	X	X	A4	A3	A2	A1	A0
ID LOCK Bit	X	X	X	X	X	X	X	X
Serial Number	X	X	X	X	A3	A2	A1	A0

The three E2, E1, and E0 device address bits to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins.

The E2, E1, and E0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are floating.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a compare of the device address, the Chip will output a zero. If a compare is not made, the device will return to a standby state.

4.8 Data Security

P24C64C has a hardware data protection scheme that allows the user to write protect the whole memory when the WCB pin is at Vcc.

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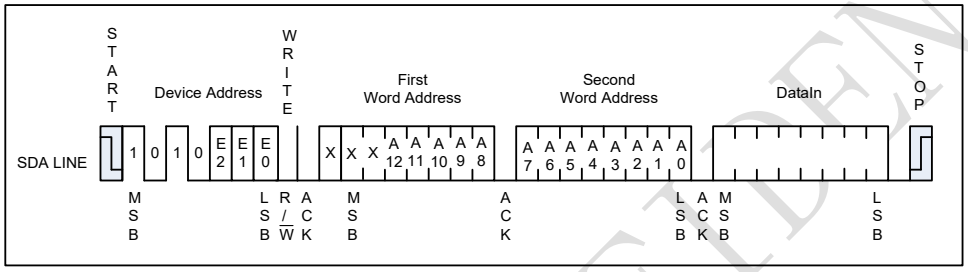
5. Instructions

5.1 Write Operations

5.1.1 Byte Write

A write operation requires two 8-bit data word address (A12~A0) following the device address word and acknowledgment. Upon receipt of this address, the P24C64C will again respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the P24C64C will output a “0” and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. And then the P24C64C enters an internally timed write cycle, all inputs are disabled during this write cycle and the P24C64C will not respond until the write is complete (see Figure 5-1).

Figure 5-1 Byte Write

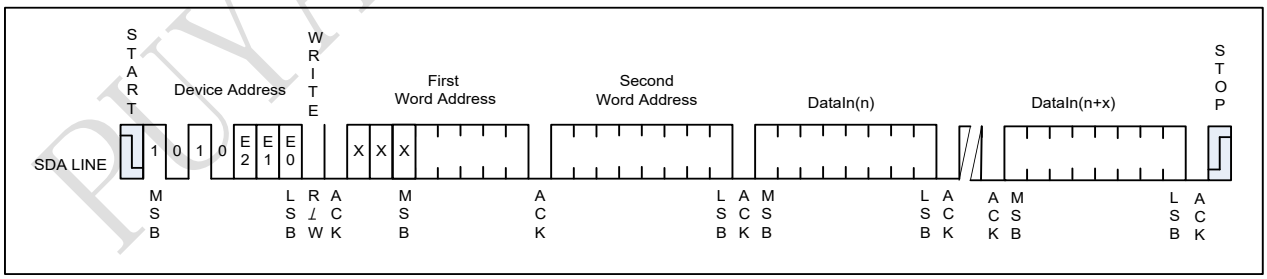


Notes: [1] x means don’t care.

5.1.2 Page Write

A page write is initiated the same as a byte write, but the master does not send a stop condition after the first data word is clocked in. Instead, after the P24C64C acknowledges receipt of the first data word, the master can transmit more data words. The P24C64C will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition.

Figure 5-2 Page Write



The lower five bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the P24C64C, the data word address will roll over, and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

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5.1.3 Acknowledge Polling

Once the internally timed write cycle has started and the P24C64C inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the P24C64C respond with a “0”, allowing the read or write sequence to continue.

5.1.4 Write Identification Page

The Identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier = 1011b
- Word Address bits A11~A10 which must be ‘00’.
- LSB address bits A4~A0 define the byte address inside the Identification page. If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoACK).

5.1.5 Lock Identification Page

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

- Device type identifier = 1011b
- Address bit A10 must be ‘1’; all other address bits are don’t care
- The data byte must be equal to the binary value xxxx xx1x, where x is don’t care

5.2 Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to “1”. There are three read operations: Current Address Read; Random Address Read and Sequential Read.

5.2.1 Current Address Read

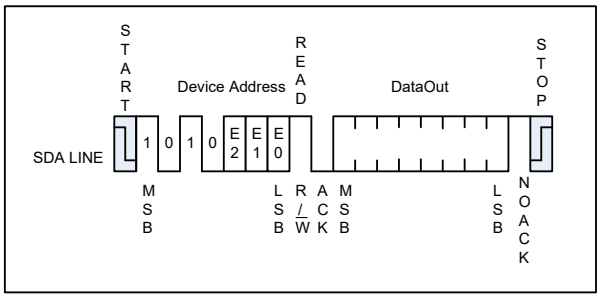
The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to “1” is clocked in and acknowledged by the P24C64C, the current address data word is serially clocked out. The microcontroller does not respond with an input “0” but does generate a following stop condition (see Figure 5-3).

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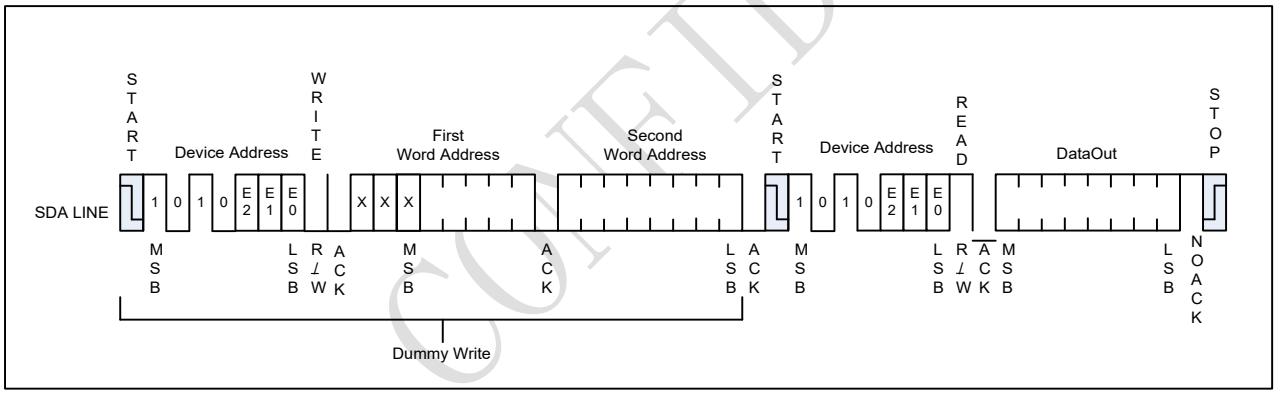
Figure 5-3 Current Address Read



5.2.2 Random Read

A Random Read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the P24C64C, the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The P24C64C acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 5-4).

Figure 5-4 Random Read



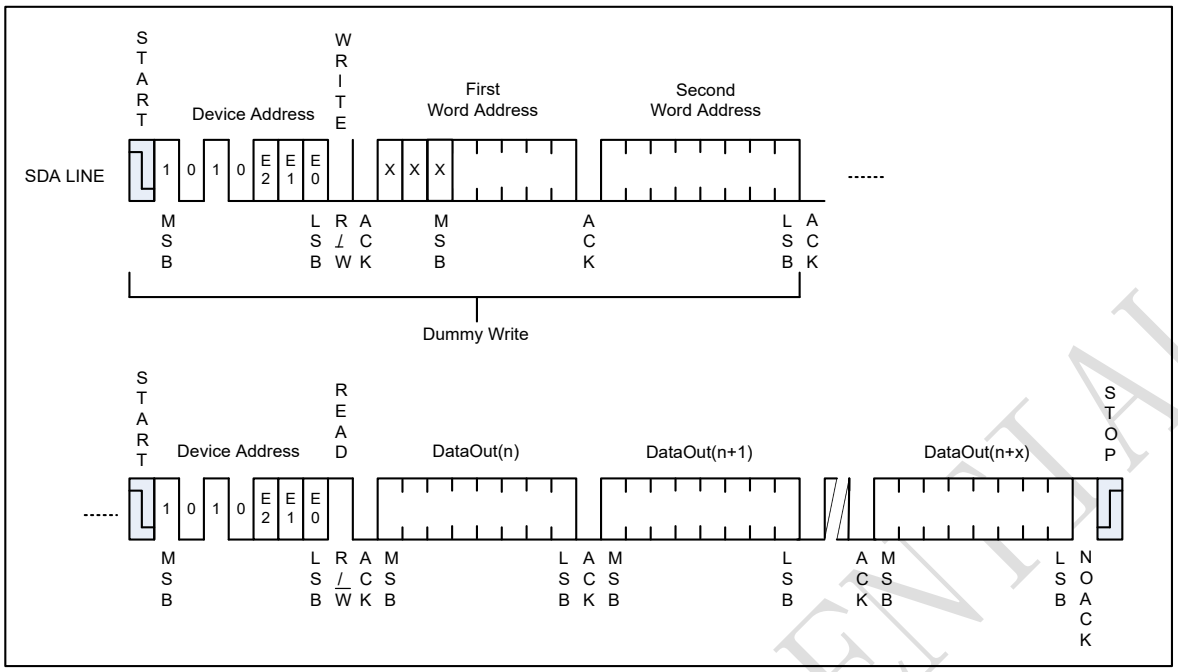
5.2.3 Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with acknowledge. As long as the P24C64C receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 5-5)

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Figure 5-5 Sequential Read



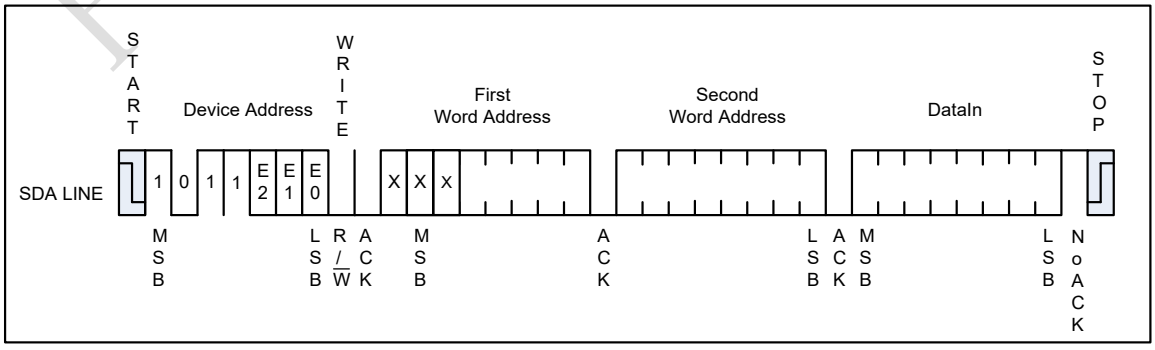
5.2.4 Read Identification Page

The Identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. The Identification Page can be read by Read Identification Page instruction which uses the same protocol and format as the Read Command (from memory array) with device type identifier defined as 1011b. The MSB address bits A12~A5 are don't care except for address bit A11~A10 which must be '00', the LSB address bits A4~A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g. when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 22, as the ID page boundary is 32 bytes).

5.2.5 Read the Lock Status

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NoACK bit if the Identification page is locked.

Figure 5-6 Lock Status Read (When Identification page locked, return NoACK after one data byte)



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5.2.6 Read Serial Number

Reading the serial number is similar to the sequential read sequence but requires use of the device address seen in Table 4-1, a dummy write, and the use of a specific word address. The entire 128 bits value must be read from the starting address of the serial number block to guarantee a unique number.

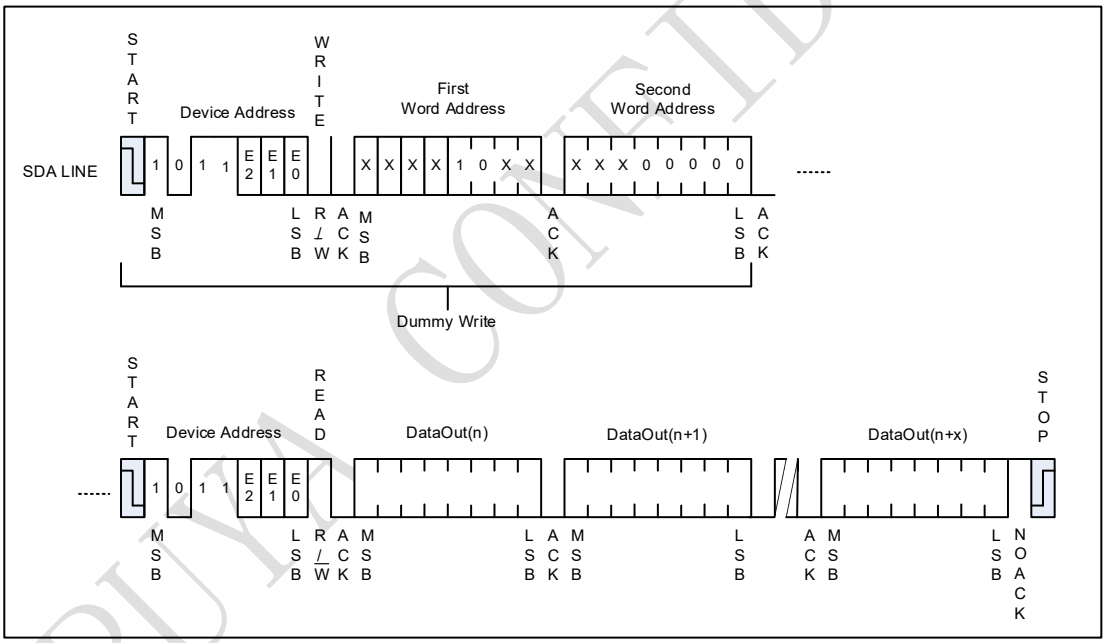
Since the address pointer of the device is shared between the regular EEPROM array and the serial number block, a dummy write sequence, as part of a Random Read or Sequential Read protocol, should be performed to ensure the address pointer is set to zero. A Current Address Read of the serial number block is supported but if the previous operation was to the EEPROM array, the address pointer will retain the last location accessed, incremented by one. Reading the serial number from a location other than the first address of the block will not result in a unique serial number.

Additionally, the word address contains a '10' sequence in bit A11 and A10 of the word address, regardless of the intended address as depicted in Table 4-2. If a word address other than '10' is used, then the device will output undefined data.

Example: If the application desires to read the first byte of the serial number, the word address input would need to be 0800h.

The Serial Number Read operation is terminated when the microcontroller does not respond with a zero (ACK) and instead issues a Stop condition (see Figure 5-7)

Figure 5-7 Serial Number Read



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6. Ordering Code Detail

Example: P 24C64C – SSH – MIT

Company Designator

P = Puya Semiconductor

Product Series Name

24C = I2C-compatible Interface EEPROM

Device Densitv

64 = 64K bits

Device Version

C = Version C

Package Option

DP: PDIP8
SS: SOP8
MS: MSOP8
TS: TSSOP8
UN: UDFN8
ST: SOT23-5
CS: WLCSP4

Plating Technology

H: RoHS Compliant, Halogen-free, Antimony- free

Operation Voltage

M: 1.7~5.5V
N: 1.8~5.5V
D: 2.5~5.5V

Device Grade

I: -40~85C
K: -40~105C
E: -40~125C

Shipping Carrier Option

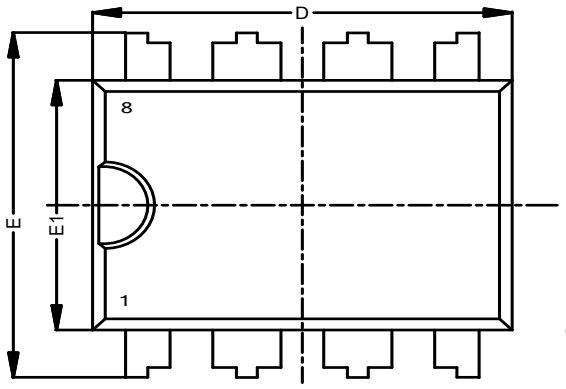
W: WAFER
T: TUBE
R: TAPE & REEL

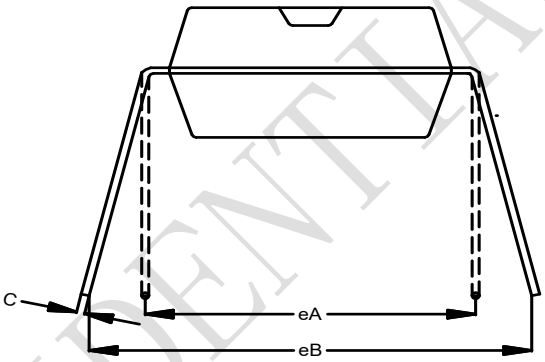
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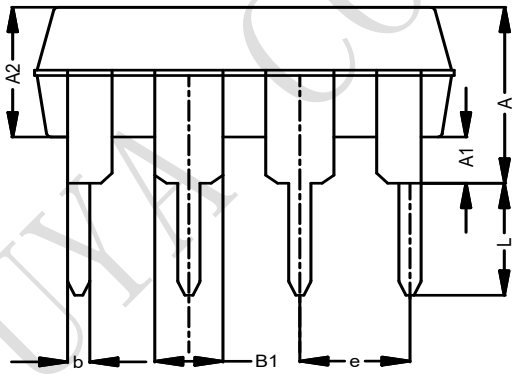
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7. Package Information

7.1 PDIP8







Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	3.600	-	5.330
A1	0.380	-	-
A2	2.920	3.300	4.950
b	0.360	-	0.570
B1	1.140	1.520	1.780
c	0.200	0.250	0.360
D	9.000	-	10.000
E	7.320	-	8.260
E1	6.100	6.350	6.600
e	0.400	-	0.700
eA	7.62REF		
eB	-	-	10.920
L	2.920	-	3.810

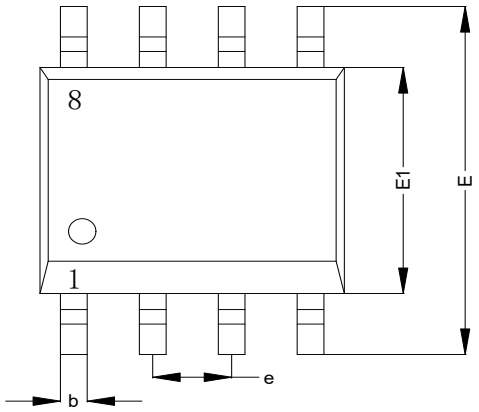
Note£ ¶. Dimensions are not to scale

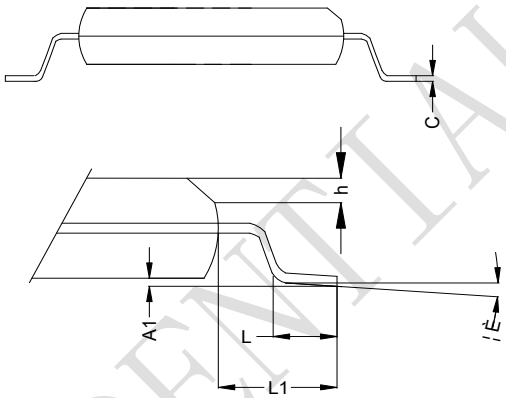
	TITLE	DRAWING NO.	REV
PUYA	Puya PDIP8 POD	QRPD-0021	1.1

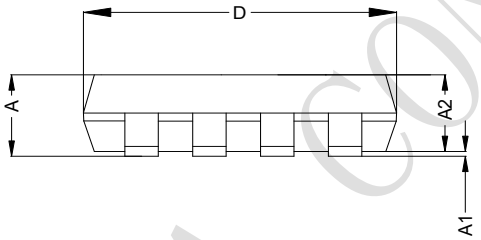
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7.2 SOP8(150mil)







Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	1.350	-	1.750
A1	0.100	-	0.250
A2	1.250	-	-
b	0.310	-	0.510
c	0.170	-	0.250
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
e	-	1.270	-
L	0.400	-	1.270
L1	-	1.050	-
¦È	0	-	8¡ã
h	0.25	-	0.50

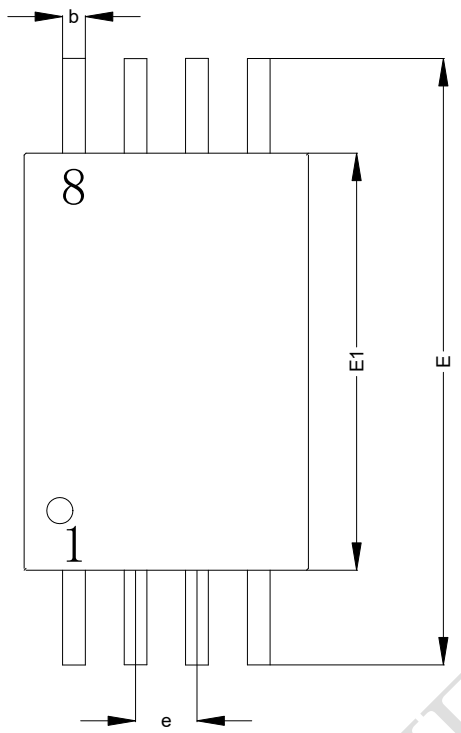
Note：1. Dimensions are not to scale

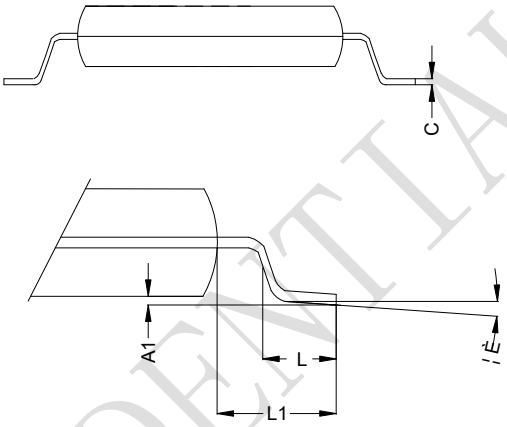
	TITLE	DRAWING NO.	REV
PUYA	Puya SOP8（150mil）POD	QRPD-0004	1.1

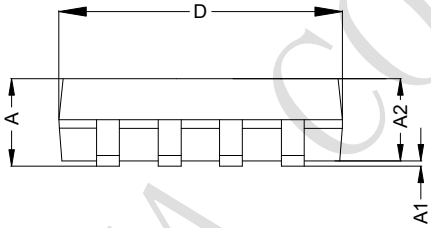
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7.3 TSSOP8







Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	1.000	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	2.900	3.000	3.100
E	6.200	6.400	6.600
E1	4.300	4.400	4.500
e	-	0.650	-
L	0.450	-	0.750
L1	-	1.000	-
¦È	0	-	8¡ã

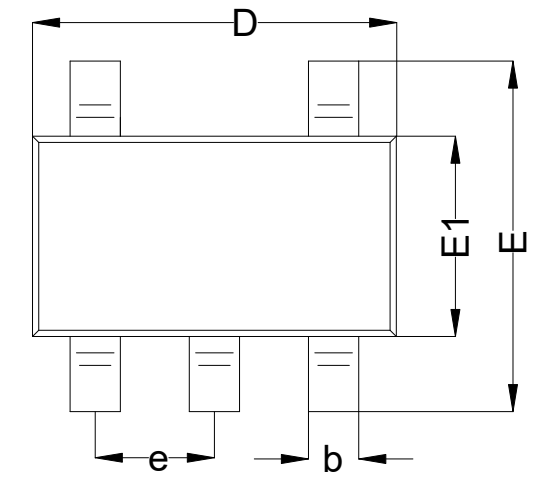
Note：1. Dimensions are not to scale

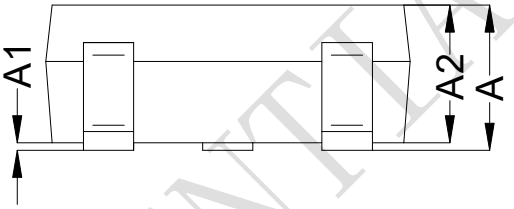
	TITLE	DRAWING NO.	REV
PUYA	PUYA TSSOP8 POD	QRPD-0019	1.1

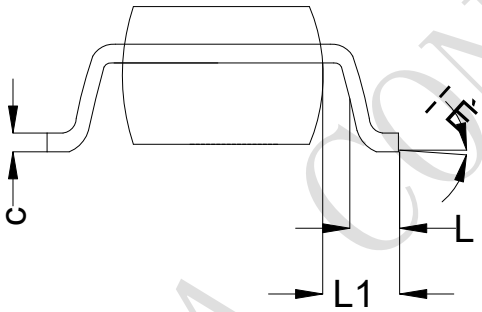
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7.4 SOT23-5







Common Dimensions

(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	1.050	-	1.250
A1	0.000	-	0.130
A2	1.000	1.100	1.200
b	0.270	-	0.500
c	0.100	-	0.230
D	2.820	2.920	3.020
E	2.600	2.800	3.000
E1	1.500	1.600	1.700
e	0.950BSC		
L	0.300	-	0.600
L1	0.600REF		
¦È	0	-	8¡ã

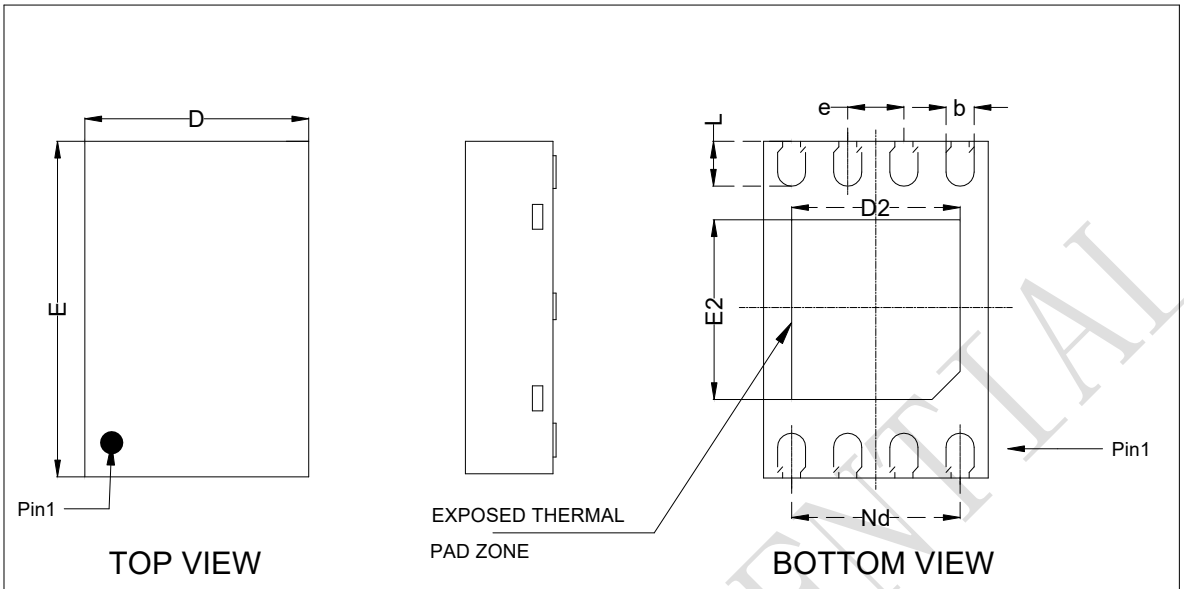
Note： Dimensions are not to scale

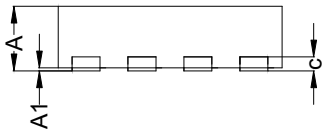
	TITLE	Drawing No.	REV
PUYA	Puya SOT23-5 POD	QRPD-0026	1.0

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7.5 UDFN8





SIDE VIEW

Common Dimensions

(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	1.90	2.00	2.10
D2	1.40	1.50	1.60
E	2.90	3.00	3.10
E2	1.50	1.60	1.70
e	0.50BSC		
L	0.30	0.40	0.50
c	0.10	0.15	0.20
Nd	1.50BSC		

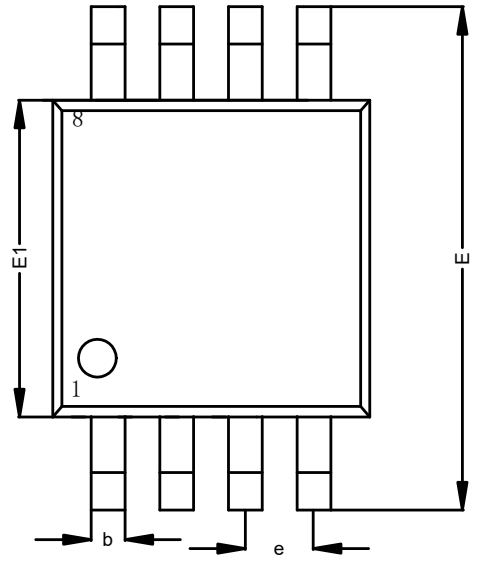
Note：1. Dimensions are not to scale

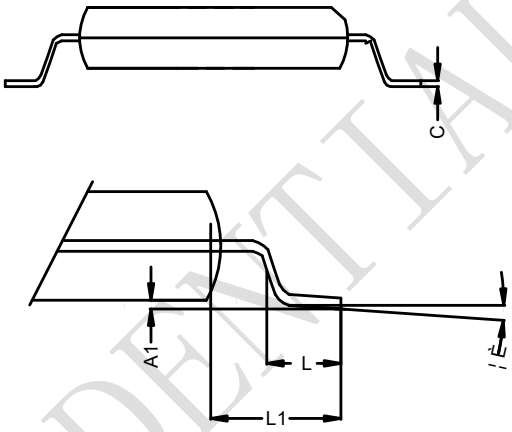
	TITLE	DRAWING NO.	REV
PUYA	Puya DFN8L 2x3X0.5-0.5PITCH POD	QRPD-0023	1.0

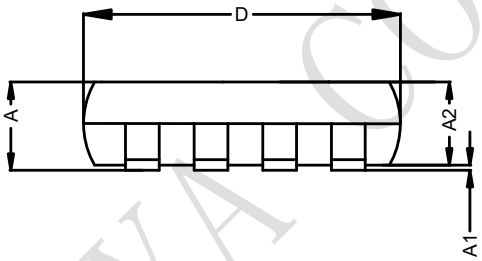
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7.6 MSOP8







Common Dimensions

(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	-	-	1.100
A1	0.050	-	0.150
A2	0.750	0.850	0.950
b	0.280	-	0.370
c	0.150	-	0.200
D	2.900	3.000	3.100
E	4.700	4.900	5.100
E1	2.900	3.000	3.100
e	-	0.650	-
L	0.400	-	0.800
L1	-	0.950	-
¦È	0	-	8¡ã

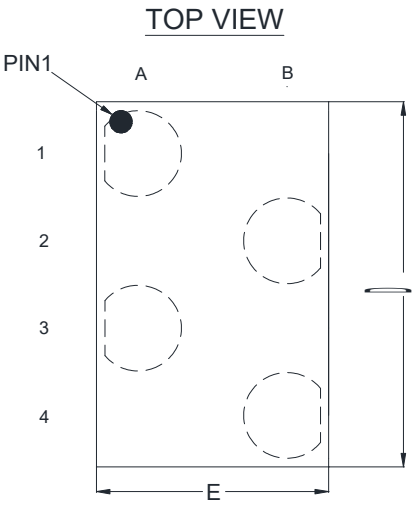
Note：1. Dimensions are not to scale

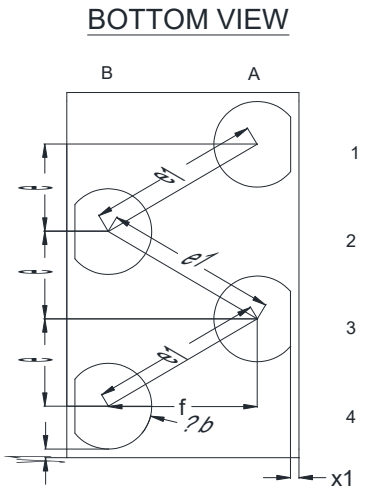
	TITLE	DRAWING NO.	REV
PUYA	Puya MSOP8 POD	QRPD-0020	1.0

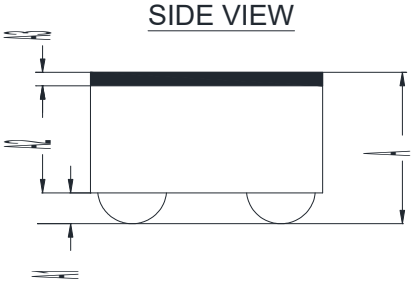
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7.7 WLCSP4 (Ball Pitch 320um*320um)







	1	2	3	4
A	VCC		SDA	
B		SCL		GND

NOTE: 1.Dimensions are NOT to scale.
2.Solder ball composition is SnAg.
3.Product offered with Back Side Coating(BSC)

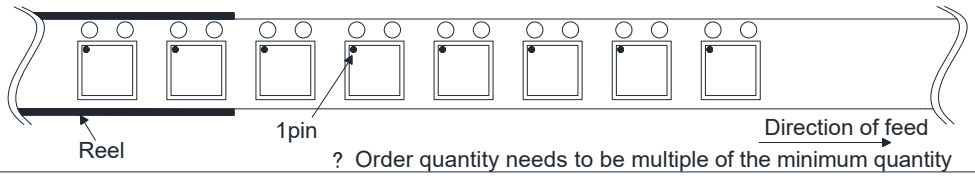
(Unit of Measure =mm)

SYMBOL	MIN	TYP	MAX	NOTE
A	0.255	0.280	0.305	
A1	0.050	0.055	0.060	
A2	0.180	0.200	0.220	
A3		0.025BSC		
D	0.692	0.722	0.752	
e	-	0.163	-	
y1		0.036REF		
E	0.439	0.469	0.499	
e1	-	0.320	-	
x1		0.035REF		
b	-	0.160	-	
f	-	0.275	-	

	TITLE	DRAWING NO.	REV
PUYA	4-ball,2x2 Array,0.163/0.320mm pitch Wafer Level Chip ScalePackage with BSC	SS-4	A

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



? Order quantity needs to be multiple of the minimum quantity

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8. Revision History

Version	Content	Date
V1.0	Initial Release	2016-05-31
V1.1	Add UDFN Package information	2016-09-13
V1.2	Correct P24C32C to P24C64C	2018-06-06
V1.3	Add package MSOP8	2019-05-07
V1.4	Update package SOT23-5	2020-04-23
V1.5	AC timing for 100KHz added	2020-05-15
V1.6	WLCSP package added	2020-12-28
V1.7	(1) Add Table 3-1 (2) Update Table 3-5 and Figure 3-1 (3) Delete 'Device Selection Table' of 'General Description'	2021-06-30
V1.8	Add 'Device Power-Up' and 'Power Up/Down and Voltage Drop'	2021-09-06
V1.9	(1) Update 'Ordering Code Detail' (2) Update '100kHz AC Characteristics'	2022-03-10
V2.0	Update t_{DH} of '100kHz AC Characteristics'	2022-07-05
V2.1	Update parameter of V_{IL}	2023-01-16
V2.2	Modify GND to Vss	2024-07-09
V2.3	(1) Update PDIP8 POD (2) Update SOP8(150mil) POD (3) Update TSSOP8 POD (4) Update SOT23-5 POD (5) Update feature description (6) Update I_{CC1} and I_{CC2} of DC Characteristics	2025-04-25

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