# P24C256B

## I²C-Compatible Serial E²PROM

**Datasheet V2.0**

## General Description

The P24C256B is I²C-compatible Serial EEPROM (Electrically Erasable Programmable Memory) device. It contains a memory array of 256 Kbits (32 Kbytes), which is organized in 64 bytes per page.

## Features

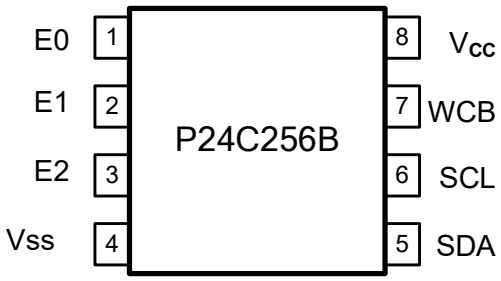
- Single Supply Voltage and High Speed Mode
  - Minimum operating voltage down to 1.7 V
  - 400 kHz/1 MHz clock from 1.7 V to 5.5 V
- Low power CMOS technology
  - Read current 0.2 mA (400 kHz, typical)
  - Write current 0.8 mA (400 kHz, typical)
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Sequential & Random Read Features
- 64 bytes Page Write Modes, Partial Page Writes Allowed
- Write protect of the whole memory array
- Additional Write Lockable Page
- Self-timed Write Cycle (5 ms maximum)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - HBM: 6 kV
  - Latch up Capability: +/- 200 mA (25 C)
- Package: PDIP8, SOP8(150mil), MSOP8, TSSOP8, DFN8, UDFN8, SOT23-5

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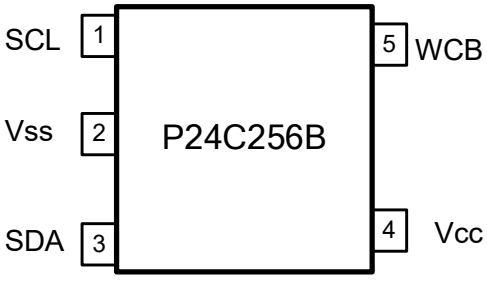
# 1. Pin Configuration

## 1.1 Pin Configuration

**Figure 1-1 Pin Configuration**




**PDIP8/SOP8(150mil)/MSOP8/TSSOP8/DFN8/UDFN8**




**SOT23-5**

## 1.2 Pin Definition

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**Table 1-1 Pin Definition**

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | E0 | Input | Slave Address Setting |
| 2 | E1 | Input | Slave Address Setting |
| 3 | E2 | Input | Slave Address Setting |
| 4 | Vss | Ground | Ground |
| 5 | SDA | I/O | Serial Data Input and Serial Data Output |
| 6 | SCL | Input | Serial Clock Input |
| 7 | WCB | Input | Write Control, Low Enable Write |
| 8 | $V_{CC}$ | Power | Power |

**Table 1-2 Pin Definition for SOT23-5 Packages**

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | SCL | Input | Serial Clock Input |
| 2 | Vss | Ground | Ground |
| 3 | SDA | I/O | Serial Data Input and Serial Data Output |
| 4 | $V_{CC}$ | Power | Power |
| 5 | WCB | Input | Write Control, Low Enable Write |



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## 1.3 Pin Descriptions

**Serial Clock (SCL):** The SCL input is used to positive-edge clock data in and negative-edge clock data out of each device.

**Serial Data (SDA):** The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wire-OR'ed with any number of other open-drain or open-collector devices.

**Device Addresses (E2, E1, E0):** The E2, E1, and E0 pins are device address inputs. Typically, the E2, E1, and E0 pins are for hardware addressing and a total of 8 devices can be connected on a single bus system. If these pins are left floating, the E2, E1, and E0 pins will be internally pulled down to Vss.

**Write Control (WCB):** The Write Control input, when WCB is connected directly to $V_{CC}$, all write operations to the memory are inhibited. When connected to Vss, allows normal write operations. If the pin is left floating, the WCB pin will be internally pulled down to Vss.

**Supply Voltage($V_{CC}$):** $V_{CC}$ is the supply voltage.

**Ground(Vss):** Vss is the reference for the $V_{CC}$ supply voltage.

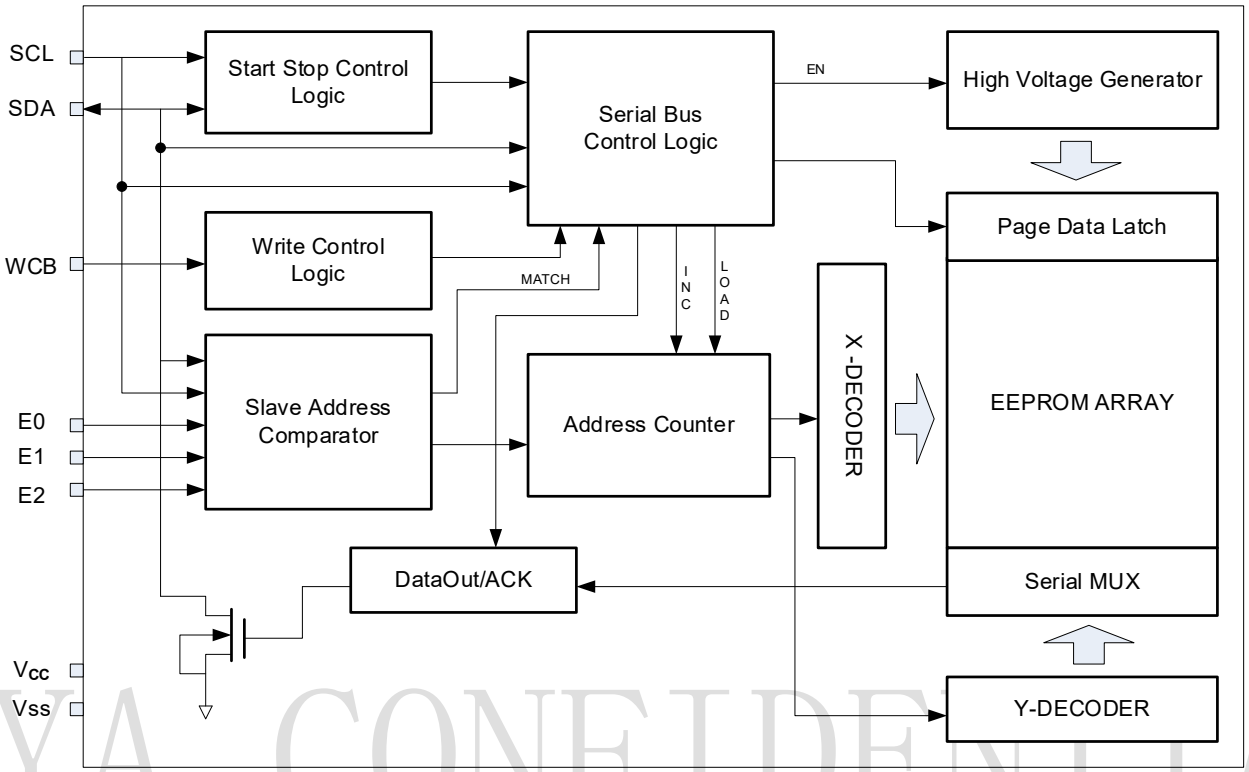
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# 2. Block Diagram

**Figure 2-1 Block Diagram**




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# 3. Electrical Characteristics

**Table 3-1 Absolute Maximum Ratings [1]**

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $T_{STG}$ | Storage Temperature | -65 | 150 | °C |
| $T_A$ | Ambient operating temperature | -40 | 125 | °C |
| $V_{CC}$ | Supply Voltage | -0.5 | 6.5 | V |
| $V_{IO}$ | Input or output range | -0.5 | 6.5 | V |
| $I_{OL}$ | DC output current (SDA=0) | - | 5 | mA |

Note: [1] Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 3-2 Pin Capacitance [1]**

| Symbol | Parameter | Max. | Units | Test Condition |
|---|---|---|---|---|
| $C_{I/O}$ | Input/Output Capacitance (SDA) | 8 | pF | $V_{I/O}$=Vss |
| $C_{IN}$ | Input Capacitance (E0,E1,E2,WCB,SCL) | 6 | pF | $V_{IN}$=Vss |

Note: [1] Test Conditions: $T_A$ = 25°C, $f_{SCL}$ = 1MHz, Vcc = 5.0V.

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**Table 3-3 DC Characteristics** (Unless otherwise specified, $V_{CC}$ = 1.7V to 5.5V, $T_A$ = –40°C to 125°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 1.7 | - | 5.5 | V | |
| | | 1.8 | - | 5.5 | V | |
| | | 2.5 | - | 5.5 | V | |
| Isb | Standby Current (Standby mode) | - | 0.7 | 3.0 | uA | Vcc = 5.5V, $T_A$ = 85°C |
| | | - | - | 6.0 | uA | Vcc = 5.5V, $T_A$ = 105°C |
| | | - | - | 10.0 | uA | Vcc = 5.5V, $T_A$ = 125°C |
| $I_{CC1}$ | Supply Current(Read) | - | 0.2 | 0.4 | mA | Vcc=5.5V, $f_{SCL}$ = 400KHz |
| $I_{CC2}$ | Supply Current(Write) | - | 0.8 | 1.6 | mA | Vcc=5.5V, $f_{SCL}$ = 400KHz |
| $I_{LI}$ | Input Leakage Current | - | 0.1 | 1.0 | μA | $V_{IN}$ = $V_{CC}$ or Vss |
| $I_{LO}$ | Output Leakage Current | - | 0.05 | 1.0 | μA | $V_{OUT}$ = $V_{CC}$ or Vss |
| $V_{IL}$ | Input Low Level | –0.5 | - | 0.3$V_{CC}$ | V | |
| $V_{IH}$ | Input High Level | 0.7$V_{CC}$ | - | $V_{CC}$+0.5 | V | |
| $V_{OL1}$ | Output Low Level $V_{CC}$ = 1.7V (SDA) | - | - | 0.2 | V | $I_{OL}$ = 0.15 mA |
| $V_{OL2}$ | Output Low Level $V_{CC}$ = 3.0V (SDA) | - | - | 0.4 | V | $I_{OL}$ = 2.1 mA |



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**Table 3-4 AC Characteristics**（Unless otherwise specified, $V_{CC}$ = 1.7V to 5.5V, $T_A$ = –40°C to 125°C, $C_L$=100pF, Test Conditions are listed in Notes [2] ）

| Symbol | Parameter | 1.7≤$V_{CC}$≤5.5 | | | 1.7≤$V_{CC}$≤5.5 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $f_{SCL}$ | Clock Frequency, SCL | - | - | 400 | - | - | 1000 | kHz |
| $t_{LOW}$ | Clock Pulse Width Low | 1.3 | - | - | 0.4 | - | - | μs |
| $t_{HIGH}$ | Clock Pulse Width High | 0.6 | - | - | 0.4 | - | - | μs |
| $t_{AA}$ | Clock Low to Data Out Valid | 0.05 | - | 0.9 | 0.05 | - | 0.55 | μs |
| $t_I$ | Noise Suppression Time | - | - | 0.1 | - | - | 0.05 | μs |
| $t_{BUF}$ | Time the bus must be free before a new transmission can start | 1.3 | - | - | 0.5 | - | - | μs |
| $t_{HD.STA}$ | Start Hold Time | 0.6 | - | - | 0.25 | - | - | μs |
| $t_{SU.STA}$ | Start Setup Time | 0.6 | - | - | 0.25 | - | - | μs |
| $t_{HD.DAT}$ | Data In Hold Time | 0 | - | - | 0 | - | - | μs |
| $t_{SU.DAT}$ | Data In Setup Time | 0.1 | - | - | 0.1 | - | - | μs |
| $t_R$ | Inputs Rise Time[1] | - | - | 0.3 | - | - | 0.3 | μs |
| $t_F$ | Inputs Fall Time[1] | - | - | 0.3 | - | - | 0.1 | μs |
| $t_{SU.STO}$ | Stop Setup Time | 0.6 | - | - | 0.25 | - | - | μs |
| $t_{DH}$ | Data Out Hold Time | 0.05 | - | - | 0.05 | - | - | μs |
| $t_{SU.WCB}$ | WCB pin Setup Time | 1.2 | - | - | 0.6 | - | - | μs |
| $t_{HD.WCB}$ | WCB pin Hold Time | 1.2 | - | - | 0.6 | - | - | μs |
| $t_{WR}$ | Write Cycle Time | - | - | 5 | - | - | 5 | ms |

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Notes: [1] This parameter is ensured by characterization not 100% tested

[2] AC measurement conditions:

- $R_L$ (connects to $V_{CC}$): 1.3k (2.5V, 5.5V), 10k (1.7V)
- Input pulse voltages: 0.3 $V_{CC}$ to 0.7 $V_{CC}$
- Input rise and fall times: ≤50ns
- Input and output timing reference voltages: 0.5$V_{CC}$

**Table 3-5 Reliability Characteristic [1]**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **EDR [2]** | Endurance | 1,000,000 | | | Write cycles |
| **DRET[3]** | Data retention | 100 | | | Years |

Note: [1] This parameter is ensured by characterization and is not 100% tested

[2] Under the condition: 25°C, 3.3V, Page mode

[3] Test condition: $T_A$ = 55°C



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**Figure 3-1 Bus Timing**

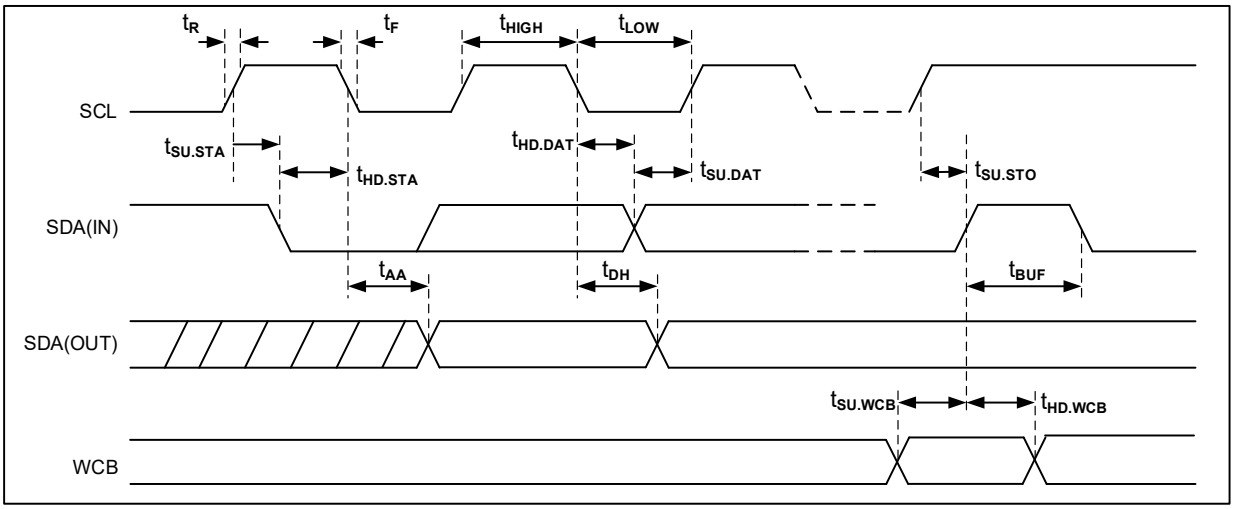
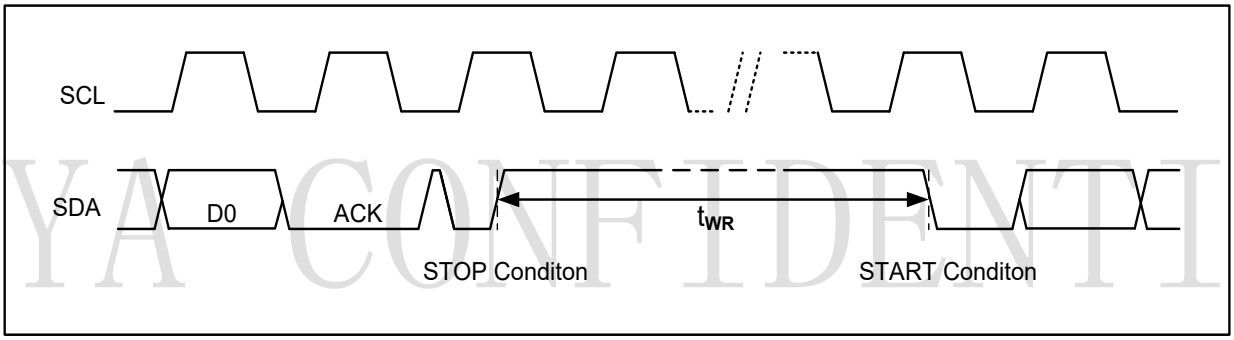



**Figure 3-2 Write Cycle Timing**




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Note: [1] The write cycle time $t_{WR}$ is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

**Device Power-Up**

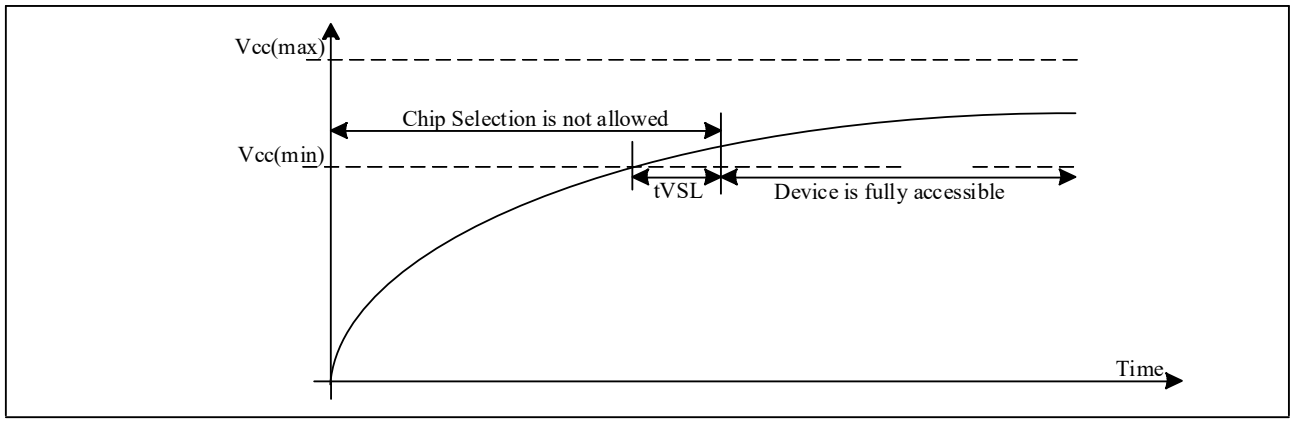
The EEPROM has a built-in power-on-reset circuit that initializes itself at the same time during power-on. Unsuccessful initialization may cause a malfunction. To operate the power-on-reset circuit normally, the following conditions must be satisfied to raise the power supply voltage.

When initialization is successfully completed by the power-on-reset circuit, the EEPROM enters the standby status. tVSL is the time required to initialize the EEPROM. No instructions are accepted during this time.



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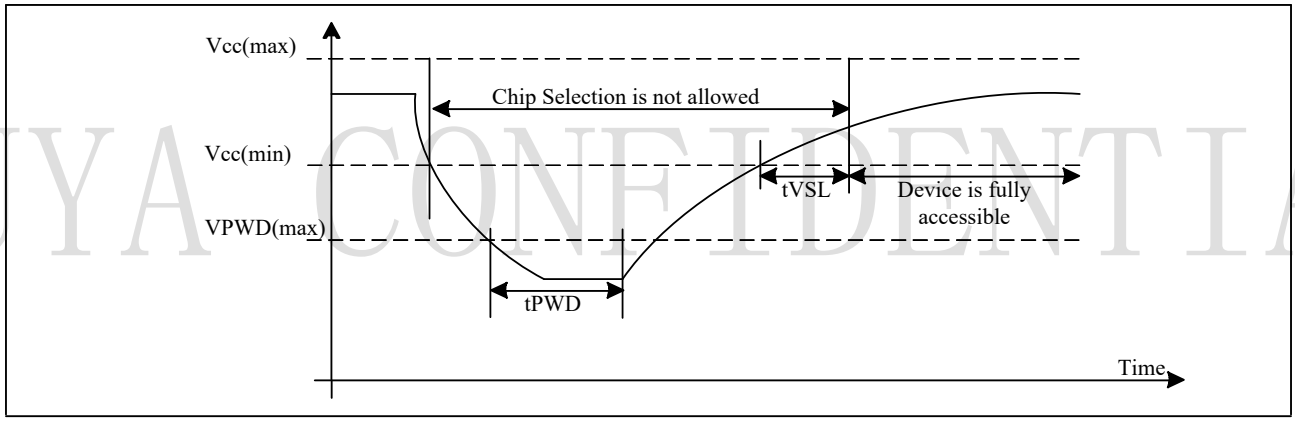
**Figure 3-3 Power up Timing**




**Power Up/Down and Voltage Drop**

For Power-down to Power-up operation, the VCC of EEPROM device must below VPWD for at least tPWD timing. Please check the table below for more detail.

**Figure 3-4 Power down-up Timing**




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| Symbol | Parameter | min | max | unit |
|---|---|---|---|---|
| VPWD | VCC voltage needed to below VPWD for ensuring initialization will occur | | 0.7 | V |
| tPWD | The minimum duration for ensuring initialization will occur | 300 | | us |
| tVSL | VCC(min.) to device operation | 70 | | us |
| tVR | VCC Rise Time | 1 | 500000 | us/V |



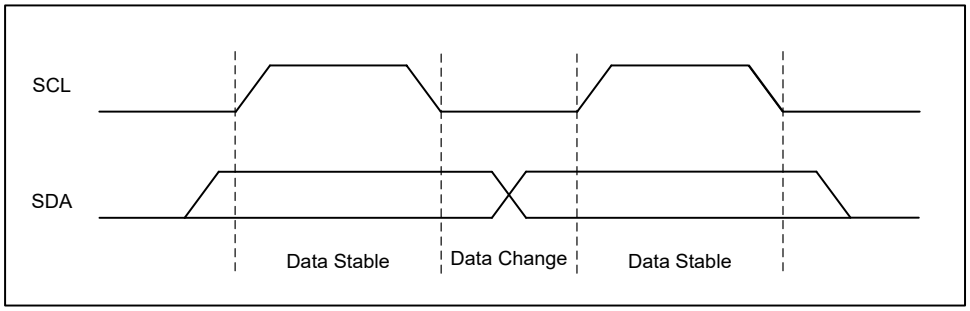
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# 4. Device Operation

## 4.1 Data Input

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 4-1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

**Figure 4-1 Data Validity**




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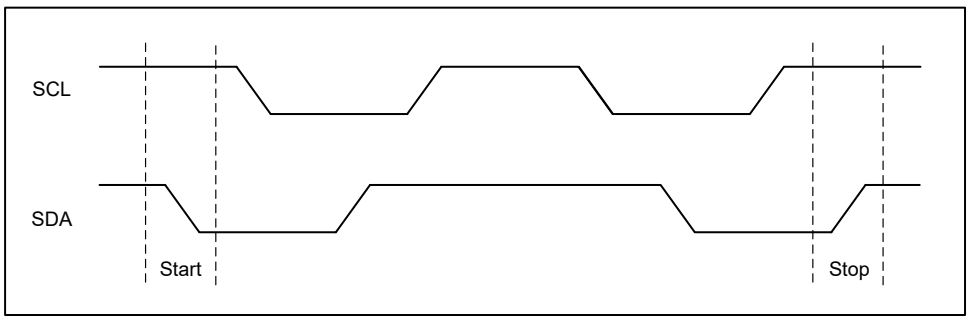
## 4.2 Start Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 4-2).

## 4.3 Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the P24C256B in a standby mode (see Figure 4-2).

**Figure 4-2 Start and Stop Definition**



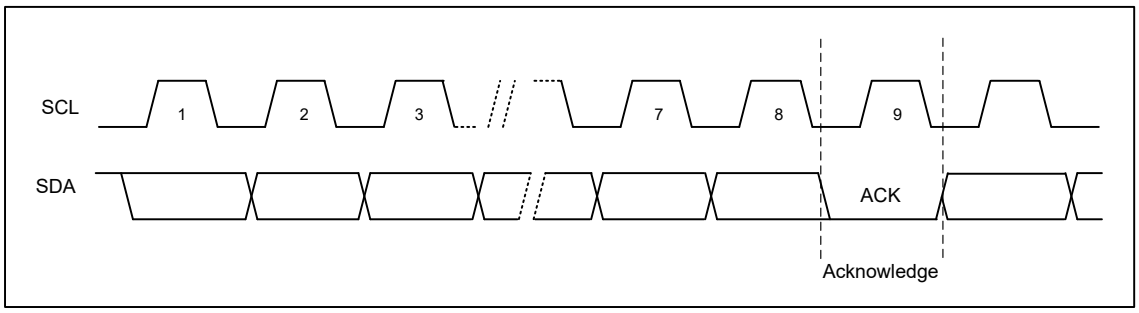



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## 4.4 Acknowledge (ACK)

All addresses and data words are serially transmitted to and from the P24C256B in 8-bit words. The P24C256B sends a “0” to acknowledge that it has received each word. This happens during the ninth clock cycle.

**Figure 4-3 Output Acknowledge**




## 4.5 Standby Mode

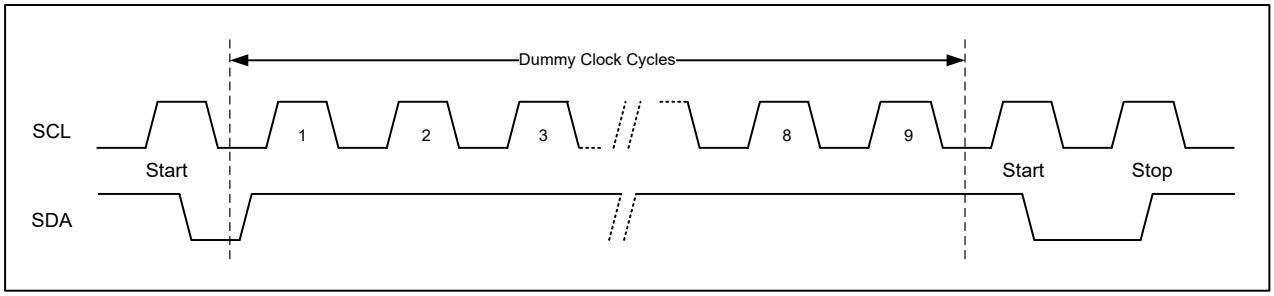
The P24C256B features a low-power standby mode which is enabled: (a) after a fresh power up, (b) after receiving a STOP bit in read mode, and (c) after completing a self-time internal programming operation

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## 4.6 Soft Reset

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps: (a) Create a start condition, (b) Clock nine cycles, and (c) create another start bit followed by stop bit condition, as shown below. The device is ready for the next communication after the above steps have been completed.

**Figure 4-4 Soft Reset**



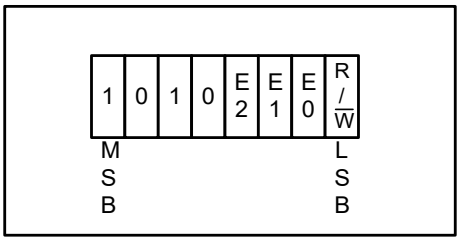



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## 4.7 Device Addressing

The P24C256B requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure4-5). The device address word consists of a mandatory one-zero sequence for the first four most-significant bits, as shown.

**Figure 4-5 Device Address**




The three E2, E1, and E0 device address bits allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins.
The E2, E1, and E0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are floating.
The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a compare of the device address, the Chip will output a zero. If a compare is not made, the device will return to a standby state.

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## 4.8 Data Security

P24C256B has a hardware data protection scheme that allows the user to write protect the whole memory when the WCB pin is at Vcc.



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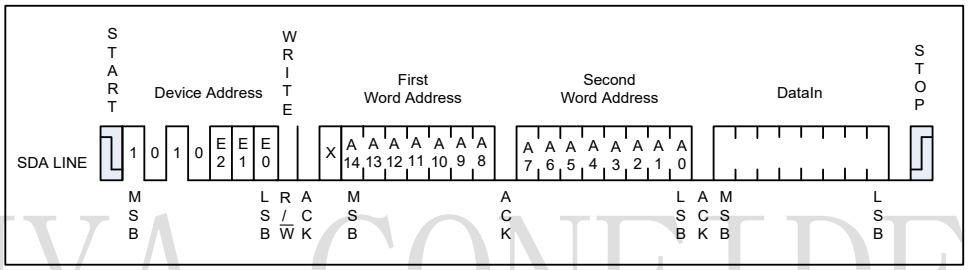
# 5. Instructions

## 5.1 Write Operations

### 5.1.1 Byte Write

A write operation requires two 8-bit data word address (A14~A0) following the device address word and acknowledgment. Upon receipt of this address, the P24C256B will again respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the P24C256B will output a “0” and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. And then the P24C256B enters an internally timed write cycle, all inputs are disabled during this write cycle and the P24C256B will not respond until the write is complete (see Figure 5-1).

**Figure 5-1 Byte Write**



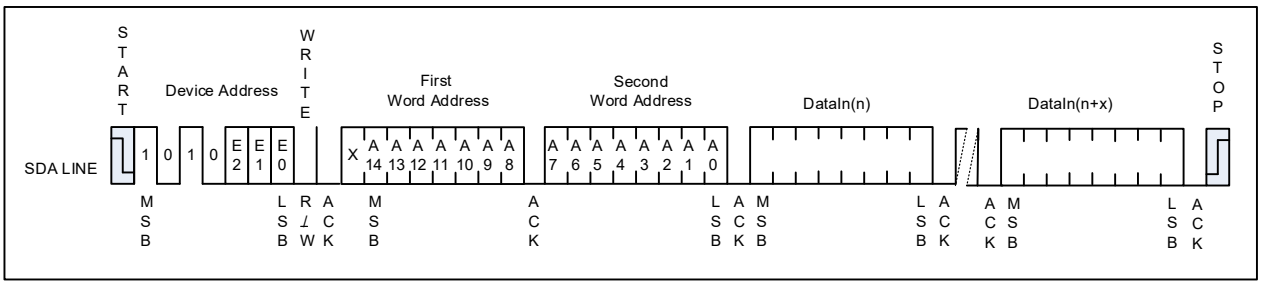

Notes: [1] x means don’t care.

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### 5.1.2 Page Write

A page write is initiated the same as a byte write, but the master does not send a stop condition after the first data word is clocked in. Instead, after the P24C256B acknowledges receipt of the first data word, the master can transmit more data words. The P24C256B will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition.

**Figure 5-2 Page Write**




The lower six bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64 data words are transmitted to the P24C256B, the data word address will roll-over, and previous data will be overwritten. The address roll-over during write is from the last



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byte of the current page to the first byte of the same page.

#### 5.1.3 Acknowledge Polling

Once the internally timed write cycle has started and the P24C256B inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the P24C256B respond with a “0”, allowing the read or write sequence to continue.

#### 5.1.4 Write Identification Page

The Identification Page (64 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier = 1011b
- MSB address bits A14~A6 are don’t care except for address bit A10 which must be ‘0’.

LSB address bits A5~A0 define the byte address inside the Identification page. If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoACK).

#### 5.1.5 Lock Identification Page

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

- Device type identifier = 1011b
- Address bit A10 must be ‘1’; all other address bits are don’t care
- The data byte must be equal to the binary value xxxx xx1x, where x is don’t care

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### 5.2 Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to “1”. There are three read operations: Current Address Read; Random Address Read and Sequential Read.

#### 5.2.1 Current Address Read

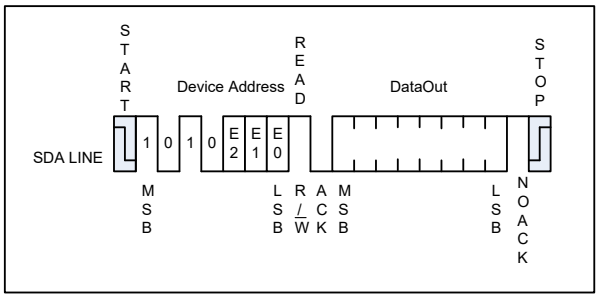
The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to “1” is clocked in and acknowledged by the P24C256B, the current address data word is serially clocked out. The microcontroller does not respond with an input “0” but does generate a following stop condition (see Figure 5-3).



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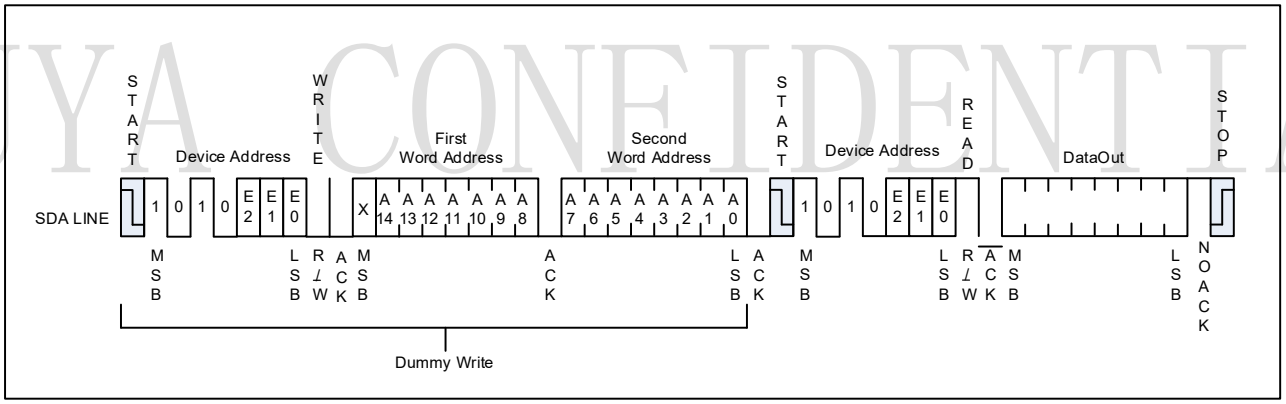
**Figure 5-3 Current Address Read**




### 5.2.2 Random Read

A Random Read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the P24C256B, the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The P24C256B acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 5-4).

**Figure 5-4 Random Read**




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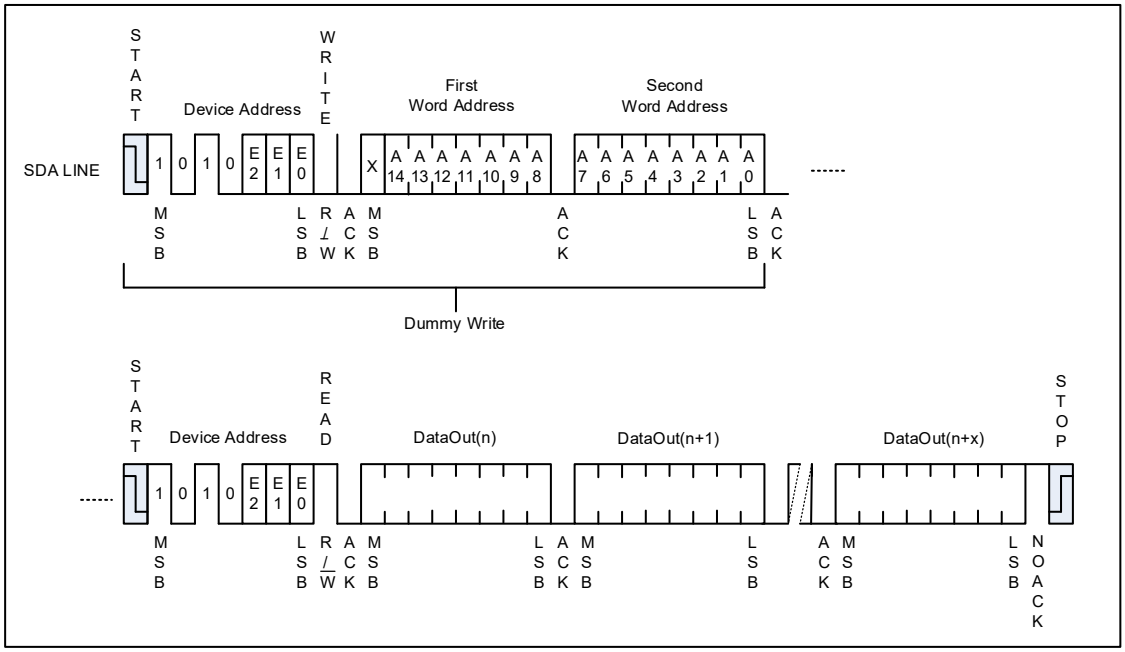
### 5.2.3 Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with acknowledge. As long as the P24C256B receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 5-5)



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**Figure 5-5 Sequential Read**




### 5.2.4 Read Identification Page

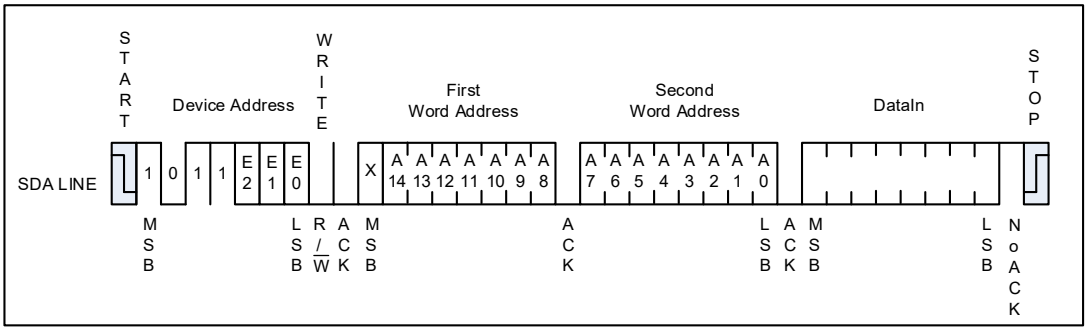
The Identification Page (64 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. The Identification Page can be read by Read Identification Page instruction which uses the same protocol and format as the Read Command (from memory array) with device type identifier defined as 1011b. The MSB address bits A14~A6 are don't care, the LSB address bits A5~A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g. when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 54, as the ID page boundary is 64 bytes).

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### 5.2.5 Read Lock Status

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NoACK bit if the Identification page is locked.

**Figure 5-6 Lock Status Read (When Identification page locked, return NoACK after one data byte)**






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# 6. Ordering Code Detail

Example: P 2 4 C 256 B – S S H – M I T

**Company Designator**

P = Puya Semiconductor

**Product Series Name**

24C = I2C-compatible Interface EEPROM

**Device Densitv**

256 =256K bits

**Device Version**

B = Version B

**Package Option**

| | |
|---|---|
| DP: PDIP8 | SS: SOP8(150mil) |
| MS: MSOP8 | TS: TSSOP8 |
| DN: DFN8 | UN: UDFN8 |
| WF: WAFER | ST: SOT23-5 |

PU DENTIAL

**Plating Technology**

H: RoHS Compliant, Halogen-free, Antimony-free

**Operation Voltage**

M: 1.7~5.5V

N: 1.8~5.5V

D: 2.5~5.5V

**Device Grade**

I: -40~85C

K: -40~105C

E: -40~125C

**Shipping Carrier Option**

W: WAFER

T: TUBE

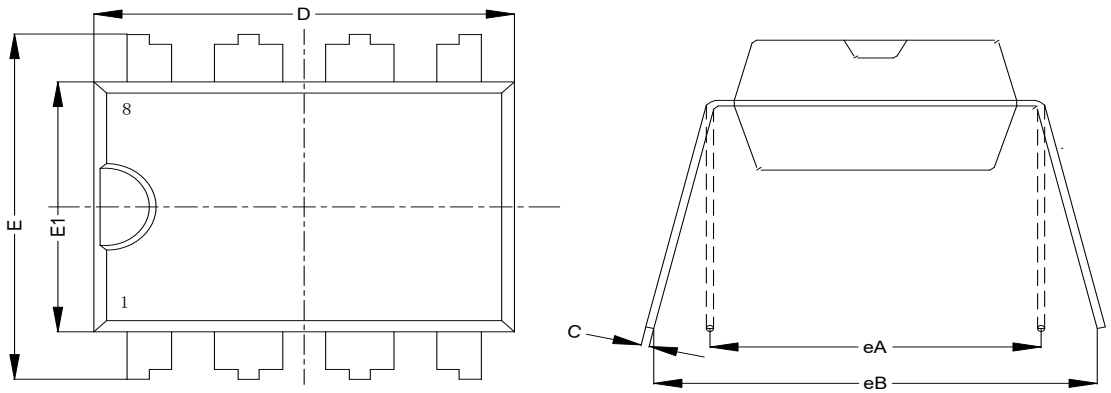
R: TAPE & REEL



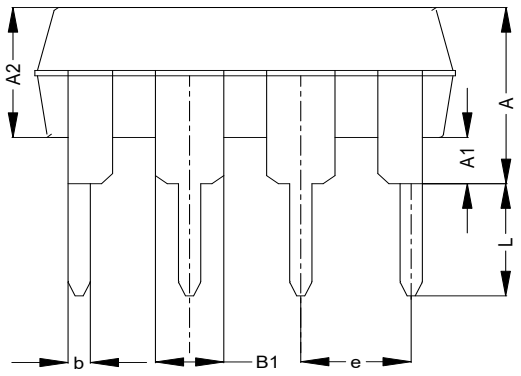
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# 7. Package Information

## 7.1 PDIP8




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Common Dimensions
(Unit of Measure=millimeters)

| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | 3.600 | - | 5.330 |
| A1 | 0.380 | - | - |
| A2 | 2.920 | 3.300 | 4.950 |
| b | 0.360 | - | 0.570 |
| B1 | 1.140 | 1.520 | 1.780 |
| c | 0.200 | 0.250 | 0.360 |
| D | 9.000 | - | 10.000 |
| E | 7.320 | - | 8.260 |
| E1 | 6.100 | 6.350 | 6.600 |
| e | 2.540BSC | | |
| eA | 7.620REF | | |
| eB | - | - | 10.920 |
| L | 2.920 | - | 3.810 |

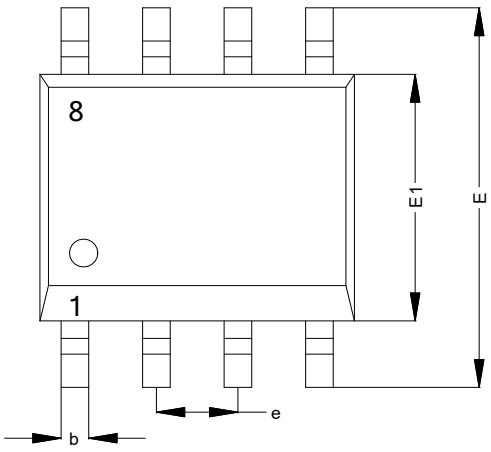
Note：1. Dimensions are not to scale

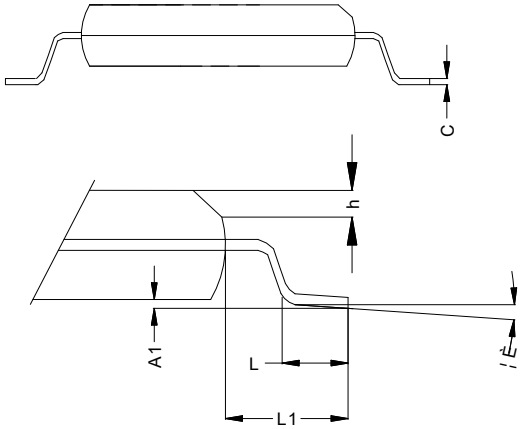
| | TITLE | DRAWING NO. | REV |
|---|---|---|---|
| PUYA | Puya PDIP8 POD | QRPD-0021 | 1.2 |



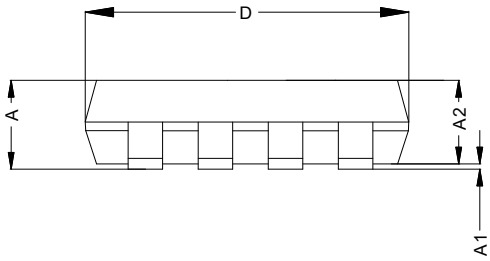
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## 7.2 SOP8(150mil)




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Common Dimensions
(Unit of Measure=millimeters)

| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | 1.350 | - | 1.750 |
| A1 | 0.100 | - | 0.250 |
| A2 | 1.250 | - | - |
| b | 0.310 | - | 0.510 |
| c | 0.170 | - | 0.250 |
| D | 4.800 | 4.900 | 5.000 |
| E | 5.800 | 6.000 | 6.200 |
| E1 | 3.800 | 3.900 | 4.000 |
| e | 1.270BSC | | |
| L | 0.400 | - | 0.900 |
| L1 | 1.050REF | | |
| ¦È | 0 | - | 8¡ã |
| h | 0.250 | - | 0.500 |

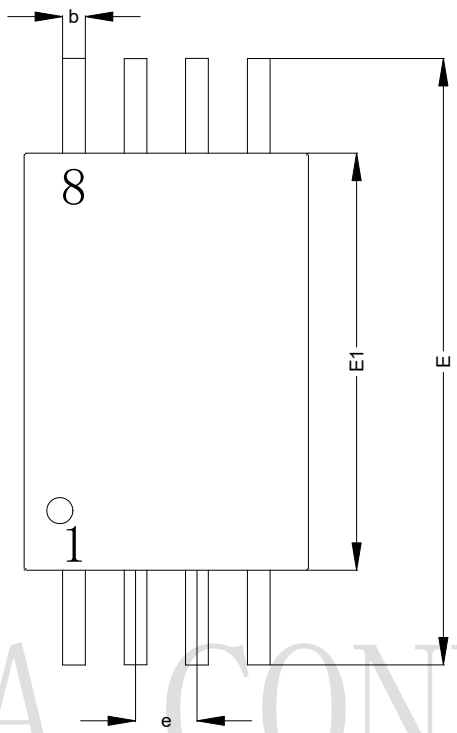
Note£ ¶1. Dimensions are not to scale

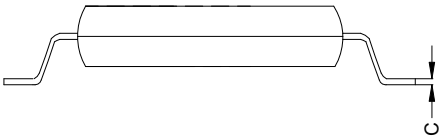
| | | | |
|---|---|---|---|
| PUYA | TITLE<br>Puya SOP8£ ¨150mil£ ©OD | DRAWING NO.<br>QRPD-0004 | REV<br>1.2 |

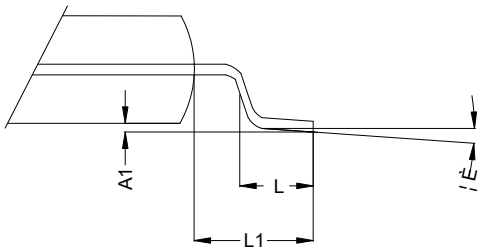


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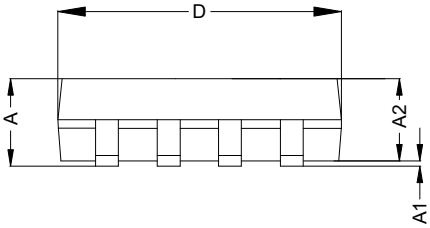
## 7.3 TSSOP8




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Common Dimensions
(Unit of Measure=millimeters)

| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | - | - | 1.200 |
| A1 | 0.050 | - | 0.150 |
| A2 | 0.800 | 1.000 | 1.050 |
| b | 0.190 | - | 0.300 |
| c | 0.090 | - | 0.200 |
| D | 2.900 | 3.000 | 3.100 |
| E | 6.200 | 6.400 | 6.600 |
| E1 | 4.300 | 4.400 | 4.500 |
| e | - | 0.650 | - |
| L | 0.450 | - | 0.750 |
| L1 | - | 1.000 | - |
| ¦È | 0 | - | 8¡ã |

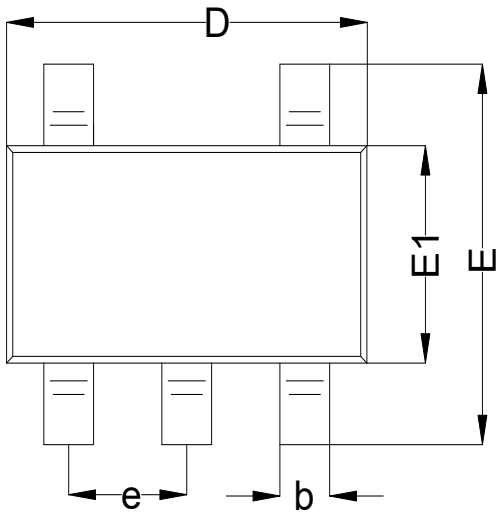
Note：1. Dimensions are not to scale

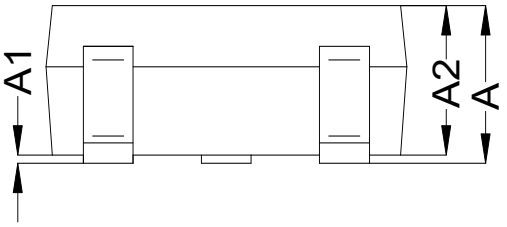
| | TITLE | DRAWING NO. | REV |
|---|---|---|---|
| PUYA | PUYA TSSOP8 POD | QRPD-0019 | 1.1 |



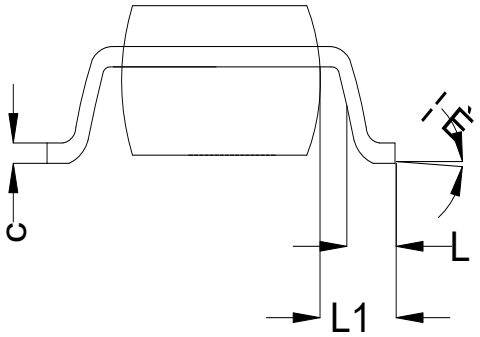
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### 7.4 SOT23-5




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Common Dimensions
(Unit of Measure=millimeters)

| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | 1.050 | - | 1.250 |
| A1 | 0.000 | - | 0.130 |
| A2 | 1.000 | 1.100 | 1.200 |
| b | 0.270 | - | 0.500 |
| c | 0.100 | - | 0.230 |
| D | 2.820 | 2.920 | 3.020 |
| E | 2.600 | 2.800 | 3.000 |
| E1 | 1.500 | 1.600 | 1.700 |
| e | 0.950BSC | | |
| L | 0.300 | - | 0.600 |
| L1 | 0.600REF | | |
| ¦È | 0 | - | 8¡ã |

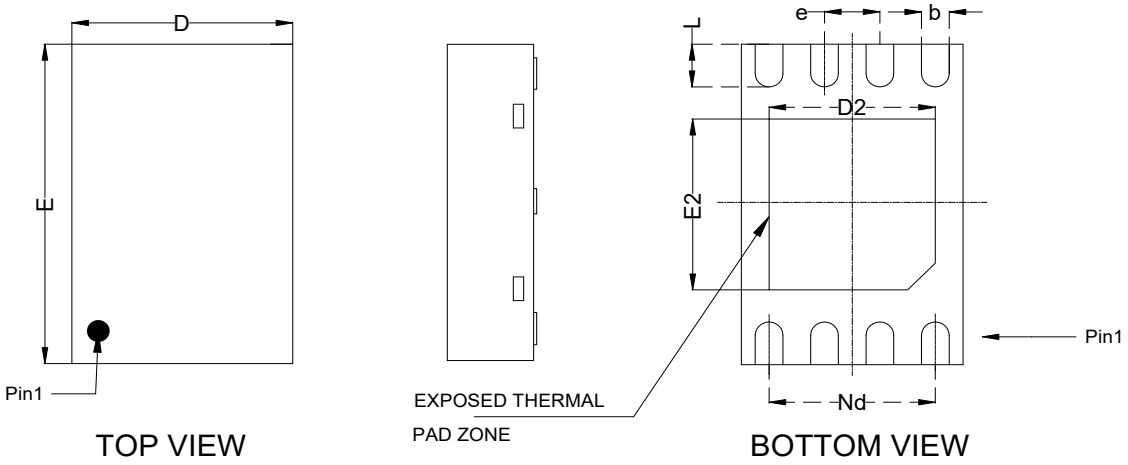
Note： Dimensions are not to scale

| | TITLE | Drawing No. | REV |
|---|---|---|---|
| PUYA | Puya SOT23-5 POD | QRPD-0026 | 1.0 |

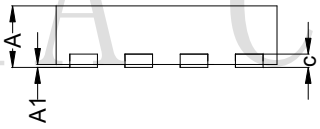


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## 7.5 DFN8




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SIDE VIEW

Common Dimensions
(Unit of Measure=millimeters)

| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| D | 1.90 | 2.00 | 2.10 |
| D2 | 1.40 | 1.50 | 1.60 |
| E | 2.90 | 3.00 | 3.10 |
| E2 | 1.50 | 1.60 | 1.70 |
| e | | 0.50BSC | |
| L | 0.30 | 0.40 | 0.50 |
| c | 0.18 | 0.15 | 0.25 |
| Nd | | 1.50BSC | |

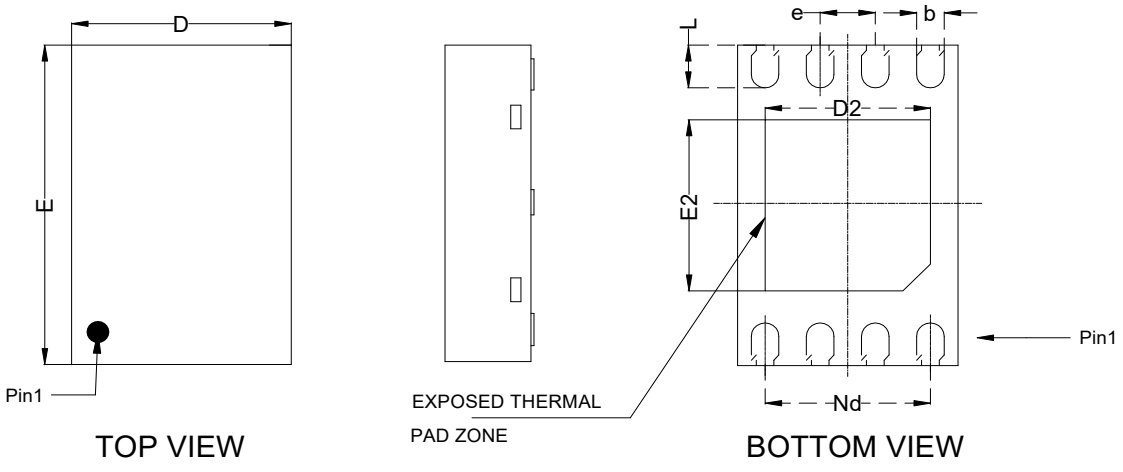
Note：1. Dimensions are not to scale

| | TITLE | DRAWING NO. | REV |
|---|---|---|---|
| PUYA | Puya DFN8L 2x3X0.75-0.5PITCH POD | QRPD-0022 | 1.0 |

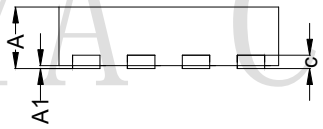


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## 7.6 UDFN8




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SIDE VIEW

Common Dimensions
(Unit of Measure=millimeters)

| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | 0.45 | 0.50 | 0.55 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| D | 1.90 | 2.00 | 2.10 |
| D2 | 1.40 | 1.50 | 1.60 |
| E | 2.90 | 3.00 | 3.10 |
| E2 | 1.50 | 1.60 | 1.70 |
| e | 0.50BSC | | |
| L | 0.30 | 0.40 | 0.50 |
| c | 0.10 | 0.15 | 0.20 |
| Nd | 1.50BSC | | |

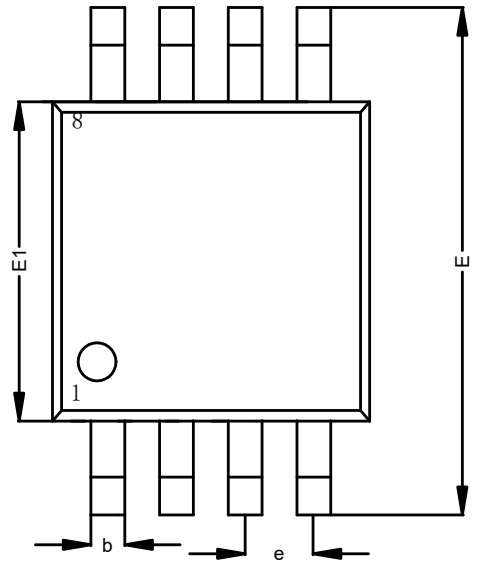
Note：1. Dimensions are not to scale

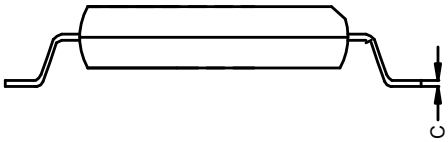
| | TITLE | DRAWING NO. | REV |
|---|---|---|---|
| PUYA | Puya DFN8L 2x3X0.5-0.5PITCH POD | QRPD-0023 | 1.0 |

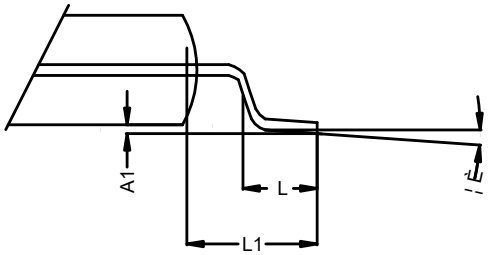


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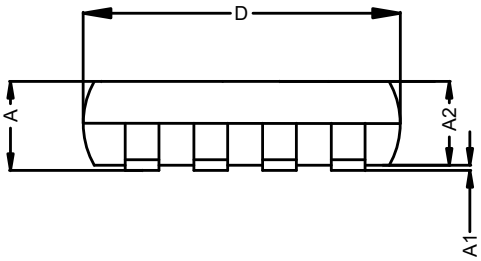
## 7.7 MSOP8




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Common Dimensions
(Unit of Measure=millimeters)

| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | - | - | 1.100 |
| A1 | 0.050 | - | 0.150 |
| A2 | 0.750 | 0.850 | 0.950 |
| b | 0.280 | - | 0.370 |
| c | 0.150 | - | 0.200 |
| D | 2.900 | 3.000 | 3.100 |
| E | 4.700 | 4.900 | 5.100 |
| E1 | 2.900 | 3.000 | 3.100 |
| e | - | 0.650 | - |
| L | 0.400 | - | 0.800 |
| L1 | - | 0.950 | - |
| ¦È | 0 | - | 8¡ã |

Note：1. Dimensions are not to scale

| | TITLE | DRAWING NO. | REV |
|---|---|---|---|
| PUYA | Puya MSOP8 POD | QRPD-0020 | 1.0 |



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## 8. Revision History

| Version | Content | Date |
|---|---|---|
| V1.0 | Initial Release | 2015-01-15 |
| V1.1 | Label changed to P24C256B | 2015-08-31 |
| V1.2 | Add SOT23-5 package | 2016-06-18 |
| V1.3 | Add UDFN package information | 2016-09-13 |
| V1.4 | Add Rpd in DC characteristics | 2017-03-10 |
| V1.5 | Add MSOP8 package | 2019-05-07 |
| V1.6 | Update SOT23-5 package | 2020-04-23 |
| V1.7 | Update feature, 3, 7.3 | 2020-02-26 |
| V1.8 | (1) Update Features<br>(2) Update Table 3-5<br>(3) Add Device Power up/Power down description | 2022-02-03 |
| V1.9 | Update parameter of $V_{IL}$ | 2023-03-26 |
| V2.0 | (1) Update PDIP8 POD<br>(2) Update SOP8(150mil) POD<br>(3) Update TSSOP8 POD<br>(4) Update SOT23-5 POD<br>(5) Update feature description<br>(6) Update $I_{CC1}$ and $I_{CC2}$ of DC Characteristics | 2025-06-16 |

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