NIRS20/NIRS21/NIRS22

High Reliability Dual Channel Digital Isolators

Datasheet (EN) 1.3

Product Overview

The NIRS2x devices are high reliability dual-channel digital isolator. The NIRS2x device is safety certified by UL1577 support 3kV$_{rms}$ insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NIRS2x is up to 1Mbps, and the common-mode transient immunity (CMTI) is up to 100kV/us. The NIRS2x device provides digital channel direction configuration and the default output high level when the input power is lost. Wide supply voltage of the NIRS2x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

Safety Regulatory Approvals

- UL recognition: up to 3000V$_{rms}$ for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Key Features

- Up to 3000V$_{rms}$ Insulation voltage
- Date rate: DC to 1Mbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 100kV/us
- Chip level ESD: HBM: ±6kV
- High system level EMC performance:
  Enhanced system level ESD, EFT, Surge immunity
- Default output high level
- Low power consumption: 1mA/ch (1Mbps)
- Propagation delay: <500ns
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:
  SOIC-8 narrow body

Device Information

Part Number	*Package*	*Body Size*
NIRS2xN1-DSPR	SOP8(150mil)	3.90mm × 4.90mm

Functional Block Diagrams

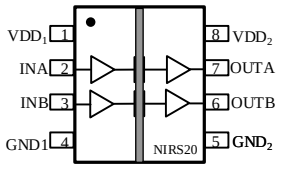


Figure 1.1 NIRS20 Block Diagram

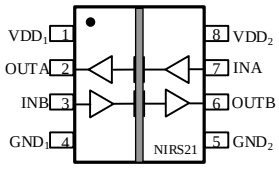


Figure 1.2 NIRS21 Block Diagram

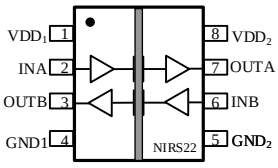


Figure 1.3 NIRS22N Block Diagram

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1. Pin Configuration and Functions

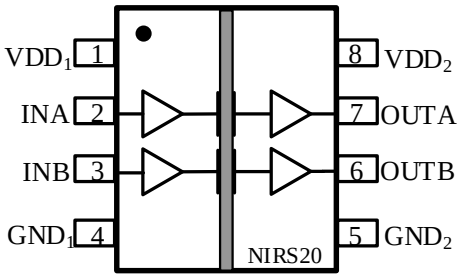


Figure 1.1 NIRS20N Package

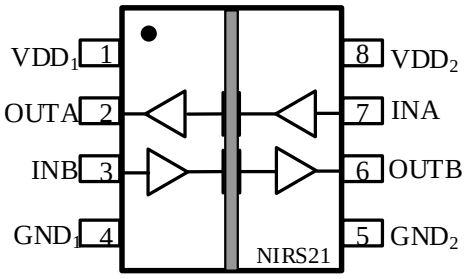


Figure 1.2 NIRS21N Package

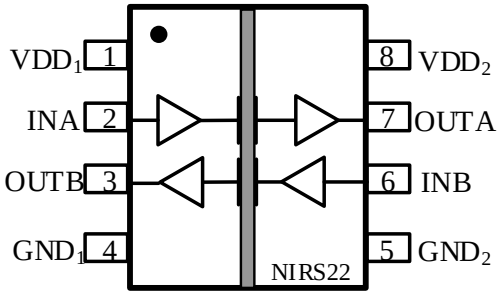


Figure 1.3 NIRS22 Package

Table1.1 NIRS20N/ NIRS21N/ NIRS22N Pin Configuration and Description

Table1.1 NIRS2XN Pin Configuration and Description

NIRS20N PIN NO.	*NIRS21N PIN NO.*	*NIRS22N PIN NO.*	*SYMBOL*	*FUNCTION*
1	1	1	VDD1	Power Supply for Isolator Side 1
7	2	7	OUTA	Logic Output A
3	3	6	INB	Logic Input B
4	4	4	GND1	Ground 1, the ground reference for Isolator Side 1
5	5	5	GND2	Ground 2, the ground reference for Isolator Side 2
6	6	3	OUTB	Logic Output B
2	7	2	INA	Logic Input A
8	8	8	VDD2	Power Supply for Isolator Side 2

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2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	VINA, VINB	-0.4		VDD+0.4[1]	V	The maximum voltage must not exceed 6.5V.
Maximum Output Voltage	V_{OUTA}, V_{OUTB}	-0.4		VDD+0.4[1]	V	The maximum voltage must not exceed 6.5V.
Maximum Input/Output Pulse Voltage	VINA, VINB, V_{OUTA}, V_{OUTB}	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	Io	-15		15	mA	
Maximum Surge Isolation Voltage	V_{IOSM}			6.1	kV	
Operating Temperature	Topr	-40		125	℃	
Junction Temperature	Tj			150	℃	
Storage Temperature	Tstg	-65		150	℃	
Electrostatic discharge	HBM			±6000	V	
	CDM			±2000	V	

3. Recommended Operating Conditions

Parameters	*Symbol*	*min*	*typ*	*max*	*unit*
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V
Operating Temperature	Topr	-40		125	℃
High Level Input Voltage	VIH	2			V
Low Level Input Voltage	VIL			0.8	V
Data rate	DR			1	Mbps

4. Thermal characteristics

Parameters	*Symbol*	*NB-SOIC-8*	*Unit*
IC Junction-to-Air Thermal Resistance	θ_{JA}	137.7	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	54.9	°C/W
Junction-to-board thermal resistance	θ_{JB}	71.7	°C/W

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5. Specifications

5.1. Electrical characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power on Reset	VDD_{POR}		2.2		V	POR threshold as during power-up
	VDD_{HYS}		0.1		V	POR threshold Hysteresis
High Level Input Voltage	V_{IH}	0.7*VDD			V	
Low Level Input Voltage	V_{IL}			0.3*VDD	V	
High Level Output Voltage	V_{OH}	VDD-0.4			V	I_{OH} ≤ 4mA
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} ≤ 4mA
Output Impedance	R_{out}		50		ohm	
Input Pull high or low Current	I_{pull}		8	15	uA	
Start Up Time after POR	trbs		40		usec	
Common Mode Transient Immunity	CMTI	±80	±100		kV/us	

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	NIRS21/ NIRS22					
	I_{DD1}(Q0)		1.42	2.13	mA	All Input at 0V
	I_{DD2}(Q0)		1.42	2.13	mA	
	I_{DD1}(Q1)		0.88	1.32	mA	All Input at supply
	I_{DD2}(Q1)		0.88	1.32	mA	
	I_{DD1}(1M)		1.17	1.76	mA	All Input with 1Mbps, C_L=15pF
	I_{DD2}(1M)		1.17	1.76	mA	
Data Rate	DR	0		1	Mbps	
Minimum Pulse Width	PW			500.0	ns	
Propagation Delay	t_{PLH}		444	480	ns	See Figure 5.1 , C_L = 15pF
	t_{PHL}		438	480	ns	See Figure 5.1 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD		6	15.0	ns	See Figure 5.1 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 5.1 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 5.1 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			10.0	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			10.0	ns	

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(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NIRS21/ NIRS22					
	I_{DD1}(Q0)		1.36	2.04	mA	All Input at 0V
	I_{DD2}(Q0)		1.36	2.04	mA	
	I_{DD1}(Q1)		0.81	1.22	mA	All Input at supply
	I_{DD2}(Q1)		0.81	1.22	mA	
	I_{DD1}(1M)		1.11	1.67	mA	All Input with 1Mbps, C_L = 15pF
	I_{DD2}(1M)		1.11	1.67	mA	
Data Rate	DR	0		1	Mbps	
Minimum Pulse Width	PW			500.0	ns	
Propagation Delay	t_{PLH}		443	480	ns	See Figure 5.1 , C_L = 15pF
	t_{PHL}		437	480	ns	See Figure 5.1 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD		6	15.0	ns	See Figure 5.1 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 5.1 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 5.1 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			10.0	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			10.0	ns	

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	NIRS21/ NIRS22					
	I_{DD1}(Q0)		1.32	1.98	mA	All Input at 0V
	I_{DD2}(Q0)		1.32	1.98	mA	
	I_{DD1}(Q1)		0.78	1.17	mA	All Input at supply
	I_{DD2}(Q1)		0.78	1.17	mA	
	I_{DD1}(1M)		1.07	1.61	mA	All Input with 1Mbps, C_L = 15pF
	I_{DD2}(1M)		1.07	1.61	mA	
Data Rate	DR	0		1	Mbps	
Minimum Pulse Width	PW			500.0	ns	
Propagation Delay	t_{PLH}		443	480	ns	See Figure 5.1 , C_L = 15pF
	t_{PHL}		437	480	ns	See Figure 5.1 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD		6	15.0	ns	See Figure 5.1 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 5.1 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 5.1 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			10.0	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			10.0	ns	

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5.2. Parameter Measurement Information

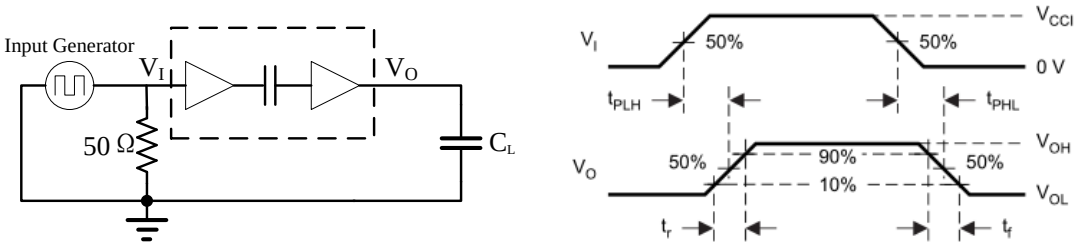


Figure 5.1 Switching Characteristics Test Circuit and Waveform

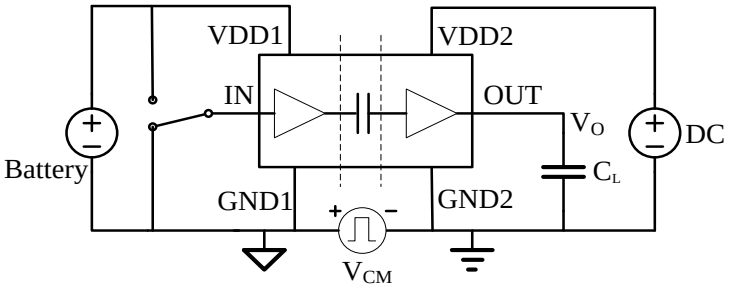


Figure 5.2 Common-Mode Transient Immunity Test Circuit

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6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
			SOP8	
Minimum External Air Gap (Clearance)		L(I01)	4.0	mm
Minimum External Tracking (Creepage)		L(I02)	4.0	mm
Minimum internal gap		DTI	20	um
Tracking Resistance (Comparative Tracking Index)	DIN EN 60112 (VDE 0303-11)	CTI	>400	V
Material Group	IEC 60112		Ⅱ	
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150V_{rms}			Ⅰ to Ⅳ	
For Rated Mains Voltage ≤ 300V_{rms}			Ⅰ to Ⅲ	
For Rated Mains Voltage ≤ 400V_{rms}			Ⅰ to Ⅲ	
Climatic Classification			10/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum repetitive isolation voltage		V_{IORM}	565	Vpeak
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	400	Vpeak
	DC voltage		565	V_{DC}
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	847	Vpeak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	678	Vpeak
After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	678	Vpeak
Maximum transient isolation voltage	t = 60 sec	VIOTM	5300	Vpeak
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, VTEST=VIOSM×1.3	VIOSM	6153	Vpeak
Isolation resistance	VIO =500V	RIO	>10^9	Ω
Isolation capacitance	f = 1MHz	CIO	0.6	pF
Input capacitance		CI	2	pF
Total Power Dissipation at 25℃		Ps	1100	mW
Safety input, output, or supply current	θJA = 137.7°C/W, V I = 5.5 V, T J = 150 °C, T A =	Is	200	mA

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Description	Test Condition	Symbol	Value	Unit
	25 °C			
Case Temperature		Ts	150	℃

6.2. Safety-Limiting Values

Basic isolation safety-limiting values as outlined in VDE-0884-11 of NIRS2x (SOP8)

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{\theta JA}$ = 137,7°C/W1, TJ = 150 °C, TA = 25 °C	908	mW
Safety Supply Current	$R_{\theta JA}$ = 137.7°C/W1, VI = 5.5V, TJ = 150 °C, TA = 25 °C	165	mA
Safety Temperature2)		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP8 package (*Thermal Information Table*) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

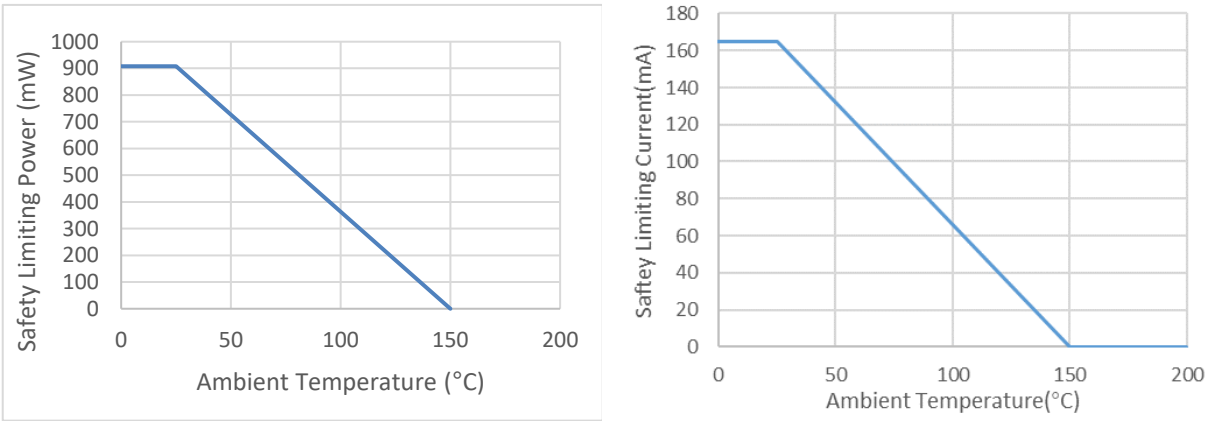


Figure 6.1 NIRS20N/NIRS21N/NIRS22N Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

6.3. Regulatory Information

The NIRS2xN are approved by the organizations listed in table.

CUL		VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11:2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3000V_{rms} Isolation voltage	Single Protection, 3000V_{rms} Isolation voltage	Basic Insulation 565Vpeak, V_{IOSM}=6153Vpeak	Basic insulation
File (E500602)	File (E500602)	File (40050121)	File (CQC20001264940)

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7. Function Description

The NIRS2x is a Dual-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NIRS2x devices are high reliability dual-channel digital isolator. The NIRS2x device is safety certified by UL1577 support 3kV$_{rms}$ insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NIRS2x is up to 1Mbps, and the common-mode transient immunity (CMTI) is up to 100kV/us. The NIRS2x device provides digital channel direction configuration and the default output high level when the input power is lost. Wide supply voltage of the NIRS2x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NIRS2x has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 4.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A within 60us after powering up.

Table 4.1 Output status vs. power status

Input	*VDD1 status*	*VDD2 status*	*Output*	*Comment*
H	Ready	Ready	H	Normal operation.
L	Ready	Ready	L	
X	Unready	Ready	H(NIRS2xN1)	The output follows the same status with the input within 60us after input side VDD1 is powered on.
X	Ready	Unready	X	The output follows the same status with the input within 60us after output side VDD2 is powered on.

8. Application Note

8.1. PCB Layout

The NIRS2x requires a 0.1 µF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 5.1 to Figure 5.4 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω, ±40%. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

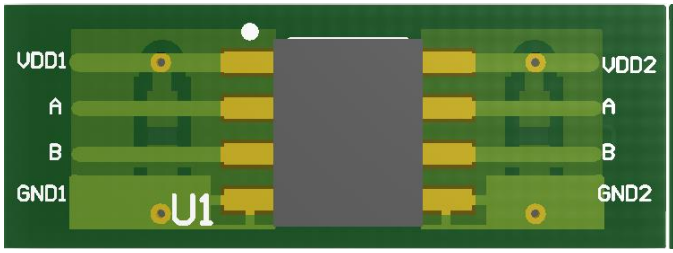


Figure8.1 Recommended PCB Layout — Top Layer

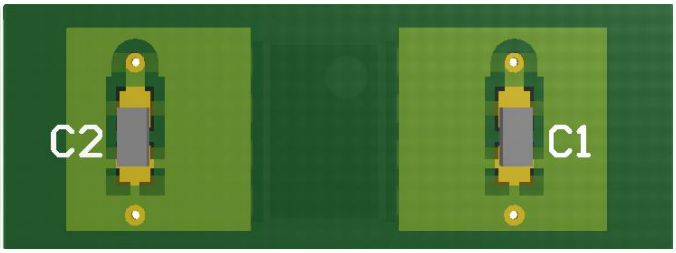
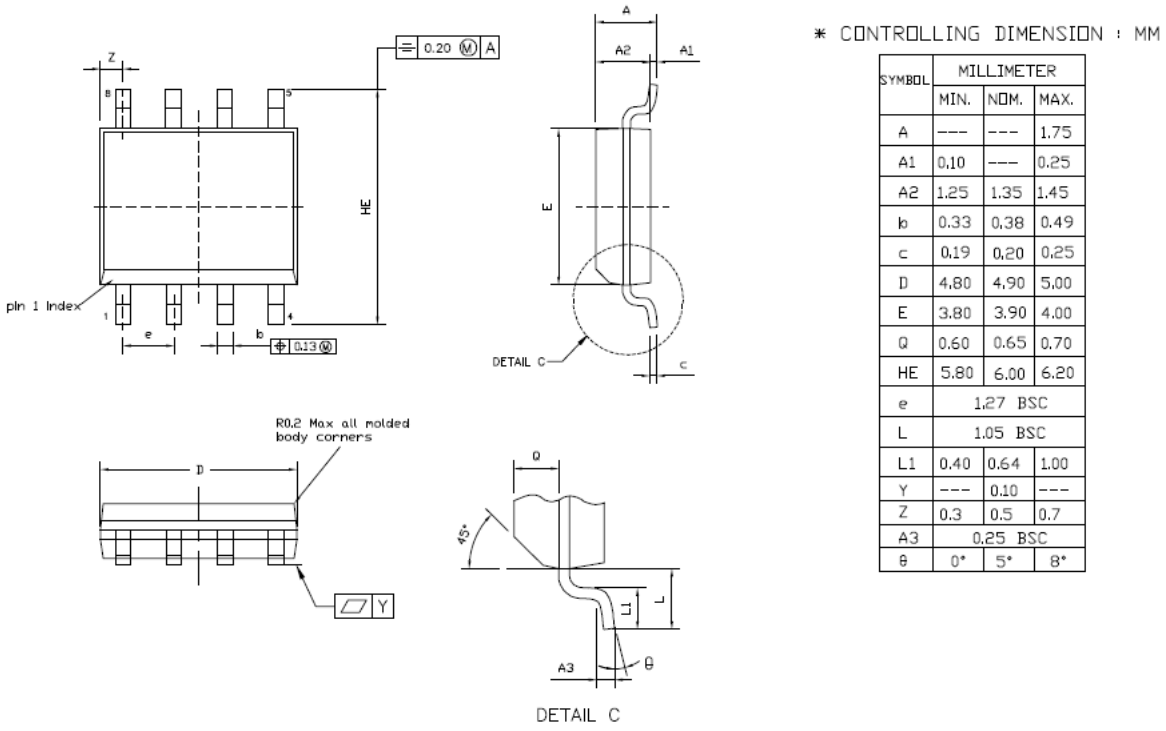


Figure8.2 Recommended PCB Layout — Bottom Layer

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9. Package information



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	1.75
A1	0.10	---	0.25
A2	1.25	1.35	1.45
b	0.33	0.38	0.49
c	0.19	0.20	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
Q	0.60	0.65	0.70
HE	5.80	6.00	6.20
e	1.27 BSC		
L	1.05 BSC		
L1	0.40	0.64	1.00
Y	---	0.10	---
Z	0.3	0.5	0.7
A3	0.25 BSC		
θ	0°	5°	8°

Figure 9.1 SOIC8 Package Shape and Dimension in millimeters (inches)

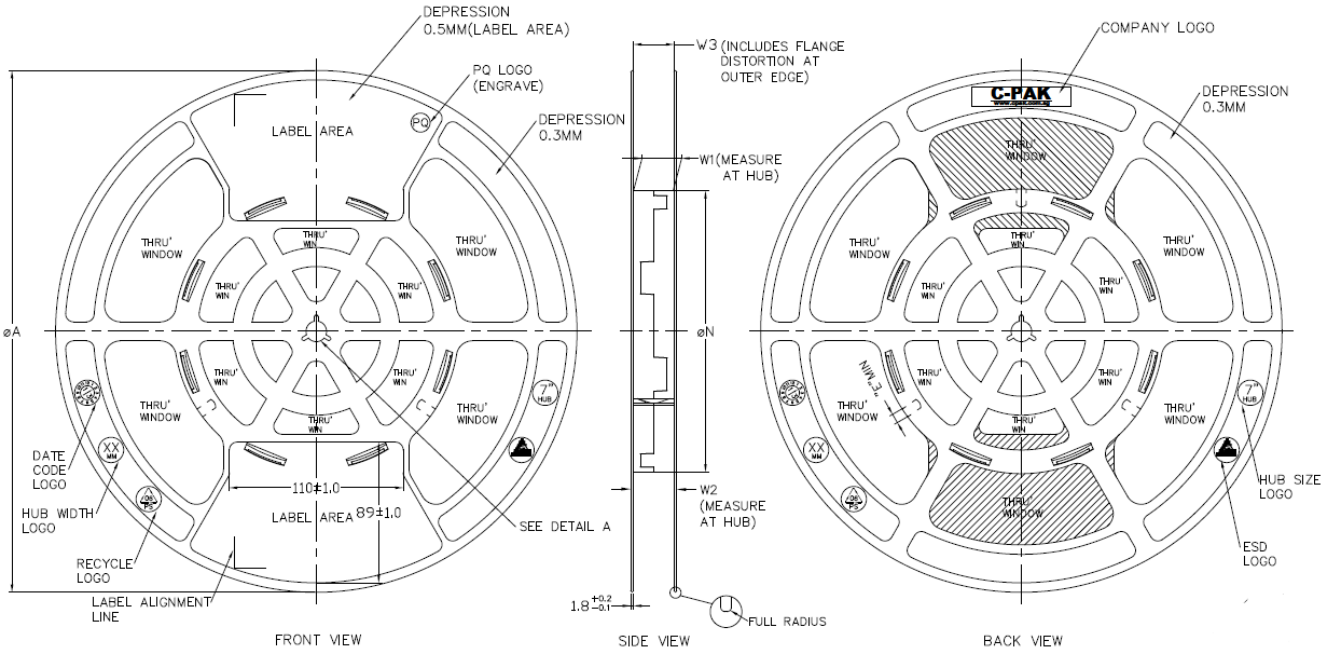
10. Documentation Support

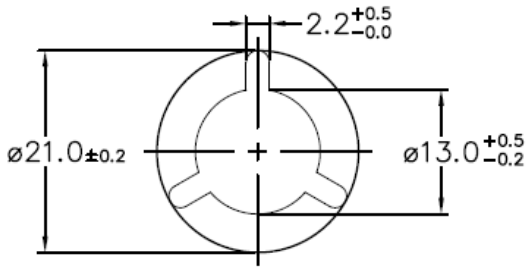
Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NIRS2x	Click here	Click here	Click here	Click here

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11. Tape and Reel Information





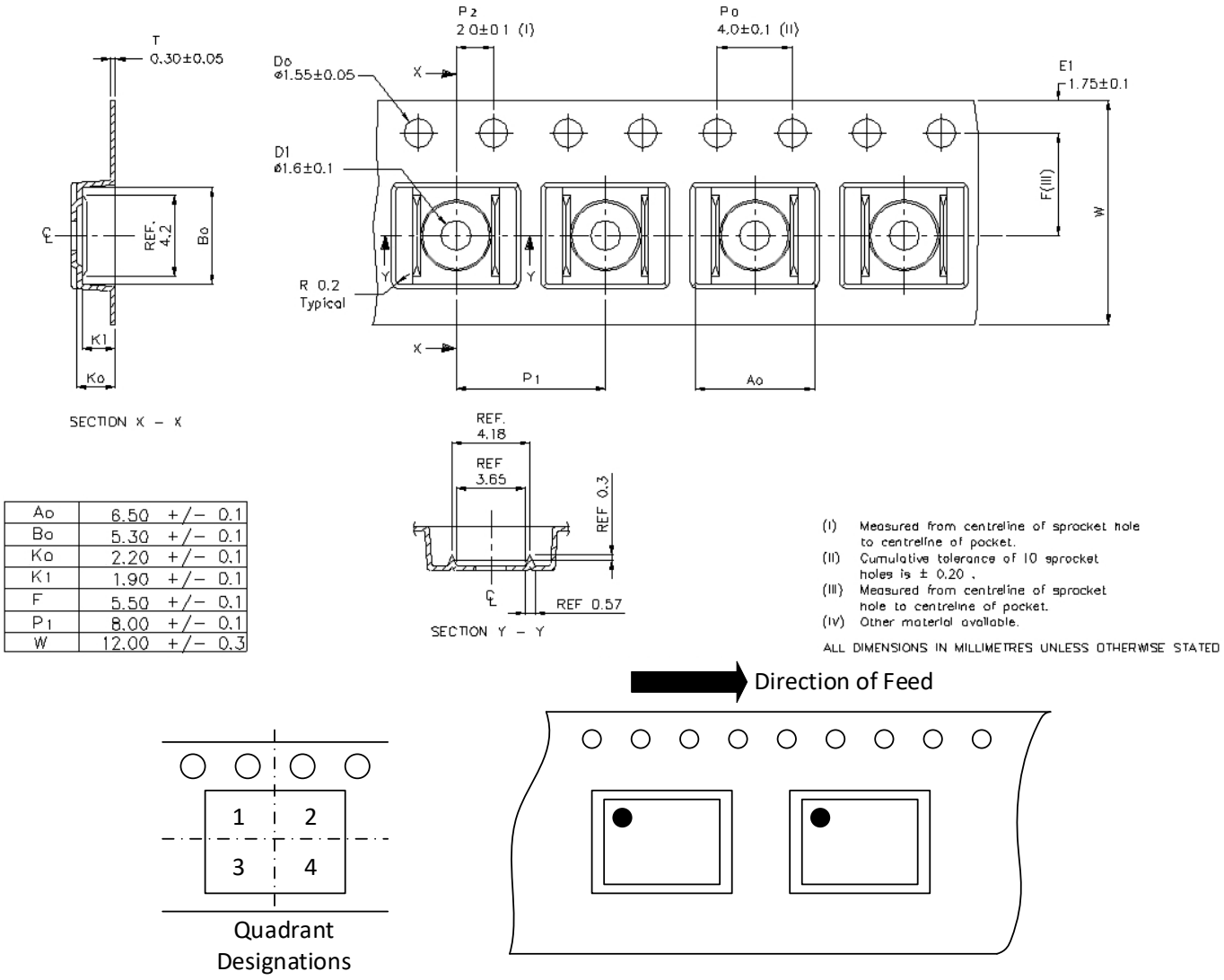
ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 −0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 −0.0	18.4		5.5
16MM	330	178	16.4 +2.0 −0.0	22.4		5.5
24MM	330	178	24.4 +2.0 −0.0	30.4		5.5
32MM	330	178	32.4 +2.0 −0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES

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A0	6.50 +/– 0.1
B0	5.30 +/– 0.1
K0	2.20 +/– 0.1
K1	1.90 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

Figure 11.1 Tape and Reel Information of SOIC8

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12. Order information

Part Number	*Isolation Rating (kV)*	*Number of side 1 inputs*	*Number of side 2 inputs*	*Max Data Rate (Mbps)*	*Default Output State*	*Temperature*	*MSL*	*Package Type*	*Package Drawing*	*SPQ*
NIRS20N1-DSPR	3	2	0	1	High	-40 to 125℃	3	SOP8 (150mil)	SOP8	2500
NIRS21N1-DSPR	3	1	1	1	High	-40 to 125℃	3	SOP8 (150mil)	SOP8	2500
NIRS22N1-DSPR	3	1	1	1	High	-40 to 125℃	3	SOP8 (150mil)	SOP8	2500
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.										

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13. Revision history

Revision	Description	Date
1.0	Original	2019/5/15
1.1	Added NIRS20 part number	2020/10/28
1.2	Modified data rate	2021/2/4
1.3	Update Insulation and Safety Related Specifications, add Thermal Derating Curve, add Junction Temperature, delate “Isolation barrier life: >60 years”	2022/10/8

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