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NCA9545

4-channel I2C-bus switch with interrupt logic and reset

Datasheet (EN) 1.1

Product Overview

The NCA9545 is a quad bidirectional translating switch controlled via the I^2C bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SCn/SDn channel or combination of channels can be selected, determined by the contents of the programmable control register. Four interrupt inputs ($\overline{INT3}$–$\overline{INT0}$), one for each of the downstream pairs, are provided. One interrupt ($\overline{INT}$) output acts as an AND of the four interrupt inputs.

An active-low reset ($\overline{RESET}$) input allows the NCA9545 to recover from a situation in which one of the downstream I^2C buses is stuck in a low state. Pulling $\overline{RESET}$ low resets the I^2C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed such that the VCC terminal can be used to limit the maximum high voltage, which will be passed by the NCA9545. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5 V tolerant.

Key Features

- 1-of-4 Bidirectional Translating Switches
- I^2C Bus and SMBus Compatible
- Four Active-Low Interrupt Inputs
- Active-Low Interrupt Output
- Active-Low Reset Input
- Two Address Terminals, Allowing up to Four Devices on the I^2C Bus
- Channel Selection via I^2C Bus, in Any Combination
- Power-Up With All Switch Channels Deselected
- Low R_{ON} Switches
- Allows Voltage-Level Translation Between 1.8-V, 2.5-V, 3.3-V, and 5-V Buses
- No Glitch on Power-Up
- Supports Hot Insertion
- Low Standby Current
- Operating Power-Supply Voltage Range of 2.3 V to 5.5 V
- 5.5 V Tolerant Inputs
- 0 to 400-kHz Clock Frequency
- Latch-Up Performance Exceeds 100 mA per JESD 78
- ESD Protection Exceeds JESD 22
  - – 2000-V Human-Body Model (A114-A)
  - – 1000-V Charged-Device Model (C101)

Applications

- Servers
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products With I^2C Slave Address Conflicts (e.g. Multiple, Identical Temp Sensors)

Device Information

Part Number	*Package*	*Body Size*
NCA9545_DTSR	TSSOP20	6.5mm*4.5mm

Functional Block Diagrams

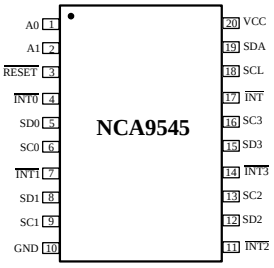


Figure 1. NCA9545 Block Diagram

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1. Pin Configuration and Functions

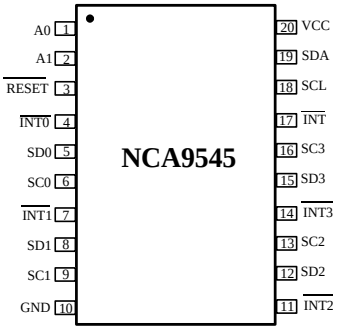


Figure 1.1 NCA9545 Package

Table 1.1 Pin Configuration and Description

Symbol	*Pin*	*Description*
A0	1	Address input 0. Connect directly to VCC or ground.
A1	2	Address input 1. Connect directly to VCC or ground.
$\overline{\text{RESET}}$	3	Active-low reset input. Connect to VCC or V_{DPUM}[1] through a pull-up resistor if not used.
$\overline{\text{INT0}}$	4	Active-low interrupt input 0. Connect to V_{DPU0}[1] through a pull-up resistor.
SD0	5	Serial data 0. Connect to V_{DPU0}[1] through a pul-up resistor.
SC0	6	Serial clock 0. Connect to V_{DPU0}[1] through a pull-up resistor.
$\overline{\text{INT1}}$	7	Active-low interrupt input 1. Connect to V_{DPU1}[1] through a pull-up resistor.
SD1	8	Serial data 1. Connect to V_{DPU1}[1] through a pull-up resistor.
SC1	9	Serial clock 1. Connect to V_{DPU1}[1] through a pull-up resistor.
GND	10	Ground
$\overline{\text{INT2}}$	11	Active-low interrupt input 2. Connect to V_{DPU2}[1] through a pull-up resistor.
SD2	12	Serial data 2. Connect to V_{DPU2}[1] through a pull-up resistor.
SC2	13	Serial clock 2. Connect to V_{DPU2}[1] through a pull-up resistor.
$\overline{\text{INT3}}$	14	Active-low interrupt input 3. Connect to V_{DPU3}[1] through a pull-up resistor.
SD3	15	Serial data 3. Connect to V_{DPU3}[1] through a pull-up resistor.
SC3	16	Serial clock 3. Connect to V_{DPU3}[1] through a pull-up resistor.
$\overline{\text{INT}}$	17	Active-low interrupt output. Connect to V_{DPUM}[1] through a pull-up resistor.
SCL	18	Serial clock line. Connect to V_{DPUM}[1] through a pull-up resistor.
SDA	19	Serial data line. Connect to V_{DPUM}[1] through a pull-up resistor.
VCC	20	Supply power

[1] V_{DPUX} is the pull-up reference voltage for the associated data line. V_{DPUM} is the master I^2C master reference voltage and V_{DPU0}–V_{DPU3} are the slave channel reference voltages.

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2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit	Conditions
Supply Voltage	V_{CC}	-0.5	7	V	
Input/output Voltage	V_I/V_O	-0.5	7	V	
Input current	I_I		±25	mA	
Output current	I_O		±25	mA	V_O<0V
Continuous current through VCC or GND	I_{CC}		±100	mA	
Operating Temperature	Topr	-40	85	℃	
Storage Temperature	Tstg	-40	150	℃	
Electrostatic discharge	HBM		±2000	V	
	CDM		±1000	V	

3. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{CC}	1.65	5.5	V	
High-level input voltage	V_{IH}	0.7*V_{CC}	6	V	SCL, SDA
		0.7*V_{CC}	V_{CC}+0.5	V	A1, A0, INT3–INT0, RESET
Low-level input voltage	V_{IL}	-0.5	0.3*V_{CC}	V	SCL, SDA
		-0.5	0.3*V_{CC}	V	A1, A0, INT3–INT0, RESET
Operating free-air temperature	T_A	-40	85	℃	

4. Thermal Information

Parameters	Symbol		Unit
Junction-to-ambient thermal resistance	θ_{JA}	115.3	℃/W
Junction-to-case(top) thermal resistance	$\theta_{JC(top)}$	48.7	℃/W
Junction-to-board thermal resistance	θ_{JB}	66.4	℃/W

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5. Specifications

5.1. Electrical Characteristics

V_{CC} = 2.7V to 5.5V; T_{amb} =-40℃ to +85℃; unless otherwise noted. Typical specification are at T_A=25℃,V_{CC}=3.3V

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Conditions*
Supply						
Supply voltage Range	V_{CC}	1.65	-	5.5	V	
Power On Reset rising	V_{PORR}	-	1.15	1.4	V	no load; V_I = V_{CC} or GND
Power On Reset falling	V_{PORF}	0.9	1.08		V	no load; VI = V_{CC} or GND
Supply current	I_{CC}	-	-	10	μA	Operating mode; V_{CC} = 5.5 V; V_I=V_{CC} or GND; no load; f_{SCL} = 100 kHz
Standby current	I_{stb}	-	0.3	5	uA	Standby mode; V_{CC} = 5.5 V; V_I=V_{CC} or GND; no load
Input SCL; Input/Output SDA						
LOW-level input voltage	V_{IL}	-0.5	-	0.3*V_{CC}	V	
HIGH-level input voltage	V_{IH}	0.7*V_{CC}	-	6	V	
LOW-level output current	I_{OL}	2.5	15	-	mA	V_{OL} = 0.4 V
		4	20		mA	V_{OL}=0.6V
Input leakage current	I_L	-1	-	+1	μA	V_I = V_{CC} or GND
Input capacitance	C_i	-	15		pF	V_I = GND
Select inputs A0,A1,$\overline{INT0}$,$\overline{INT1}$,$\overline{INT2}$,$\overline{INT3}$,$\overline{RESET}$						
LOW-level input voltage	V_{IL}	-0.5	-	0.3*V_{CC}	V	
HIGH-level input voltage	V_{IH}	0.7*V_{CC}	-	6	V	
Leakage current	I_L	-1	-	1	uA	V_I = V_{CC} or GND
Input capacitance	C_i	-	1.6	3	pF	V_I = GND
$\overline{INT}$ output						
HIGH-level output current	I_{OH}	-	-	±1	uA	

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LOW-level output current	I_{OL}	3	12	-	mA	V_{CC} =3.6V,V_{OL} = 0.4V[2]
		4	17	-	mA	V_{CC} =3.6V,V_{OL} = 0.6 V[2]
Pass gate						
On-state resistance	R_{on}	4	14	20	Ω	Vo=0.4 V, I_O = 15 mA, V_{CC} = 4.5V
		5	16	25	Ω	Vo=0.4 V, I_O = 15 mA, V_{CC} = 3V
		6	19	30		Vo=0.4 V, I_O = 10 mA, V_{CC} = 2.3V
		10	28	40		Vo=0.4 V, I_O = 10 mA, V_{CC} = 1.65V
Switch output voltage	$V_{O(SW)}$		3.64		V	V_{CC} = 5 V, $I_{O(SW)}$ =-100uA
		2.6		4.5		V_{CC} = 4.5V to 5.5 V, $I_{O(SW)}$ =-100uA
			2.15			V_{CC} = 3.3 V, $I_{O(SW)}$ =-100uA
		1.6		2.8	V	V_{CC} = 3 V to 3.6 V, $I_{O(SW)}$ =-100uA
			1.46			V_{CC} = 2.5 V, $I_{O(SW)}$ =-100uA
		1		1.9		V_{CC} = 2.3 V to 2.7 V, $I_{O(SW)}$ =-100uA
			0.99		V	V_{CC} = 1.8 V, $I_{O(SW)}$ =-100uA
		0.5		1.2		V_{CC} = 1.65 V to 1.95 V, $I_{O(SW)}$ =-100uA
Leakage current	I_L	-1	-	+1	µA	V_I = V_{CC} or GND
C_{io}	Input/output capacitance	-	-	6	pF	V_I=GND

5.2. Dynamic Characteristics

Parameters	*Symbol*	*Standard-mode I2C-bus*		*Fast-mode I2C-bus*		*Unit*
		Min	*Max*	*Min*	*Max*	
propagation delay	t_{PD}[1]		0.3		0.3	ns
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	µs
hold time (repeated) START condition	$t_{HD;STA}$[2]	4.0	-	0.6	-	µs
set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	µs
set-up time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	µs
data valid acknowledge time	$t_{VD;ACK}$	0.3	3.45	0.1	0.9	µs
data hold time	$t_{HD;DAT}$[3]	0	-	0	-	ns
data valid time	$t_{VD;DAT}$[4]	300	-	50	-	ns
data set-up time	$t_{SU;DAT}$	250	-	100	-	ns

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LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	µs
fall time of both SDA and SCL signals	t_f	-	300	20 + 0.1C_b[5]	300	ns
rise time of both SDA and SCL signals	t_r	-	1000	20 + 0.1C_b[5]	300	ns
pulse width of spikes that must be suppressed by the input filter	t_{SP}	-	50	-	50	ns
data output valid time	$t_{v(Q)}$	-	200	-	200	ns
data input set-up time	$t_{su(D)}$	150	-	150	-	ns
data input hold time	$t_{h(D)}$	1	-	1	-	µs
$\overline{INT}$						
Valid time from $\overline{INTn}$ to $\overline{INT}$ singal	$t_{iv(INTnN-INT)}$	-	4	-	4	µs
Delay time from $\overline{INTn}$ to $\overline{INT}$ inactive	$t_{ir(INTnN-INT)}$	-	2	-	2	µs
Low-level rejection time	$T_{w(rej)L}$	1	-	1	-	µs
High-level rejection time	$T_{w(rej)H}$	0.5	-	0.5	-	µs
$\overline{RESET}$						
Low-level reset time	$T_{w(rst)L}$	4		4		ns
Reset time	t_{rst}	500		500		ns
Recovery time to START condition		0		0		ns

[1]Pass gate propagation delay is calculated from the 20 Ω typical Ron and the 15 pF load capacitance.

[2]After this period, the first clock pulse is generated.

[3]A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

[4]Measurements taken with 1 k Ω pull-up resistor and 50 pF load.

[5]C_b = total capacitance of one bus line in pF.

5.3. Parameter Measurement Information

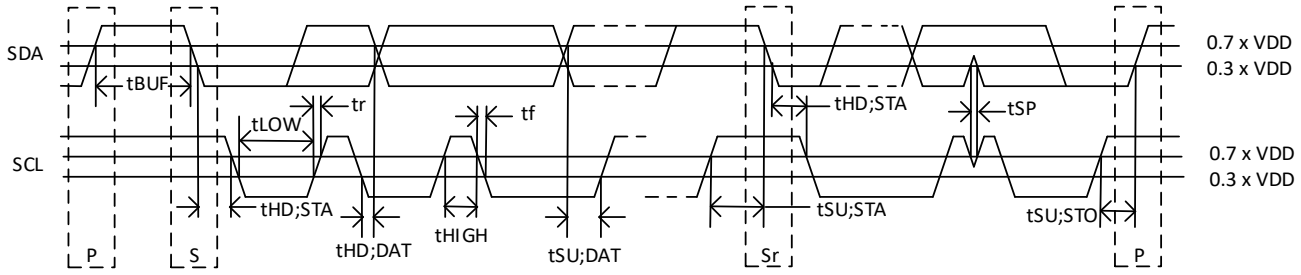


Figure 5.1 Definition of timing on I²C-bus

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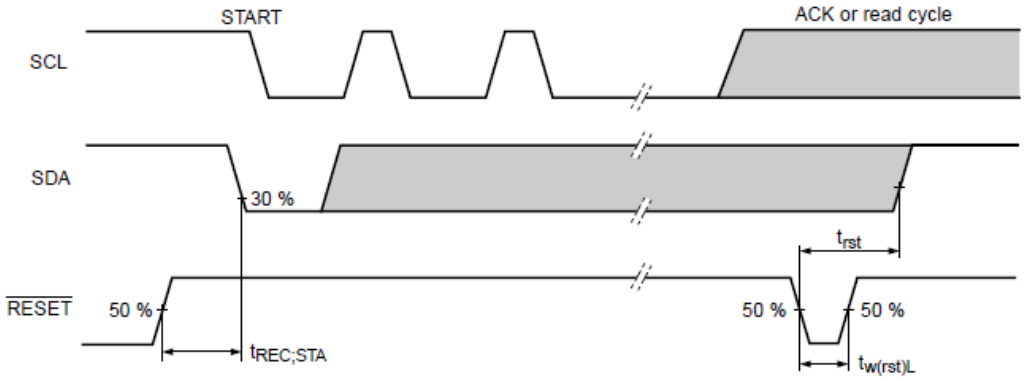


Figure 5.2 Definition of RESET timing

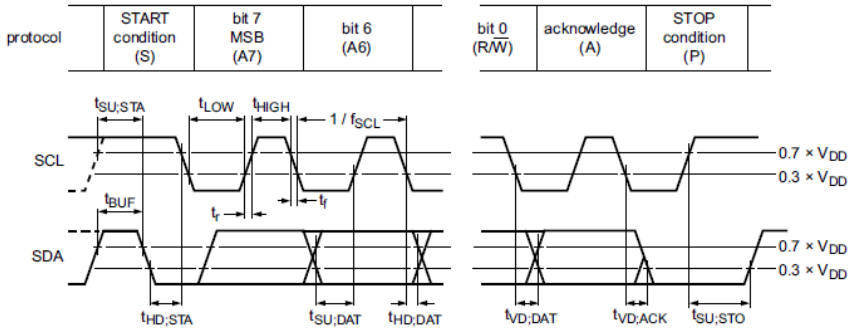


Figure 5.3 I^2C-bus timing diagram

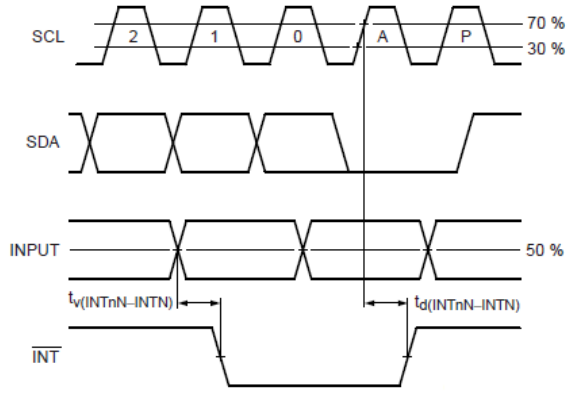
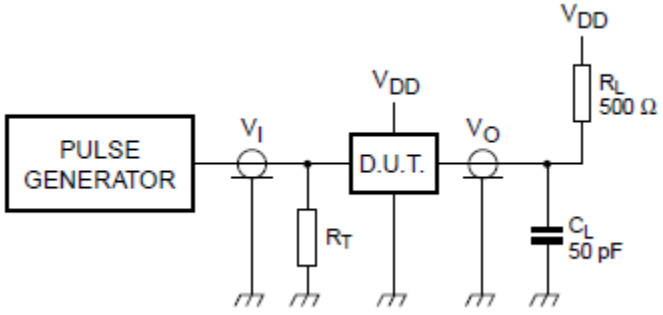


Figure 5.4 Expanded view of read input port register



Definitions test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.

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R_T = Termination resistance should be equal to the output impedance Zo of the pulse generator.

Figure 5.5 Test circuitry for switching times

6. Detailed Description

6.1. Overview

The NCA9545 is a 4-channel, bidirectional translating I²C switch. The master SCL/SDA signal pair is directed to four channels of slave devices, SC0/SD0-SC3/SD3. Any individual downstream channel can be selected as well as any combination of the four channels. The NCA9545 also supports interrupt signals in order for the master to detect an interrupt on the $\overline{INT}$ output terminal that can result from any of the slave devices connected to the $\overline{INT3}$-$\overline{INT0}$ input terminals.

The device offers an active-low $\overline{RESET}$ input which resets the state machine and allows the NCA9545 to recover should one of the downstream I²C buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply, V_{CC}, also known as a power-on reset (POR) Both the RESET function and a POR will cause all channels to be deselected.

The connections of the I²C data path are controlled by the same I²C master device that is switched to communicate with multiple I²C slaves. After the successful acknowledgment of the slave address (hardware selectable by A0 and A1 terminals), a single 8-bit control register is written to or read from to determine the selected channels and state of the interrupts.

The NCA9545 may also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel.

6.2. Functional Block Diagram

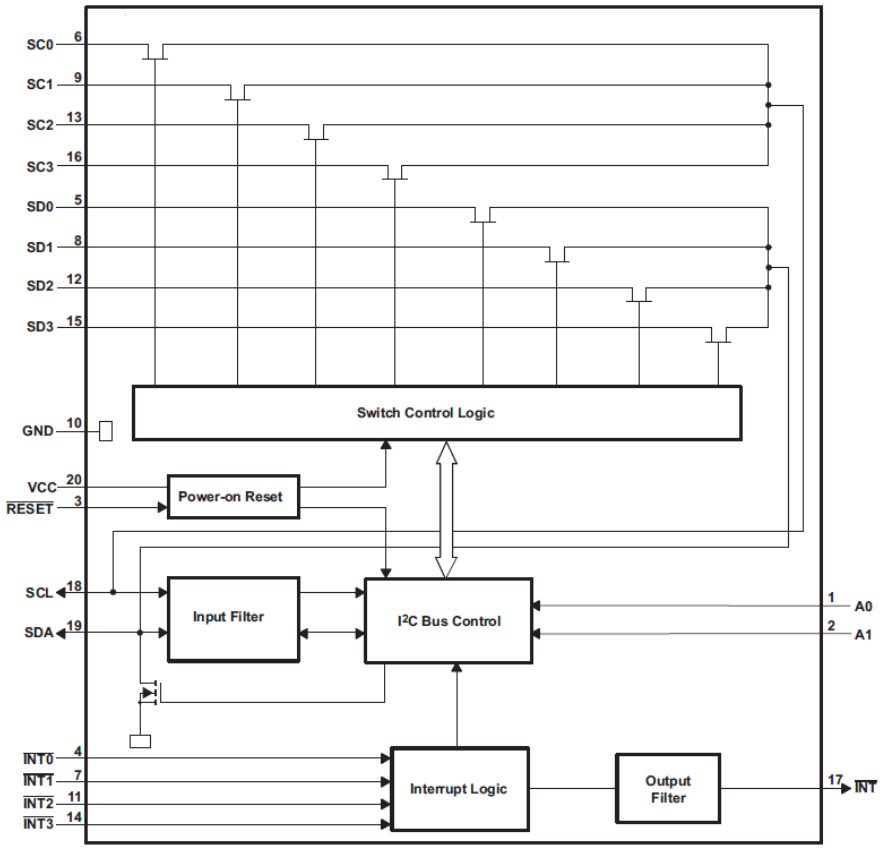


Figure 6.1 NCA9545 Functional block

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6.3. Feature Description

The NCA9545 is a 4-channel, bidirectional translating switch for I²C buses that supports Standard-Mode (100 kHz) and Fast-Mode (400 kHz) operation. The NCA9545 features I²C control using a single 8-bit control register in which the four least significant bits control the enabling and disabling of the 4 switch channels of I²C data flow.

The NCA9545 also supports interrupt signals for each slave channel and this data is held in the four most significant bits of the control register. Depending on the application, voltage translation of the I²C bus can also be achieved using the NCA9545 to allow 1.8-V, 2.5-V, or 3.3-V parts to communicate with 5-V parts. Additionally, in the event that communication on the I²C bus enters a fault state, the NCA9545 can be reset to resume normal operation using the $\overline{\text{RESET}}$ pin feature or by a power-on reset which results from cycling power to the device.

6.4. Device Functional Modes

6.5. $\overline{\text{RESET}}$ Input

The $\overline{\text{RESET}}$ input can be used to recover the NCA9545 from a bus-fault condition. The registers and the I²C state machine within this device initialize to their default states if this signal is asserted low for a minimum of t_{WL}.

All channels also are deselected in this case. $\overline{\text{RESET}}$ must be connected to V_{CC} through a pull-up resistor.

6.6. Power-On Reset

When power is applied to VCC, an internal power-on reset holds the NCA9545 in a reset condition until V_{CC} has reached V_{PORR}. At this point, the reset condition is released and the NCA9545 registers and I²C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below at least V_{PORF} to reset the device.

6.7. Programming

6.8. I²C Interface

The I²C bus is for two-way two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer can be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse, as changes in the data line at this time are interpreted as control signals (see Figure 6.1)

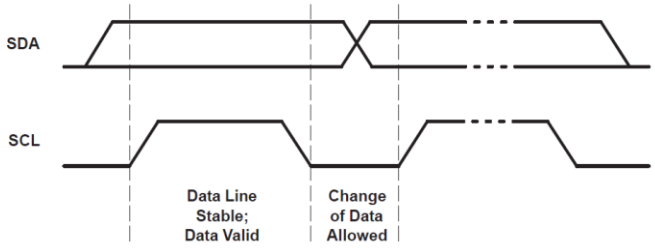


Figure 6.1 Bit Transfer

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see Figure 6.2).

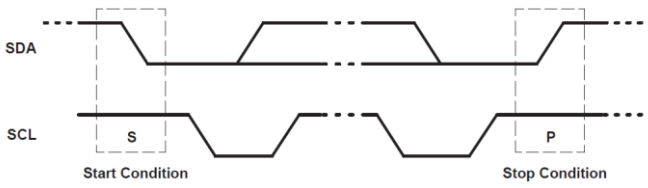


Figure 6.2 Definition of Start and Stop Conditions

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master, and the devices that are controlled by the master are the slaves (see Figure 6.3).

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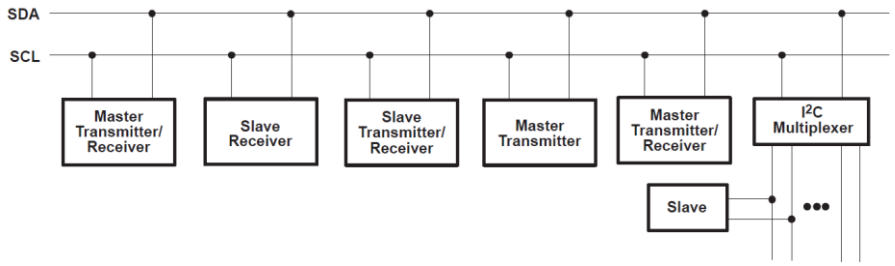


Figure 6.3 System Configuration

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge (ACK) bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

When a slave receiver is addressed, it must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 6.4). Setup and hold times must be taken into account.

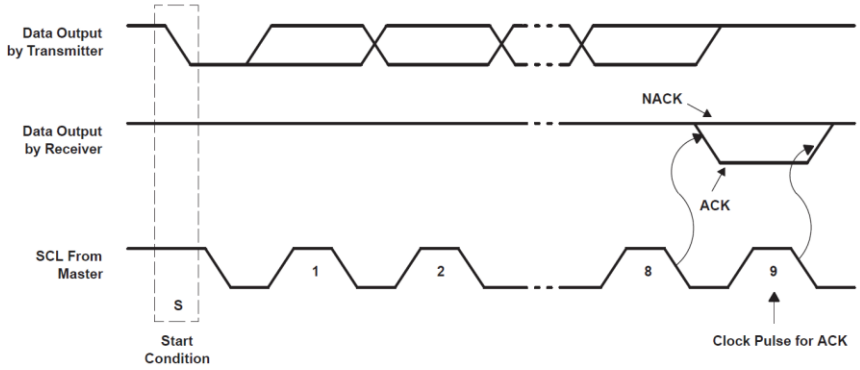


Figure 6.4 Acknowledgment on the I²C Bus

A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition. Data is transmitted to the NCA9545 control register using the write mode shown in Figure 6.5.

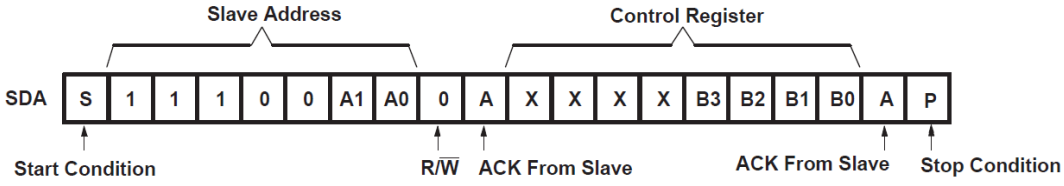


Figure 6.5 Write Control Register

Data is read from the NCA9545 control register using the read mode shown in Figure 6.6.

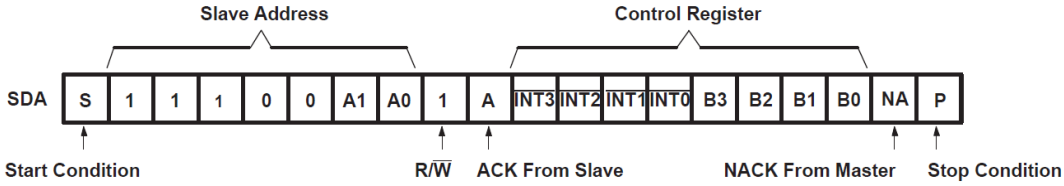


Figure 6.6 Read Control Register

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6.9. Control Register

6.10. Device Address

Following a start condition, the bus master must output the address of the slave it is accessing. The address of the NCA9545 is shown in Figure 6.7 To conserve power, no internal pull-up resistors are incorporated on the hardware-selectable address terminals, and they must be pulled high or low.

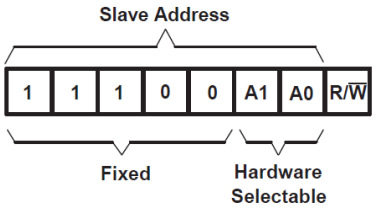


Figure 6.7 NCA9545 Address

The last bit of the slave address defines the operation to be performed. When set to a logic 1, a read is selected, while a logic 0 selects a write operation.

6.11. Control Register Description

Following the successful acknowledgment of the slave address, the bus master sends a byte to the NCA9545, which is stored in the control register (see Figure 6.8). If multiple bytes are received by the NCA9545, it saves the last byte received. This register can be written and read via the I^2C bus.

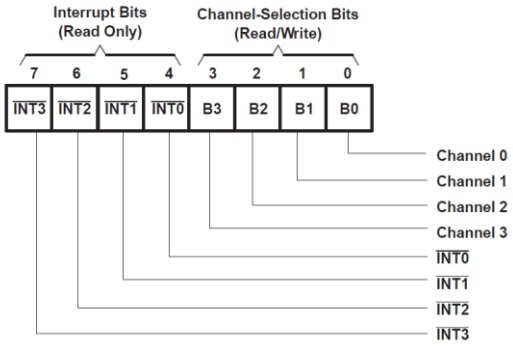


Figure 6.8 Control Register

6.12. Control Register Definition

One or several SCn/SDn downstream pairs, or channels, are selected by the contents of the control register (see Table 1). After the NCA9545 has been addressed, the control register is written. The four LSBs of the control byte are used to determine which channel or channels are to be selected. When a channel is selected, the channel becomes active after a stop condition has been placed on the I2C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition must occur always right after the acknowledge cycle.

Table 1. Control Register Write (Channel Selection), Control Register Read (Channel Status)

INT3	INT2	INT1	INT0	B3	B2	B1	B0	COMMAND
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 enabled
X	X	X	X	X	X	0	X	Channel 1 disabled
						1		Channel 1 enabled
X	X	X	X	X	0	X	X	Channel 2 disabled
					1			Channel 2 enabled
X	X	X	X	0	X	X	X	Channel 3 disabled
				1				Channel 3 enabled
0	0	0	0	0	0	X	0	No channel selected, power-up/reset default state

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[1] Several channels can be enabled at the same time. For example, B3 = 0, B2 = 1, B1 = 1, B0 = 0 means that channels 0 and 3 are disabled, and channels 1 are 2 and enabled. Care should be taken not to exceed the maximum bus capacity.

6.13. Interrupt Handling

The NCA9545 provides four interrupt inputs (one for each channel) and one open-drain interrupt output (see Table 2). When an interrupt is generated by any device, it is detected by the NCA9545 and the interrupt output is driven low. The channel does not need to be active for detection of the interrupt. A bit also is set in the control register. Bits 4–7 of the control register correspond to channels 0–3 of the NCA9545, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master then can address the NCA9545 and read the contents of the control register to determine which channel contains the device generating the interrupt. The master then can reconfigure the NCA9545 to select this channel and locate the device generating the interrupt and clear it.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs can be used as general-purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to VCC.

Table 2. Control Register Read (Interrupt)[1]

$\overline{INT3}$	$\overline{INT2}$	$\overline{INT1}$	$\overline{INT0}$	B3	B2	B1	B0	COMMAND
X	X	X	0	X	X	X	X	No interrupt on channel 0
			1					Interrupt on channel 0
X	X	0	X	X	X	X	X	No interrupt on channel 1
		1						Interrupt on channel 1
X	0	X	X	X	X	X	X	No interrupt on channel 2
	1							Interrupt on channel 2
0	X	X	X	X	X	X	X	No interrupt on channel 3
1								Interrupt on channel 3

[1] Several interrupts can be active at the same time. For example, INT3 = 0, INT2 = 1, INT1 = 1, INT0 = 0 means that there is no interrupt on channels 0 and 3, and there is interrupt on channels 1 and 2.

7. Application and Implementation

Applications of the NCA9545 will contain an I^2C (or SMBus) master device and up to four I^2C slave devices. The downstream channels are ideally used to resolve I^2C slave address conflicts. For example, if four identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0, 1, 2, and 3. When the temperature at a specific location needs to be read, the appropriate channel can be enabled and all other channels switched off, the data can be retrieved, and the I^2C master can move on and read the next channel.

In an application where the I^2C bus will contain many additional slave devices that do not result in I^2C slave address conflicts, these slave devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels. If multiple switches will be enabled simultaneously, additional design requirements must be considered (See Design Requirements and Detailed Design Procedure).

7.1. Typical Application

A typical application of the NCA9545 will contain anywhere from 1 to 5 separate data pull-up voltages, V_{DPUX} , one for the master device (V_{DPUM}) and one for each of the selectable slave channels (V_{DPU0} – V_{DPU3}). In the event where the master device and all slave devices operate at the same voltage, then the pass voltage, $V_{pass} = V_{DPUX}$. Once the maximum Vpass is known, Vcc can be selected easily using Figure 7.2 In an application where voltage translation is necessary, additional design requirements must be considered (See Design Requirements).

Figure 7.1 shows an application in which the NCA9545 can be used.

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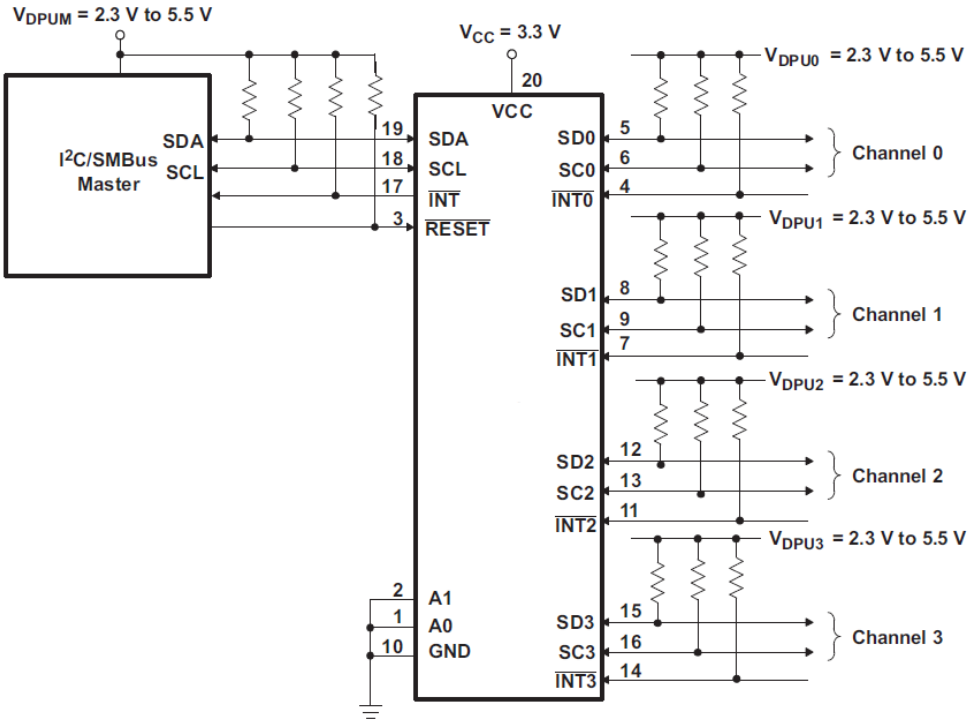


Figure 7.1 Typical Application Schematic

7.2. Design Requirements

The pull-up resistors on the $\overline{INT3}$-$\overline{INT0}$ terminals in the application schematic are not required in all applications. If the device generating the interrupt has an open-drain output structure or can be tri-stated, a pull-up resistor is required. If the device generating the interrupt has a push-pull output structure and cannot be tri-stated, a pull-up resistor is not required. The interrupt inputs should not be left floating in the application.

The A0 and A1 terminals are hardware selectable to control the slave address of the NCA9545. These terminals may be tied directly to GND or VCC in the application.

If multiple slave channels will be activated simultaneously in the application, then the total I_{OL} from SCL/SDA to GND on the master side will be the sum of the currents through all pull-up resistors, R_p.

The pass-gate transistors of the NCA9545 are constructed such that the VCC voltage can be used to limit the maximum voltage that is passed from one I^2C bus to another.

Figure 7.2 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the Electrical Characteristics section of this data sheet). In order for the NCA9545 to act as a voltage translator, the V_{pass} voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V, V_{pass} must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 7.2, Vpass(max) is 2.7 V when the NCA9545A supply voltage is 4 V or lower, so the NCA9545A supply voltage could be set to 3.3 V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 7.1).

7.3. Detailed Design Procedure

Once all the slaves are assigned to the appropriate slave channels and bus voltages are identified, the pull-up resistors, R_p, for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of V_{DPUX}, $V_{OL,(max)}$, and $_{IOL}$:

$$R_{p(min)} = \frac{V_{DPUV} - V_{OL(max)}}{I_{OL}} \qquad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, tr (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \qquad (2)$$

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The maximum bus capacitance for an I²C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the NCA9545, $C_{io(OFF)}$, the capacitance of wires/connections/traces, and the capacitance of each individual slave on a given channel. If multiple channels will be activated simultaneously, each of the slaves on all channels will contribute to total bus capacitance.

7.4. NCA9545 Application Curves

Figure 7.2 Pass-Gate Voltage (V_{pass}) vs Supply Voltage(V_{CC}) at Three Temperature Points

Figure 7.3 Maximum Pull-Up resistance($R_{p(max)}$) vs Bus Capacitance(C_b)

Figure 7.4 Minimum Pull-Up resistance($R_{p(min)}$) vs Pull-up reference voltage(V_{DPUX})

8. Layout

8.1. Layout Guidelines

For PCB layout of the NCA9545, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I²C signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and terminals that are connected to ground should have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC terminal, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all VDPUX voltages and VCC could be at the same potential and a single copper plane could connect all of pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, V_{DPUM}, V_{DPU0}, V_{DPU1}, V_{DPU2}, and V_{DPU3} may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I2C bus capacitance added by PCB parasitics, data lines (SCn, SDn and INTn) should be a short as possible and the widths of the traces should also be minimized (e.g. 5-10 mils depending on copper weight).

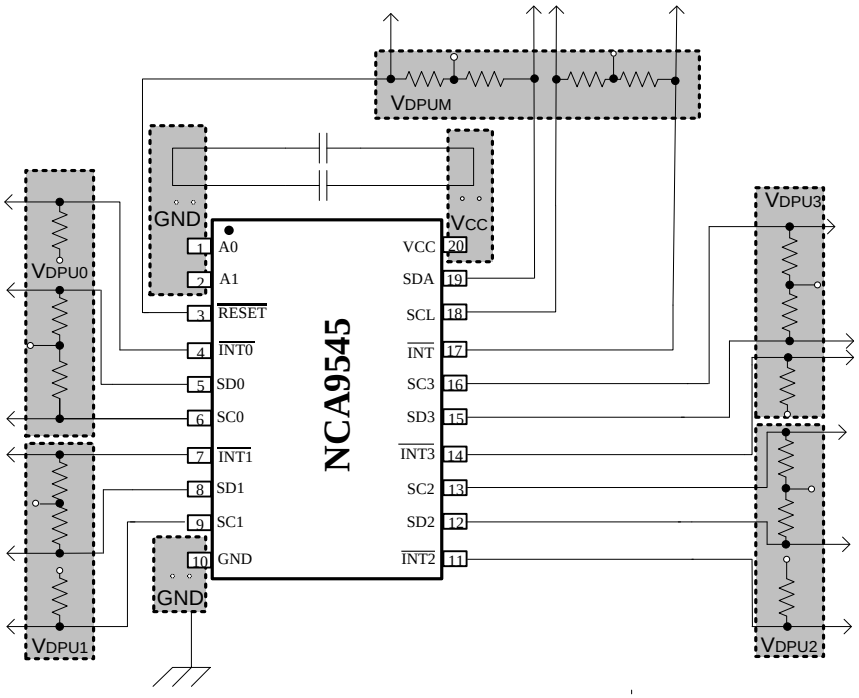
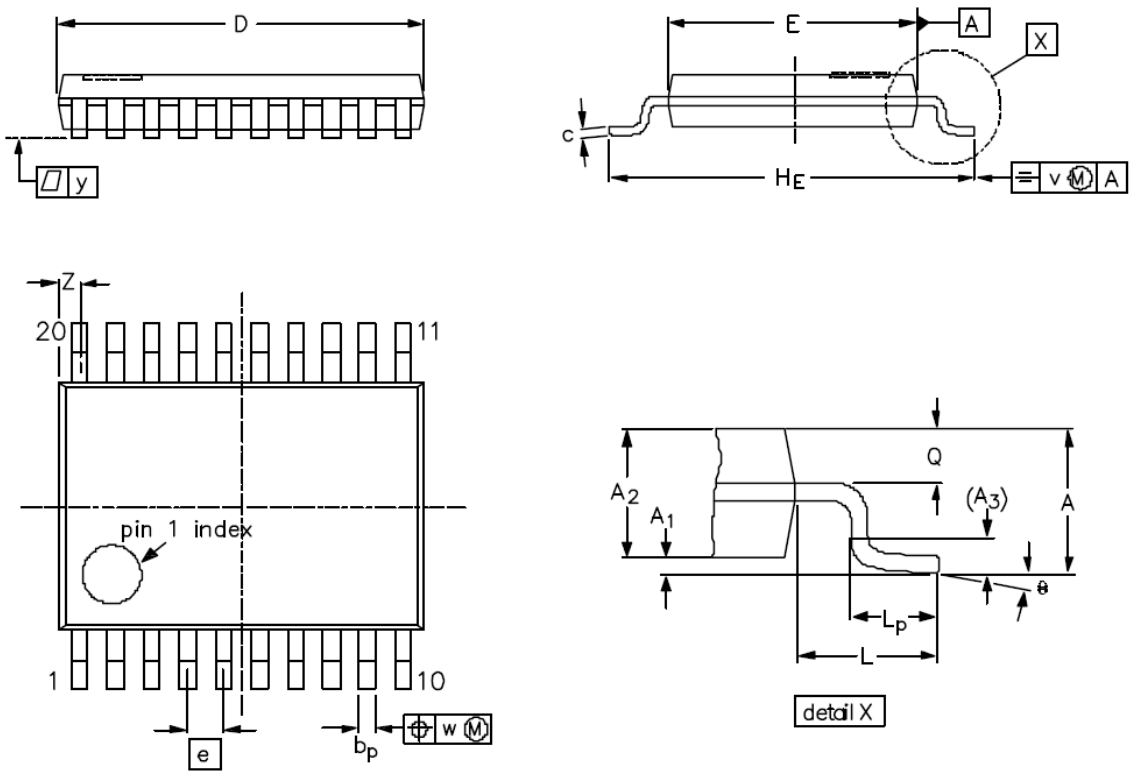


Figure 8.1 Typical Application PCB

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9. Package Information



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Figure 9.1 Package outline for TSSOP20

10. Order information

Part Number	*Pins*	*Temperature*	*MSL*	*Package Type*	*Package Drawing*	*Package Qty*
NCA9545-DTSR	20	-40 to 85℃	1	TSSOP20	TSSOP	2500

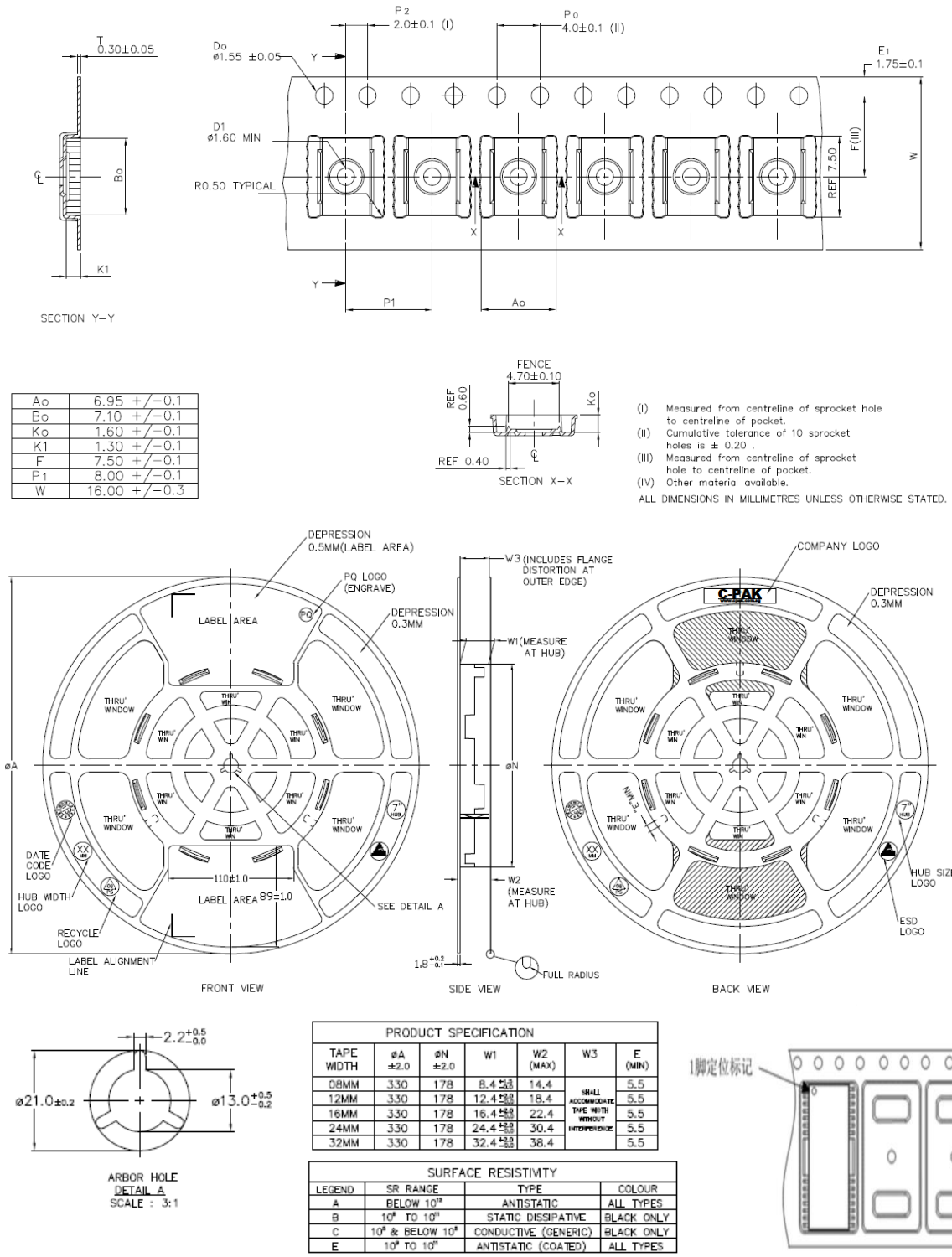
11. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NCA9545	Click here	Click here	Click here	Click here

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12. Tape and Reel Information



Ao	6.95 +/−0.1
Bo	7.10 +/−0.1
Ko	1.60 +/−0.1
K1	1.30 +/−0.1
F	7.50 +/−0.1
P1	8.00 +/−0.1
W	16.00 +/−0.3

PRODUCT SPECIFICATION

TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 −0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 −0.0	18.4		5.5
16MM	330	178	16.4 +2.0 −0.0	22.4		5.5
24MM	330	178	24.4 +2.0 −0.0	30.4		5.5
32MM	330	178	32.4 +2.0 −0.0	38.4		5.5

SURFACE RESISTIVITY

LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{9} TO 10^{12}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{9}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{6} TO 10^{9}	ANTISTATIC (COATED)	ALL TYPES

Figure 12.1 Tape and Reel Information of TSSOP

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13. Revision History

Revision	Description	Date
1.0	Initial version	2020/4/29
1.1	Added tape and reel information	2020/7/6

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