3V, 2G-bit Serial NAND Flash Memory

MX35LF2G14AC

深圳市满度科技有限公司
Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com
微信扫码咨询客服

Contents

1. FEATURES 5

2. GENERAL DESCRIPTIONS 6

Figure 1. Logic Diagram 6

3. ORDERING INFORMATION 7

4. BALL ASSIGNMENT AND DESCRIPTIONS 8

Figure 2. 8-WSON (8x6mm) 8

5. PIN DESCRIPTIONS 8

6. DEVICE OPERATION 9

Figure 3. Serial Mode Supported 9

7. ADDRESS MAPPING 10

8. COMMAND DESCRIPTION 11

Table 1. Command Set 11

8-1. WRITE Operations 12

8-1-1. Write Enable 12

Figure 4. Write Enable (WREN) Sequence 12

8-1-2. Write Disable (04h) 12

Figure 5. Write Disable (WRDI) Sequence 12

8-2. Feature Operations 13

8-2-1. GET Feature (0Fh) and SET Feature (1Fh) 13

Table 2. Feature Settings 13

Figure 6. GET FEATURE (0Fh) Timing 13

Figure 7. SET FEATURE (1Fh) Timing 14

8-3. READ Operations 14

8-3-1. PAGE READ (13h) 14

Table 3. Wrap Address bit Table 14

8-3-2. QE bit 14

Figure 8. PAGE READ (13h) Timing x1 15

Figure 9. RANDOM DATA READ (03h or 0Bh) Timing 16

Figure 10. READ FROM CACHE x 2 17

Figure 11. READ FROM CACHE x 4 18

8-3-3. Page Read Cache Sequential (31h) / Page Read Cache End (3Fh) 19

Figure 12. Page Read Cache Sequential (31h) 19

Figure 13. Page Read Cache End (3Fh) 20

Figure 14. Page Read Cache Flow 21

深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

8-3-4. READ ID (9Fh) **22**
Table 4. READ ID Table 22
Figure 15. READ ID (9Fh) Timing 22
8-4. Parameter Page **23**
Table 5. Parameter Page Data Structure 23
8-5. UniqueID Page **25**
8-6. Program Operations **26**
8-6-1. PAGE PROGRAM **26**
Figure 16. PROGRAM LOAD (02h) Timing 26
Figure 17. PROGRAM LOAD RANDOM DATA (84h) Timing 27
8-6-2. QUAD IO PAGE PROGRAM **28**
Figure 18. PROGRAM LOAD X4 (32h) Timing 28
Figure 19. QUAD IO PROGRAM RANDOM INPUT (34h) Timing 29
Figure 20. PROGRAM EXECUTE (10h) Timing 30
9. BLOCK OPERATIONS **31**
9-1. Block Erase (D8h) **31**
Figure 21. Block Erase (BE) Sequence 31
10. Feature Register **32**
10-1. Block Protection Feature **32**
Table 6. Definition of Protection Bits 33
10-2. Secure OTP (One-Time-Programmable) Feature **34**
Table 7. Secure OTP States 34
10-3. Status Register **35**
Table 8. Status Register Bit Descriptions 35
11. SOFTWARE ALGORITHM **36**
11-1. Invalid Blocks (Bad Blocks) **36**
Figure 22. Bad Blocks 36
Table 9. Valid Blocks 36
11-2. Bad Block Test Flow **37**
Figure 23. Bad Block Test Flow 37
11-3. Failure Phenomena for Read/Program/Erase Operations **37**
Table 10. Failure Modes 37
12. DEVICE POWER-UP **38**
12-1. Power-up **38**
Figure 24. Power On Sequence 38

深圳市满度科技有限公司 Tel:+86-1290-5940
Web:www.manduic.com Email:sales@manduic.com

13. PARAMETERS 39
13-1. ABSOLUTE MAXIMUM RATINGS 39
Figure 25. Maximum Negative Overshoot Waveform 39
Table 11. AC Testing Conditions 39
Table 12. Capacitance 39
Table 13. Operating Range 39
Figure 26. Maximum Positive Overshoot Waveform 39
Table 14. DC Characteristics 40
Table 15. General Timing Characteristics 40
Table 16. PROGRAM/READ/ERASE Characteristics 40
Figure 27. WP# Setup Timing and Hold Timing during SET FEATURE when BPRWD=1 41
Figure 28. Serial Input Timing 41
Figure 29. Serial Output Timing 41
Figure 30. Hold Timing 42
14-1. 8-WSON (8x6x0.8mm) 43
14. PACKAGE INFORMATION 43
15. REVISION HISTORY 44

深圳市满度科技有限公司
Web:www.manduic.com
Tel:86-1290-5940
Email:sales@manduic.com

1. FEATURES

- **2Gb SLC NAND Flash**
  - Bus: x4
  - Page size: (2048+64) byte
  - Block size: (128K+4K) byte
- **4-bit ECC/ 528B is required**
- **Fast Read Access**
  - Supports Random data read out by x1 x2 & x4 modes, (1-1-1,1-1-2, 1-1-4)[Note 1]
  - Latency of array to register: 25us
  - Frequency: 104MHz
- **Page Program Operation**
  - Page program time: 300us (typ)
- **Block Erase Operation**
  - Block erase time: 1ms (typ.)
- **Single Voltage Operation:**
  - VCC: 2.7 to 3.6V
- **BP bits for block group protection**
- **Low Power Dissipation**
  - Max 30mA
    Active current (Read/Program/Erase)
- **Sleep Mode**
  - 50uA (Max) standby current
- **High Reliability**
  - Program / Erase Endurance: Typical 100K cycles (with 4-bit ECC per 512+16) Byte
  - Data Retention: 10 years
- **Wide Temperature Operating Range**
  -40°C to +85°C
- **Package:**
  8-WSON (8x6mm)
  All packaged devices are RoHS Compliant and Halogen-free.

***Note 1**. Which indicates the number of I/O for command, address and data.*

深圳市满度科技有限公司 Tel:+86-1290-5940
Web:www.manduic.com Email:sales@manduic.com

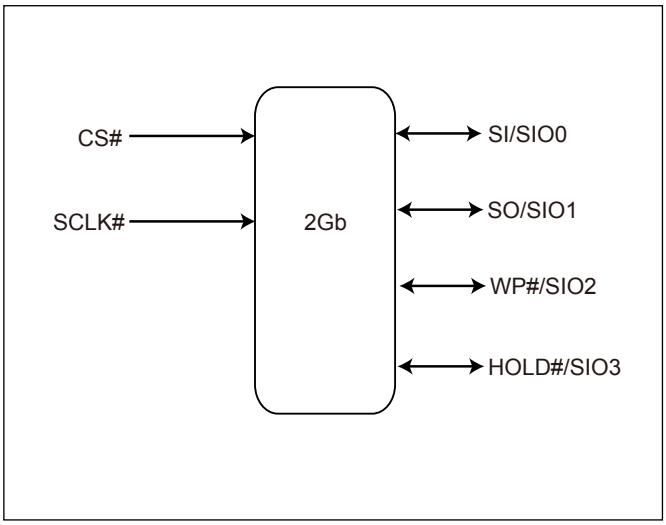
2. GENERAL DESCRIPTIONS

The MX35LF2G14AC is a 2Gb SLC NAND Flash memory device with Serial interface.

The memory array of this device adopted the same cell architecture as the parallel NAND, however implementing the industry standard serial interface.

The device needs the micro controller of host side to support 4-bit ECC/528-byte operation.

Figure 1. Logic Diagram

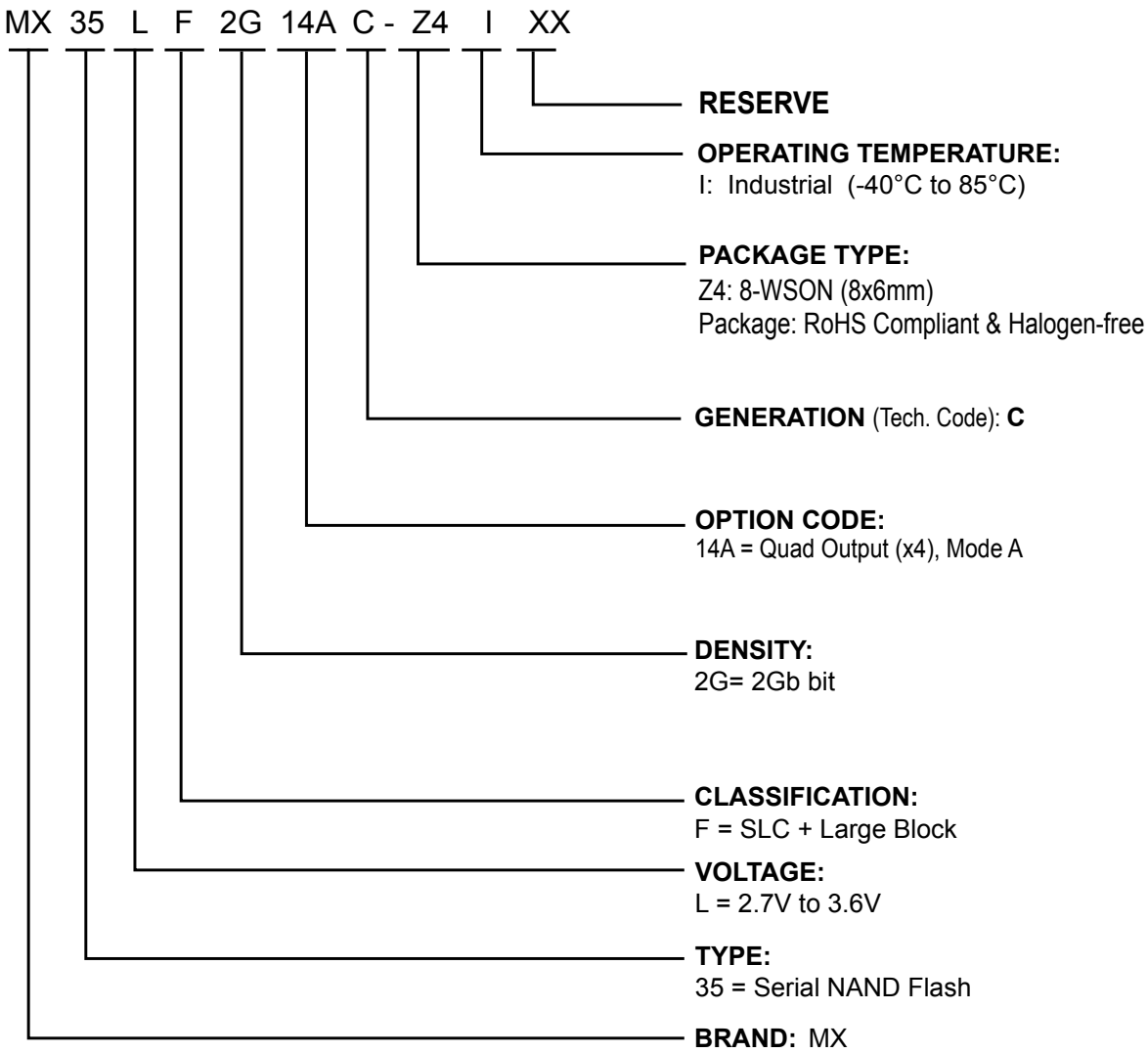


深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

3. ORDERING INFORMATION

Part Name Description

Macronix NAND Flash devices are available in different configurations and densities. Verify valid part numbers by using Macronix's product search at http://www.Macronix.com. Contact Macronix sales for devices not found.



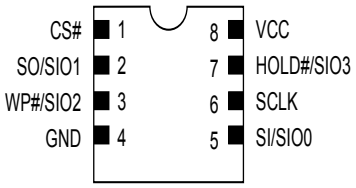
Please contact our regional sales for the latest product selection and available form factors.

Part Number	Density	Organization	VCC Range	Package	Temperature Grade
MX35LF2G14AC-Z4I	2Gb	x4	3V	8-WSON	Industrial

深圳市满度科技有限公司
Web:www.manduic.com
Tel:+86-1290-5940
Email:sales@manduic.com

4. BALL ASSIGNMENT AND DESCRIPTIONS

Figure 2. 8-WSON (8x6mm)



5. PIN DESCRIPTIONS

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (For 1-1-2 or 1-1-4[note1] mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (For 1-1-2 or 1-1-4[note1] mode)
SCLK	Clock Input
WP#/SIO2	Write protection: connect to GND or Serial Data Input & Output (For 1-1-4[note1] mode)
HOLD#/SIO3	Hold or Serial Data Input & Output (For 1-1-4[note1] mode)
VCC	+ 3V Power Supply
GND	Ground
NC	No Connection
DNU	Do not use

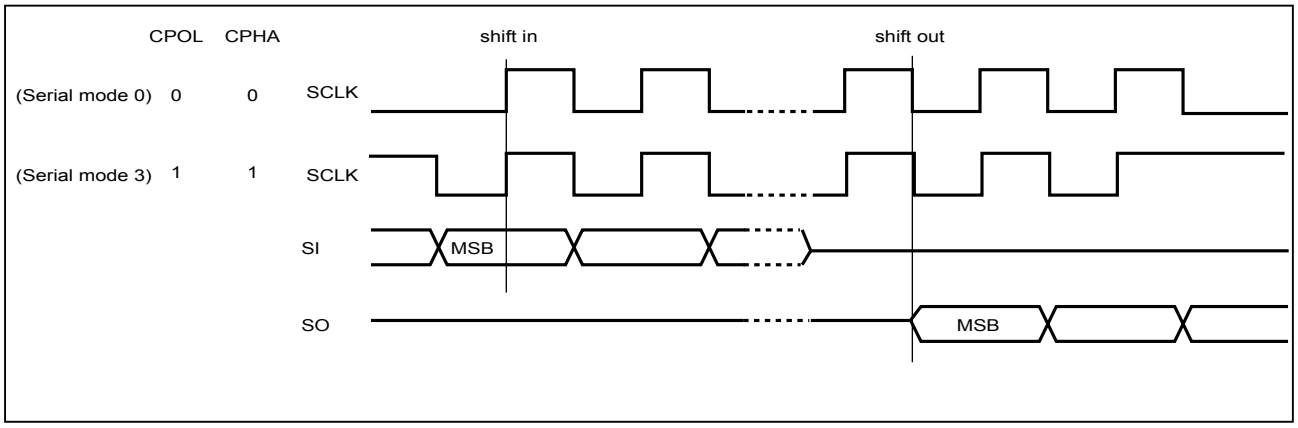
***Note 1**. Which indicates the number of I/O for command, address, and data.*

深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

6. DEVICE OPERATION

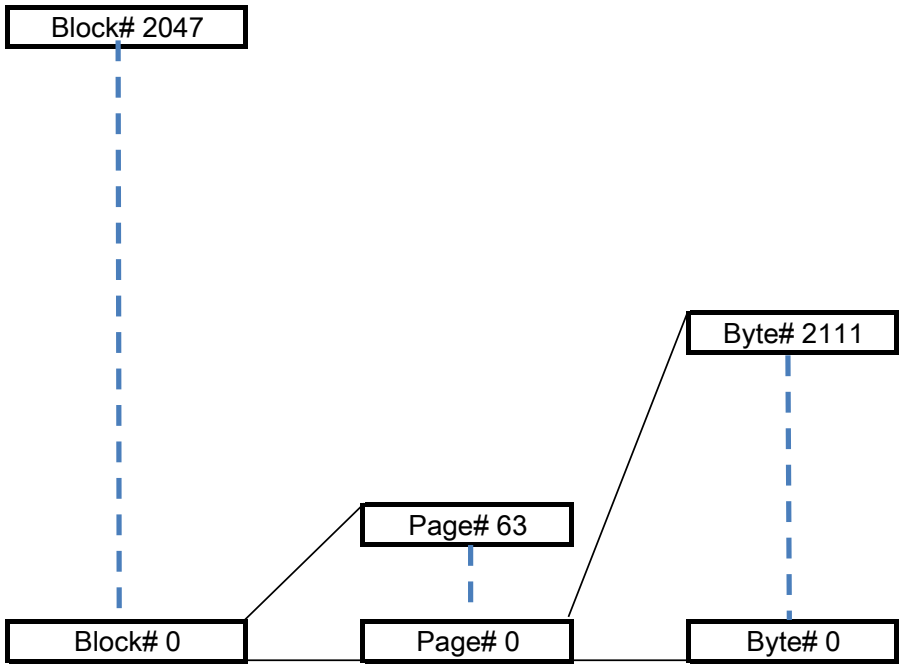
1. Before a command is issued, status register should be checked via get features operations to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this device, this device becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this device should be High-Z.
3. When correct command is inputted to this device, this device becomes active mode and keeps the active mode until next CS# rising edge.
4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as **"Figure 3. Serial Mode Supported"**.
5. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 3. Serial Mode Supported



深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

7. ADDRESS MAPPING



Block address	Page address	Byte address
RA [16:6] Note 1	RA [5:0]	CA [11:0]

***Note 1**: RA[6] is for plane select*

深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

8. COMMAND DESCRIPTION

Table 1. Command Set

Read/Write Array Commands

Command Type	GET FEATURE	SET FEATURE	PAGE READ	READ FROM CACHE	READ FROM CACHE x2
Command Code	0Fh	1Fh	13h	03h, 0Bh	3Bh
Address Bytes	1	1	3	2	2
Dummy Bytes	0	0	0	1	1
Data Bytes	1	1	0	1 to 2112	1 to 2112
Actions	Get features	Set features	Array read	Output cache data on SO	Output cache data on SI and SO

Command Type	READ FROM CACHE x4	PAGE Read Cache Sequential	PAGE Read Cache End	READ ID	BLOCK ERASE	PROGRAM EXECUTE	PROGRAM LOAD
Command Code	6Bh	31h	3Fh	9Fh	D8h	10h	02h
Address Bytes	2	0	0	0	3	3	2
Dummy Bytes	1	0	0	1	0	0	0
Data Bytes	1 to 2112	1 to 2112	1 to 2112	2	0	0	1 to 2112
Actions	Output cache data on SI, SO, WP#, HOLD#	The next page data is transferred to buffer	The last page data is transferred to buffer	Read device ID	Block erase	Enter block/ page address, no data, execute	Load program data with cache reset first

Command Type	PROGRAM LOAD RANDOM DATA	WRITE ENABLE	WRITE DISABLE	PROGRAM LOAD x4	PROGRAM LOAD RANDOM DATA x4	RESET
Command Code	84h	06h	04h	32h	34h	FFh
Address Bytes	2	0	0	2	2	0
Dummy Bytes	0	0	0	0	0	0
Data Bytes	1 to 2112	0	0	1 to 2112	1 to 2112	0
Actions	Load program data without cache reset			Program Load operation with X4 data input	Program Load random data operation with X4 data input	Reset the device

深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

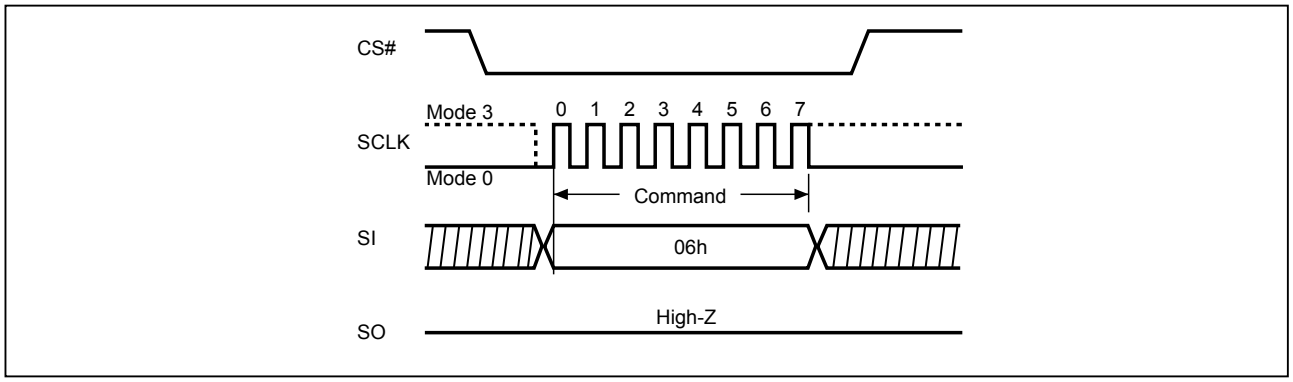
8-1. WRITE Operations

8-1-1. Write Enable

The Write Enable (WREN, 06h) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like Page Program, Secure OTP program, Block Erase, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

Figure 4. Write Enable (WREN) Sequence



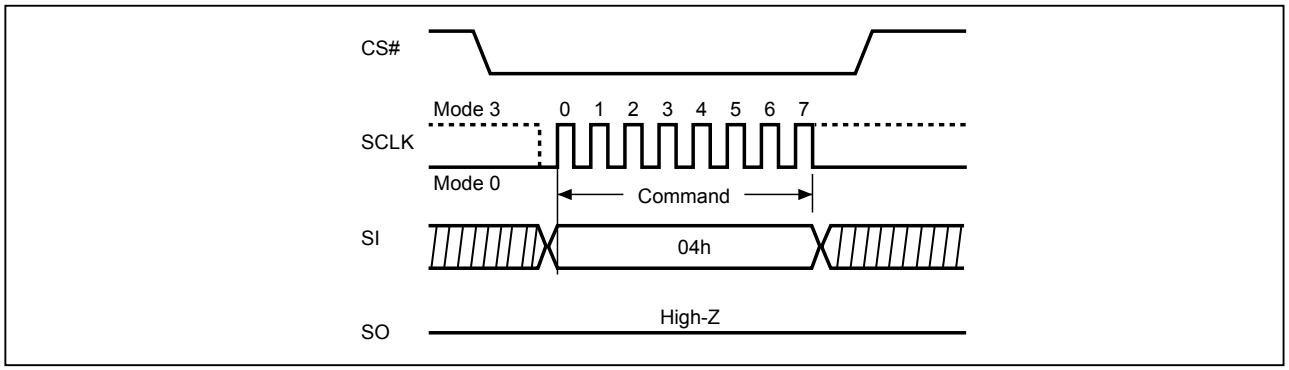
8-1-2. Write Disable (04h)

The Write Disable (WRDI, 04h) instruction is to reset Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high. It disables the following operations:

- Block Erase
- Secure OTP program
- Page program

Figure 5. Write Disable (WRDI) Sequence



深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

8-2. Feature Operations

8-2-1. GET Feature (0Fh) and SET Feature (1Fh)

By issuing a one byte address into the feature address, the device may then decide if it's a feature read or feature modification. (0Fh) is for the "GET FEATURE"; (1Fh) is for the "SET FEATURE".

The RESET command (FFh) will not clear the previous feature setting, the feature setting data bits remain until the power is being cycled or modified by the settings in the table below. After a RESET command (FFh) is issued, the Status register OIP bit0 will go high. This bit can be polled to determine when the Reset operation is complete, as it will return to the default value (0) after the reset operation is finished. Issuing the RESET command (FFh) has no effect on the Block Protection and Configuration registers.

The Block Protection and Configuration registers (except Secure OTP Protect bit) will return to their default state after a power cycle, and can also be changed using the Set Feature command. Issuing the Get Feature command to read the selected register value will not affect register content.

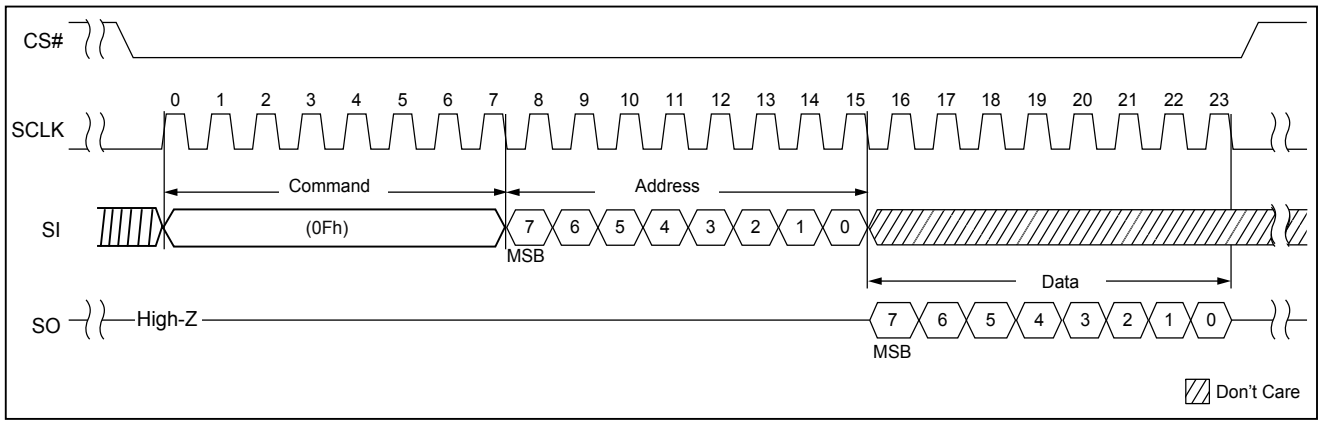
Table 2. Feature Settings

Register	Address	Data Bits							
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Configuration	B0h	Secure OTP Protect	Secure OTP Enable	Reserved	Reserved	Reserved(0)	Reserved	Reserved	QE
Status	C0h	Reserved	CRBSY	Reserved	Reserved	P_Fail	E_Fail	WEL	OIP
Block Protection	A0h	BPRWD[1]	Reserved	BP2	BP1	BP0	Invert	Complementary	SP[2]

Note 1: *If BPRWD is enabled and WP# is LOW, then the block protection register cannot be changed.*

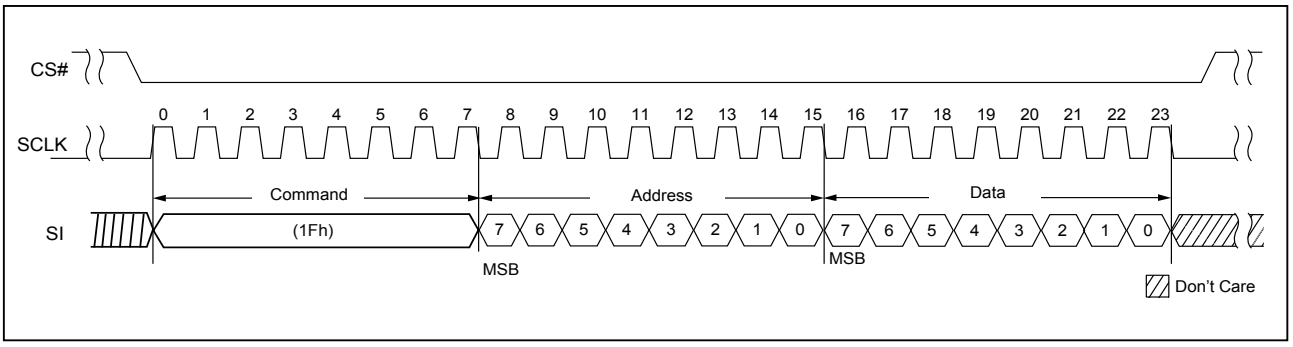
Note 2: *SP bit is for Solid-protection. Once the SP bit sets as 1, the rest of the protection bits (BPx bits, Invert bits, complementary bits) cannot be changed during the current power cycle.*

Figure 6. GET FEATURE (0Fh) Timing



深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

Figure 7. SET FEATURE (1Fh) Timing



8-3. READ Operations

The device supports "Power-on Read" function, after power up, the device will automatically load the data of the 1st page of 1st block from array to cache. The host micro-controller may directly read the 1st page of 1st block data from the cache buffer.

8-3-1. PAGE READ (13h)

The page read operation transfers data from array to cache by issuing the page read (13h)command followed by the 24-bit address (including the dummy/block/page address).

The device will have a period of time (tRD) being busy after the CS# goes high. The 0Fh (GET FEATURE) may be used to poll the operation status.

After read operation is completed, the RANDOM DATA READ (03H or 0Bh), Read from cache (x2) (3Bh), and Read from cache (x4) (6Bh) may be issued to fetch the data.

Wrap Read Operation

There are four wrap address bits which define the four wrap length as below table. After the Read from cache command (03h, 0Bh, 3Bh, 6Bh), setting the wrap address bits, and followed by the 12-bit column address to define the starting address. The starting address for wrap read only can be 0 - 2112. The data will be output from the starting address, once it reaches the end of the boundary of wrap length, the data will be wrap around the beginning starting wrap address until CS# goes high.

Table 3. Wrap Address bit Table

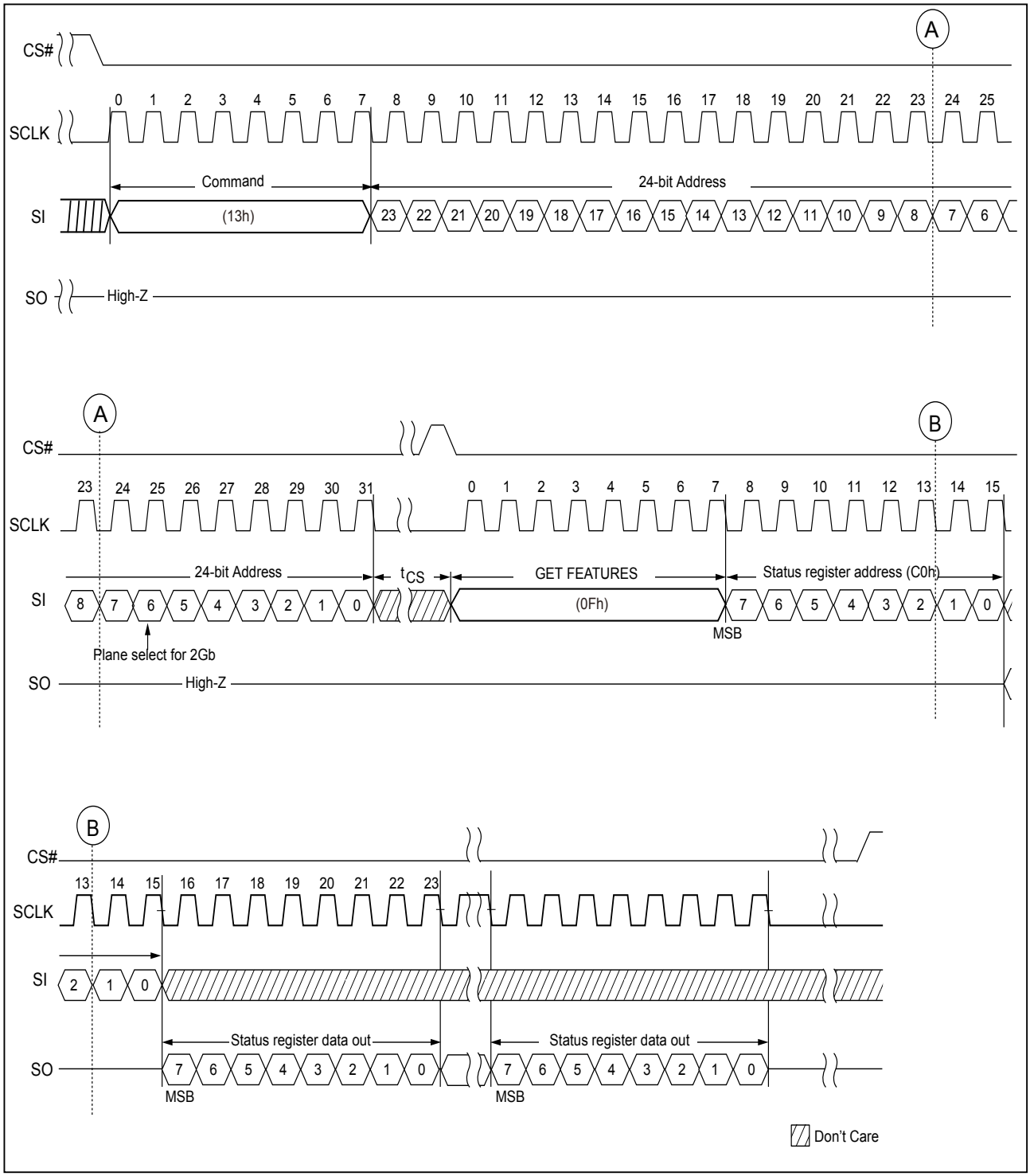
Wrap [1]	Wrap [0]	Wrap Length (byte)
0	0	2112
0	1	2048
1	0	64
1	1	16

8-3-2. QE bit

The Quad Enable (QE) bit, volatile bit, while it is "0" (factory default), it performs non-Quad and WP#, HOLD# are enabled. While QE is "1", it performs Quad I/O mode and WP#, HOLD# are disabled. In another word, if the system goes into four I/O mode (QE=1), the feature of Hardware Protection Mode(HPM) and HOLD will be disabled. Upon power cycle, the QE bit will go into the factory default setting "0".

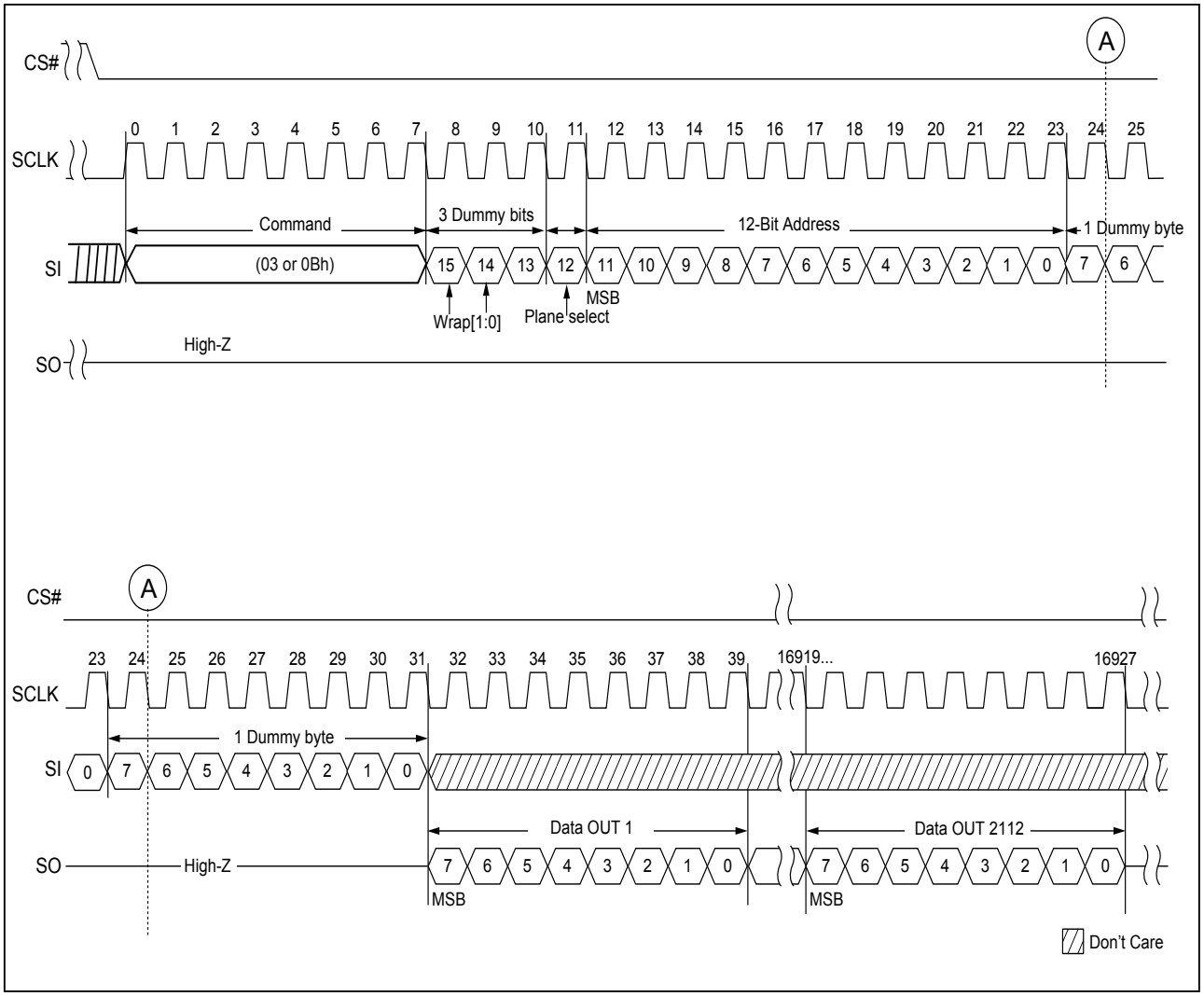
深圳市满度科技有限公司 Tel:139-1290-5940
Web:www.manduic.com Email:sales@manduic.com

Figure 8. PAGE READ (13h) Timing x1



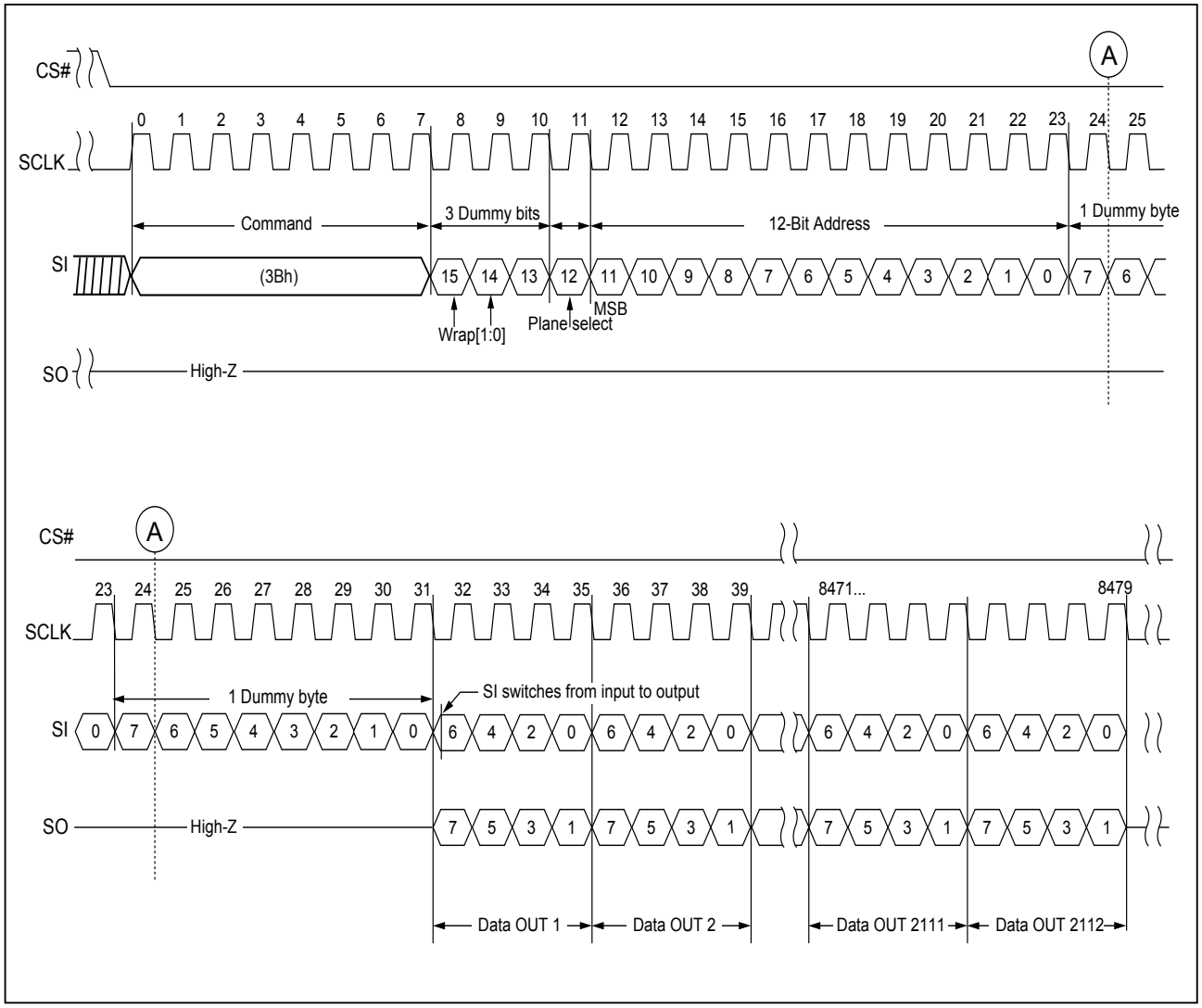
深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

Figure 9. RANDOM DATA READ (03h or 0Bh) Timing



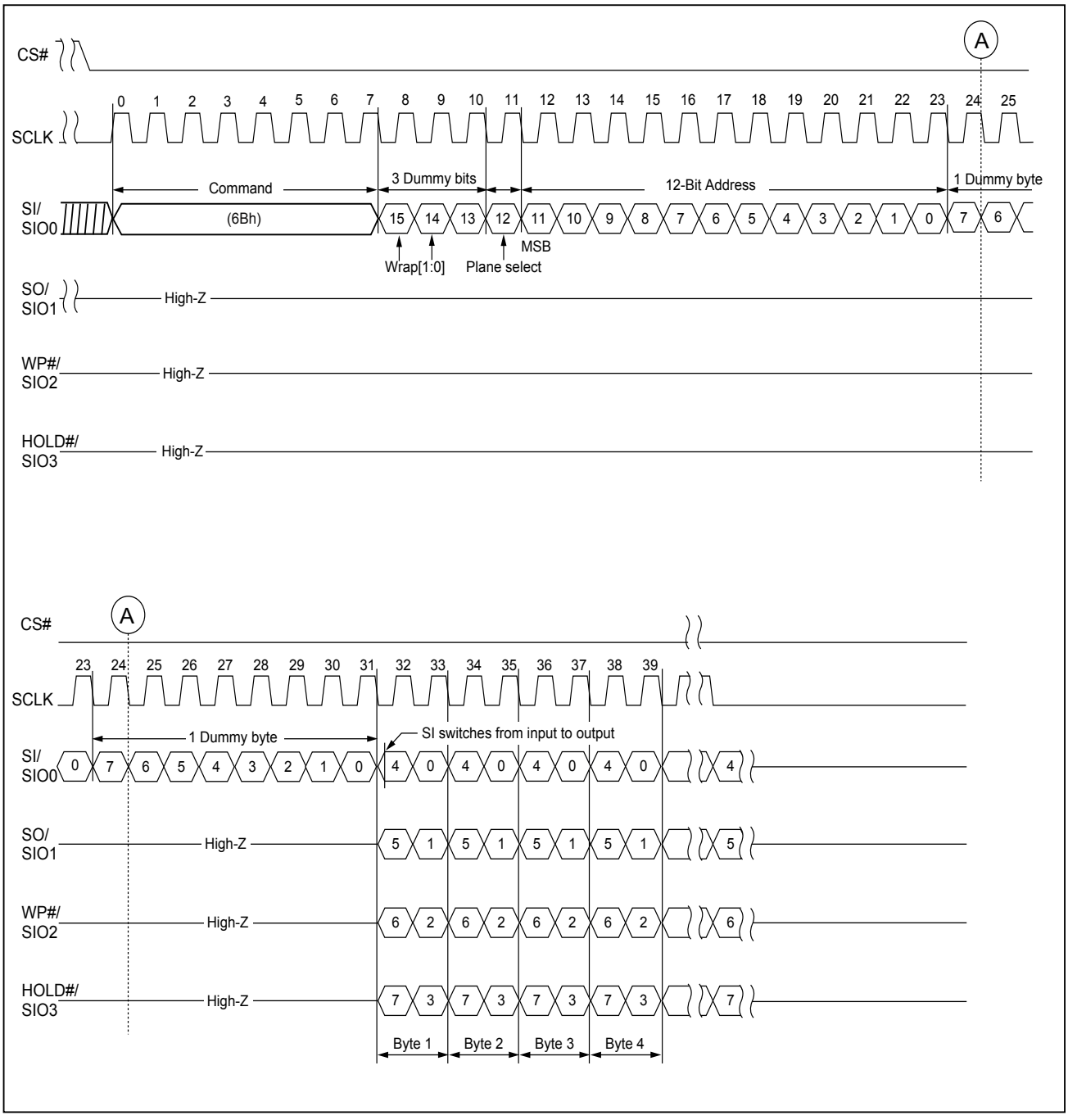
深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

Figure 10. READ FROM CACHE x 2



深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

Figure 11. READ FROM CACHE x 4



深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

8-3-3. Page Read Cache Sequential (31h) / Page Read Cache End (3Fh)

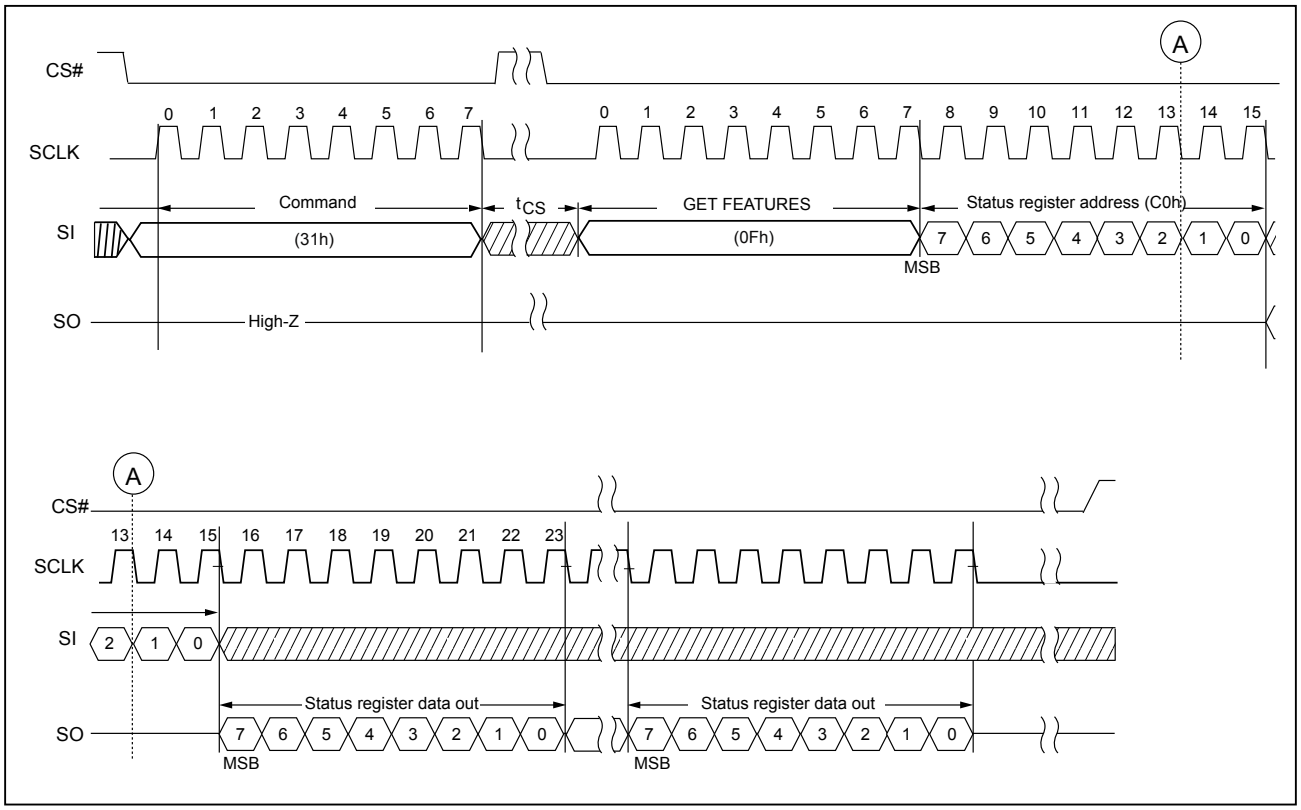
The page read cache sequential operation is for throughput enhancement by using the internal cache buffer. It allows the consecutive pages to be read-out without giving next page address, which reduces the latency time from tRD to tRCBSY between pages or blocks. While the data is read out on one page, the data of next page can be read into the cache buffer.

After writing the 13h command and giving the 24-bit address, the device will have a period of time (tRD) being busy after the CS# goes high. The 0Fh (GET FEATURE) may be used to poll the operation status. After the status of successfully completed, following the cache read sequential (31h) command being sent to NAND device; the NAND device will be at a busy time of tRCBSY for the next page data transferring to cache. And then following the cache read command (03h/0Bh/3Bh/6Bh) may get the prior page data output from cache at the same time.

To confirm the last page to be read-out during the cache read sequential operation, a 3Fh command is needed to replace the 31h command prior to the last data-out.

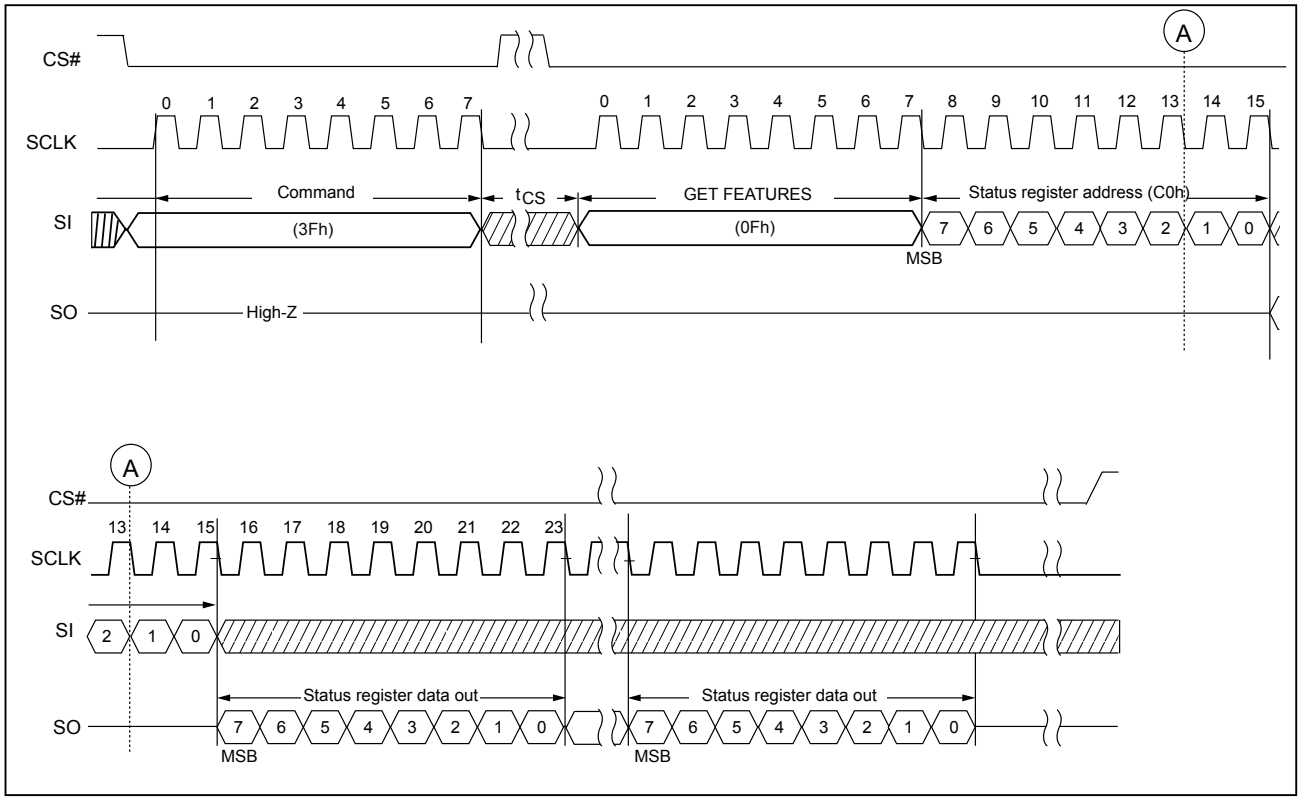
The PAGE READ CACHE SEQUENTIAL command is also valid for the consecutive page cross block.

Figure 12. Page Read Cache Sequential (31h)



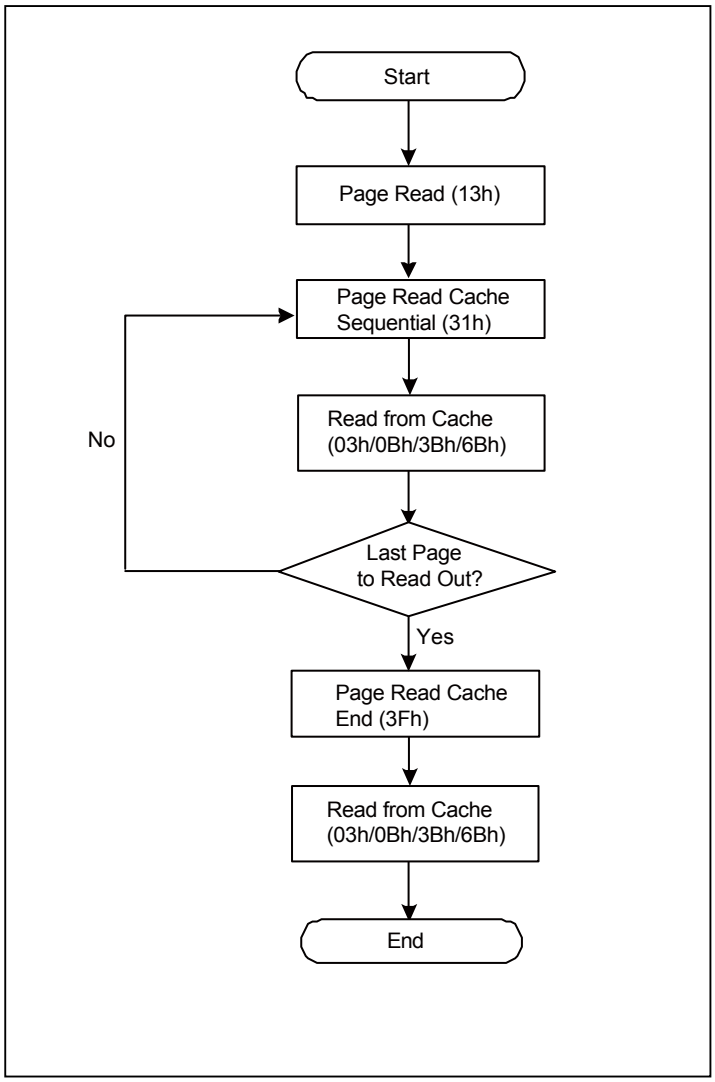
深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

Figure 13. Page Read Cache End (3Fh)



深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

Figure 14. Page Read Cache Flow



深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

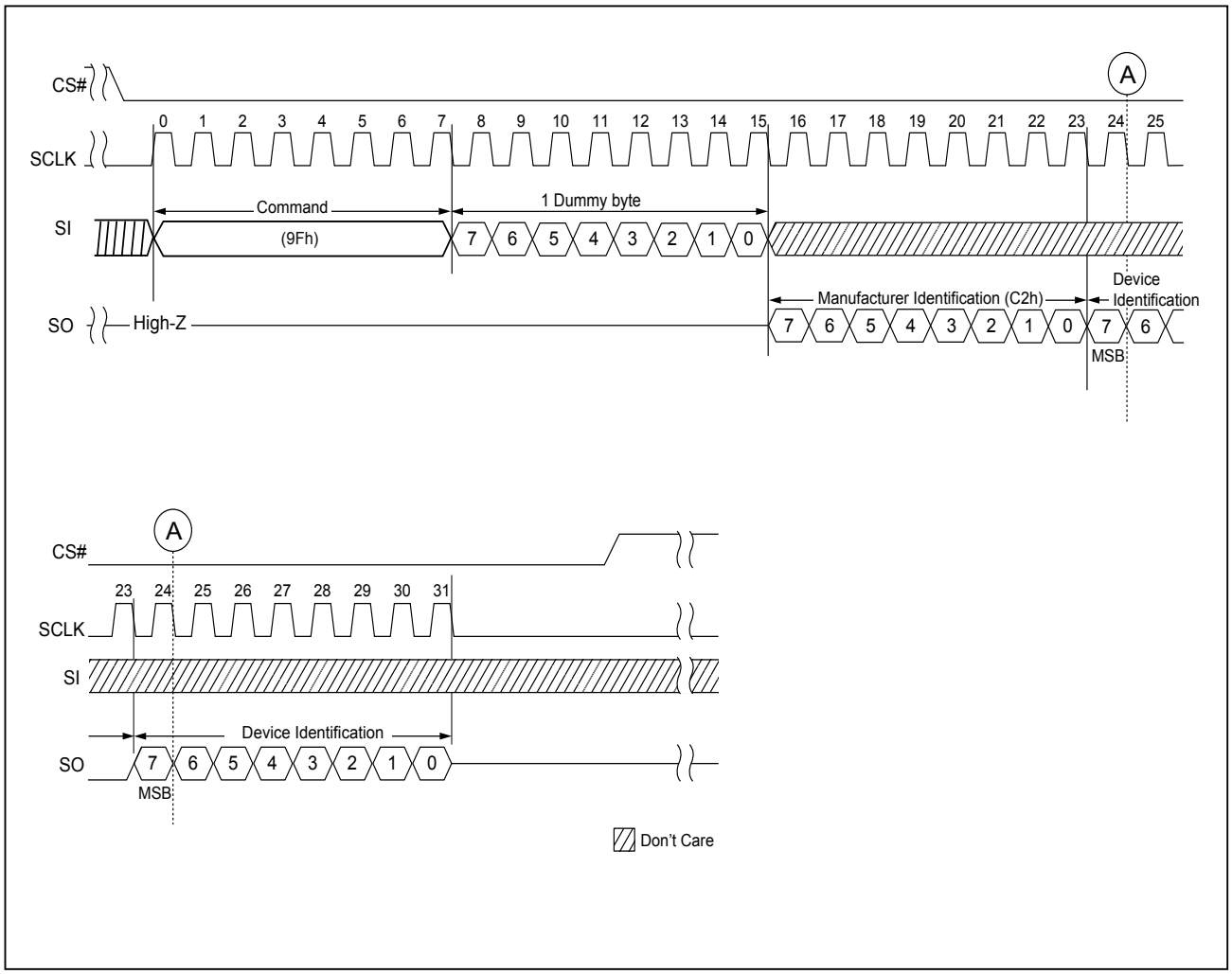
8-3-4. READ ID (9Fh)

The READ ID command is shown as the table below.

Table 4. READ ID Table

Byte	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value
Byte 0	Manufacturer ID (Macronix)	1	1	0	0	0	0	1	0	C2h
Byte 1	Device ID (Serial NAND)	0	0	1	0	0	0	0	0	20h

Figure 15. READ ID (9Fh) Timing



深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

8-4. Parameter Page

The parameter page is accessed by the following command flows:

Issue 1Fh (SET FEATURE) command with Secure OTP enable (B0h for address & 40h for data) → Issue 13h (PAGE READ) with 01h address, issue 0Fh (GET FEATURE) with C0h feature address to poll the status of read completion. → Issue 03h (READ FROM CACHE) with address A[11:0]=000h and read data → Issue 1Fh (SET FEATURE) with feature address B0h to disable Secure OTP feature (data byte = 00h) [exit parameter page read].

Table 5. Parameter Page Data Structure

	Revision Information and Features Block		
Byte#	**Description**		**Data**
0-3	Parameter Page Signature		4Fh, 4Eh, 46h, 49h
4-5	Revision Number		00h, 00h
6-7	Features Supported (N/A)		00h, 00h
8-9	Optional Commands Supported		06h, 00h
10-31	Reserved		00h
	Manufacturer Information Block		
Byte#	**Description**		**Data**
32-43	Device Manufacturer (12 ASCII characters)		4Dh, 41h, 43h, 52h, 4Fh, 4Eh, 49h, 58h, 20h, 20h, 20h, 20h
44-63	Device Model (20 ASCII Characters)	MX35LF2G14AC	4Dh, 58h, 33h, 35h, 4Ch, 46h, 32h, 47h, 31h, 34h, 41h, 43h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID		C2h
65-66	Date Code		00h, 00h
67-79	Reserved		00h

深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

Memory Organization Block			
Byte#	**Description**		**Data**
80-83	Number of Data Bytes per Page	2048-byte	00h, 08h, 00h, 00h
84-85	Number of Spare Bytes per Page	64-byte	40h, 00h
86-89	Number of Data Bytes per Partial Page	512-byte	00h, 02h, 00h, 00h
90-91	Number of Spare Bytes per Partial Page	16-byte	10h, 00h
92-95	Number of Pages per Block		40h, 00h, 00h, 00h
96-99	Number of Blocks per Unit		00h, 08h, 00h, 00h
100	Number of Logical Units		01h
101	Number of Address Cycles (N/A)		00h
102	Number of Bits per Cell		01h
103-104	Bad Blocks Maximum per unit		28h, 00h
105-106	Block endurance		01h, 05h
107	Guarantee Valid Blocks at Beginning of Target		01h
108-109	Block endurance for guaranteed valid blocks		00h, 00h
110	Number of Programs per Page		04h
111	Partial Programming Attributes		00h
112	Number of ECC bits		04h
113	Number of Interleaved Address Bits (N/A)		00h
114	Interleaved Operation Attributes (N/A)		00h
115-127	Reserved		00h
Electrical Parameters Block			
Byte#	**Description**		**Data**
128	I/O Pin Capacitance		0Ah
129-130	Timing Mode Support (N/A)		00h, 00h
131-132	Program Cache Timing (N/A)		00h, 00h
133-134	tPROG Maximum Page Program Time (uS)	600us	58h, 02h
135-136	BE Maximum Block Erase time (uS)	3500us	ACh, 0Dh
137-138	tRD Maximum Page Read time (uS)	25us	19h, 00h
139-140	tCCS Minimum (N/A)	0ns	00h, 00h
141-163	Reserved		00h
Vendor Blocks			
Byte#	**Description**		**Data**
164-165	Vendor Specific Revision Number		00h, 00h
166-253	Vendor Specific		00h
254-255	Integrity CRC		Set at Test ***(Note)***
Redundant Parameter Pages			
Byte#	**Description**		**Data**
256-511	Value of Bytes 0-255		Same as 0~255 Byte
512-767	Value of Bytes 0-255		Same as 0~255 Byte
768+	Additional Redundant Parameter Pages		

Note:
The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host. Please refer to ONFI 1.0 specifications for details.

The CRC shall be calculated using the following 16-bit generator polynomial:
$G(X) = X^{16} + X^{15} + X^2 + 1$

深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

8-5. UniqueID Page

The UniqueID page is accessed by the following command flows:

Issue 1Fh (SET FEATURE) command with Secure OTP enable (B0h for address & 40h for data) → Issue 13h (PAGE READ) with 00h address, issue 0Fh (GET FEATURE) with C0h feature address to poll the status of read completion → Issue 03h (READ FROM CACHE) with address A[11:0]=000h and read data → Issue 1Fh (SET FEATURE) with feature address B0h to disable Secure OTP function (data byte = 00h) [exit unique ID read].

UniqueID data: 16x32byte of UniqueID data. On each 32byte, the first 16byte and following 16byte should be XOR to be FFh.

深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

8-6. Program Operations

8-6-1. PAGE PROGRAM

With following operation sequences, the PAGE PROGRAM operation programs the page from byte 1 to byte 2112.

WRITE ENABLE (06h) → PROGRAM LOAD (02h) → PROGRAM LOAD RANDOM DATA (84h) if needed → PROGRAM EXECUTE (10h) → GET FEATUR from command to read status (0Fh).

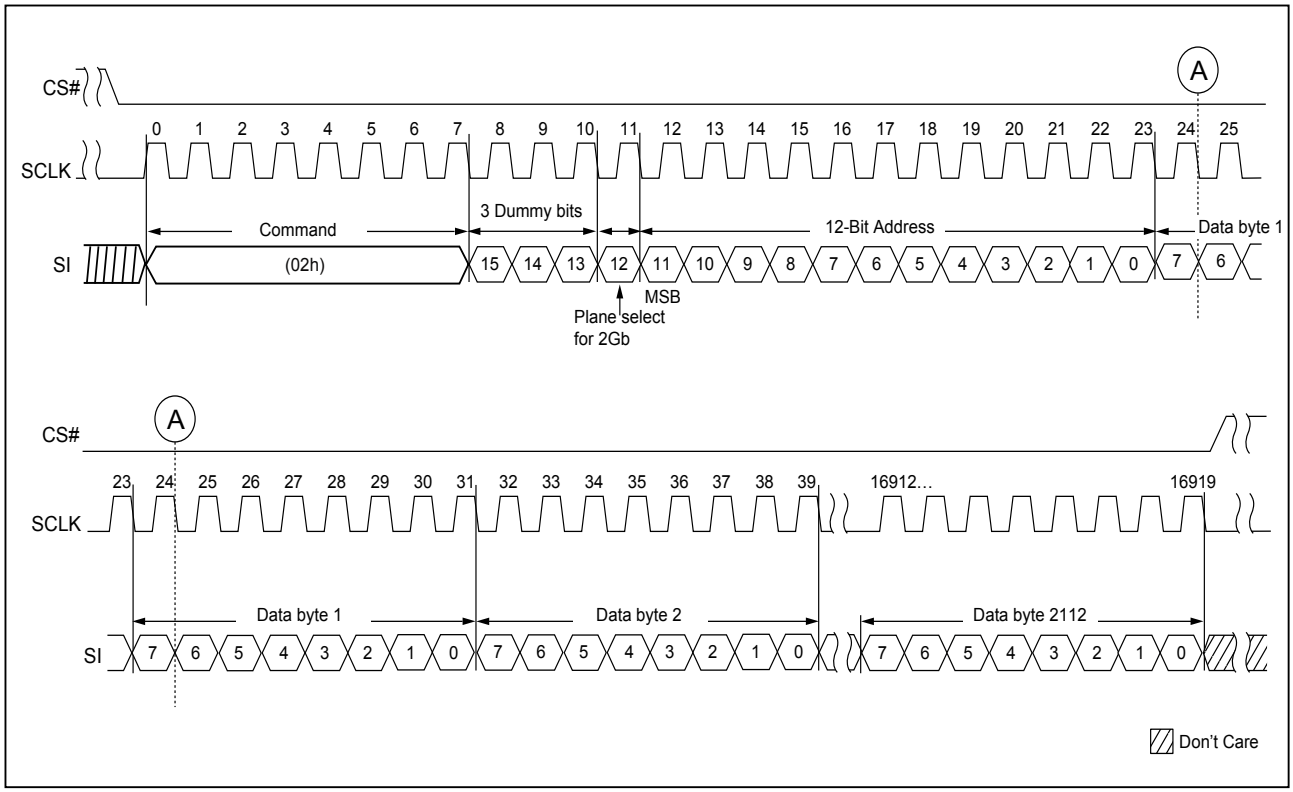
WEL bit is set with the WRITE ENABLE (06h) issued. The program operation will be ignored if 06h command not issued. In a single page, four partial page programs are allowed. Exceeded bytes (Page address is larger than 2112) for "PROGRAM LOAD" or "PROGRAM LOAD RANDOM DATA", the exceeding bytes will be ignored. When CS goes high, the "PROGRAM LOAD" or "PROGRAM LOAD RANDOM DATA" operation" terminates. Please note the figure below for PROGRAM LOAD.

After PROGRAM LOAD is done, the programming of data should be as following steps: issue 10h (PROGRAM EXECUTE) with 1byte command code, 24 bits address → code programming to memory and busy for tPROG → Program complete.

During programming, status to be polled by the status register.

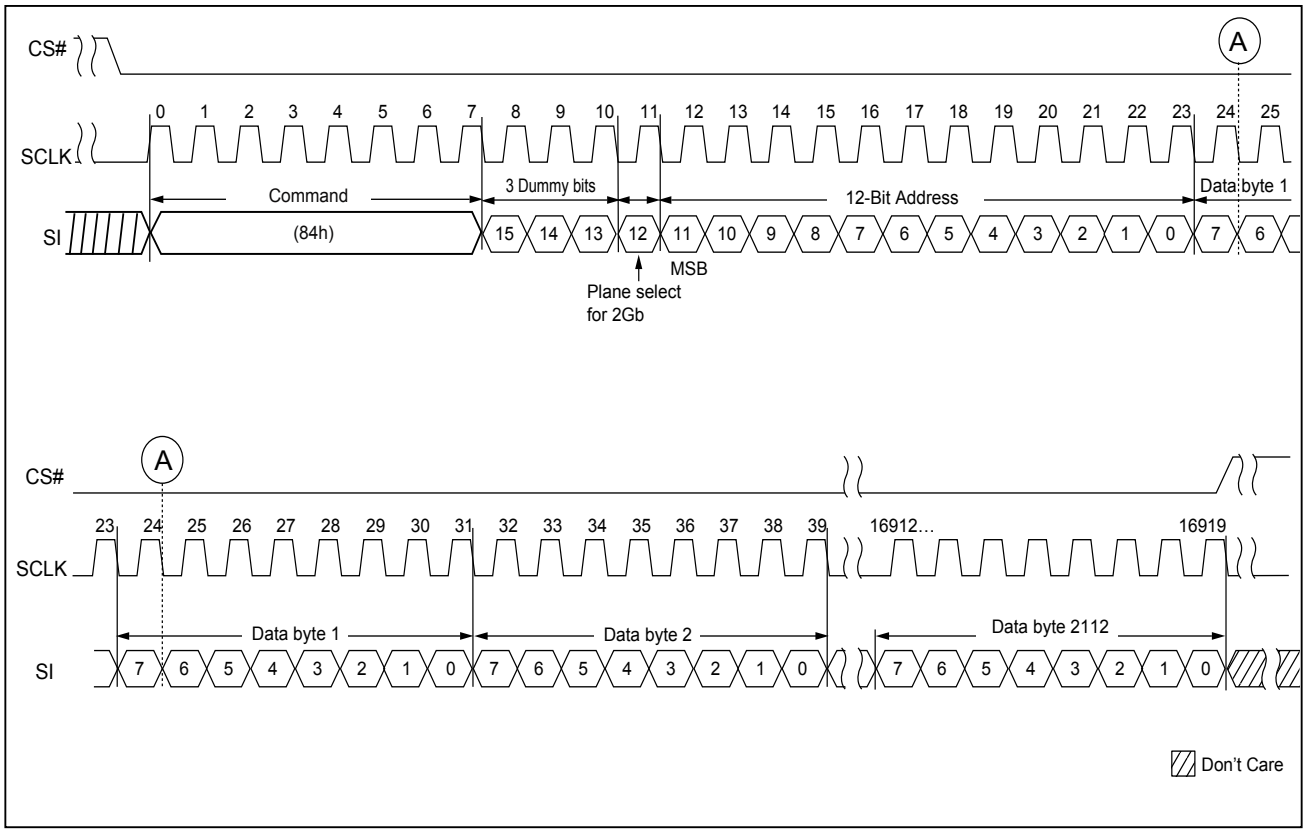
Operation shows in the Figure below.

Figure 16. PROGRAM LOAD (02h) Timing



深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

Figure 17. PROGRAM LOAD RANDOM DATA (84h) Timing

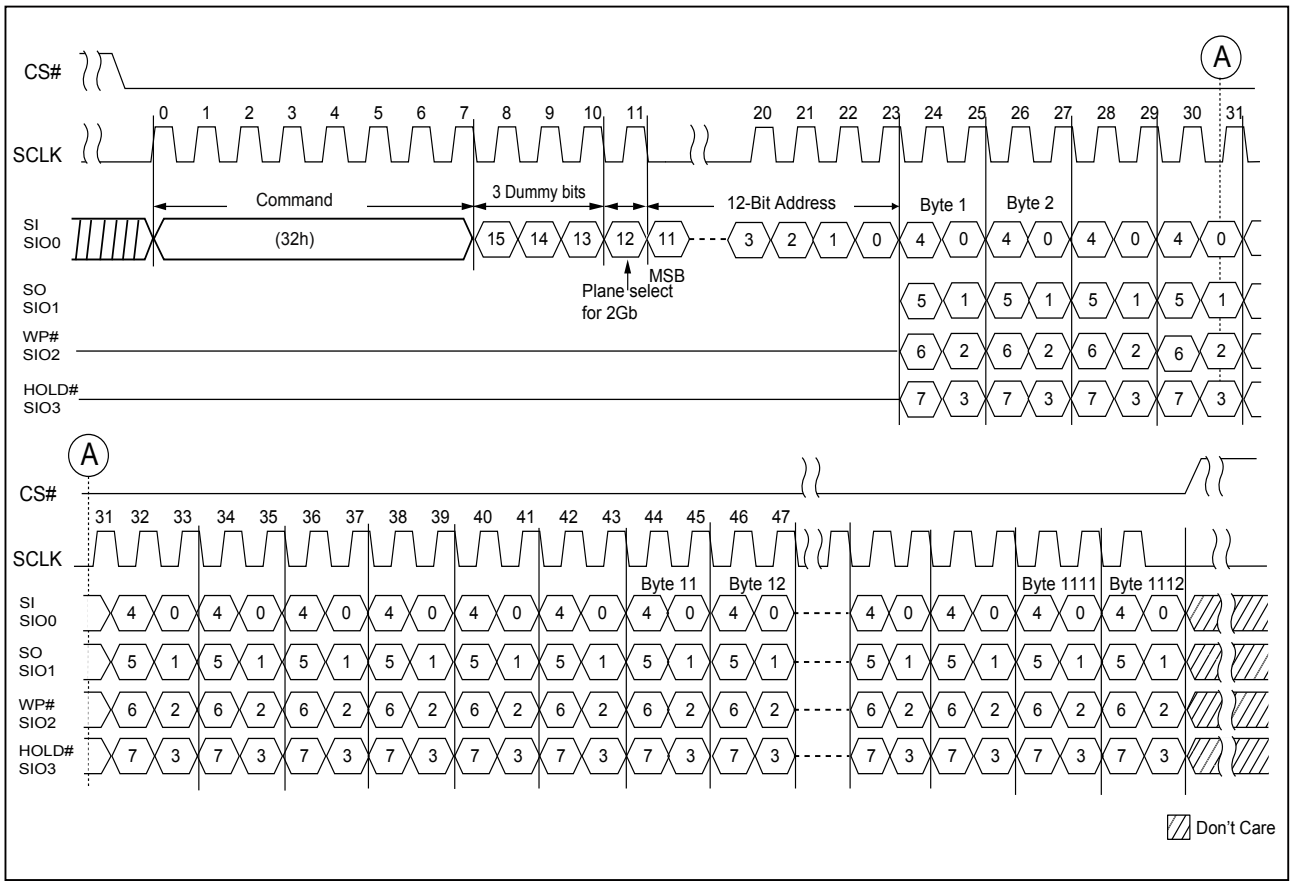


深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

8-6-2. QUAD IO PAGE PROGRAM

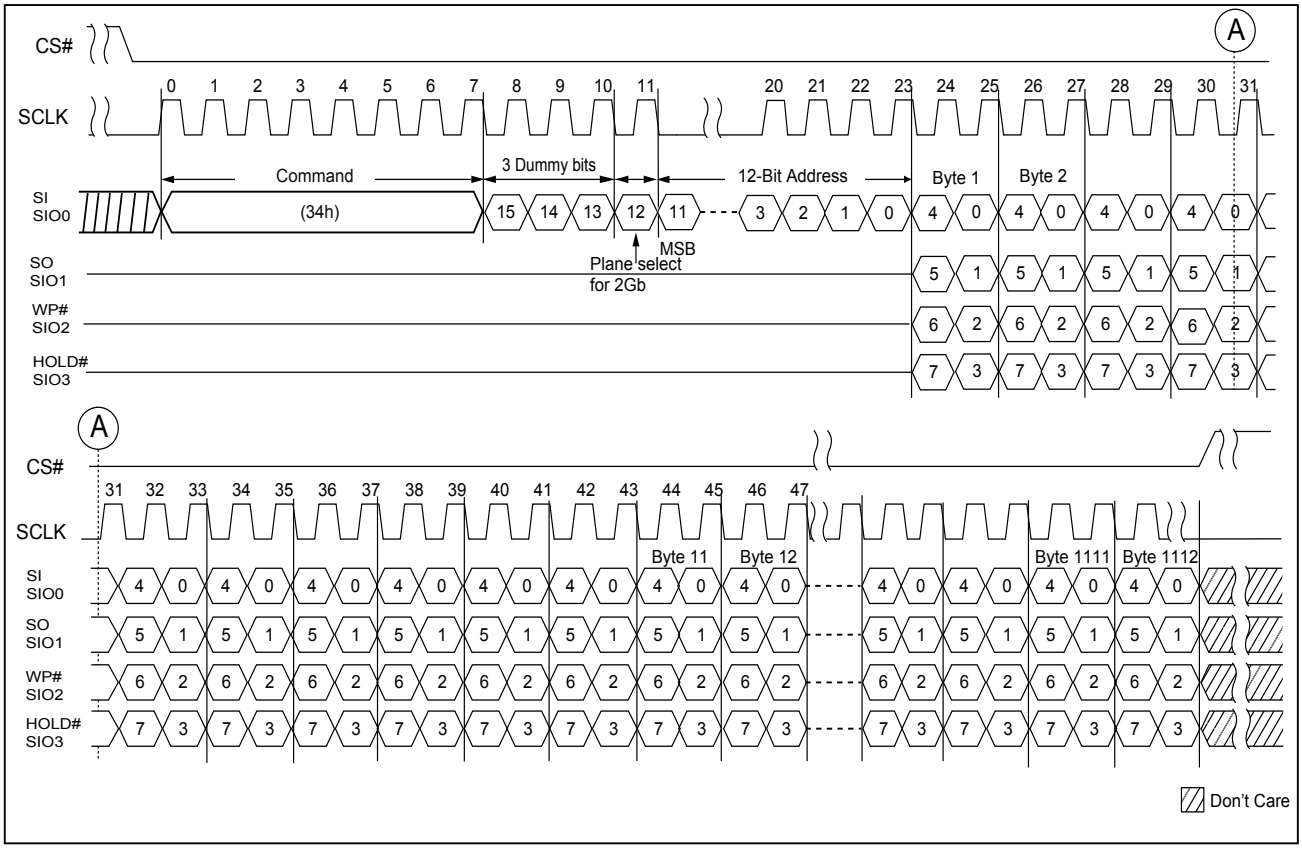
QUAD IO PAGE PROGRAM conducts the 2Kbyte program with 4 I/O mode. The steps are: WRITE ENABLE (06h) → PROGRAM LOAD X4 (32h) → PROGRAM LOAD RANDOM DATA (34h) if needed → PROGRAM EXECUTE (10h) → Poll status by issuing GET FEATURE (0Fh).

Figure 18. PROGRAM LOAD X4 (32h) Timing



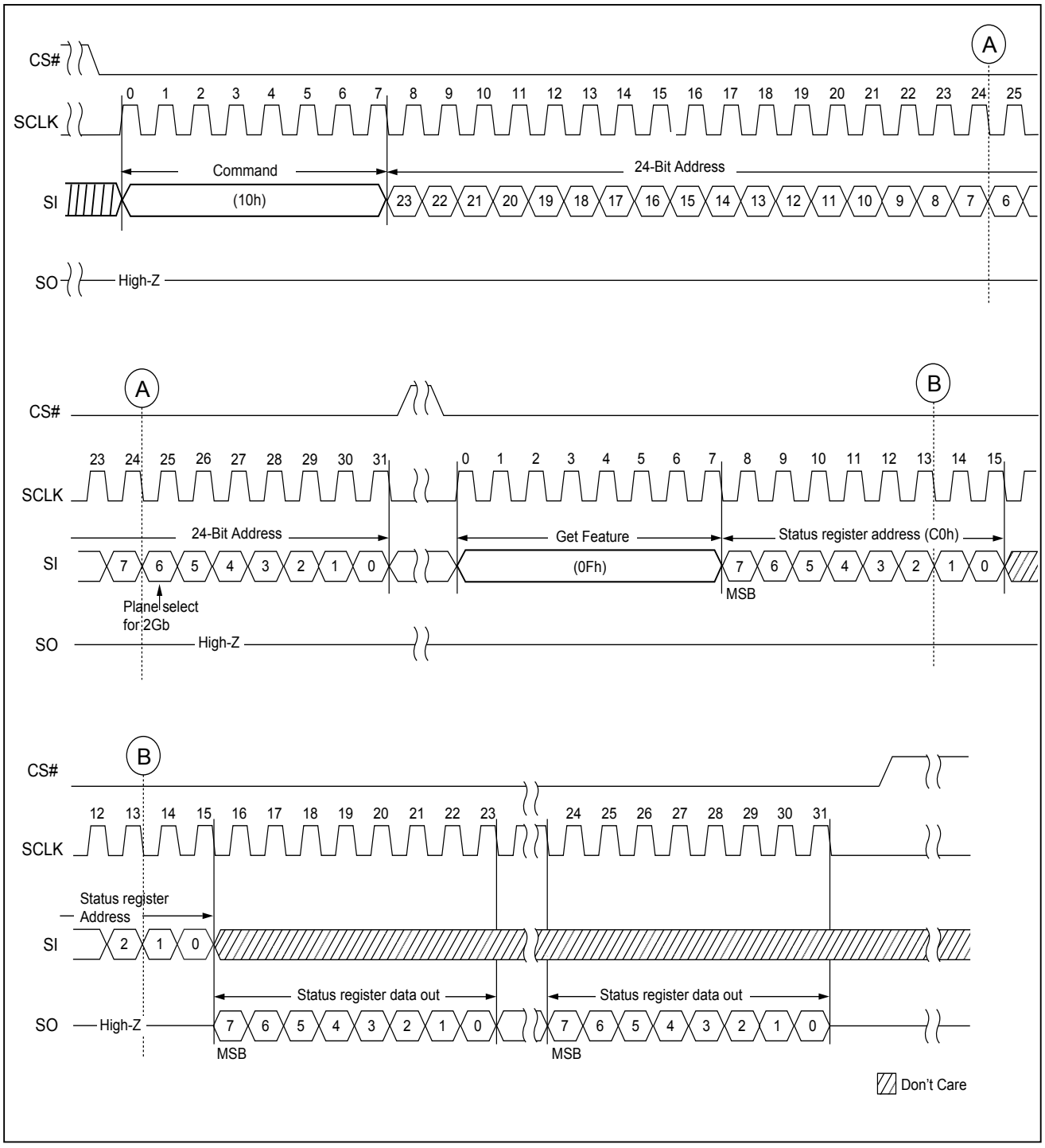
深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

Figure 19. QUAD IO PROGRAM RANDOM INPUT (34h) Timing



深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

Figure 20. PROGRAM EXECUTE (10h) Timing



深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

9. BLOCK OPERATIONS

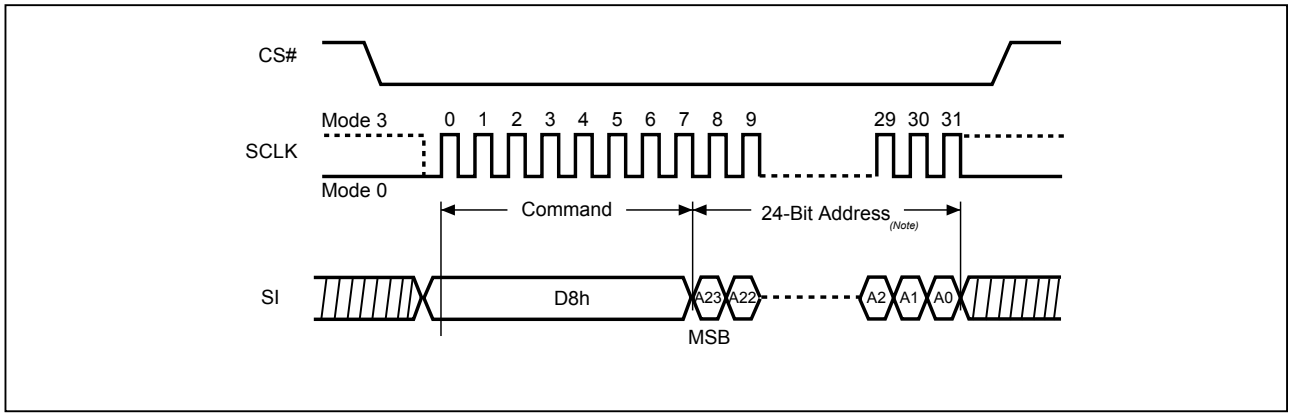
9-1. Block Erase (D8h)

The Block Erase (D8h) instruction is for erasing the data of the chosen block to be "1". The instruction is used for a block of 128K-byte erase operation. A Write Enable (WREN) instruction be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (D8h). Any address of the block is a valid address for Block Erase (D8h) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed. Finally, a Get Feature(0Fh) instruction to check the status is necessary.

The sequence of issuing Block Erase instruction is: CS# goes low→ sending Block Erase instruction code→ 24-bit address on SI→CS# goes high.

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Get Feature (0Fh) instruction with Address (C0h) may check the status of the operation during the Block Erase cycle is in progress (please refer to the Get Feature waveform and table of Feature Setting). The OIP bit is "1" during the tBE timing, and is cleared to "0" when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared.

Figure 21. Block Erase (BE) Sequence



Note: *The 24-bit Address includes: 17-bit row address and 7-bit dummy.*

深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

10. Feature Register

Feature register defines various register's definitions (Block Protection, Secure OTP, Status register). The definition of each register is defined in **"Table 6. Definition of Protection Bits"**.

10-1. Block Protection Feature

The Block Protection feature includes three block protection bits (BPx), Block Protection Register Write Disable (BPRWD). Inverse bit (INVERT), complement bit (COMPLEMENTARY) and Solid Protection Bit (SP).

Soft Protection Mode (SPM)

The SPM uses the BPx bits, INVERT, and COMPLEMENTARY bits to allow part of memory to be protected as read only. The protected area definition is shown as **"Table 6. Definition of Protection Bits"**. The protected areas are more flexible which may protect various area by setting value of BP0-BP2 and Invert bit, and Complementary bit. These are volatile bits and can be modified by set feature command.

After power-up, the chip is in protection state, that is, the feature bits BPx is 1, all other bits (BPRWD, INVERT, COMPLEMENTARY and SP) are 0. The Set feature instruction (1Fh) with feature address (A0h) may change the value of the block protection bits and un-protect whole chip or a certain area for further program/erase operation. For example, after the power-on, the whole chip is protected from program/erase operation, the top 1/64 area may be un-protected by using the Set feature instruction (1Fh) with the feature address (A0h) to change the values of BP2 and BP1 from "1" to "0" as below table of **"Block protection register bits"**

Hardware Protection Mode (HPM) & Solid Protection Mode (SDPM)

Under the Hardware Protection mode and Solid Protection Mode, the (BPx, INVERT, COMPLEMENTART) bits can not be changed.

Hardware Protection Mode: The device enters HPM if BPRWD bits is set to 1 and WP#/SIO2 is driven to 0.

Note 1: *HPM also requires SP bit to be 0 state .*

Note 2: *The Quad mode is not supported in HPM.*

Solid Protection Mode: If SP bit is set to 1, the device enters SDPM. After that, the selected block is solid protected and can not be un-protected until next power cycle.

深圳市满度科技有限公司 Tel:+86-1290-5940
Web:www.manduic.com Email:sales@manduic.com

Table 6. Definition of Protection Bits

BP2	BP1	BP0	Invert	Complementary	Protection Area
0	0	0	x	x	all unlocked
0	0	1	0	0	upper 1/64 locked
0	1	0	0	0	upper 1/32 locked
0	1	1	0	0	upper 1/16 locked
1	0	0	0	0	upper 1/8 locked
1	0	1	0	0	upper 1/4 locked
1	1	0	0	0	upper 1/2 locked
1	1	1	x	x	all locked (default)
0	0	1	1	0	lower 1/64 locked
0	1	0	1	0	lower 1/32 locked
0	1	1	1	0	lower 1/16 locked
1	0	0	1	0	lower 1/8 locked
1	0	1	1	0	lower 1/4 locked
1	1	0	1	0	lower 1/2 locked
0	0	1	0	1	lower 63/64 locked
0	1	0	0	1	lower 31/32 locked
0	1	1	0	1	lower 15/16 locked
1	0	0	0	1	lower 7/8 locked
1	0	1	0	1	lower 3/4 locked
1	1	0	0	1	block 0
0	0	1	1	1	upper 63/64 locked
0	1	0	1	1	upper 31/32 locked
0	1	1	1	1	upper 15/16 locked
1	0	0	1	1	upper 7/8 locked
1	0	1	1	1	upper 3/4 locked
1	1	0	1	1	block0

Note: *Block #0 is at lower portion.*

深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

10-2. Secure OTP (One-Time-Programmable) Feature

There is an Secure OTP area which has 30 full pages (30 x 2112-byte) from page 02h to page 1Fh guarantee to be good for system device serial number storage or other fixed code storage. The Secure OTP area is a non-erasable and one-time-programmable area, which is default to “1” and allows partial page program to be “0”, once the Secure OTP protection mode is set, the Secure OTP area becomes read-only and cannot be programmed again.

The Secure OTP operation is operated by the Set Feature instruction with feature address (B0h) to access the Secure OTP operation mode and Secure OTP protection mode.

To check the NAND device is ready or busy in the Secure OTP operation mode, the status register bit 0 (OIP bit) may report the status by Get Feature command operation.

To exit the Secure OTP operation or protect mode, it can be done by writing "0" to both Bit7 (Secure OTP protect bit) and bit6 (Secure OTP enable bit) for returning to the normal operation.

Secure OTP Read

1. Issuing the Set Feature instruction (1Fh)
2. Sending the Feature address (B0h) and set the "Secure OTP Enabled Bit" as "1".
3. Issuing normal Page Read command (13h)

Secure OTP Program (if the "Secure OTP Protection Bit" is "0") for

1. Issuing the Set Feature instruction (1Fh)
2. Sending the Feature address (B0h) and set the "Secure OTP Enabled Bit" as "1".
3. Issuing Page Program command (02h)
4. Issuing program execute command (10h)

Secure OTP Protection

1. Issuing the Set Feature instruction (1Fh)
2. Sending the Feature address (B0h) and set both the "Secure OTP Protection Bit" and "Secure OTP Enabled Bit" as "1".
3. Issuing program execute command (10h)

Table 7. Secure OTP States

Secure OTP Protection Bit[Note1]	Secure OTP Enabled Bit	State
0	0	Normal operation
0	1	Access the Secure OTP for reading or programming
1	0	Not applicable
1	1	Secure OTP Protection by using the Program Execution command (10h)[Note2]

Note 1. *OTP protection bit is non-volatile.*

Note 2. *Once the "Secure OTP Protection Bit" and "Secure OTP Enabled Bit" are set as "1", the secure OTP becomes read only.*

深圳市满度科技有限公司 Tel:+86-1290-5940
Web:www.manduic.com Email:sales@manduic.com

10-3. Status Register

The MX35LF2G14AC provides a status register that outputs the device status by writing a Get Feature command (0Fh) with the feature address (C0h), and then the IO pins output the status.

The Get Feature (0Fh) command with the feature address(C0h) will keep the device at the status read mode unless next valid command is issued. The resulting information is outlined in the table below.

Table 8. Status Register Bit Descriptions

SR Bit	Bit Name	Description
SR[0] (OIP)	Operation in progress	The bit value indicates whether the device is busy in operations of read/ program execute/ erase/ reset command. 1: Busy, 0: Ready
SR[1] (WEL)	Write enable latch	The bit value indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, and then the device can accept program/ erase/write status register instruction. 1: write enable, 0: not write enable The bit value will be cleared (as "0") by issuing Write Disable command(04h).
SR[2] (ERS_Fail)	Erase fail	The bit value shows the status of erase failure or if host erase any invalid address or protected area (including protected blocks or protected Secure OTP area). 0: Passed, 1: Failed The bit value will be cleared (as "0") by RESET command or at the beginning of the block erase command operation.
SR[3] (PGM_Fail)	Program fail	The bit value shows the status of program failure or if host program any invalid address or protected area (including protected blocks or protected Secure OTP area). 0: Passed, 1: Failed The bit value will be cleared (as "0") by RESET command or during the program execute command operation.
SR[5:4]	Reserved	
SR[6] (CRBSY)	Cache Status Bit	The bit value indicates whether the internal cache is busy in Page Read Cache Sequential command. 1: Busy- internal cache is busy on data transfer 0: Ready- device is ready for cache data out
SR[7]	Reserved	

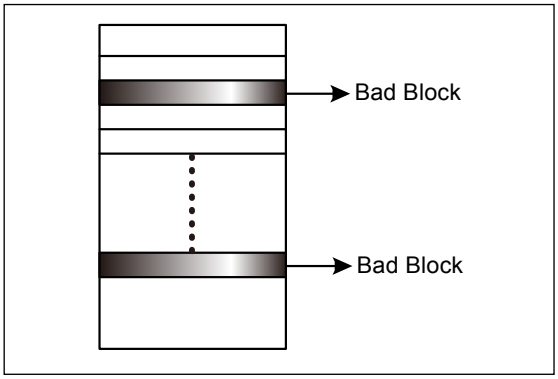
深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

11. SOFTWARE ALGORITHM

11-1. Invalid Blocks (Bad Blocks)

The bad blocks are included in the device while it gets shipped. During the time of using the device, the additional bad blocks might be increasing; therefore, it is necessary to check the bad block marks and avoid using the bad blocks. Furthermore, please read out the bad block information before any erase operation since the bad block marks may be cleared by any erase operation.

Figure 22. Bad Blocks



While the device is shipped, the value of all data bytes of the good blocks are FFh. The 1st byte of the 1st and 2nd page in the spare area for bad block will be 00h. The erase operation at the bad blocks is not recommended.

After the device is installed in the system, the bad block checking is recommended. **"Figure 23. Bad Block Test Flow"** shows the brief test flow by the system software managing the bad blocks while the bad blocks were found. When a block gets damaged, it should not be used any more.

Due to the blocks are isolated from bit-line by the selected gate, the performance of good blocks will not be impacted by bad ones.

Table 9. Valid Blocks

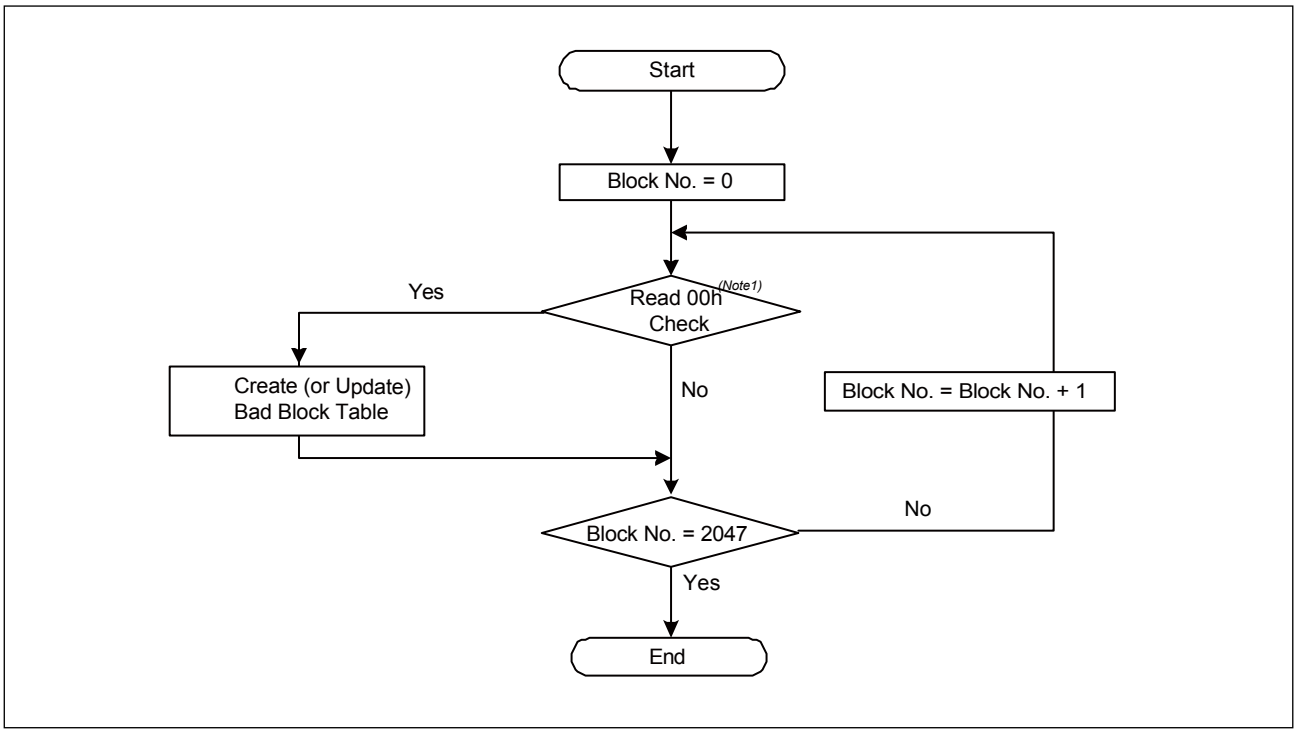
	Density	Min.	Typ.	Max.	Unit	Remark
Valid (Good) Block Number	2Gb	2008		2048	Block	Block 0 is guaranteed to be good (with ECC).

深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

11-2. Bad Block Test Flow

Although the initial bad blocks are marked by the flash vendor, they could be inadvertently erased and destroyed by a user that does not pay attention to them. To prevent this from occurring, it is necessary to always know where any bad blocks are located. Continually checking for bad block markers during normal use would be very time consuming, so it is highly recommended to initially locate all bad blocks and build a bad block table and reference it during normal NAND flash use. This will prevent having the initial bad block markers erased by an unexpected program or erase operation. Failure to keep track of bad blocks can be fatal for the application. For example, if boot code is programmed into a bad block, a boot up failure may occur. **"Figure 23. Bad Block Test Flow"** shows the recommended flow for creating a bad block table.

Figure 23. Bad Block Test Flow



Note 1: *Read 00h check is at the 1st byte of the 1st and 2nd pages of the block spare area.*

11-3. Failure Phenomena for Read/Program/Erase Operations

The device may fail during a Read, Program or Erase operation. The following possible failure modes should be considered when implementing a highly reliable system:

Table 10. Failure Modes

Failure Mode	Detection and Countermeasure	Sequence
Erase Failure	Status Read after Erase	Block Replacement
Programming Failure	Status Read after Program	Block Replacement
Read Failure	Read Failure	ECC

深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

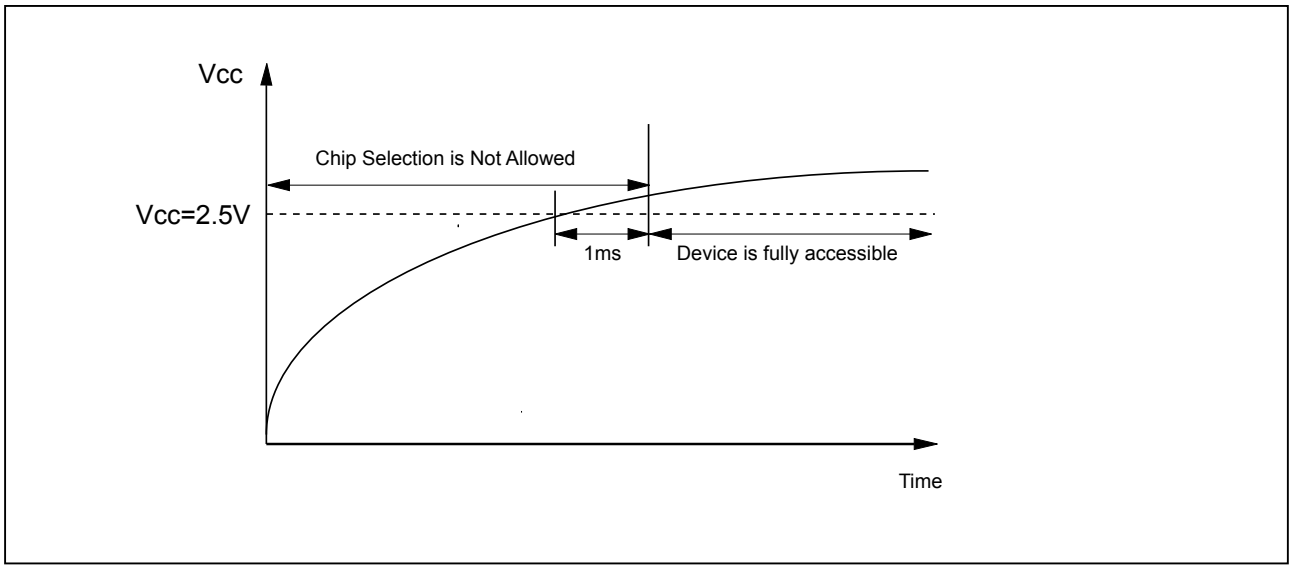
12. DEVICE POWER-UP

12-1. Power-up

After the Chip reaches the power on level, the internal power on reset sequence will be triggered. During the internal power on reset period, no any external command is accepted. The device can be fully accessible when VCC reaches the power-on level and wait 1ms.

During the power on and power off sequence, it is necessary to keep the WP# = Low for internal data protection.

Figure 24. Power On Sequence



深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

13. PARAMETERS

13-1. ABSOLUTE MAXIMUM RATINGS

Temperature under Bias	-50°C to +125°C
Storage temperature	-65°C to +150°C
All input voltages with respect to ground (Note 2)	-0.6V to 4.6V
VCC supply voltage with respect to ground (Note 2)	-0.6V to 4.6V
ESD protection	>2000V

Notes:

1. The reliability of device may be impaired by exposing to extreme maximum rating conditions for long range of time.

2. Permanent damage may be caused by the stresses higher than the "Absolute Maximum Ratings" listed.

3. During voltage transitions, all pins may overshoot Vss to -2.0V and Vcc to +2.0V for periods up to 20ns, please refer to **"Figure 25. Maximum Negative Overshoot Waveform"** *and* **"Figure 26. Maximum Positive Overshoot Waveform"**.

Figure 25. Maximum Negative Overshoot Waveform

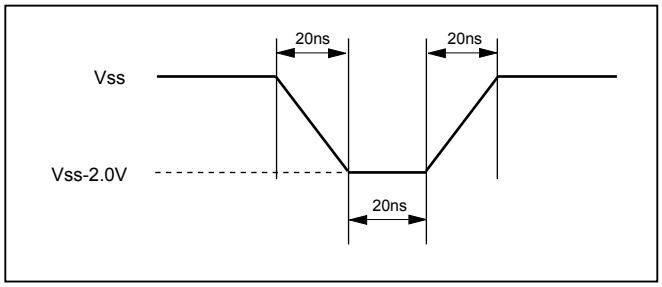


Figure 26. Maximum Positive Overshoot Waveform

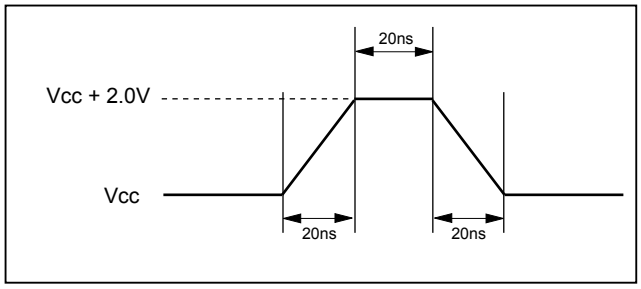


Table 11. AC Testing Conditions

Testing Conditions	Value	Unit
Input pulse level	0 to VCC	V
Output load capacitance	1TTL+CL(30)	pF
Input rising & falling time	5	ns
Input timing measurement reference levels	VCC/2	V
Output timing measurement reference levels	VCC/2	V

Table 12. Capacitance

TA = +25°C, F = 1 MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
CIN	Input capacitance			6	pF	VIN = 0V
COUT	Output capacitance			8	pF	VOUT = 0V

Note: *CIN/COUT=10pF/10pF for 2Gb*

Table 13. Operating Range

Temperature	VCC	Tolerance
-40°C to + 85°C	+3.3V	2.7 - 3.6V

深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

Table 14. DC Characteristics

Symbol	Parameter	Min.	Typical	Max.	Unit	Test Conditions
ILI	Input leakage current			+/- 10	uA	VIN= 0 to VCC Max.
ILO	Output leakage current			+/- 10	uA	VOUT= 0 to VCC Max.
ISB	VCC standby current (CMOS)		15	50	uA	VIN=VCC or GND, CS#=VCC
ICC1	VCC active current (Sequential Read)		15	30	mA	f=104MHz
ICC2	VCC active current (Program)		15	30	mA	
ICC3	VCC active current (Erase)		15	30	mA	
VIL	Input low level	-0.3		0.2VCC	V	
VIH	Input high level	0.8VCC		VCC + 0.3	V	
VOL	Outout low voltage			0.2	V	IOL= -1mA
VOH	Outout high voltage	VCC-0.2			V	IOH= -20uA

Table 15. General Timing Characteristics

Symbol	Parameter	Min.	Max.	Unit
fC	Clock Frequency	-	104	MHz
tCHHH	HOLD# high hold time relative to SCLK	5	-	ns
tCHHL	HOLD# low hold time relative to SCLK	5	-	ns
tCS	Command diselect time	100	-	ns
tCHSH	Chip select# hold time	4	-	ns
tSLCH	Chip select# setup time	4	-	ns
tSHCH	Chip select# non-active setup time	4		ns
tCHSL	Chip select# non-active hold time	4		ns
tDIS	Output disable time	-	20	ns
tHC	Hold# non-active setup time relative to SCLK	5	-	ns
tHD	Hold# setup time relative to SCLK	5	-	ns
tHDDAT	Data input hold time	3.5	-	ns
tHO	Output hold time	1	-	ns
tHZ	Hold to output High-Z	-	15	ns
tLZ	Hold to output low-Z	-	15	ns
tSUDAT	Data input setup time	3.5	-	ns
tV	Clock LOW to output Valid	-	8	ns
tWH	Clock HIGH time	4	-	ns
tWL	Clock LOW time	4	-	ns
tWPH	WP# hold time	100	-	ns
tWPS	WP# setup time	20	-	ns

Table 16. PROGRAM/READ/ERASE Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRD	Data transfer time from NAND Flash array to data register.		-	25	us
tRCBSY	Dummy busy time for data read sequential	-	3.5	25	us
tRST	Device reset time (Read/ Program/ Erase)			5/10/500	us
tPROG	Page programming time		300	600	us
tERS	Block Erase Time		1	3.5	ms
NOP	Number of partial-page programming operation supported			4	cycle

深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

Figure 27. WP# Setup Timing and Hold Timing during SET FEATURE when BPRWD=1

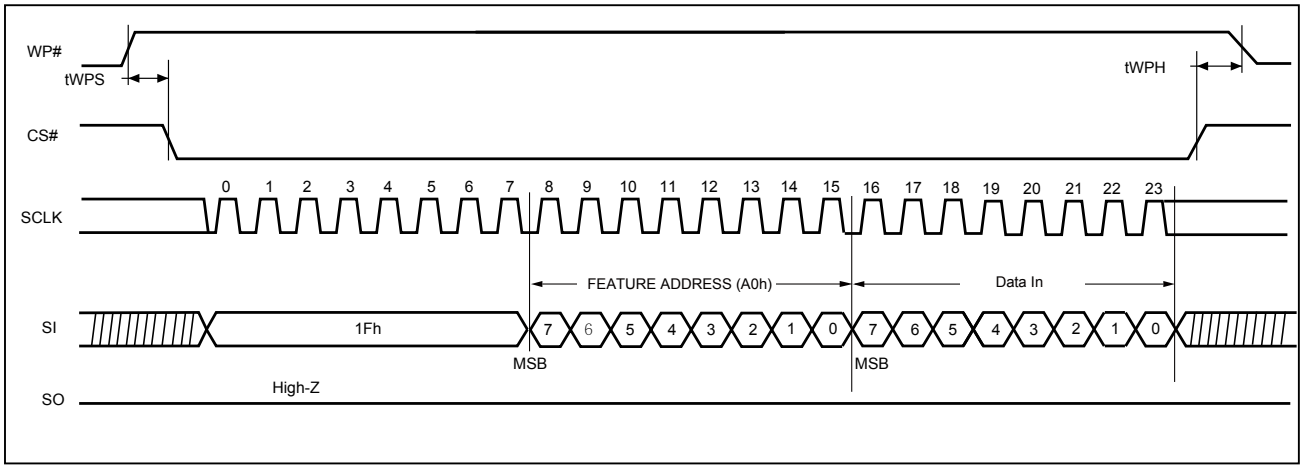


Figure 28. Serial Input Timing

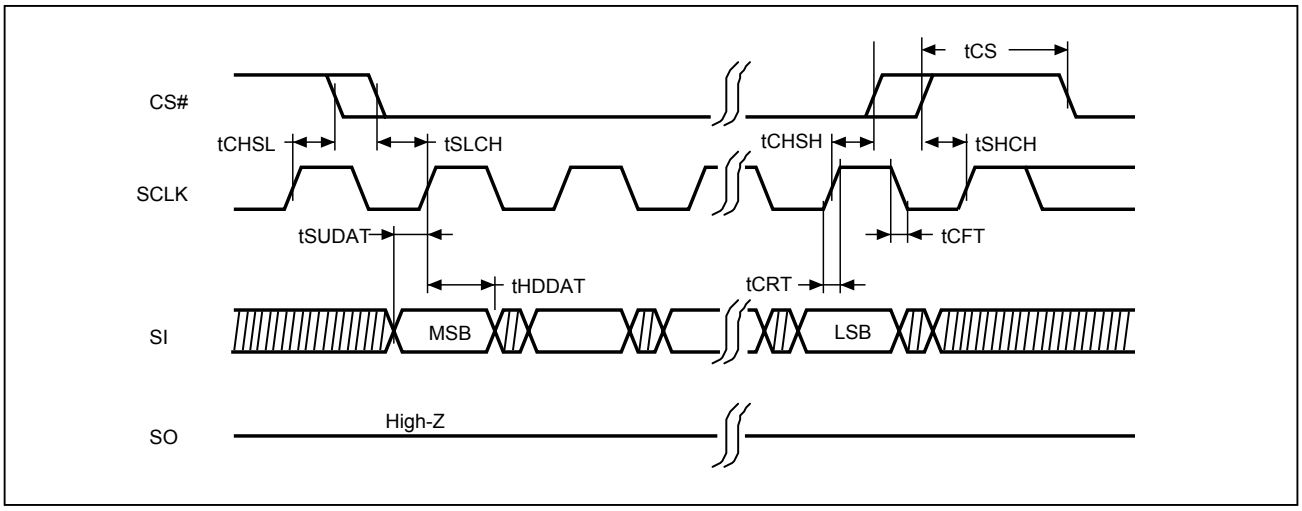
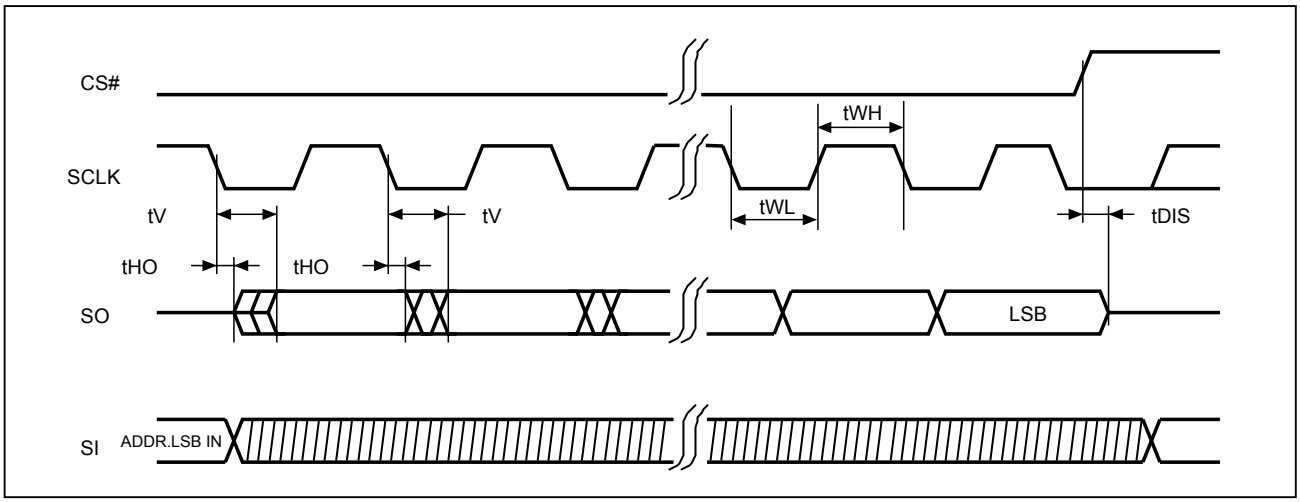
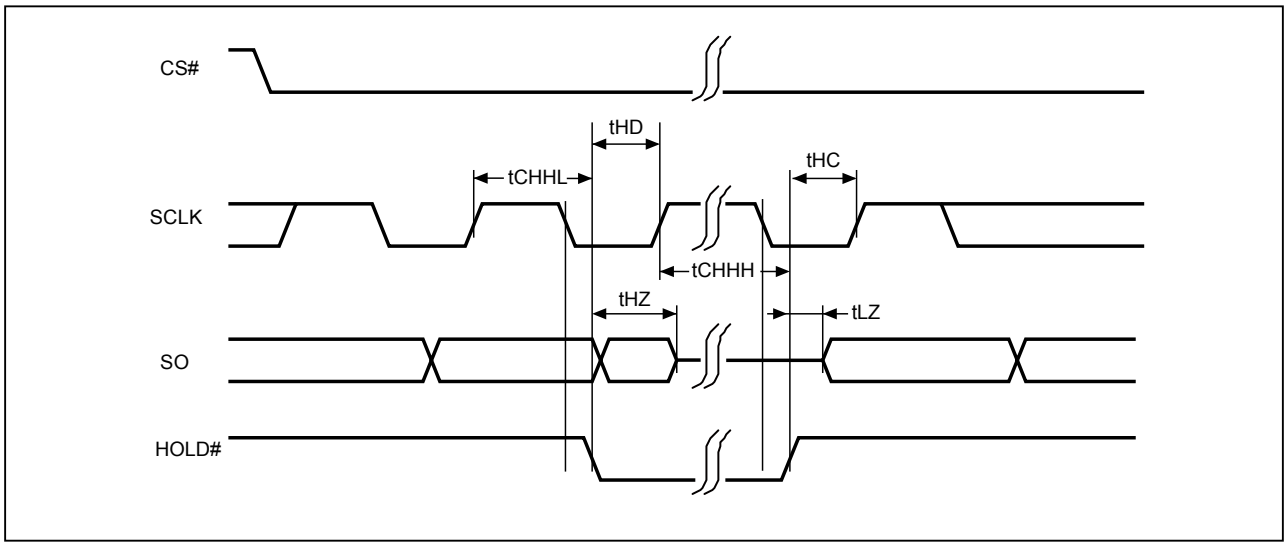


Figure 29. Serial Output Timing



深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

Figure 30. Hold Timing



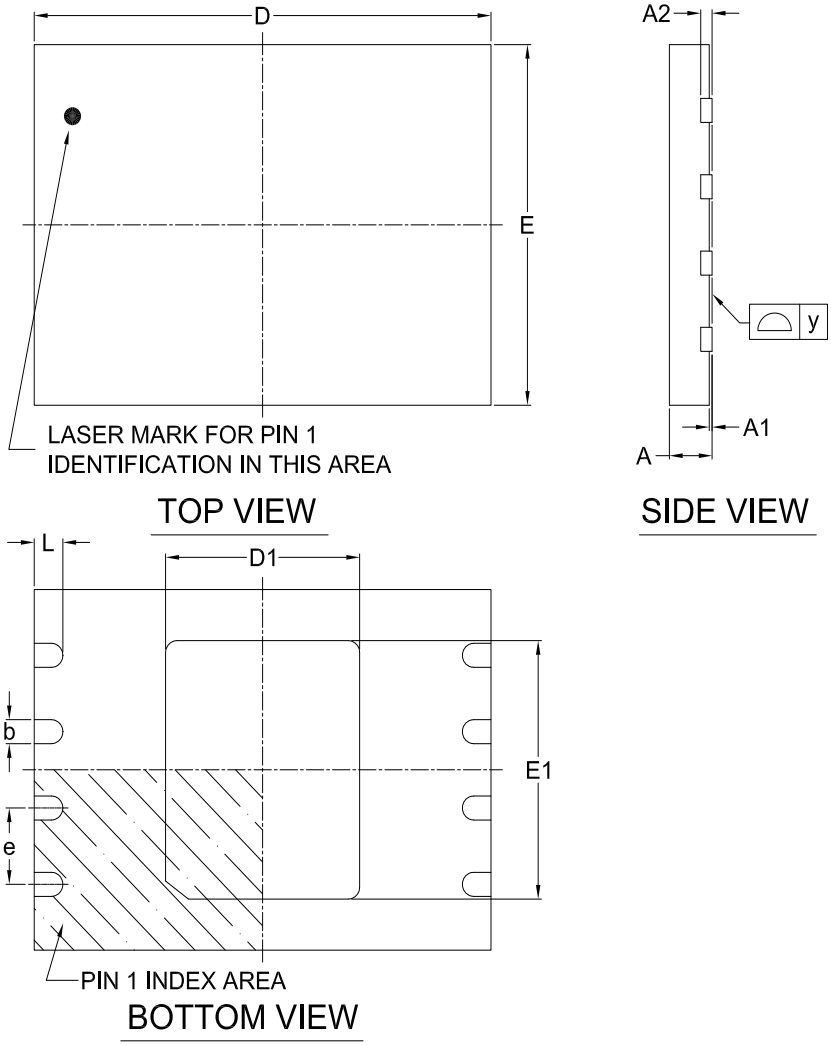
Note: *SI is "don't care" during HOLD operation.*

深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

14. PACKAGE INFORMATION

14-1. 8-WSON (8x6x0.8mm)

Doc. Title: Package Outline for WSON 8L (8x6x0.8MM, LEAD PITCH 1.27MM, E.P. 3.4x4.3MM)



Note:

This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	L	e	y
mm	Min.	0.70	---	---	0.35	7.90	3.35	5.90	4.25	0.45	---	0.00
	Nom.	---	---	0.20	0.40	8.00	3.40	6.00	4.30	0.50	1.27	---
	Max.	0.80	0.05	---	0.48	8.10	3.45	6.10	4.35	0.55	---	0.05
Inch	Min.	0.028	---	---	0.014	0.311	0.132	0.232	0.167	0.018	---	0.00
	Nom.	---	---	0.008	0.016	0.315	0.134	0.236	0.169	0.020	0.05	---
	Max.	0.032	0.002	---	0.019	0.319	0.136	0.240	0.171	0.022	---	0.002

深圳市满度科技有限公司
Web:www.manduic.com
Tel:139-1290-5940
Email:sales@manduic.com

15. REVISION HISTORY

Revision	Descriptions	Page
March 15, 2017		
0.00	Initial Release	ALL
June 06, 2017		
0.01	1. Changed the package type from Z2 to Z4	P7, P43
	2. Re-wording the reset command effect on the feature setting	P13
	3. Renamed the register of address B0h from "Secure OTP" to "Configuration"	P13
	4. Changed page title from "Advanced Information" to "Preliminary"	ALL
June 19, 2017		
1.0	1. Removed the title of "Preliminary"	ALL
October 23, 2020		
1.1	1. Added "Macronix Proprietary" footnote	ALL
	2. Supplement on bit3 of ADD=B0h of Configuration Register table as "Reserved (0)"	P13
	3. Updated **"14-1. 8-WSON (8x6x0.8mm)"** in Min./Max. D1, E1 and L values	P43
	4. Format modification	P41, 43

深圳市满度科技有限公司 Tel:+86-1290-5940
Web:www.manduic.com Email:sales@manduic.com

Except for customized products which have been expressly identified in the applicable agreement, Macronix's products are designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only, and not for use in any applications which may, directly or indirectly, cause death, personal injury, or severe property damages. In the event Macronix products are used in contradicted to their target usage above, the buyer shall take any and all actions to ensure said Macronix's product qualified for its actual use in accordance with the applicable laws and regulations; and Macronix as well as it's suppliers and/or distributors shall be released from any and all liability arisen therefrom.

Copyright© Macronix International Co., Ltd. 2017-2020. All rights reserved, including the trademarks and tradename thereof, such as Macronix, MXIC, MXIC Logo, MX Logo, Integrated Solutions Provider, Nbit, Macronix NBit, HybridNVM, HybridFlash, HybridXFlash, XtraROM, KH Logo, BE-SONOS, KSMC, Kingtech, MXSMIO, Macronix vEE, RichBook, Rich TV, OctaBus, FitCAM, ArmorFlash. The names and brands of third party referred thereto (if any) are for identification purposes only.

For the contact and order information, please visit Macronix's Web site at: http://www.macronix.com

MACRONIX INTERNATIONAL CO., LTD. reserves the right to change product and specifications without notice.

深圳市满度科技有限公司 Tel:139-1290-5940
Web:www.manduic.com Email:sales@manduic.com