# MX25U8033E

## 1.8V, 8M-BIT [x 1/x 2/x 4]
## CMOS MXSMIO® (SERIAL MULTI I/O)
## FLASH MEMORY

### *Key Features*

- *HOLD feature*
- *Multi I/O Support - Single I/O, Dual I/O and Quad I/O*
- *Auto Erase and Auto Program Algorithm*
- *Low Power Consumption*
- *Individual Protect*

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# 1. FEATURES

## GENERAL

- Single Power Supply Operation
  - 1.65 to 2.0 volt for read, erase, and program operations
- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- 8M: 8,388,608 x 1 bit structure or 4,194,304 x 2 bits (two I/O read mode) structure or 2,097,152 x 4 bits (four I/O read mode) structure
- 256 Equal Sectors with 4K byte each
  - Any Sector can be erased individually
- 32 Equal Blocks with 32K byte each
  - Any Block can be erased individually
- 16 Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Program Capability
  - Byte base
  - Page base (256 bytes)
- Latch-up protected to 100mA from -1V to Vcc +1V

## PERFORMANCE

- High Performance
  - Fast read
    - 1 I/O: 80MHz with 8 dummy cycles
    - 2 I/O: 80MHz with 4 dummy cycles, equivalent to 160MHz
    - 4 I/O: 70MHz with 6 dummy cycles, equivalent to 280MHz;
  - Fast program time: 1.2ms(typ.) and 3.0ms(max.)/page (256-byte per page)
  - Byte program time: 10us (typ.)
  - Fast erase time
    - 30ms(typ.) and 200ms(max.)/sector (4K-byte per sector)
    - 200ms(typ.) and 1000ms(max.)/block (32K-byte per block)
    - 500ms(typ.) and 2000ms(max.)/block (64K-byte per block)
    - 5.0s(typ.) and 10s(max.)/chip
- Low Power Consumption
  - Low active read current: 12mA(max.) at 80MHz, 7mA(max.) at 33MHz
  - Low active erase/programming current: 25mA (max.)
  - Low standby current: 8uA (typ.)/30uA (max.)
- Low Deep Power Down current: 8uA(max.)
- Typical 100,000 erase/program cycles
- 20 years data retention

## SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection

    The BP0-BP3 status bit defines the size of the area to be software protection against program and erase instructions
  - Additional 4K-bit secured OTP for unique identifier
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector or block
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first).


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- Status Register Feature
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS, REMS2 and REMS4 commands for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameter (SFDP) mode

**HARDWARE FEATURES**

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
  - Hardware write protection or Serial Data Input/Output for 4 x I/O read mode
- HOLD#/SIO3
  - HOLD feature, to pause the device without deselecting the device or Serial Data Input/Output for 4 x I/O read mode
- PACKAGE
  - 8-land USON (4x4mm)
  - 8-pin SOP (150mil)
  - 8-pin SOP (200mil)
  - 8-land WSON (6x5mm)
  - 8-WLCSP (Height: 0.45mm)
  - 8-WLCSP (Height: 0.33mm)
  - **All devices are RoHS Compliant and Halogen-free**

## 2. GENERAL DESCRIPTION

The MX25U8033E is 8,388,608 bit serial Flash memory, which is configured as 1,048,576 x 8 internally. The MX25U8033E features a serial peripheral interface and software protocol allowing operation on a simple 4-wire bus while it is in single I/O mode. The four bus signals are a clock input (SCLK), a serial data input (SI), a serial data output (SO) and a chip select (CS#). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin, WP# pin and HOLD# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX25U8033E MXSMIO® (Serial Multi I/O) provides sequential read operation on the whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis. Erase command is executed on 4K-byte sector, 32K-byte block, or 64K-byte block, or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via the WIP bit.
Advanced security features enhance the protection and security functions, please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode.

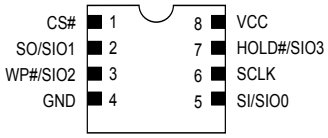
The MX25U8033E utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

**Table 1. Additional Feature Comparison**

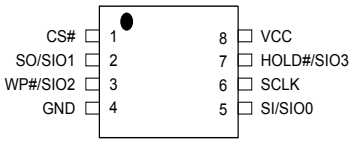
| Additional Features / Part Name | Protection and Security | | | Read Performance | | Identifier | | |
|---|---|---|---|---|---|---|---|---|
| | Flexible Block Protection (BP0-BP3) | Individual Protect | 4K-bit secured OTP | 2 I/O Read | 4 I/O Read | RES (Command: AB hex) | REMS/ REMS2/ REMS4 (Command: 90/EF/DF hex) | RDID (Command: 9F hex) |
| MX25U8033E | V | V | V | V | V | 34 (hex) | C2 34 (hex) (if ADD=0) | C2 25 34 (hex) |

## 3. PIN CONFIGURATIONS

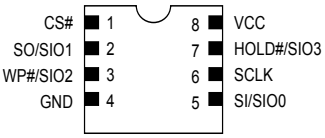
### 8-LAND USON (4x4mm)



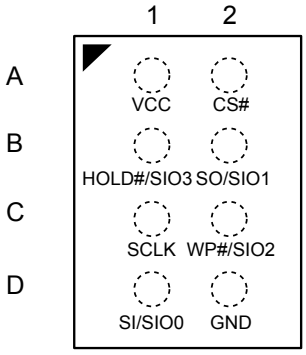

### 8-PIN SOP (150mil/200mil)




### 8-LAND WSON (6x5mm)



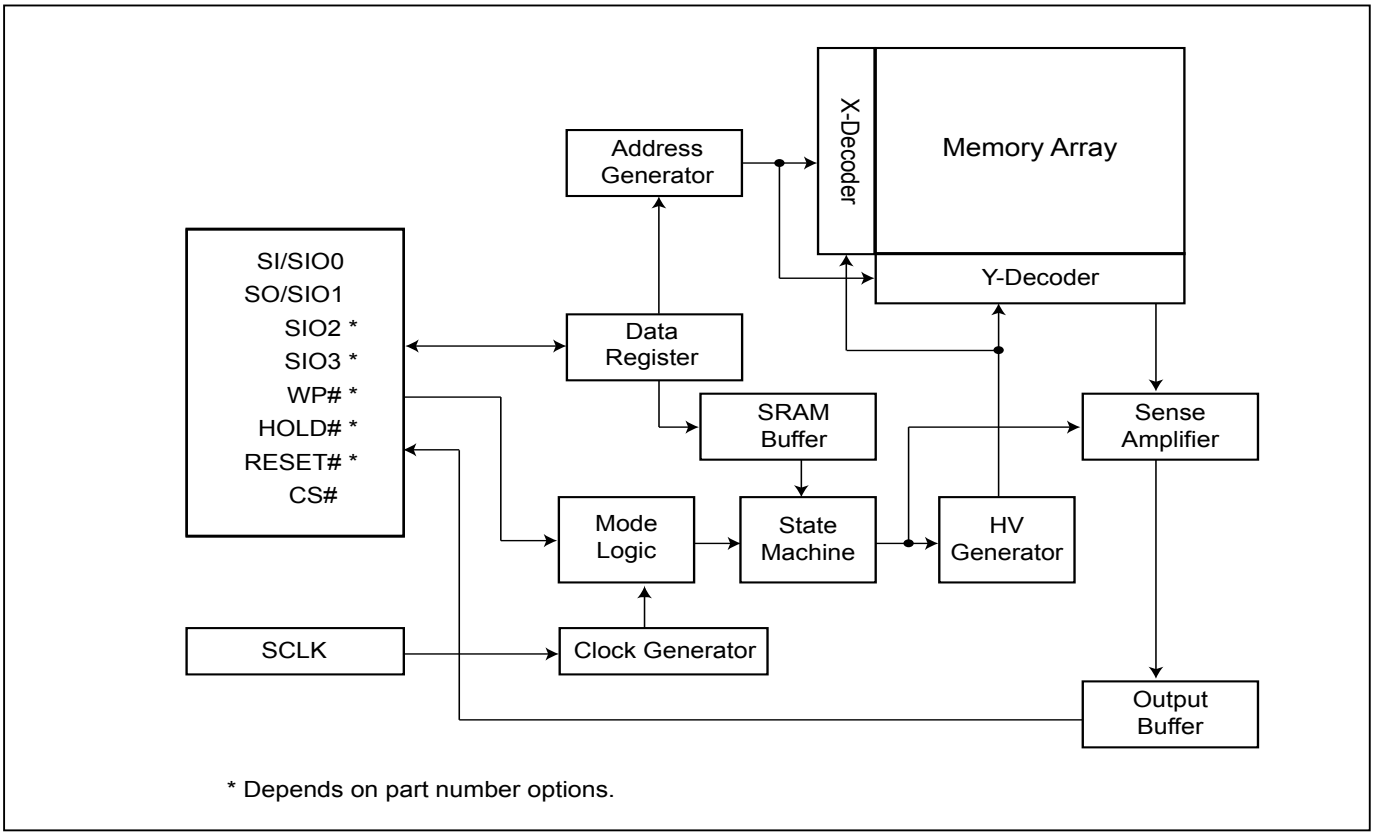

### 8-WLCSP (Height: 0.45mm, 0.33mm) TOP View




## 4. PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|---|---|
| CS# | Chip Select |
| SI/SIO0 | Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode) |
| SO/SIO1 | Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode) |
| SCLK | Clock Input |
| WP#/SIO2 | Write Protection Active Low or Serial Data Input & Output (for 4xI/O read mode) |
| HOLD#/SIO3 | To pause the device without deselecting the device or Serial Data Input & Output (for 4xI/O read mode) |
| VCC | + 1.8V Power Supply |
| GND | Ground |

## 5. BLOCK DIAGRAM



## 6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.

- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before issuing other commands to change data. The WEL bit will return to resetting stage while the following conditions occurred:
  - Power-up
  - Completion of Write Disable (WRDI) command
  - Completion of Write Status Register (WRSR) command
  - Completion of Page Program (PP) command
  - Completion of Quad page program (4PP) command
  - Completion of Sector Erase (SE) command
  - Completion of Block Erase 32KB (BE32K) command
  - Completion of Block Erase (BE) command
  - Completion of Chip Erase (CE) command
  - Completion of Write Protection Select (WPSEL) command
  - Completion of Write Security Register (WRSCUR) command
  - Completion of Single Block Lock/Unlock (SBLK/SBULK) command
  - Completion of Gang Block Lock/Unlock (GBLK/GBULK) command

- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES).

- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

**I. Block lock protection**

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as table of *"Table 2. Protected Area Sizes"*, the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.
Please refer to table of *"Table 2. Protected Area Sizes"*.
- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and SRWD bit. If the system goes into four I/O read mode, the feature of HPM will be disabled.


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**Table 2. Protected Area Sizes**

| Status Bit | | | | Protect Level |
|---|---|---|---|---|
| BP3 | BP2 | BP1 | BP0 | 8Mb |
| 0 | 0 | 0 | 0 | 0 (none) |
| 0 | 0 | 0 | 1 | 1 (1block, protected block 15th) |
| 0 | 0 | 1 | 0 | 2 (2blocks, protected block 14th~15th) |
| 0 | 0 | 1 | 1 | 3 (4blocks, protected block 12nd~15th) |
| 0 | 1 | 0 | 0 | 4 (8blocks, protected block 8th~15th) |
| 0 | 1 | 0 | 1 | 5 (16blocks, protected all) |
| 0 | 1 | 1 | 0 | 6 (16blocks, protected all) |
| 0 | 1 | 1 | 1 | 7 (16blocks, protected all) |
| 1 | 0 | 0 | 0 | 8 (16blocks, protected all) |
| 1 | 0 | 0 | 1 | 9 (16blocks, protected all) |
| 1 | 0 | 1 | 0 | 10 (16blocks, protected all) |
| 1 | 0 | 1 | 1 | 11 (8blocks, protected block 0th~7th) |
| 1 | 1 | 0 | 0 | 12 (12blocks, protected block 0th~11st) |
| 1 | 1 | 0 | 1 | 13 (14blocks, protected block 0th~13rd) |
| 1 | 1 | 1 | 0 | 14 (15blocks, protected block 0th~14th) |
| 1 | 1 | 1 | 1 | 15 (16blocks, protected all) |

II. **Additional 4K-bit secured OTP** for unique identifier: to provide 4K-bit One-Time Program area for setting device unique serial number - Which may be set by factory or system maker. Please refer to Table 3. 4K-bit Secured OTP Definition.

- Security register bit 0 indicates whether the chip is locked by factory or not.
- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing EXSO command.
- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to table of "Security Register Definition" for security register bit definition and table of "4K-bit Secured OTP Definition" for address range definition.

Note:
Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit Secured OTP mode, array access is not allowed.

**Table 3. 4K-bit Secured OTP Definition**

| Address range | Size | Standard Factory Lock | Customer Lock |
|---|---|---|---|
| xxx000~xxx00F | 128-bit | ESN (electrical serial number) | Determined by customer |
| xxx010~xxx1FF | 3968-bit | N/A | |


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## 7. MEMORY ORGANIZATION

### Table 4. Memory Organization

| Block (64KB) | Block (32KB) | Sector (4KB) | Address Range | | |
|---|---|---|---|---|---|
| 15 | 31 \| 30 | 255 | 0FF000h | 0FFFFFh | ▲ Individual Sector Lock/Unlock ▼ |
| | | : | : | : | |
| | | 240 | 0F0000h | 0F0FFFh | |
| 14 | 29 \| 28 | 239 | 0EF000h | 0EFFFFh | ▲ |
| | | : | : | : | |
| | | 224 | 0E0000h | 0E0FFFh | |
| 13 | 27 \| 26 | 223 | 0DF000h | 0DFFFFh | |
| | | : | : | : | |
| | | 208 | 0D0000h | 0D0FFFh | |
| 12 | 25 \| 24 | 207 | 0CF000h | 0CFFFFh | |
| | | : | : | : | |
| | | 192 | 0C0000h | 0C0FFFh | |
| 11 | 23 \| 22 | 191 | 0BF000h | 0BFFFFh | |
| | | : | : | : | |
| | | 176 | 0B0000h | 0B0FFFh | |
| 10 | 21 \| 20 | 175 | 0AF000h | 0AFFFFh | |
| | | : | : | : | |
| | | 160 | 0A0000h | 0A0FFFh | |
| 9 | 19 \| 18 | 159 | 09F000h | 09FFFFh | |
| | | : | : | : | |
| | | 144 | 090000h | 090FFFh | |
| 8 | 17 \| 16 | 143 | 08F000h | 08FFFFh | |
| | | : | : | : | |
| | | 128 | 080000h | 080FFFh | |
| 7 | 15 \| 14 | 127 | 07F000h | 07FFFFh | |
| | | : | : | : | |
| | | 112 | 070000h | 070FFFh | Individual Block Lock/Unlock |
| 6 | 13 \| 12 | 111 | 06F000h | 06FFFFh | |
| | | : | : | : | |
| | | 96 | 060000h | 060FFFh | |
| 5 | 11 \| 10 | 95 | 05F000h | 05FFFFh | |
| | | : | : | : | |
| | | 80 | 050000h | 050FFFh | |
| 4 | 9 \| 8 | 79 | 04F000h | 04FFFFh | |
| | | : | : | : | |
| | | 64 | 040000h | 040FFFh | |
| 3 | 7 \| 6 | 63 | 03F000h | 03FFFFh | |
| | | : | : | : | |
| | | 48 | 030000h | 030FFFh | |
| 2 | 5 \| 4 | 47 | 02F000h | 02FFFFh | |
| | | : | : | : | |
| | | 32 | 020000h | 020FFFh | |
| 1 | 3 \| 2 | 31 | 01F000h | 01FFFFh | |
| | | : | : | : | |
| | | 16 | 010000h | 010FFFh | ▼ |
| 0 | 1 \| 0 | 15 | 00F000h | 00FFFFh | ▲ |
| | | : | : | : | |
| | | 2 | 002000h | 002FFFh | Individual Sector Lock/Unlock |
| | | 1 | 001000h | 001FFFh | |
| | | 0 | 000000h | 000FFFh | ▼ |


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## 8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this device, it enters standby mode and remains in the standby mode until next CS# falling edge. In standby mode, SO pin of the device is High-Z.

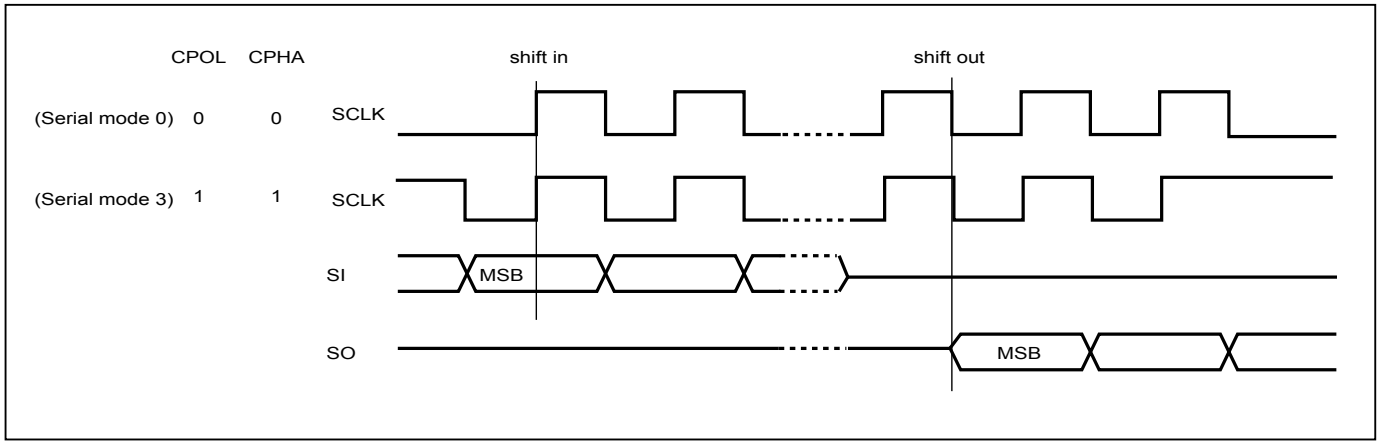
3. When correct command is inputted to this device, it becomes active mode and remains in the active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock (SCLK) and data is shifted out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *"Figure 1. Serial Modes Supported"*.

5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, 2READ, DREAD, 4READ, RES, REMS, REMS2, REMS4 and RDSFDP, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE32K, BE, CE, PP, 4PP, RDP, DP, WPSEL, SBLK, SBULK, GBLK, GBULK,ENSO, EXSO, and WRSCUR, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. While a Write Status Register, Program or Erase operation is in progress, to the memory array is neglected and while not affect the current operation of WRSCUR, WPSEL Write Status Register, Program and Erase.

**Figure 1. Serial Modes Supported**




**Note:**
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

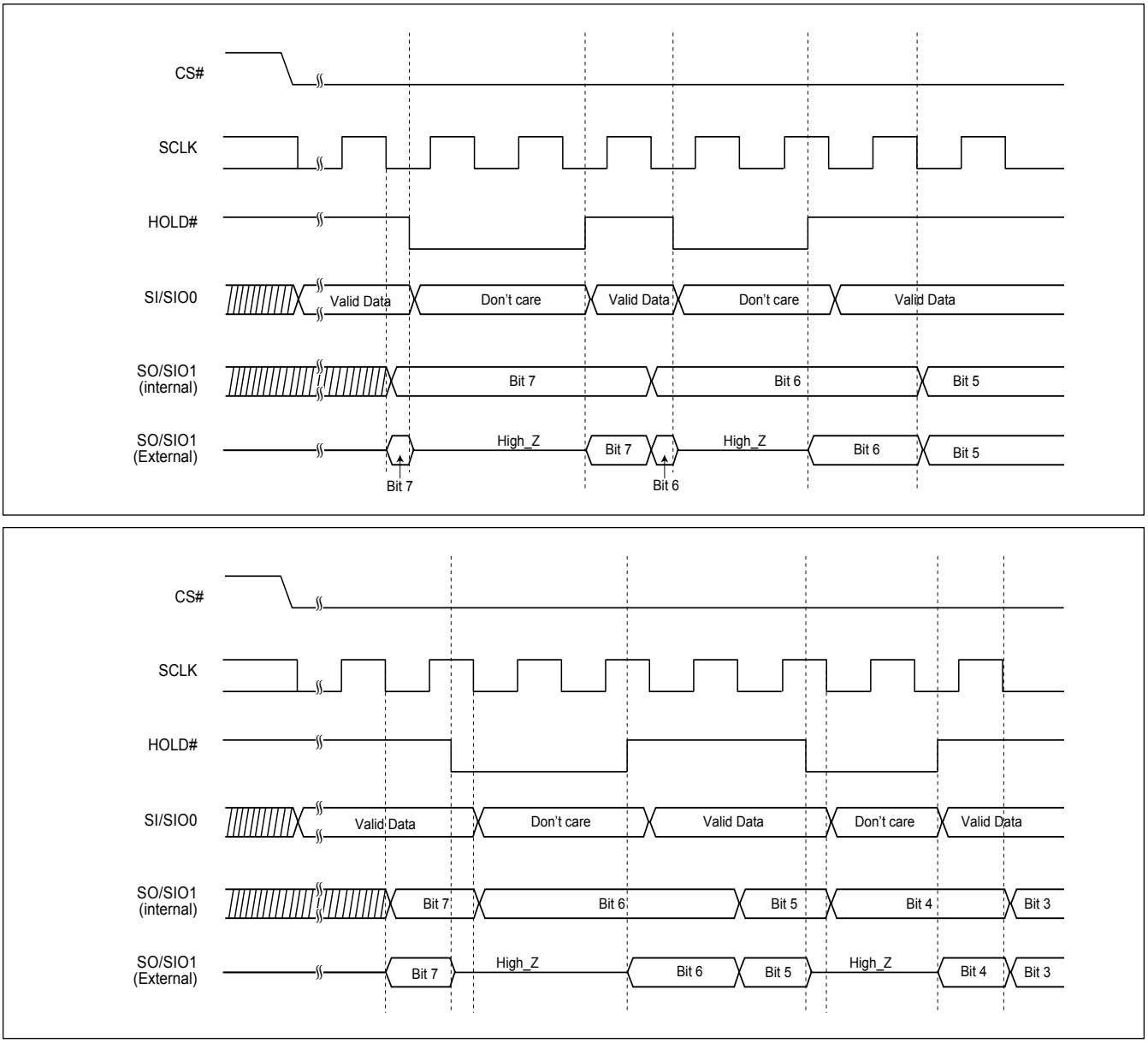

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## 9. HOLD FEATURE

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select (CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock(SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low).

**Figure 2. Hold Condition Operation**




During the HOLD operation, the Serial Data Output (SO) is high impedance when Hold# pin goes low and will keep high impedance until Hold# pin goes high. The Serial Data Input (SI) is don't care if both Serial Clock (SCLK) and Hold# pin goes low and will keep the state until SCLK goes low and Hold# pin goes high. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low. (***Note:*** The HOLD feature is disabled during Quad I/O mode.)

## 10. COMMAND DESCRIPTION

### Table 5. Command Set

#### Read Commands

| I/O | 1 | 1 | 1 | 2 | 2 | 4 |
|---|---|---|---|---|---|---|
| Command (byte) | READ (normal read) | FAST READ (fast read data) | RDSFDP (Read SFDP) | 2READ (2 x I/O read command) | DREAD (1I / 2O read command) | 4READ (4 x I/O read command) |
| Clock rate (MHz) | 50 | 80 | 80 | 80 | 80 | 70 |
| 1st byte | 03 (hex) | 0B (hex) | 5A (hex) | BB (hex) | 3B (hex) | EB (hex) |
| 2nd byte | AD1 | AD1 | AD1 | AD1 | AD1 | AD1 |
| 3rd byte | AD2 | AD2 | AD2 | AD2 | AD2 | AD2 |
| 4th byte | AD3 | AD3 | AD3 | AD3 | AD3 | AD3 |
| 5th byte | | Dummy | Dummy | Dummy | Dummy | Dummy |
| Action | n bytes read out until CS# goes high | n bytes read out until CS# goes high | Read SFDP mode | n bytes read out by 2 x I/O until CS# goes high | | n bytes read out by 4 x I/O until CS# goes high |

#### Program/Erase Commands

| Command (byte) | WREN (write enable) | WRDI (write disable) | RDSR (read status register) | WRSR (write status register) | SE (sector erase) | BE 32K (block erase 32KB) | BE (block erase 64KB) |
|---|---|---|---|---|---|---|---|
| 1st byte | 06 (hex) | 04 (hex) | 05 (hex) | 01 (hex) | 20 (hex) | 52 (hex) | D8 (hex) |
| 2nd byte | | | | Values | AD1 | AD1 | AD1 |
| 3rd byte | | | | | AD2 | AD2 | AD2 |
| 4th byte | | | | | AD3 | AD3 | AD3 |
| Action | sets the (WEL) write enable latch bit | resets the (WEL) write enable latch bit | to read out the values of the status register | to write new values of the status register | to erase the selected sector | to erase the selected 32KB block | to erase the selected block |

| Command (byte) | CE (chip erase) | PP (page program) | 4PP (Quad page program) | DP (Deep power down) | RDP (Release from deep power down) |
|---|---|---|---|---|---|
| 1st byte | 60 or C7 (hex) | 02 (hex) | 38 (hex) | B9 (hex) | AB (hex) |
| 2nd byte | | AD1 | AD1 | | |
| 3rd byte | | AD2 | AD2 | | |
| 4th byte | | AD3 | AD3 | | |
| Action | to erase whole chip | to program the selected page | quad input to program the selected page | enters deep power down mode | release from deep power down mode |


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## Security/ID/Mode Setting/Reset Commands

| Command (byte) | RDID (read identific-ation) | RES (read electronic ID) | REMS (read electronic manufacturer & device ID) | REMS2 (read ID for 2x I/O mode) | REMS4 (read ID for 4x I/O mode) | ENSO (enter secured OTP) | EXSO (exit secured OTP) |
|---|---|---|---|---|---|---|---|
| 1st byte | 9F (hex) | AB (hex) | 90 (hex) | EF (hex) | DF (hex) | B1 (hex) | C1 (hex) |
| 2nd byte | | x | x | X | x | | |
| 3rd byte | | x | x | X | x | | |
| 4th byte | | x | ADD | ADD | ADD | | |
| Action | outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID | to read out 1-byte Device ID | output the Manufacturer ID & Device ID | output the Manufacturer ID & Device ID | output the Manufacturer ID & Device ID | to enter the 4K-bit secured OTP mode | to exit the 4K-bit secured OTP mode |

| Command (byte) | RDSCUR (read security register) | WRSCUR (write security register) | SBLK (single block lock | SBULK (single block unlock) | RDBLOCK (block protect read) | GBLK (gang block lock) | GBULK (gang block unlock) |
|---|---|---|---|---|---|---|---|
| 1st byte | 2B (hex) | 2F (hex) | 36 (hex) | 39 (hex) | 3C (hex) | 7E (hex) | 98 (hex) |
| 2nd byte | | | AD1 | AD1 | AD1 | | |
| 3rd byte | | | AD2 | AD2 | AD2 | | |
| 4th byte | | | AD3 | AD3 | AD3 | | |
| Action | to read value of security register | to set the lock-down bit as "1" (once lock-down, cannot be update) | individual block (64K-byte) or sector (4K-byte) write protect | individual block (64K-byte) or sector (4K-byte) unprotect | read individual block or sector write protect status | whole chip write protect | whole chip unprotect |

| Command (byte) | WPSEL (Write Protect Selection) |
|---|---|
| 1st byte | 68 (hex) |
| 2nd byte | |
| 3rd byte | |
| 4th byte | |
| Action | to enter and enable individual block protect mode |

Note 1: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.
2: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.


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### 10-1. Write Enable (WREN)

The Write Enable (WREN) instruction is to set Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, SE, BE32K, BE, CE, WPSEL, WRSCUR, SBLK, SBULK, GBLK, GBULK and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high. (Please refer to *"Figure 19. Write Enable (WREN) Sequence (Command 06)"*)

### 10-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high. (Please refer to *"Figure 20. Write Disable (WRDI) Sequence (Command 04)"*)

The WEL bit will be reset while the following conditions occurred:

- Power-up
- Completion of Write Disable (WRDI) instruction
- Completion of Write Status Register (WRSR) instruction
- Completion of Page Program (PP) instruction
- Completion of Quad page program (4PP) instruction
- Completion of Sector Erase (SE) instruction
- Completion of Block Erase 32KB (BE32K) instruction
- Completion of Block Erase (BE) instruction
- Completion of Chip Erase (CE) instruction
- Completion of Write Protection Select (WPSEL) instruction
- Completion of Write Security Register (WRSCUR) instruction
- Completion of Single Block Lock/Unlock (SBLK/SBULK) instruction
- Completion of Gang Block Lock/Unlock (GBLK/GBULK) instruction

### 10-3. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID and Device ID are listed as *"Table 8. ID Definitions"*.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out. (Please refer to *"Figure 21. Read Identification (RDID) Sequence (Command 9F)"*)

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

### 10-4. Read Status Register (RDSR)

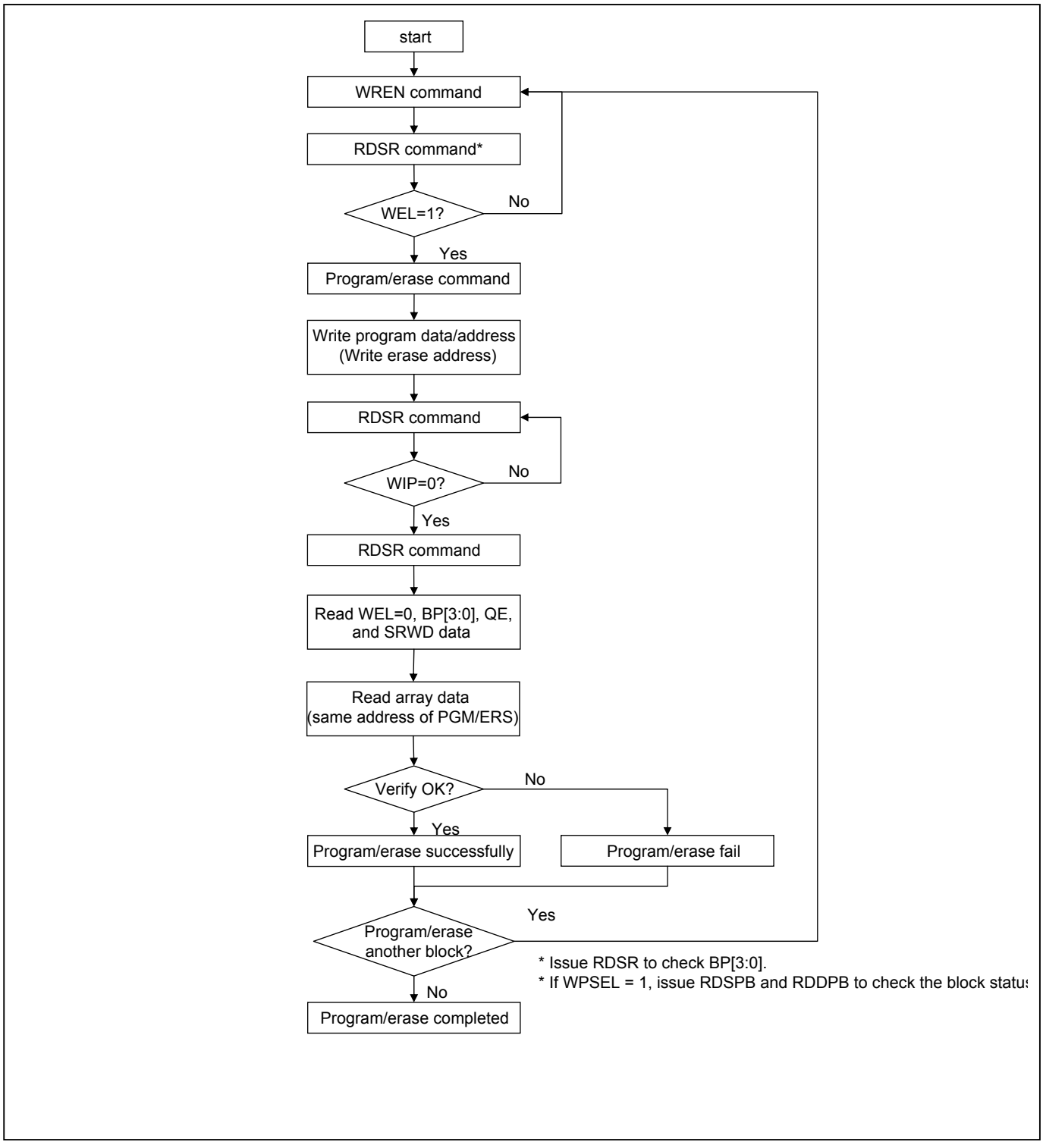
The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/WPSEL/WRSCUR/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.


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The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO. (Please refer to *"Figure 22. Read Status Register (RDSR) Sequence (Command 05)"*)

For user to check if Program/Erase operation is finished or not, RDSR instruction flow are shown as follows:

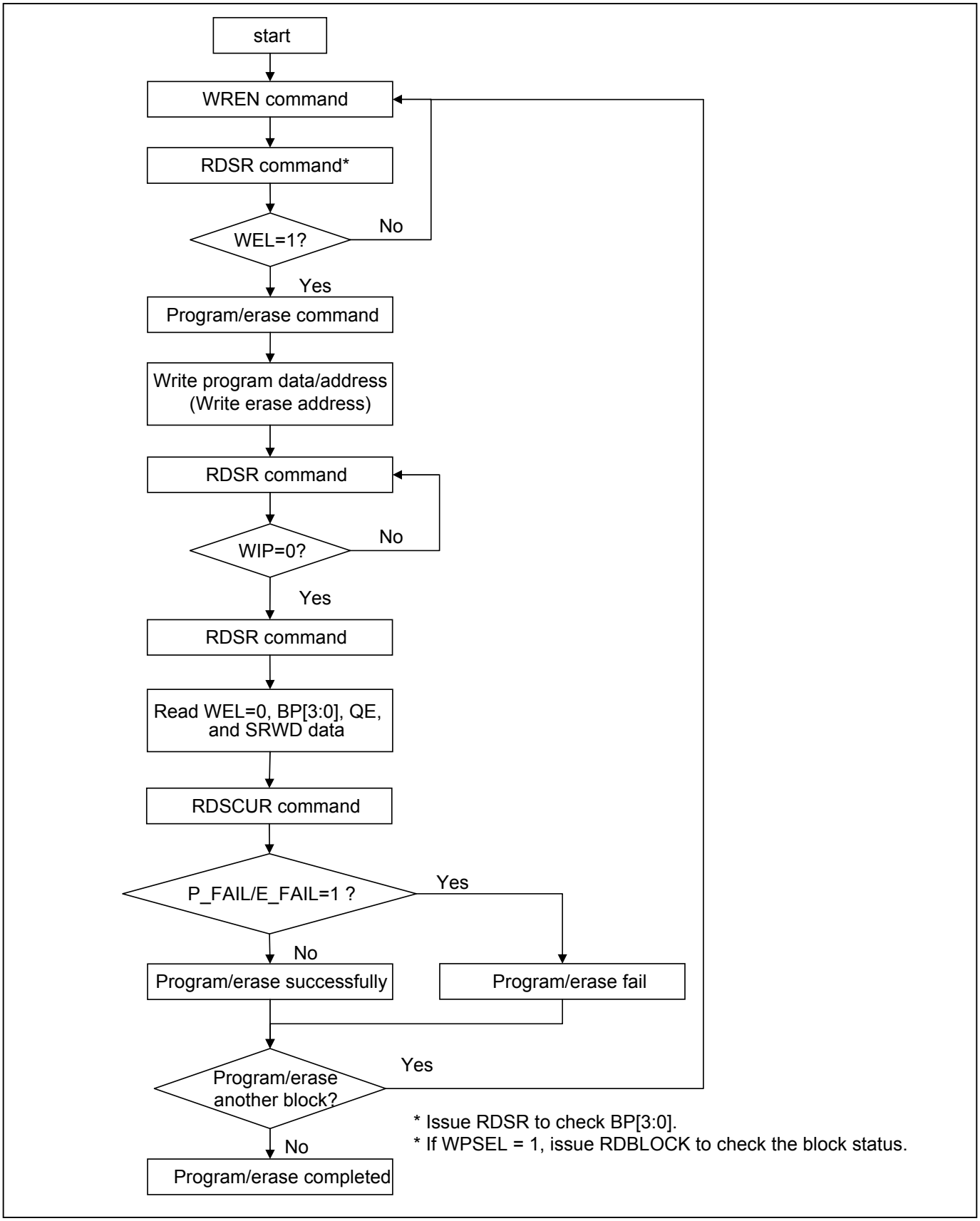
**Figure 3. Program/Erase Flow with Read Array Data**





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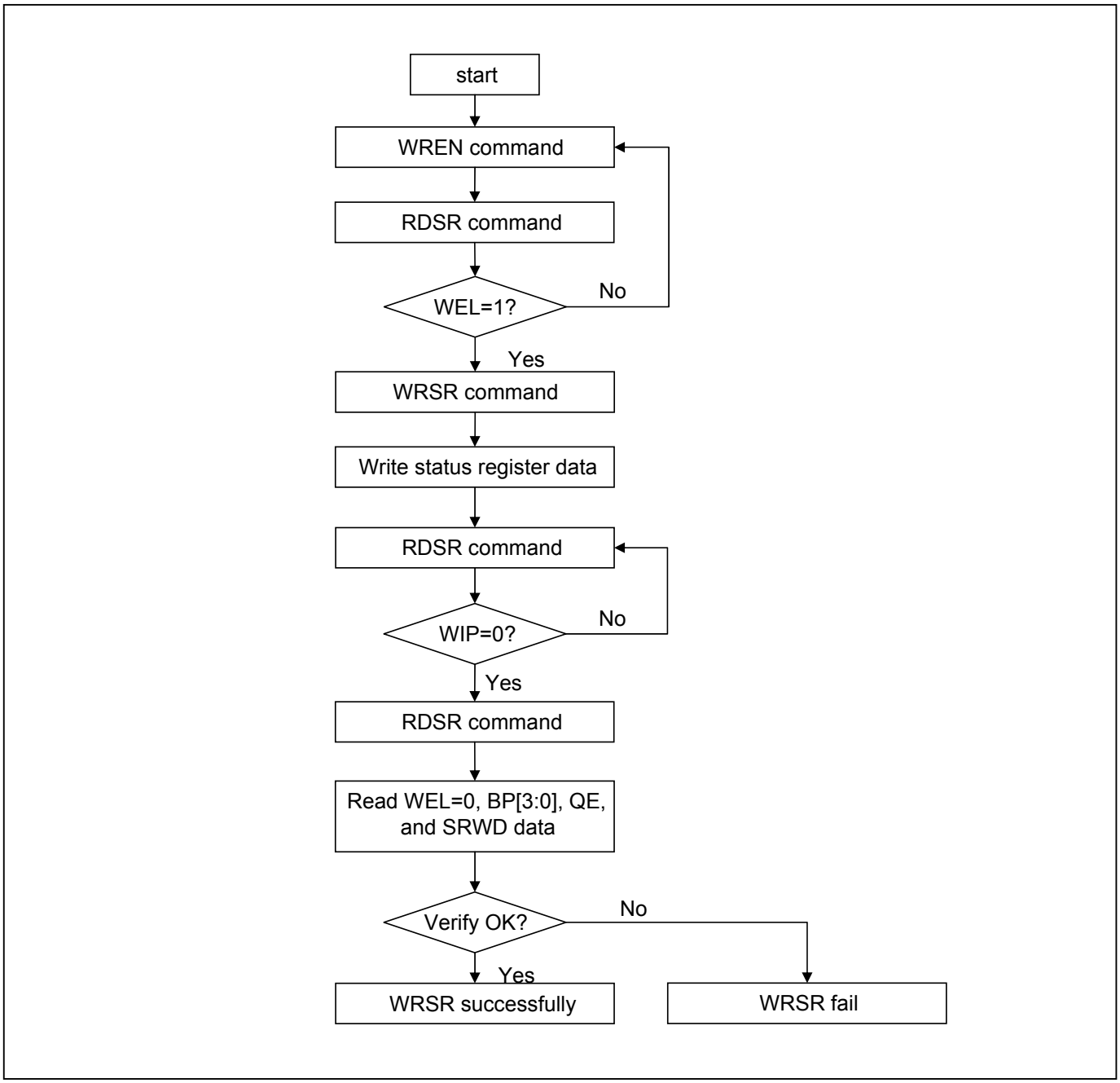
**Figure 4. Program/ Erase Flow without Read Array Data (read P_FAIL/E_FAIL flag)**





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**Figure 5. WRSR Flow**





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The definition of the status register bits is as below:

**WIP bit.** The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

**WEL bit.** The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored if it is applied to a protected memory area. To ensure both WIP bit & WEL bit are both set to 0 and available for next program/erase/operations, WIP bit needs to be confirm to be 0 before polling WEL bit. After WIP bit confirmed, WEL bit needs to be confirm to be 0.

**BP3, BP2, BP1, BP0 bits.** The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in *"Table 2. Protected Area Sizes"*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase 32KB (BE32K), Block Erase (BE) and Chip Erase (CE) instructions (only if Block Protect bits (BP3:BP0) set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default. Which is unprotected.

**QE bit.** The Quad Enable (QE) bit is a non-volatile bit with a factory default of “0”. When QE is “0”, Quad mode commands are ignored; pins WP#/SIO2 and HOLD#/SIO3 function as WP# and HOLD#, respectively. When QE is “1”, Quad mode is enabled and Quad mode commands are supported along with Single and Dual mode commands. Pins WP#/SIO2 and HOLD#/SIO3 function as SIO2 and SIO3, respectively, and their alternate pin functions are disabled. Enabling Quad mode also disables the HPM and HOLD features

**SRWD bit.** The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only. The SRWD bit defaults to be "0".

**Table 6. Status Register**

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|
| SRWD (status register write protect) | QE (Quad Enable) | BP3 (level of protected block) | BP2 (level of protected block) | BP1 (level of protected block) | BP0 (level of protected block) | WEL (write enable latch) | WIP (write in progress bit) |
| 1=status register write disabled 0=status register write enabled | 1=Quad Enabled 0=not Quad Enabled | *(note 1)* | *(note 1)* | *(note 1)* | *(note 1)* | 1=write enabled 0=not write enabled | 1=write operation 0=not in write operation |
| Non-volatile bit | Non-volatile bit | Non-volatile bit | Non-volatile bit | Non-volatile bit | Non-volatile bit | volatile bit | volatile bit |

Note 1: Please refer to the *"Table 2. Protected Area Sizes"*.

### 10-5. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in *"Table 2. Protected Area Sizes"*). The WRSR also can set or reset the Quad enable (QE) bit and set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#/SIO2) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the status register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→CS# goes high. (Please refer to *"Figure 23. Write Status Register (WRSR) Sequence (Command 01)"*)

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

**Table 7. Protection Modes**

| Mode | Status register condition | WP# and SRWD bit status | Memory |
|---|---|---|---|
| Software protection mode (SPM) | Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed | WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1 | The protected area cannot be program or erase. |
| Hardware protection mode (HPM) | The SRWD, BP0-BP3 of status register bits cannot be changed | WP#=0, SRWD bit=1 | The protected area cannot be program or erase. |

**Note:**
1. As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in *"Table 2. Protected Area Sizes"*).

As the above table showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode (SPM):
- When SRWD bit=0, no matter WP#/SIO2 is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP#/SIO2 is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM)

**Note:**
If SRWD bit=1 but WP#/SIO2 is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.


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Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP#/SIO2 is low (or WP#/SIO2 is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and hardware protected mode by the WP#/SIO2 to against data modification.

**Note:**
To exit the hardware protected mode requires WP#/SIO2 driving high once the hardware protected mode is entered. If the WP#/SIO2 pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0.
If the system enter Quad I/O QE=1, the feature of HPM will be disabled.

### 10-6. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→sending READ instruction code→ 3-byte address on SI→ data out on SO→to end READ operation can use CS# to high at any time during data out. (Please refer to *"Figure 24. Read Data Bytes (READ) Sequence (Command 03) (50MHz)"*)

### 10-7. Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code→ 3-byte address on SI→1-dummy byte (default) address on SI→ data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out. (Please refer to *"Figure 25. Read at Higher Speed (FAST_READ) Sequence (Command 0B)"*)

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

### 10-8. Dual Read Mode (DREAD)

The DREAD instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.


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The sequence of issuing DREAD instruction is: CS# goes low → sending DREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SO1 & SO0 → to end DREAD operation can use CS# to high at any time during data out. (Please refer to *"Figure 26. Dual Read Mode Sequence (Command 3B)"*)

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

### 10-9. 2 x I/O Read Mode (2READ)

The 2READ instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→ sending 2READ instruction→ 24-bit address interleave on SIO1 & SIO0→ 4 dummy cycles on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out (Please refer to *"Figure 27. 2 x I/O Read Mode Sequence (Command BB)"* for 2 x I/O Read Mode Timing Waveform).

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

### 10-10. 4 x I/O Read Mode (4READ)

The 4READ instruction enable quad throughput of Serial Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4READ instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing 4READ instruction is: CS# goes low→ sending 4READ instruction→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→2+4 dummy cycles→data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out. (Please refer to *"Figure 28. 4 x I/O Read Mode Sequence (Command EB)"*)

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.


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### 10-11.Performance Enhance Mode

The device could waive the command cycle bits if the two cycle bits after address cycle toggles. (Please note *"Figure 29. 2 x I/O Read Enhance Performance Mode Sequence (Command BB)"* and *"Figure 30. 4 x I/O Read Enhance Performance Mode Sequence (Command EB)"* )

After entering enhance mode, following CS# go high, the device will stay in the read mode and treat CS# go low of the first clock as address instead of command cycle.

Another sequence of issuing 2READ (or 4READ) instruction especially useful in random access is: CS# goes low→sending 2READ (or 4READ) instruction→3-bytes address interleave on SIO1, SIO0 (SIO3, SIO2, SIO1 & SIO0)→Performance enhance toggling bit P[3:0] ( P[7:0] )→ 2 (or 4) dummy cycles →data out still CS# goes high → CS# goes low (reduce 2READ or 4READ instruction) →24-bit random access address (Please refer to *"Figure 29. 2 x I/O Read Enhance Performance Mode Sequence (Command BB)"* and *"Figure 30. 4 x I/O Read Enhance Performance Mode Sequence (Command EB)"* ).

In the 2xI/O performance-enhancing mode, P[3:2] must be toggling with P[1:0]; likewise P[3:0]=3h, 6h, 9h or Ch can make this mode continue and reduce the next 2READ instruction. Once P[3:2] is no longer toggling with P[1:0]; likewise P[3:0]=0h, 5h, Ah or Fh and afterwards CS# is raised and then lowered, the system then will escape from performance enhance mode and return to normal operation.

In the 4xI/O performance-enhancing mode, P[7:4] must be toggling with P[3:0] ; likewise P[7:0]=A5h, 5Ah, F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh,00h,AAh or 55h and afterwards CS# is raised and then lowered, the system then will escape from performance enhance mode and return to normal operation.

### 10-12. Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see *"Table 4. Memory Organization"*) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of the address been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low→ sending SE instruction code→ 3-byte address on SI→ CS# goes high. (Please refer to *"Figure 33. Sector Erase (SE) Sequence (Command 20)"*)

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Sector Erase cycle is in progress. The WIP sets during the tSE timing, and clears when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the sector is protected by BP3 ~ 0 (WPSEL=0) or by individual lock (WPSEL=1), the Sector Erase (SE) instruction will not be executed on the sector.


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### 10-13. Block Erase (BE32K)

The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block (see table of memory organization) is a valid address for Block Erase (BE32K) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE32K instruction is: CS# goes low→ sending BE32K instruction code→ 3-byte address on SI→CS# goes high. (Please refer to *"Figure 34. Block Erase 32KB (BE32K) Sequence (Command 52)"*)

The self-timed Block Erase Cycle time (tBE32K) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while he Block Erase cycle is in progress. The WIP sets during the tBE32K timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP3 ~ 0 (WPSEL=0) or by individual lock (WPSEL=1), the Block Erase (tBE32K) instruction will not be executed on the block.

### 10-14. Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (Please refer to *"Table 4. Memory Organization"*) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low→ sending BE instruction code→ 3-byte address on SI→ CS# goes high. (Please refer to *"Figure 35. Block Erase (BE) Sequence (Command D8)"*)

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP3 ~ 0 (WPSEL=0) or by individual lock (WPSEL=1), the Block Erase (BE) instruction will not be executed on the block.

### 10-15. Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→sending CE instruction code→CS# goes high. (Please refer to *"Figure 36. Chip Erase (CE) Sequence (Command 60 or C7)"*)

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Chip Erase cycle is in progress. The WIP sets during the tCE timing, and clears when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the chip is protected by BP3 ~ 0 (WPSEL=0) or by individual lock (WPSEL=1), the Chip Erase (CE) instruction will not be executed. It will be only executed when BP3, BP2, BP1, BP0 all set to "0".

### 10-16. Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. If the entire 256 data bytes are going to be programmed, A7-A0 (The eight least significant address bits) should be cleared. The last address byte (the 8 least significant address bits, A7-A0) should be set to 0 for 256 bytes page program. If A7-A0 are not all zero, transmitted data that exceed page length are programmed from the starting address (24-bit address that last 8 bit are all 0) of currently selected page. If the data bytes sent to the device exceeds 256, the last 256 data byte is programmed at the request page and previous data will be disregarded. If the data bytes sent to the device has not exceeded 256, the data will be programmed at the request address of the page. There will be no effort on the other data bytes of the same page.

The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→ 3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high. (Please refer to *"Figure 31. Page Program (PP) Sequence (Command 02)"*)

The CS# must be kept to low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary (the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Page Program cycle is in progress. The WIP sets during the tPP timing, and clears when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the page is protected by BP3 ~ 0 (WPSEL=0) or by individual lock (WPSEL=1), the Page Program (PP) instruction will not be executed.

### 10-17. 4 x I/O Page Program (4PP)

The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit must be set to "1" before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3 as address and data input, which can improve programmer performance and the effectiveness of application of lower clock less than 70MHz. For system with faster clock, the Quad page program cannot provide more actual favors, because the required internal page program time is far more than the time data flows in. Therefore, we suggest that while executing this command (especially during sending data), user can slow the clock speed down to 70MHz below. The other function descriptions are as same as standard page program.

The sequence of issuing 4PP instruction is: CS# goes low→ sending 4PP instruction code→ 3-byte address on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→CS# goes high. (Please refer to *"Figure 32. 4 x I/O Page Program (4PP) Sequence (Command 38)"*)

If the page protected by BP3 ~ 0 (WPSEL=0) or by individual lock (WPSEL=1), the Quad page program (4PP) instruction will not be executed.

### 10-18. Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device to minimizing the power consumption, (the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored.


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The sequence of issuing DP instruction is: CS# goes low→sending DP instruction code→CS# goes high.
(Please refer to *"Figure 37. Deep Power-down (DP) Sequence (Command B9)"*)

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction. (Those instructions allow the ID being reading out). When Power-down, or software reset command the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For DP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode.

### 10-19. Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is completed by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES1, and Chip Select (CS#) must remain High for at least tRES1(max), as specified in *"Table 14. AC Characteristics"*. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions. The RDP instruction is only for releasing from Deep Power Down Mode.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions on next page. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.

The sequence is shown as *"Figure 38. Release from Deep Power-down and Read Electronic Signature (RES) (Command AB)"* and *"Figure 39. Release from Deep Power-down (RDP) Sequence (Command AB)"*. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

### 10-20. Read Electronic Manufacturer ID & Device ID (REMS), (REMS2), (REMS4)

The REMS, REMS2 and REMS4 instruction provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The instruction is initiated by driving the CS# pin low and shift the instruction code "90h", "DFh" or "EFh" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID for Macronix (C2h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in *"Figure 40. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90/EF/DF)"*. The Device ID values are listed in table of ID Definitions. If the one-byte address is initially set to 01h, then the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.


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**Table 8. ID Definitions**

| Command Type | MX25U8033E | | |
|---|---|---|---|
| RDID (JEDEC ID) | manufacturer ID | memory type | memory density |
| | C2 | 25 | 34 |
| RES | electronic ID | | |
| | 34 | | |
| REMS/REMS2/REMS4 | manufacturer ID | device ID | |
| | C2 | 34 | |

### 10-21. Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 4K-bit secured OTP mode. While device is in 4K-bit secured OTP mode, main array access is not available. The additional 4K-bit secured OTP is independent from main array, and may be used to store unique serial number for system identifier. After entering the Secured OTP mode, follow standard read or program procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low→ sending ENSO instruction to enter Secured OTP mode→ CS# goes high.

Please note that WRSR/WRSCUR/WPSEL commands are not acceptable during the access of secure OTP region, once security OTP is lock down, only read related commands are valid.

### 10-22. Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 4K-bit secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low→ sending EXSO instruction to exit Secured OTP mode→ CS# goes high.

### 10-23. Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low→sending RDSCUR instruction→Security Register data out on SO→ CS# goes high. (Please see *"Figure 41. Read Security Register (RDSCUR) Sequence (Command 2B)"*)

The definition of the Security Register bits is as below:

**Secured OTP Indicator bit.** The Secured OTP indicator bit shows the chip is locked by factory or not. When it is "0", it indicates non-factory lock; "1" indicates factory-lock.

**Lock-down Secured OTP (LDSO) bit.** By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 4K-bit Secured OTP area cannot be updated any more.


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**Table 9. Security Register Definition**

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| WPSEL | E_FAIL | P_FAIL | Reserved | Reserved | Reserved | LDSO (indicate if lock-down) | Secured OTP indicator bit |
| 0=Software Protect Mode (SPM) 1=Individual Protect mode (default=0) | 0=normal Erase succeed 1=indicate Erase failed (default=0) | 0=normal Program succeed 1=indicate Program failed (default=0) | - | - | - | 0 = not lock-down 1 = lock-down (cannot program/ erase OTP) | 0 = non-factory lock 1 = factory lock |
| Non-volatile bit (OTP) | Volatile bit | Volatile bit | Volatile bit | Volatile bit | Volatile bit | Non-volatile bit (OTP) | Non-volatile bit (OTP) |

### 10-24. Write Security Register (WRSCUR)

The WRSCUR instruction is for setting the values of Security Register Bits. The WREN (Write Enable) instruction is required before issuing WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 4K-bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more. The LDSO bit is an OTP bit. Once the LDSO bit is set, the value of LDSO bit can not be altered any more.

The sequence of issuing WRSCUR instruction is :CS# goes low→ sending WRSCUR instruction → CS# goes high. (Please see *"Figure 42. Write Security Register (WRSCUR) Sequence (Command 2F)"*)

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

### 10-25. Write Protection Selection (WPSEL)

When the system accepts and executes WPSEL instruction, bit 7 in the security register will be set. The WREN (Write Enable) instruction is required before issuing WPSEL instruction. It will activate SBLK, SBULK, RDBLOCK, GBLK, GBULK etc instructions to conduct block lock protection and replace the original Software Protect Mode (SPM) use (BP3-BP0) indicated block methods.

The WPSEL bit of the Security Register selects between SPM (Software Protection Mode) and Individual Block Lock Mode. If WPSEL is “0” (factory default), SPM is enabled and Individual Block Lock Mode is disabled. If WPSEL is “1”, Individual Block Lock Mode is enabled and SPM is disabled.

The sequence of issuing WPSEL instruction is: CS# goes low → send WPSEL instruction to enter the individual block protect mode→ CS# goes high.

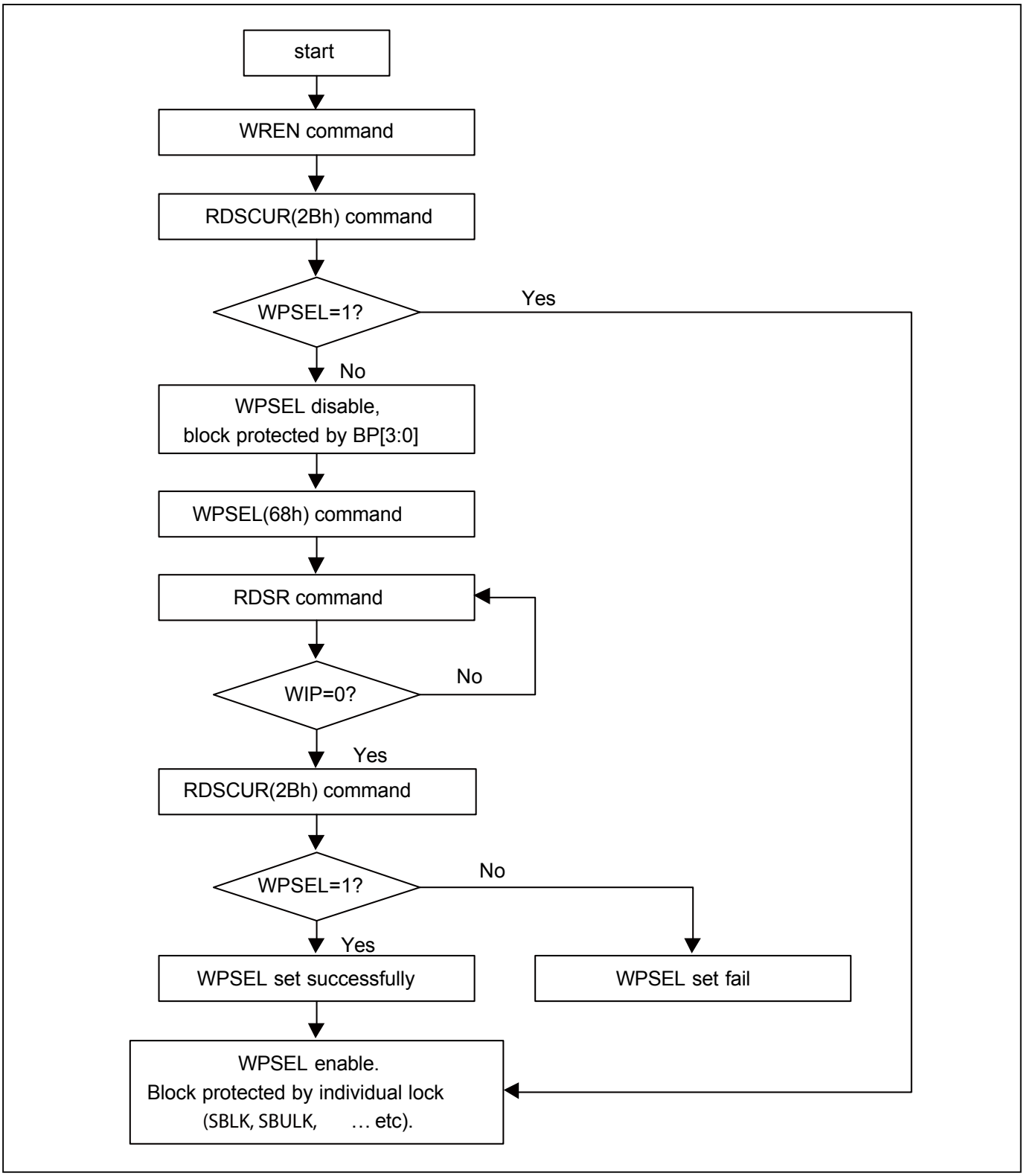
Every time after the system is powered-on the Security Register bit 7 is checked, if WPSEL=1, then all the blocks and sectors will be write-protected by default. User may only unlock the blocks or sectors via SBULK and GBULK instructions. Program or erase functions can only be operated after the Unlock instruction is executed.

Once WPSEL is set, it cannot be changed.


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WPSEL instruction function flow is as follows:

**Figure 6. WPSEL Flow**





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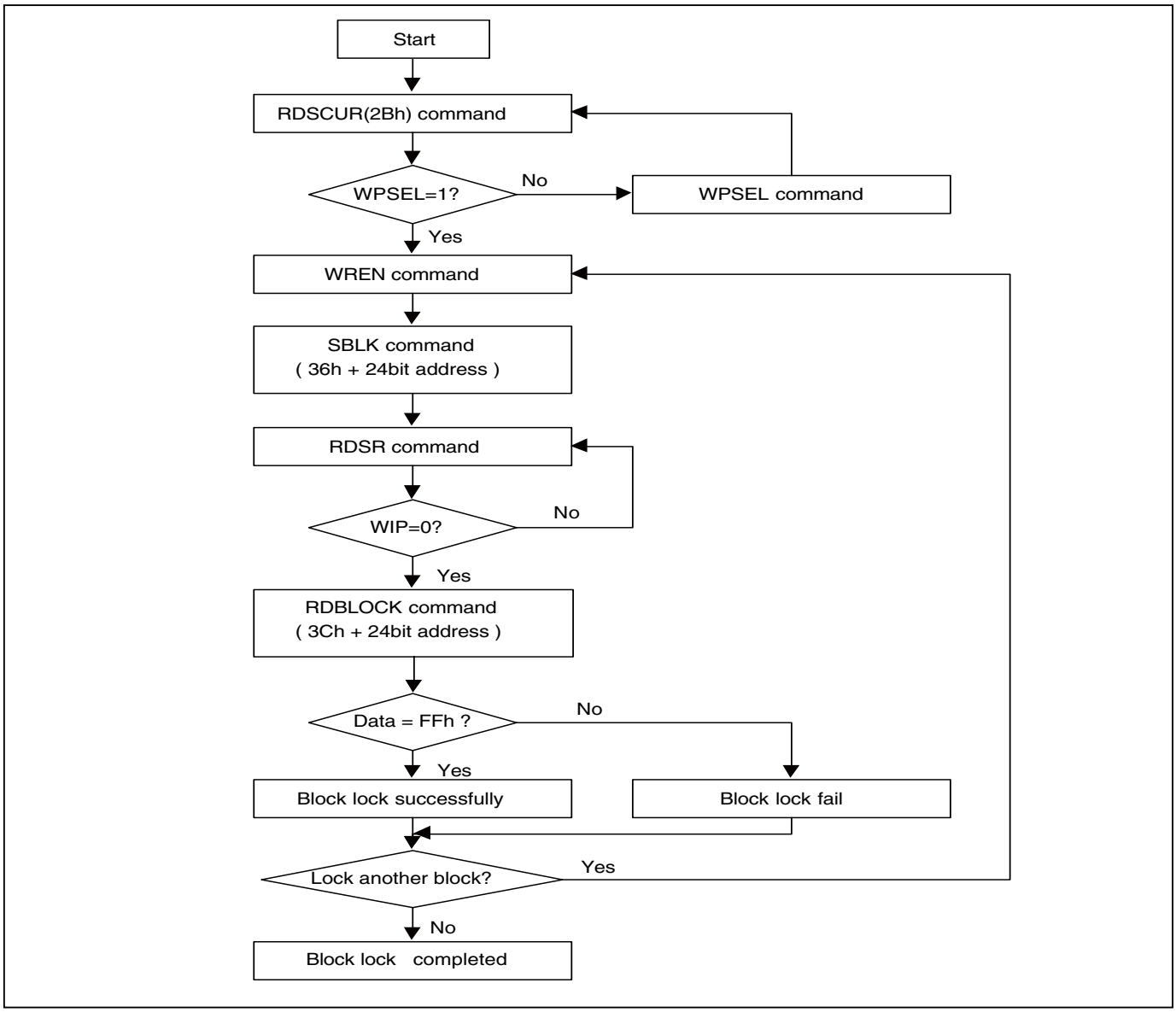
### 10-26. Single Block Lock/Unlock Protection (SBLK/SBULK)

These instructions are only effective after WPSEL was executed. The SBLK instruction is for write protection a specified block (or sector) of memory, using $A_{MAX}$-A16 or ($A_{MAX}$-A12) address bits to assign a 64Kbyte block (or 4K bytes sector) to be protected as read only. The SBULK instruction will cancel the block (or sector) write protection state. This feature allows user to stop protecting the entire block (or sector) through the chip unprotect command (GBULK).

The WREN (Write Enable) instruction is required before issuing SBLK/SBULK instruction.
The sequence of issuing SBLK/SBULK instruction is: CS# goes low → send SBLK/SBULK (36h/39h) instruction→send 3 address bytes assign one block (or sector) to be protected on SI pin → CS# goes high. The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not be executed.

SBLK/SBULK instruction function flow is as follows:

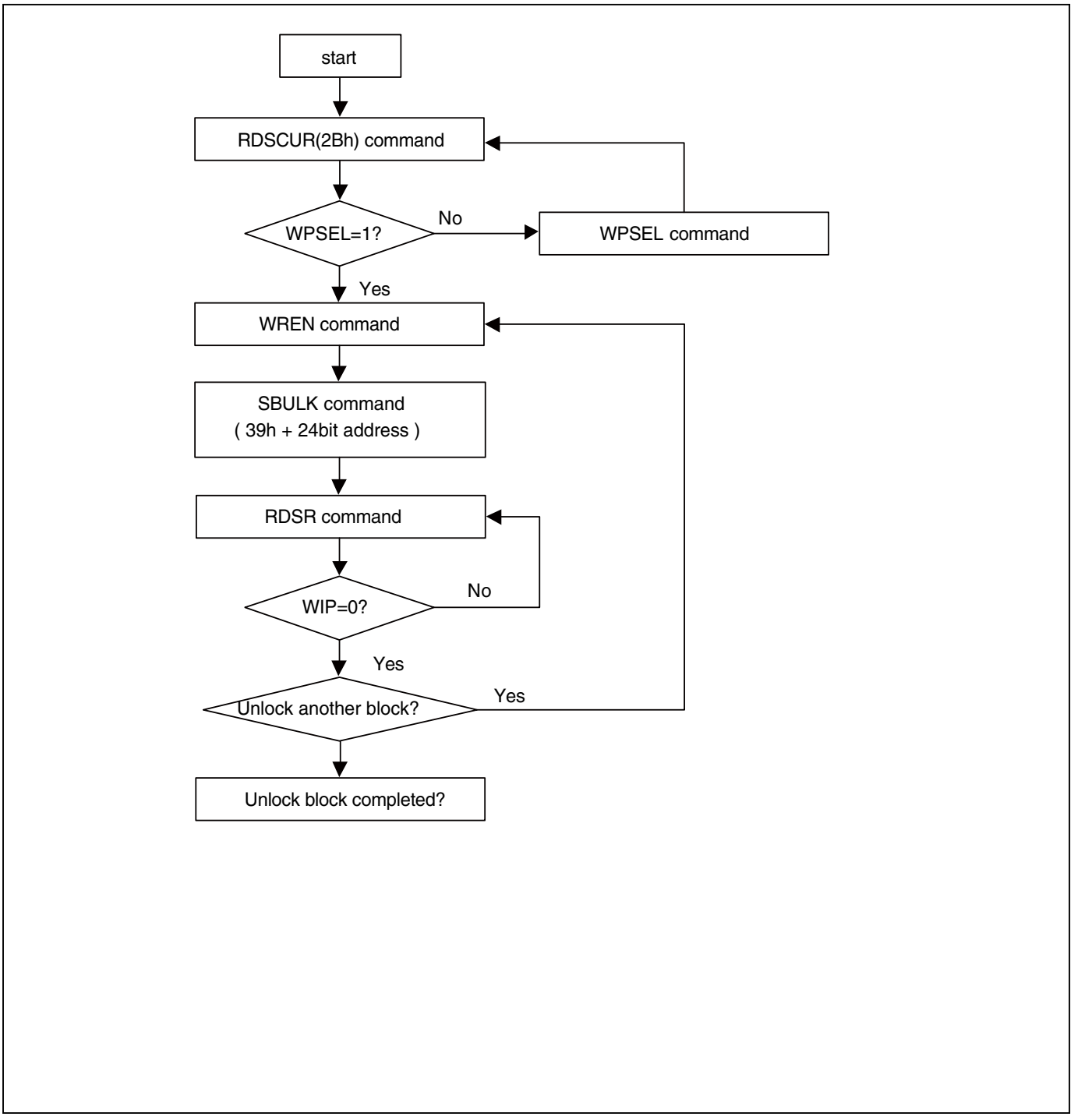
**Figure 7. Block Lock Flow**





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**Figure 8. Block Unlock Flow**





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### 10-27. Read Block Lock Status (RDBLOCK)

This instruction is only effective after WPSEL was executed. The RDBLOCK instruction is for reading the status of protection lock of a specified block (or sector), using AMAX-A16 (or AMAX-A12) address bits to assign a 64K bytes block (4K bytes sector) and read protection lock status bit which the first byte of Read-out cycle. The status bit is"1" to indicate that this block has be protected, that user can read only but cannot write/program /erase this block. The status bit is "0" to indicate that this block hasn't be protected, and user can read and write this block.

The sequence of issuing RDBLOCK instruction is: CS# goes low → send RDBLOCK (3Ch) instruction → send 3 address bytes to assign one block on SI pin → read block's protection lock status bit on SO pin → CS# goes high.

### 10-28. Gang Block Lock/Unlock (GBLK/GBULK)

These instructions are only effective after WPSEL was executed. The GBLK/GBULK instruction is for enable/disable the lock protection block of the whole chip.

The WREN (Write Enable) instruction is required before issuing GBLK/GBULK instruction.
The sequence of issuing GBLK/GBULK instruction is: CS# goes low → send GBLK/GBULK (7Eh/98h) instruction →CS# goes high.

The CS# must go high exactly at the byte boundary, otherwise, the instruction will be rejected and not be executed.

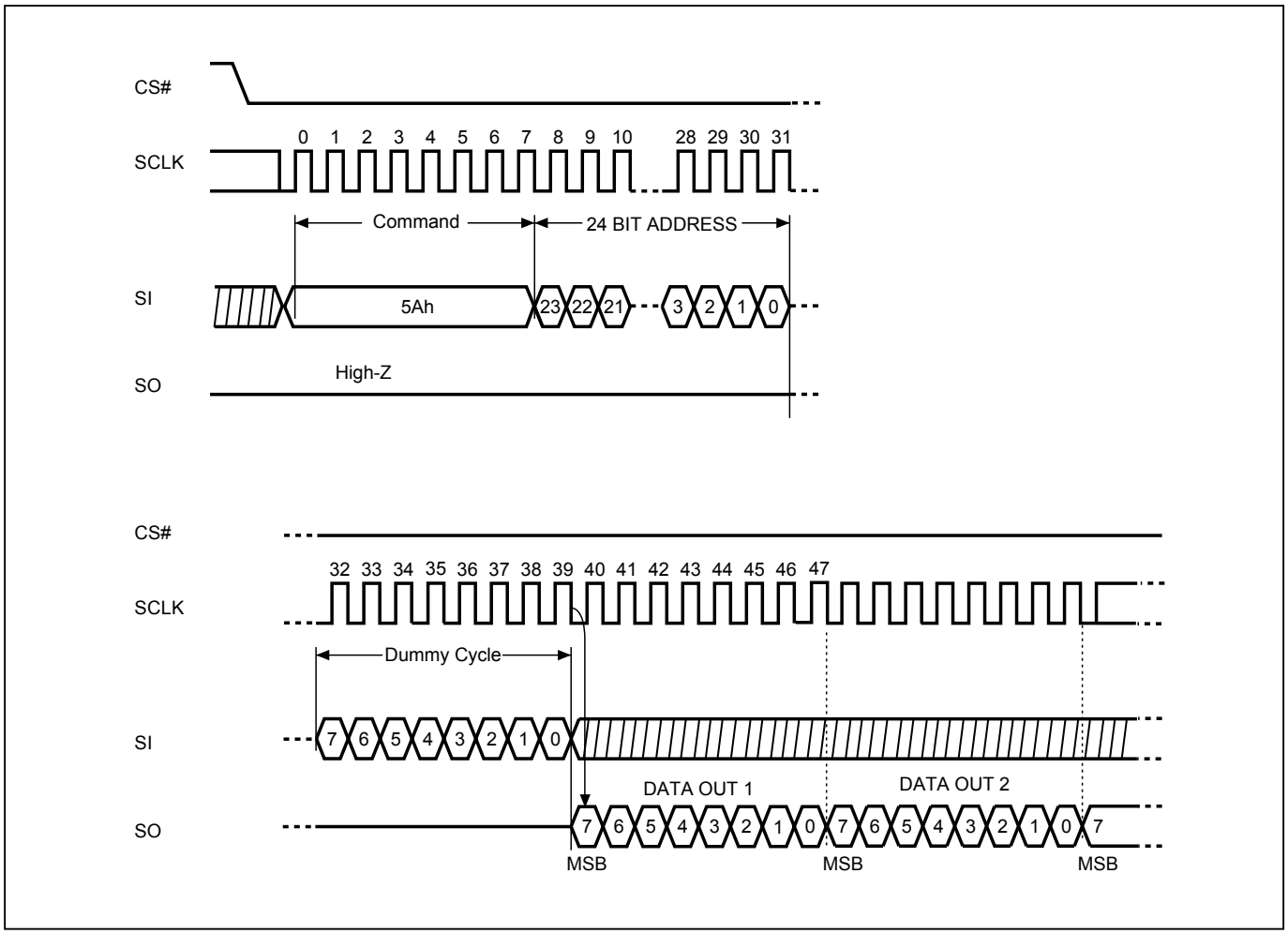
### 10-29. Read SFDP Mode (RDSFDP)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is CS# goes low→send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→send 1 dummy byte on SI pin→read SFDP code on SO→to end RDSFDP operation can use CS# to high at any time during data out.

SFDP is a JEDEC Standard, JESD216.

**Figure 9. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence**





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**Table 10. Signature and Parameter Identification Data Values**

SFDP Table below is for MX25U8033EM1I-12G, MX25U8033EZNI-12G, MX25U8033EZUI-12G, MX25U8033EM2I-12G, MX25U8033EBAI-12G and MX25U8033EBCI-12G

| Description | Comment | Add (h) (Byte) | DW Add (Bit) | Data (h/b) (Note1) | Data (h) |
|---|---|---|---|---|---|
| SFDP Signature | Fixed: 50444653h | 00h | 07:00 | 53h | 53h |
| | | 01h | 15:08 | 46h | 46h |
| | | 02h | 23:16 | 44h | 44h |
| | | 03h | 31:24 | 50h | 50h |
| SFDP Minor Revision Number | Start from 00h | 04h | 07:00 | 00h | 00h |
| SFDP Major Revision Number | Start from 01h | 05h | 15:08 | 01h | 01h |
| Number of Parameter Headers | This number is 0-based. Therefore, 0 indicates 1 parameter header. | 06h | 23:16 | 01h | 01h |
| Unused | | 07h | 31:24 | FFh | FFh |
| ID number (JEDEC) | 00h: it indicates a JEDEC specified header. | 08h | 07:00 | 00h | 00h |
| Parameter Table Minor Revision Number | Start from 00h | 09h | 15:08 | 00h | 00h |
| Parameter Table Major Revision Number | Start from 01h | 0Ah | 23:16 | 01h | 01h |
| Parameter Table Length (in double word) | How many DWORDs in the Parameter table | 0Bh | 31:24 | 09h | 09h |
| Parameter Table Pointer (PTP) | First address of JEDEC Flash Parameter table | 0Ch | 07:00 | 30h | 30h |
| | | 0Dh | 15:08 | 00h | 00h |
| | | 0Eh | 23:16 | 00h | 00h |
| Unused | | 0Fh | 31:24 | FFh | FFh |
| ID number (Macronix manufacturer ID) | it indicates Macronix manufacturer ID | 10h | 07:00 | C2h | C2h |
| Parameter Table Minor Revision Number | Start from 00h | 11h | 15:08 | 00h | 00h |
| Parameter Table Major Revision Number | Start from 01h | 12h | 23:16 | 01h | 01h |
| Parameter Table Length (in double word) | How many DWORDs in the Parameter table | 13h | 31:24 | 04h | 04h |
| Parameter Table Pointer (PTP) | First address of Macronix Flash Parameter table | 14h | 07:00 | 60h | 60h |
| | | 15h | 15:08 | 00h | 00h |
| | | 16h | 23:16 | 00h | 00h |
| Unused | | 17h | 31:24 | FFh | FFh |


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**Table 11. Parameter Table (0): JEDEC Flash Parameter Tables**

SFDP Table below is for MX25U8033EM1I-12G, MX25U8033EZNI-12G, MX25U8033EZUI-12G, MX25U8033EM2I-12G, MX25U8033EBAI-12G and MX25U8033EBCI-12G

| Description | Comment | Add (h) (Byte) | DW Add (Bit) | Data (h/b) (Note1) | Data (h) |
|---|---|---|---|---|---|
| Block/Sector Erase sizes | 00: Reserved, 01: 4KB erase,<br>10: Reserved,<br>11: not support 4KB erase | 30h | 01:00 | 01b | E5h |
| Write Granularity | 0: 1Byte, 1: 64Byte or larger | | 02 | 1b | |
| Write Enable Instruction Required for Writing to Volatile Status Registers | 0: not required<br>1: required 00h to be written to the status register | | 03 | 0b | |
| Write Enable Opcode Select for Writing to Volatile Status Registers | 0: use 50h opcode,<br>1: use 06h opcode<br>Note: If target flash status register is nonvolatile, then bits 3 and 4 must be set to 00b. | | 04 | 0b | |
| Unused | Contains 111b and can never be changed | | 07:05 | 111b | |
| 4KB Erase Opcode | | 31h | 15:08 | 20h | 20h |
| (1-1-2) Fast Read (Note2) | 0=not support 1=support | 32h | 16 | 1b | B1h |
| Address Bytes Number used in addressing flash array | 00: 3Byte only, 01: 3 or 4Byte,<br>10: 4Byte only, 11: Reserved | | 18:17 | 00b | |
| Double Transfer Rate (DTR) Clocking | 0=not support 1=support | | 19 | 0b | |
| (1-2-2) Fast Read | 0=not support 1=support | | 20 | 1b | |
| (1-4-4) Fast Read | 0=not support 1=support | | 21 | 1b | |
| (1-1-4) Fast Read | 0=not support 1=support | | 22 | 0b | |
| Unused | | | 23 | 1b | |
| Unused | | 33h | 31:24 | FFh | FFh |
| Flash Memory Density | | 37h:34h | 31:00 | 007F FFFFh | |
| (1-4-4) Fast Read Number of Wait states (Note3) | 0 0000b: Wait states (Dummy Clocks) not support | 38h | 04:00 | 0 0100b | 44h |
| (1-4-4) Fast Read Number of Mode Bits (Note4) | 000b: Mode Bits not support | | 07:05 | 010b | |
| (1-4-4) Fast Read Opcode | | 39h | 15:08 | EBh | EBh |
| (1-1-4) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 3Ah | 20:16 | 0 0000b | 00h |
| (1-1-4) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 23:21 | 000b | |
| (1-1-4) Fast Read Opcode | | 3Bh | 31:24 | FFh | FFh |


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SFDP Table below is for MX25U8033EM1I-12G, MX25U8033EZNI-12G, MX25U8033EZUI-12G, MX25U8033EM2I-12G, MX25U8033EBAI-12G and MX25U8033EBCI-12G

| Description | Comment | Add (h) (Byte) | DW Add (Bit) | Data (h/b) (Note1) | Data (h) |
|---|---|---|---|---|---|
| (1-1-2) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 3Ch | 04:00 | 0 1000b | 08h |
| (1-1-2) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 07:05 | 000b | |
| (1-1-2) Fast Read Opcode | | 3Dh | 15:08 | 3Bh | 3Bh |
| (1-2-2) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 3Eh | 20:16 | 0 0100b | 04h |
| (1-2-2) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 23:21 | 000b | |
| (1-2-2) Fast Read Opcode | | 3Fh | 31:24 | BBh | BBh |
| (2-2-2) Fast Read | 0=not support 1=support | 40h | 00 | 0b | EEh |
| Unused | | | 03:01 | 111b | |
| (4-4-4) Fast Read | 0=not support 1=support | | 04 | 0b | |
| Unused | | | 07:05 | 111b | |
| Unused | | 43h:41h | 31:08 | FFh | FFh |
| Unused | | 45h:44h | 15:00 | FFh | FFh |
| (2-2-2) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 46h | 20:16 | 0 0000b | 00h |
| (2-2-2) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 23:21 | 000b | |
| (2-2-2) Fast Read Opcode | | 47h | 31:24 | FFh | FFh |
| Unused | | 49h:48h | 15:00 | FFh | FFh |
| (4-4-4) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 4Ah | 20:16 | 0 0000b | 00h |
| (4-4-4) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 23:21 | 000b | |
| (4-4-4) Fast Read Opcode | | 4Bh | 31:24 | FFh | FFh |
| Sector Type 1 Size | Sector/block size = 2^N bytes (Note5)<br>0x00b: this sector type doesn't exist | 4Ch | 07:00 | 0Ch | 0Ch |
| Sector Type 1 erase Opcode | | 4Dh | 15:08 | 20h | 20h |
| Sector Type 2 Size | Sector/block size = 2^N bytes<br>0x00b: this sector type doesn't exist | 4Eh | 23:16 | 0Fh | 0Fh |
| Sector Type 2 erase Opcode | | 4Fh | 31:24 | 52h | 52h |
| Sector Type 3 Size | Sector/block size = 2^N bytes<br>0x00b: this sector type doesn't exist | 50h | 07:00 | 10h | 10h |
| Sector Type 3 erase Opcode | | 51h | 15:08 | D8h | D8h |
| Sector Type 4 Size | Sector/block size = 2^N bytes<br>0x00b: this sector type doesn't exist | 52h | 23:16 | 00h | 00h |
| Sector Type 4 erase Opcode | | 53h | 31:24 | FFh | FFh |


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**Table 12. Parameter Table (1): Macronix Flash Parameter Tables**

SFDP Table below is for MX25U8033EM1I-12G, MX25U8033EZNI-12G, MX25U8033EZUI-12G, MX25U8033EM2I-12G, MX25U8033EBAI-12G and MX25U8033EBCI-12G

| Description | Comment | Add (h) (Byte) | DW Add (Bit) | Data (h/b) (Note1) | Data (h) |
|---|---|---|---|---|---|
| Vcc Supply Maximum Voltage | 2000h=2.000V<br>2700h=2.700V<br>3600h=3.600V | 61h:60h | 07:00<br>15:08 | 00h<br>20h | 00h<br>20h |
| Vcc Supply Minimum Voltage | 1650h=1.650V<br>2250h=2.250V<br>2350h=2.350V<br>2700h=2.700V | 63h:62h | 23:16<br>31:24 | 50h<br>16h | 50h<br>16h |
| H/W Reset# pin | 0=not support 1=support | 65h:64h | 00 | 0b | 4FF6h |
| H/W Hold# pin | 0=not support 1=support | | 01 | 1b | |
| Deep Power Down Mode | 0=not support 1=support | | 02 | 1b | |
| S/W Reset | 0=not support 1=support | | 03 | 0b | |
| S/W Reset Opcode | Reset Enable (66h) should be issued before Reset Opcode | | 11:04 | 1111 1111b (FFh) | |
| Program Suspend/Resume | 0=not support 1=support | | 12 | 0b | |
| Erase Suspend/Resume | 0=not support 1=support | | 13 | 0b | |
| Unused | | | 14 | 1b | |
| Wrap-Around Read mode | 0=not support 1=support | | 15 | 0b | |
| Wrap-Around Read mode Opcode | | 66h | 23:16 | FFh | FFh |
| Wrap-Around Read data length | 08h:support 8B wrap-around read<br>16h:8B&16B<br>32h:8B&16B&32B<br>64h:8B&16B&32B&64B | 67h | 31:24 | FFh | FFh |
| Individual block lock | 0=not support 1=support | 6Bh:68h | 00 | 1b | C8D9h |
| Individual block lock bit (Volatile/Nonvolatile) | 0=Volatile 1=Nonvolatile | | 01 | 0b | |
| Individual block lock Opcode | | | 09:02 | 0011 0110b (36h) | |
| Individual block lock Volatile protect bit default protect status | 0=protect 1=unprotect | | 10 | 0b | |
| Secured OTP | 0=not support 1=support | | 11 | 1b | |
| Read Lock | 0=not support 1=support | | 12 | 0b | |
| Permanent Lock | 0=not support 1=support | | 13 | 0b | |
| Unused | | | 15:14 | 11b | |
| Unused | | | 31:16 | FFh | FFh |
| Unused | | 6Fh:6Ch | 31:00 | FFh | FFh |


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Note 1: h/b is hexadecimal or binary.

Note 2: **(x-y-z)** means I/O mode nomenclature used to indicate the number of active pins used for the opcode (x), address (y), and data (z). At the present time, the only valid Read SFDP instruction modes are: (1-1-1), (2-2-2), and (4-4-4)

Note 3: **Wait States** is required dummy clock cycles after the address bits or optional mode bits.

Note 4: **Mode Bits** is optional control bits that follow the address bits. These bits are driven by the system controller if they are specified. (eg,read performance enhance toggling bits)

Note 5: 4KB=2^0Ch,32KB=2^0Fh,64KB=2^10h

Note 6: All unused and undefined area data is blank FFh for SFDP Tables that are defined in Parameter Identification Header. All other areas beyond defined SFDP Table are reserved by Macronix.

## 11. POWER-ON STATE

The device is at below states when power-up:
- Standby Mode ( please note it is not Deep Power Down Mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level:
- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The read, write, erase, and program command should be sent after the below time delay:
- tVSL after VCC reached VCC minimum level

Note:
- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)


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## 12. ELECTRICAL SPECIFICATIONS

### 12-1. Absolute Maximum Ratings

| RATING | | VALUE |
|---|---|---|
| Ambient Operating Temperature | Industrial grade | -40°C to 85°C |
| Storage Temperature | | -65°C to 150°C |
| Applied Input Voltage | | -0.5V to VCC+0.5V |
| Applied Output Voltage | | -0.5V to VCC+0.5V |
| VCC to Ground Potential | | -0.5V to 2.5V |

NOTICE:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot to VCC+1.0V or -1.0V for period up to 20ns.

**Figure 10. Maximum Negative Overshoot Waveform**

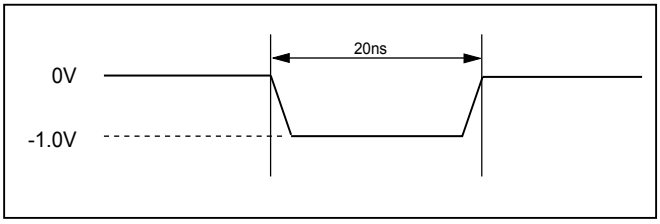
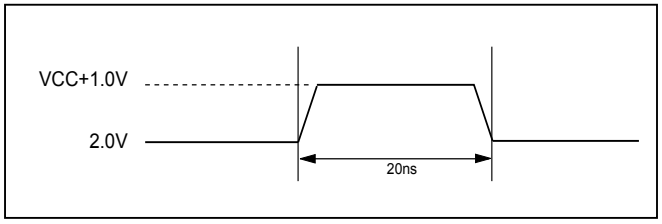



**Figure 11. Maximum Positive Overshoot Waveform**

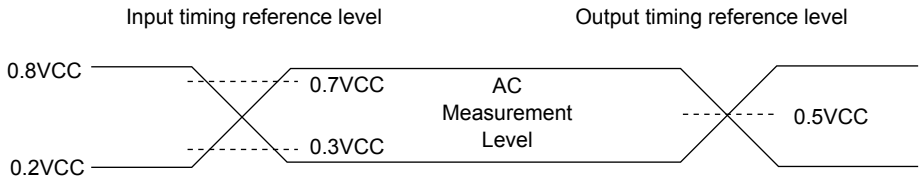



### 12-2. Capacitance TA = 25°C, f = 1.0 MHz

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| CIN | Input Capacitance | | | 6 | pF | VIN = 0V |
| COUT | Output Capacitance | | | 8 | pF | VOUT = 0V |

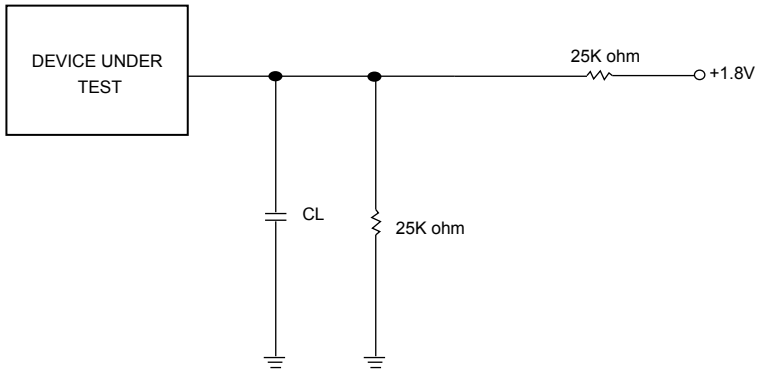

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**Figure 12. Input Test Waveforms and Measurement Level**




Note: Input pulse rise and fall time are <5ns

**Figure 13. Output Loading**




CL=30pF Including jig capacitance

**Figure 14. SCLK TIMING DEFINITION**

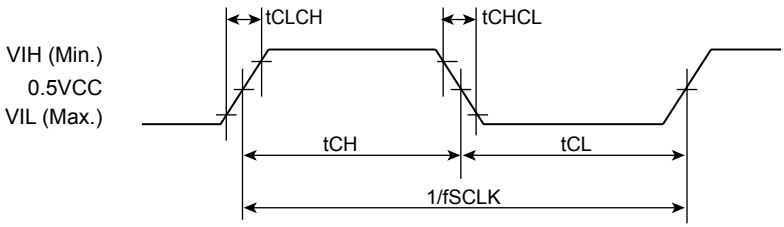


**Table 13. DC Characteristics**

Temperature = -40°C to 85°C, VCC = 1.65V ~ 2.0V

| SYMBOL | PARAMETER | NOTES | MIN. | TYP. | MAX. | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|
| ILI | Input Load Current | 1 | | | ±2 | uA | VCC = VCC Max, VIN = VCC or GND |
| ILO | Output Leakage Current | 1 | | | ±2 | uA | VCC = VCC Max, VOUT = VCC or GND |
| ISB1 | VCC Standby Current | 1 | | 8 | 30 | uA | VIN = VCC or GND, CS# = VCC |
| ISB2 | Deep Power-down Current | | | 2 | 8 | uA | VIN = VCC or GND, CS# = VCC |
| ICC1 | VCC Read | 1 | | | 12 | mA | f=80MHz, SCLK=0.1VCC/0.9VCC, SO=Open |
| | | | | | 7 | mA | f=33MHz, SCLK=0.1VCC/0.9VCC, SO=Open |
| ICC2 | VCC Program Current (PP) | 1 | | 20 | 25 | mA | Program in Progress, CS# = VCC |
| ICC3 | VCC Write Status Register (WRSR) Current | | | 8 | 20 | mA | Program status register in progress, CS#=VCC |
| ICC4 | VCC Sector/Block (32K, 64K) Erase Current (SE/BE/BE32K) | 1 | | 20 | 25 | mA | Erase in Progress, CS#=VCC |
| ICC5 | VCC Chip Erase Current (CE) | 1 | | 20 | 25 | mA | Erase in Progress, CS#=VCC |
| VIL | Input Low Voltage | | -0.5 | | 0.2VCC | V | |
| VIH | Input High Voltage | | 0.8VCC | | VCC+0.4 | V | |
| VOL | Output Low Voltage | | | | 0.2 | V | IOL = 100uA |
| VOH | Output High Voltage | | VCC-0.2 | | | V | IOH = -100uA |

Note 1. Typical values at VCC = 1.8V, T = 25°C. These currents are valid for all product versions (package and speeds).


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**Table 14. AC Characteristics**

Temperature = -40°C to 85°C, VCC = 1.65V ~ 2.0V

| Symbol | Alt. | Parameter | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| fSCLK | fC | Clock Frequency for the following instructions: FAST_READ, RDSFDP, PP, SE, BE, CE, DP, RES, RDP WREN, WRDI, RDID, RDSR, WRSR | | D.C. | | 80 | MHz |
| fRSCLK | fR | Clock Frequency for READ instructions | | | | 50 | MHz |
| fTSCLK | fT | Clock Frequency for 2READ/DREAD instructions | | | | 80 | MHz |
| | fQ | Clock Frequency for 4READ/QREAD instructions | | | | 70 | MHz |
| f4PP | | Clock Frequency for 4PP (Quad page program) | | | | 70 | MHz |
| tCH(1) | tCLH | Clock High Time | Serial (fSCLK) | 6 | | | ns |
| | | | Normal Read (fRSCLK) | 9 | | | ns |
| | | | 4PP (70MHz) | 7 | | | |
| tCL(1) | tCLL | Clock Low Time | Serial (fSCLK) | 6 | | | ns |
| | | | Normal Read (fRSCLK) | 9 | | | ns |
| | | | 4PP (70MHz) | 7 | | | |
| tCLCH(2) | | Clock Rise Time (peak to peak) | | 0.1 | | | V/ns |
| tCHCL(2) | | Clock Fall Time (peak to peak) | | 0.1 | | | V/ns |
| tSLCH | tCSS | CS# Active Setup Time (relative to SCLK) | | 7 | | | ns |
| tCHSL | | CS# Not Active Hold Time (relative to SCLK) | | 5 | | | ns |
| tDVCH | tDSU | Data In Setup Time | | 2 | | | ns |
| tCHDX | tDH | Data In Hold Time | | 5 | | | ns |
| tCHSH | | CS# Active Hold Time (relative to SCLK) | | 5 | | | ns |
| tSHCH | | CS# Not Active Setup Time (relative to SCLK) | | 7 | | | ns |
| tSHSL | tCSH | CS# Deselect Time | From Read to next Read | 12 | | | ns |
| | | | From Write/Erase/Program to Read Status Register | 30 | | | ns |
| tSHQZ(2) | tDIS | Output Disable Time | | | | 8 | ns |
| tHLCH | | HOLD# Active Setup Time (relative to SCLK) | | 4 | | | ns |
| tCHHH | | HOLD# Active Hold Time (relative to SCLK) | | 4 | | | ns |
| tHHCH | | HOLD# Not Active Setup Time (relative to SCLK) | | 4 | | | ns |
| tCHHL | | HOLD# Not Active Hold Time (relative to SCLK) | | 4 | | | ns |
| tHHQX | tLZ | HOLD# to Output Low-Z | | | | 8 | ns |
| tHLQZ | tHZ | HOLD# to Output High-Z | | | | 8 | ns |
| tCLQV | tV | Clock Low to Output Valid Loading: 30pF/15pF | Loading: 30pF | | | 8 | ns |
| | | | Loading: 15pF | | | 6 | ns |
| tCLQX | tHO | Output Hold Time | | 0 | | | ns |
| tWHSL(3) | | Write Protect Setup Time | | 20 | | | ns |
| tSHWL(3) | | Write Protect Hold Time | | 100 | | | ns |
| tDP(2) | | CS# High to Deep Power-down Mode | | | | 10 | us |
| tRES1(2) | | CS# High to Standby Mode without Electronic Signature Read | | | | 10 | us |
| tRES2(2) | | CS# High to Standby Mode with Electronic Signature Read | | | | 10 | us |
| tW | | Write Status Register Cycle Time | | | | 40 | ms |
| tBP | | Byte-Program | | | 10 | 30 | us |
| tPP | | Page Program Cycle Time | | | 1.2 | 3 | ms |
| tSE | | Sector Erase Cycle Time | | | 30 | 200 | ms |
| tBE32 | | Block Erase (32KB) Cycle Time | | | 200 | 1000 | ms |
| tBE | | Block Erase (64KB) Cycle Time | | | 500 | 2000 | ms |
| tCE | | Chip Erase Cycle Time | | | 5 | 10 | s |

Notes:

1. tCH + tCL must be greater than or equal to 1/ Frequency.
2. Value guaranteed by characterization, not 100% tested in production.
3. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
4. Test condition is shown as *"Figure 12. Input Test Waveforms and Measurement Level"*, *"Figure 13. Output Loading"*.


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## 13. Timing Analysis

**Figure 15. Serial Input Timing**

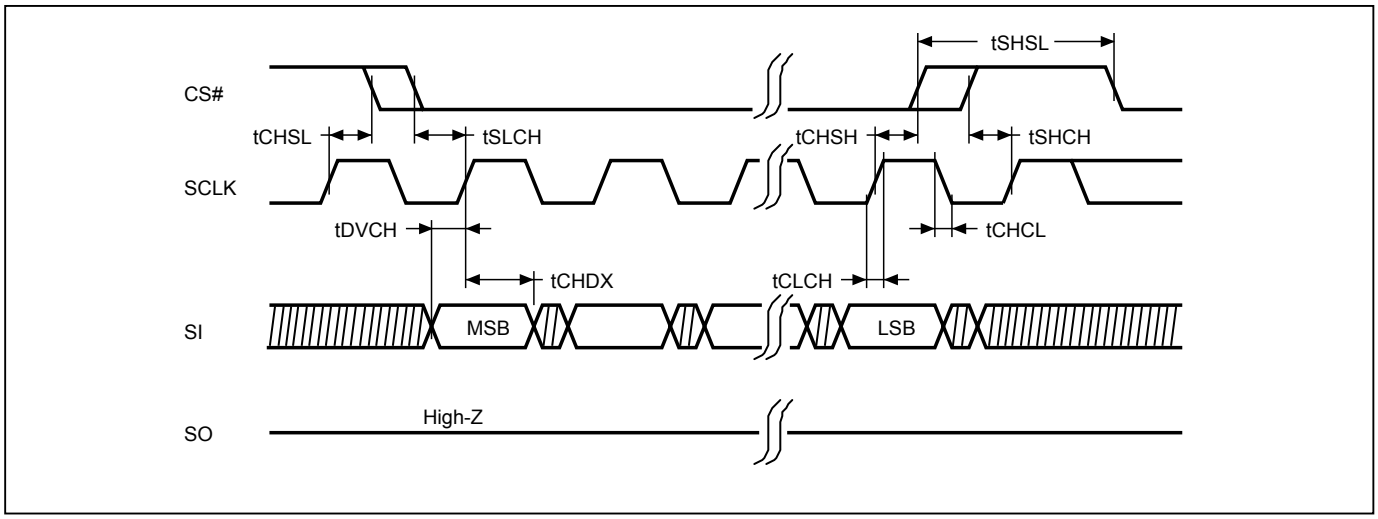



**Figure 16. Output Timing**

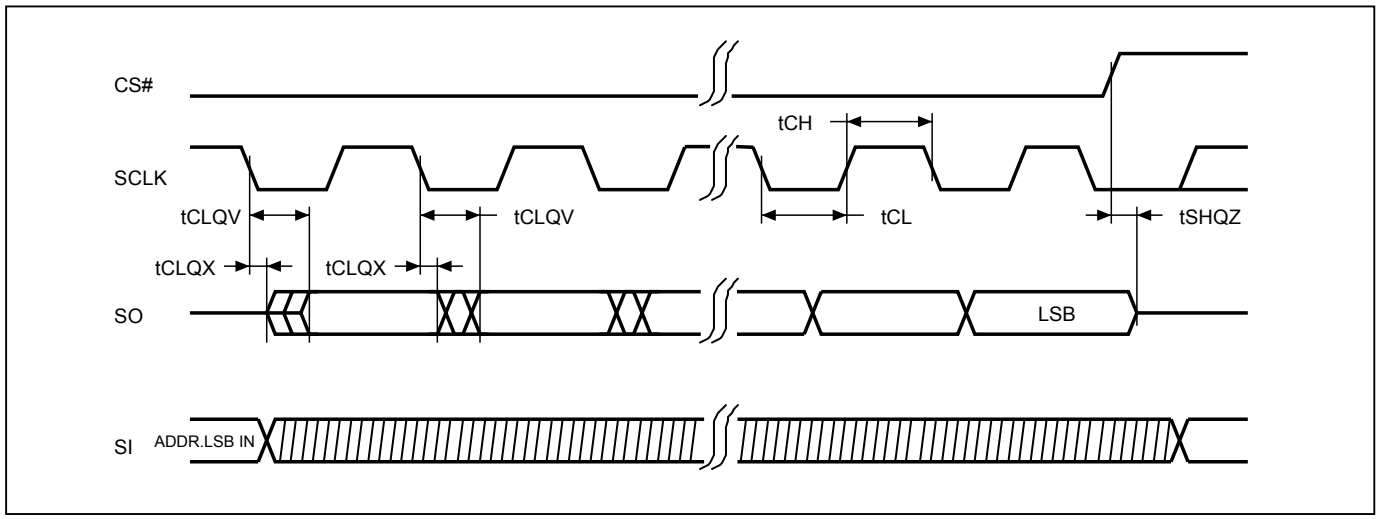


**Figure 17. Hold Timing**

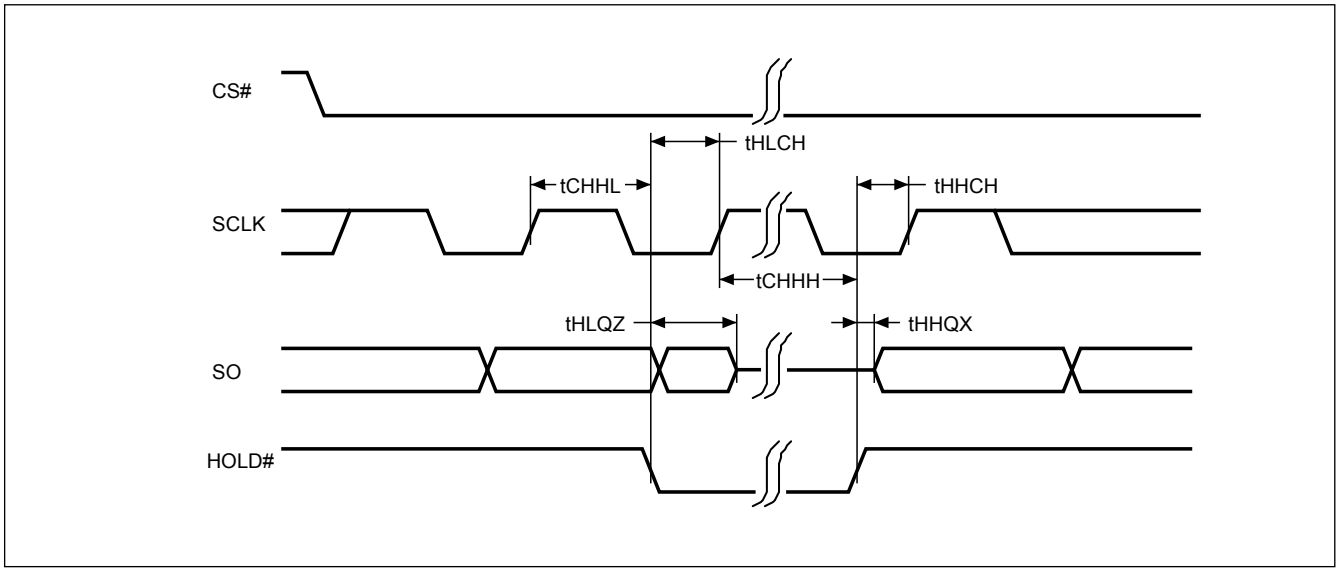



**Figure 18. WP# Setup Timing and Hold Timing during WRSR when SRWD=1**

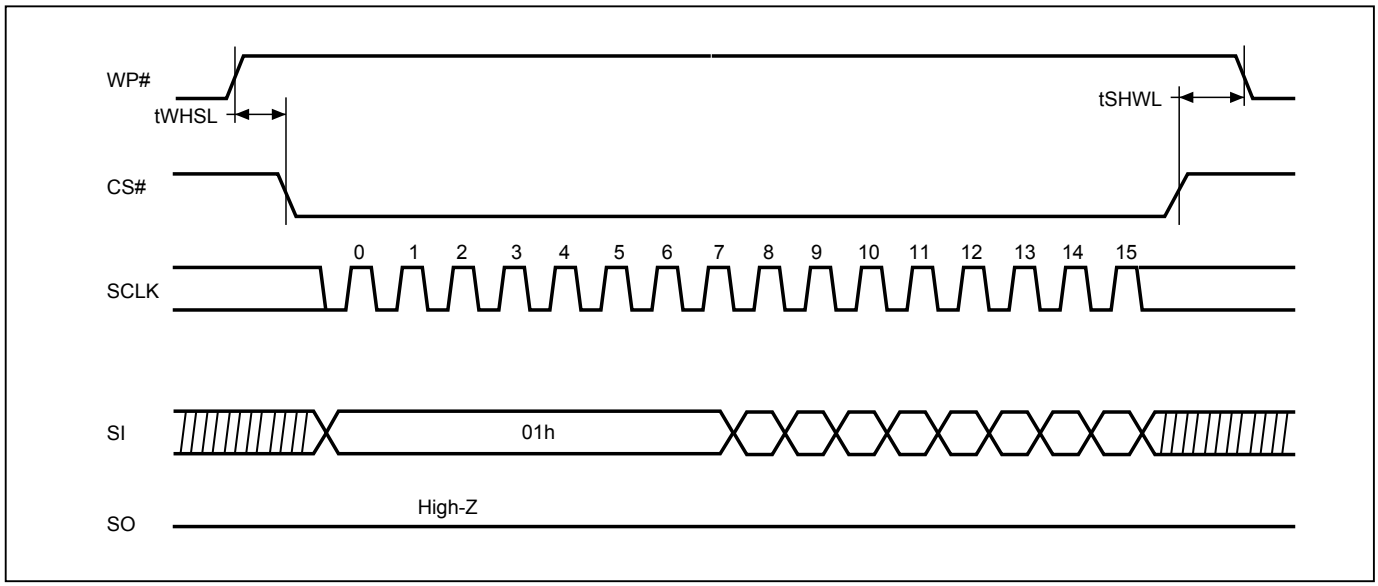
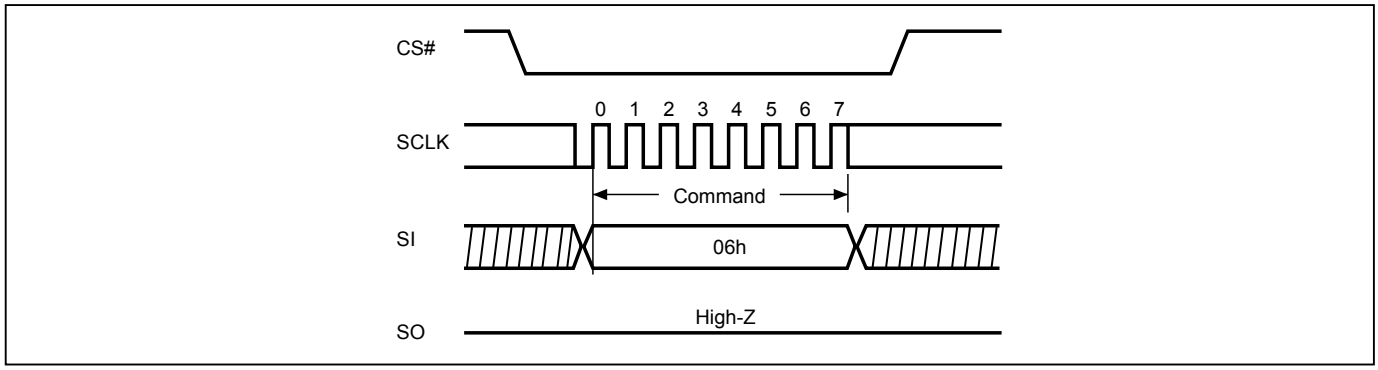



**Figure 19. Write Enable (WREN) Sequence (Command 06)**





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**Figure 20. Write Disable (WRDI) Sequence (Command 04)**

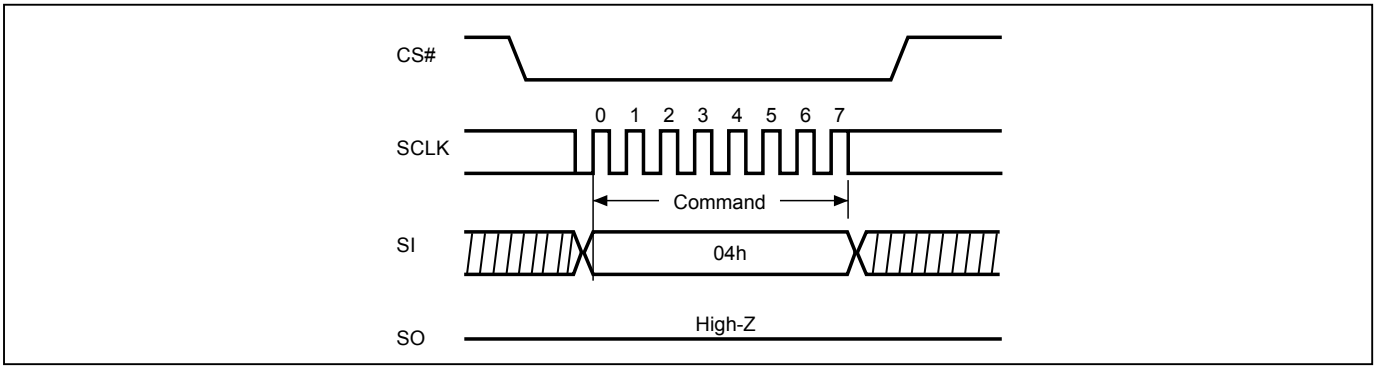



**Figure 21. Read Identification (RDID) Sequence (Command 9F)**

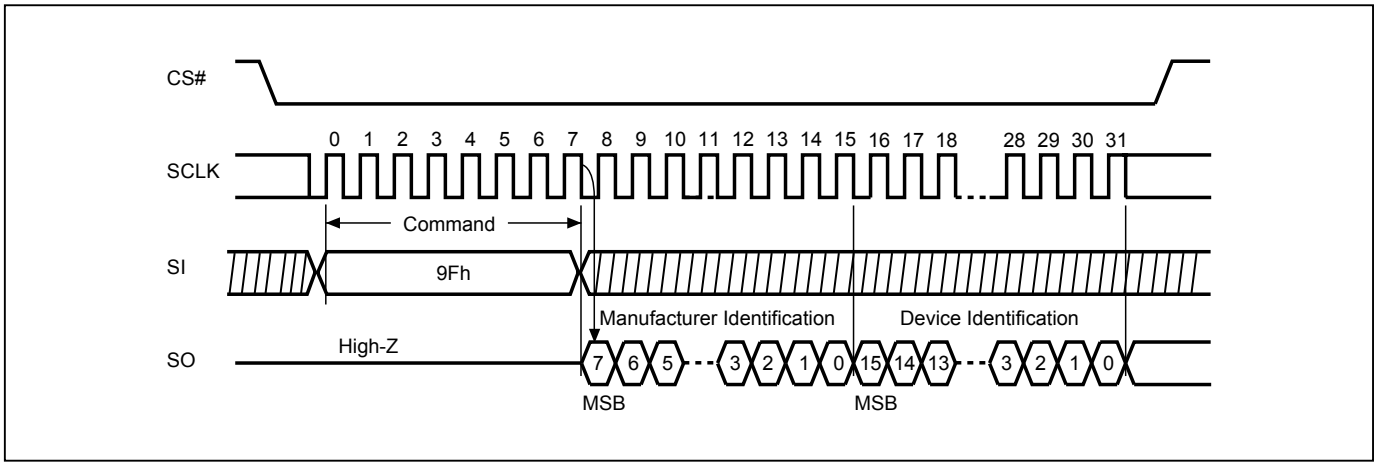
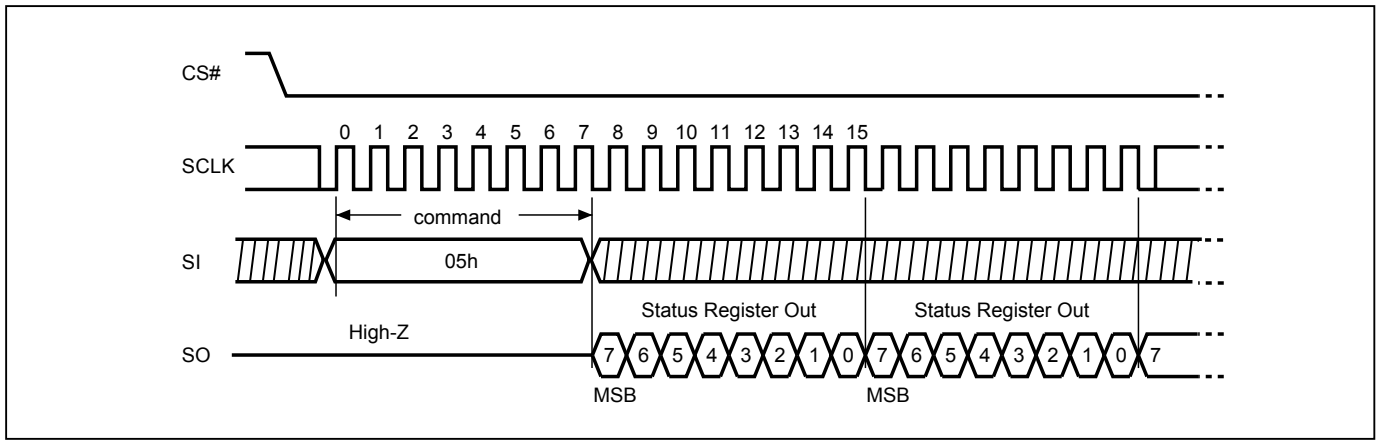



**Figure 22. Read Status Register (RDSR) Sequence (Command 05)**





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**Figure 23. Write Status Register (WRSR) Sequence (Command 01)**

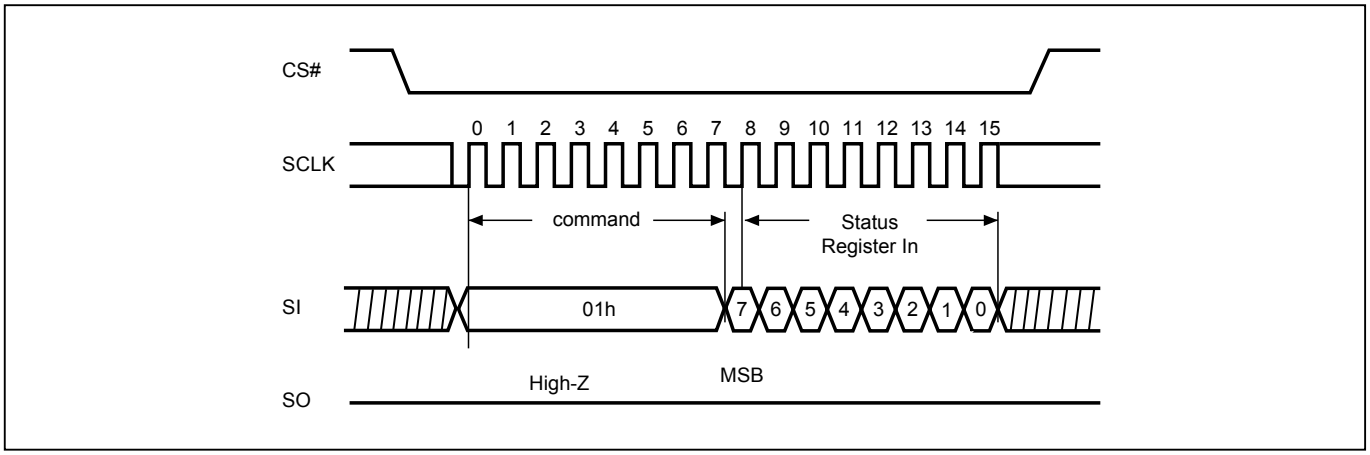



**Figure 24. Read Data Bytes (READ) Sequence (Command 03) (50MHz)**

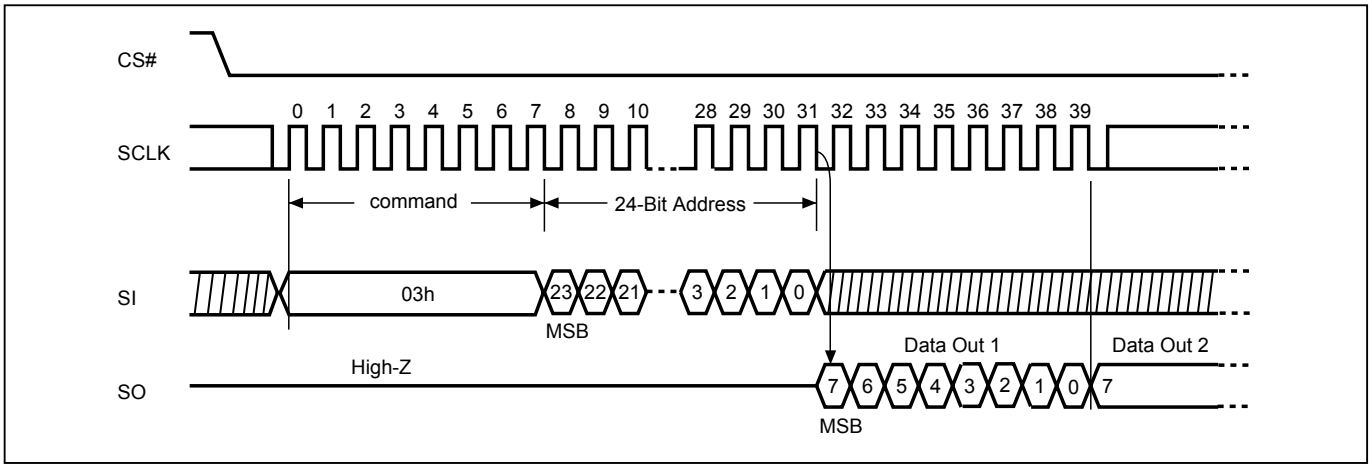


**Figure 25. Read at Higher Speed (FAST_READ) Sequence (Command 0B)**

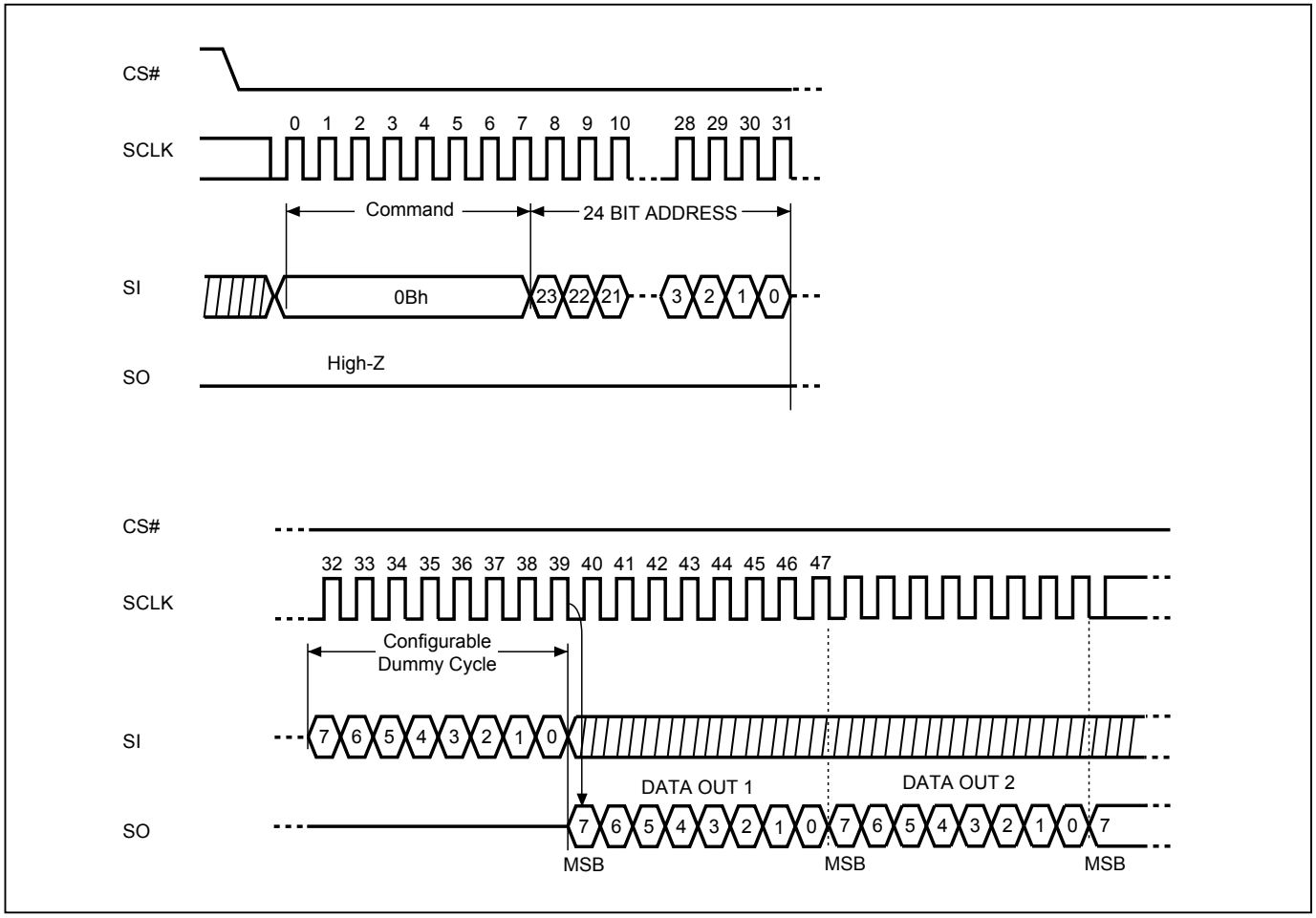
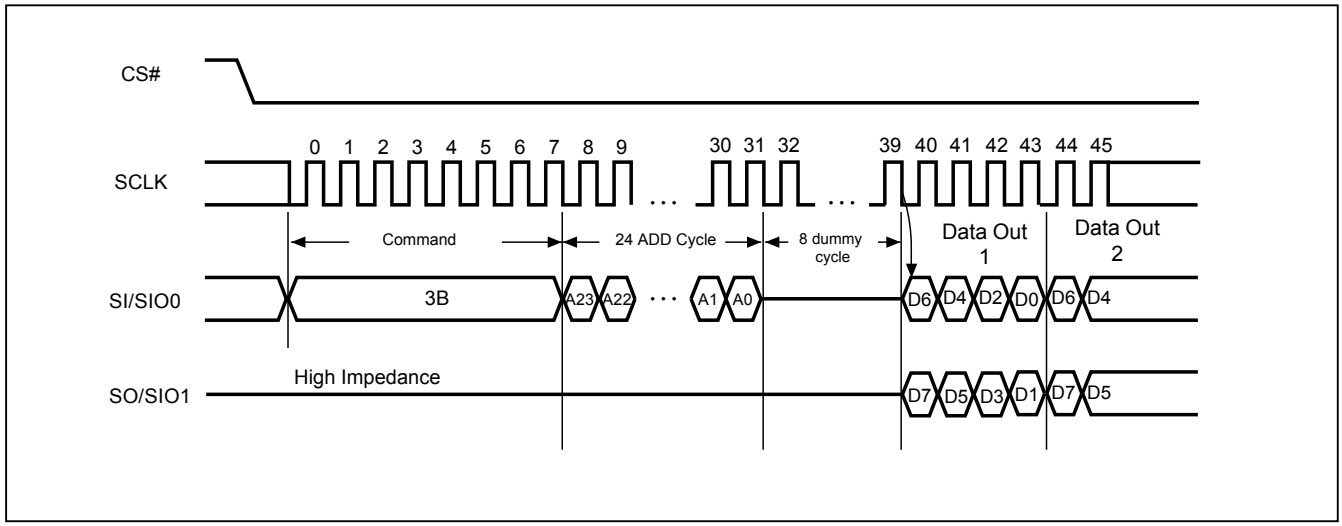


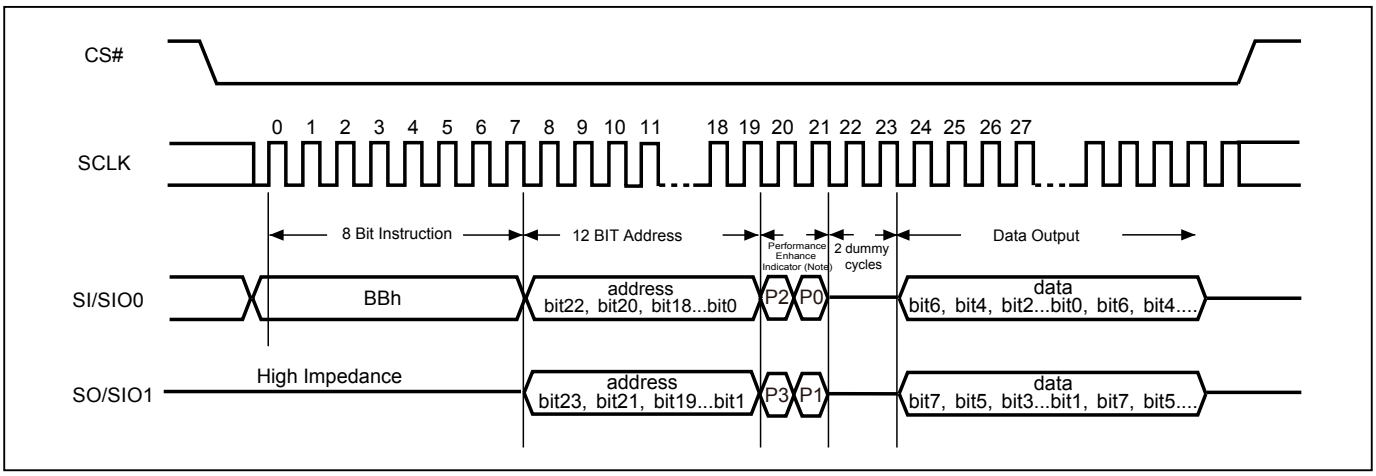

**Figure 26. Dual Read Mode Sequence (Command 3B)**





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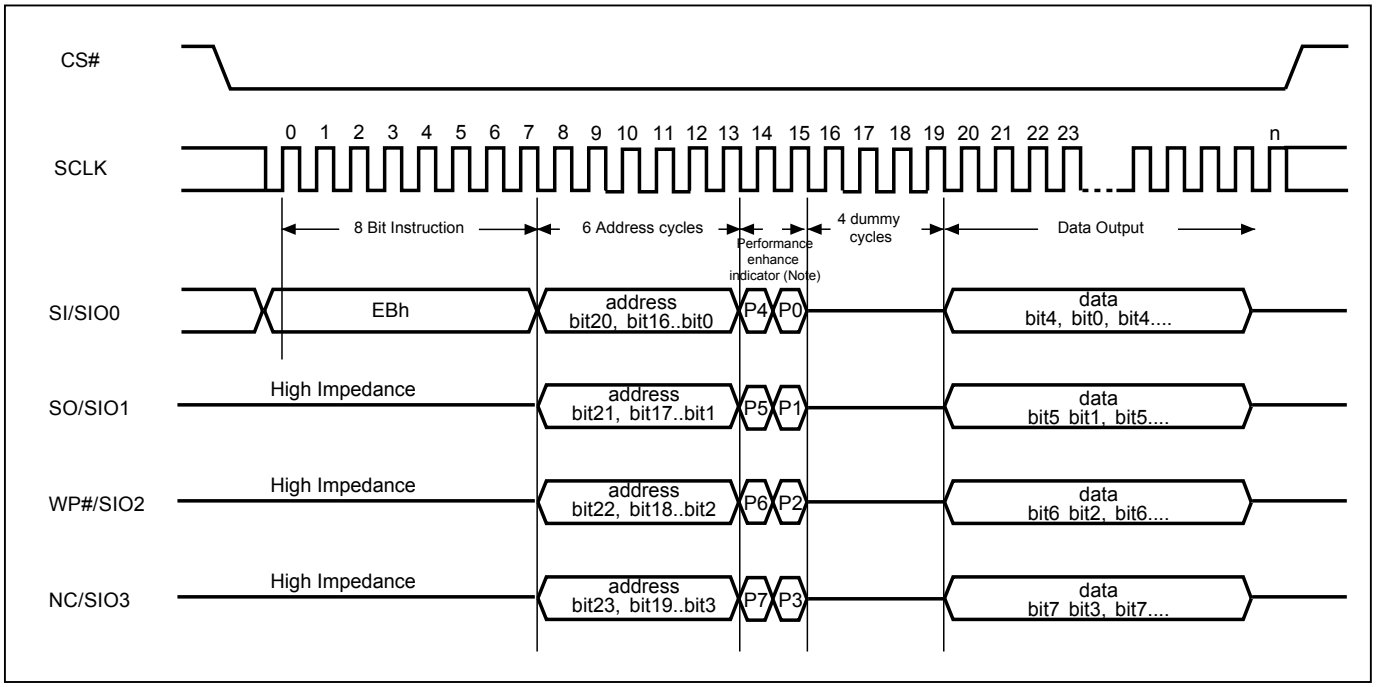
**Figure 27. 2 x I/O Read Mode Sequence (Command BB)**




Notes:

1. Hi-impedance is inhibited for the two clock cycles.
2. P3≠P1 & P2≠P0 (Toggling) is inhibited.

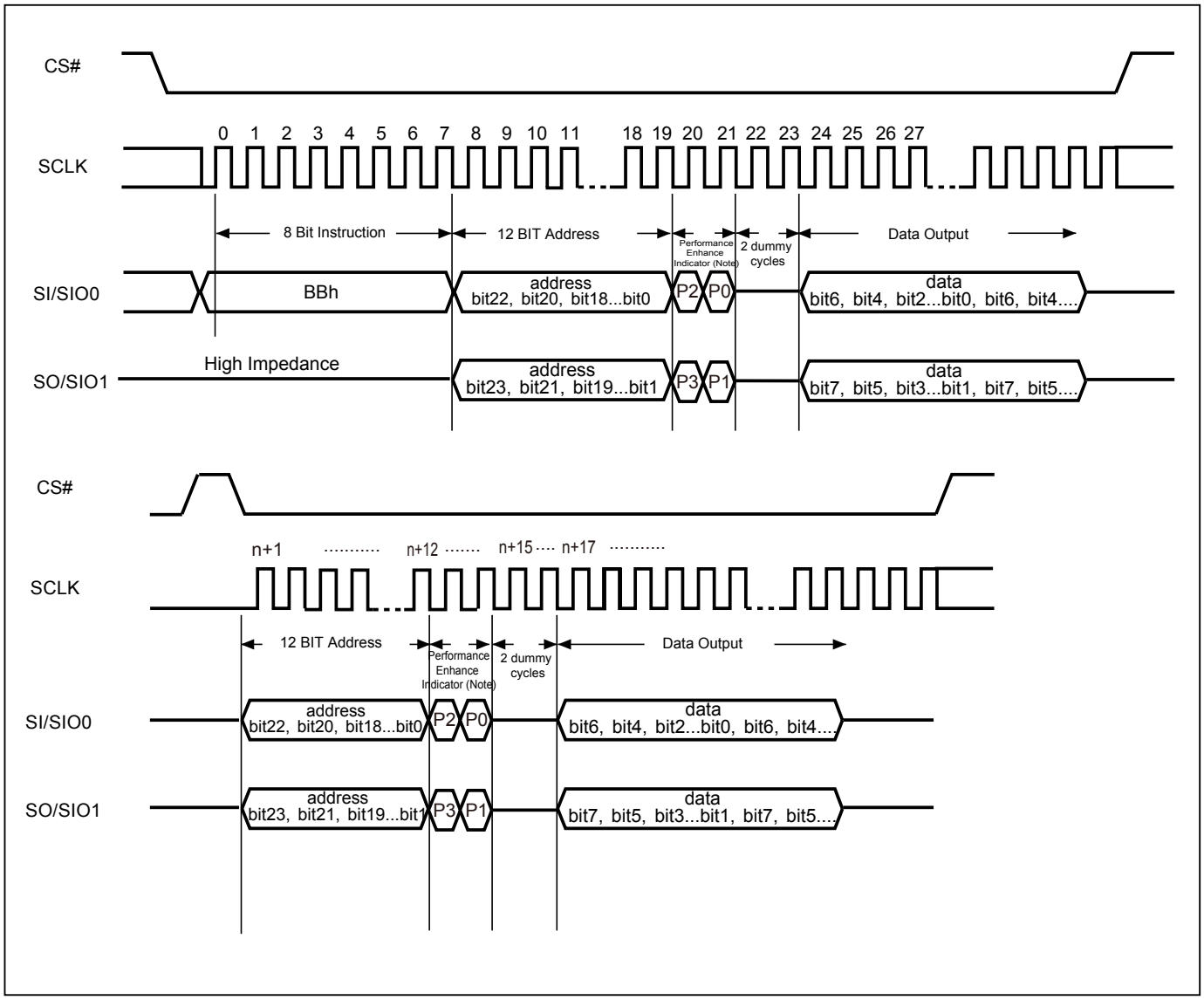
**Figure 28. 4 x I/O Read Mode Sequence (Command EB)**




Notes:

1. Hi-impedance is inhibited for the two clock cycles.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) is inhibited.

**Figure 29. 2 x I/O Read Enhance Performance Mode Sequence (Command BB)**

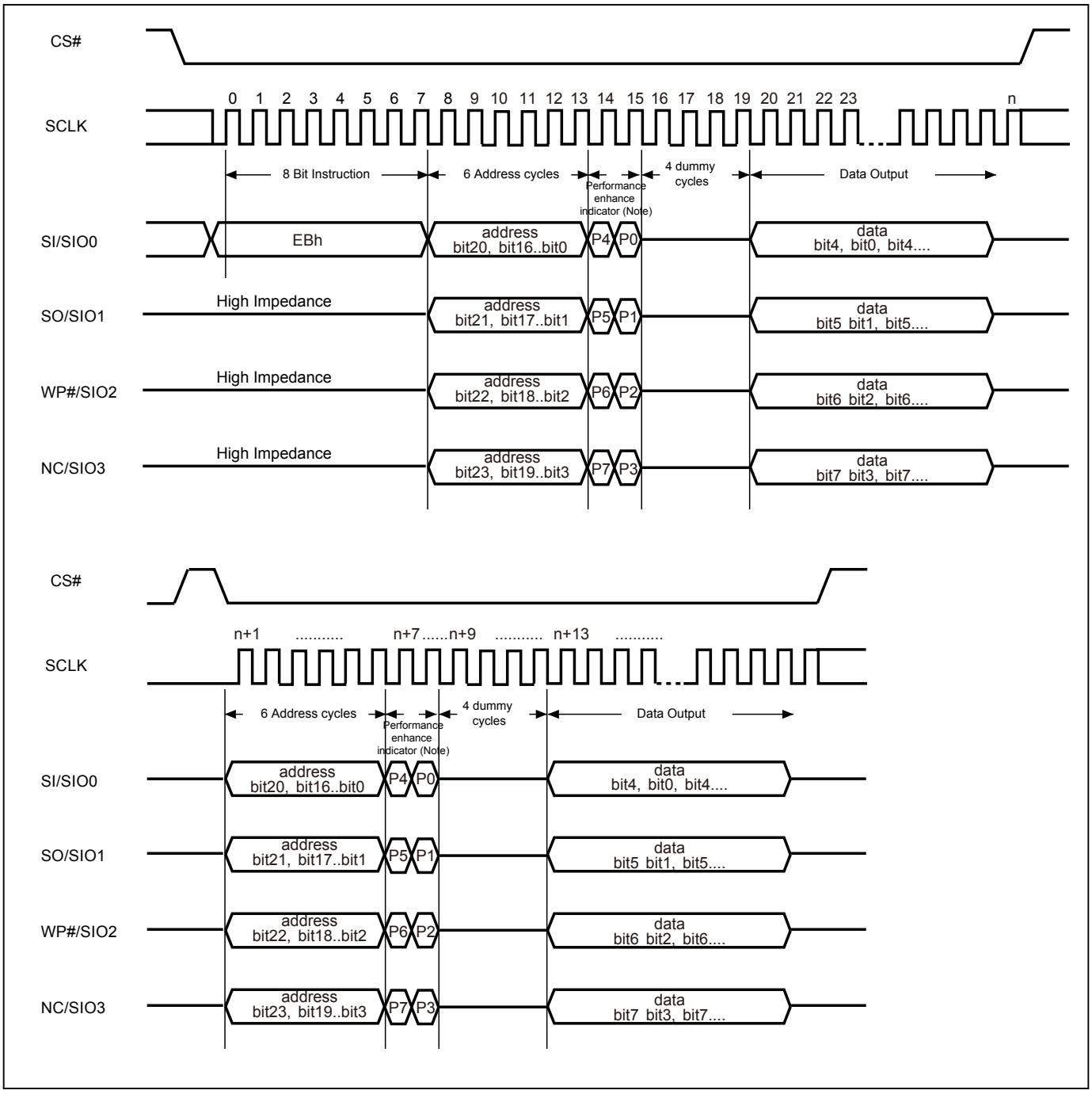



Notes:

1. Performance enhance mode, if P3≠P1 & P2≠P0 (Toggling), ex: 3h, 6h, 9h or Ch.
   Performance enhance recommend to keep 1 or 0 in performance enhance indicator.
2. Reset the performance enhance mode, if P3=P1 or P2=P0 (Not Toggling), ex: 0h, 5h, Ah or Fh.


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**Figure 30. 4 x I/O Read Enhance Performance Mode Sequence (Command EB)**




Notes:

1. Performance enhance mode, if P7≠P3 & P6≠P2 & P5≠P1 & P4≠P0 (Toggling), ex: A5h, 5Ah, 0Fh, F0h. Performance enhance recommend to keep 1 or 0 in performance enhance indicator.
2. Reset the performance enhance mode, if P7=P3 or P6=P2 or P5=P1 or P4=P0 (Not Toggling), ex: AAh, 55h, 00h, FFh.

**Figure 31. Page Program (PP) Sequence (Command 02)**

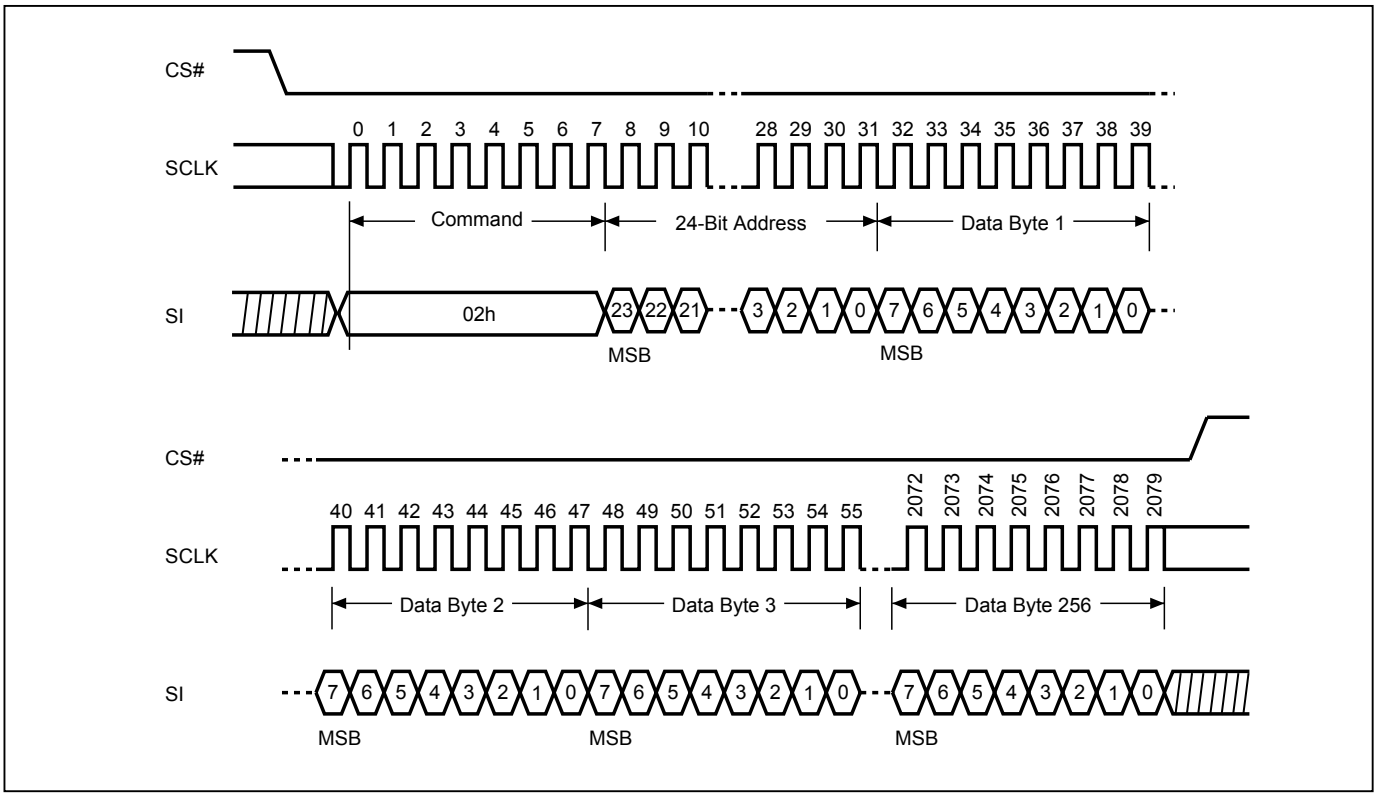
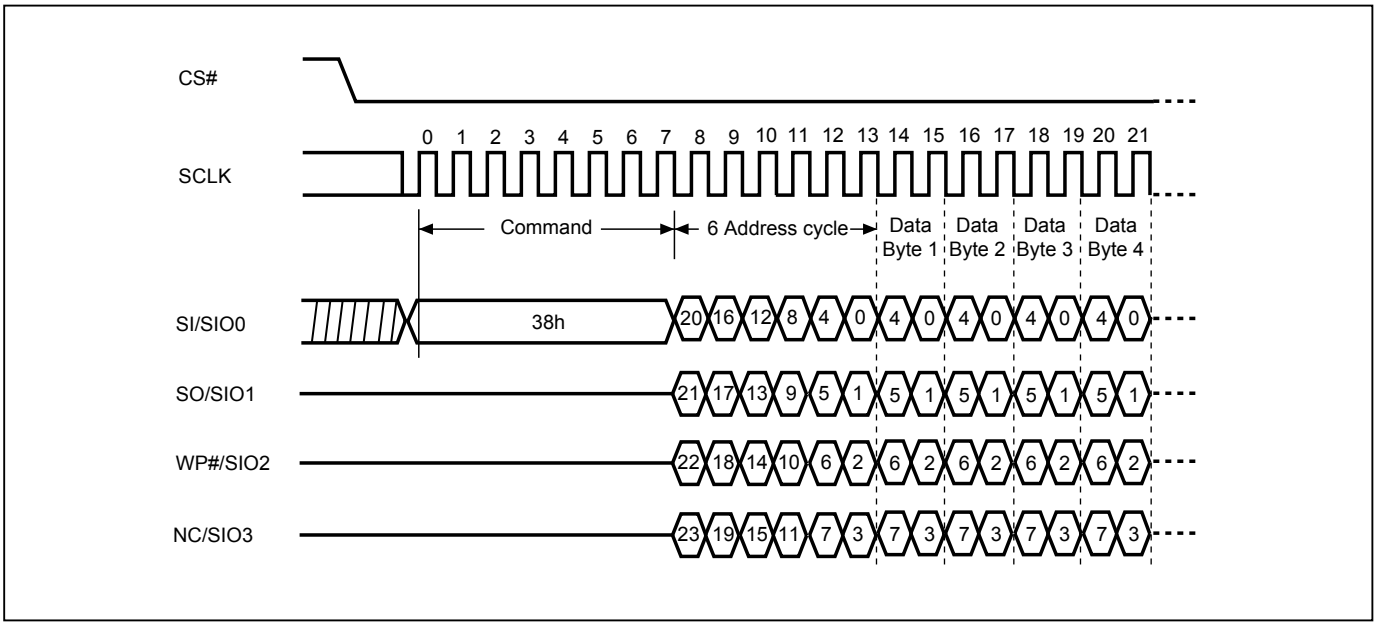



**Figure 32. 4 x I/O Page Program (4PP) Sequence (Command 38)**





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**Figure 33. Sector Erase (SE) Sequence (Command 20)**

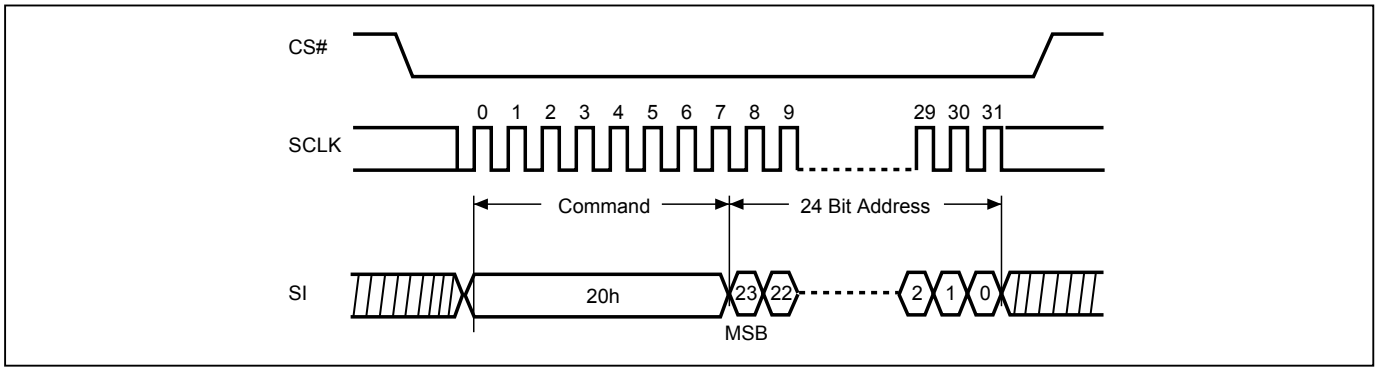



**Figure 34. Block Erase 32KB (BE32K) Sequence (Command 52)**

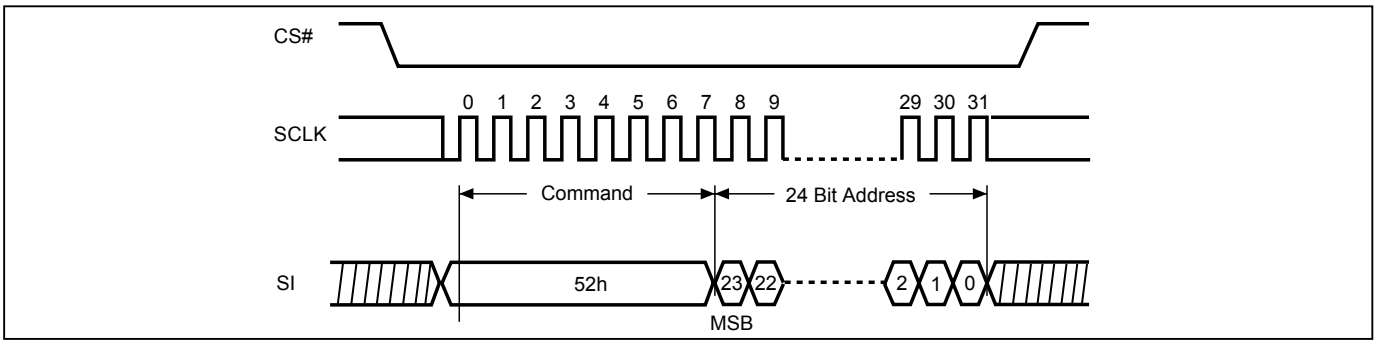



**Figure 35. Block Erase (BE) Sequence (Command D8)**

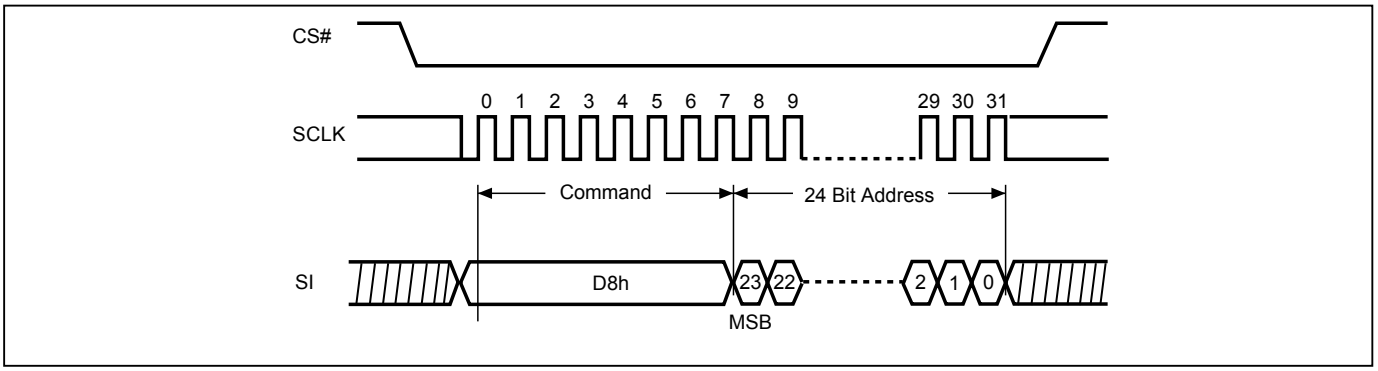
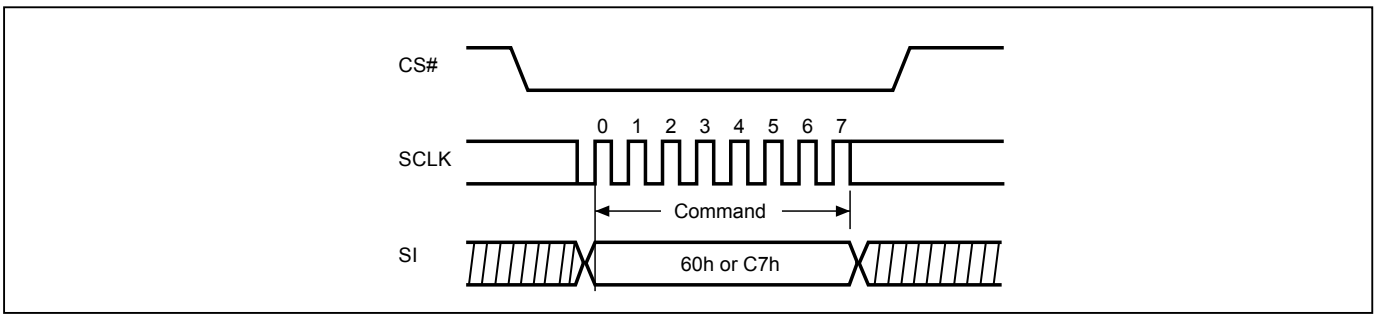



**Figure 36. Chip Erase (CE) Sequence (Command 60 or C7)**





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**Figure 37. Deep Power-down (DP) Sequence (Command B9)**

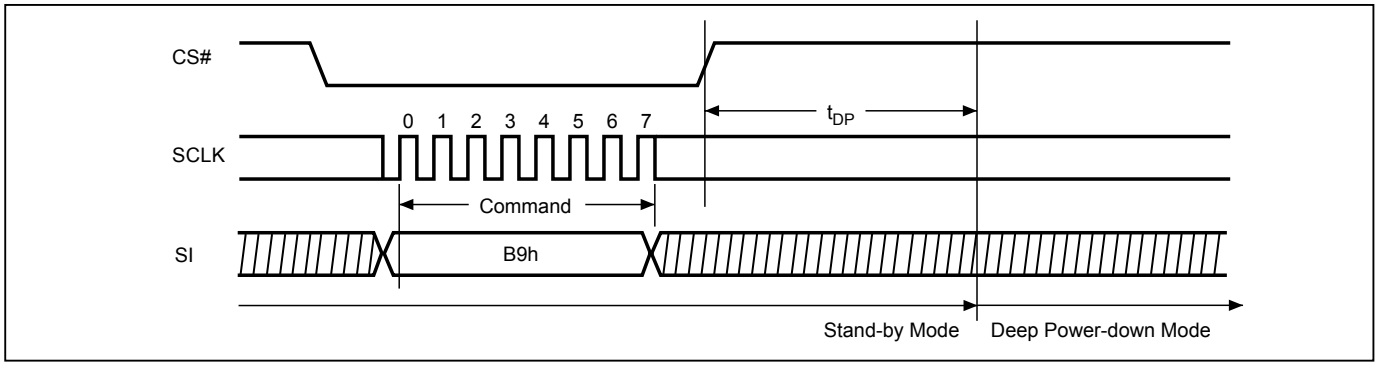



**Figure 38. Release from Deep Power-down and Read Electronic Signature (RES) (Command AB)**

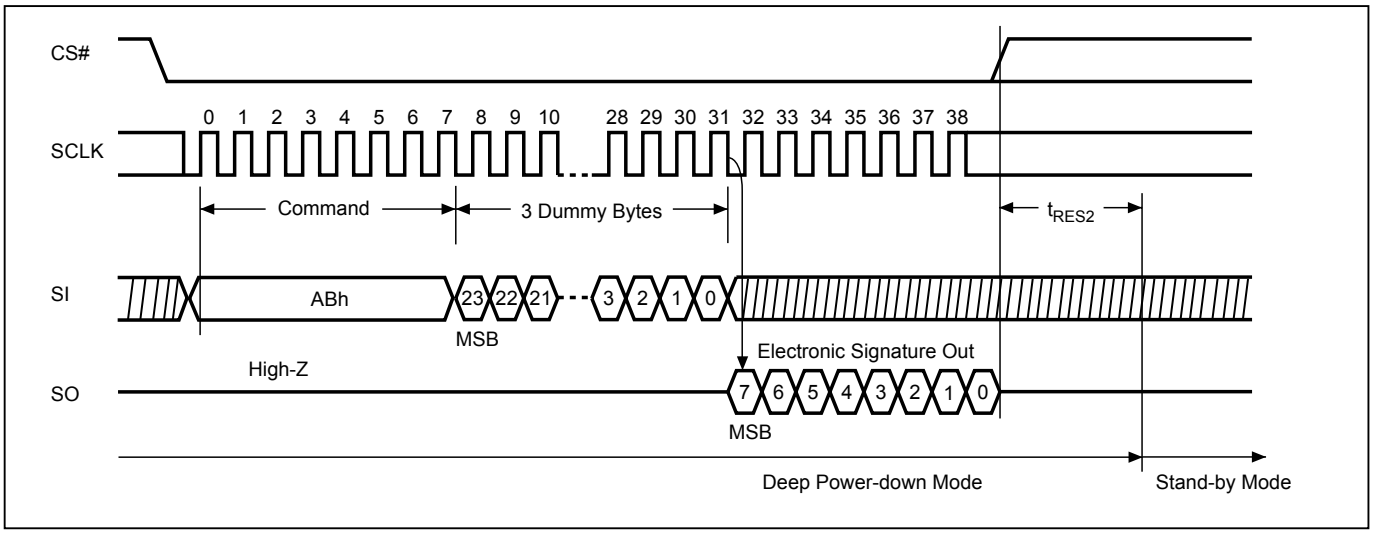


**Figure 39. Release from Deep Power-down (RDP) Sequence (Command AB)**

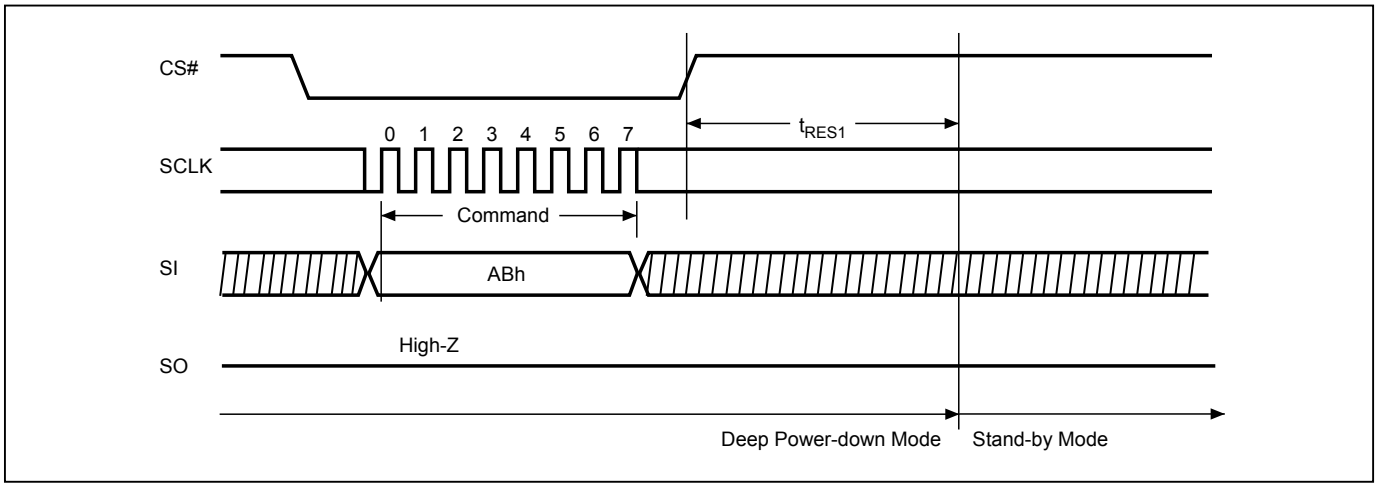
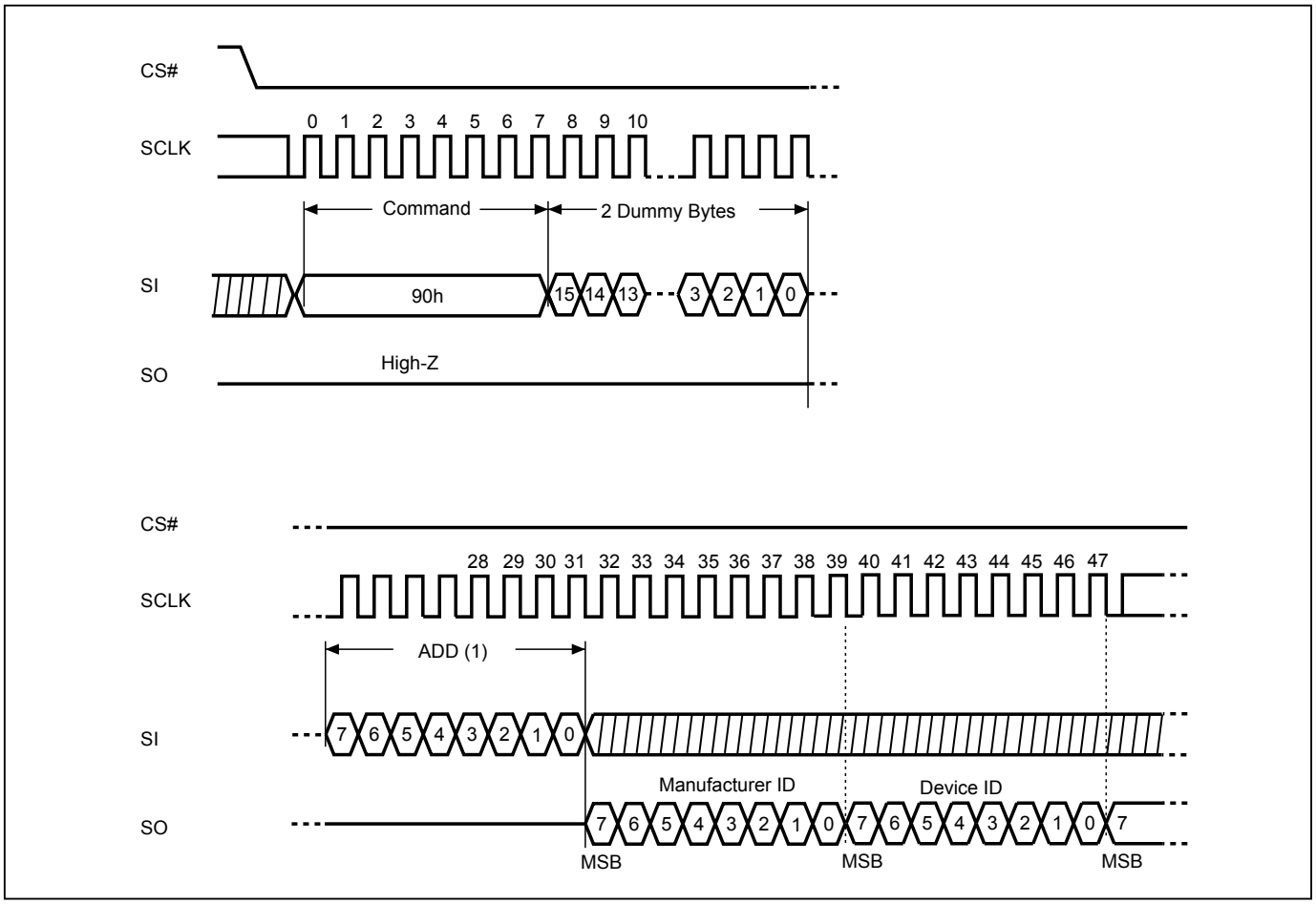



**Figure 40. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90/EF/DF)**




Note: ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.


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**Figure 41. Read Security Register (RDSCUR) Sequence (Command 2B)**

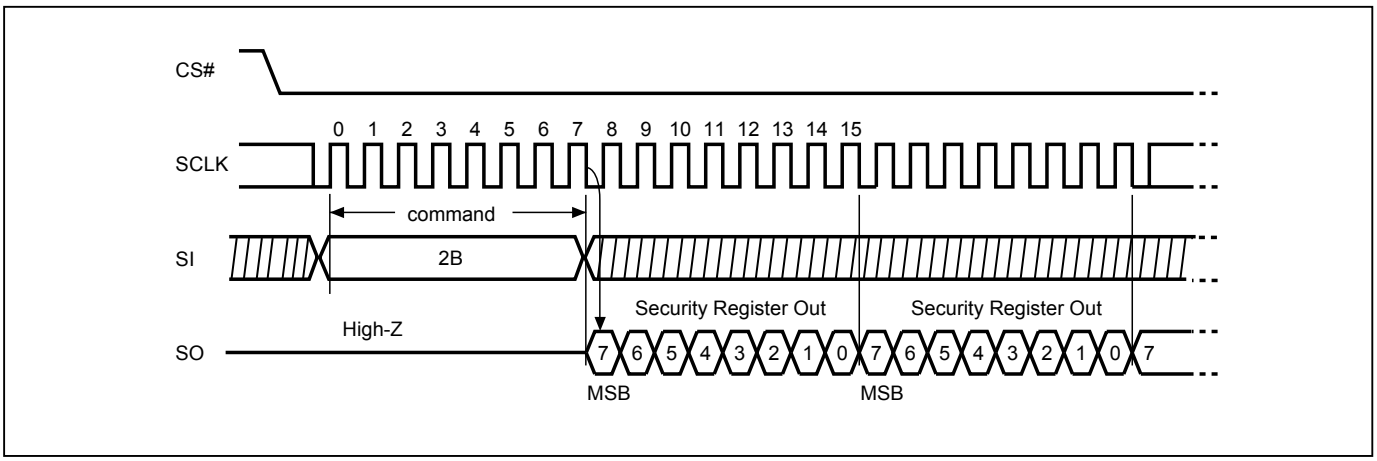
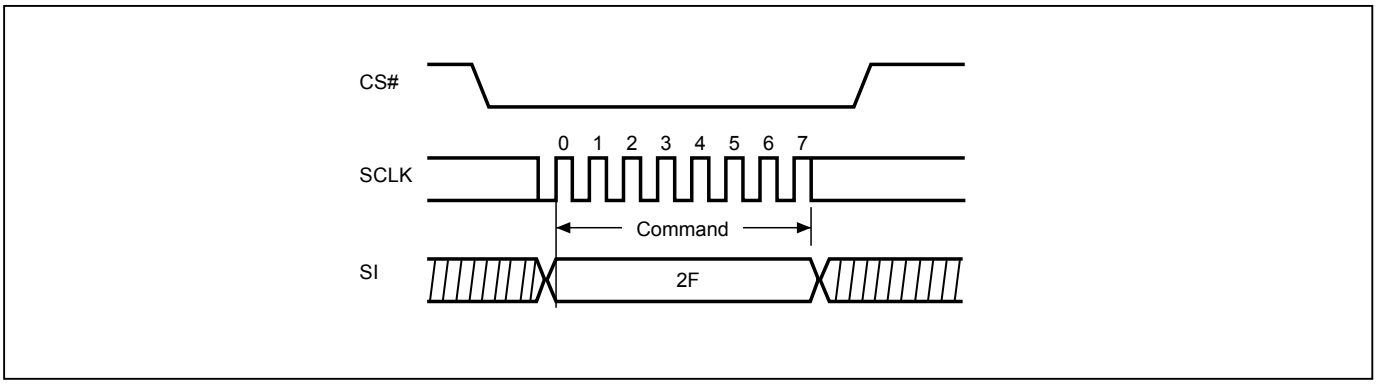


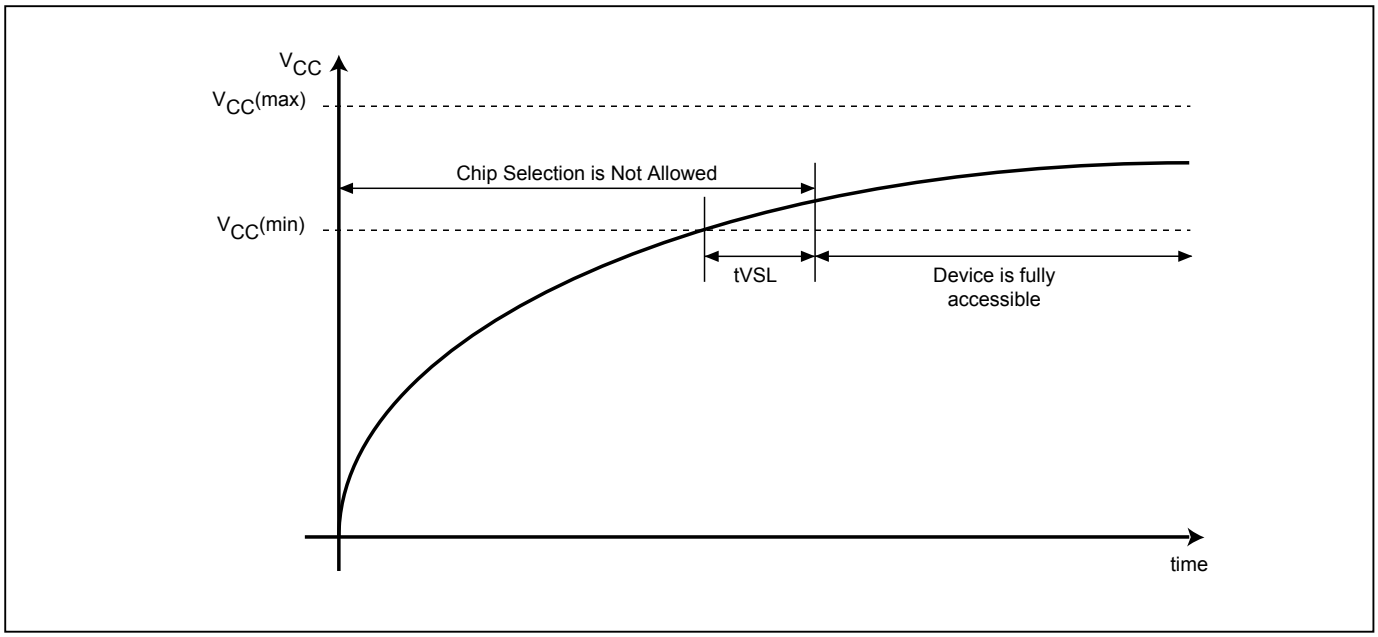

**Figure 42. Write Security Register (WRSCUR) Sequence (Command 2F)**





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**Figure 43. Power-up Timing**




Note: VCC (max.) is 2.0V and VCC (min.) is 1.65V.

**Table 15. Power-Up Timing**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| tVSL(1) | VCC(min) to CS# low (VCC Rise Time) | 300 | | us |

Note: 1. The parameters is characterized only.

### 13-1. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).


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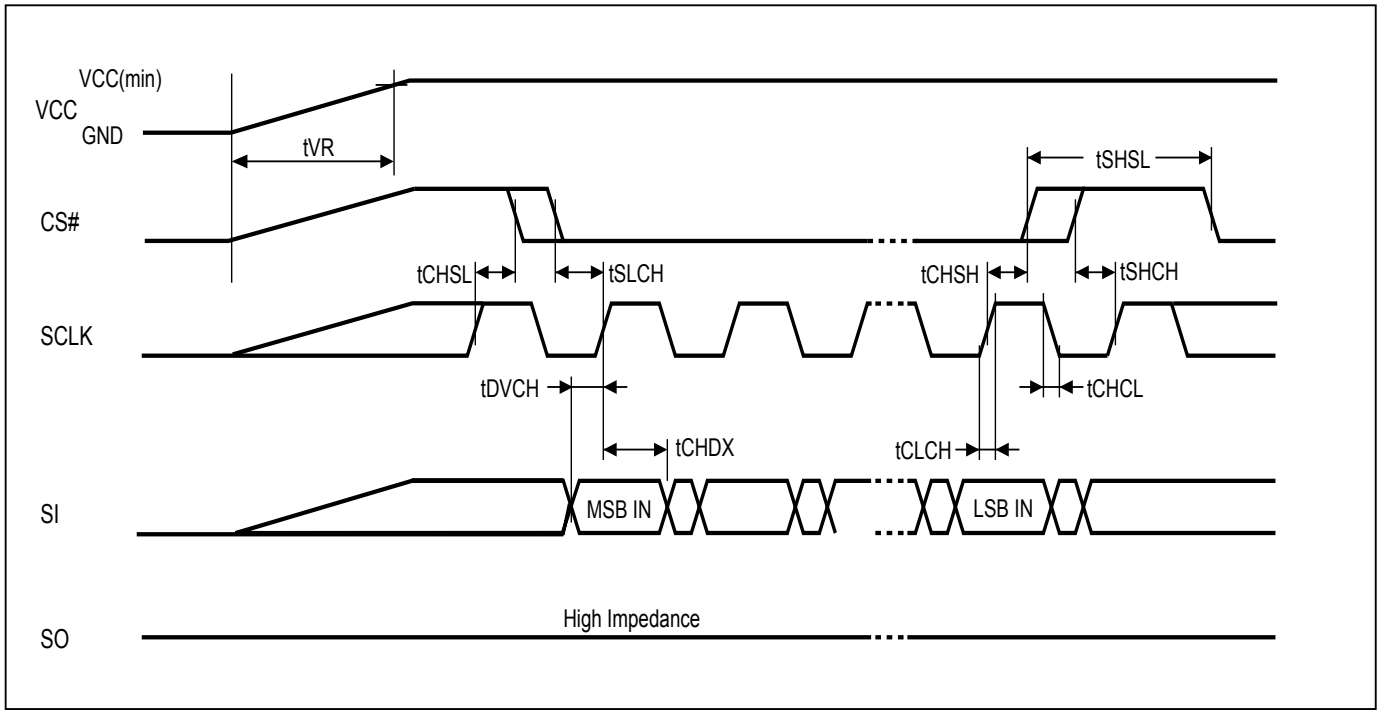
## 14. OPERATING CONDITIONS

### At Device Power-Up and Power-Down

AC timing illustrated in *"Figure 44. AC Timing at Device Power-Up"* and *"Figure 45. Power-Down Sequence"* are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

**Figure 44. AC Timing at Device Power-Up**



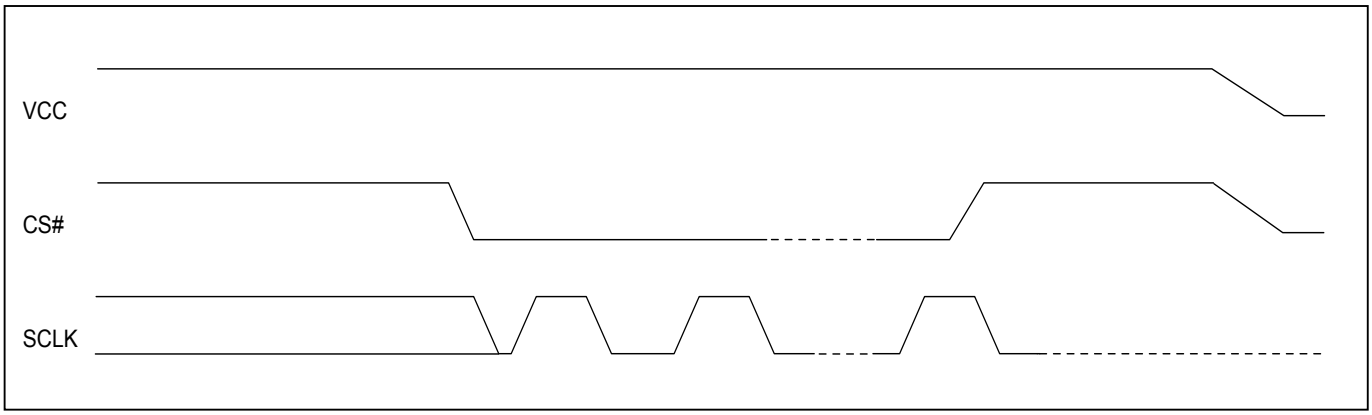

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| tVR | VCC Rise Time | 1 | | 500000 | us/V |

Notes :
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to *"Table 14. AC Characteristics"* table.


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**Figure 45. Power-Down Sequence**

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.



## 15. ERASE AND PROGRAMMING PERFORMANCE

| Parameter | Min. | Typ. (1) | Max. (2) | Unit |
|---|---|---|---|---|
| Write Status Register Cycle Time | | | 40 | ms |
| Sector Erase Cycle Time (4KB) | | 30 | 200 | ms |
| Block Erase Cycle Time (32KB) | | 200 | 1000 | ms |
| Block Erase Cycle Time (64KB) | | 500 | 2000 | ms |
| Chip Erase Cycle Time | | 5 | 10 | s |
| Byte Program Time (via page program command) | | 10 | 30 | us |
| Page Program Time | | 1.2 | 3 | ms |
| Erase/Program Cycle | | 100,000 | | cycles |

Note:
1. Typical program and erase time assumes the following conditions: 25°C, 1.8V, and checkerboard pattern.
2. Under worst conditions of 85°C and 1.65V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.

## DATA RETENTION

| Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|
| Data retention | 55˚C | 20 | | years |

## 16. LATCH-UP CHARACTERISTICS

| | MIN. | MAX. |
|---|---|---|
| Input Voltage with respect to GND on all power pins, SI, CS# | -1.0V | 2 VCCmax |
| Input Voltage with respect to GND on SO | -1.0V | VCC + 1.0V |
| Current | -100mA | +100mA |
| Includes all pins except VCC. Test conditions: VCC = 1.8V, one pin at a time. | | |


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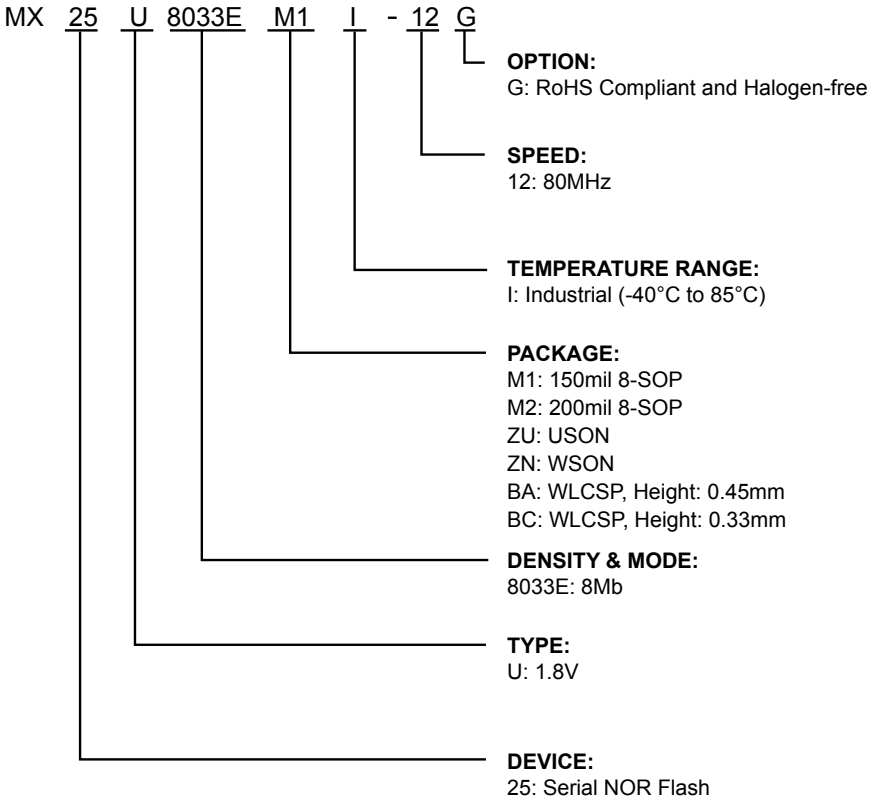
## 17. ORDERING INFORMATION

Please contact Macronix regional sales for the latest product selection and available form factors.

| PART NO. | CLOCK (MHz) | TEMPERATURE | PACKAGE | Remark |
|---|---|---|---|---|
| MX25U8033EM1I-12G | 80 | -40°C~85°C | 8-SOP (150mil) | |
| MX25U8033EZUI-12G | 80 | -40°C~85°C | 8-USON (4x4mm) | |
| MX25U8033EZNI-12G | 80 | -40°C~85°C | 8-WSON (6x5mm) | |
| MX25U8033EM2I-12G | 80 | -40°C~85°C | 8-SOP (200mil) | |
| MX25U8033EBAI-12G | 80 | -40°C ~ 85°C | 8-WLCSP (Height: 0.45mm, Max.) | |
| MX25U8033EBCI-12G | 80 | -40°C ~ 85°C | 8-WLCSP (Height: 0.33mm, Max.) | |


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## 18. PART NAME DESCRIPTION



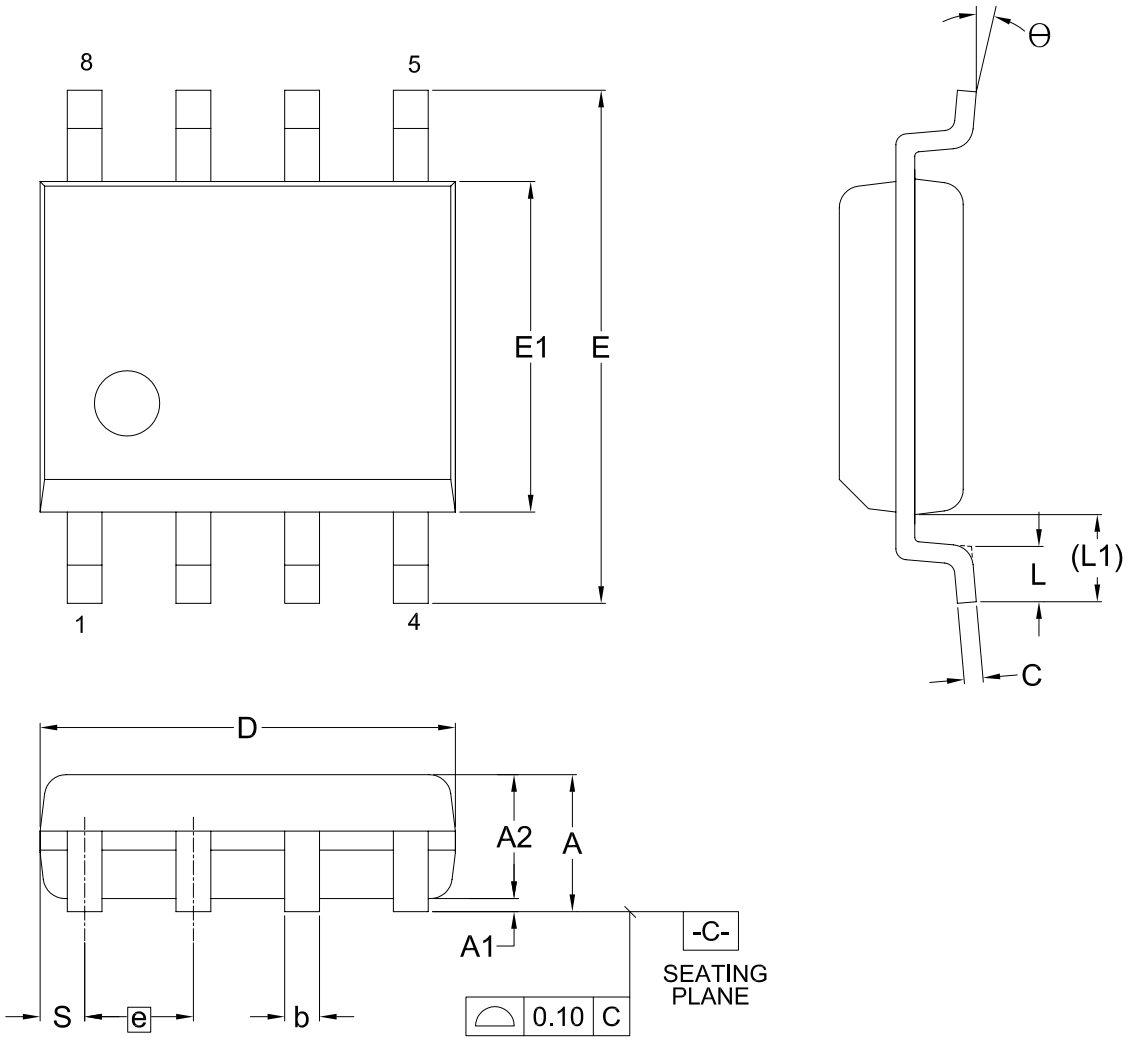


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## 19. PACKAGE INFORMATION

### 19-1. 8-pin SOP (150mil)

Doe. Title: Package Outline for SOP 8L (150MIL)

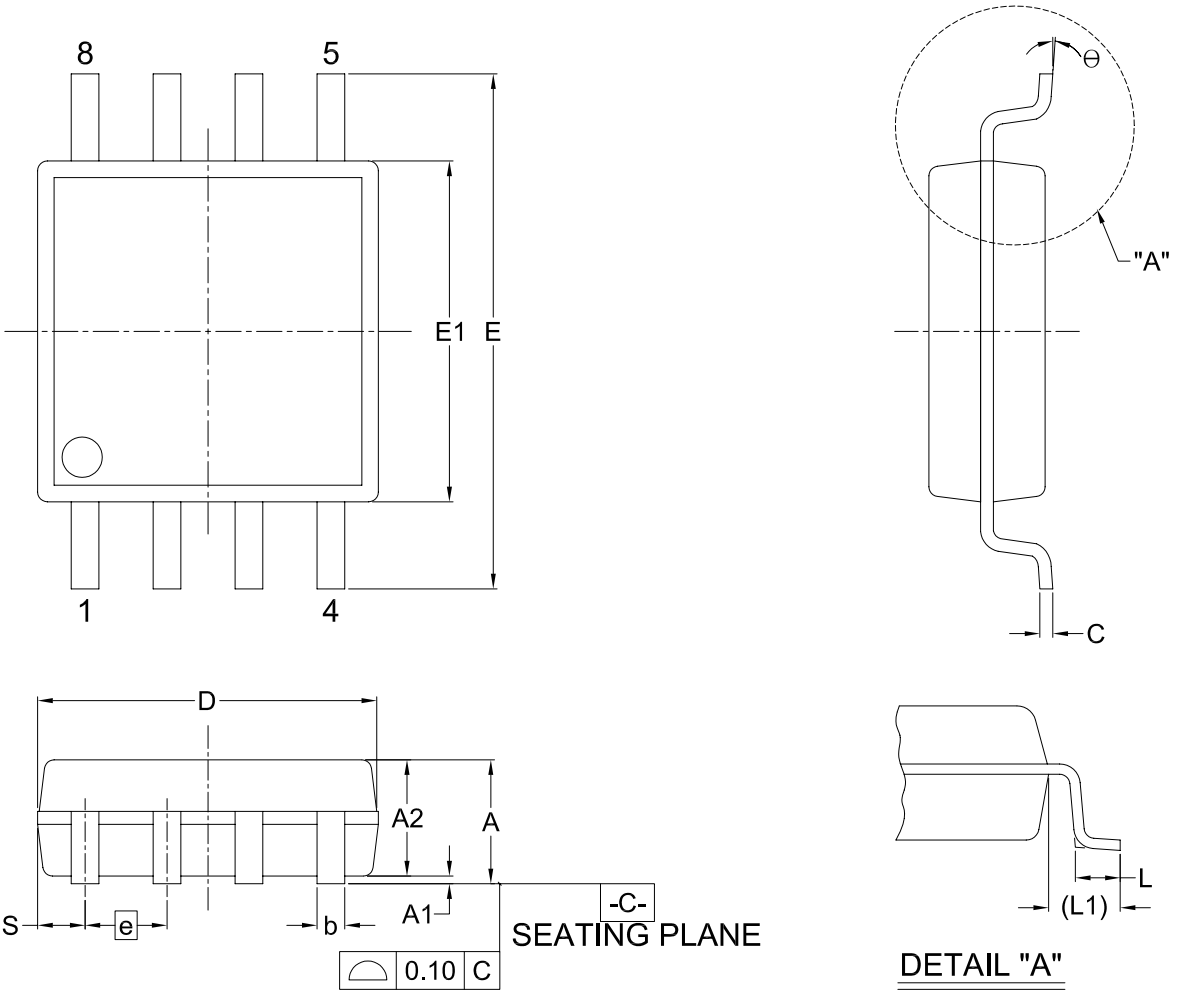



Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | C | D | E | E1 | e | L | L1 | S | Θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | --- | 0.10 | 1.35 | 0.36 | 0.15 | 4.77 | 5.80 | 3.80 | --- | 0.46 | 0.85 | 0.41 | 0° |
| | Nom. | --- | 0.15 | 1.45 | 0.41 | 0.20 | 4.90 | 5.99 | 3.90 | 1.27 | 0.66 | 1.05 | 0.54 | 5° |
| | Max. | 1.75 | 0.20 | 1.55 | 0.51 | 0.25 | 5.03 | 6.20 | 4.00 | --- | 0.86 | 1.25 | 0.67 | 8° |
| Inch | Min. | --- | 0.004 | 0.053 | 0.014 | 0.006 | 0.188 | 0.228 | 0.150 | --- | 0.018 | 0.033 | 0.016 | 0° |
| | Nom. | --- | 0.006 | 0.057 | 0.016 | 0.008 | 0.193 | 0.236 | 0.154 | 0.050 | 0.026 | 0.041 | 0.021 | 5° |
| | Max. | 0.069 | 0.008 | 0.061 | 0.020 | 0.010 | 0.198 | 0.244 | 0.158 | --- | 0.034 | 0.049 | 0.026 | 8° |

**19-2. 8-pin SOP (200mil)**

Doc. Title: Package Outline for SOP 8L 200MIL (official name - 209MIL)

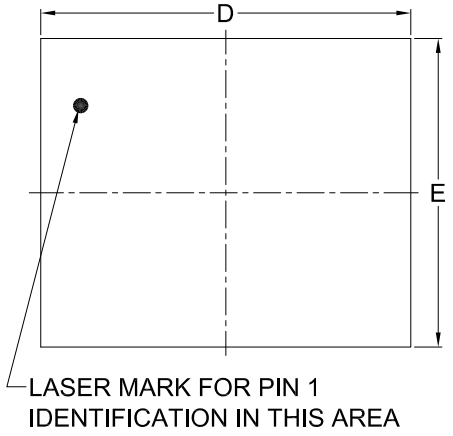



Dimensions (inch dimensions are derived from the original mm dimensions)

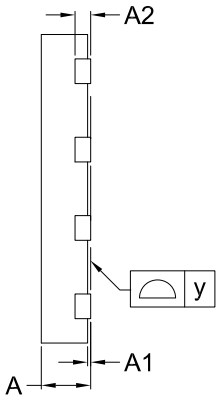
| SYMBOL / UNIT | | A | A1 | A2 | b | C | D | E | E1 | e | L | L1 | S | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | 1.75 | 0.05 | 1.70 | 0.36 | 0.19 | 5.13 | 7.70 | 5.18 | --- | 0.50 | 1.21 | 0.62 | 0° |
| | Nom. | 1.95 | 0.15 | 1.80 | 0.41 | 0.20 | 5.23 | 7.90 | 5.28 | 1.27 | 0.65 | 1.31 | 0.74 | 5° |
| | Max. | 2.16 | 0.20 | 1.91 | 0.51 | 0.25 | 5.33 | 8.10 | 5.38 | --- | 0.80 | 1.41 | 0.88 | 8° |
| Inch | Min. | 0.069 | 0.002 | 0.067 | 0.014 | 0.007 | 0.202 | 0.303 | 0.204 | --- | 0.020 | 0.048 | 0.024 | 0° |
| | Nom. | 0.077 | 0.006 | 0.071 | 0.016 | 0.008 | 0.206 | 0.311 | 0.208 | 0.050 | 0.026 | 0.052 | 0.029 | 5° |
| | Max. | 0.085 | 0.008 | 0.075 | 0.020 | 0.010 | 0.210 | 0.319 | 0.212 | --- | 0.031 | 0.056 | 0.035 | 8° |

### 19-3. 8-land WSON (6x5mm)

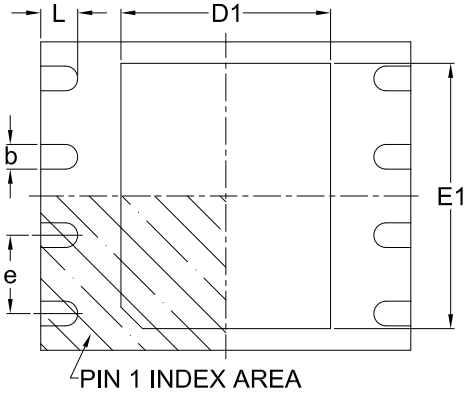
**Doc. Title: Package Outline for WSON 8L (6x5x0.8MM, LEAD PITCH 1.27MM)**




TOP VIEW




SIDE VIEW




BOTTOM VIEW

Note:

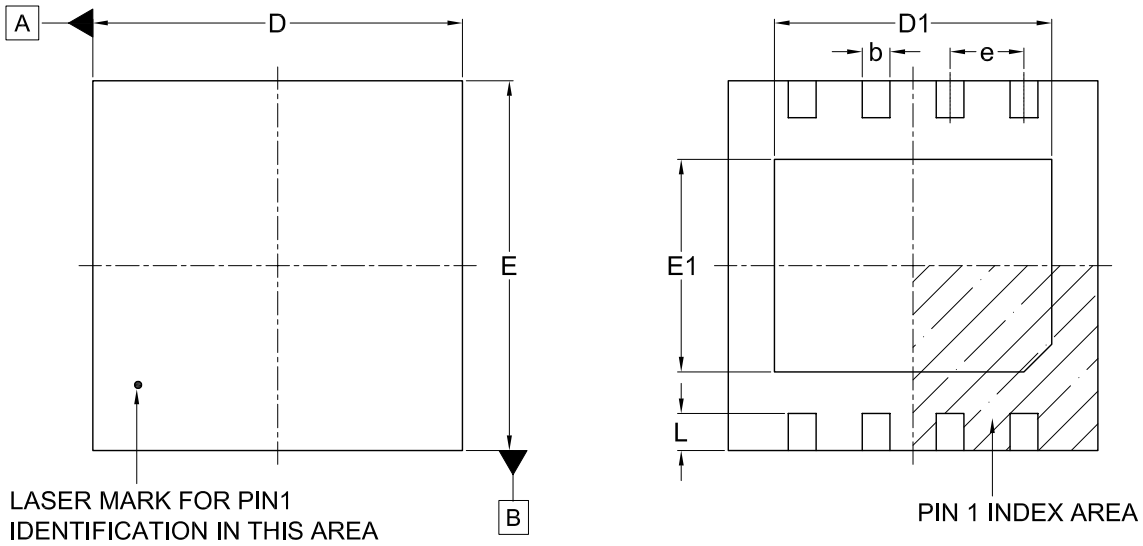
This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

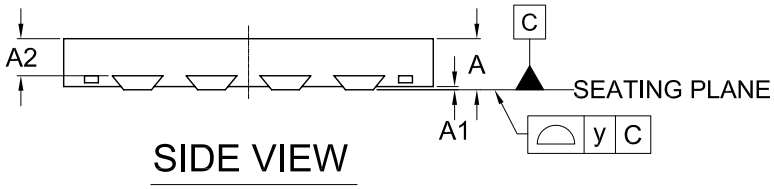
Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | D | D1 | E | E1 | L | e | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | 0.70 | --- | --- | 0.35 | 5.90 | 3.35 | 4.90 | 3.95 | 0.55 | --- | 0.00 |
| | Nom. | --- | --- | 0.20 | 0.40 | 6.00 | 3.40 | 5.00 | 4.00 | 0.60 | 1.27 | --- |
| | Max. | 0.80 | 0.05 | --- | 0.48 | 6.10 | 3.45 | 5.10 | 4.05 | 0.65 | --- | 0.05 |
| Inch | Min. | 0.028 | --- | --- | 0.014 | 0.232 | 0.132 | 0.193 | 0.156 | 0.022 | --- | 0.00 |
| | Nom. | --- | --- | 0.008 | 0.016 | 0.236 | 0.134 | 0.197 | 0.157 | 0.024 | 0.05 | --- |
| | Max. | 0.032 | 0.002 | --- | 0.019 | 0.240 | 0.136 | 0.201 | 0.159 | 0.026 | --- | 0.002 |

### 19-4. 8-land USON (4x4mm)

**Doc. Title: Package Outline for USON 8L (4x4x0.6MM, LEAD PITCH 0.8MM)**




Note:

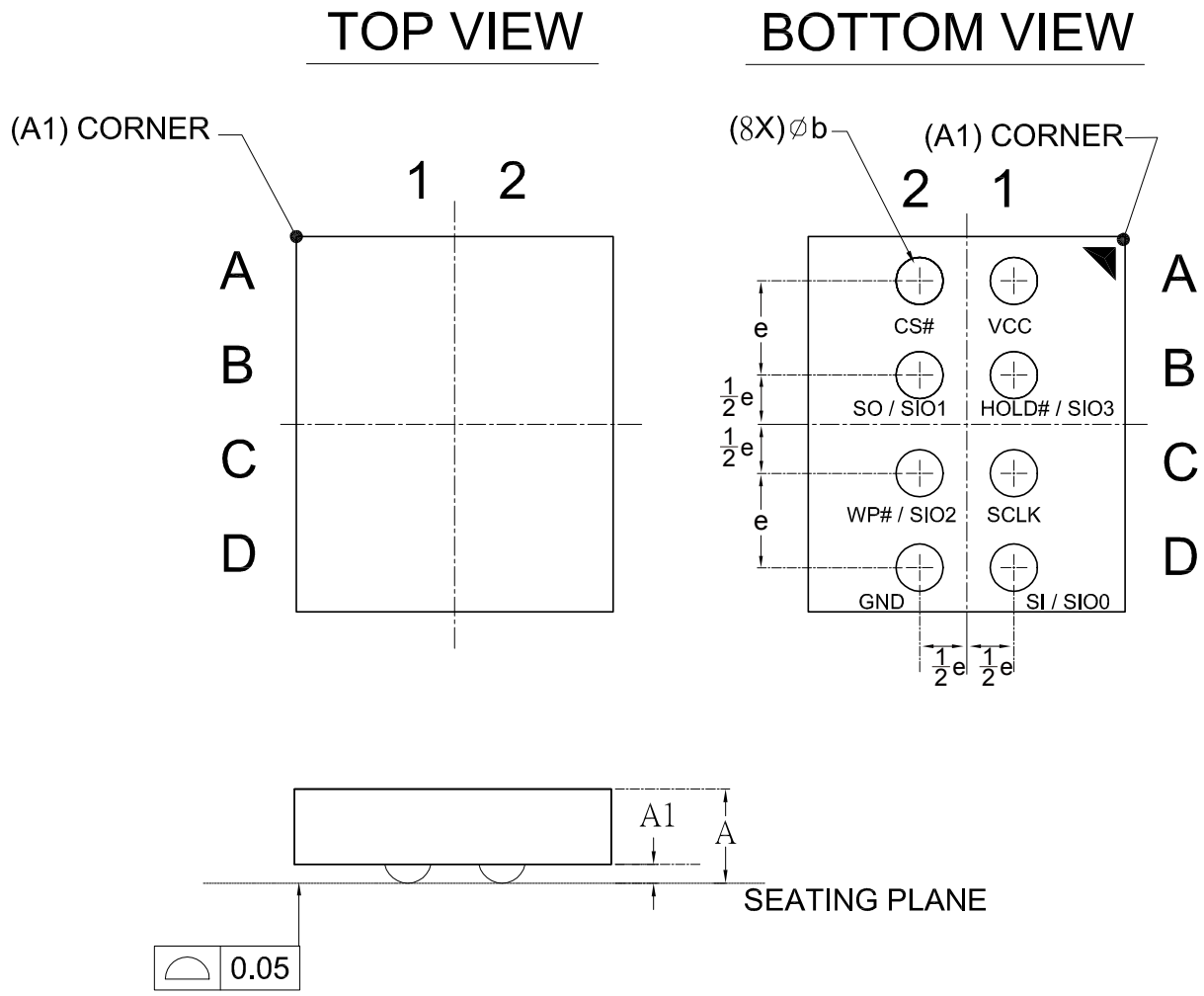
This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | A2 | b | D | D1 | E | E1 | L | e | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min. | 0.50 | --- | --- | 0.25 | 3.90 | 2.90 | 3.90 | 2.20 | 0.35 | --- | 0.00 |
| | Nom. | 0.55 | 0.04 | 0.40 | 0.30 | 4.00 | 3.00 | 4.00 | 2.30 | 0.40 | 0.80 | --- |
| | Max. | 0.60 | 0.05 | 0.43 | 0.35 | 4.10 | 3.10 | 4.10 | 2.40 | 0.45 | --- | 0.08 |
| Inch | Min. | 0.020 | --- | --- | 0.010 | 0.154 | 0.114 | 0.154 | 0.087 | 0.014 | --- | 0.00 |
| | Nom. | 0.022 | 0.002 | 0.016 | 0.011 | 0.157 | 0.118 | 0.157 | 0.091 | 0.016 | 0.031 | --- |
| | Max. | 0.024 | 0.002 | 0.017 | 0.014 | 0.161 | 0.122 | 0.161 | 0.094 | 0.018 | --- | 0.003 |

**19-5. 8-WLCSP (Height: 0.45mm)**

**Title: Package Outline for 8BALL WLCSP, BALL PITCH 0.5mm, BALL DIAMETER 0.25MM**



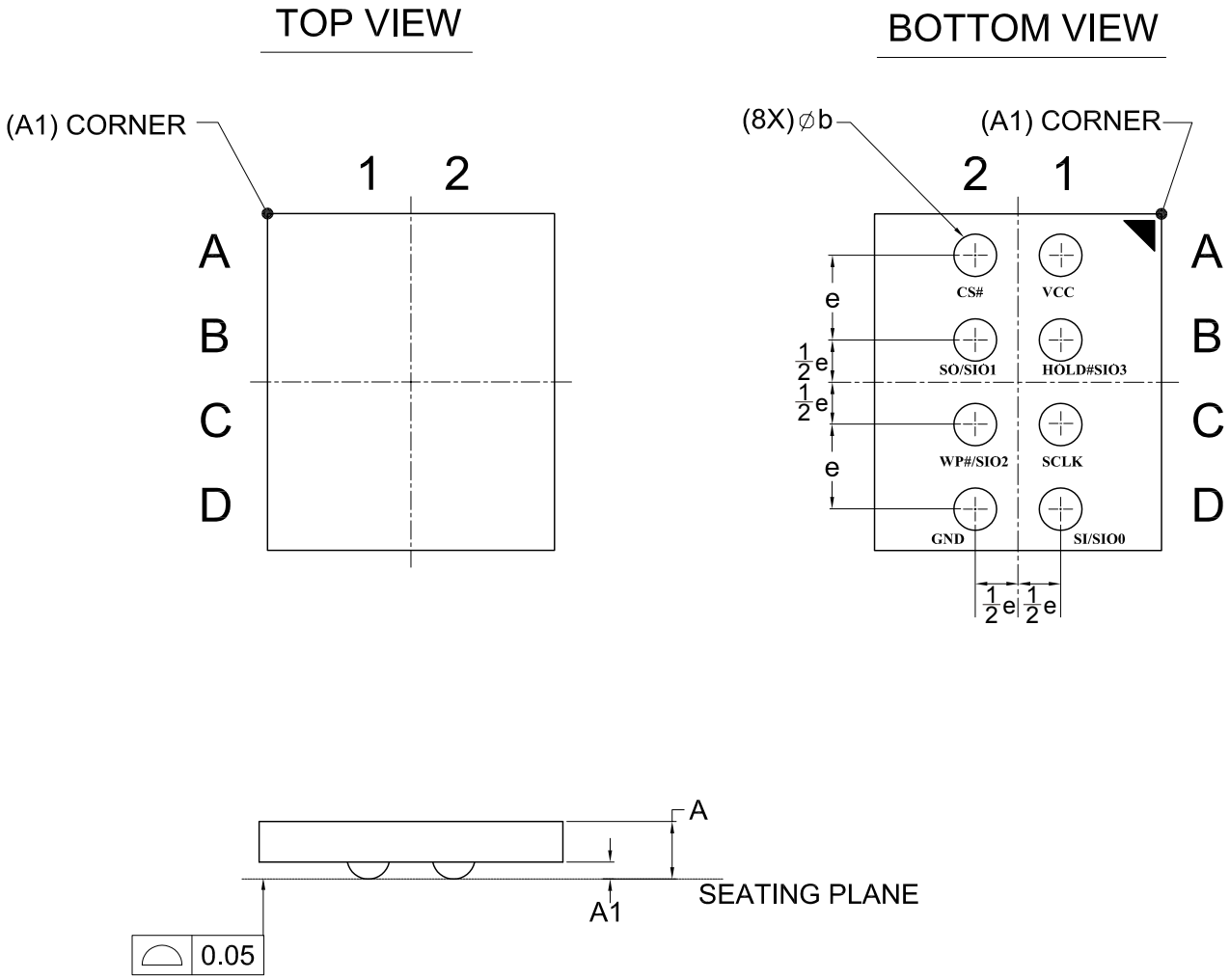

Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | b | e |
|---|---|---|---|---|---|
| mm | Min. | 0.35 | 0.105 | 0.22 | --- |
| | Nom. | 0.40 | 0.135 | 0.25 | 0.50 BSC |
| | Max. | 0.45 | 0.165 | 0.28 | --- |
| Inch | Min. | 0.014 | 0.0041 | 0.009 | --- |
| | Nom. | 0.016 | 0.0053 | 0.010 | 0.020 BSC |
| | Max. | 0.018 | 0.0065 | 0.011 | --- |

**Please contact local Macronix sales channel for complete package dimensions.**

**19-6. 8-WLCSP (Height: 0.33mm)**

**Title: Package Outline for 8BALL WLCSP, BALL PITCH 0.5mm, BALL DIAMETER 0.22MM**




Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL / UNIT | | A | A1 | b | e |
|---|---|---|---|---|---|
| mm | Min. | 0.27 | 0.048 | 0.19 | --- |
| | Nom. | 0.30 | 0.068 | 0.22 | 0.50 BSC |
| | Max. | 0.33 | 0.088 | 0.25 | --- |
| Inch | Min. | 0.011 | 0.0019 | 0.007 | --- |
| | Nom. | 0.012 | 0.0027 | 0.009 | 0.020 BSC |
| | Max. | 0.013 | 0.0035 | 0.010 | --- |

**Please contact local Macronix sales channel for complete package dimensions.**

## 20. REVISION HISTORY

| Rev. No. | Descriptions | Page | Date |
|---|---|---|---|
| 1.0 | 1. Added 200mil 8SOP Package solution<br>2. Modified Order Information format | P3,5,54,55,57<br>P54 | NOV/09/2011 |
| 1.1 | 1. Removed Advanced Information from Ordering Information | P54 | DEC/27/2011 |
| 1.2 | 1. Added SFDP content | P12,32~37,42 | MAR/20/2012 |
| 1.3 | 1. Added DREAD function<br>2. Modified SFDP wording | P13,15,23,37,38,50<br>P35~40 | APR/15/2013 |
| 1.4 | 1. Modified ABSOLUTE MAXIMUM RATINGS Table<br>2. Updated parameters for DC Characteristics.<br>3. Updated Erase and Programming Performance. | P42<br>P5, 44<br>P5, 45, 62 | NOV/15/2013 |
| 1.5 | 1. Added WLCSP package and Part No.<br>2. Added SFDP Table for WLCSP package | P6,8,63,64,69,70<br>P40~43 | APR/15/2014 |
| 1.6 | 1. Modified toggling description of DREAD function<br>2. WLCSP supported DREAD (including SFDP) to align with other packages | P25,52<br>P23,37,38,63 | APR/24/2014 |
| 1.7 | 1. Modified Power-up Timing figure and parameter | P41,59 | JUL/01/2014 |
| 1.8 | 1. Updated *"19-1. 8-pin SOP (150mil)"*: added the unit of "Θ" values.<br>2. Updated *"19-2. 8-pin SOP (200mil)"*: added the unit of "Θ" values.<br>3. Updated *"19-3. 8-land WSON (6x5mm)"*: revised "y" values and the exposed metal pad drawing; revised in Min./Max. D1, E1 and L values.<br>4. Updated *"19-6. 8-WLCSP (Height: 0.33mm)"*: revised ball diameter and "b" values.<br>5. Updated *"5. BLOCK DIAGRAM"*.<br>6. Updated *"9. HOLD FEATURE"*.<br>7. Added Key Features on the cover page<br>8. Revised Note 6 of the SFDP Tables<br>9. Added *"Figure 14. SCLK TIMING DEFINITION"*.<br>10. Updated tVR values.<br>11. Added a statement for product ordering information.<br>12. Content modification.<br>13. Format modification. | P65<br>P66<br>P67<br><br><br>P70<br><br>P9<br>P14<br>P1<br>P40<br>P43<br>P60<br>P63<br>P21,28,30,45<br>P65-68 | OCT/24/2017 |


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