MX25LW51245G

3V 512M-BIT [x 1/x 8]
Read-While-Write octaflash Memory

Key Features

- *Support octaflash Interface with Simultaneous Read while Write operations*
- *Support DTR (Double Transfer Rate) Mode*
- *Support clock frequency up to 133MHz*

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3V 512M-BIT [x 1/x 8] Read-While-Write octaflash Memory

1. FEATURES

GENERAL

- Supports Serial Peripheral Interface -- Mode 0
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- 512Mb: 536,870,912 x 1 bit structure or 67,108,864 x 8 bits (Octa I/O mode) structure
- Protocol Support
  - Single I/O and Octa I/O
  - Support DTR (Double Transfer Rate) Mode
- Support Simultaneous Read while Write operations
  - The read operation can be executing from one bank while Program/ or erase is processing in another bank
- Multiple bank architecture
  - Four uniform banks are provided
  - Read operation can be occur in any of the three banks which is not doing programmed or erased operation
- Fast frequency support
  - Support clock frequency up to
    - Single I/O mode: 133MHz
    - Octa I/O mode: 133MHz
  - Configurable dummy cycle number for OPI read operation
- Equal Sectors with 4K byte each, or Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Write Buffer:
  - 256byte page buffer
  - Support interruptible write
  - Support write buffer read
- Data Integrity Check function :
  - ECC (Error Checking and Correcting): to prevent the data storage errors
  - CRC1 : to prevent the data transmission errors
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - SPI: 1-byte command code
  - OPI: 2-byte command code
- Advanced Security Features
  - Block lock protection

    The BP0-BP3 and T/B status bits define the size of the area to be protected against program and erase instructions
  - Individual Sector Protection (Solid Protect)
- Additional 8K bit security OTP
  - Features unique identifier
  - Factory locked identifiable, and customer lockable
- Command Reset
- Program/Erase Suspend and Resume operation
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SIO0 - SIO7
  - Serial Data Input or Serial Data Output
- DQS
  - Data strobe signal
- ECS#
  - ECC Correction Signal
- RESET#
  - Hardware Reset pin
- PACKAGE
  - 24-Ball BGA (5x5 ball array)
  - **All devices are RoHS Compliant and Halogen Free.**

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2. GENERAL DESCRIPTION

MX25LW51245G is 512Mb bits Octal interface Serial NOR Flash memory, which is configured as 67,108,864 x 8 internally. MX25LW51245G feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

The MX25LW51245G octaflash provides multiple bank architecture with Simultaneous Read while Write operations.

The sequential read operation can be occur in any of the three banks which is not been programmed or erased.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Meanwhile, the read operation can be executing in another bank .

Program command is executed on byte, word or page (256 bytes) basis. Erase command is executed on sector (4K-byte), or block (64K-byte), or whole chip basis.

To provide user with ease of interface, a status register and RWW status register are included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

When the device is not in operation and CS# is high, it is put in standby mode.

The MX25LW51245G utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

Table 1. Operating Frequency Comparison

	Numbers of Dummy Cycle							
	6	8	10	12	14	16	18	20
Octa I/O STR (MHz)	66	84	104	104	133	133	133	133*
Octa I/O DTR (MHz)	66	84	104	104	133	133	133	133*

Notes: * means default status

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3. PIN CONFIGURATIONS

24-BALL BGA (5x5 ball array)

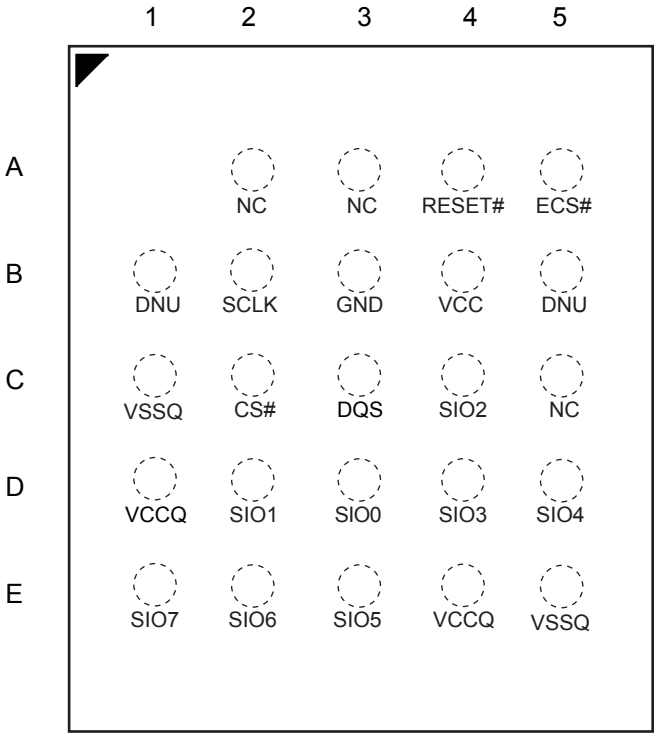


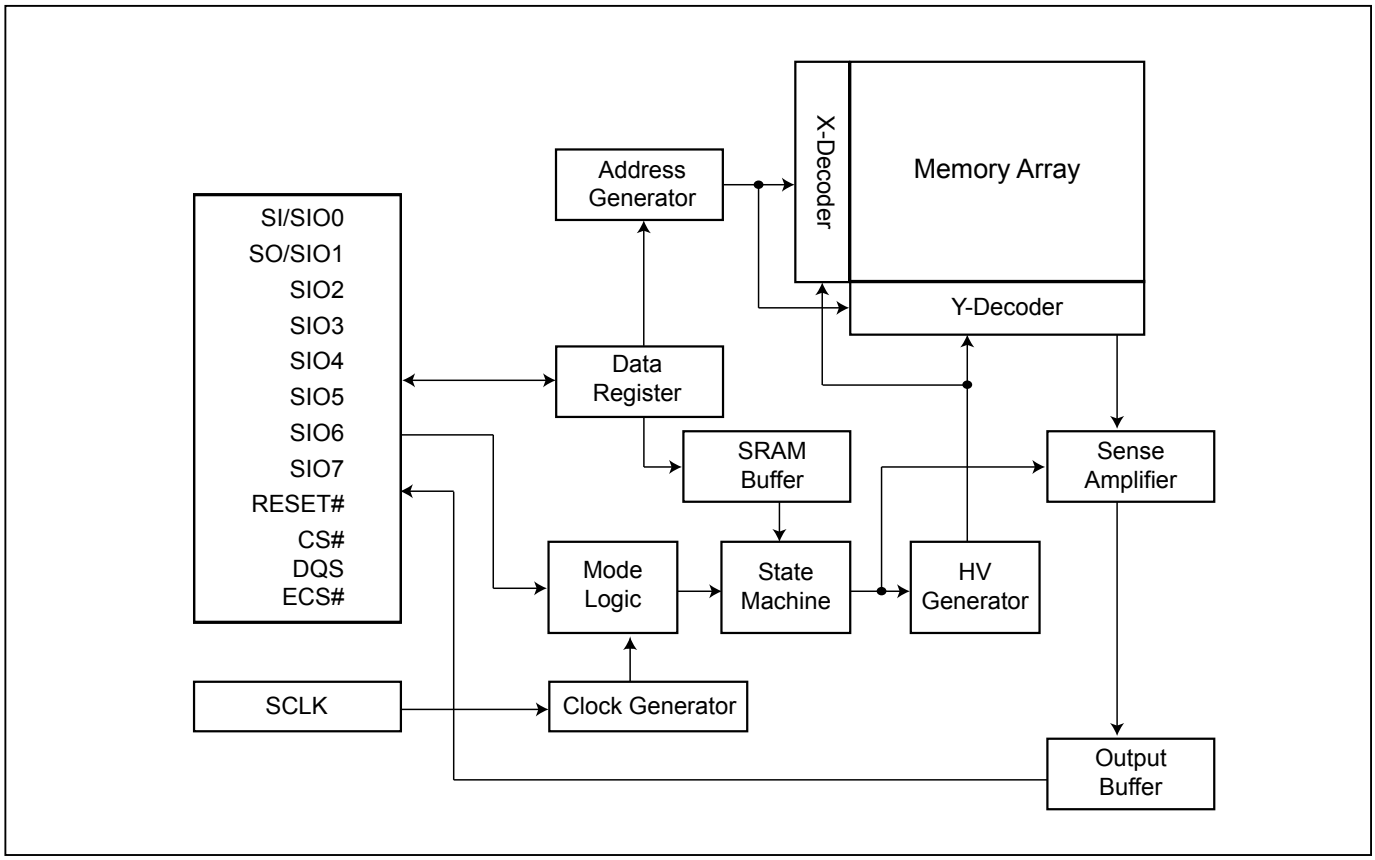
Table 2. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SCLK	Clock Input
RESET#	Hardware Reset Pin Active low[Note 1]
ECS#	ECC Correction Signal (open drain)
DQS	Data Strobe Signal
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 8 x I/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 8 x I/O read mode)
SIO2-SIO7	Serial Data Input & Output (for 8 x I/O read mode)
VCC	3V Power Supply
VCCQ	3V Buffer Power Supply
GND	Ground
VSSQ	IO Ground Supply
NC	No Connection
DNU	Do Not Use

Notes:
1. The pin of RESET# will remain internal pull up function while this pin is not physically connected in system configuration.
   However, the internal pull up function will be disabled if the system has physical connection to RESET# pin.

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4. BLOCK DIAGRAM



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5. MEMORY ORGANIZATION

The Flash memory array is divided into banks. The multi bank structure enables read-while-write (RWW) feature, which means read data one bank while another bank is programing or erasing. The details of the address ranges and the corresponding sector and block addresses are shown in *"Table 3. MEMORY ORGANIZATION"*.

The device can be operated in following three modes:
• Normal Read Mode
• Program/erase Mode (PE Mode)
• Write Register Mode

Normal Read Mode: The device will be in Normal Read Mode after following status: Hardware Reset, Power on, command reset, Exit from PE mode or Write Register Mode.

PE Mode: The Program & Erase operation can be conducted in one bank, however, in the same bank, no read is allowed. Other PE banks are available for read operation at the same time. This is the “Read-While-Write” operation. In PE mode, RDSR, RDCR, RDSCUR, part of RDCR2, part of WRCR2, WRDI, RSTEN, RST commands are allowed, others are not allowed. At any time, only one bank is available to use PE mode.

Write Register Mode: The device will be in Write Register Mode after accepting register write command (WREN, WRDI, WRSR, WRCR2, WRFBR, WRSCUR, WRLR, WRSPB, WRDPB, WPSEL, GBLK, GBULK,WRPASS, PASSULK) or Programming Secured OTP. In this mode, RDSR, RDCR, RDSCUR, part of RDCR2, part of WRCR2, WRDI, RSTEN, RST commands are valid, others are invalid.

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Table 3. MEMORY ORGANIZATION

Bank (16MB)	Block (64KB)	Sector (4KB)	Address Range	
0	0	0	0000000h	0000FFFh
		⋮	⋮	⋮
		7	0007000h	0007FFFh
		8	0008000h	0008FFFh
		⋮	⋮	⋮
		15	000F000h	000FFFFh
	1	16	0010000h	0010FFFh
		⋮	⋮	⋮
		23	0017000h	0017FFFh
		24	0018000h	0018FFFh
		⋮	⋮	⋮
		31	001F000h	001FFFFh
	≀	≀	≀	≀
	255	4080	0FF0000h	0FF0FFFh
		⋮	⋮	⋮
		4087	0FF7000h	0FF7FFFh
		4088	0FF8000h	0FF8FFFh
		⋮	⋮	⋮
		4095	0FFF000h	0FFFFFFh

Bank (16MB)	Block (64KB)	Sector (4KB)	Address Range	
1	256	4096	1000000h	1000FFFh
		⋮	⋮	⋮
		4103	1007000h	1007FFFh
		4104	1008000h	1008FFFh
		⋮	⋮	⋮
		4111	100F000h	100FFFFh
	257	4112	1010000h	1010FFFh
		⋮	⋮	⋮
		4119	1017000h	1017FFFh
		4120	1018000h	1018FFFh
		⋮	⋮	⋮
		4127	101F000h	101FFFFh
	≀	≀	≀	≀
	511	8176	1FF0000h	1FF0FFFh
		⋮	⋮	⋮
		8183	1FF7000h	1FF7FFFh
		8184	1FF8000h	1FF8FFFh
		⋮	⋮	⋮
		8191	1FFF000h	1FFFFFFh

Bank (16MB)	Block (64KB)	Sector (4KB)	Address Range	
2	512	8192	2000000h	2000FFFh
		⋮	⋮	⋮
		8199	2007000h	2007FFFh
		8200	2008000h	2008FFFh
		⋮	⋮	⋮
		8207	200F000h	200FFFFh
	513	8208	2010000h	2010FFFh
		⋮	⋮	⋮
		8215	2017000h	2017FFFh
		8216	2018000h	2018FFFh
		⋮	⋮	⋮
		8223	201F000h	201FFFFh
	≀	≀	≀	≀
	767	12272	2FF0000h	2FF0FFFh
		⋮	⋮	⋮
		12279	2FF7000h	2FF7FFFh
		12280	2FF8000h	2FF8FFFh
		⋮	⋮	⋮
		12287	2FFF000h	2FFFFFFh

Bank (16MB)	Block (64KB)	Sector (4KB)	Address Range	
3	768	12288	3000000h	3000FFFh
		⋮	⋮	⋮
		12295	3007000h	3007FFFh
		12296	3008000h	3008FFFh
		⋮	⋮	⋮
		12303	300F000h	300FFFFh
	769	12304	3010000h	3010FFFh
		⋮	⋮	⋮
		12311	3017000h	3017FFFh
		12312	3018000h	3018FFFh
		⋮	⋮	⋮
		12319	301F000h	301FFFFh
	≀	≀	≀	≀
	1023	16368	3FF0000h	3FF0FFFh
		⋮	⋮	⋮
		16375	3FF7000h	3FF7FFFh
		16376	3FF8000h	3FF8FFFh
		⋮	⋮	⋮
		16383	3FFF000h	3FFFFFFh

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6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length (SPI Mode) or command/command# combination (OPI Mode) will be checked.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data.
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write.

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6-1. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0 and T/B) bits to allow part of memory to be protected as read only. The protected area definition is shown as *Table 4* Protected Area Sizes, the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.

Table 4. Protected Area Sizes

Protected Area Sizes (T/B bit = 0)

Status bit				Protect Level
BP3	BP2	BP1	BP0	512Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 1023rd)
0	0	1	0	2 (2 blocks, protected block 1022nd~1023rd)
0	0	1	1	3 (4 blocks, protected block 1020th~1023rd)
0	1	0	0	4 (8 blocks, protected block 1016th~1023rd)
0	1	0	1	5 (16 blocks, protected block 1008th~1023rd)
0	1	1	0	6 (32 blocks, protected block 992nd~1023rd)
0	1	1	1	7 (64 blocks, protected block 960th~1023rd)
1	0	0	0	8 (128 blocks, protected block 896th~1023rd)
1	0	0	1	9 (256 blocks, protected block 768th~1023rd)
1	0	1	0	10 (512 blocks, protected block 512nd~1023rd)
1	0	1	1	11 (1024 blocks, protected all)
1	1	0	0	12 (1024 blocks, protected all)
1	1	0	1	13 (1024 blocks, protected all)
1	1	1	0	14 (1024 blocks, protected all)
1	1	1	1	15 (1024 blocks, protected all)

Protected Area Sizes (T/B bit = 1)

Status bit				Protect Level
BP3	BP2	BP1	BP0	512Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 0th)
0	0	1	0	2 (2 blocks, protected block 0th~1st)
0	0	1	1	3 (4 blocks, protected block 0th~3rd)
0	1	0	0	4 (8 blocks, protected block 0th~7th)
0	1	0	1	5 (16 blocks, protected block 0th~15th)
0	1	1	0	6 (32 blocks, protected block 0th~31st)
0	1	1	1	7 (64 blocks, protected block 0th~63rd)
1	0	0	0	8 (128 blocks, protected block 0th~127th)
1	0	0	1	9 (256 blocks, protected block 0th~255th)
1	0	1	0	10 (512 blocks, protected block 0th~511th)
1	0	1	1	11 (1024 blocks, protected all)
1	1	0	0	12 (1024 blocks, protected all)
1	1	0	1	13 (1024 blocks, protected all)
1	1	1	0	14 (1024 blocks, protected all)
1	1	1	1	15 (1024 blocks, protected all)

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6-2. Additional 8K-bit secured OTP

The secured OTP for unique identifier: to provide 8K-bit one-time program area for setting device unique serial number. Which may be set by factory or system customer.

- Security register bit 0 indicates whether the chip is locked by factory or not.

- To program the 8K-bit secured OTP by entering secured OTP mode (with Enter Security OTP command), and going through normal program procedure, and then exiting secured OTP mode by writing Exit Security OTP command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to *"Table 9. Security Register Definition"* for security register bit definition and *"Table 5. Secured OTP Definition"* for address range definition.

- Note: Once lock-down by factory or customer, the corresponding range cannot be changed any more. While in secured OTP mode, array access is not allowed.

Table 5. Secured OTP Definition

Address range	Size	Lock-down
xxx000~xxx1FF	4096-bit	Determined by Customer
xxx200~xxx3FF	4096-bit	Determined by Factory

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7. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command# sequence is inputted to this device, this device becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this device should be High-Z.

3. When correct command# sequence is inputted to this device, this device becomes active mode and keeps the active mode until next CS# rising edge.

4. When device under STR mode, input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. When device under DTR mode, input data is latched on the both rising and falling edge of Serial Clock (SCLK) and data shifts out on both rising and falling edge of SCLK.

5. While a Write Status Register, access to the memory array is neglected.

6. When Program or Erase is in progress, read command can be issued on any of the three non-busy banks.

Figure 1. Input Timing (STR mode)

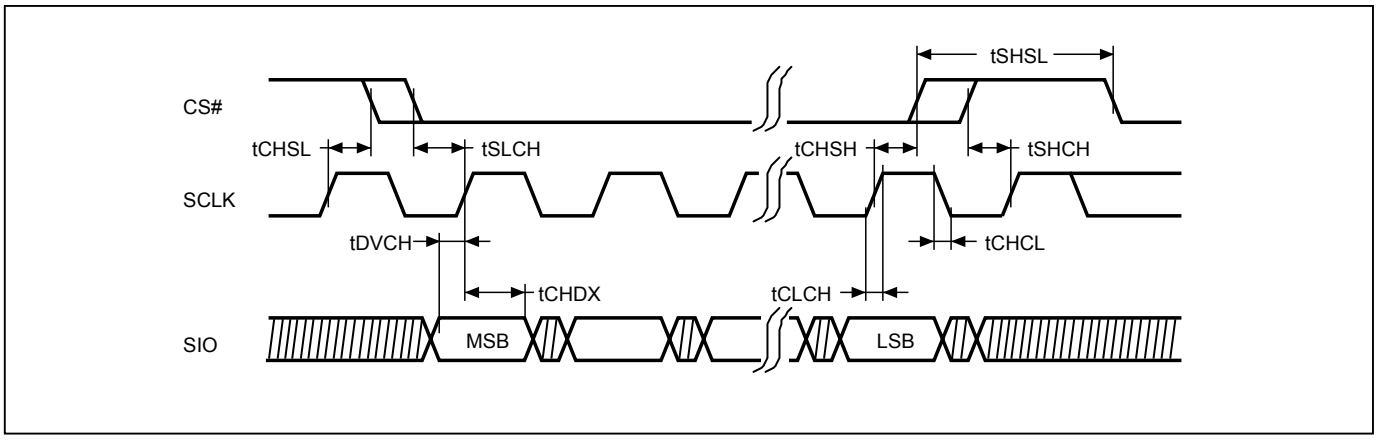
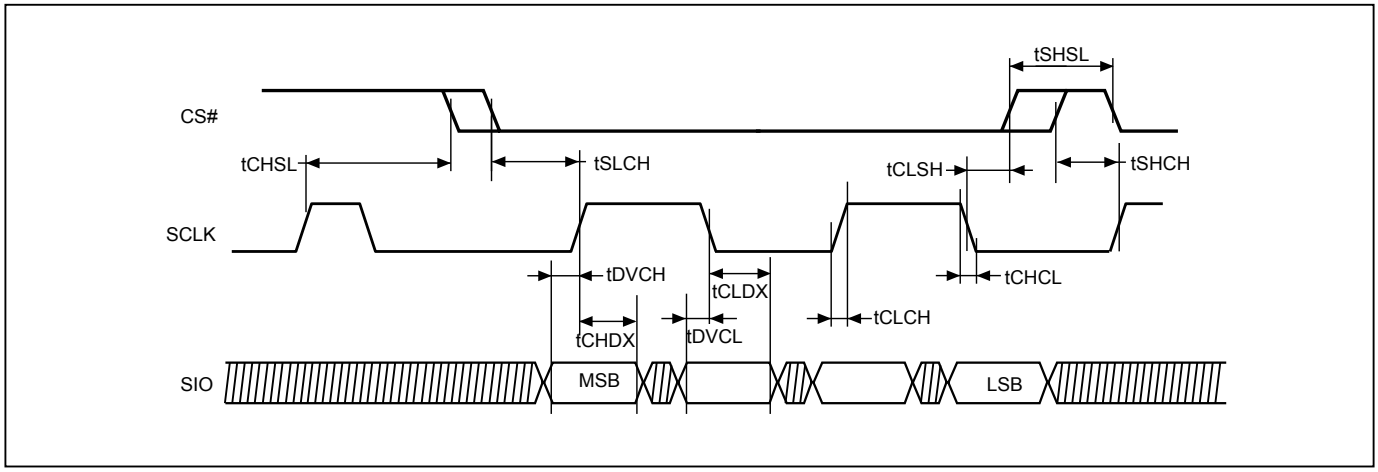


Figure 2. Input Timing (DTR mode)



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Figure 3. Output Timing (STR mode)

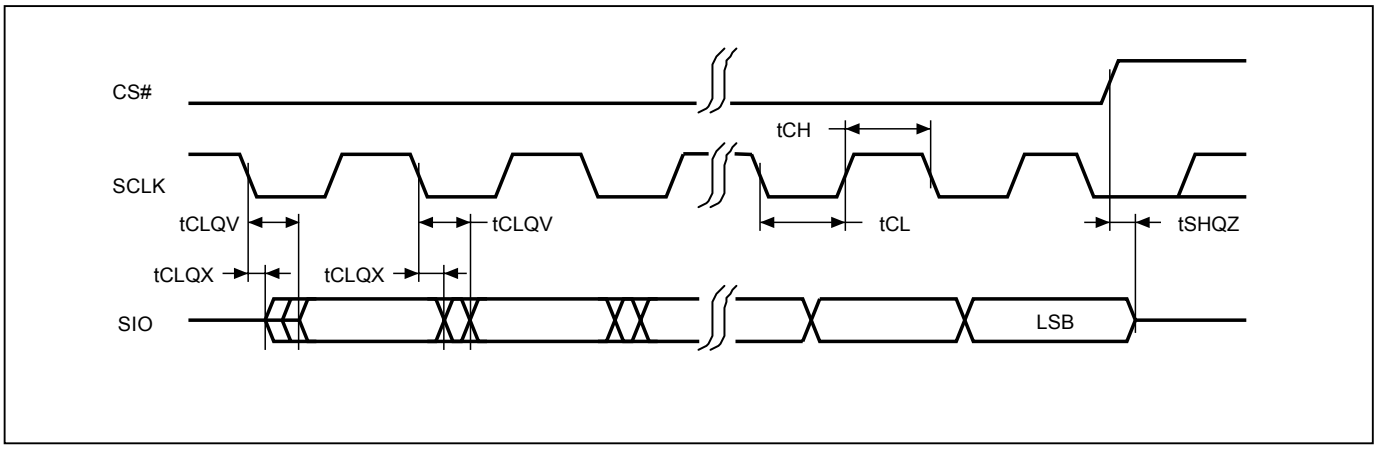
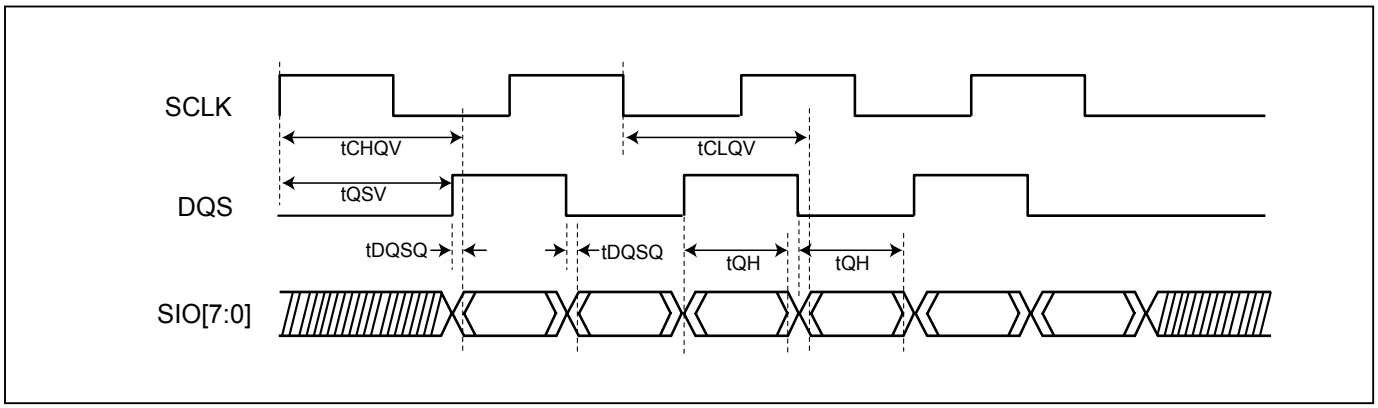


Figure 4. Output Timing (DTR mode)



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8. COMMAND SET

8-1. SPI Command Set

	Command Code	Address Byte					Dummy Cycle	Data Byte
		Total ADD Byte	Byte 1	Byte 2	Byte 3	Byte 4		
Array access								
READ3B (normal read)	03 (hex)	3	ADD1	ADD2	ADD3		0	1- ∞
FAST READ3B (fast read data)	0B (hex)	3	ADD1	ADD2	ADD3		8	1- ∞
PP3B (page program)	02 (hex)	3	ADD1	ADD2	ADD3		0	1-256
SE3B (sector erase)	20 (hex)	3	ADD1	ADD2	ADD3		0	0
BE3B (block erase 64KB)	D8 (hex)	3	ADD1	ADD2	ADD3		0	0
READ4B	13 (hex)	4	ADD1	ADD2	ADD3	ADD4	0	1- ∞
FAST READ4B	0C (hex)	4	ADD1	ADD2	ADD3	ADD4	8	1- ∞
PP4B	12 (hex)	4	ADD1	ADD2	ADD3	ADD4	0	1-256
SE4B (Sector erase 4KB)	21 (hex)	4	ADD1	ADD2	ADD3	ADD4	0	0
BE4B (block erase 64KB)	DC (hex)	4	ADD1	ADD2	ADD3	ADD4	0	0
CE (chip erase)	60 or C7 (hex)	0					0	0
Write Buffer Access								
RDBUF (Write Buffer Read)	25 (hex)	4	ADD1	ADD2	ADD3	ADD4	8	1-256
WRBI (Write Buffer Initial)	22 (hex)	4	ADD1	ADD2	ADD3	ADD4	0	0-256
WRCT (Write Buffer Continue)	24 (hex)	4	ADD1	ADD2	ADD3	ADD4	0	0-256
WRCF (Write Buffer Confirm)	31 (hex)	0					0	0
Device operation								
WREN (write enable)	06 (hex)	0					0	0
WRDI (write disable)	04 (hex)	0					0	0
WPSEL (Write Protect Selection)	68 (hex)	0					0	0
PGM/ERS Suspend (Suspends Program/ Erase)	B0 (hex)	0					0	0
PGM/ERS Resume (Resumes Program/ Erase)	30 (hex)	0					0	0
DP (Deep power down)	B9 (hex)	0					0	0
NOP (No Operation)	00 (hex)	0					0	0

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	Command Code	Address Byte					Dummy Cycle	Data Byte
		Total ADD Byte	Byte 1	Byte 2	Byte 3	Byte 4		
RSTEN (Reset Enable)	66 (hex) *(Note2)*	0					0	0
RST (Reset Memory)	99 (hex) *(Note2)*	0					0	0
GBLK (gang block lock)	7E (hex)	0					0	0
GBULK (gang block unlock)	98 (hex)	0					0	0
Register Access								
RDID (read identification)	9F (hex)	0					0	3
RDSFDP (Read SFDP Table)	5A (hex)	3	ADD1	ADD2	ADD3		8	0
RDSR (read status register)	05 (hex)	0					0	1
RDCR (read configuration register)	15 (hex)	0					0	1
WRSR/WRCR (write status/configuration register)	01 (hex)	0					0	1-2
RDCR2 (read configuration register2)	71 (hex)	4	ADD1	ADD2	ADD3	ADD4	0	1
WRCR2 (write configuration register2)	72 (hex)	4	ADD1	ADD2	ADD3	ADD4	0	1
RDSCUR (read security register)	2B (hex)	0					0	0
WRSCUR (write security register)	2F (hex)	0					0	0
RDFBR (read fast boot register)	16 (hex)	0					0	1-4
WRFBR (write fast boot register)	17 (hex)	0					0	4
ESFBR (erase fast boot register)	18 (hex)	0					0	0
SBL (Set Burst Length)	C0 (hex)	0					0	1
ENSO (enter secured OTP)	B1 (hex)	0					0	0
EXSO (exit secured OTP)	C1 (hex)	0					0	0
WRLR (write Lock register)	2C (hex)	0					0	1
RDLR (read Lock register)	2D (hex)	0					0	1
WRSPB (SPB bit program)	E3 (hex)	4	ADD1	ADD2	ADD3	ADD4	0	0
ESSPB (all SPB bit erase)	E4 (hex)	0					0	0
RDSPB (read SPB status)	E2 (hex)	4	ADD1	ADD2	ADD3	ADD4	0	1

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	Command Code	Address Byte					Dummy Cycle	Data Byte
		Total ADD Byte	Byte 1	Byte 2	Byte 3	Byte 4		
WRDPB (write DPB register)	E1 (hex)	4	ADD1	ADD2	ADD3	ADD4	0	1
RDDPB (read DPB register)	E0 (hex)	4	ADD1	ADD2	ADD3	ADD4	0	1
RDPASS (read password register)	27 (hex)	4	00h	00h	00h	00h	8	8
WRPASS (write password register)	28 (hex)	4	00h	00h	00h	00h	0	8
PASSULK (password unlock)	29 (hex)	4	00h	00h	00h	00h	0	8

Note 1: It is not recommended to adopt any other code/address not in the command definition table, which will potentially enter the hidden mode.

Note 2: The RSTEN command must be executed before executing the RST command. If any other command is issued in-between RSTEN and RST, the RST command will be ignored.

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8-2. OPI Command Set

	Command Set		8-8-8 (STR)	8-8-8 (DTR)	Address Byte					Dummy Cycle	Data Byte
	1'st Byte	2'nd Byte			Total ADD Byte	Byte 1	Byte 2	Byte 3	Byte 4		
Array access											
8READ (8 I/O read)	EC (hex)	13 (hex)	V		4	ADD1	ADD2	ADD3	ADD4	6-20 *(Note3)*	1- ∞
8DTRD (8 I/O DT Read)	EE (hex)	11 (hex)		V	4	ADD1	ADD2	ADD3	ADD4 *(Note5)*	6-20 *(Note3)*	1- ∞
PP4B (Page Program)	12 (hex)	ED (hex)	V	V	4	ADD1	ADD2	ADD3	ADD4 *(Note5)*	0	1-256
SE4B (Sector erase 4KB)	21 (hex)	DE (hex)	V	V	4	ADD1	ADD2	ADD3	ADD4	0	0
BE4B (block erase 64KB)	DC (hex)	23 (hex)	V	V	4	ADD1	ADD2	ADD3	ADD4	0	0
CE (chip erase)	60 or C7 (hex)	9F or 38 (hex)	V	V	0					0	0
Write Buffer Access											
RDBUF (Read Buffer)	25 (hex)	DA (hex)		V	4	ADD1	ADD2	ADD3	ADD4	6-20	1-256
WRBI (Write Buffer Initial)	22 (hex)	DD (hex)	V	V	4	ADD1	ADD2	ADD3	ADD4	0	0-256
WRCT (Write Buffer Continue)	24 (hex)	DB (hex)	V	V	4	ADD1	ADD2	ADD3	ADD4	0	0-256
WRCF (Write Buffer Confirm)	31 (hex)	CE (hex)	V	V	0					0	0
Device operation											
WREN (write enable)	06 (hex)	F9 (hex)	V	V	0					0	0
WRDI (write disable)	04 (hex)	FB (hex)	V	V	0					0	0
WPSEL (Write Protect Selection)	68 (hex)	97 (hex)	V	V	0					0	0
PGM/ERS Suspend (Suspends Program/ Erase)	B0 (hex)	4F (hex)	V	V	0					0	0
PGM/ERS Resume (Resumes Program/ Erase)	30 (hex)	CF (hex)	V	V	0					0	0
DP (Deep power down)	B9 (hex)	46 (hex)	V	V	0					0	0
NOP (No Operation)	00 (hex)	FF (hex)	V	V	0					0	0
RSTEN (Reset Enable)	66 (hex) *(Note2)*	99 (hex)	V	V	0					0	0
RST (Reset Memory)	99 (hex) *(Note2)*	66 (hex)	V	V	0					0	0
GBLK (gang block lock)	7E (hex)	81 (hex)	V	V	0					0	0
GBULK (gang block unlock)	98 (hex)	67 (hex)	V	V	0					0	0

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	Command Set		8-8-8 (STR)	8-8-8 (DTR)	Address Byte					Dummy Cycle	Data Byte
	1'st Byte	2'nd Byte			Total ADD Byte	Byte 1	Byte 2	Byte 3	Byte 4		
Register Access											
RDID (read identification)	9F (hex)	60 (hex)	V	V	4	00h	00h	00h	00h	4	3 *(Note6)*
RDSFDP (Read SFDP Table)	5A (hex)	A5 (hex)	V	V	4	ADD1	ADD2	ADD3	ADD4	20	
RDSR (read status register)	05 (hex)	FA (hex)	V	V	4	00h	00h	00h	00h	4 *(Note4)*	1
RDCR (read configuration register)	15 (hex)	EA (hex)	V	V	4	00h	00h	00h	01h	4 *(Note4)*	1
WRSR (write status register)	01 (hex)	FE (hex)	V	V	4	00h	00h	00h	00h	0	1
WRCR (configuration register)	01 (hex)	FE (hex)	V	V	4	00h	00h	00h	01h	0	1
RDCR2 (read configuration register2)	71 (hex)	8E (hex)	V	V	4	ADD1	ADD2	ADD3	ADD4	4 *(Note4)*	1
WRCR2 (write configuration register2)	72 (hex)	8D (hex)	V	V	4	ADD1	ADD2	ADD3	ADD4	0	1
RDSCUR (read security register)	2B (hex)	D4 (hex)	V	V	4	00h	00h	00h	00h	4 *(Note4)*	1
WRSCUR (write security register)	2F (hex)	D0 (hex)	V	V	0					0	0
SBL (Set Burst Length)	C0 (hex)	3F (hex)	V	V	4	00h	00h	00h	00h	0	1
RDFBR (read fast boot register)	16 (hex)	E9 (hex)	V	V	4	00h	00h	00h	00h	4 *(Note4)*	1-4 *(Note6)*
WRFBR (write fast boot register)	17 (hex)	E8 (hex)	V	V	4	00h	00h	00h	00h	0	4
ESFBR (erase fast boot register)	18 (hex)	E7 (hex)	V	V	0					0	0
ENSO (enter secured OTP)	B1 (hex)	4E (hex)	V	V	0					0	0
EXSO (exit secured OTP)	C1 (hex)	3E (hex)	V	V	0					0	0
WRLR (write Lock register)	2C (hex)	D3 (hex)	V	V	4	00h	00h	00h	00h	0	1
RDLR (read Lock register)	2D (hex)	D2 (hex)	V	V	4	00h	00h	00h	00h	4 *(Note4)*	1
WRSPB (SPB bit program)	E3 (hex)	1C (hex)	V	V	4	ADD1	ADD2	ADD3	ADD4	0	0
ESSPB (all SPB bit erase)	E4 (hex)	1B (hex)	V	V	0					0	0
RDSPB (read SPB status)	E2 (hex)	1D (hex)	V	V	4	ADD1	ADD2	ADD3	ADD4	6-20 *(Note3)*	1
WRDPB (write DPB register)	E1 (hex)	1E (hex)	V	V	4	ADD1	ADD2	ADD3	ADD4	0	1
RDDPB (read DPB register)	E0 (hex)	1F (hex)	V	V	4	ADD1	ADD2	ADD3	ADD4	6-20 *(Note3)*	1
RDPASS (read password register)	27 (hex)	D8 (hex)	V	V	4	00h	00h	00h	00h	20	8
WRPASS (write password register)	28 (hex)	D7 (hex)	V	V	4	00h	00h	00h	00h	0	8
PASSULK (password unlock)	29 (hex)	D6 (hex)	V	V	4	00h	00h	00h	00h	0	8

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Note 1: It is not recommended to adopt any other code/address not in the command definition table, which will potentially enter the hidden mode.

Note 2: The RSTEN command must be executed before executing the RST command. If any other command is issued in-between RSTEN and RST, the RST command will be ignored.

Note 3: See dummy cycle and frequency table.

Note 4: 4 dummy cycles in both STR/DTR.

Note 5: The starting address must be even byte (A0 must be 0) in DTR OPI mode.

Note 6: Data bytes are always output in STR.

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9. REGISTER DESCRIPTION

9-1. Status Register

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit is a volatile bit that is set to “1” by the WREN instruction. WEL needs to be set to “1” before the device can accept program and erase instructions, otherwise the program and erase instructions are ignored. WEL automatically clears to “0” when a program or erase operation completes. To ensure that both WIP and WEL are “0” and the device is ready for the next program or erase operation, it is recommended that WIP be confirmed to be “0” before checking that WEL is also “0”. If a program or erase instruction is applied to a protected memory area, the instruction will be ignored and WEL will clear to “0”.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in *Table 4*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP/PP3B/PP4B), Sector Erase (SE/SE3B/SE4B), Block Erase (BE/BE3B/BE4B) and Chip Erase (CE) instructions (only if Block Protect bits (BP3:BP0) set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default. Which is un-protected.

Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved	Reserved	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
Reserved	Reserved	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Reserved	Reserved	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note 1: see the *Table 4* "Protected Area Size".

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9-2. Configuration Register

The Configuration Register is able to change the default status of Flash memory. Flash memory will be configured after the CR bit is set.

ODS bit
The output driver strength (ODS2, ODS1, ODS0) bits are volatile bits, which indicate the output driver level (as defined in *"Table 6. Output Driver Strength Table"*) of the device. After power-up or reset operation, the ODS bits' value are determined by settings in NV-CR2 register and is defaulted 24ohm when delivered from factory. To write the ODS bits requires the Write Status Register (WRSR) instruction to be executed.

TB bit
The Top/Bottom (TB) bit is a non-volatile bit. The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bit (BP3, BP2, BP1, BP0), starting from TOP or Bottom of the memory array. The TB bit is defaulted as “0”, which means Top area protect. When it is set as “1”, the protect area will change to Bottom area of the memory device. To write the TB bits requires the Write Status Register (WRSR) instruction to be executed.

PBE bit
The Preamble Bit Enable (PBE) bit is a volatile bit. It is used to enable or disable the preamble bit data pattern output on dummy cycles. When shipping from factory, the PBE bit is defaulted as “0”, which means preamble bit is disabled. When it is set as “1”, the preamble bit will be enabled, and inputted into dummy cycles. To write the PBE bits requires the Write Status Register (WRSR) instruction to be executed. System could change power-up or reset value of the PBE bit via setting NV-CR2 register.

Configuration Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved	Reserved	Reserved	PBE (Preamble bit Enable)	TB (top/bottom selected)	ODS 2 (output driver strength)	ODS 1 (output driver strength)	ODS 0 (output driver strength)
x	x	x	0=Disable 1=Enable	0=Top area protect 1=Bottom area protect (Default=0)	(Note 1)	(Note 1)	(Note 1)
x	x	x	volatile bit	OTP	volatile bit	volatile bit	volatile bit

Note 1: see *"Table 6. Output Driver Strength Table"*.

Table 6. Output Driver Strength Table

ODS2	ODS1	ODS0	Resistance (Ohm)	Note
0	0	0	146 Ohms	Impedance at VCC/2 (Typical)
0	0	1	76 Ohms	
0	1	0	52 Ohms	
0	1	1	41 Ohms	
1	0	0	34 Ohms	
1	0	1	30 Ohms	
1	1	0	26 Ohms	
1	1	1	24 Ohms (Default)	

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9-3. Configuration Register 2

The MX25LW51245G product provides both Volatile and Non-Volatile configuration registers to set the device operation condition.

Non-Volatile configuration register bits are used to set the default device status. After the default status has been set, device will return to this default status after a power-on action or a reset cycle.

Notes:
1. The NV-CR2 bits are "one time programmable" (OTP). Once they have been set, the bit values cannot be altered anymore.
2. To prevent users from accidentally starting the status configuration, MX25LW51245G product provides NV-CR2 locked down bit (40000100h bit[0]: FTRLKDN bit) to lock the NV-CR2 configuration. We strongly suggest users to lock the FTRLKDN bit after the completion of default device status setting.

MX25LW51245G also provides Volatile configuration register bits to temporarily change the device operation condition. Volatile-CR2 bits can be set to change the setting originally set by NV-CR2 bits. To clear the volatile-CR2 setting, users can initiate a power-on action or reset cycle, and the device will return to the default status set by NV-CR2 bits.

Table 7. Configuration Register 2 - Volatile Bit

Address	Bit	Symbol	Description	Define	Factory Default	Readable/ Writable	Type
00000000h	Bit 7-4	x	Reserved (4)	Reserved	0	x	x
	Bit 3	CRCEN	Enable Parity checking	1= Parity check Enable 0= Parity check Disable	0	R/W	Volatile Bit
	Bit 2	x	Reserved (4)	Reserved	0	x	x
	Bit 1	DOPI (3)	DTR OPI Enable	00= SPI 01= STR OPI enable 10= DTR OPI enable 11= inhibit	0	R/W	Volatile Bit
	Bit 0	SOPI (3)	STR OPI Enable		0	R/W	Volatile Bit
00000200h	Bit 7-2	x	Reserved (4)	Reserved	0	x	x
	Bit 1	DOS	DQS on STR mode	0= Disable 1= Enable	0	R/W	Volatile Bit
	Bit 0	DQSPRC	DTR DQS pre-cycle	DOPI: 0= 0 cycle 1= 1 cycle SOPI: Reserved	0	R/W	Volatile Bit
00000300h	Bit 7-3	x	Reserved (4)	Reserved	0	x	x
	Bit 2-0	DC	Dummy cycle	Refer to *"Dummy Cycle and Frequency Table (MHz)"*	0	R/W	Volatile Bit
00000400h	Bit 7-2	x	Reserved (4)	Reserved	0	x	x
	Bit 1-0	ECS	ECS# pin goes low define	00= 2 bit error or double programmed 01= 1 or 2 bit error or double programmed 10= 2 bit error only 11= 1 or 2 bit error	0	R/W	Volatile Bit

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Address	Bit	Symbol	Description	Define	Factory Default	Readable/ Writable	Type
00000500h	Bit 7	CRCBIN	CRC# input enable	0= CRC# input Disable 1= CRC# input Enable	0	R/W	Volatile Bit
	Bit 6-5	CRC CYC	CRC chunk size configuration	00= 16Byte 01= 32Byte 10= 64Byte 11= 128Byte	0	R/W	Volatile Bit
	Bit 4	CRCBEN	CRC# output enable	0= CRC# output Disable 1= CRC# output Enable	0	R/W	Volatile Bit
	Bit 3-1	x	Reserved (4)	Reserved	0	x	x
	Bit 0	PPTSEL	Preamble pattern selection	refer to *"9-3-2. Preamble Pattern Select Bit Table"*	0	R/W	Volatile Bit
00000800h (9)	Bit 7	ECCFAVLD	ECC fail address valid indicator	0= ECC failure address invalid (no fail address recorded) 1= ECC failure address valid (there's fail address recorded)	0	R	Volatile Bit
	Bit 6-4	ECCFS	ECC fail status	000= None xx1= 1 bit corrected x1x= 2 bits deteced 1xx= Double programmed page detected	0	R	Volatile Bit
	Bit 3-0	*ECCCNT*(1)	ECC failure chunk counter		0	R	Volatile Bit
00000C00h(2)	Bit 7-4	ECCFA	ECC failure chunk address	ECC 1st failure chunk address(A7:A4)	x	R	Volatile Bit
	Bit 3-0	x	Reserved (4)	Reserved	x	x	Volatile Bit
00000D00h(2)	Bit 7-0	ECCFA	ECC failure chunk address	ECC 1st failure chunk address(A15:A8)	x	R	Volatile Bit
00000E00h(2)	Bit 7-0	ECCFA	ECC failure chunk address	ECC 1st failure chunk address(A23:A16)	x	R	Volatile Bit
00000F00h(2)	Bit 7-2	x	Reserved (4)	Reserved	x	x	Volatile Bit
	Bit 1-0	ECCFA	ECC failure chunk address	ECC 1st failure chunk address(A25:A24)	x	R	Volatile Bit
Cx000000h(5)(7)	Bit 7-2	x	Reserved (4)	x	x	x	x
	Bit 1	RWWBS(6)	RWW Bank Status 0= ready 1= busy	00= No active program or erase operation 01= program/erase in other bank 10= invalid 11= program/erase operation in addressed bank	0	R	Volatile Bit
	Bit 0	RWWDS	RWW Device Status 0= ready 1= busy		0	R	Volatile Bit

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Address	Bit	Symbol	Description	Define	Factory Default	Readable/ Writable	Type
80000000h (10)	Bit 7-5	x	Reserved (4)	Reserved	x	x	x
	Bit 4	CRCERR	CMD# or Parity checked fail	0= CMD# or Parity check pass 1= CMD# or Parity check fail	0	R	Volatile Bit
	Bit 3	WBSS	Write buffer sequence status	0= Not initiated 1= Initiated	0	R	Volatile Bit
	Bit 2-0	x	Reserved (4)	Reserved	x	x	x
80000100h	Bit 7-4	x	Reserved (4)	x	x	x	x
	Bit 3	BKST3(8)	Bank3 status	1: Bank during program/ erase operation 0: Bank is ready	0	R	Volatile bit
	Bit 2	BKST2(8)	Bank2 status				
	Bit 1	BKST1(8)	Bank1 status				
	Bit 0	BKST0(8)	Bank0 status				

Notes:
1. ECC failure chunk counter (00000800h bit[3:0]) stops counting once reach maximum value 15. The counting number increases if user reads the failure chunk multipe times.
2. ECC fail address only records first fail chunk fail address. For both 1bit and 2bit fail. ECCFA is valid only if ECCFAVLD value is 1.
3. The default status of DOPI and SOPI in volatile bit reflect the DOPI# and SOPI# setting in nonvolatile bit. For example, if DOPI#/SOPI# are 01, DOPI and SOPI value will change to 10 after next Power on or reset and default status of the device will be DTR OPI.
4. All reserved bits must keep value factory default. All addresses not shown in the table must keep value unchanged.
5. Cx000000h: A27~A24 for Bank Address identical. C0=Bank 0, C1=Bank 1, C2= Bank 2, C3=Bank 3.
6. The RWWBS bit will output specified Bank status according to identical bank address
7. RWWBS and RWWDS will be set to "11" when the device is in Write Register Mode.
8. BKST3-BKST0 will be set to "1" when the device is in Write Register Mode.
9. Write "00" data into 00000800h can reset the ECC status registers.
10. Write "00" data into 80000000h can reset the CMD# or Parity check status register.

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Table 8. Configuration Register 2 - Nonvolatile Bit

Address	Bit	Symbol	Description	Define	Factory Default	Readable/ Writable	Type
40000000h	Bit 7-4	x	Reserved (3)	Reserved	1111	x	x
	Bit 3	CRCEN#	Enable Parity checking	0= Parity check Enable 1= Parity check Disable	1	R/W	OTP
	Bit 2	x	Reserved (3)	Reserved	1	x	x
	Bit 1	DOPI# (1)	Enable DOPI after Power on or reset	00= inhibit 01= DTR OPI mode 10= STR OPI mode 11= SPI mode	1	R/W	OTP
	Bit 0	SOPI# (1)	Enable SOPI after Power on or reset		1	R/W	OTP
40000100h	Bit 7-1	x	Reserved (3)	Reserved	0000000	x	X
	Bit 0	FTRLKDN	Lock down all the NV bit of CR2	0= All NV bit of CR2 are unlock 1= All NV bit of CR2 are lockdown	0	R/W	OTP
40000200h	Bit 7-2	x	Reserved	Reserved	000000	x	X
	Bit 1	DOS	DQS on STR mode	0= Disable 1= Enable	0	R/W	OTP
	Bit 0	DQSPRC	DQS pre-toggle at DOPI mode	DOPI: 0= 0 cycle 1= 1 cycle	0	R/W	OTP
40000300h	Bit 7-3	x	Reserved (3)	Reserved	00000	x	X
	Bit 2-0	DC	Dummy cycle	Refer to *"Dummy Cycle and Frequency Table (MHz)"*	000	R/W	OTP
40000400h	Bit 7-2	x	Reserved (3)	Reserved	000000	x	X
	Bit 1-0	ECS	ECS# pin goes low define	00= 2 bit error or double programmed 01= 1 or 2 bit error or double programmed 10= 2 bit error only 11= 1 or 2 bit error	00	R/W	OTP
40000500h	Bit 7	CRCBIN	CRC# input enable	0= CRC# input Disable 1= CRC# input Enable	0	R/W	OTP
	Bit 6-5	CRC CYC	CRC chunk size configuration	00= 16Byte 01= 32Byte 10= 64Byte 11= 128Byte	00	R/W	OTP
	Bit 4	CRCBEN	CRC# output enable	0= CRC# output Disable 1= CRC# output Enable	0	R/W	OTP
	Bit 3-1	x	Reserved (3)	Reserved	000	x	X
	Bit 0	DLPPTSEL	Learning pattern selection (1 for logic CKB)	refer to *"9-3-2. Preamble Pattern Select Bit Table"*	0	R/W	OTP
40000600h	Bit 7-5	x	Reserved (3)	Reserved	000	R/W	OTP
	Bit 4	PBE	Data learning pattern enable	0= Disable 1=Enable	0	R/W	OTP
	Bit 3	x	Reserved (3)	Reserved	0	x	X
	Bit 2-0	ODS	Output strength selection	Refer to *"Table 6. Output Driver Strength Table"*	111	R/W	OTP

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Address	Bit	Symbol	Description	Define	Factory Default	Readable/ Writable	Type
40000700h	Bit 7-5	x	Reserved (3)	Reserved	000	x	X
	Bit 4	ENWRAP#	Enable wrap around	1= Disable 0=Enable	1	R/W	OTP
	Bit 3-2	x	Reserved (3)	Reserved	00	x	X
	Bit 1-0	WRAPSIZE	Wrap around size selection	00= Reserved 01= 16 Byte 10= 32 Byte 11= 64 Byte	00	R/W	OTP

Notes:
1. The default status of DOPI and SOPI in volatile bit reflect the DOPI# and SOPI# setting in nonvolatile bit. For example, if DOPI#/SOPI# are 01, DOPI and SOPI value will change to 10 after next Power on or reset and default status of the device will be DTR OPI.
2. The default DOPI# status depends on the device model selection.
3. All reserved bits must keep value factory default. All addresses not shown in the table must keep value unchanged.

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9-3-1. Dummy Cycle and Frequency Table (MHz)

DC [2:0]	Numbers of Dummy Cycle	Octa I/O STR (MHz)	Octa I/O DTR (MHz)
000(Default)	20	133	133
001	18	133	133
010	16	133	133
011	14	133	133
100	12	104	104
101	10	104	104
110	8	84	84
111	6	66	66

9-3-2. Preamble Pattern Select Bit Table

	All SIOs (Except SIO3)	SIO3
Bit 0= 0	0011 0100 1001 1010	0011 0101 0001 0100
Bit 0= 1	0101 0101 0101 0101	0101 0101 0101 0101

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9-4. Security Register

The definition of the Security Register bits is as below:

Erase Fail bit. The Erase Fail bit is a status flag, which shows the status of last Erase operation. It will be set to "1", if the erase operation fails or the erase region is protected. It will be set to "0", if the last operation is successful. Please note that it will not interrupt or stop any operation in the flash memory.

Program Fail bit. The Program Fail bit is a status flag, which shows the status of last Program operation. It will be set to "1", if the program operation fails or the program region is protected. It will be set to "0", if the last operation is successful. Please note that it will not interrupt or stop any operation in the flash memory.

Erase Suspend bit. Erase Suspend Bit (ESB) indicates the status of Erase Suspend operation. Users may use ESB to identify the state of flash memory. After the flash memory is suspended by Erase Suspend command, ESB is set to "1". ESB is cleared to "0" after erase operation resumes.

Program Suspend bit. Program Suspend Bit (PSB) indicates the status of Program Suspend operation. Users may use PSB to identify the state of flash memory. After the flash memory is suspended by Program Suspend command, PSB is set to "1". PSB is cleared to "0" after program operation resumes.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 4K-bit Secured OTP area cannot be updated any more. While it is in 8K-bit secured OTP mode, main array access is not allowed.

Secured OTP Indicator bit. The Secured OTP indicator bit shows the secured OTP area is locked by factory or not. When it is "0", it indicates non-factory lock; "1" indicates factory-lock.

Table 9. Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WPSEL	E_FAIL	P_FAIL	Reserved	ESB (Erase Suspend bit)	PSB (Program Suspend bit)	LDSO (indicate if lock-down)	Secured OTP indicator bit
0=normal WP mode 1=individual mode (default=0)	0=normal Erase succeed 1=indicate Erase failed (default=0)	0=normal Program succeed 1=indicate Program failed (default=0)	-	0=Erase is not suspended 1= Erase suspended (default=0)	0=Program is not suspended 1= Program suspended (default=0)	0 = not lock-down 1 = lock-down (cannot program/ erase OTP)	0 = non-factory lock 1 = factory lock
Non-volatile bit (OTP)	Volatile bit	Volatile bit	-	Volatile bit	Volatile bit	Non-volatile bit (OTP)	Non-volatile bit (Read only)

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10. COMMAND DESCRIPTION

10-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP/PP3B/PP4B, SE/SE3B/SE4B, BE/BE3B/BE4B, CE, WRSR, WRCR2, SBL, WRFBR, ESFBR, WRSCUR, WRLR, WSPB and ESSPB which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit. WREN is also required before initiation of write-to-buffer sequence (WRBI command).

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

WREN instruction is not allowed while the device is operating in PE mode or Write Register Mode.

Figure 5. Write Enable (WREN) Sequence (SPI Mode)

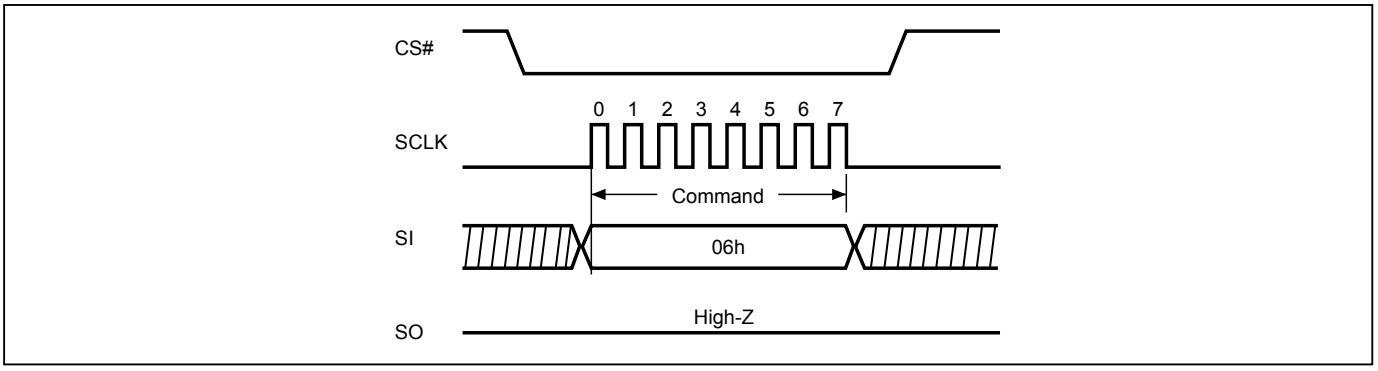


Figure 6. Write Enable (WREN) Sequence (STR-OPI Mode)

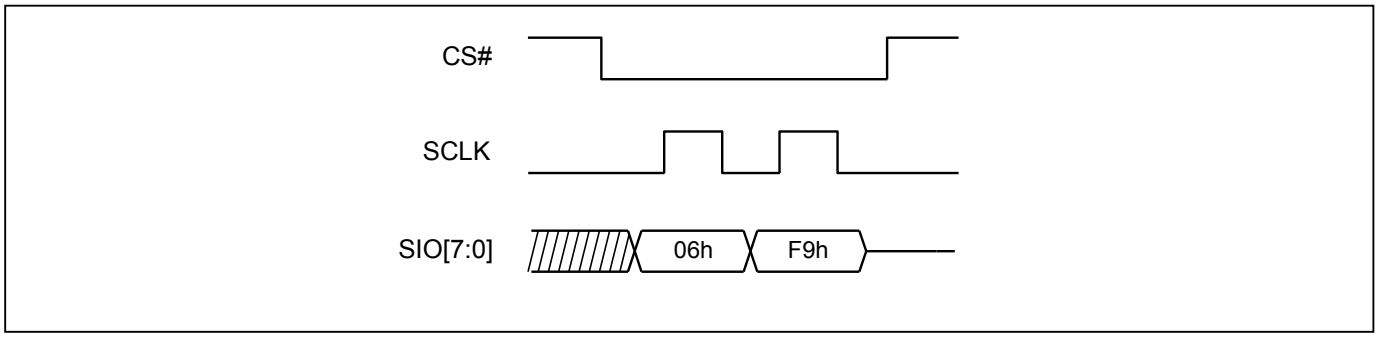
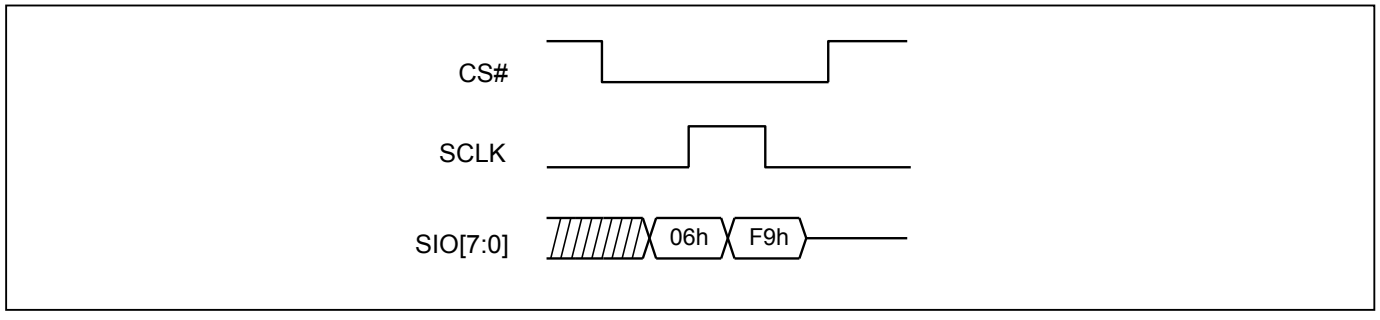


Figure 7. Write Enable (WREN) Sequence (DTR-OPI Mode)



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10-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit. The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high.
The WEL bit is reset by following situations:

- Power-up
- Reset# pin driven low
- WRDI command completion
- WRSR/WRCR/WRCR2 command completion
- PP/PP3B/PP4B/WRCF command completion
- SE/SE3B/SE4B/BE/BE3B/BE4B/CE command completion
- SBL command completion
- PGM/ERS Suspend command completion
- Softreset command completion
- WRSCUR command completion
- WRFBR/ESFBR command completion
- WRLR/WSPB/ESSPB command completion
- GBLK/GBULK command completion
- WRDPB command completion
- WPSEL command completion
- WRPASS, PASSULK command completion

WRDI command will abort the write-to-buffer sequence.

Figure 8. Write Disable (WRDI) Sequence (SPI Mode)

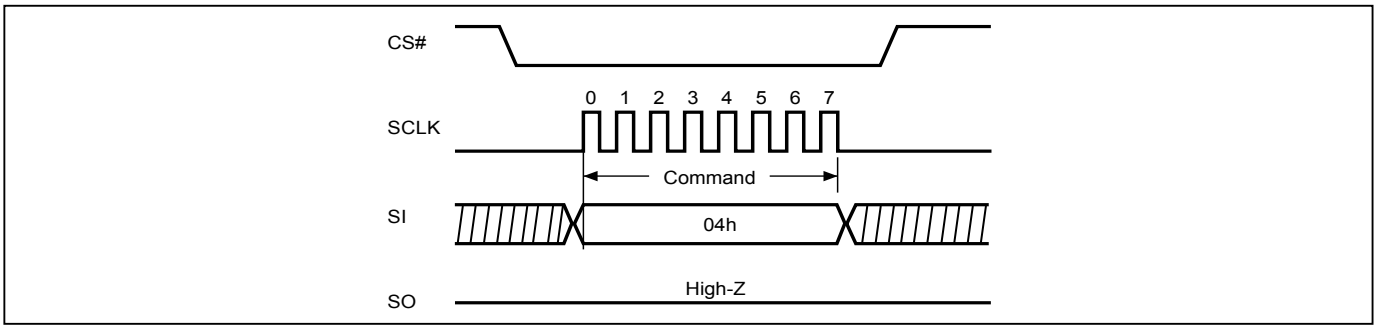


Figure 9. Write Disable (WRDI) Sequence (STR-OPI Mode)

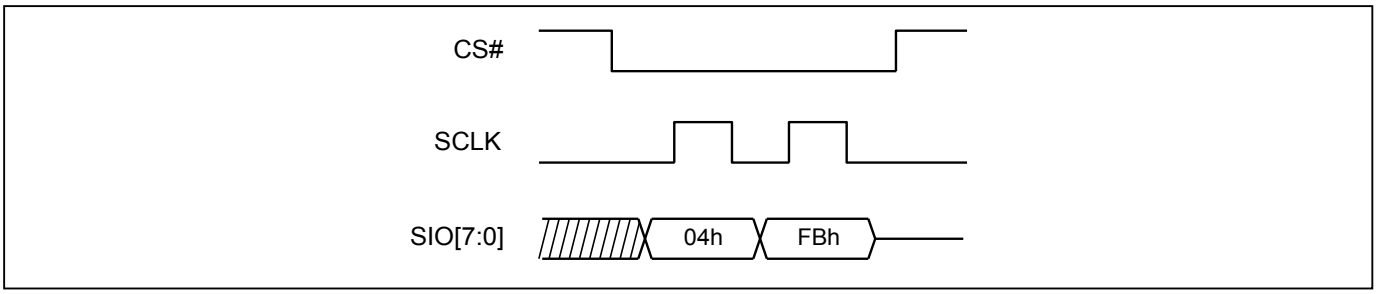
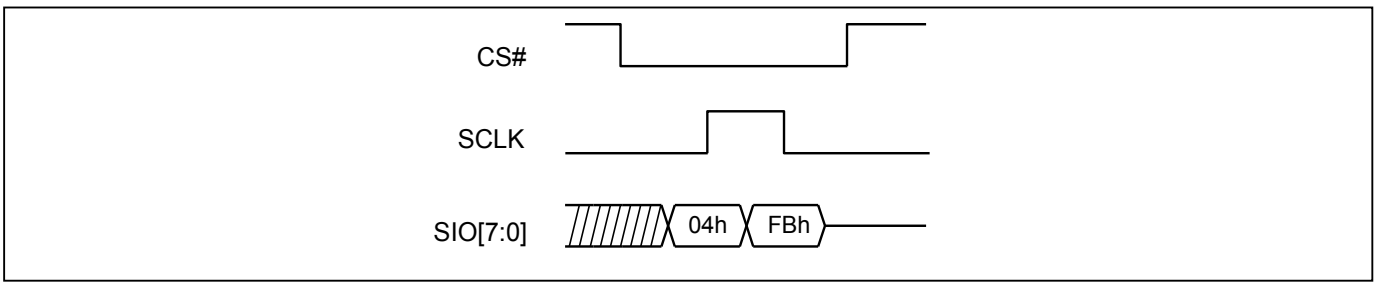


Figure 10. Write Disable (WRDI) Sequence (DTR-OPI Mode)



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10-3. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID and Device ID are listed as *Table 10* ID Definitions.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

RDID instruction is not allowed while the device is operating in PE mode or Write Register Mode.

Table 10. ID Definitions

RDID	9Fh	Manufacturer ID	Memory type	Memory density
		C2	86	3A

Figure 11. Read Identification (RDID) Sequence (SPI mode)

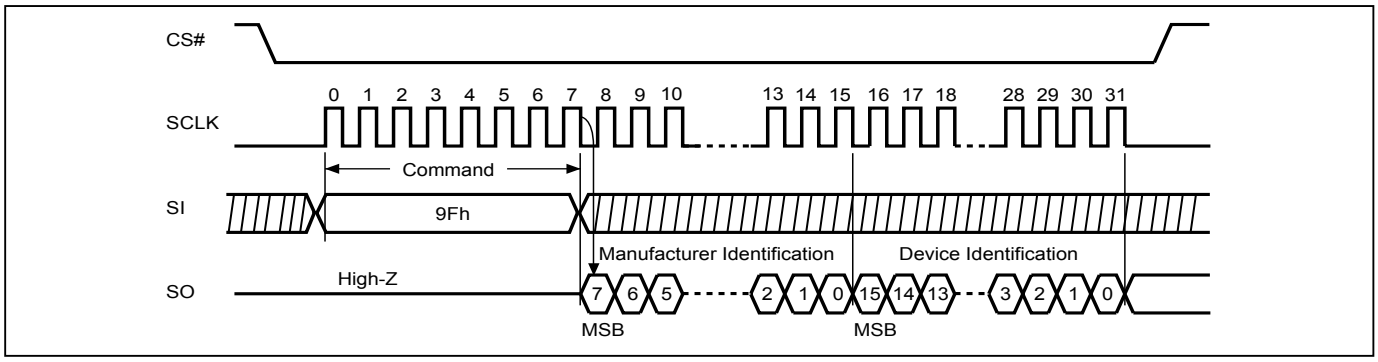


Figure 12. Read Identification (RDID) Sequence (STR-OPI Mode)

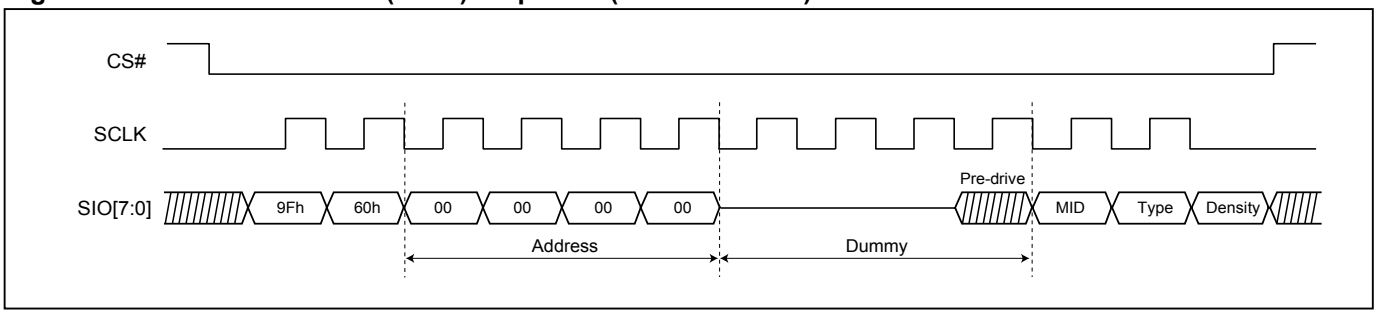
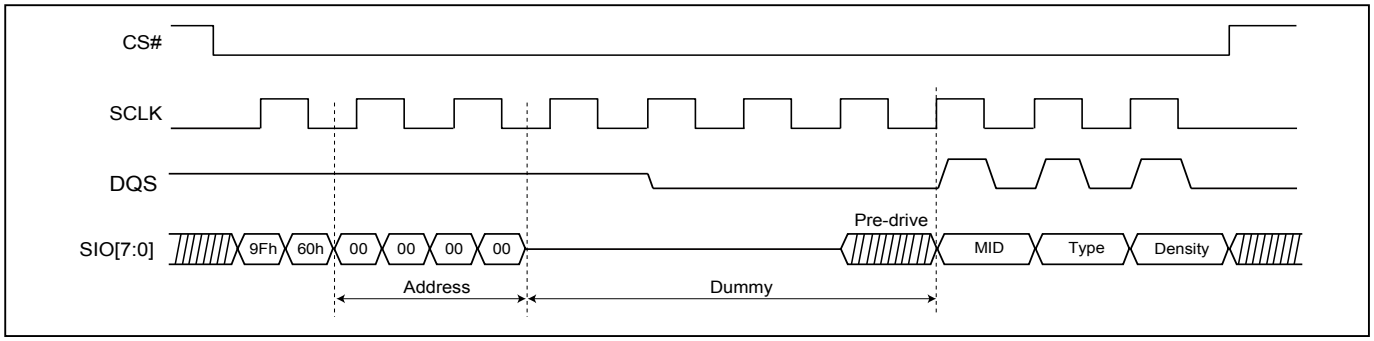


Figure 13. Read Identification (RDID) Sequence (DTR-OPI Mode)



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10-4. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO.

Figure 14. Read Status Register (RDSR) Sequence (SPI Mode)

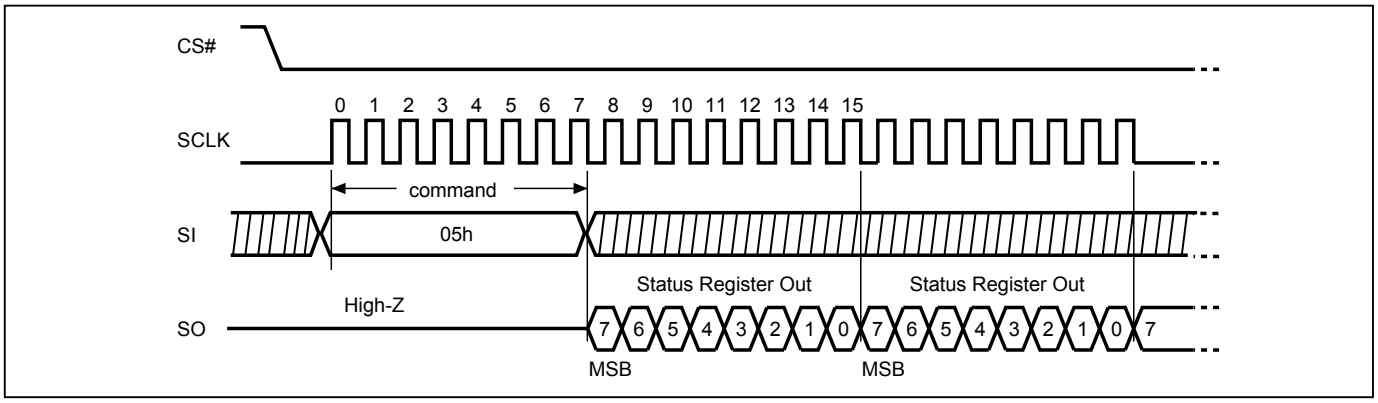


Figure 15. Read Status Register (RDSR) Sequence (STR-OPI Mode)

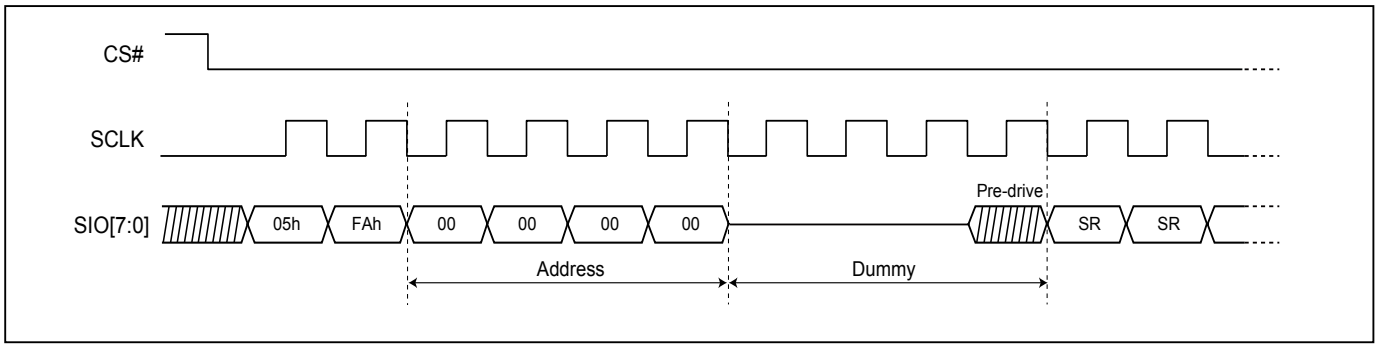
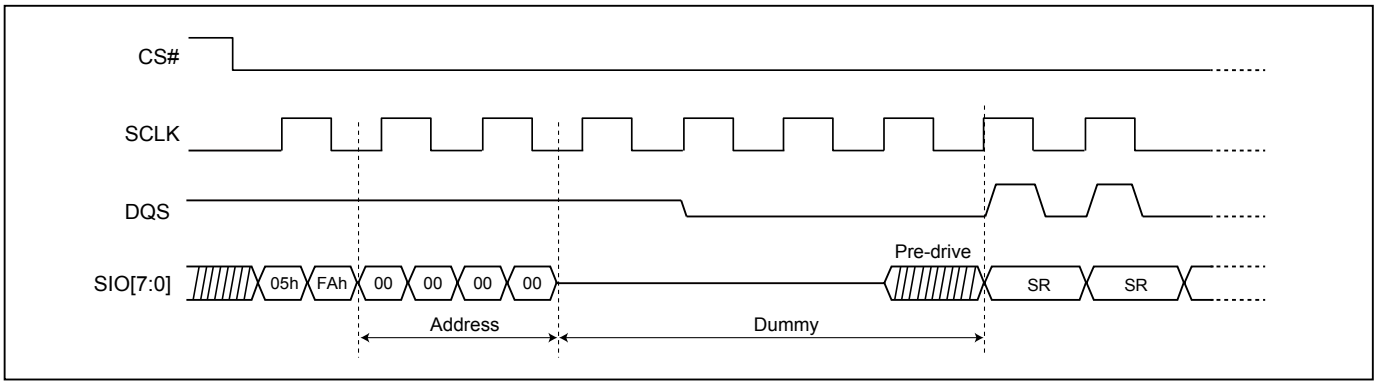


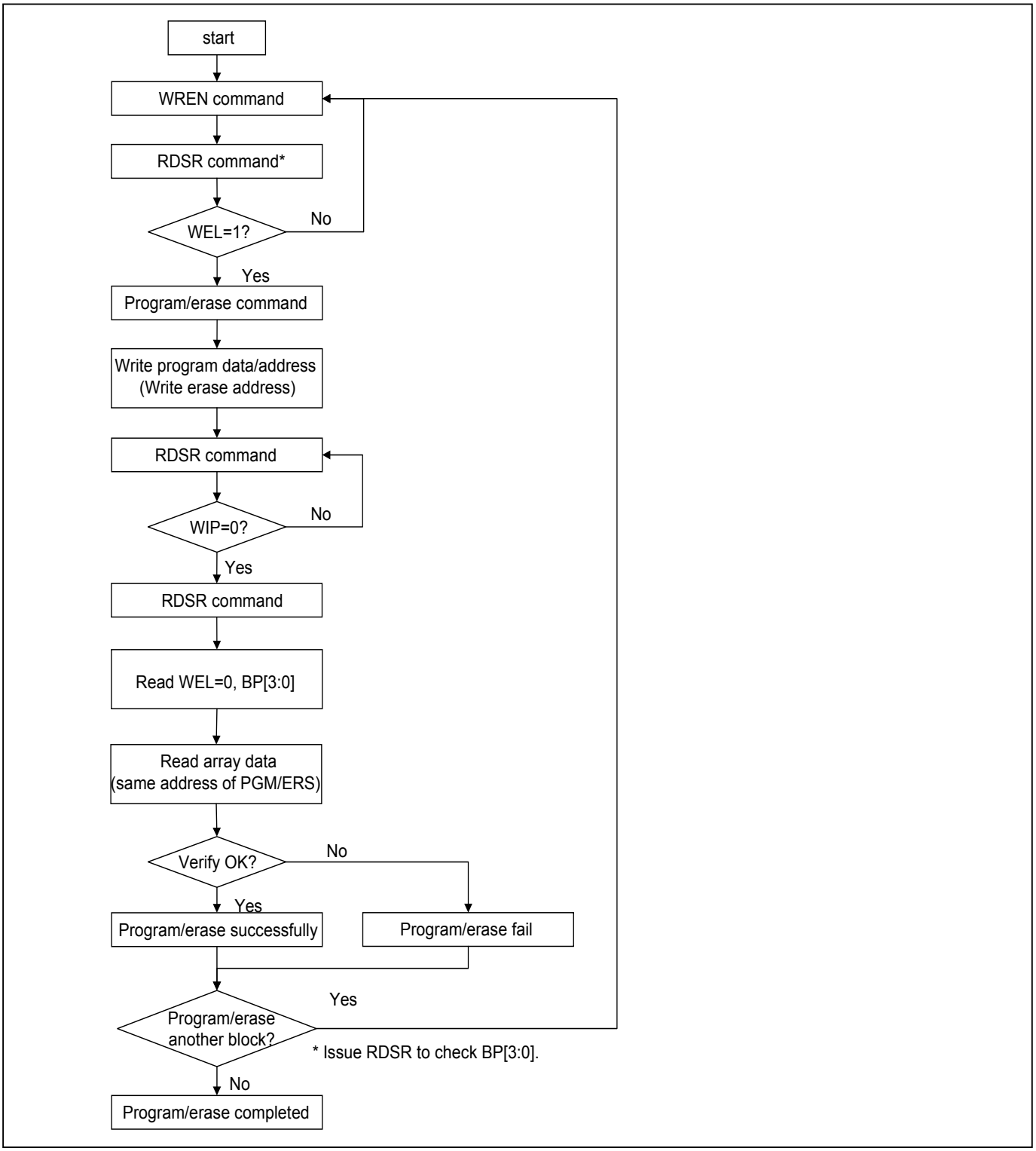
Figure 16. Read Status Register (RDSR) Sequence (DTR-OPI Mode)



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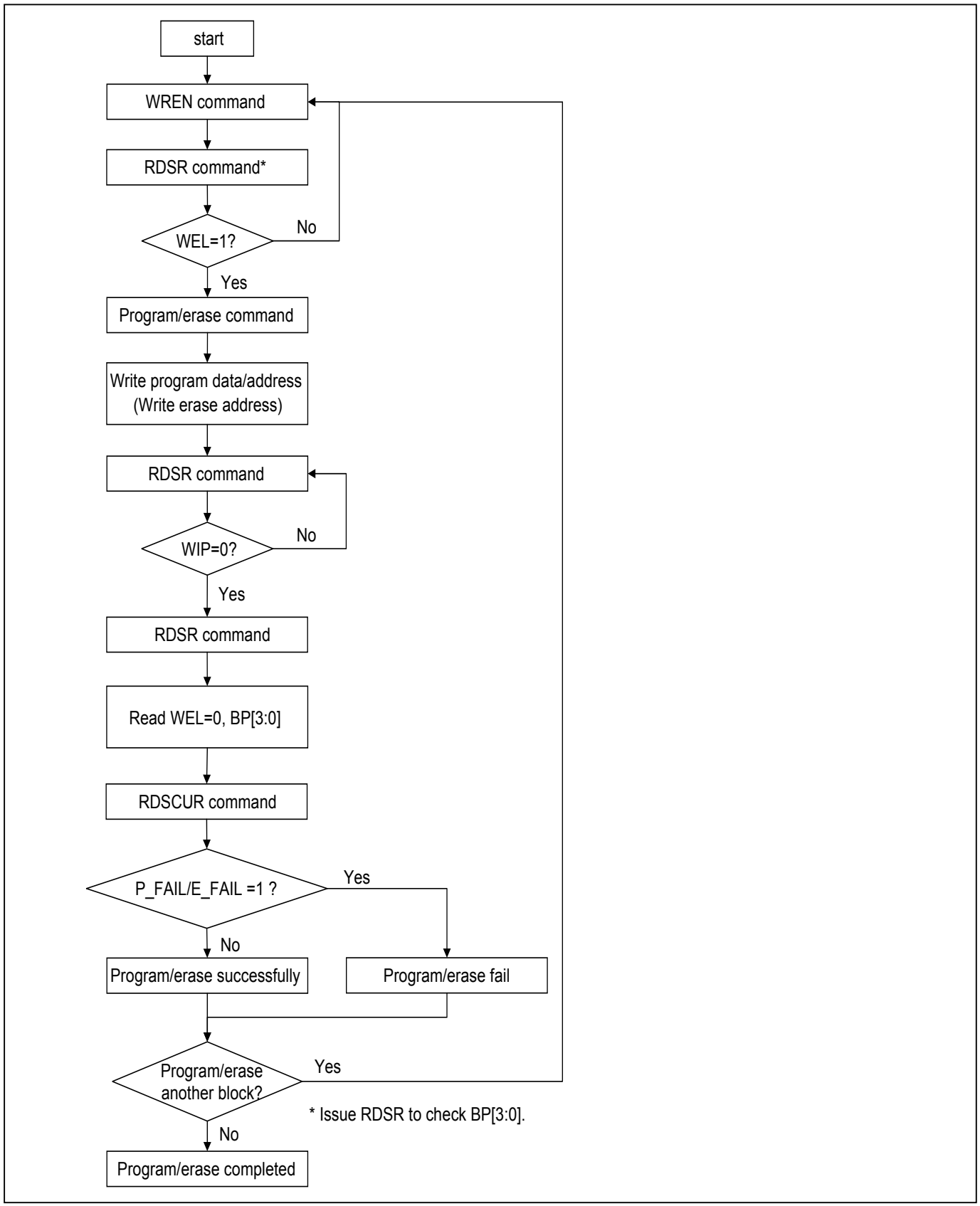
For user to check if Program/Erase operation is finished or not, RDSR instruction flow are shown as follows:

Figure 17. Program/Erase flow with read array data



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Figure 18. Program/Erase flow without read array data (read P_FAIL/E_FAIL flag)



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10-5. Read Configuration Register (RDCR)

The RDCR instruction is for reading Configuration Register Bits. The Read Configuration Register can be read at any time (even in program/erase/write configuration register condition).

The sequence of issuing RDCR instruction is: CS# goes low→ sending RDCR instruction code→ Configuration Register data out on SO.

Figure 19. Read Configuration Register (RDCR) Sequence (SPI Mode)

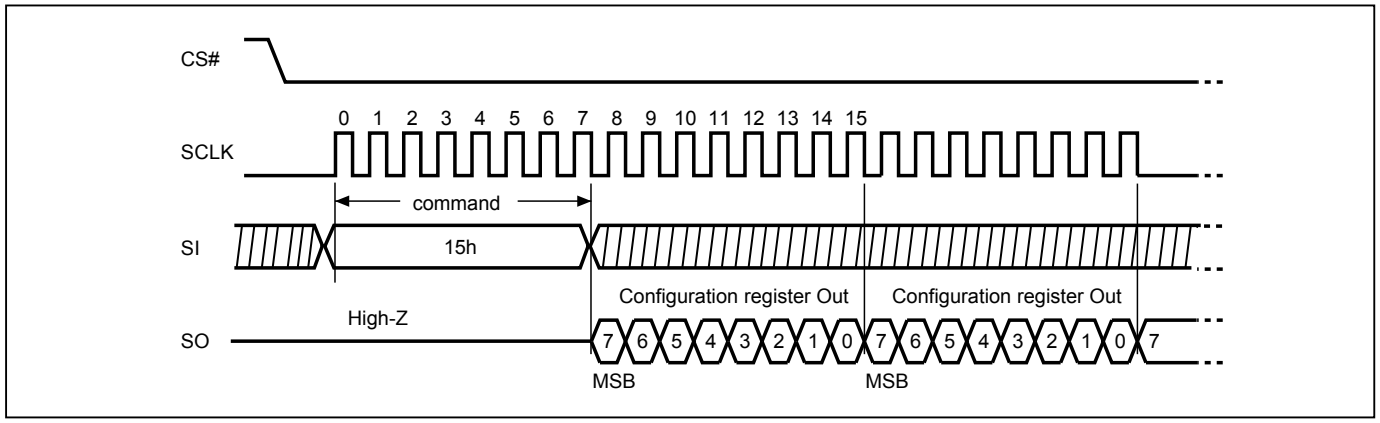


Figure 20. Read Configuration Register (RDCR) (STR-OPI Mode)

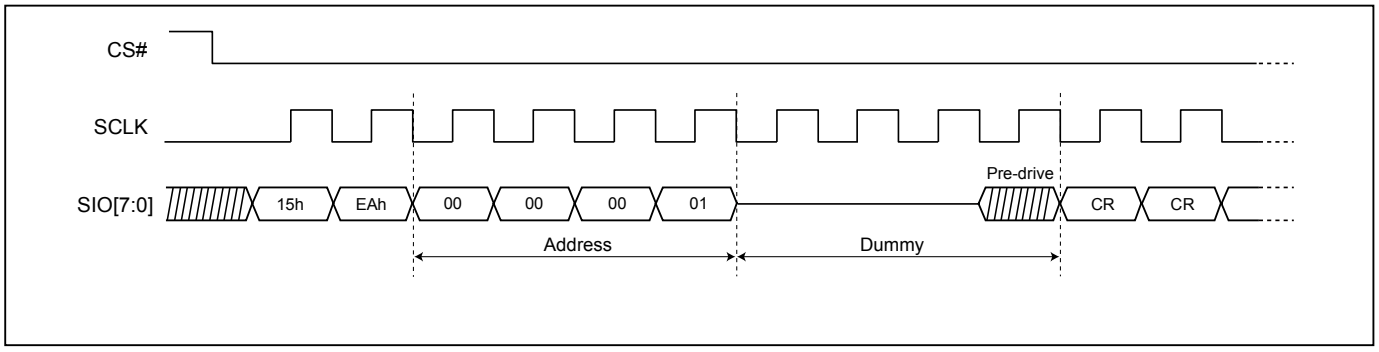
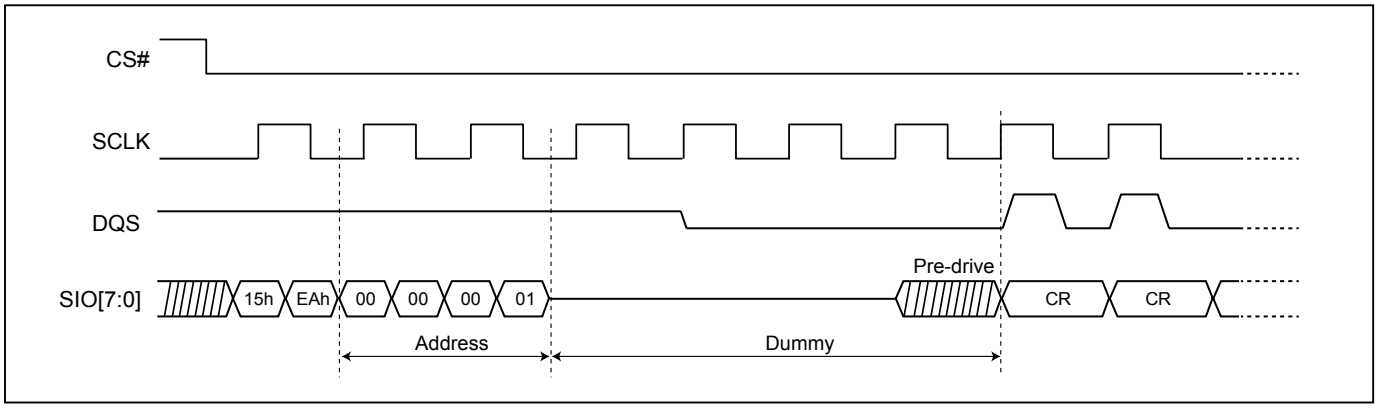


Figure 21. Read Configuration Register (RDCR) (DTR-OPI Mode)



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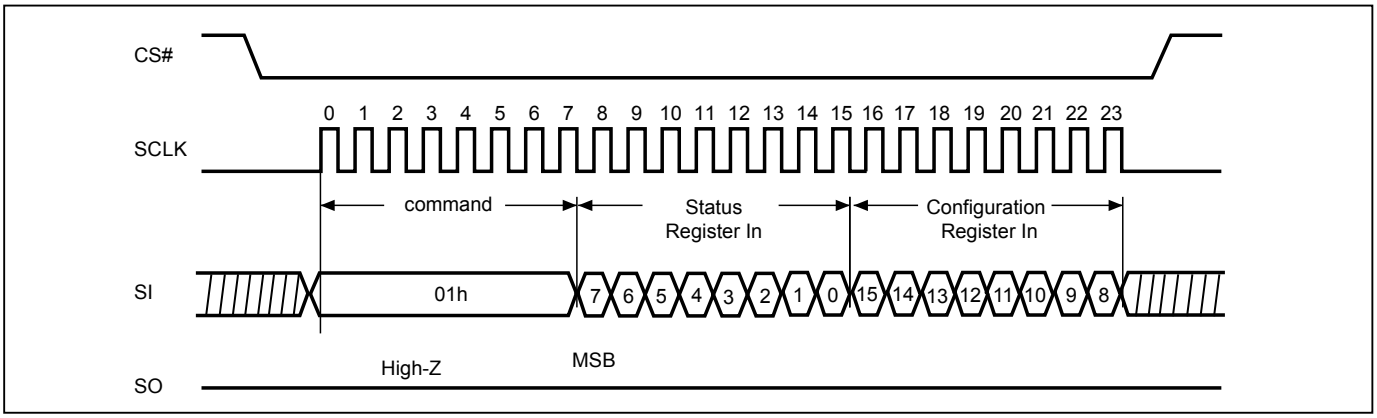
10-6. Write Status Register (WRSR) / Write Configuration Register (WRCR)

The WRSR instruction is for changing the values of Status Register Bits and Configuration Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in *"Table 4. Protected Area Sizes"*).

In SPI, CS# must go high exactly at the 8 bits or 16 bits data boundary; In DOPI, CS# must go high while clock is low; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

WRSR and WRCR instructions are not allowed while the device is operating in PE mode or Write Register Mode.

Figure 22. Write Status Register (WRSR) Sequence (SPI Mode)



Note : The CS# must go high exactly at 8 bits or 16 bits data boundary to completed the write register command.

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Figure 23. Write Status Register (WRSR) Sequence (STR-OPI Mode)

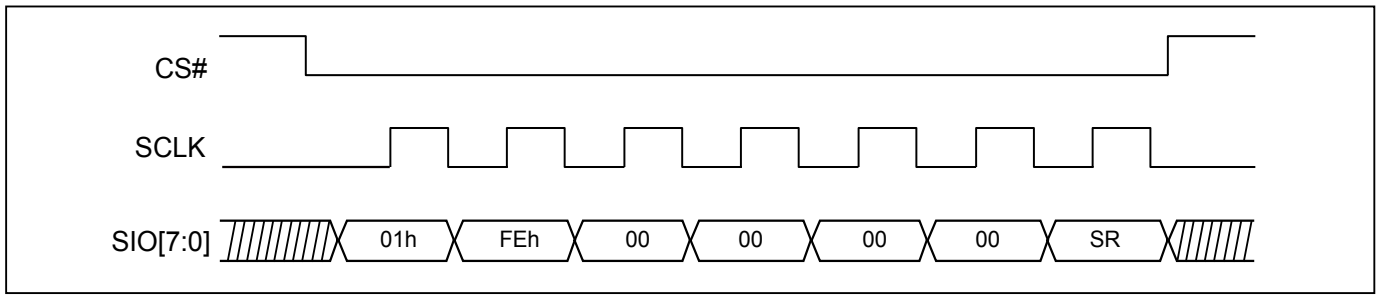
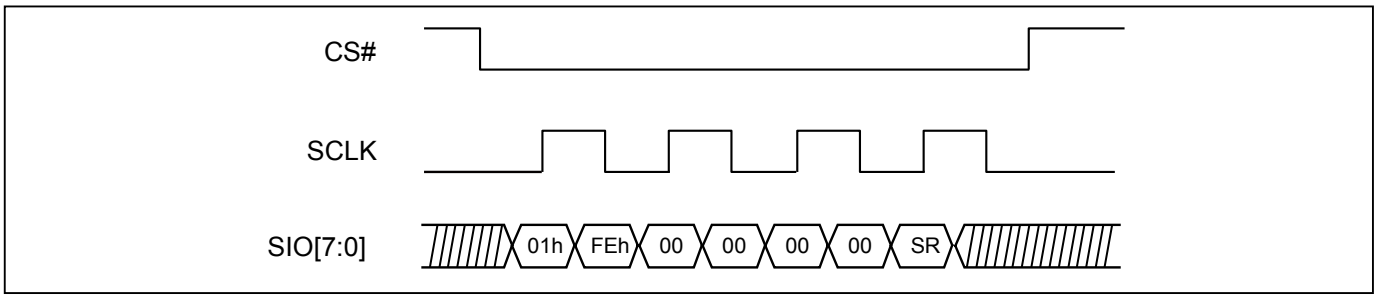


Figure 24. Write Status Register (WRSR) Sequence (DTR-OPI Mode)



Note: CS# must go high while SCLK is low.

Figure 25. Write Configuration Register (WRCR) Sequence (STR-OPI Mode)

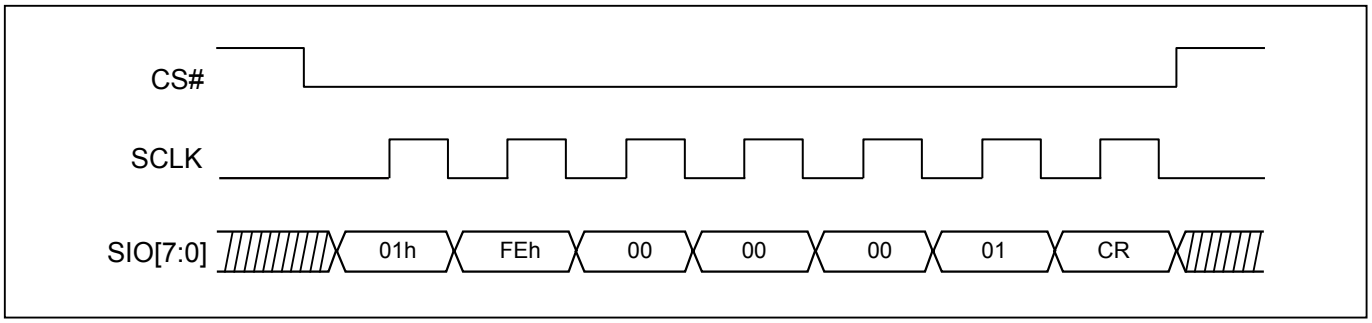
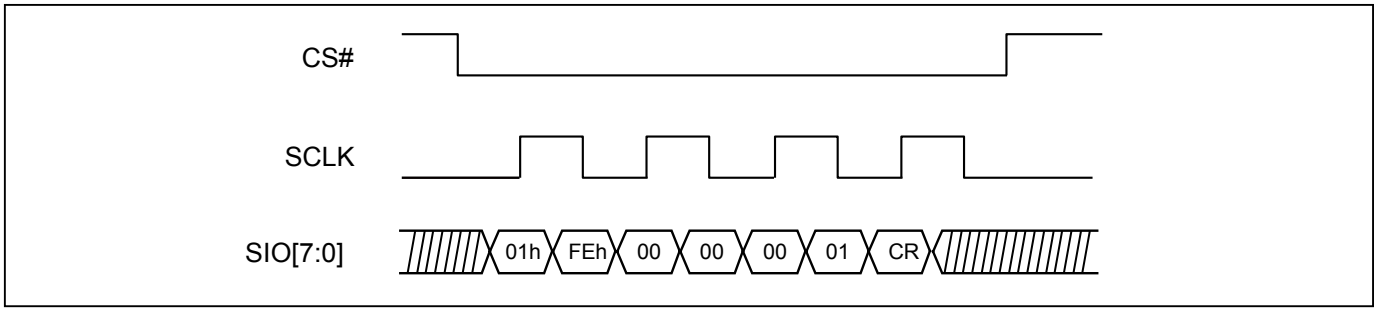


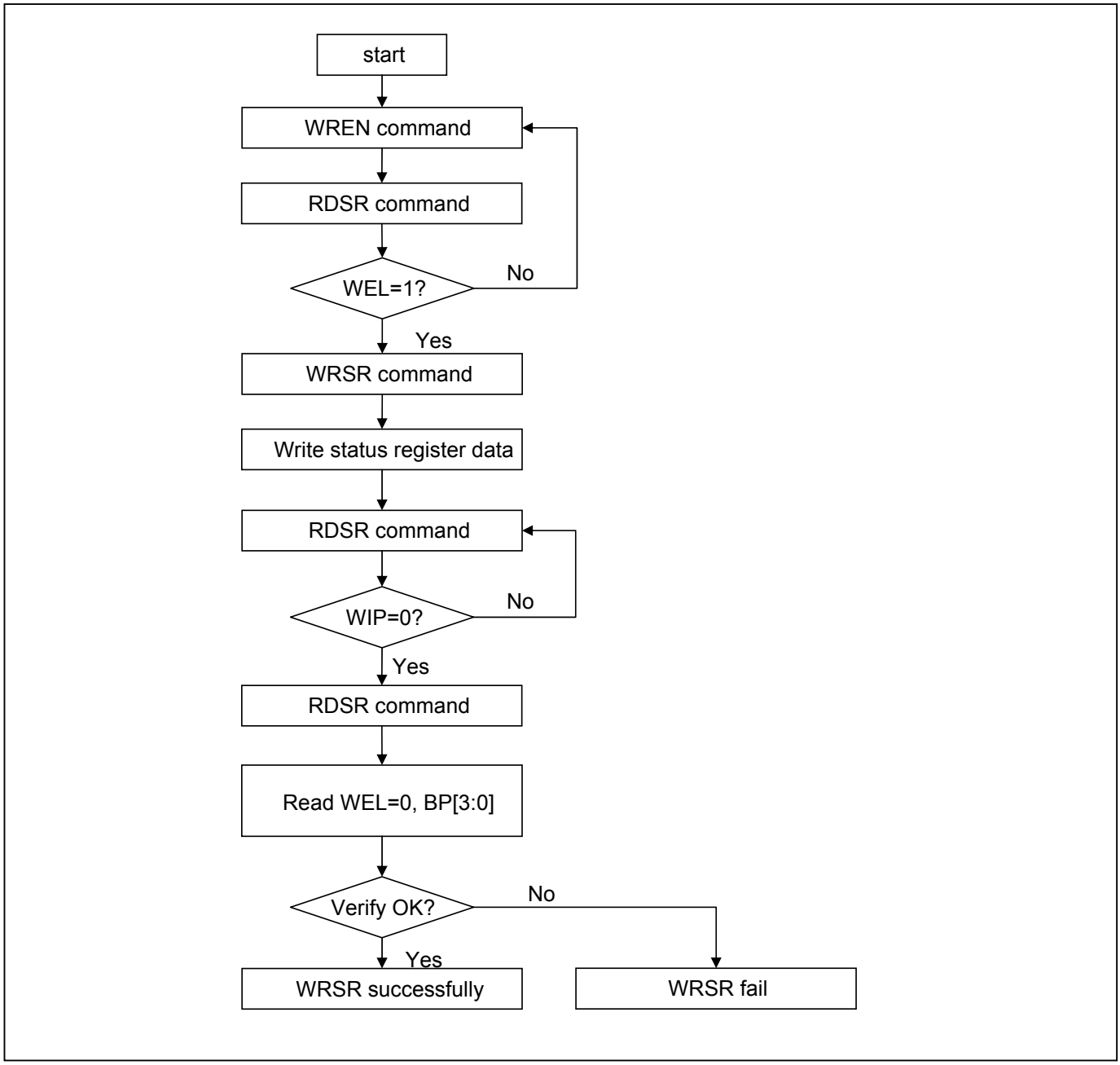
Figure 26. Write Configuration Register (WRCR) Sequence (DTR-OPI Mode)



Note: CS# must go high while SCLK is low.

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Figure 27. WRSR flow



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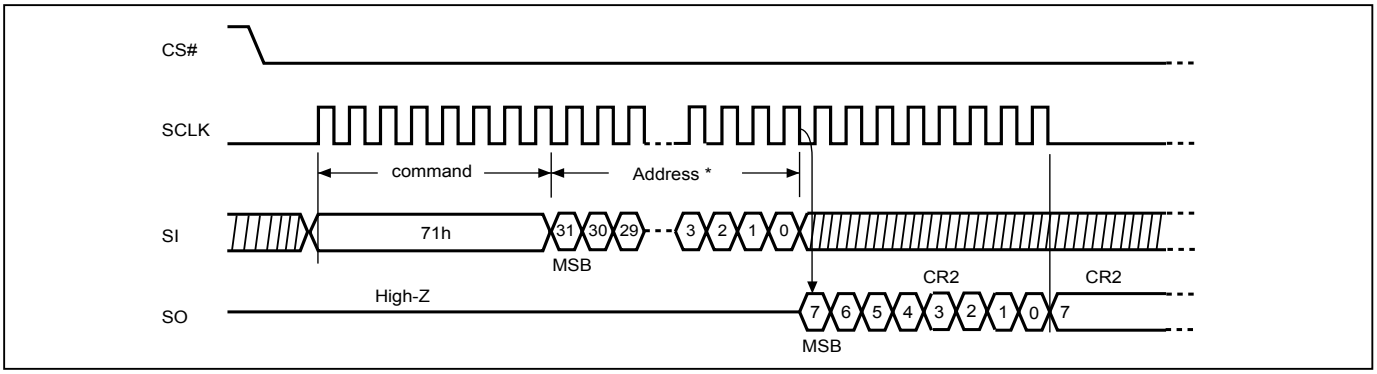
10-7. Read Configuration Register 2 (RDCR2)

The RDCR2 instruction is for reading Configuration Register 2.

The sequence of issuing RDCR2 instruction is: CS# goes low→ sending RDCR2 instruction code→ Sending 4 byte address → Configuration Register 2 data out on SO.

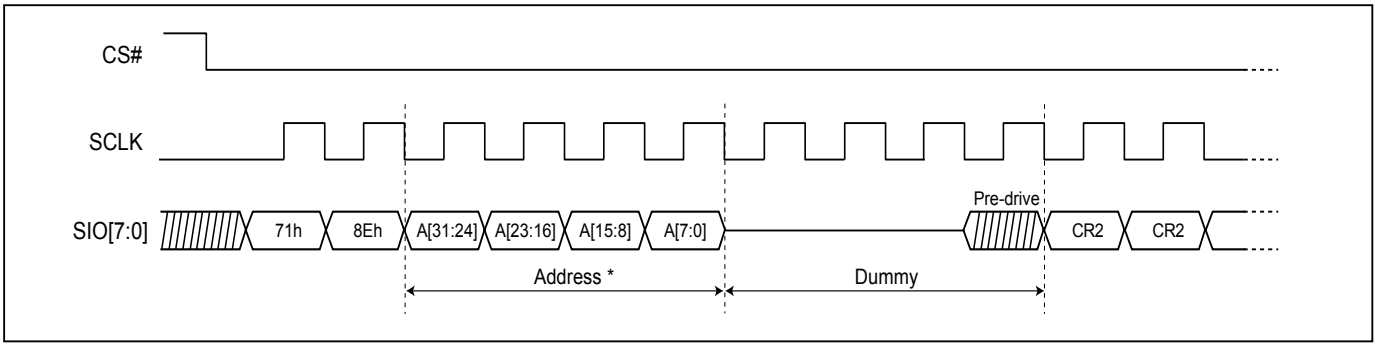
RDCR2 instruction is not allowed while the device is operating in PE Mode or Write Register Mode, except while accessing address 80000000h or Cx000000h.

Figure 28. Read Configuration Register 2 (RDCR2) Sequence (SPI Mode)



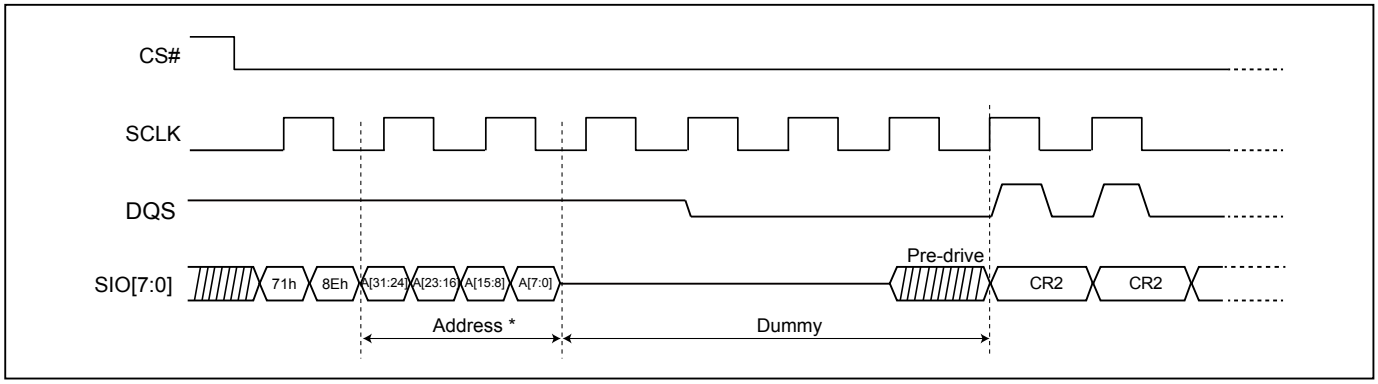
Note: * See *"9-3. Configuration Register 2"* for defining address .

Figure 29. Read Configuration Register 2 (RDCR2) Sequence (STR-OPI Mode)



Note: * See *"9-3. Configuration Register 2"* for defining address .

Figure 30. Read Configuration Register 2 (RDCR2) (DTR-OPI Mode)



Note: * See *"9-3. Configuration Register 2"* for defining address .

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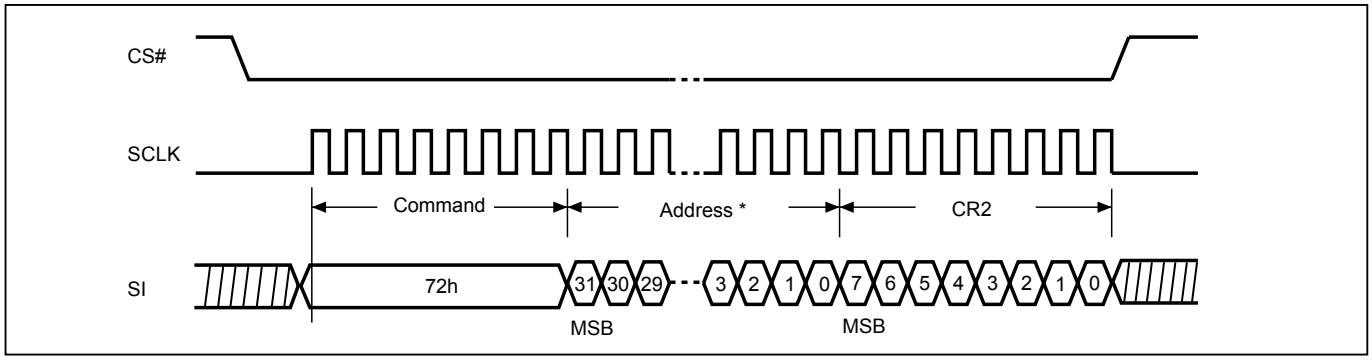
10-8. Write Configuration Register 2 (WRCR2)

The WRCR2 instruction is for changing the values of Configuration Register 2. Before sending WRCR2 instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance.

In SPI, CS# must go high exactly at the 8 bits data boundary; In DOPI, CS# must go high while clock is low; otherwise, the instruction will be rejected and not executed, and the Write Enable Latch (WEL) bit is reset.

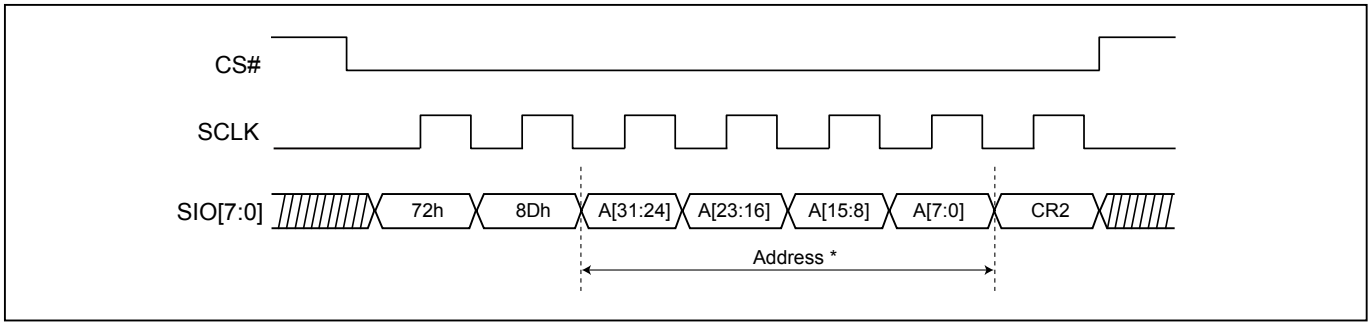
WRCR2 instruction is not allowed while the device is operating in PE Mode or Write Register Mode, except while accessing address 80000000h.

Figure 31. Write Configuration Register 2 (WRCR2) Sequence (SPI Mode)



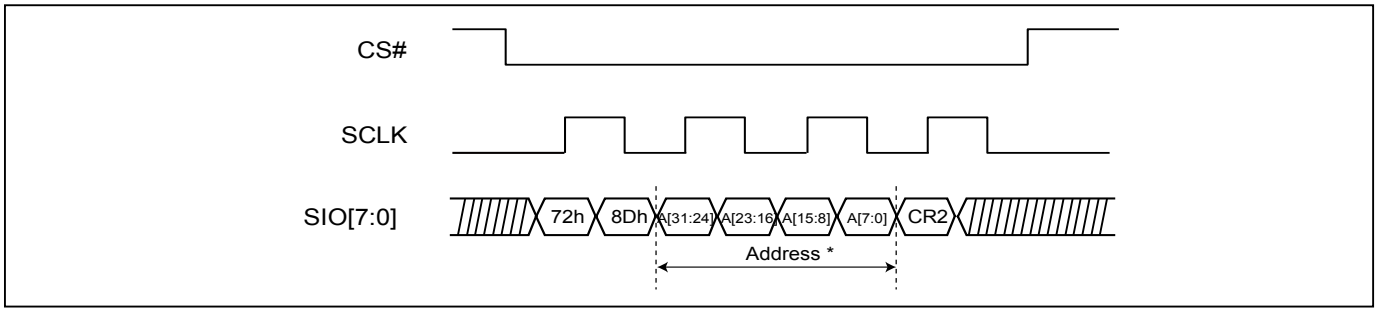
Note 1: * See *"9-3. Configuration Register 2"* for defining address .

Figure 32. Write Configuration Register 2 (WRCR2) Sequence (STR-OPI Mode)



Note 1: * See *"9-3. Configuration Register 2"* for defining address .

Figure 33. Write Configuration Register 2 (WRCR2) Sequence (DTR-OPI Mode)



Note 1 : * See *"9-3. Configuration Register 2"* for defining address.
Note 2 : CS# must go high while SCLK is low

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10-9. Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low→sending RDSCUR instruction→Security Register data out on SO→ CS# goes high.

Figure 34. Read Security Register (RDSCUR) Sequence (SPI Mode)

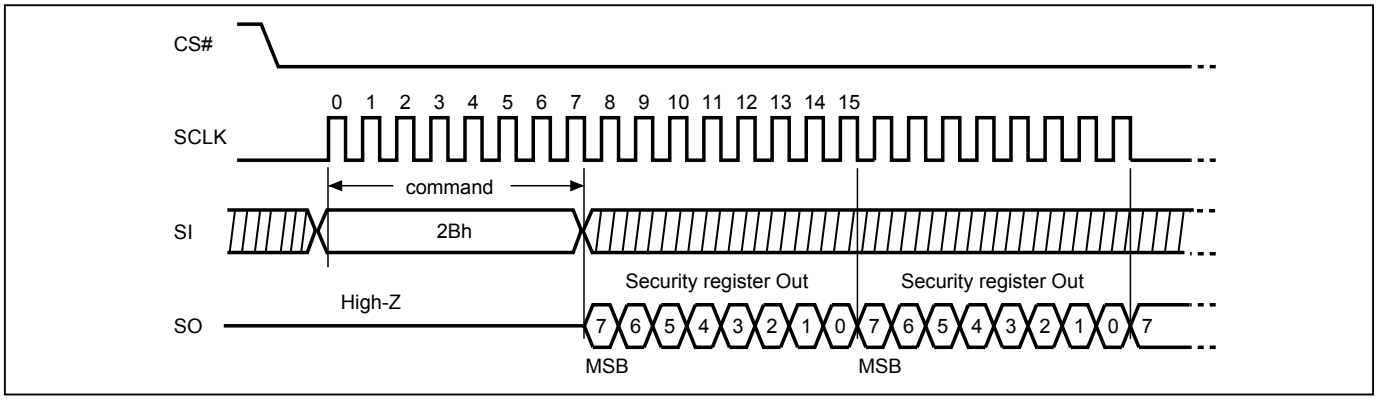


Figure 35. Read Security Register (RDSCUR) Sequence (STR-OPI Mode)

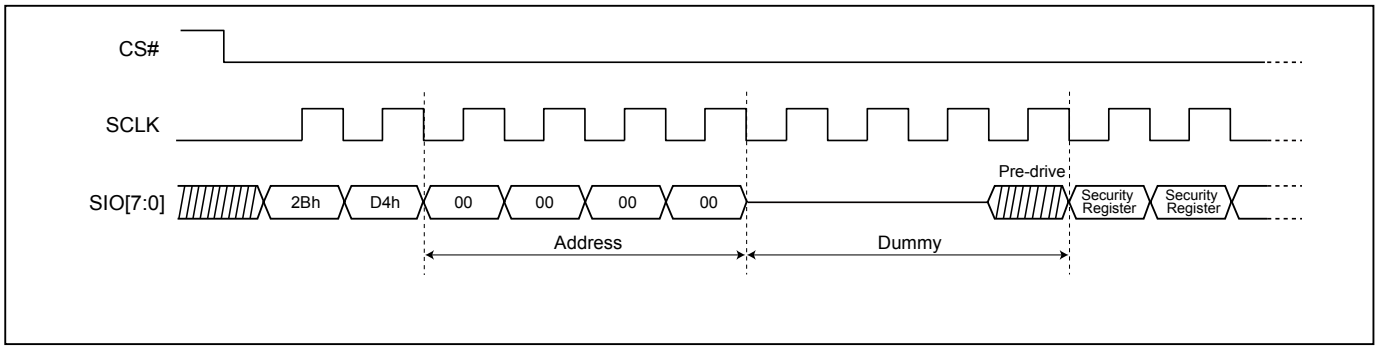
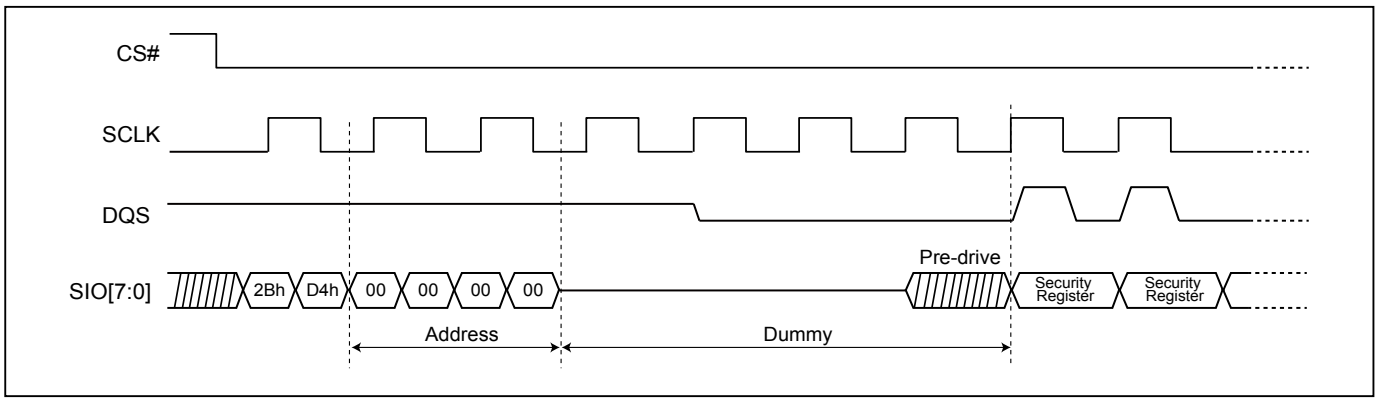


Figure 36. Read Security Register (RDSCUR) Sequence (DTR-OPI Mode)



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10-10. Write Security Register (WRSCUR)

The WRSCUR instruction sets the LDSO bit of the Security Register. The WREN (Write Enable) instruction is required before issuing WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 4K-bit customer usage area of Secured OTP. Once the LDSO bit is set to "1", the customer usage area of Secured OTP cannot be updated any more.

The sequence of issuing WRSCUR instruction is :CS# goes low→ sending WRSCUR instruction → CS# goes high.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

WRSCUR instruction is not allowed while the device is operating in PE mode or Write Register Mode.

Figure 37. Write Security Register (WRSCUR) Sequence (SPI Mode)

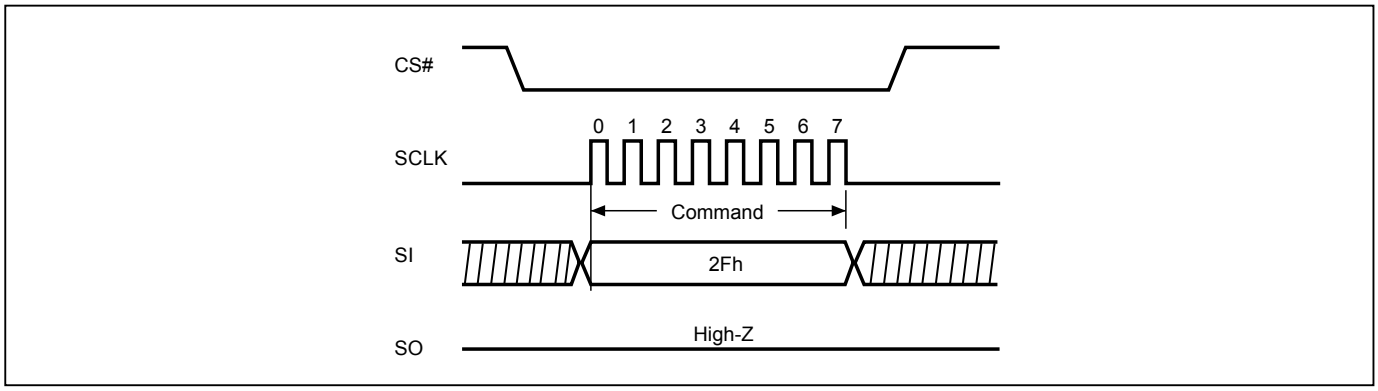


Figure 38. Write Security Register (WRSCUR) Sequence (STR-OPI Mode)

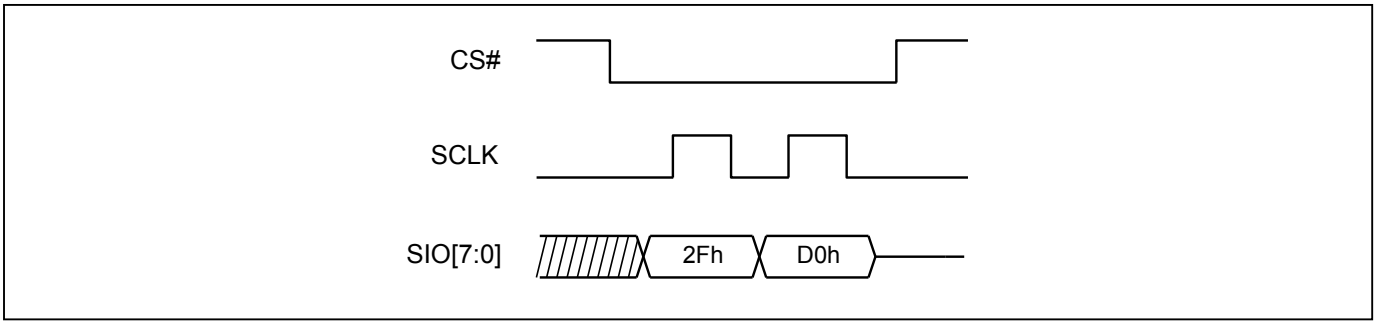
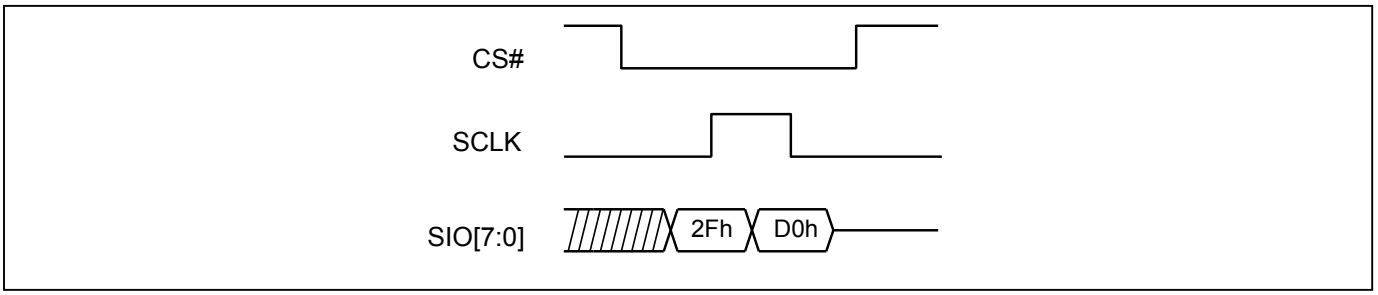


Figure 39. Write Security Register (WRSCUR) Sequence (DTR-OPI Mode)



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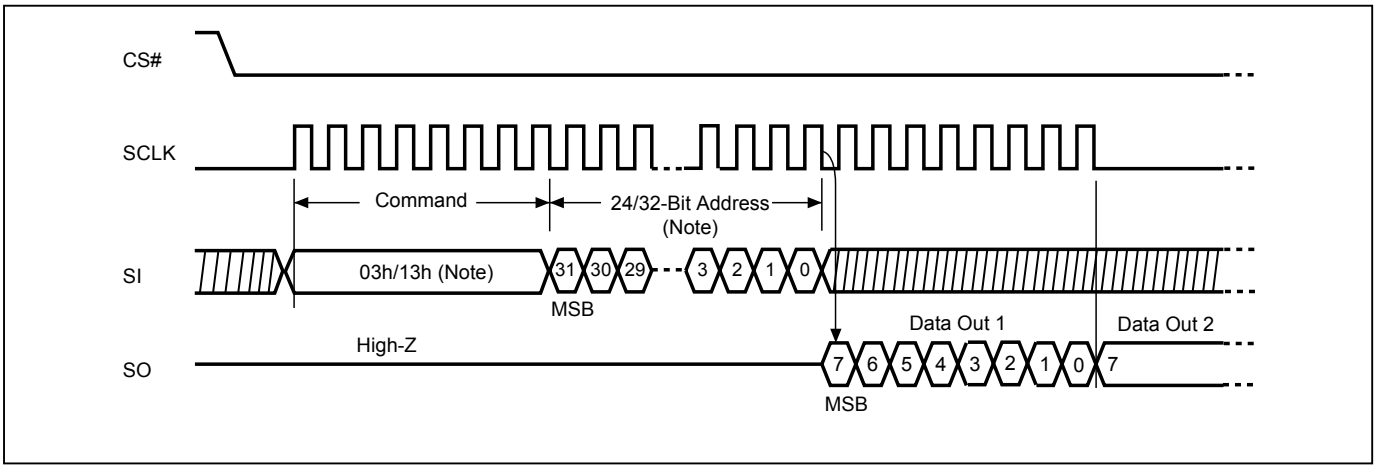
10-11. Read Data Bytes (READ/READ3B/READ4B)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ/READ3B/READ4B instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ/READ3B/READ4B instruction is: CS# goes low→sending READ/READ3B/READ4B instruction code→ 3-byte or 4-byte address on SI→ data out on SO→to end READ/READ3B/READ4B operation can use CS# to high at any time during data out.

In the bank which is being operated programming , erasing or Write Register Mode, read operation can not be executed and any read command will be ignored.

Figure 40. Read Data Bytes (READ/READ3B/READ4B) Sequence (SPI Mode only)



Note: The number of address cycles are based on different address mode. In 3-Byte command operation, it is 24-bit. In 4-Byte command operation, it is 32-bit.

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10-12. Read Data Bytes at Higher Speed (FAST_READ/FAST_READ3B/FAST_READ4B)

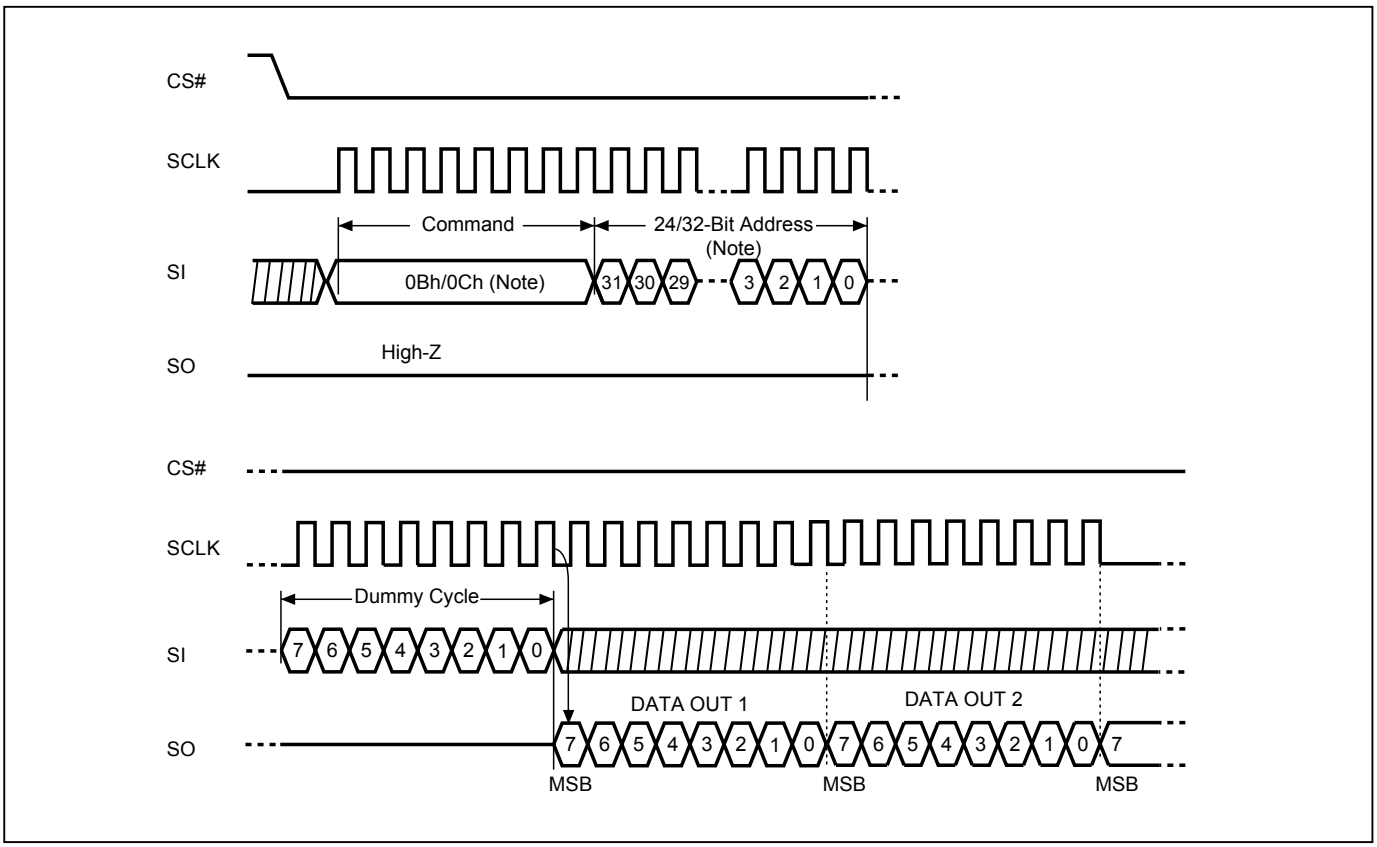
The FAST_READ/FAST_READ3B/FAST_READ4B instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ/FAST_READ3B/FAST_READ4B instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ/FAST_READ3B/FAST_READ4B instruction is: CS# goes low→ sending FAST_READ/FAST_READ3B/FAST_READ4B instruction code→ 3-byte or 4-byte address on SI→ 8 dummy cycles → data out on SO→ to end FAST_READ/FAST_READ3B/FAST_READ4B operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ/FAST_READ3B/FAST_READ4B instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

In the bank which is being operated programming , erasing or Write Register Mode, read operation can not be executed and any read command will be ignored.

Figure 41. Read at Higher Speed (FAST_READ/FAST_READ3B/FAST_READ4B) Sequence (SPI Mode only)



Note: The number of address cycles are based on different address mode. In 3-Byte command operation, it is 24-bit. In 4-Byte command operation, it is 32-bit.

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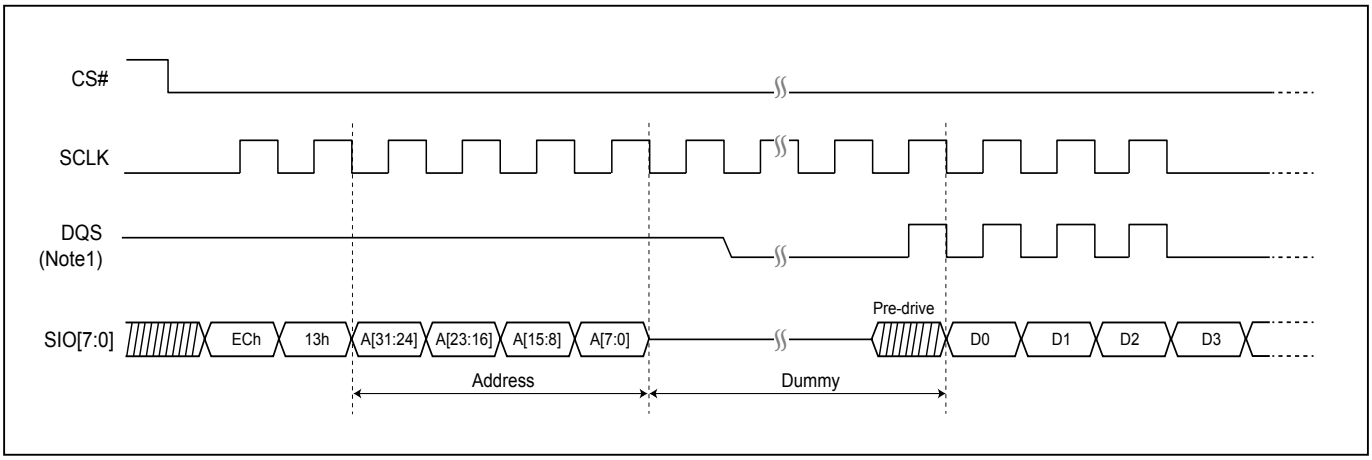
10-13. OCTA Read Mode (8READ)

The 8READ instruction enable Octa throughput of Serial NOR Flash in read mode. An OPI Enable bit of Configuration Register 2 must be set to "1" before sending the STR Octa READ instruction.

While Program/Erase/Write Status Register cycle is in progress, 8READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

In the bank which is being operated programming, erasing or Write Register Mode, read operation can not be executed and any read command will be ignored.

Figure 42. OCTA Read Mode Sequence (STR-OPI Mode)



Note1: DQS is enabled only when DOS (DQS on STR mode) bit is set. Otherwise, it keeps Hi-Z.

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10-14. OCTA DTR Read Mode (8DTRD)

The 8DTRD instruction enable DTR Octa throughput of Serial NOR Flash in read mode. An DOPI Enable bit of Configuration Register 2 must be set to "1" before sending the DTR Octa READ instruction.

While Program/Erase/Write Status Register cycle is in progress, 8DTRD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

In DTR Octa READ mode, the starting address must be even byte (A0=0).

In the bank which is being operated programming, erasing or Write Register Mode, read operation can not be executed and any read command will be ignored.

Figure 43. OCTA Read Mode Sequence (DTR-OPI Mode)

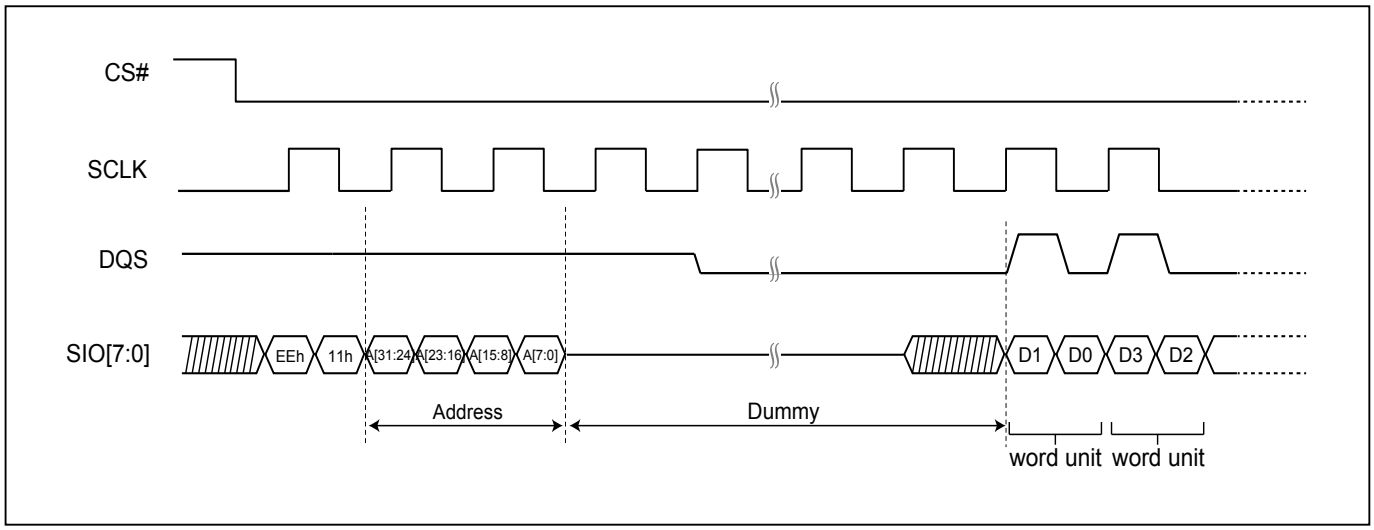
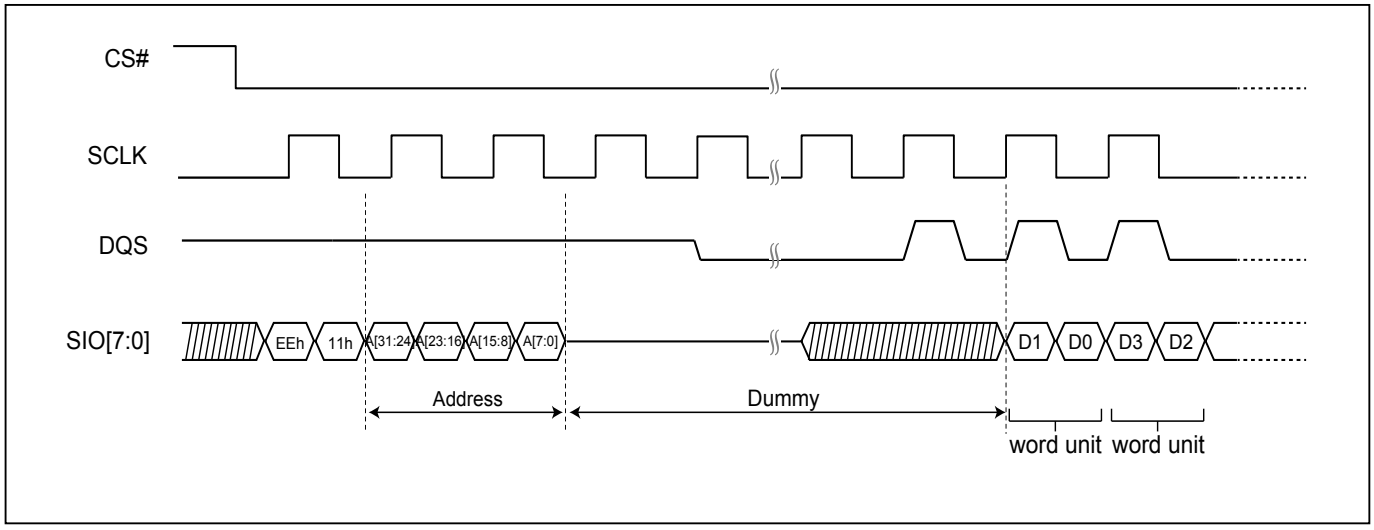


Figure 44. OCTA Read Mode Sequence (DTR-OPI Mode) with DQS pre-cycle enabled (CR2 DQSPRC=1)



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10-15. Preamble Bit

The Preamble Bit data pattern supports system/memory controller to determine the valid windows of data output more easily and improve data capture reliability while the flash memory is running in high frequency.

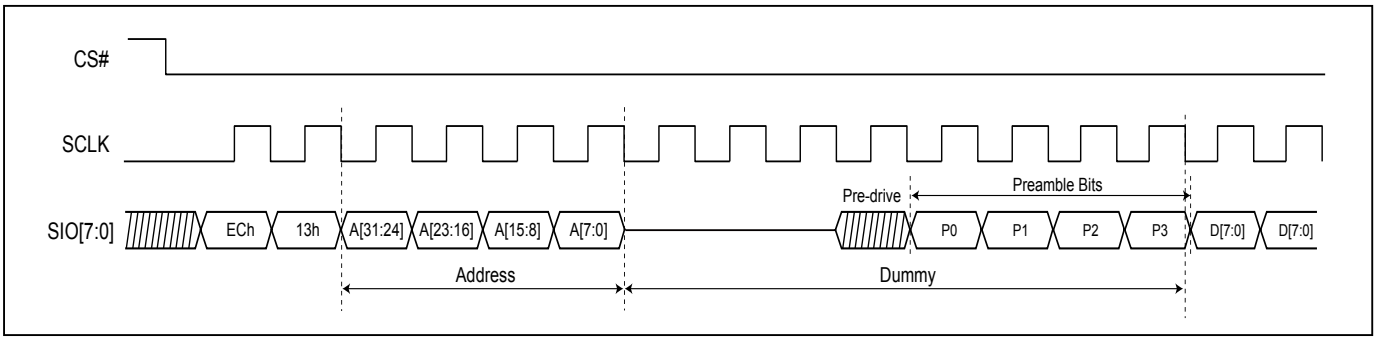
The preamble bit is designed as a 16-bit data pattern, which can be enabled or disabled by setting the bit4 of Configuration register (Preamble bit Enable bit). Once CR<4> is set, the preamble bit is inputted into dummy cycles. Two different patterns are selectable by setting CR<2> PSB (Pattern Select Bit), and please refer to *"9-3. Configuration Register 2"* for details.

Once Preamble Bit feature is enabled, the preamble bit pattern will be output after a pre-driven signal. When the device is under OPI mode, all SIO pins except SIO3 will output the same learning pattern. The signal on SIO3 will be different from other I/O pins in case PSB=0.

In OPI, when dummy cycle number reaches 20, the complete 16 bits will start to output right after the pre-driven signal. When dummy cycle number is not sufficient of 16 cycles, the rest of the preamble bits will be cut off.

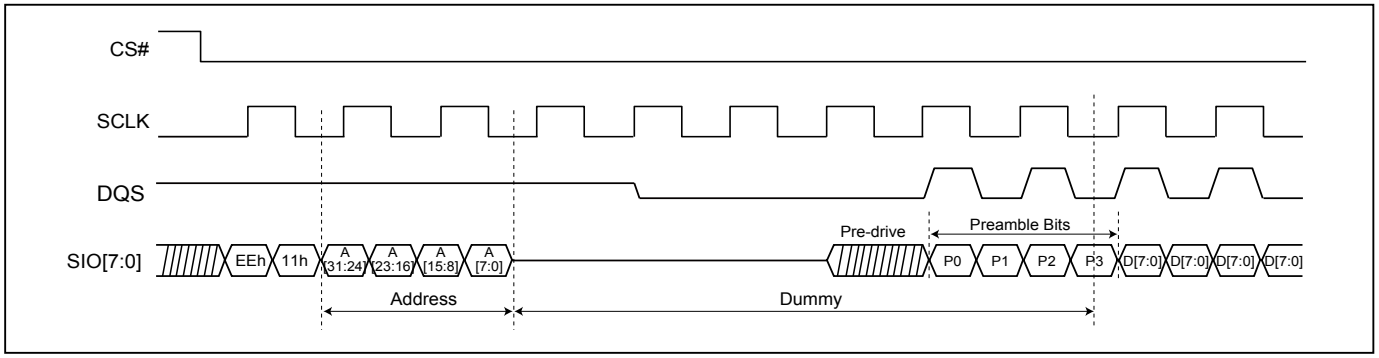
In DOPI, when dummy cycles number reaches 12, the complete 16 bits will start to output right after the pre-driven signal.

Figure 45. Preamble Bit data pattern Output Sequence (STR-OPI Mode)



Note: 8 dummy cycle example.

Figure 46. Preamble Bit data pattern Output Sequence (DTR-OPI Mode)



Note: 6 dummy cycle example.

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10-16. Burst Read

To set the Burst length, following command operation is required to issue command: “C0h” in the first Byte, following clock defining wrap around register value.

Their definitions are as the following table:

Data	Wrap Around	Wrap Depth
00h	Reserved	Reserved
01h	Yes	16-byte
02h	Yes	32-byte
03h	Yes	64-byte
1xh	No	X

The wrap around unit is defined with the 16/32/64Byte, with random initial address. It is defined as “wrap-around mode disable” for the default state of the device. To exit wrap around, it is required to issue another “C0h” command in which data=‘1xh”. Otherwise, wrap around status will be retained until power down or reset command. To change wrap around depth, it is requried to issue another “C0h” command in which data=“0xh”. Burst read is supported only in OPI/DOPI mode after wrap around is enable. The default state after device power-up or reset is determined by settings in NV-CR2 registers.

Figure 47. Set Burst Length (SPI Mode)

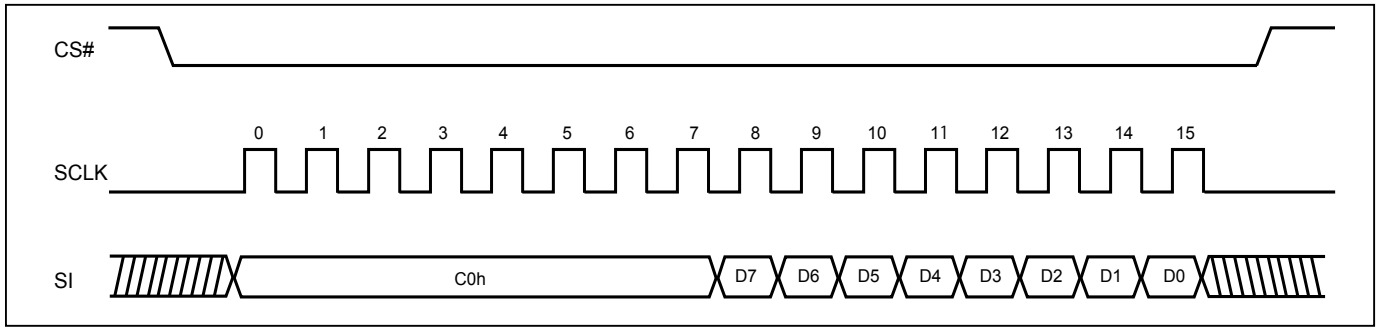
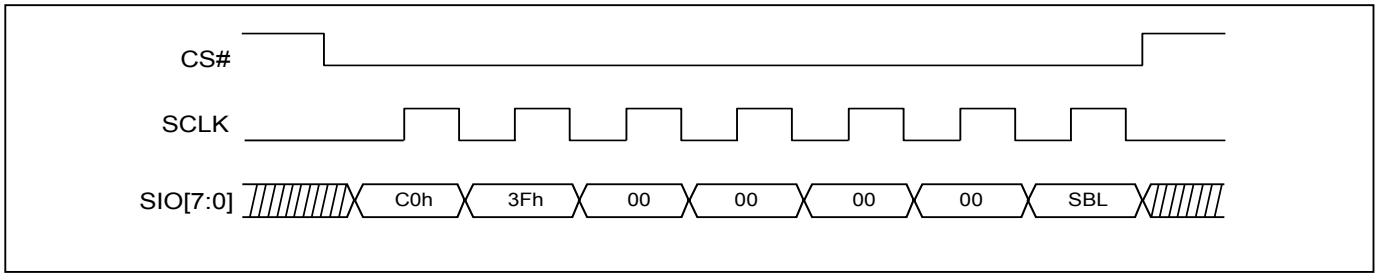


Figure 48. Set Burst Length (STR-OPI Mode)



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10-17. Fast Boot

The Fast Boot Feature provides the ability to automatically execute read operation after power on cycle or reset without any read instruction.

A Fast Boot Register is provided on this device. It can enable the Fast Boot function and also define the number of delay cycles and start address (where boot code being transferred). Instruction WRFBR (write fast boot register) and ESFBR (erase fast boot register) can be used for the status configuration or alternation of the Fast Boot Register bit. RDFBR (read fast boot register) can be used to verify the program state of the Fast Boot Register. The default number of delay cycles is 21 cycles in OPI/DOPI; while the number of delay cycles is 13 in SPI and there is a 16bytes boundary address for the start of boot code access.

When CS# starts to go low, data begins to output from default address after the delay cycles. After CS# returns to go high, the device will go back to standard SPI/OPI/DOPI mode and user can start to input command. In the fast boot data out process from CS# goes low to CS# goes high, a minimum of one byte must be output.

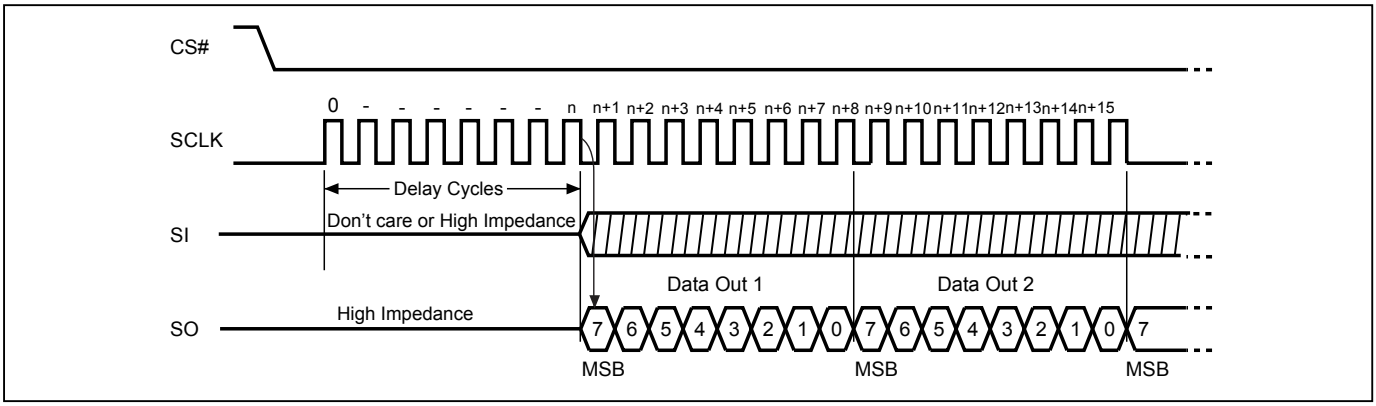
Once Fast Boot feature has been enabled, the device will automatically start a read operation after power on cycle, reset command, or hardware reset operation. Beside Fast Boot Register, the following bits inside NV-CR2 also affects Fast Boot Read behavior: CRCEN#, DOPI#, SOPI#, ODS, DOS, DQSPRC, ECS, CRCCYC, CRCBEN.

RDFBR, WRFBR and ESFBR instructions are not allowed while the device is operating in PE mode or Write Register Mode.

Fast Boot Register (FBR)

Bits	Description	Bit Status	Default State	Type
31 to 4	FBSA (FastBoot Start Address)	16 bytes boundary address for the start of boot code access.	FFFFFFF	Non-Volatile
3	Reserved		1	Non-Volatile
2 to 1	FBSD (FastBoot Start Delay Cycle)	00: 11 delay cycles 01: 15 delay cycles 10: 17 delay cycles 11: 21 delay cycles	11	Non-Volatile
0	FBE (FastBoot Enable)	0=FastBoot is enabled. 1=FastBoot is not enabled.	1	Non-Volatile

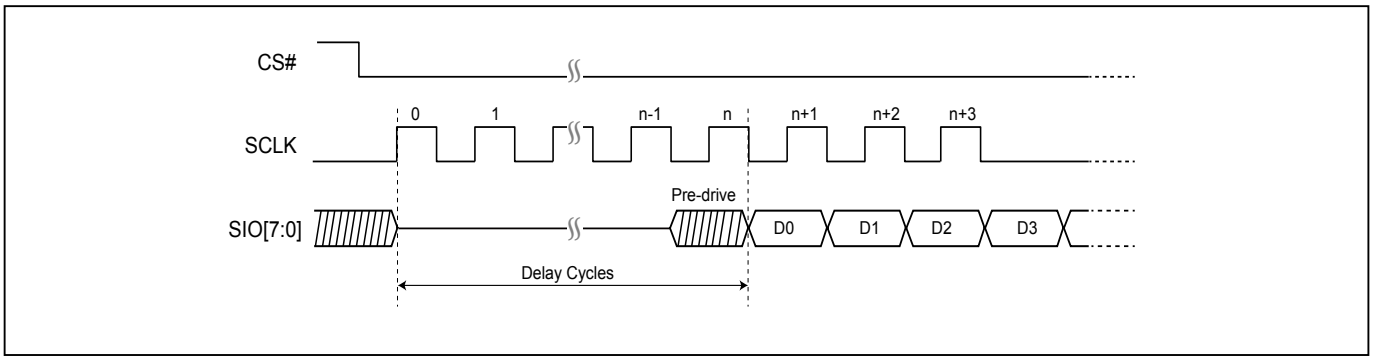
Figure 49. Fast Boot Sequence (SPI Mode)



Note: The delay cycle is always 13 in SPI mode.

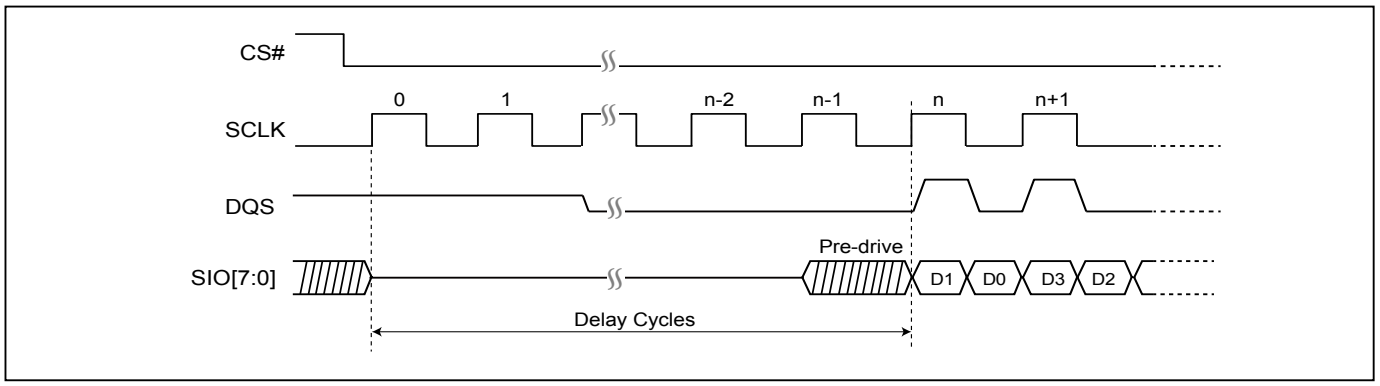
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Figure 50. Fast Boot Sequence (STR-OPI Mode)



Note: If FBSD = 11, delay cycles is 21 and n is 20.
If FBSD = 10, delay cycles is 17 and n is 16.
If FBSD = 01, delay cycles is 15 and n is 14.
If FBSD = 00, delay cycles is 11 and n is 10.

Figure 51. Fast Boot Sequence (DTR-OPI Mode)



Note: If FBSD = 11, delay cycles is 21 and n is 21.
If FBSD = 10, delay cycles is 17 and n is 17.
If FBSD = 01, delay cycles is 15 and n is 15.
If FBSD = 00, delay cycles is 11 and n is 11.

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Figure 52. Read Fast Boot Register (RDFBR) Sequence

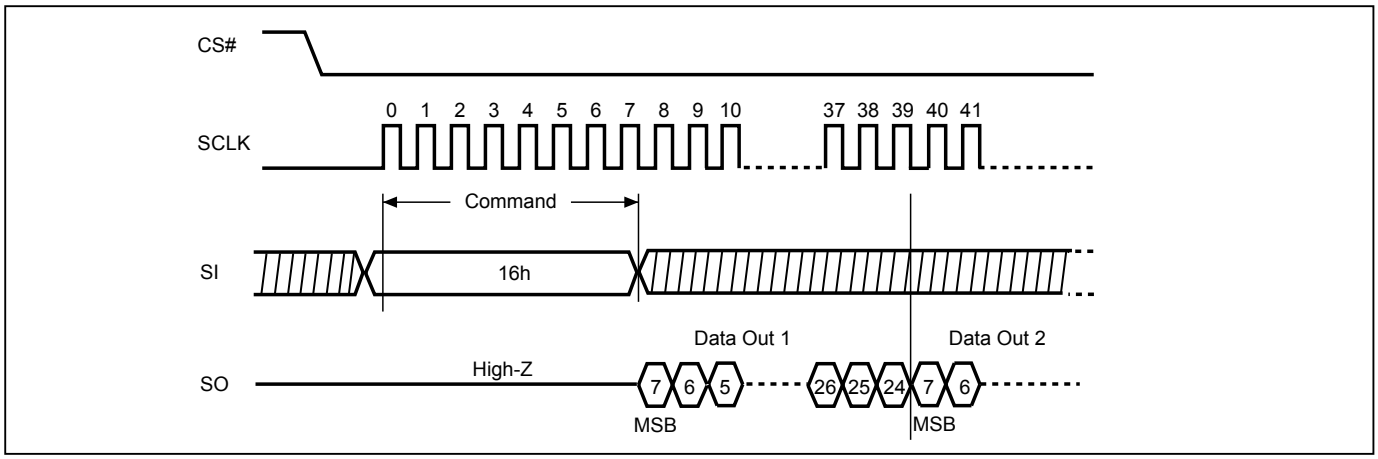


Figure 53. Read Fast Boot Register (RDFBR) Sequence (STR-OPI Mode)

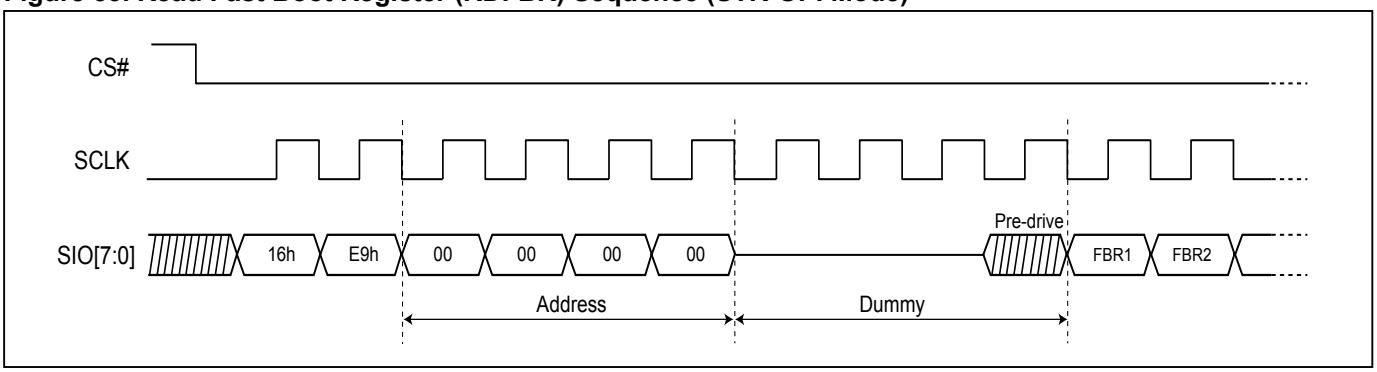
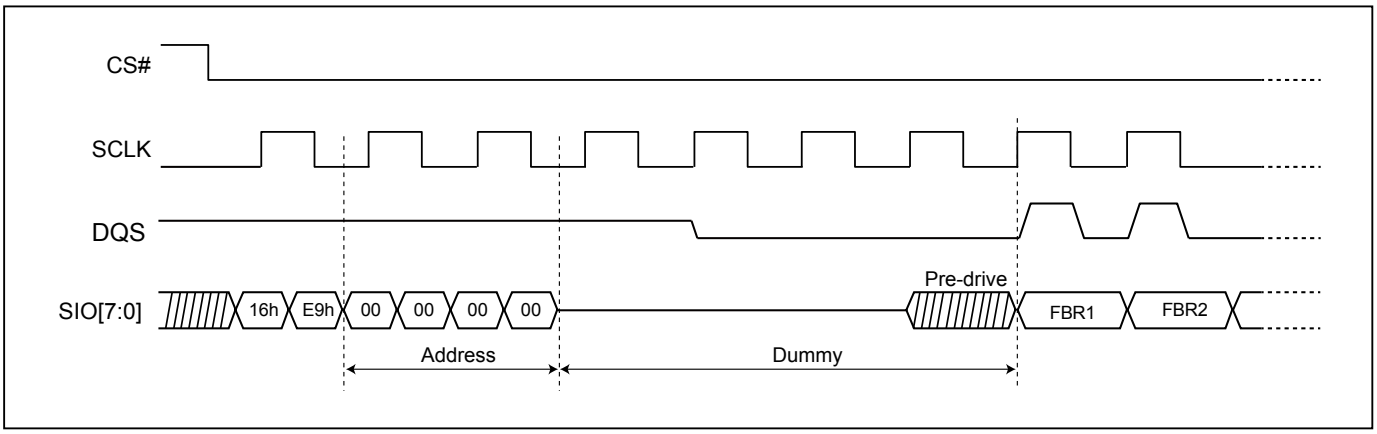


Figure 54. Read Fast Boot Register (RDFBR) Sequence (DTR-OPI Mode)



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Figure 55. Write Fast Boot Register (WRFBR) Sequence

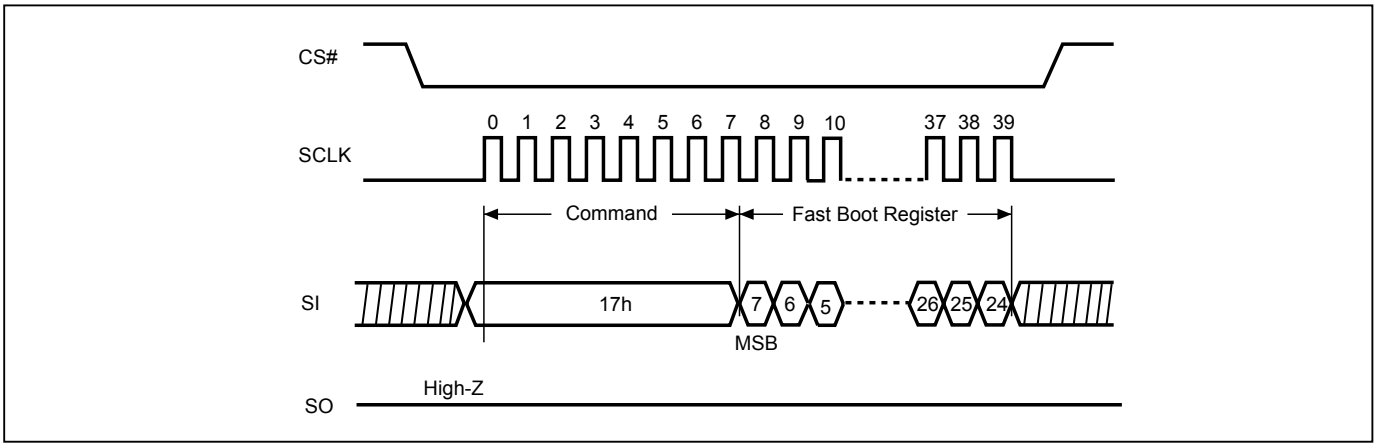


Figure 56. Write Fast Boot Register (WRFBR) Sequence (STR-OPI Mode)

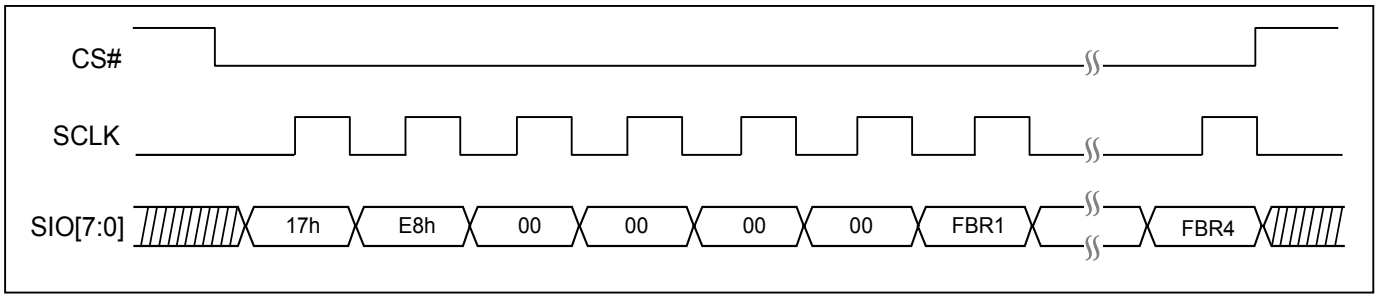
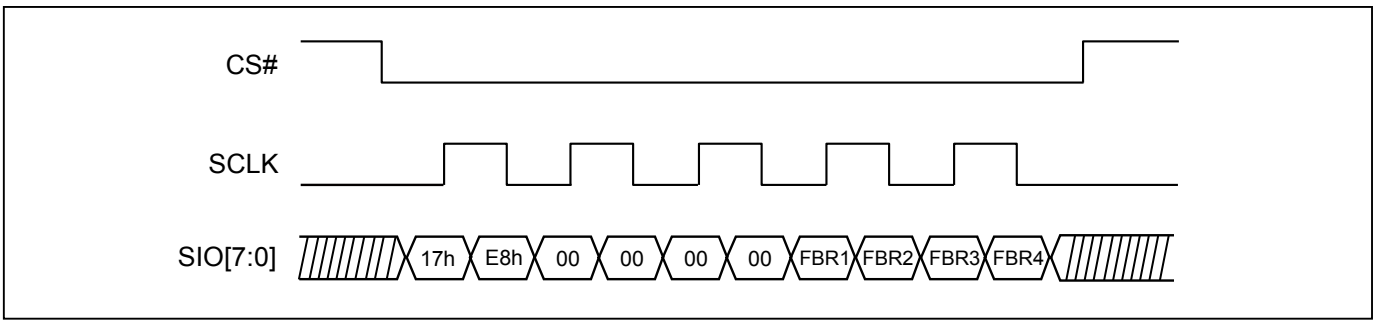


Figure 57. Write Fast Boot Register (WRFBR) Sequence (DTR-OPI Mode)



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Figure 58. Erase Fast Boot Register (ESFBR) Sequence

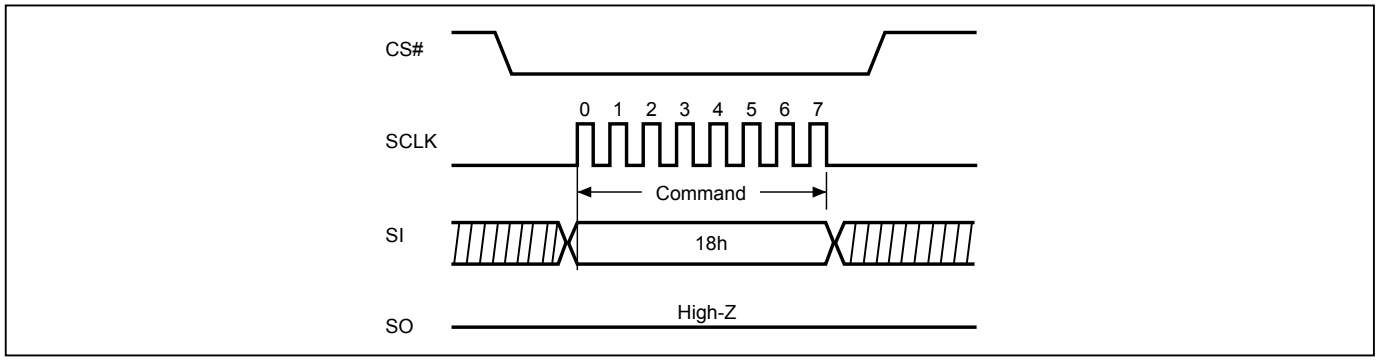


Figure 59. Erase Fast Boot Register (ESFBR) Sequence (STR-OPI Mode)

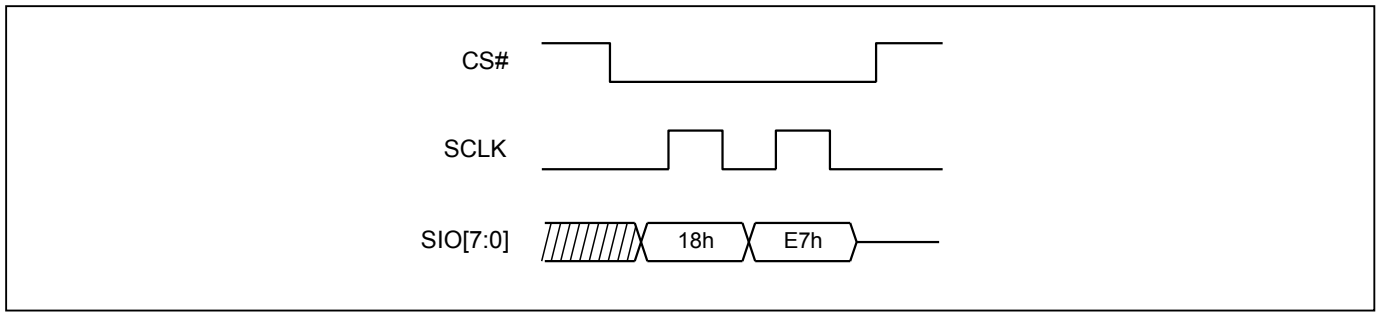
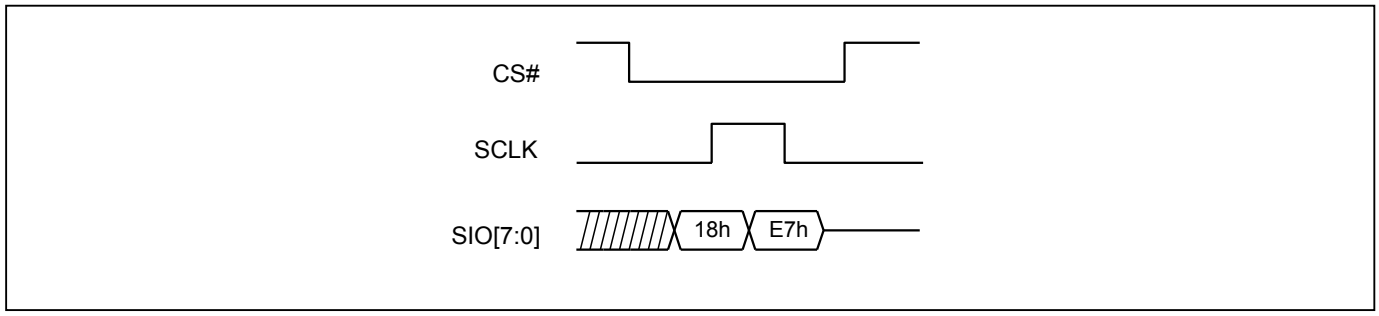


Figure 60. Erase Fast Boot Register (ESFBR) Sequence (DTR-OPI Mode)



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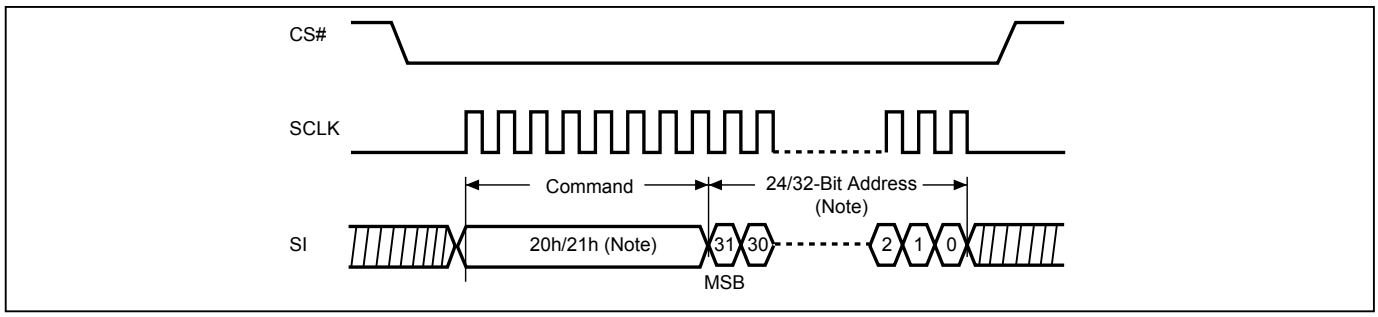
10-18. Sector Erase (SE/SE3B/SE4B)

The Sector Erase (SE/SE3B/SE4B) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE/SE3B/SE4B). Any address of the sector (Please refer to *"5. MEMORY ORGANIZATION"*) is a valid address for Sector Erase (SE/SE3B/SE4B) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of the address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing SE/SE3B/SE4B instruction is: CS# goes low→ sending SE/SE3B/SE4B instruction code→ 3-byte or 4-byte address → CS# goes high.

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and clears when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the Block is protected by BP bits (Block Protect Mode), the Sector Erase (SE/SE3B/SE4B) instruction will not be executed on the block.

Figure 61. Sector Erase (SE/SE3B/SE4B) Sequence (SPI Mode)



Note: The number of address cycles are based on different address mode. In 3-Byte command operation, it is 24-bit. In 4-Byte command operation, it is 32-bit.

Figure 62. Sector Erase (SE) Sequence (STR-OPI Mode)

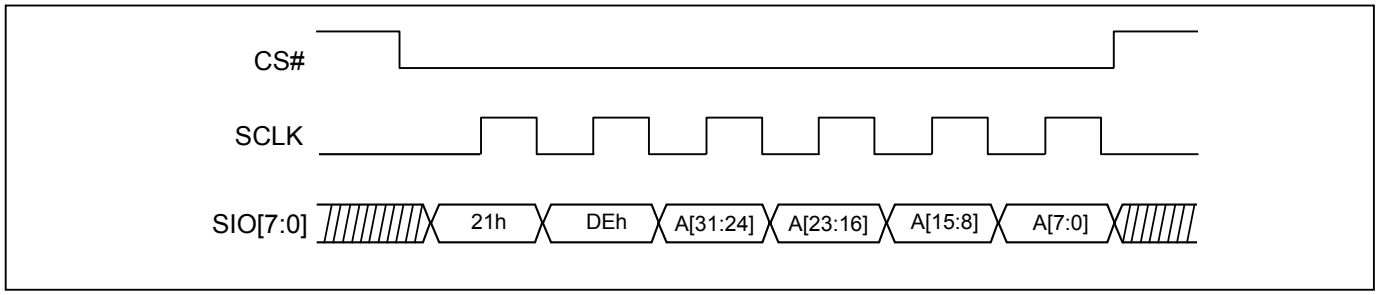
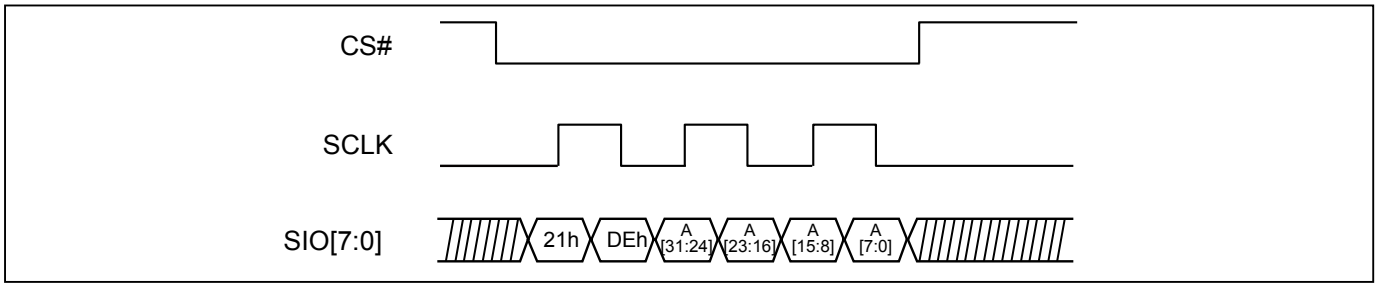


Figure 63. Sector Erase (SE) Sequence (DTR-OPI Mode)



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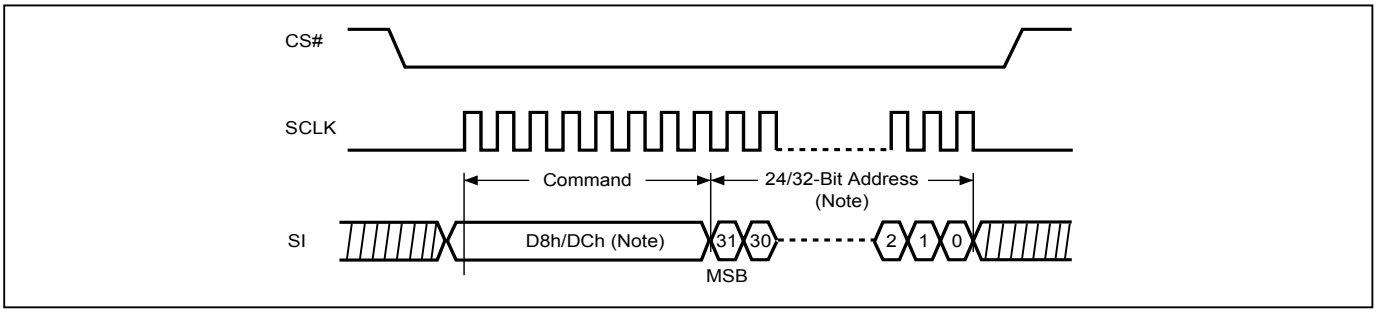
10-19. Block Erase (BE/BE3B/BE4B)

The Block Erase (BE/BE3B/BE4B) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE/BE3B/BE4B). Any address of the block (Please refer to *"5. MEMORY ORGANIZATION"*) is a valid address for Block Erase (BE/BE3B/BE4B) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE/BE3B/BE4B instruction is: CS# goes low→ sending BE/BE3B/BE4B instruction code→ 3-byte or 4-byte address → CS# goes high.

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the Block is protected by BP bits (Block Protect Mode), the Block Erase (BE/BE3B/BE4B) instruction will not be executed on the block.

Figure 64. Block Erase (BE/BE3B/BE4B) Sequence (SPI Mode)



Note: The number of address cycles are based on different address mode. In 3-Byte command operation, it is 24-bit. In 4-Byte command operation, it is 32-bit.

Figure 65. Block Erase (BE) Sequence (STR-OPI Mode)

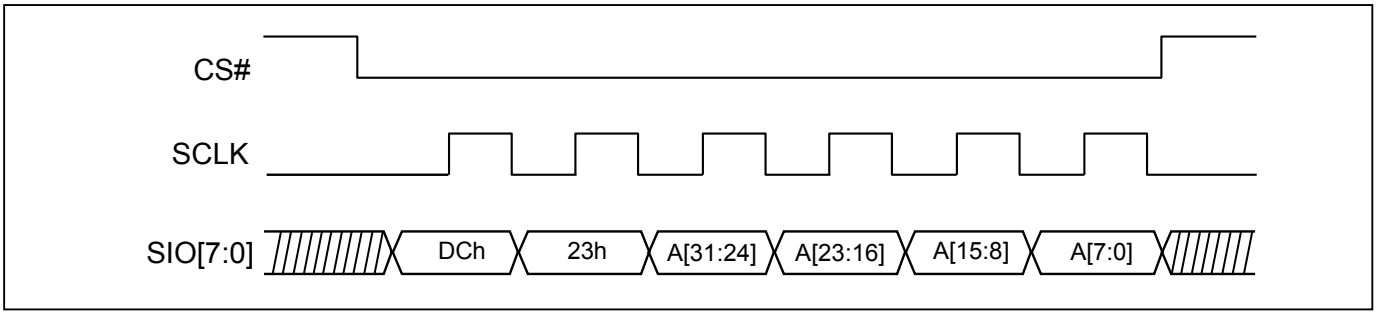
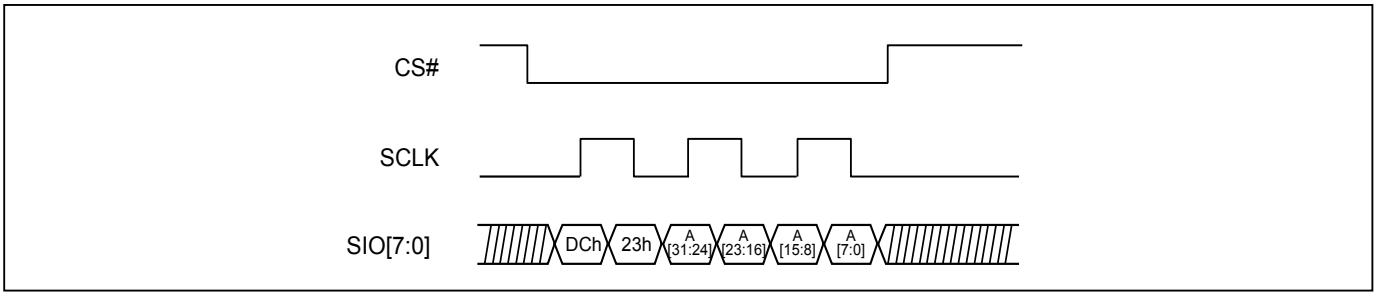


Figure 66. Block Erase (BE) Sequence (DTR-OPI Mode)



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10-20. Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→sending CE instruction code→CS# goes high.

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Chip Erase cycle is in progress. The WIP sets during the tCE timing, and clears when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared.

When the chip is under "Block protect (BP) Mode". The Chip Erase (CE) instruction will not be executed, if one (or more) sector is protected by BP3-BP0 bits. It will be only executed when BP3-BP0 all set to "0".

Figure 67. Chip Erase (CE) Sequence (SPI Mode)

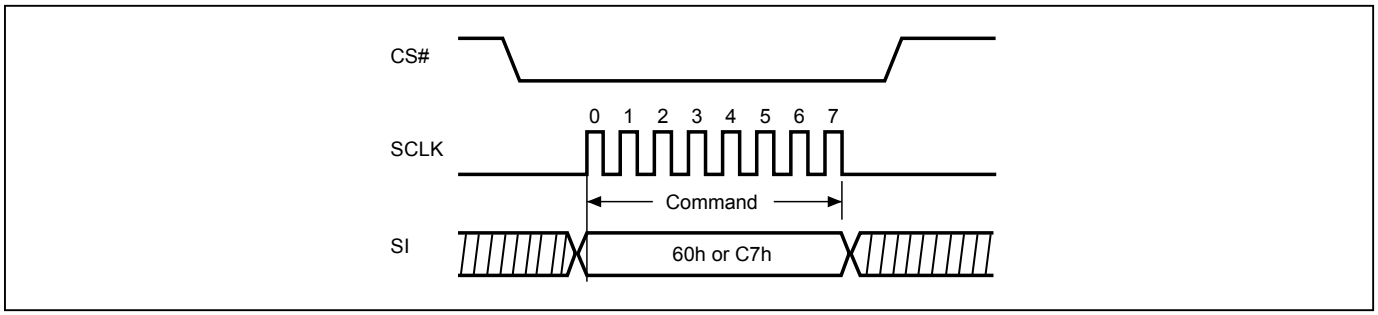


Figure 68. Chip Erase (CE) Sequence (STR-OPI Mode)

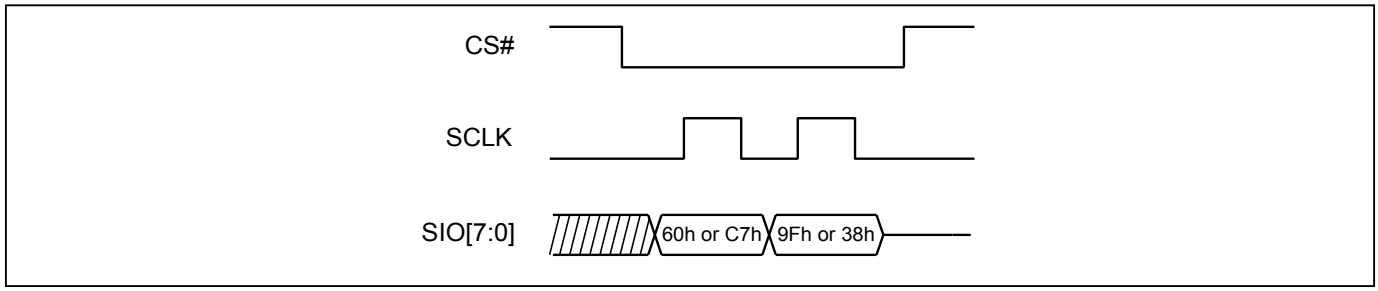
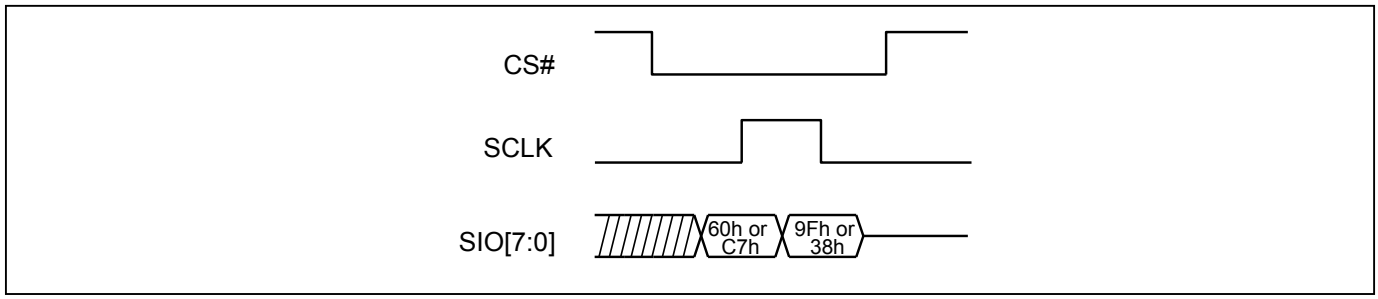


Figure 69. Chip Erase (CE) Sequence (DTR-OPI Mode)



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10-21. Page Program (PP/PP3B/PP4B)

The Page Program (PP/PP3B/PP4B) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending each Page Program (PP/PP3B/PP4B) command. The device programs only the last 256 data bytes sent to the device. The last address byte (the 8 least significant address bits, A7-A0) must be set to 0 for 256 bytes page program. If A7-A0 are not all zero, transmitted data that exceed page length are programmed from the starting address (32-bit address that last 8 bit are all 0) of currently selected page. If the data bytes sent to the device exceeds 256, the last 256 data byte is programmed at the request page and previous data will be disregarded. If the data bytes sent to the device has not exceeded 256, the data will be programmed at the request address of the page. There will be no effort on the other data bytes of the same page. Please refer *"12-1. ECC (Error Checking and Correcting)"* for Partial program or double program restriction.

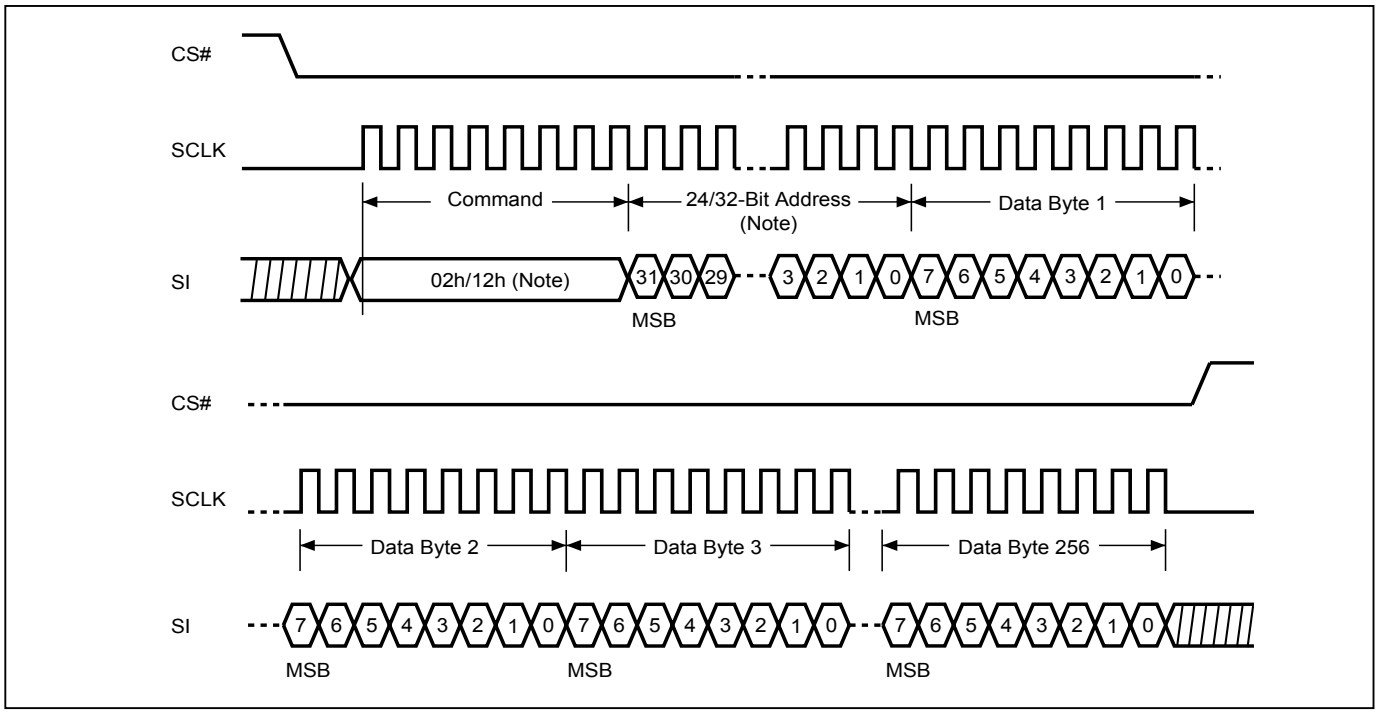
In DTR OPI, the starting address given must be even address (A0=0) and data byte number must be even.

The sequence of issuing PP/PP3B/PP4B instruction is: CS# goes low→ sending PP/PP3B/PP4B instruction code→ 3-byte or 4-byte address → at least 1-byte on data in SPI and STR OPI; at least two bytes in DOPI→ CS# goes high.

The CS# must be kept to low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary in SPI (the latest eighth bit of data being latched in), CS# must go high while SCLK is low in DOPI, otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Page Program cycle is in progress. The WIP sets during the tPP timing, and clears when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the page is protected by BP bits (Block Protect Mode), the Page Program (PP/PP3B/PP4B) instruction will not be executed.

Figure 70. Page Program (PP/PP3B/PP4B) Sequence (SPI Mode)



Note: The number of address cycles are based on different address mode. In 3-Byte command operation, it is 24-bit. In 4-Byte command operation, it is 32-bit.

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Figure 71. Page Program (PP) Sequence (STR-OPI Mode)

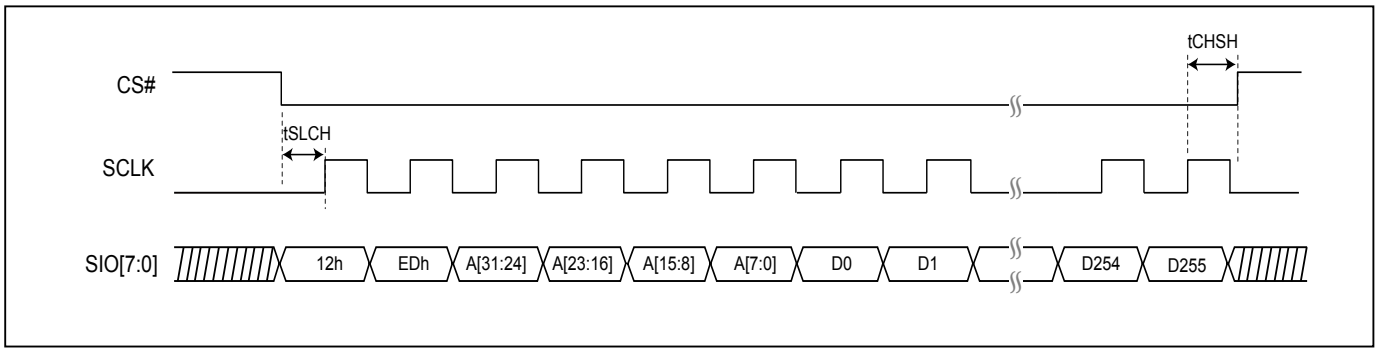
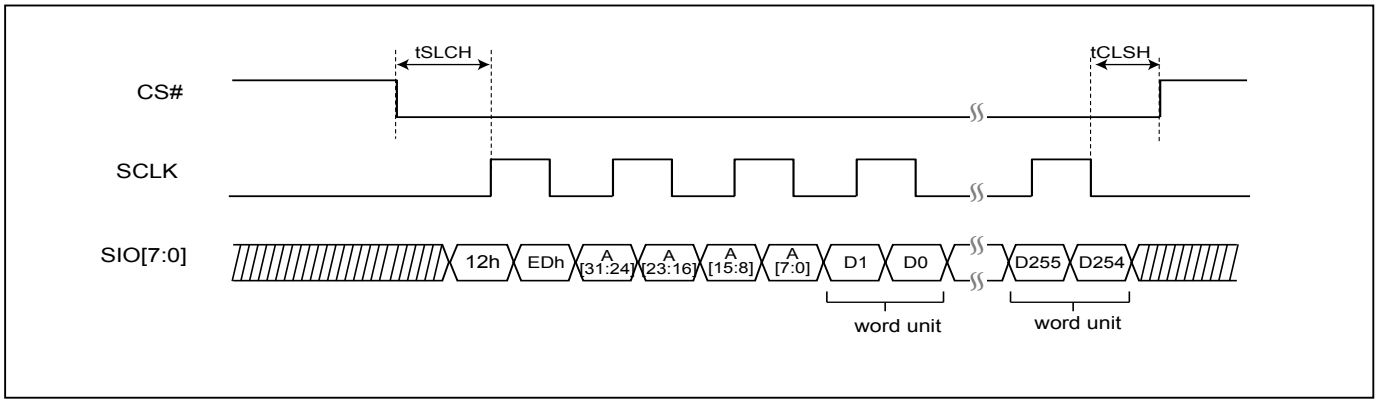


Figure 72. Page Program (PP) Sequence (DTR-OPI Mode)



Note: CS# must go high while SCLK is low.

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10-22. Interruptible Write to Buffer Sequence

The multi-bank read-while-write flash memory provides an interruptible write-to-buffer sequence during programming. This sequence provides the advantage that read operations could be inserted among program data write cycles. There are three steps for the operation: issuing WRBI (Write Buffer Initial command), WRCT (Write Buffer Continue command), and WRCF (Write Confirm command) as shown in *Figure 73*.

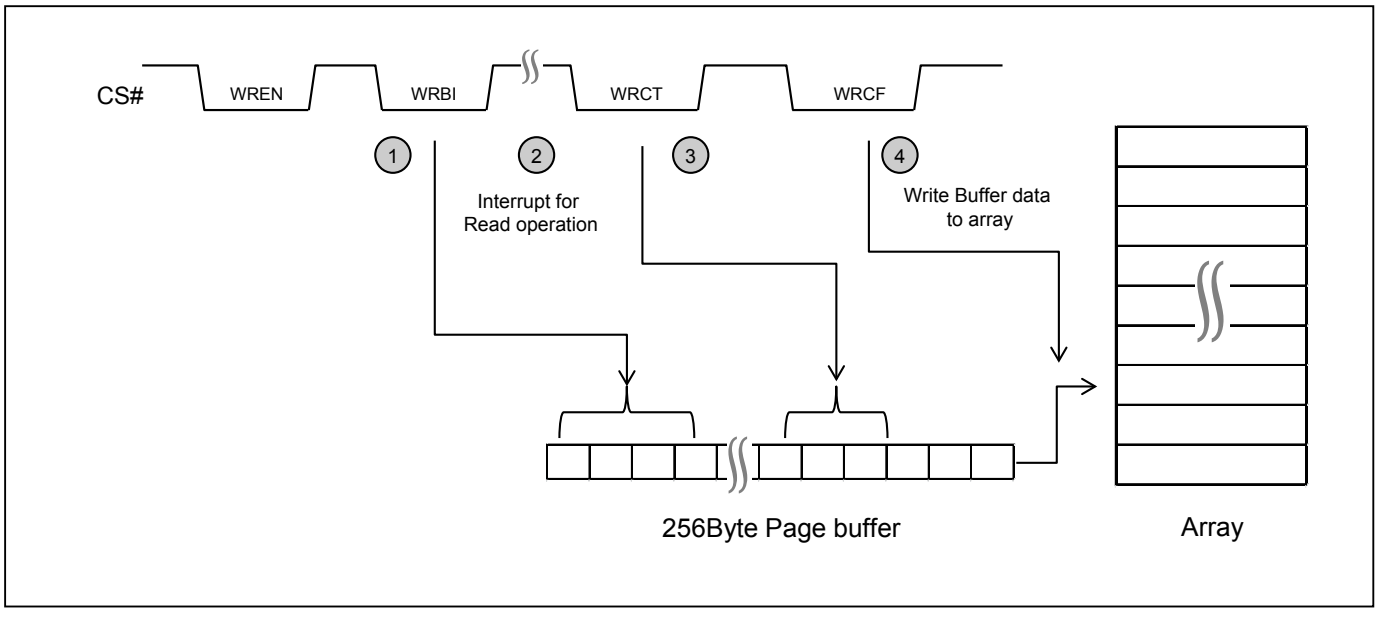
To trigger the interruptible write-to-buffer sequence, the system issues WREN command first to enable the WEL bit, and then issues WRBI with 4-byte address and data of 0~256 byte. After CS# has gone high, the flash memory will return to the standby status, waiting for the next command. The system could either perform read operation or issue Write Buffer Continue command (WRCT) to write more data to the page buffer. After the data writing has finished, the system will issue a Write Confirm (WRCF) command to initiate an automatic program operation to write the page buffer data into the array cell.

Multiple read or WRCT commands can be issued between the WRBI and WRCF commands. The system could also issue a WRBI directly followed by a WRCF command if there is no need for write interrupt on the system.

WRBI command can clear the page buffer area. If a WRBI command is issued following another WRBI command, the data written by the previous WRBI command would be abandoned. Any WRCT or WRCF command without a preceding WRBI command would be ignored. After WRBI/WRCT command, the WEL bit is kept set. A program, erase or write register command following WRBI/WRCT takes action without additional WREN command, and the write-to-buffer sequence is then discontinued; system has to do WREN and WRBI again to initiate another write-to-buffer sequence. A WRDI or reset commmand would also abort the sequence.

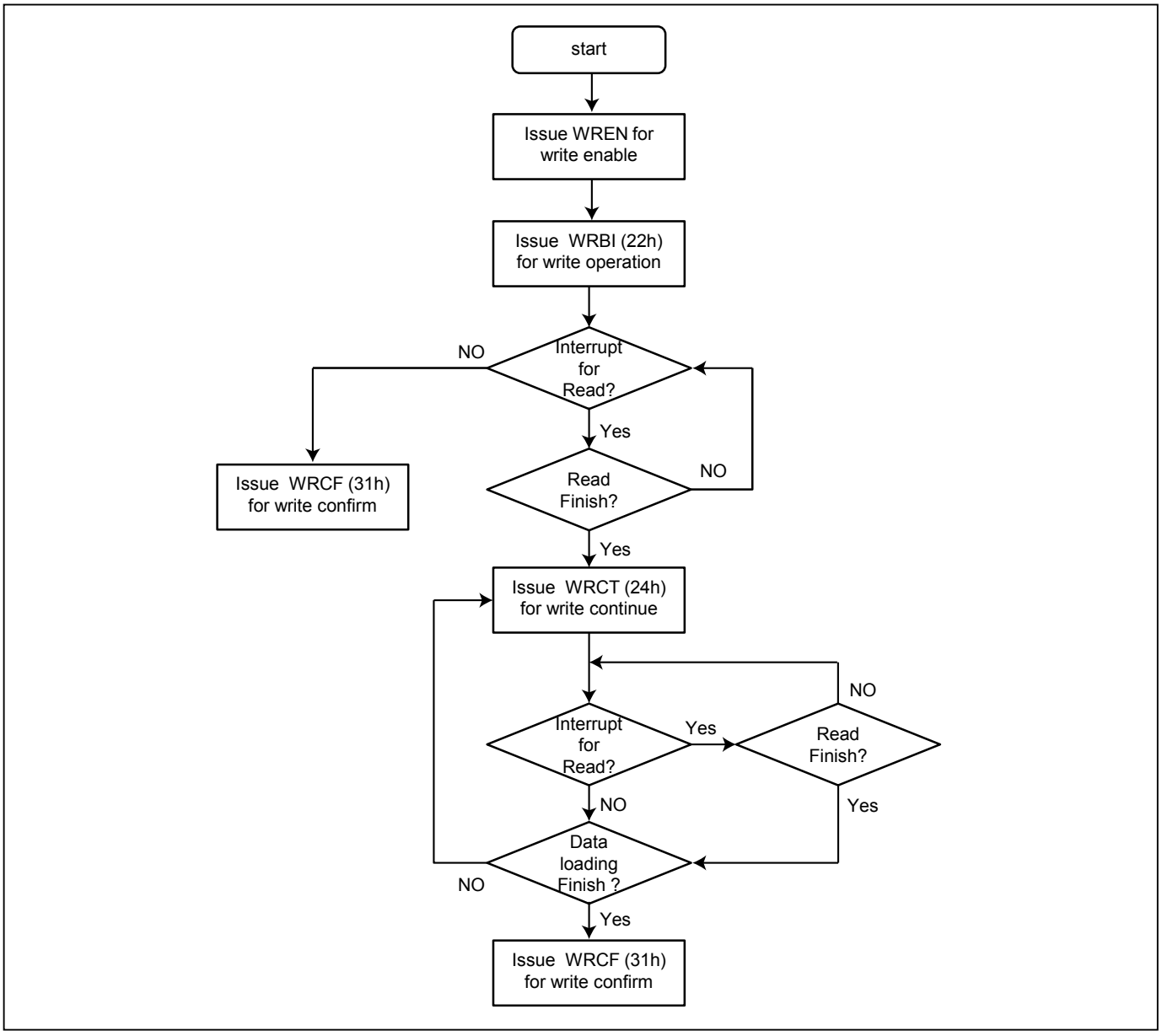
Notes:
- A WRBI command without fully 4-byte address cycle is invalid and will also abort previous initiated sequence.
- If CRC is not enabled, a WRBI/WRCT command with 4-byte address and without any data input cycle is regarded as valid.
- If CRC is enabled, at least one CRC chunk of data byte has to be issued in WRBI/WRCT, otherwise the sequence would be aborted.

Figure 73. Write Buffer Sequence



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Figure 74. Interruptible Write to Buffer Operation Flowchart



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Figure 75. Write Buffer Initial (WRBI) Sequence (SPI Mode)

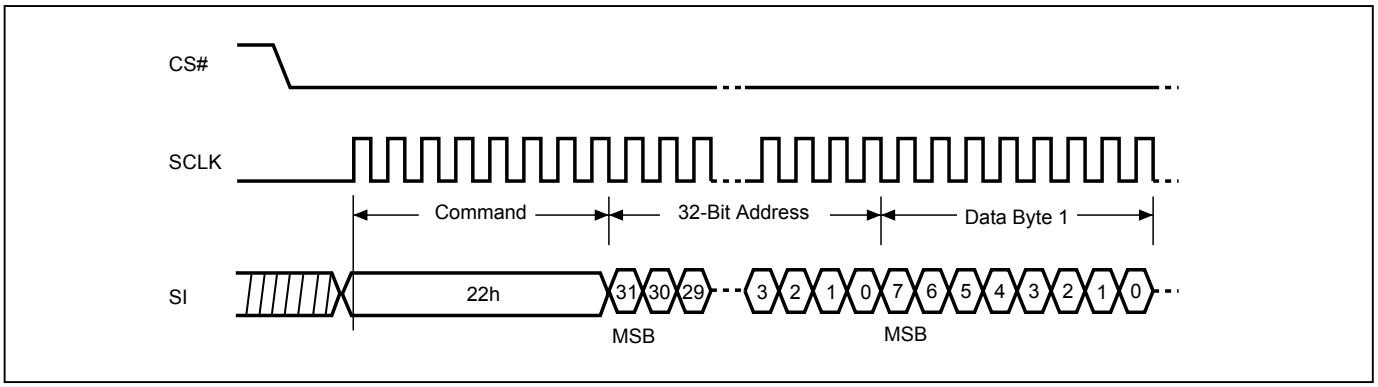


Figure 76. Write Buffer Initial (WRBI) Sequence (STR-OPI Mode)

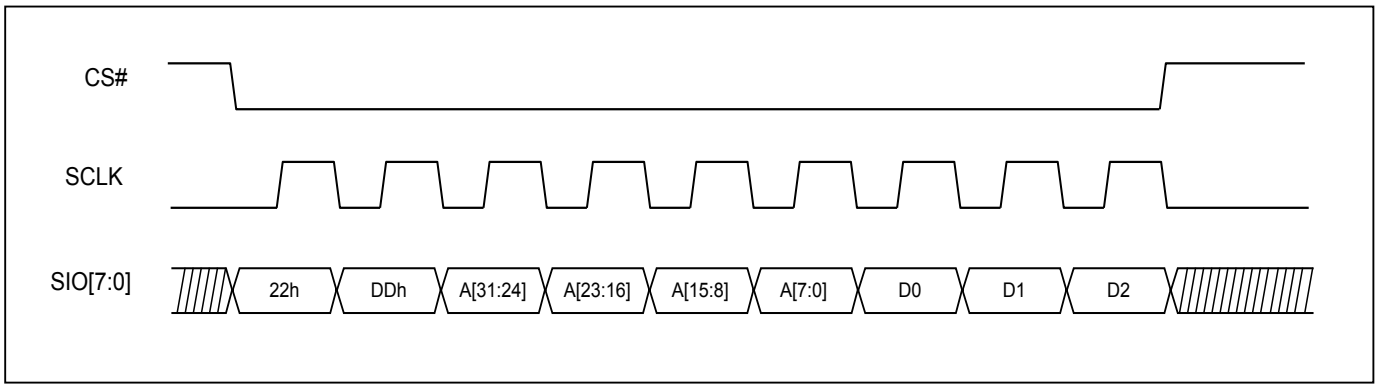
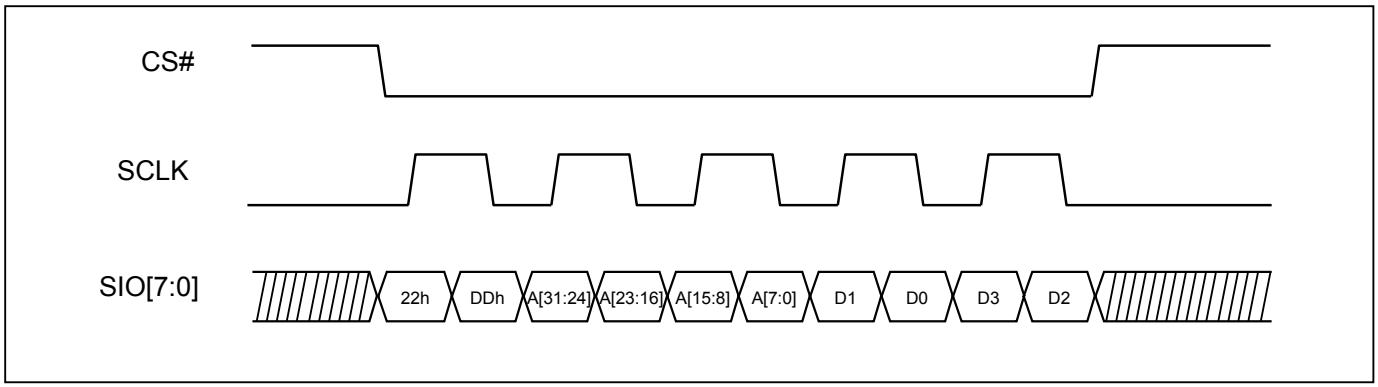
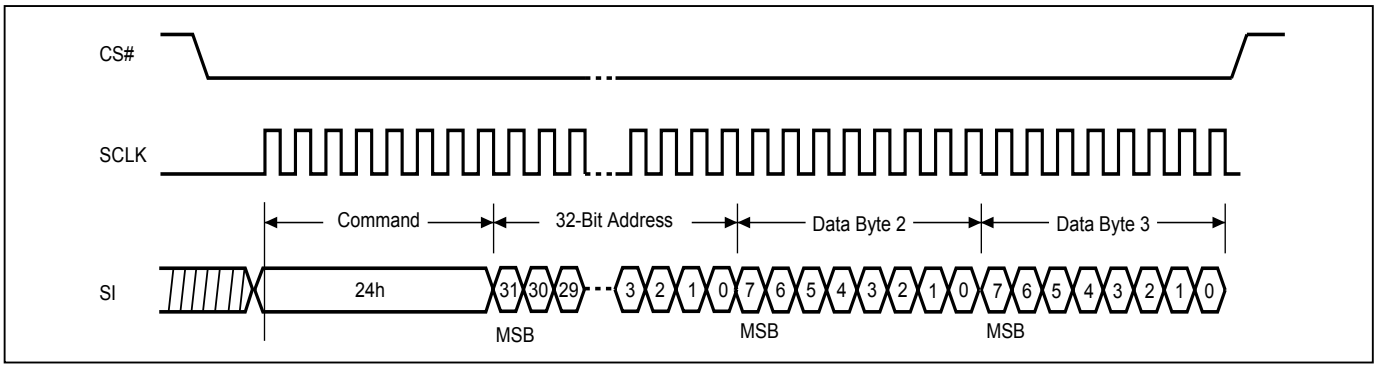


Figure 77. Write Buffer Initial (WRBI) Sequence (DTR-OPI Mode)



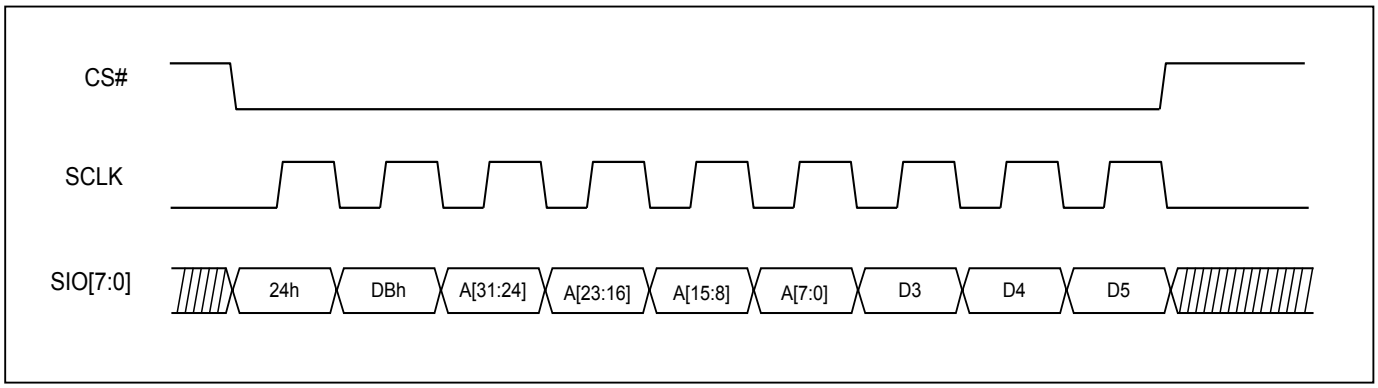
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Figure 78. Write Buffer Continue (WRCT) Sequence (SPI Mode)



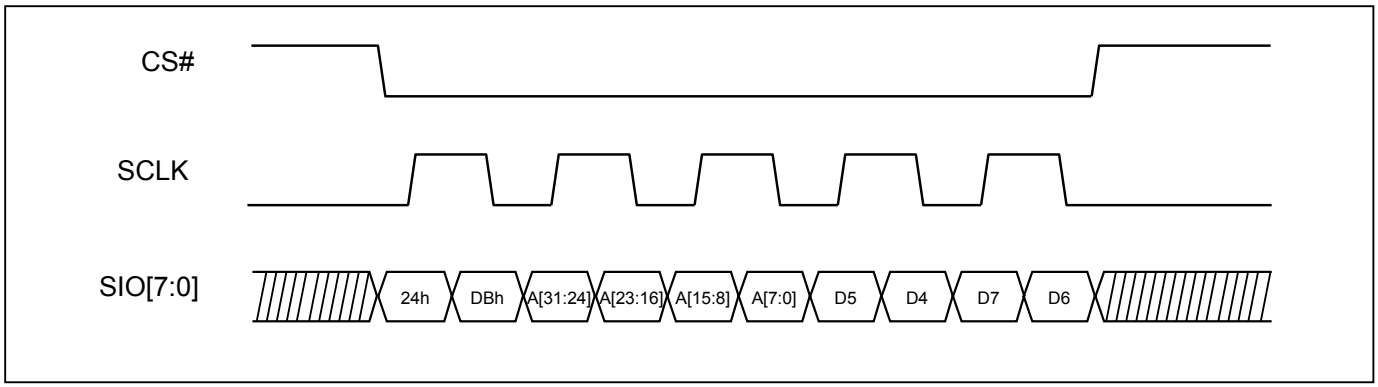
Note: Page address A[25:8] is don't care.

Figure 79. Write Buffer Continue (WRCT) Sequence (STR-OPI Mode)



Note: Page address A[25:8] is don't care.

Figure 80. Write Buffer Continue (WRCT) Sequence (DTR-OPI Mode)



Note: Page address A[25:8] is don't care.

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Figure 81. Write Buffer Confirm (WRCF) Sequence (SPI Mode)

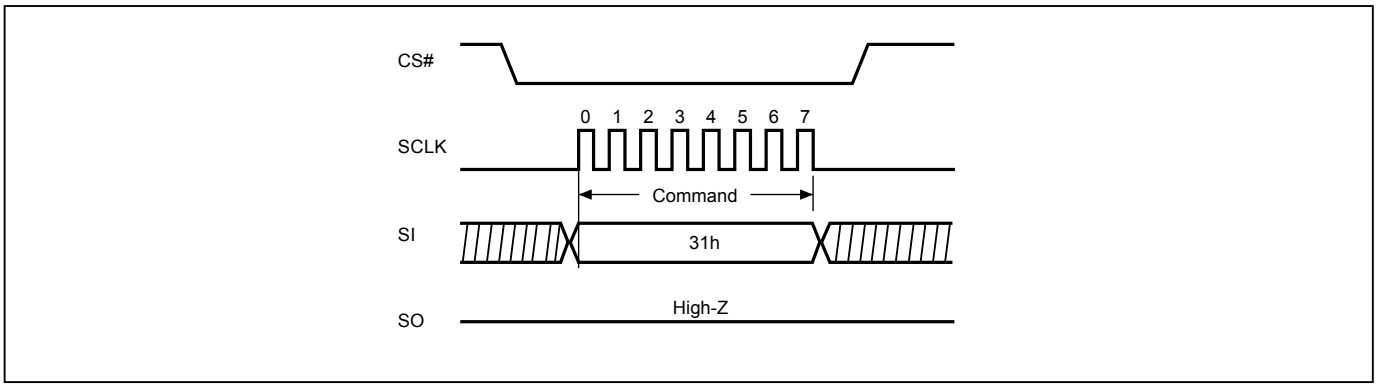


Figure 82. Write Buffer Confirm (WRCF) Sequence (STR-OPI Mode)

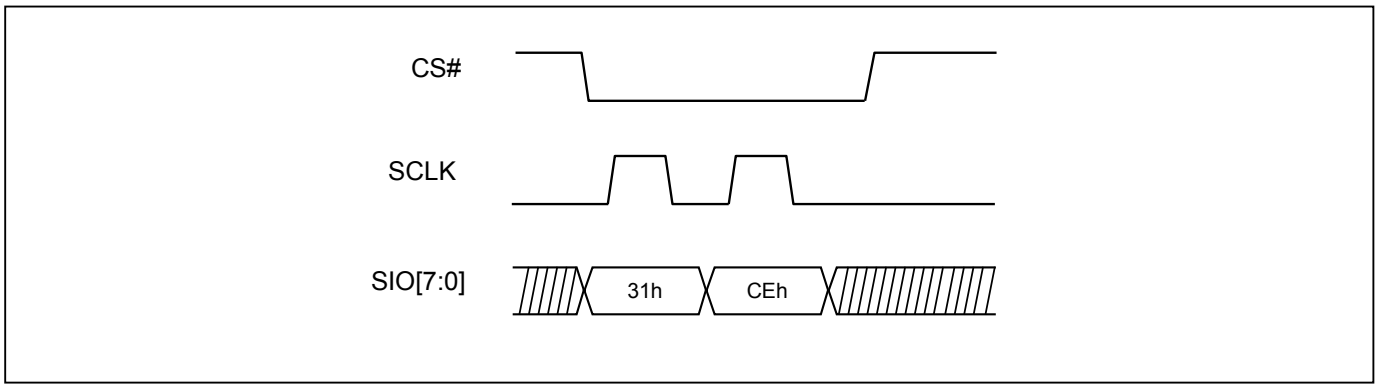
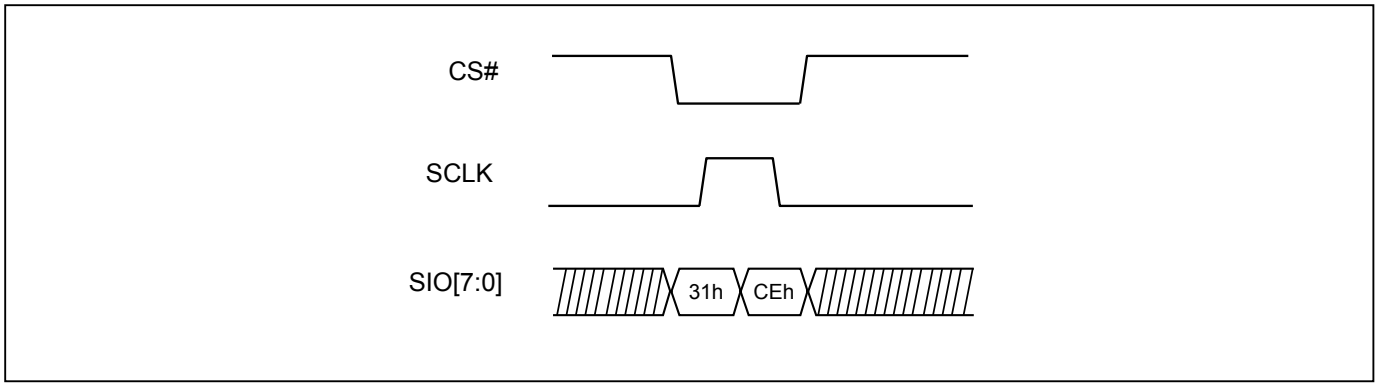


Figure 83. Write Buffer Confirm (WRCF) Sequence (DTR-OPI Mode)



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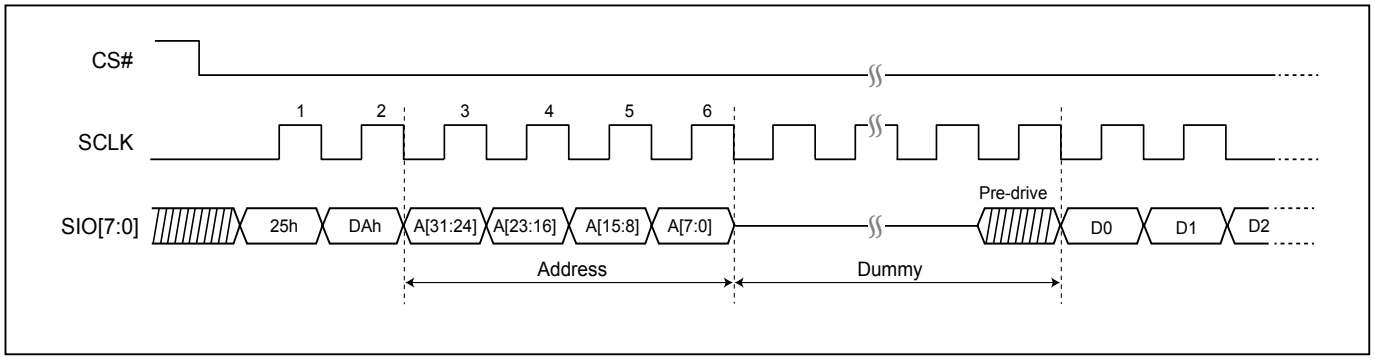
10-23. Page Buffer Read (RDBUF)

After the write-to-buffer sequence is initiated, the datum written into page buffer can be read out through RDBUF command.

To read the page buffer content, the system issues RDBUF command with 4-byte address followed by the configured dummy cycles and 1~256 data bytes. The dummy cycle number is determined by DC bits in Configuration Register 2.

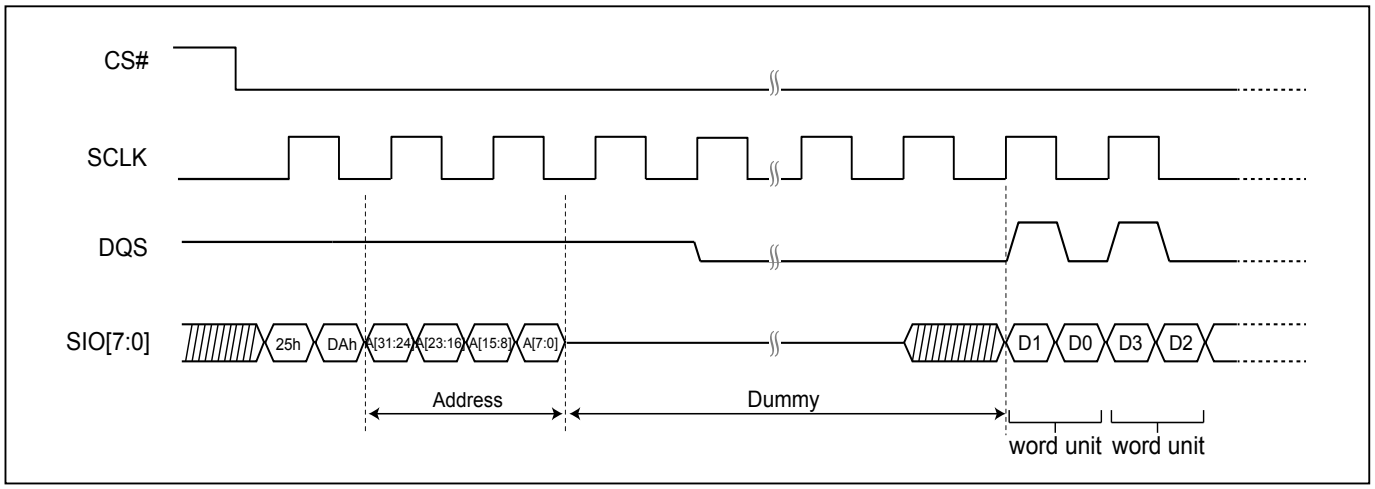
If system issues RDBUF without write-to-buffer initiation, data FFh will be output.
RDBUF command is effective only if flash is in standby state. RDBUF command is not affected by SBL command.

Figure 84. Page Buffer Read (RDBUF) Sequence (STR-OPI Mode)



Note: Only A[7:0] address bits are effective. Other address bits are don't care

Figure 85. Page Buffer Read (RDBUF) Sequence (DTR-OPI Mode)



Note: Only A[7:0] address bits are effective. Other address bits are don't care.

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10-24. Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device to minimum power consumption (the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When CS# goes high, it's only in deep power-down mode not standby mode. It's different from Standby mode.

The sequence of issuing DP instruction is: CS# goes low→sending DP instruction code→CS# goes high.

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction and softreset command. (those instructions allow the ID being reading out). When Power-down, or software reset command the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For DP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode.

The device exits Deep Power-down mode and returns to Stand-by mode if CS# pulses low for tCRDP or if the device is power-cycled or hardware reset. After CS# goes high, there is a delay of tRES1 before the device transitions from Deep Power-down mode back to Stand-by mode.

Figure 86. Deep Power-down (DP) Sequence (SPI Mode)

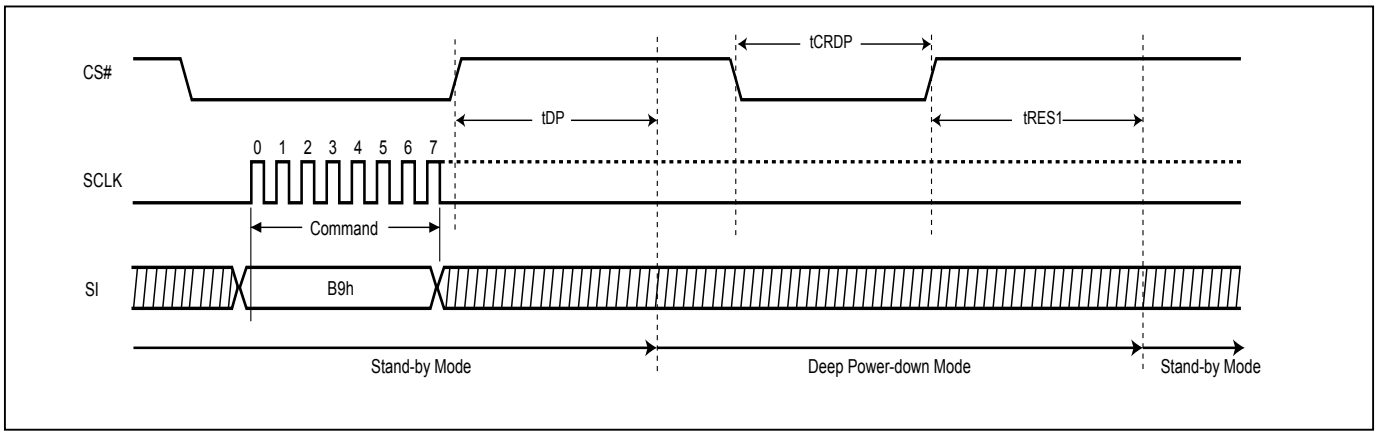
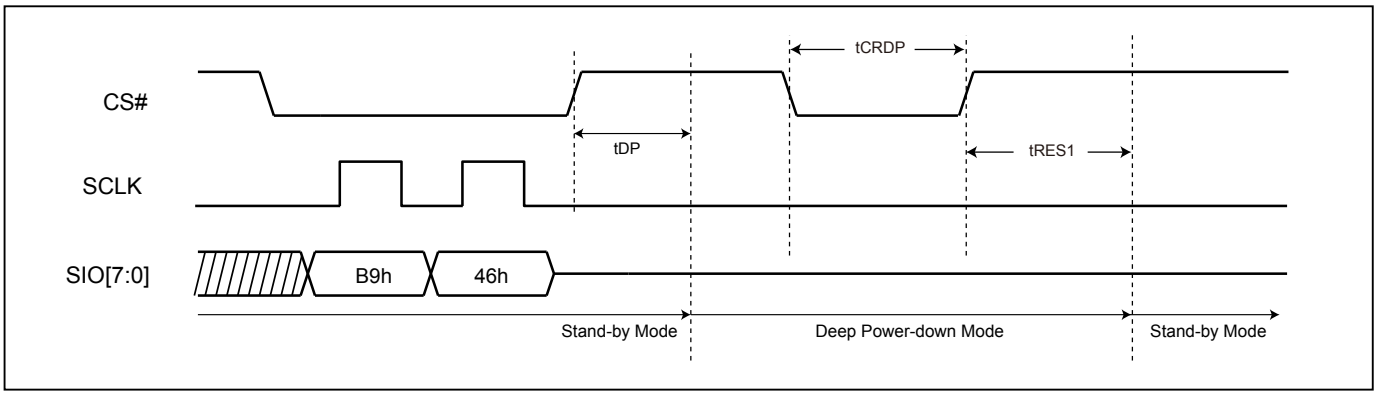
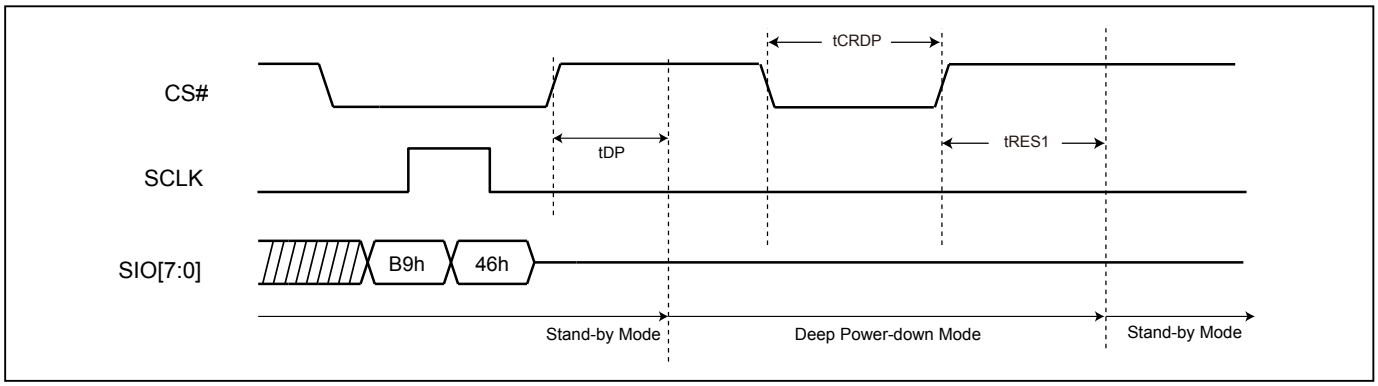


Figure 87. Deep Power-down (DP) Sequence (STR-OPI Mode)



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Figure 88. Deep Power-down (DP) Sequence (DTR-OPI Mode)



10-25. Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 8K-bit secured OTP mode. While device is in 8K-bit secured OTP mode, main array access is not available. The additional 8K-bit secured OTP is independent from main array and may be used to store unique serial number for system identifier. After entering the Secured OTP mode, follow standard read or program procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low→ sending ENSO instruction to enter Secured OTP mode→ CS# goes high.

Please note that after issuing ENSO command user can only access secure OTP region with standard read or program procedure. Furthermore, once security OTP is lock down, only read related commands are valid.

ENSO instruction is not allowed while the device is operating in PE mode or Write Register Mode.

10-26. Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 8K-bit secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low→ sending EXSO instruction to exit Secured OTP mode→ CS# goes high.

EXSO instruction is not allowed while the device is operating in PE mode or Write Register Mode.

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10-27. Write Protection Selection (WPSEL)

There are two write protection methods provided on this device, (1) Block Protection (BP) mode or (2) Advanced Sector Protection mode. The protection modes are mutually exclusive. The WPSEL bit selects which protection mode is enabled. If WPSEL=0 (factory default), BP mode is enabled and Advanced Sector Protection mode is disabled. If WPSEL=1, Advanced Sector Protection mode is enabled and BP mode is disabled. The WPSEL command is used to set WPSEL=1. A WREN command must be executed to set the WEL bit before sending the WPSEL command. **Please note that the WPSEL bit is an OTP bit. Once WPSEL is set to "1", it cannot be programmed back to "0".**

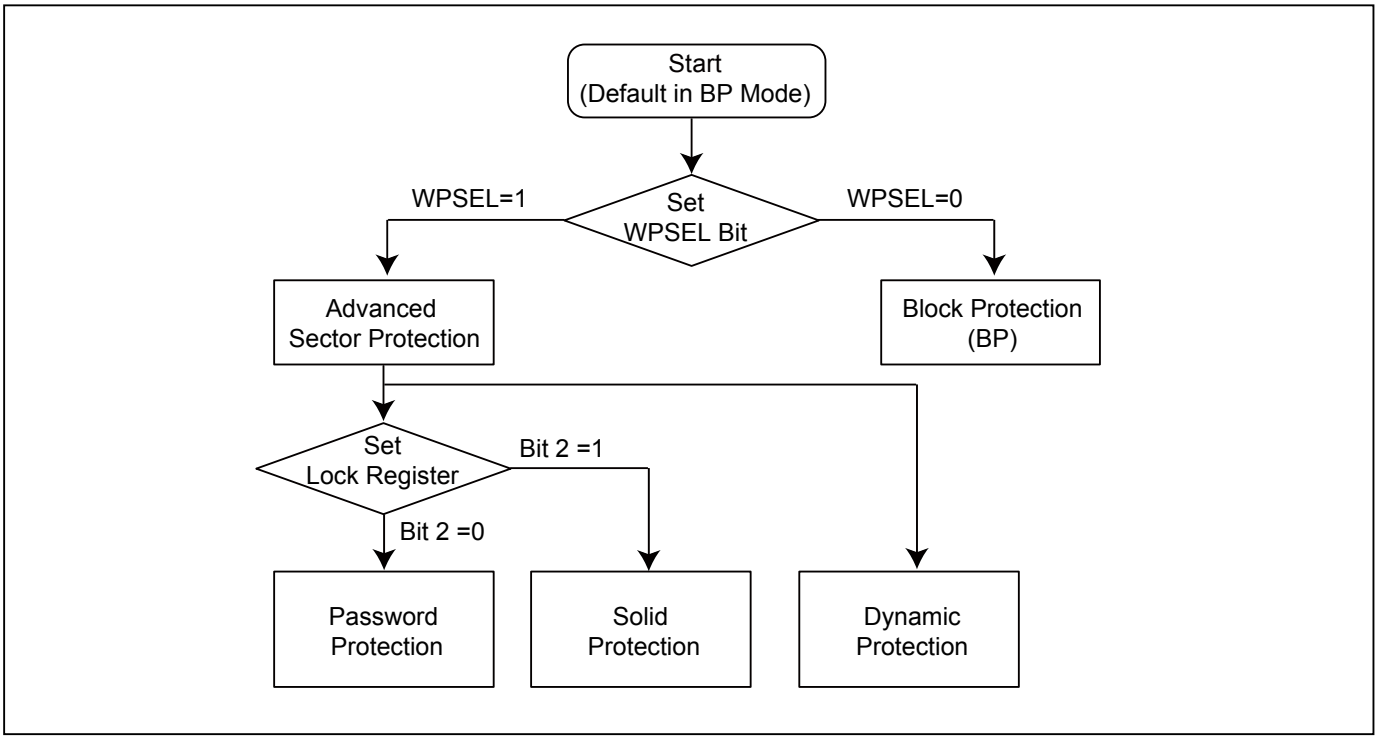
When WPSEL = 0: Block Protection (BP) mode,
The memory array is write protected by the BP3~BP0 bits.

When WPSEL =1: Advanced Sector Protection mode,
Blocks are individually protected by their own SPB or DPB. On power-up, all blocks are write protected by the Dynamic Protection Bits (DPB) by default. The Advanced Sector Protection instructions WRLR, RDLR, WRPASS, RDPASS, PASSULK, WRSPB, ESSPB, WRDPB, RDDPB, GBLK, and GBULK are activated. The BP3~BP0 bits of the Status Register are disabled and have no effect.

The sequence of issuing WPSEL instruction is: CS# goes low → send WPSEL instruction to enable the Advanced Sector Protect mode → CS# goes high.

WPSEL instruction is not allowed while the device is operating in PE mode or Write Register Mode.

Write Protection Selection



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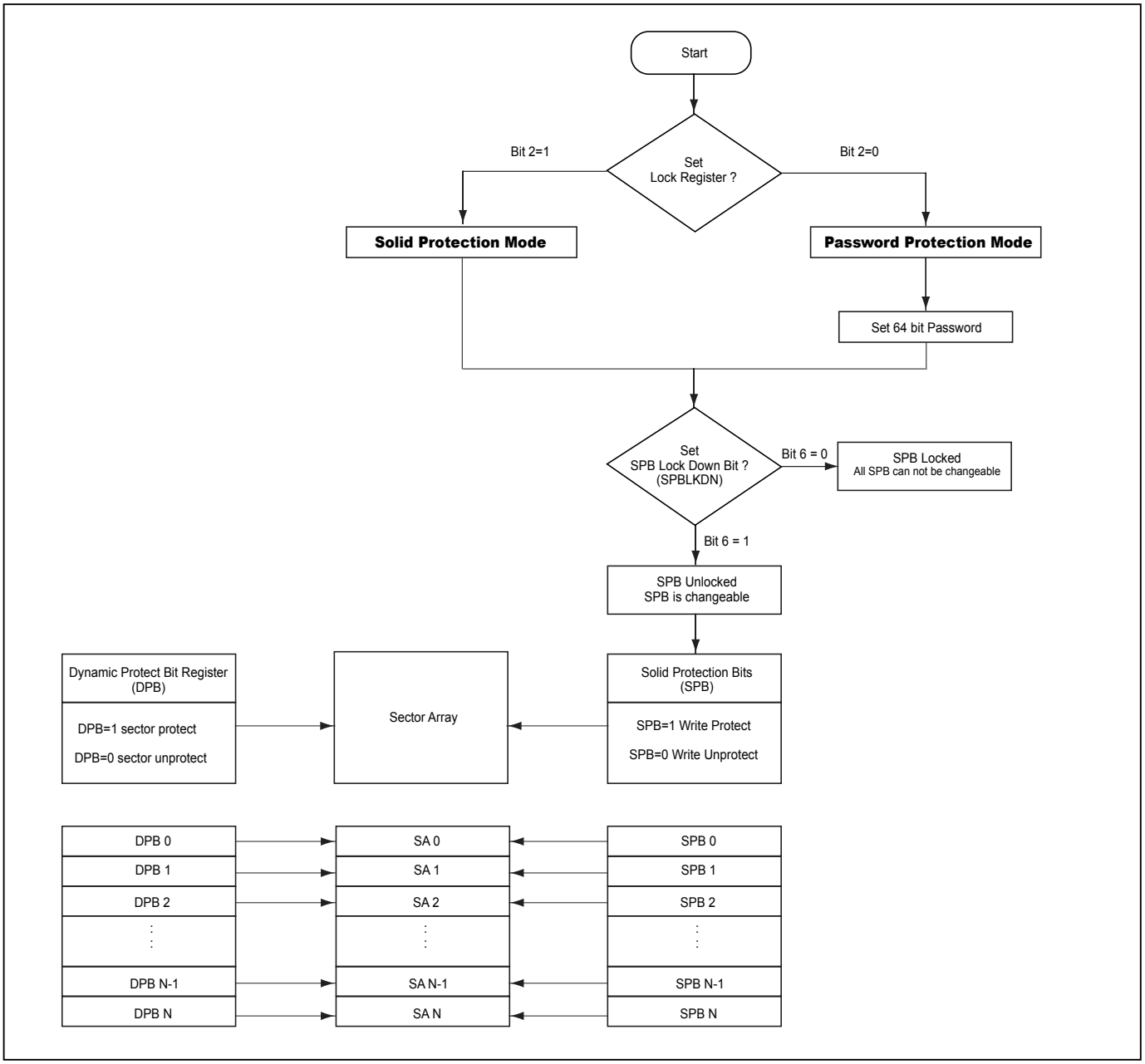
10-28. Advanced Sector Protection

There are two ways to implement software Advanced Sector Protection on this device. Through these two protection methods, user can disable or enable the programming or erasing operation to any individual sector or all sectors.

There is a non-volatile (SPB) and volatile (DPB) protection bit related to the single sector in main flash array. Each of the sectors is protected from programming or erasing operation when the bit is set.

The figure below helps describing an overview of these methods. The device is default to the Solid mode when shipped from factory. The detail algorithm of advanced sector protection is shown as follows:

Figure 89. Advanced Sector Protection Overview



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10-28-1. Lock Register

The Lock Register is a 8-bit register. Lock Register Bit[6] is SPB Lock Down Bit (SPBLKDN) which is assigned to control all SPB bit status. Lock Register Bit[2] is Password Protection Mode Lock Bit. Both bits are defaulted as 1 when shipping from factory.

When SPBLKDN is 1, SPB can be changed. When it is locked as 0, all SPB can not be changed.

Users can choose their favorite sector protecting method via setting Lock Register Bit[2] using WRLR command. The device default status was in Solid Protection Mode (Bit[2]=1), Once Bit[2] has been programmed (cleared to "0"), the device will enable the Password Protection Mode and lock in that mode permanently.

In Solid Protection Mode (Bit[2]=1, factory default), the SPBLKDN can be programmed using the WRLR command and permanently lock down the SPB bits. After programming SPBLKDN to 0, all SPB can not be changed anymore, and neither Lock Register Bit[2] nor Bit[6] can be altered anymore.

In Password Protection Mode (Bit[2]=0), the SPBLKDN becomes a volatile bit with default 0 (SPB bit protected). A correct password is required with PASSULK command to set SPBLKDN to 1. To clear SPBLKDN back to 0, a Hardware/Software Reset or power-up cycle is required.

If user selects Password Protection mode, the password setting is required. User can set password by issuing WRPASS command before Lock Register Bit[2] set to 0.

Lock Register

Bits	Description	Bit Status	Default	Type
7	Reserved	Reserved		Reserved
6	SPB Lock Down bit (SPBLKDN)	0: SPB bit Protected 1: SPB bit Unprotected	Solid Protection Mode: 1 Password Protection Mode: 0	Bit 2=1: OTP Bit 2=0: Volatile
5 to 3	Reserved	Reserved		Reserved
2	Password Protection Mode Lock Bit	0=Password Protection Mode Enable 1= Solid Protection Mode	1	OTP
1 to 0	Reserved	Reserved		Reserved

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Figure 90. Read Lock Register (RDLR) Sequence

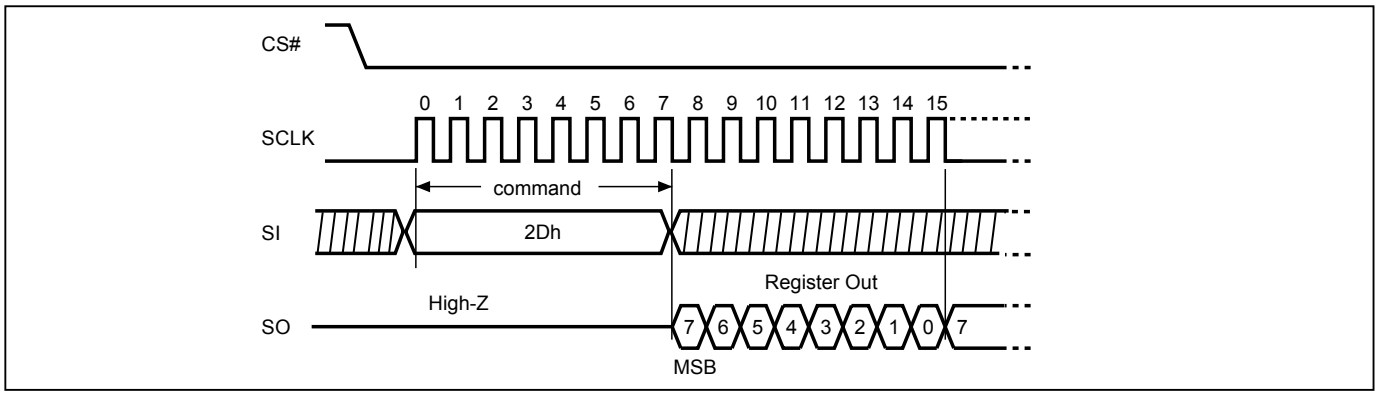


Figure 91. Read Lock Register (RDLR) Sequence (STR-OPI Mode)

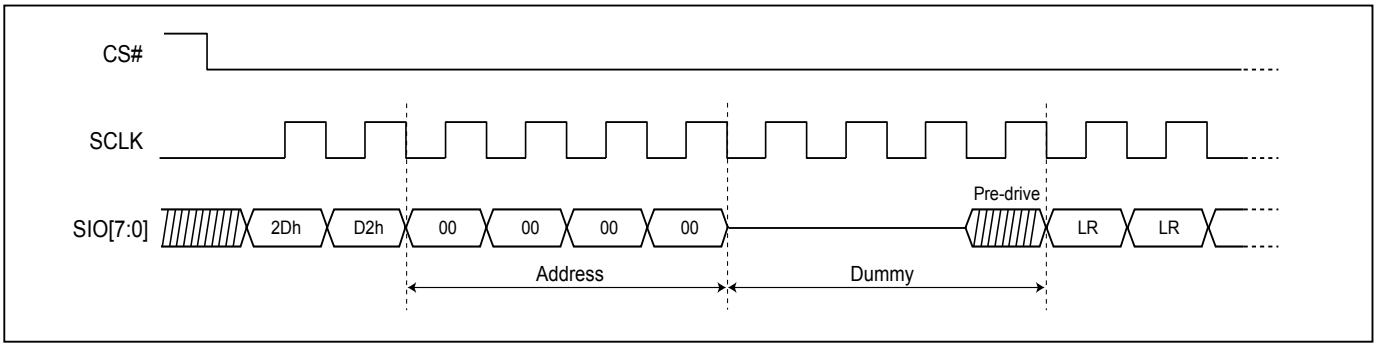
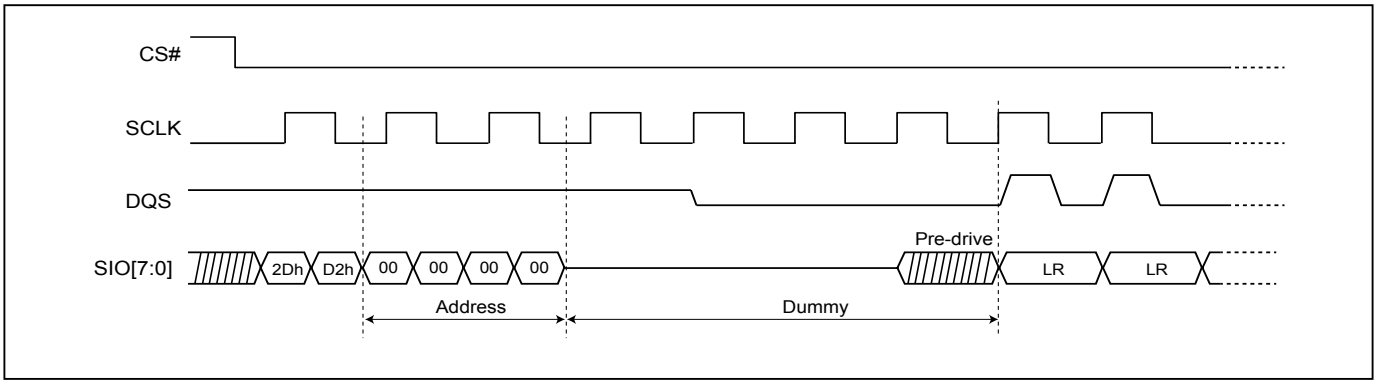


Figure 92. Read Lock Register (RDLR) Sequence (DTR-OPI Mode)



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Figure 93. Write Lock Register (WRLR) Sequence

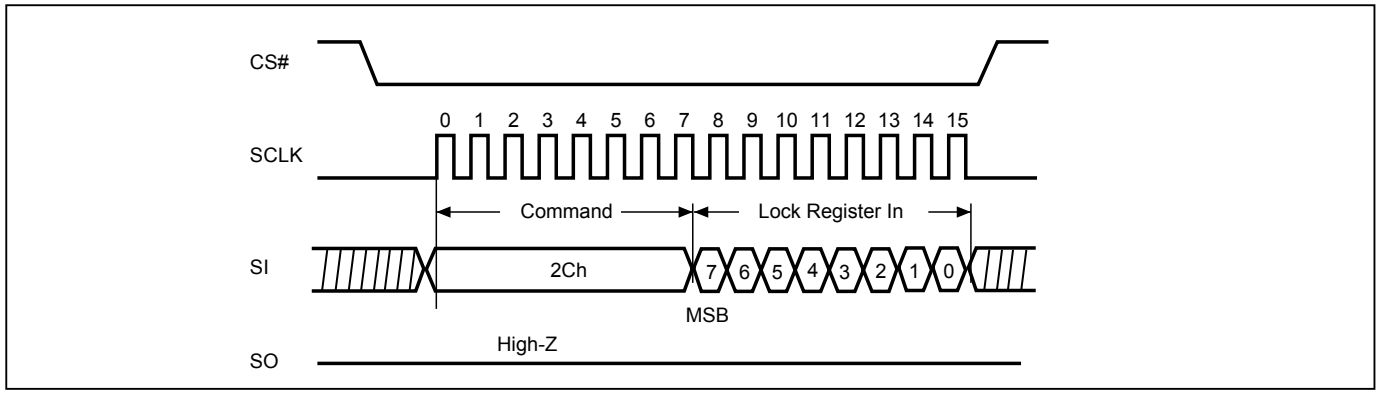


Figure 94. Write Lock Register (WRLR) Sequence (STR-OPI Mode)

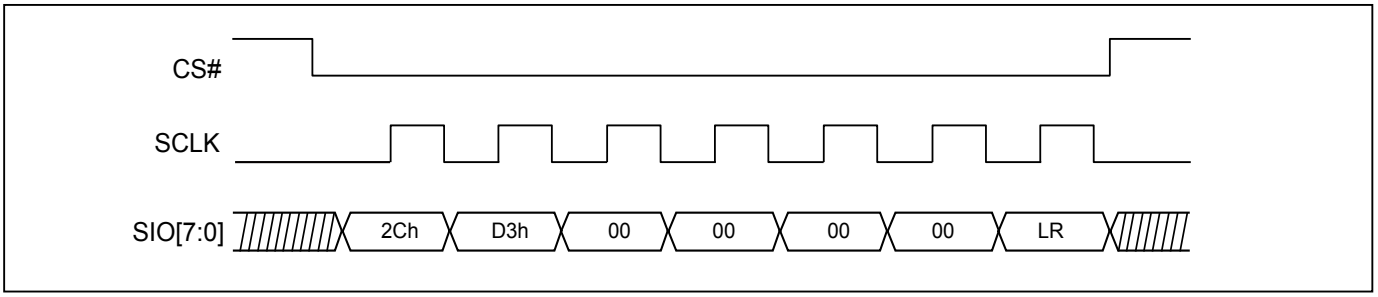
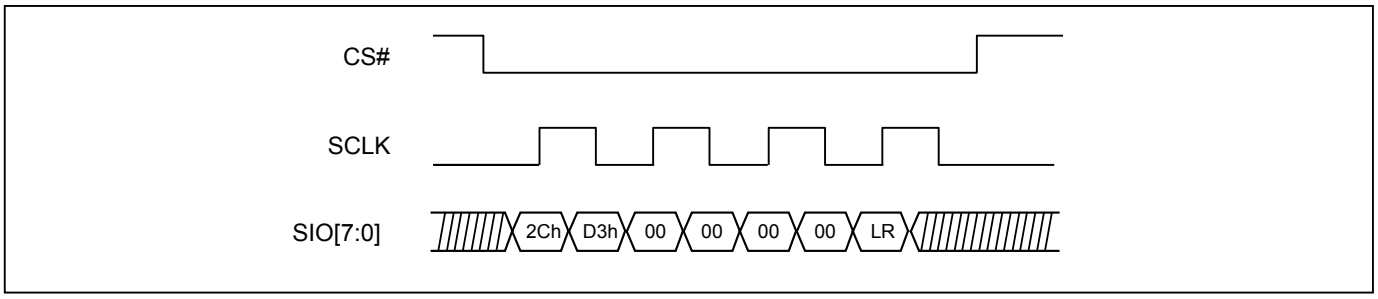


Figure 95. Write Lock Register (WRLR) Sequence (DTR-OPI Mode)



Note: CS# must go high while SCLK is low.

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10-28-2. Solid Protection Bits

The Solid Protection Bits (SPBs) are nonvolatile bits for enabling or disabling write-protection to sectors and blocks. The SPB bits have the same endurance as the Flash memory. An SPB is assigned to each 4KB sector in the bottom and top 64KB of memory and to each 64KB block in the remaining memory. The factory default state of the SPB bits is “0”, which has the sector/block write-protection disabled.

When an SPB is set to “1”, the associated sector or block is write-protected. Program and erase operations on the sector or block will be inhibited. SPBs can be individually set to “1” by the WRSPB command. However, the SPBs cannot be individually cleared to “0”. Issuing the ESSPB command clears all SPBs to “0”. A WREN command must be executed to set the WEL bit before sending the WRSPB or ESSPB command.

The RDSPB command reads the status of the SPB of a sector or block. The RDSPB command returns 00h if the SPB is “0”, indicating write-protection is disabled. The RDSPB command returns FFh if the SPB is “1”, indicating write-protection is enabled.

RDSPB, ESSPB and WRSPB instructions are not allowed while the device is operating in PE mode or Write Register Mode.

Note: If SPBLKDN=0, commands to set or clear the SPB bits will be ignored.

SPB Register

Bit	Description	Bit Status	Default	Type
7 to 0	SPB (Solid Protection Bit)	00h = Unprotect Sector / Block FFh = Protect Sector / Block	00h	Non-volatile

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Figure 96. Read SPB Status (RDSPB) Sequence

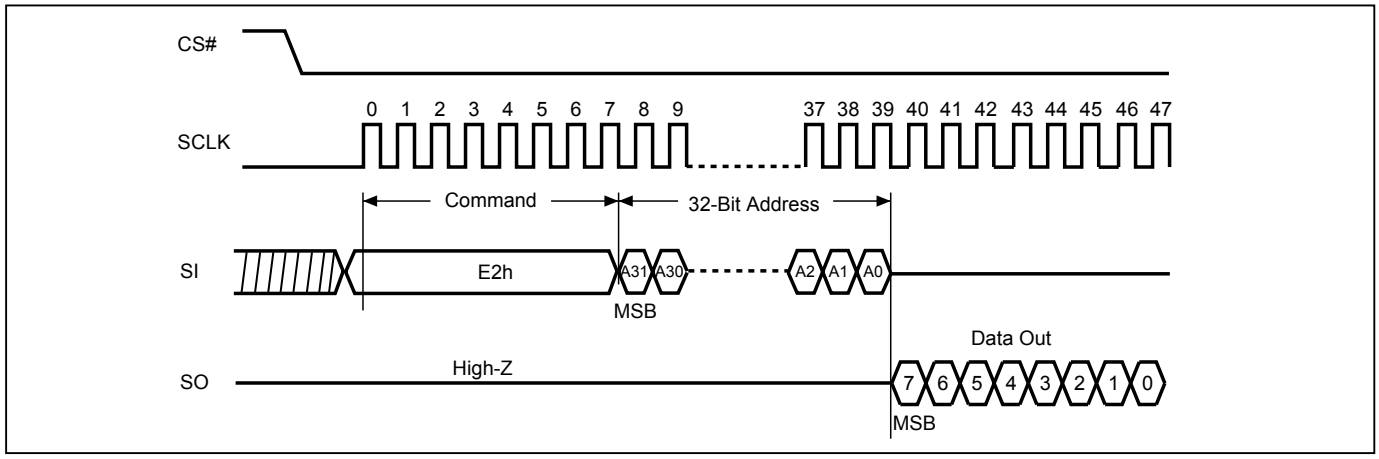


Figure 97. Read SPB Status (RDSPB) Sequence (STR-OPI Mode)

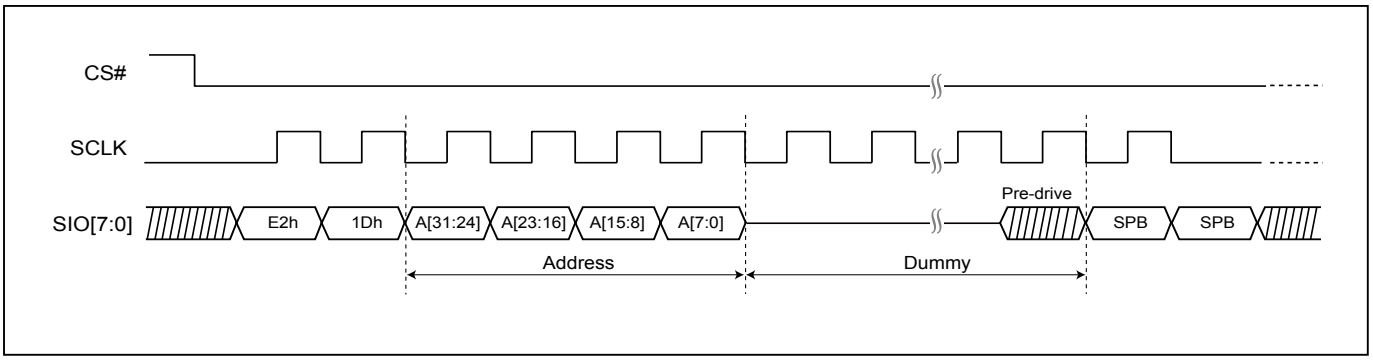
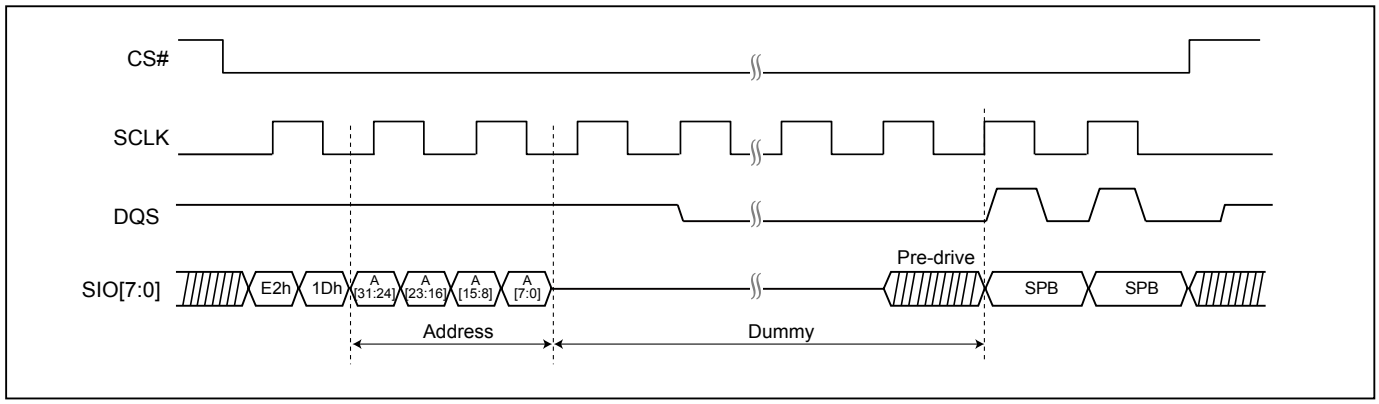


Figure 98. Read SPB Status (RDSPB) Sequence (DTR-OPI Mode)



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Figure 99. SPB Erase (ESSPB) Sequence

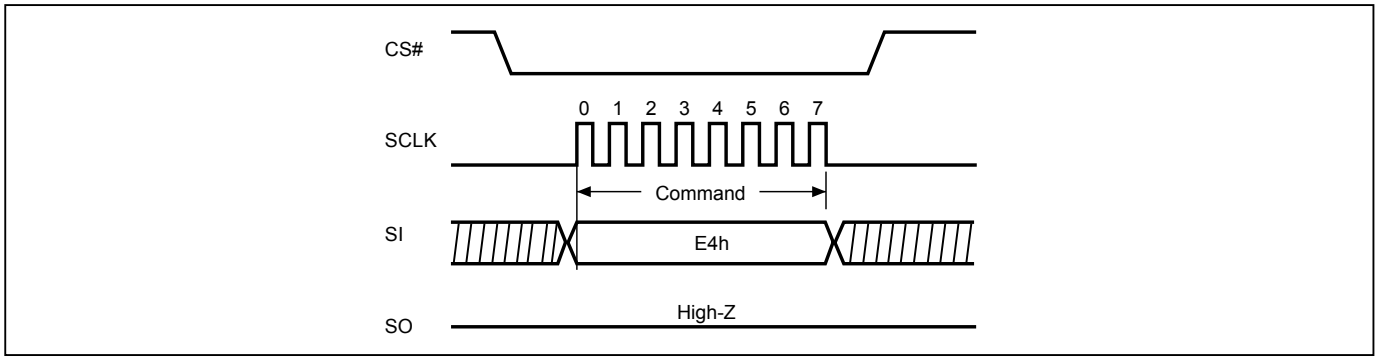


Figure 100. SPB Erase (ESSPB) Sequence (STR-OPI Mode)

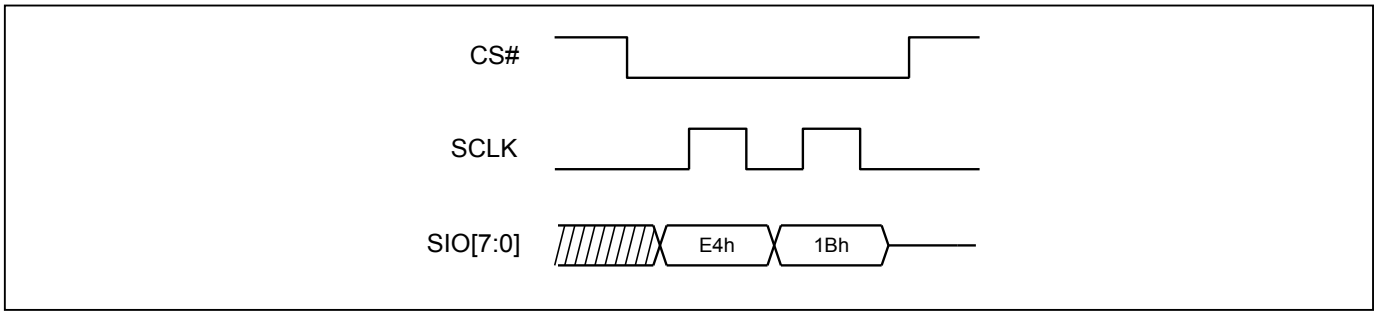
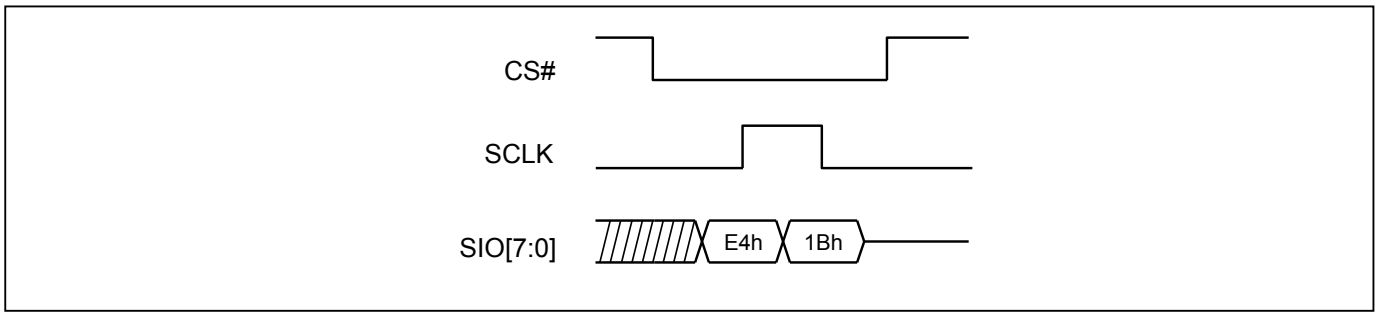


Figure 101. SPB Erase (ESSPB) Sequence (DTR-OPI Mode)



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Figure 102. SPB Program (WRSPB) Sequence

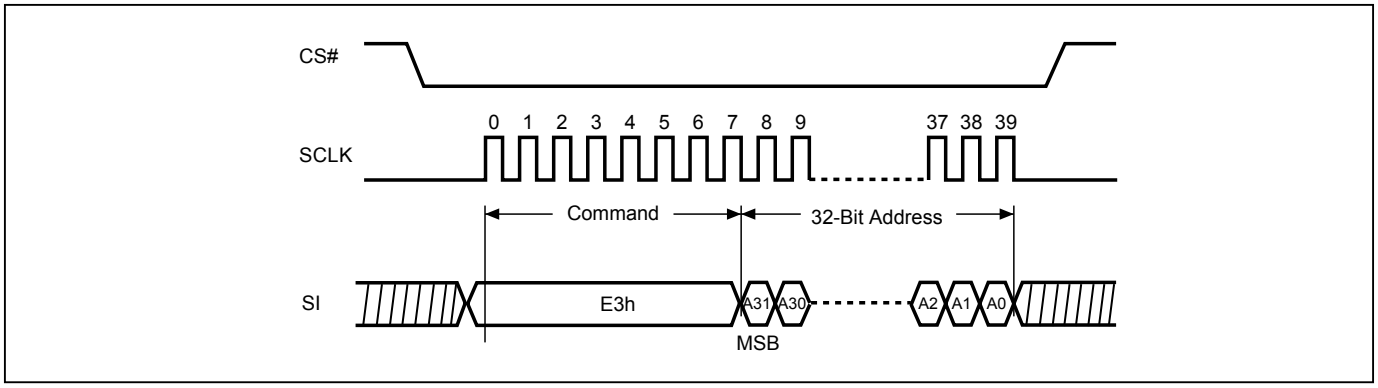


Figure 103. SPB Program (WRSPB) Sequence (STR-OPI Mode)

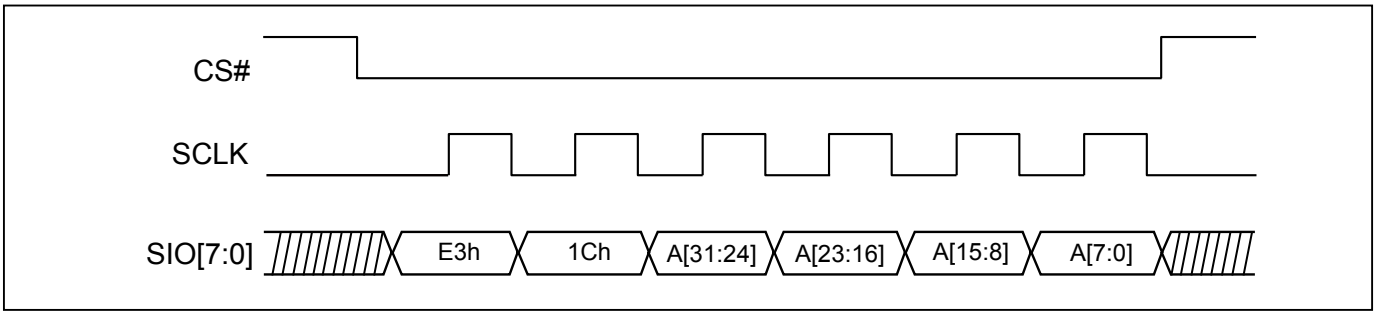
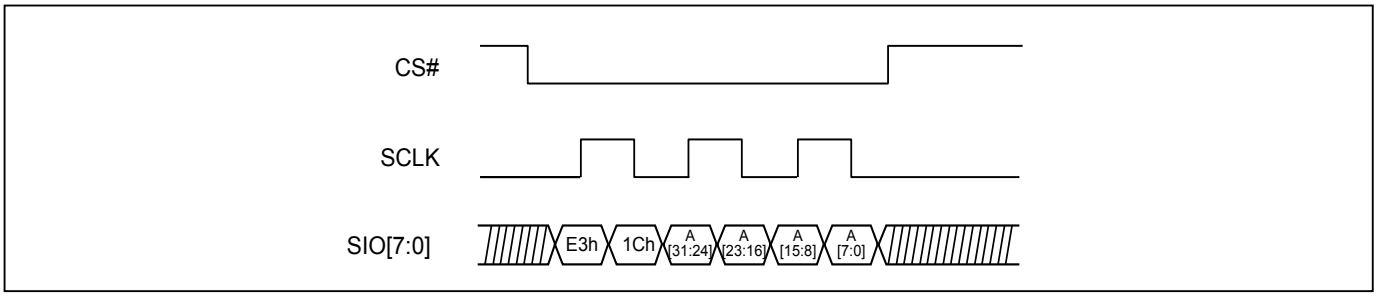


Figure 104. SPB Program (WRSPB) Sequence (DTR-OPI Mode)



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10-28-3. Dynamic Write Protection Bits

The Dynamic Protection features a volatile type protection to each individual sector. It can protect sectors from unintentional change, and is easy to disable when there are necessary changes.

All DPBs are default as protected (FFh) after reset or upon power up cycle. Via setting up Dynamic Protection bit (DPB) by write DPB command (WRDPB), user can cancel the Dynamic Protection of associated sector.

The Dynamic Protection only works on those unprotected sectors whose SPBs are cleared. After the DPB state is cleared to “0”, the sector can be modified if the SPB state is unprotected state.

RDDPB and WRDPB instructions are not allowed while the device is operating in PE mode or Write Register Mode.

DPB Register

Bit	Description	Bit Status	Default	Type
7 to 0	DPB (Dynamic protected Bit)	00h= DPB for the sector address unprotected FFh= DPB for the sector address protected	FFh	Volatile

Figure 105. Read DPB Register (RDDPB) Sequence

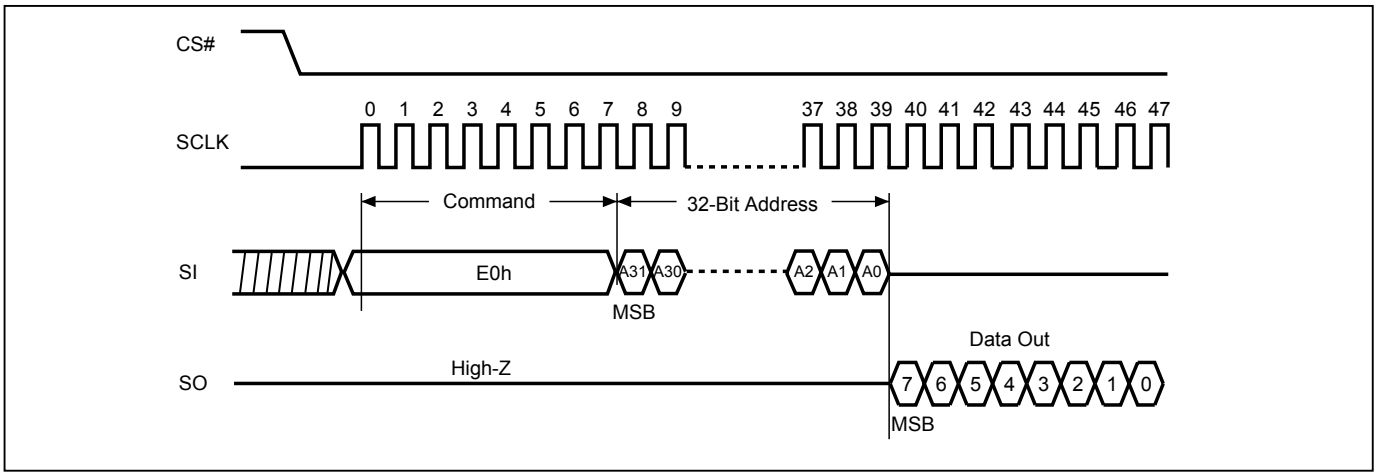
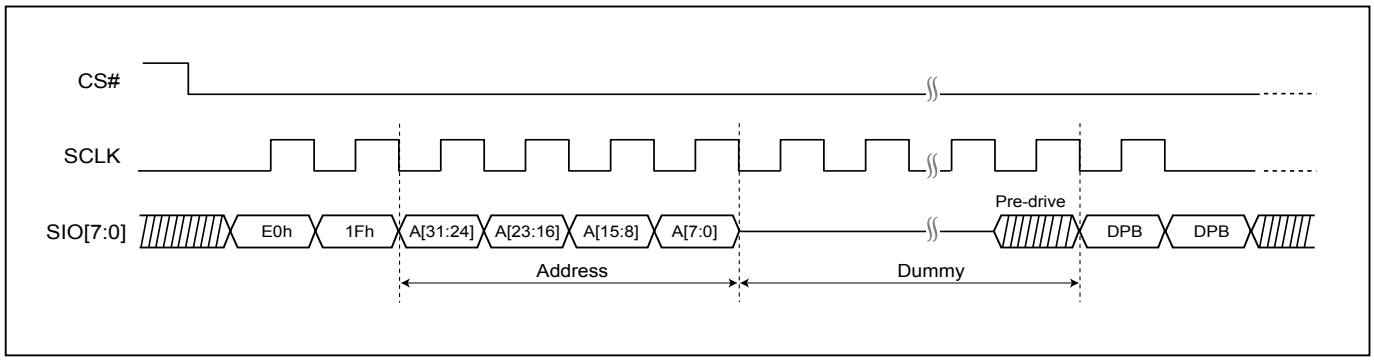


Figure 106. Read DPB Register (RDDPB) Sequence (STR-OPI Mode)



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Figure 107. Read DPB Register (RDDPB) Sequence (DTR-OPI Mode)

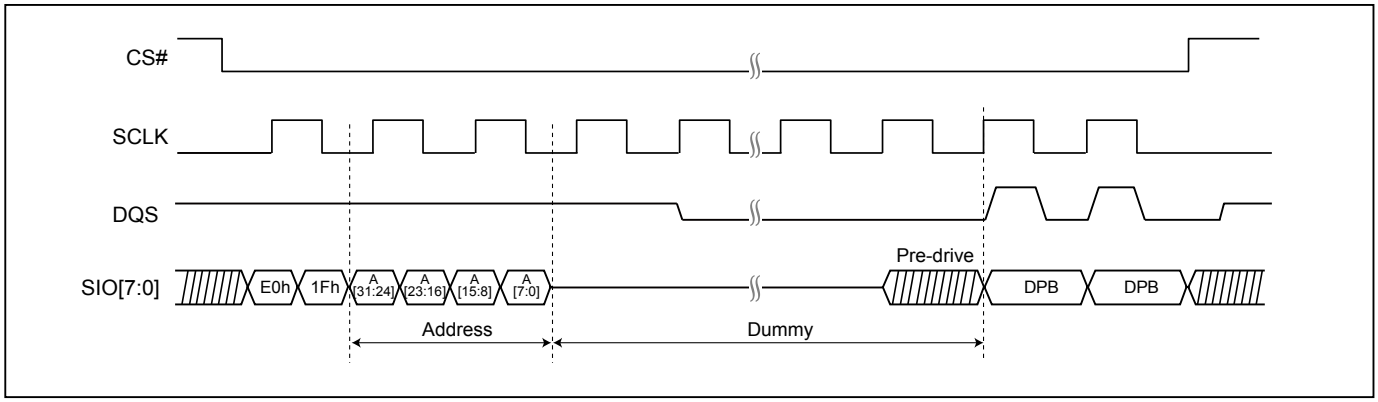


Figure 108. Write DPB Register (WRDPB) Sequence

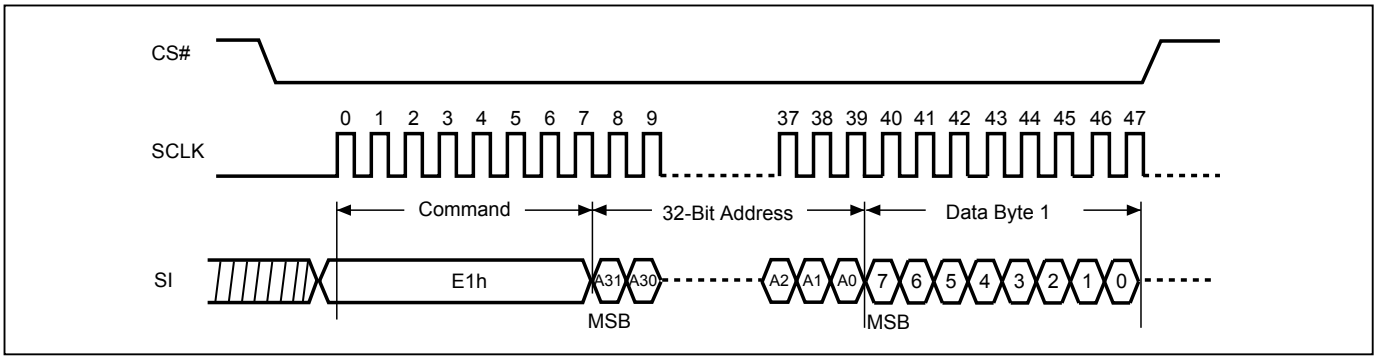


Figure 109. Write DPB Register (WRDPB) Sequence (STR-OPI Mode)

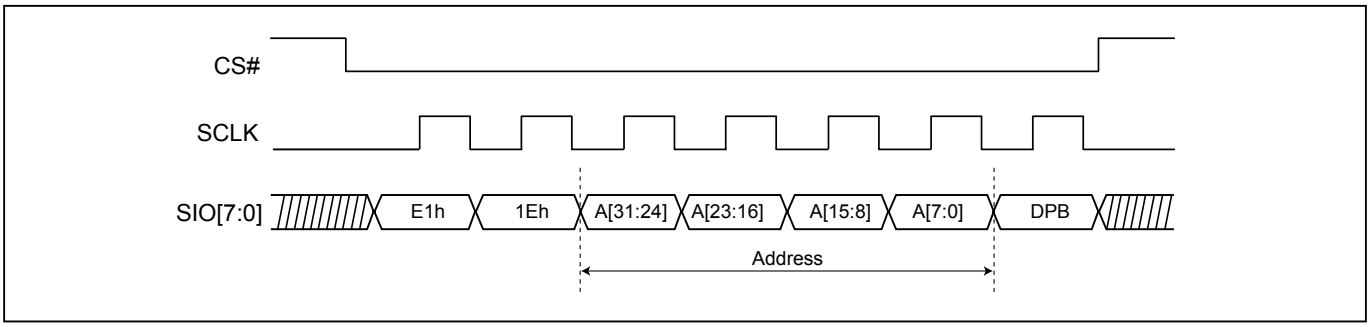
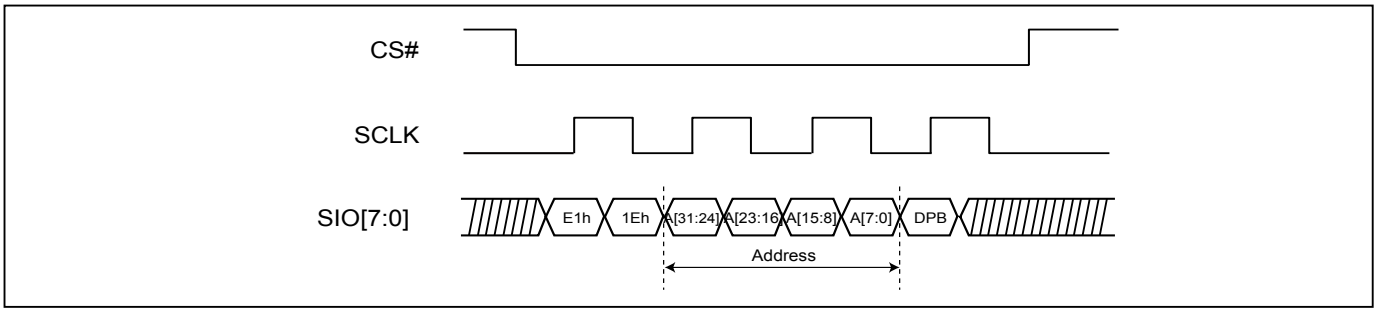


Figure 110. Write DPB Register (WRDPB) Sequence (DTR-OPI Mode)



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10-28-4. Password Protection Mode

Password Protection mode potentially provides a higher level of security than Solid Protection mode. In Password Protection mode, the SPBLKDN bit defaults to "0" after a power-on cycle or reset. When SPBLKDN=0, the SPBs are locked and cannot be modified. A 64-bit password must be provided to unlock the SPBs.

The PASSULK command with the correct password will set the SPBLKDN bit to "1" and unlock the SPB bits. After the correct password is given, a wait of 2us is necessary for the SPB bits to unlock. The Status Register WIP bit will clear to "0" upon completion of the PASSULK command. Once unlocked, the SPB bits can be modified. A WREN command must be executed to set the WEL bit before sending the PASSULK command.

Several steps are required to place the device in Password Protection mode. Prior to entering the Password Protection mode, it is necessary to set the 64-bit password and verify it. The WRPASS command writes the password and the RDPASS command reads back the password. Password verification is permitted until the Password Protection Mode Lock Bit has been written to "0". Password Protection mode is activated by programming the Password Protection Mode Lock Bit to "0". This operation is not reversible. Once the bit is programmed, it cannot be erased. The device remains permanently in Password Protection mode and the 64-bit password can neither be retrieved nor reprogrammed.

The password is all "1's" when shipped from the factory. The WRPASS command can only program password bits to "0". The WRPASS command cannot program "0's" back to "1's". All 64-bit password combinations are valid password options. A WREN command must be executed to set the WEL bit before sending the WRPASS command.

- The unlock operation will fail if the password provided by the PASSULK command does not match the stored password. This will set the P_FAIL bit to "1" and insert a delay before clearing the WIP bit to "0". User has to wait 150us before issuing another PASSULK command. This restriction makes it impractical to attempt all combinations of a 64-bit password (such an effort would take millions of years). Monitor the WIP bit to determine whether the device has completed the PASSULK command.

- When a valid password is provided, the PASSULK command does not insert the delay before returning the WIP bit to zero. The SPBLKDN bit will set to "1" and the P_FAIL bit will be "0".

- It is not possible to set the SPBLKDN bit to "1" if the password had not been set prior to the Password Protection mode being selected.

RDPASS, WRPASS and PASSULK instructions are not allowed while the device is operating in PE mode or Write Register Mode.

Password Register (PASS)

Bits	Field Name	Function	Type	Default State	Description
63 to 0	PWD	Hidden Password	OTP	FFFFFFFFFFFFFFFFh	Non-volatile OTP storage of 64 bit password. The password is no longer readable after the Password Protection mode is selected by programming Lock Register bit 2 to zero.

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Figure 111. Read Password Register (RDPASS) Sequence

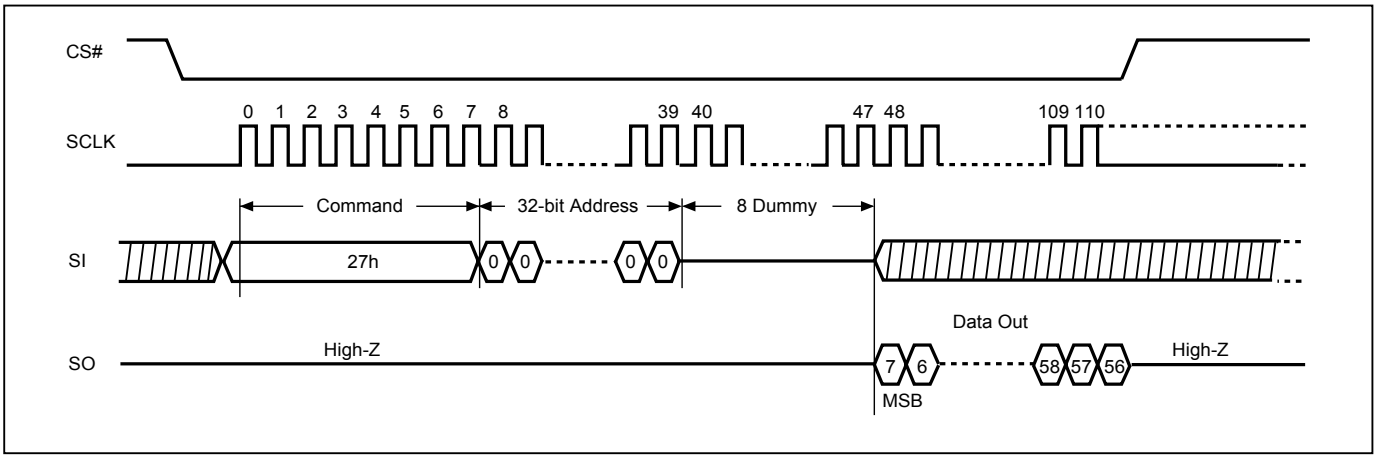


Figure 112. Read Password Register (RDPASS) Sequence (STR-OPI Mode)

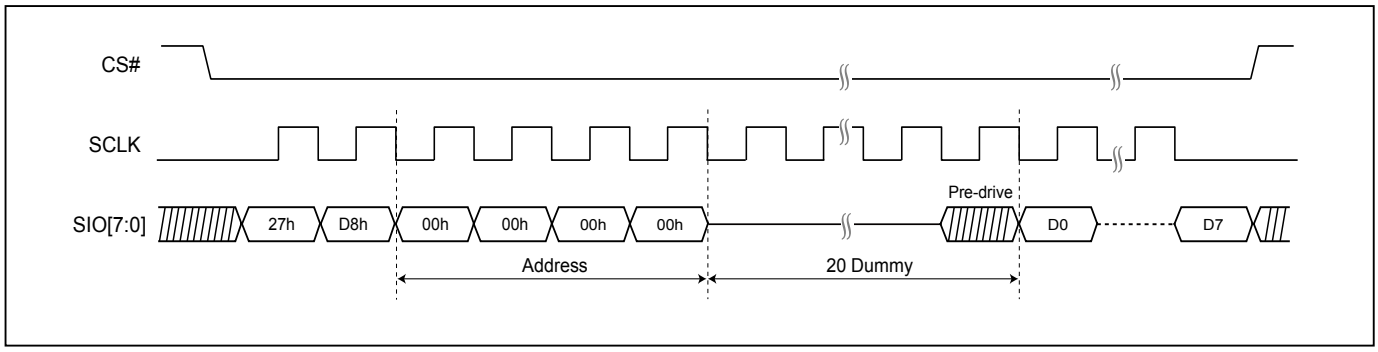
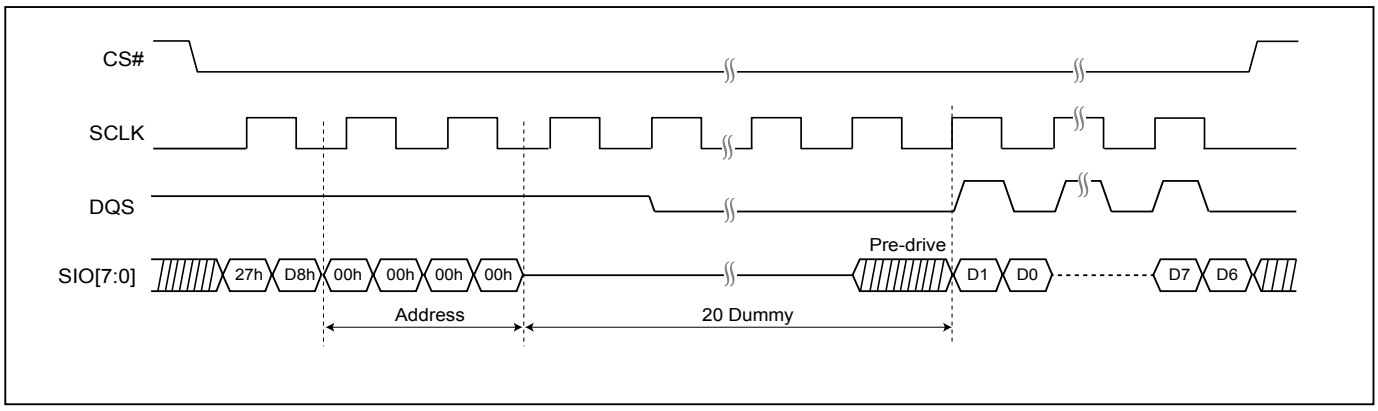


Figure 113. Read Password Register (RDPASS) Sequence (DTR-OPI Mode)



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Figure 114. Write Password Register (WRPASS) Sequence

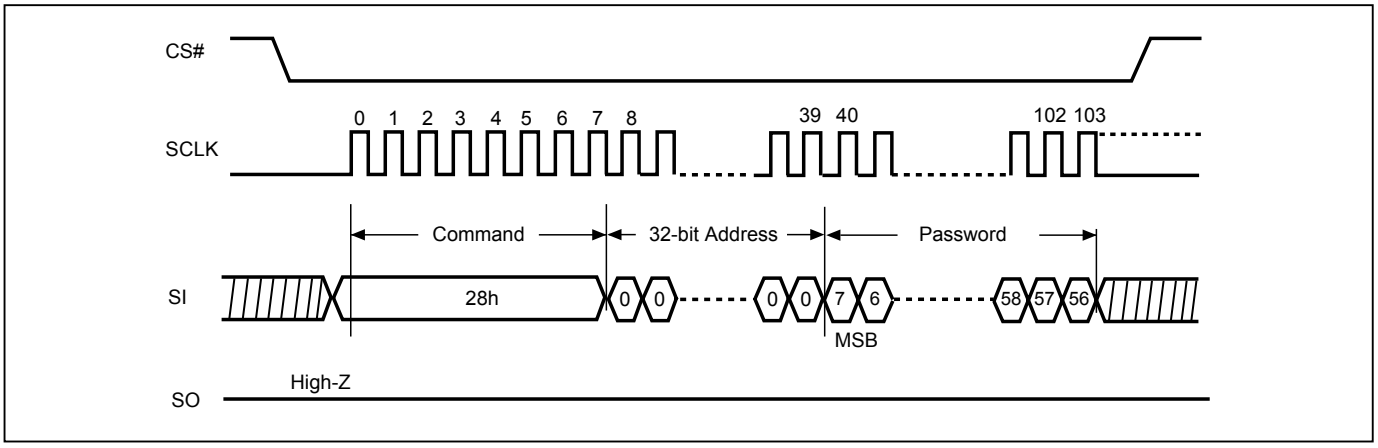


Figure 115. Write Password Register (WRPASS) Sequence (STR-OPI Mode)

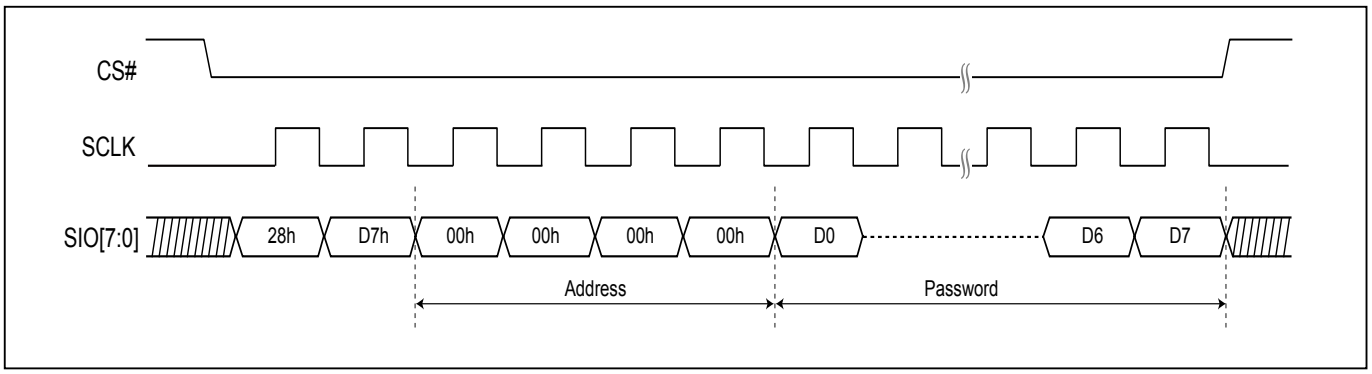
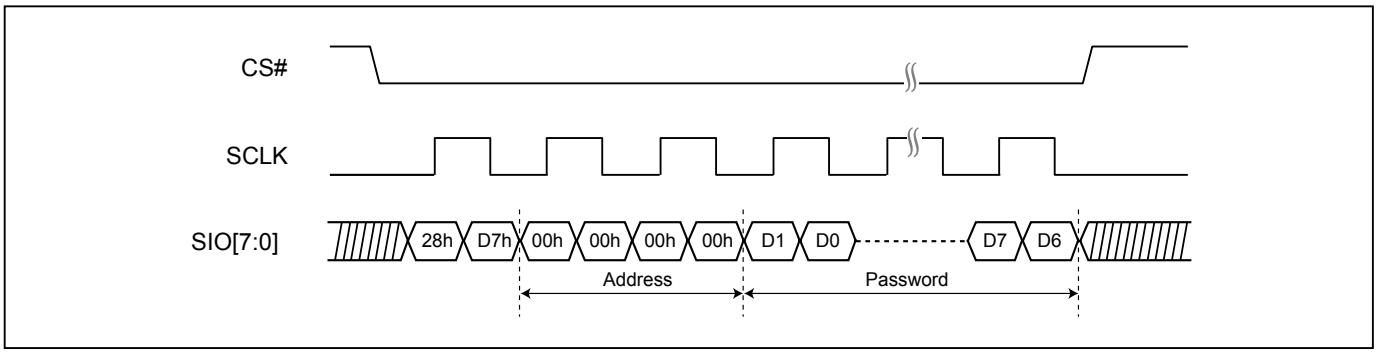


Figure 116. Write Password Register (WRPASS) Sequence (DTR-OPI Mode)



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Figure 117. Password Unlock (PASSULK) Sequence

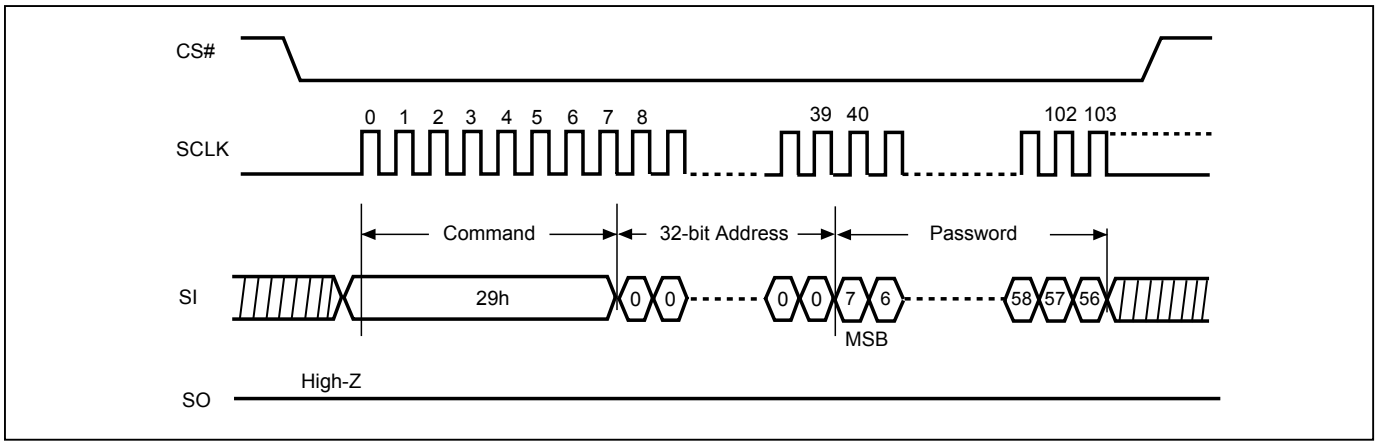


Figure 118. Password Unlock (PASSULK) (STR-OPI Mode)

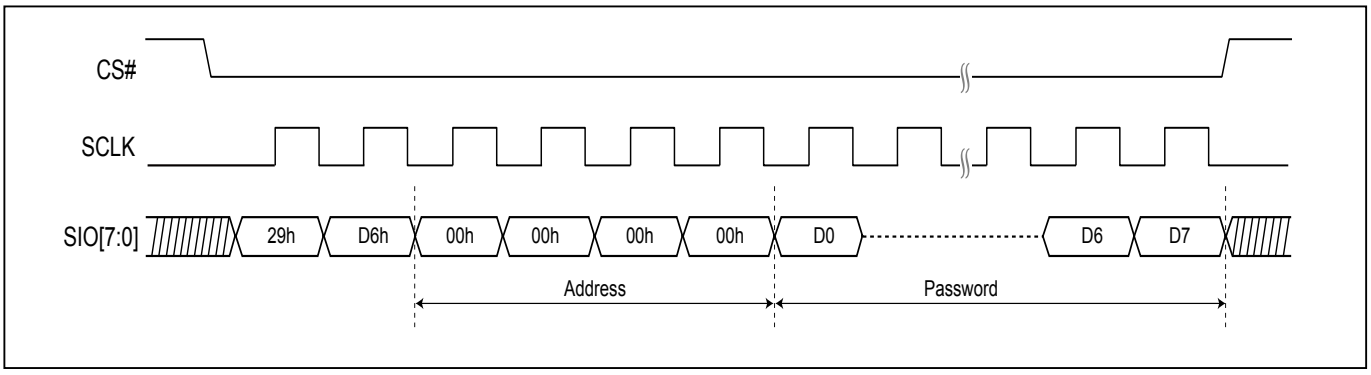
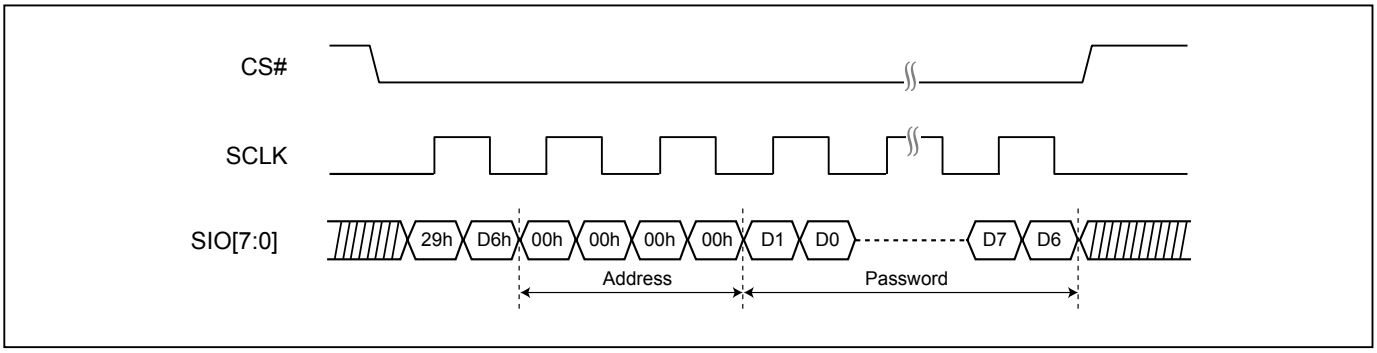


Figure 119. Password Unlock (PASSULK) (DTR-OPI Mode)



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10-28-5. Gang Block Lock/Unlock (GBLK/GBULK)

These instructions are only effective after WPSEL was executed. The GBLK/GBULK instruction is a chip-based protected or unprotected operation. It can enable or disable all DPB.

The WREN (Write Enable) instruction is required before issuing GBLK/GBULK instruction.
The sequence of issuing GBLK/GBULK instruction is: CS# goes low → send GBLK/GBULK (7Eh/98h) instruction →CS# goes high.

The CS# must go high exactly at the byte boundary, otherwise, the instruction will be rejected and not be executed.

GBLK and GBULK instructions are not allowed while the device is operating in PE mode or Write Register Mode.

10-28-6. Sector Protection States Summary Table

Protection Status		Sector State
DPB bit	SPB bit	
0	0	Unprotect
0	1	Protect
1	0	Protect
1	1	Protect

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10-29. Program Suspend and Erase Suspend

The Suspend instruction interrupts a Program or Erase operation to allow the device conduct other operations.

After the device has entered the suspended state, the memory array can be read except for the page being programmed or the sector being erased.

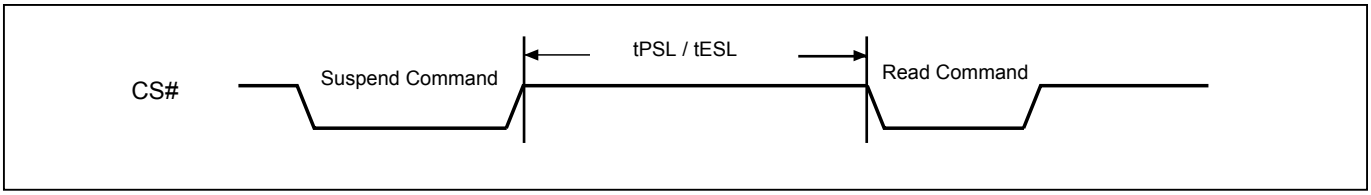
Security Register bit 2 (PSB) and bit 3 (ESB) can be read to check the suspend status. The PSB (Program Suspend Bit) sets to “1” when a program operation is suspended. The ESB (Erase Suspend Bit) sets to “1” when an erase operation is suspended. The PSB or ESB clears to “0” when the program or erase operation is resumed.

When the Serial NOR Flash receives the Suspend instruction, Program Suspend Latency(tPSL) or Erase Suspend latency(tESL) is required to complete suspend operation. (Refer to *"Table 19. AC CHARACTERISTICS"*) After the device has entered the suspended state, the WEL bit is clears to “0” and the PSB or ESB in security register is set to “1”, then the device is ready to acceptanother command.

However, some commands can be executed without tPSL or tESL latency during the program/erase suspend, and can be issued at any time during the Suspend.

Please refer to *"Table 11. Acceptable Commands During Suspend"*.

Figure 120. Suspend to Read Latency



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Table 11. Acceptable Commands During Suspend

Command Name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
Commands which require tPSL/tESL delay			
READ	03h/13h	•	•
FAST_READ	0Bh/0Ch	•	•
8READ	ECh	•	•
8DTRD	EEh	•	•
RDSFDP	5Ah	•	•
RDID	9Fh	•	•
SBL	C0h	•	•
ENSO	B1h	•	•
EXSO	C1h	•	•
WREN	06h	•	•
RESUME	30h	•	•
RDLR	2Dh	•	•
RDSPB	E2h	•	•
RDFBR	16h	•	•
RDDPB	E0h	•	•
RDCR2 with A[31:30]=00/01	71h	•	•
WRCR2 with A[31:30]=00	72h	•	•
WRCR2 with A[31:30]=01			
Commands not required tPSL/tESL delay			
WRDI	04h	•	•
RDSR	05h	•	•
RDCR	15h	•	•
RDCR2 with A[31:30]=10/11	71h	•	•
WRCR2 with A[31:30]=10	72h	•	•
RDSCUR	2Bh	•	•
RSTEN	66h	•	•
RST	99h	•	•
NOP	00h	•	•

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10-30. Program Resume and Erase Resume

The Resume instruction resumes a suspended Program or Erase operation. After the device receives the Resume instruction, the WEL and WIP bits are set to “1” and the PSB or ESB is cleared to “0”.The program or erase operation will continue until it is completed or until another Suspend instruction is received.

To issue another Suspend instruction, the minimum resume-to-suspend latency (tPRS or tERS) is required. However, in order to finish the program or erase progress, a period equal to or longer than the typical timing is required.

To issue other command except suspend instruction, a latency of the self-timed Page Program Cycle time (tPP) or Sector Erase (tSE) is required. The WEL and WIP bits are cleared to “0” after the Program or Erase operation is completed.

Figure 121. Resume to Read Latency

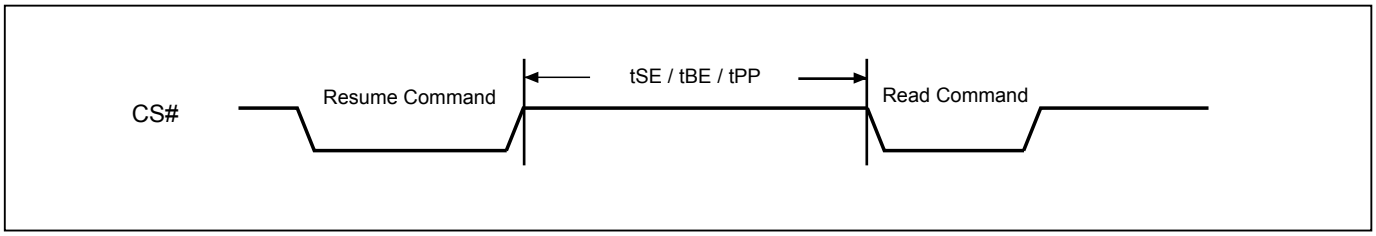
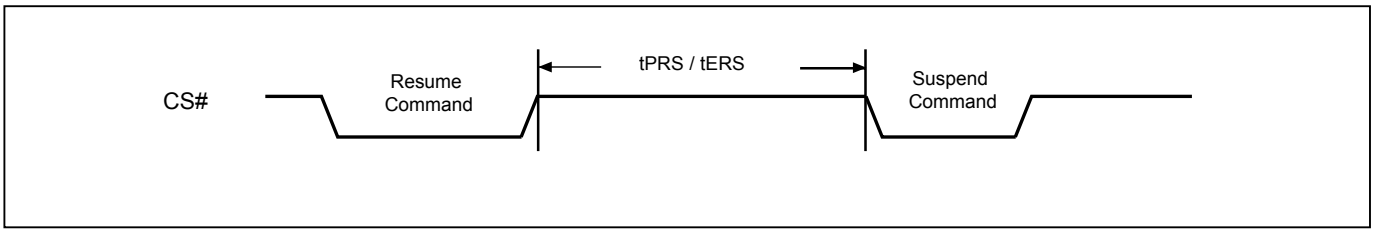


Figure 122. Resume to Suspend Latency



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10-31. No Operation (NOP)

The “No Operation” command is only able to terminate the Reset Enable (RSTEN) command and will not affect any other command.

10-32. Software Reset (Reset-Enable (RSTEN) and Reset (RST))

The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command following a Reset (RST) command. It returns the device to a standby mode. All the volatile bits and settings will be cleared then, which makes the device return to the default status as power on.

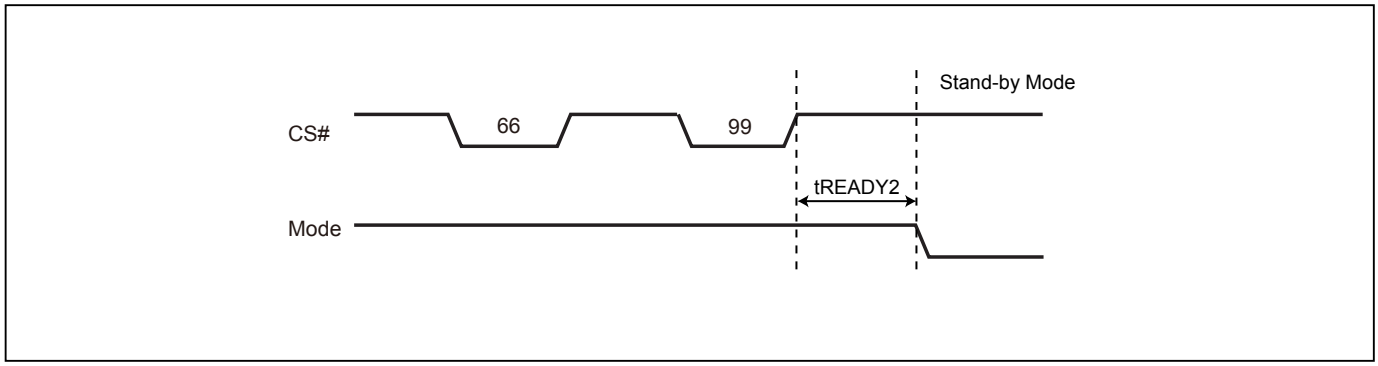
To execute Reset command (RST), the Reset-Enable (RSTEN) command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the Reset-Enable will be invalid.

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged or lost.

The reset time is different depending on the last operation. For details, please refer to *"Table 15. Reset Timing-(Other Operation)"* for tREADY2.

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Figure 123. Software Reset Recovery



Note: Refer to *"Table 15. Reset Timing-(Other Operation)"* for tREADY2.

Figure 124. Reset Sequence (SPI mode)

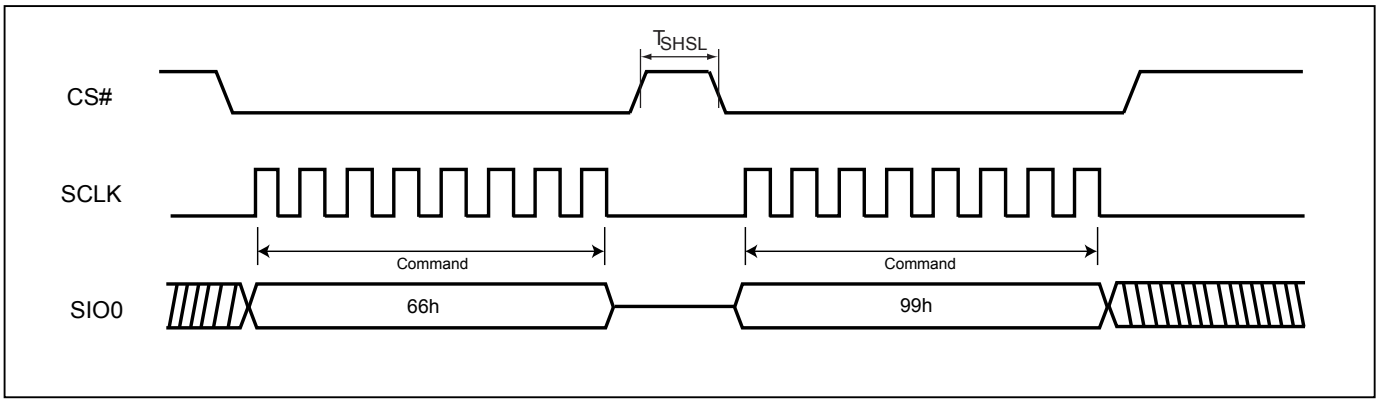


Figure 125. Reset Sequence (STR-OPI mode)

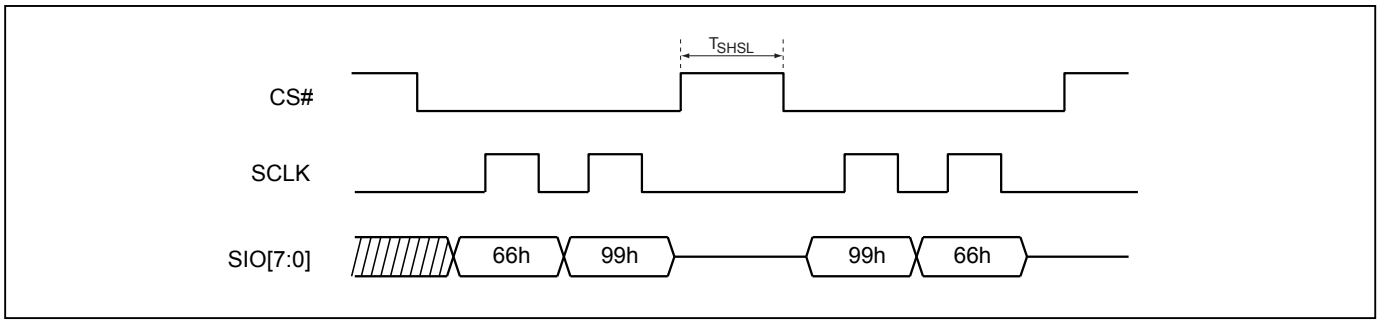
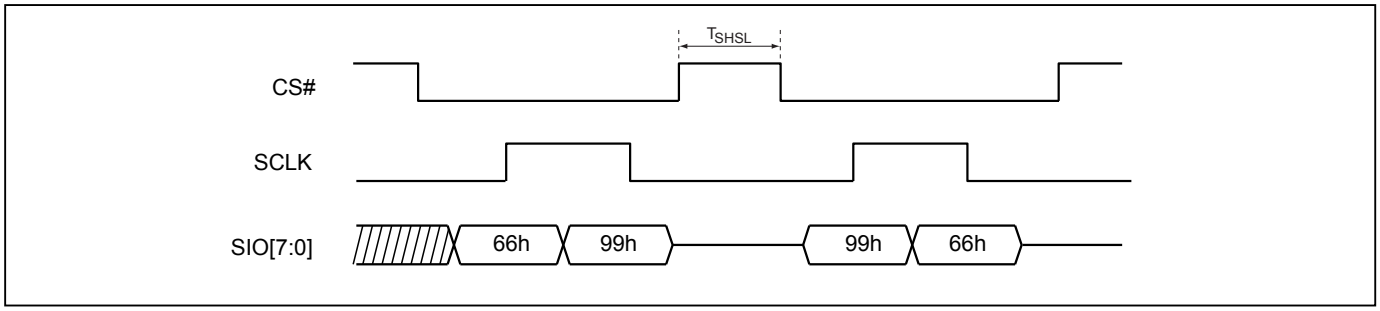


Figure 126. Reset Sequence (DTR-OPI mode)



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11. Serial Flash Discoverable Parameter (SFDP)

11-1. Read SFDP Mode (RDSFDP)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

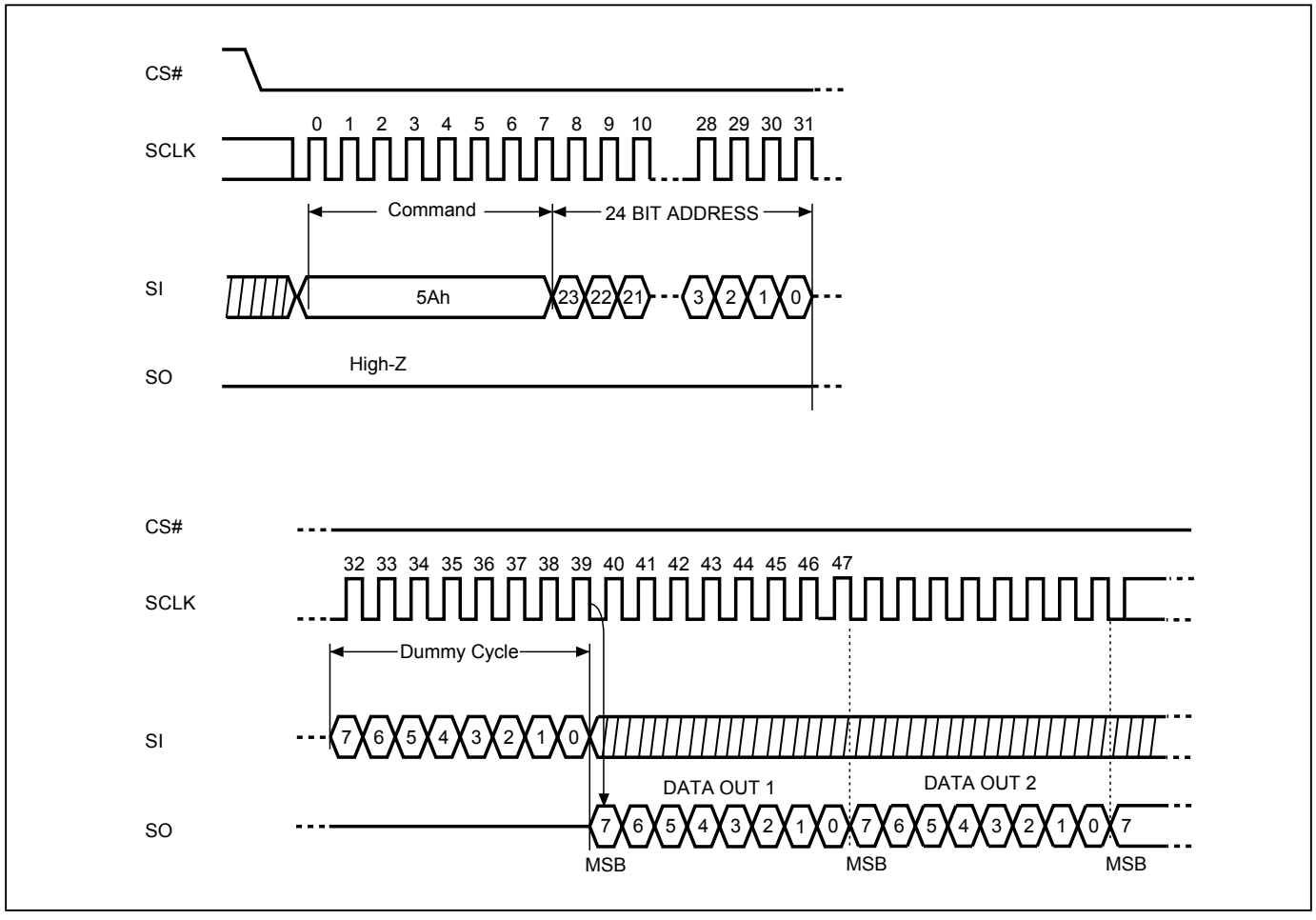
The sequence of issuing RDSFDP instruction in SPI is CS# goes low→send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→ send 8 dummy cycles → read SFDP code on SO→to end RDSFDP operation can use CS# to high at any time during data out.

SFDP in SPI is a JEDEC standard, JESD216D.

The sequcn of issuing RDSFDP instruction in OPI/DOPI mode:
CS# low → send RDSFDP instruction (5Ah/A5h) → send 4 address bytes on SIO pin→ send 20 dummy cycles → read SFDP code on SIO[7:0] → to end RDSFDP operation can use CS# to high at any time during data out.

RDSFDP instruction is not allowed while the device is operating in PE mode or Write Register Mode.

Figure 127. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence



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Figure 128. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence (STR-OPI Mode)

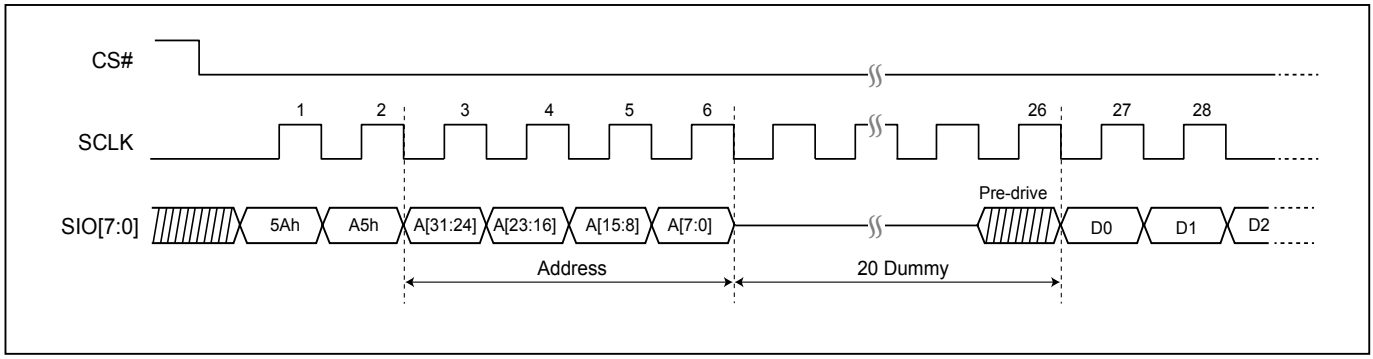
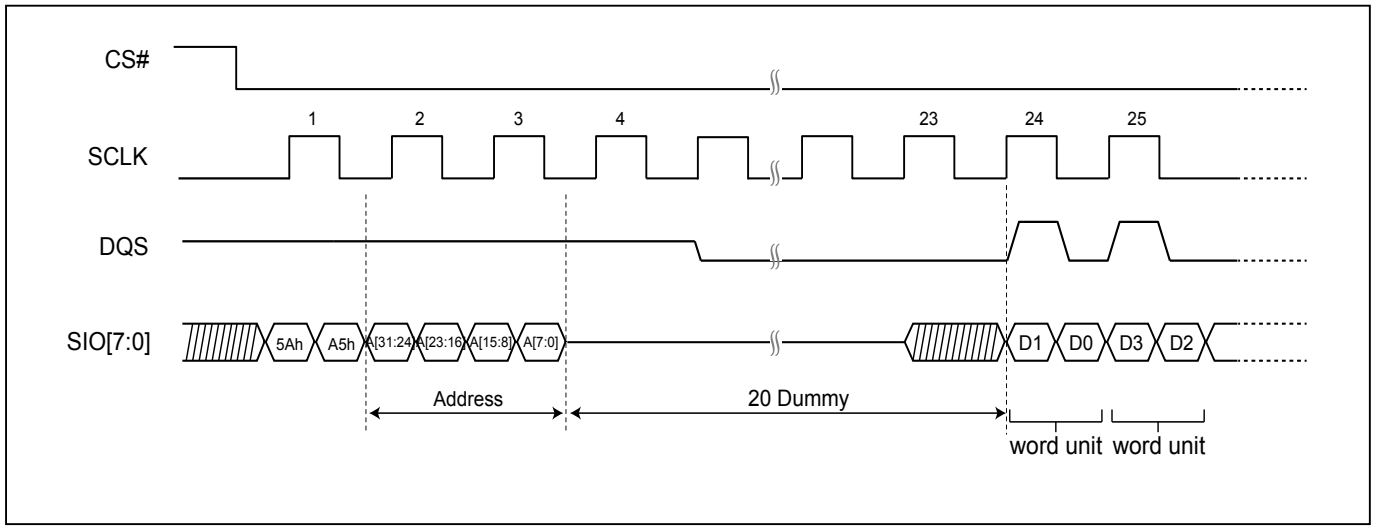


Figure 129. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence (DTR-OPI Mode)



Note: Address must be low byte (A0=0) in DTR OPI.

Table 12. Signature and Parameter Identification Data Values

For SFDP register values detail, please contact local Macronix sales channel for Application Note.

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12. Data Integrity check

The data storage and transmission errors will cause unexpected Flash device variation that makes a harmful impact on overall system functions. To prevent these errors, MX25LW51245G product provides advanced Data Integrity Check function. For the data storage and data transmission in the flash device, Data Integrity Check can check errors and correct them, allowing self-checking and preventing errors in advance.

The Data Integrity Check function includes two methods:

- ECC (Error Checking and Correcting): to prevent the data storage errors

- Parity Check (CRC1): to prevent the data transmission errors

The status register data and software signals can also be used to associate the Data Integrity Check function to fully record the results of checking, and can also immediately feedback.

12-1. ECC (Error Checking and Correcting)

Macronix Serial Octa SPI Flash have built-in ECC. The ECC algorithm uses a Hamming code that can correct a single bit error per 16-Byte chunk. During a page program operation, the internal state machine will create the ECC automatically. During a read operation, the internal ECC state machine corrects bit errors automatically.

It is recommended that data be programmed in multiples of 16 bytes in the predefined 16-byte chunk address (see *"Table 13. 16-Byte Chunks within a Page"*) using the Page Program command instead of programming a byte or a word at a time using the Program command. However, partial program of 16-byte chunk is allowed under the restriction that user won't program or alter the content of partially programmed chunk without erasing the sector first.

ECC checking of a 16-Byte chunk will be disabled if double program (rewriting without erase), or rewrite a chunk (alternating of single bit, byte, or word) happens in that chunk. Once ECC checking of a chuck is disabled, it will not be re-activated until the sector, containing the ECC disabled chunk, is erased.

The ECC registers show detailed information for error correction activity on the device. The ECC status registers are placed on CR2. Which include 3-bit ECC status to identify the error type, 4-bit failure chunk counter and first failure chunk address.

The ECC register can be reset through either of the following situations:

- Write "00" data into ECC status register
- Issuing Software Reset Command
- Hardware Reset
- Power-up cycle

Table 13. 16-Byte Chunks within a Page

Chunk#	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
16 Bytes	B0 ~B15	B16 ~B31	B32 ~B47	B48 ~B63	B64 ~B79	B80 ~B95	B96 ~B111	B112 ~B127	B128 ~B143	B144 ~B159	B160 ~B175	B176 ~B191	B192 ~B207	B208 ~B223	B224 ~B239	B240 ~B255

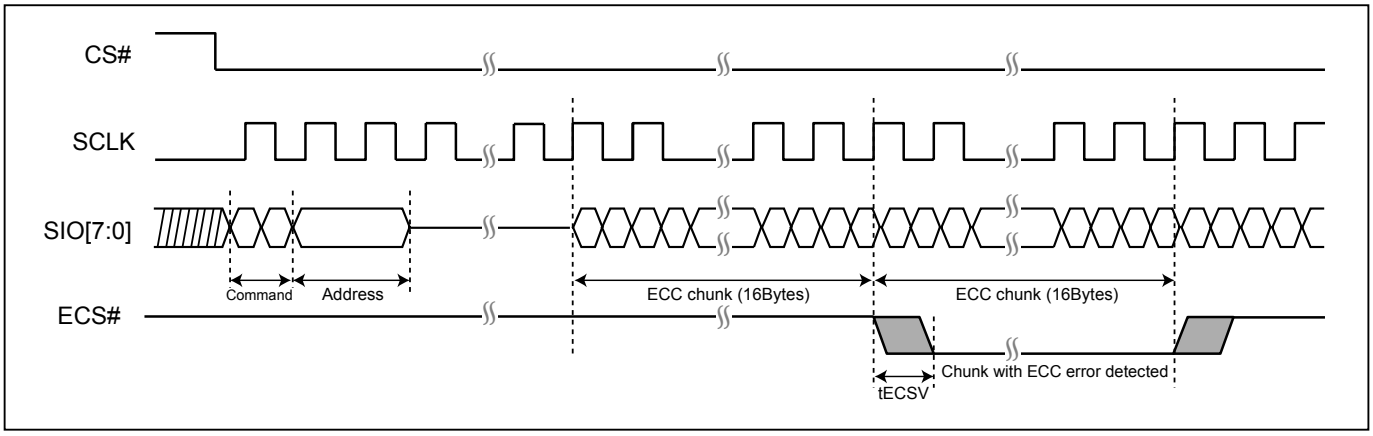
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12-2. ECS# (Error corrected Signal) Pin

The ECS# pin is a real time hardware signal to feedback the ECC correction status. The ECS# pin is designed as an open drain structure. In normal situation, the ECS# is kept on Hi-Z state. Once error correction begins, the ECS# pin will pull low during the whole ECC chunk unit after a duration of tECSV delay timing.

The ECS# pin is default as going low when 2-bit error detection is enabled and double program detected. However, user can select the different option for error correction by setting the ECS register in CR2 [00000400h].

Figure 130. ECS# Timing



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12-3. Parity Check (CRC1)

The parity check function can only be operated at DTR OPI mode, it does not support OPI mode. The CRCEN# bit in CR2 [address 40000000h] bit3 can enable the parity check function. CRCEN# is an OTP bit; once it is programmed to "0", it cannot be disabled anyhow.

For write operation after the Parity check function is enabled, the CRC code needs to be set after the address and data cycles. The starting address for the Flash device has to be issued at CRC chunk boundary, and the data CRC bit also should be output by each CRC chunk unit. Otherwise, read CRC code might be error; and program command would abort.

There is a bit [CR2 00000500h] that output data is CRC on both clock edges, or is CRC/CRC# on clock rising/ falling edge respectively. The CRC chunk unit is default to set as 16bytes. It can also configure the chunk unit to 32bytes, 64bytes or 128bytes by CRC register setting in CR2 [address 00000500h].

For register write, an extra DATA# cycle must be set right after data cycle as in *"Figure 134. CRC Timing (Write Register - example for 1byte data)"*.
For register read, an extra DATA# would be output after the data cycle as in *"Figure 135. CRC Timing (Read register - example for 1byte data)"*.

The address CRC byte is calculated by bitwise exclusive-OR of all the address bytes; the data CRC bytes are calculated by bitwise exclusive-OR of all the data bytes in the CRC chunk.

Figure 131. CRC Timing (Without CRC# output)

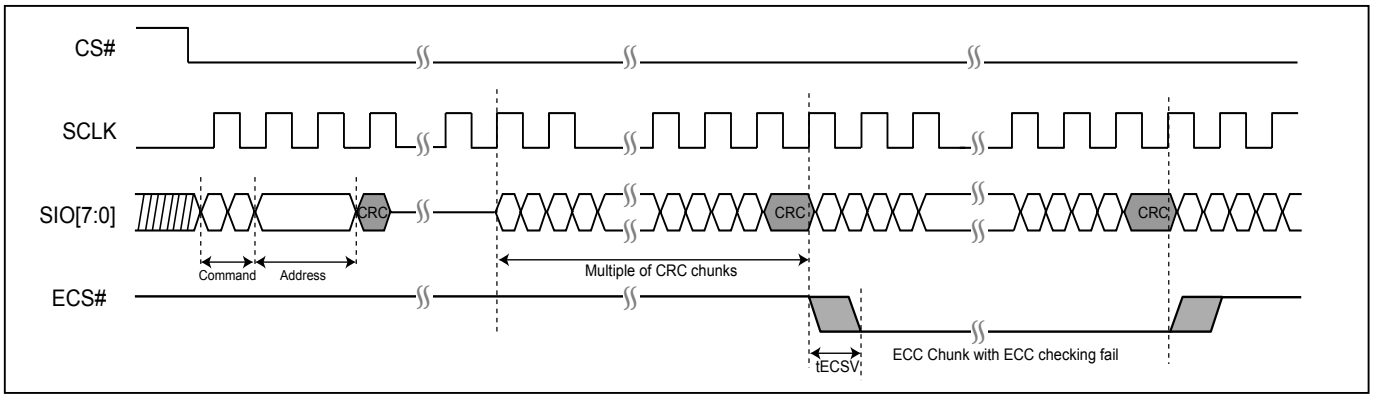
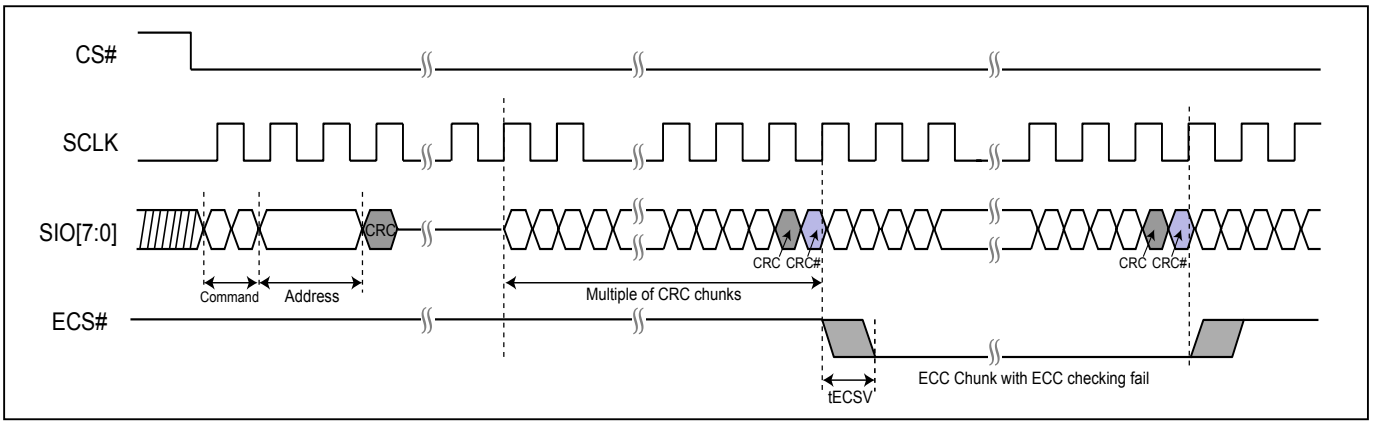


Figure 132. CRC Timing (With CRC# output)



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Figure 133. CRC Timing (Page Program)

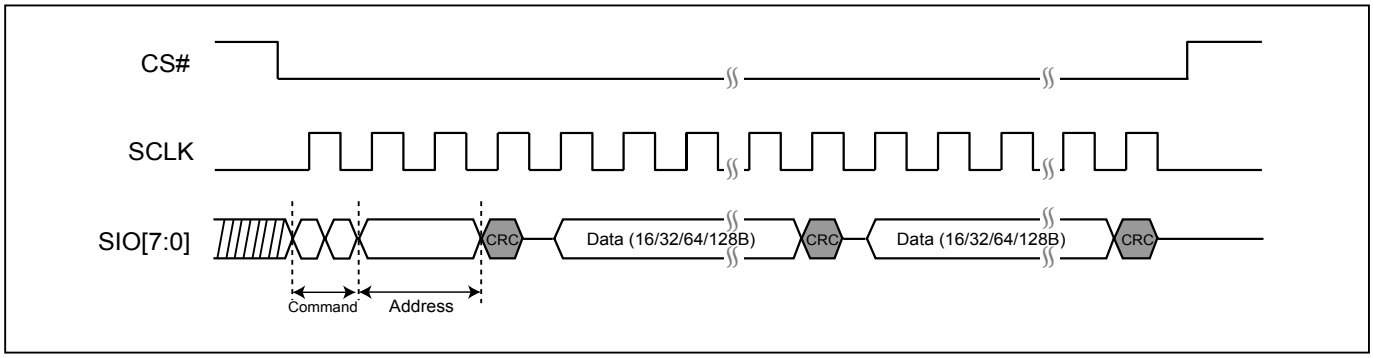


Figure 134. CRC Timing (Write Register - example for 1byte data)

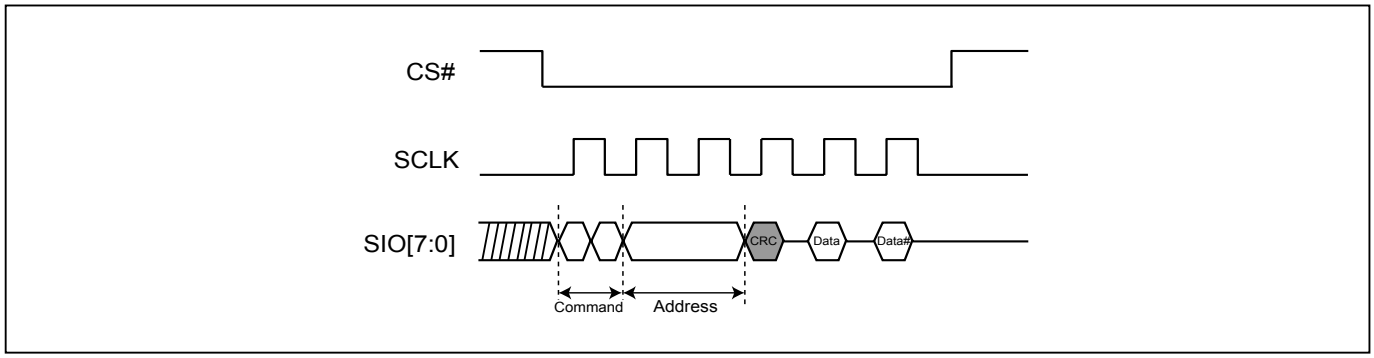
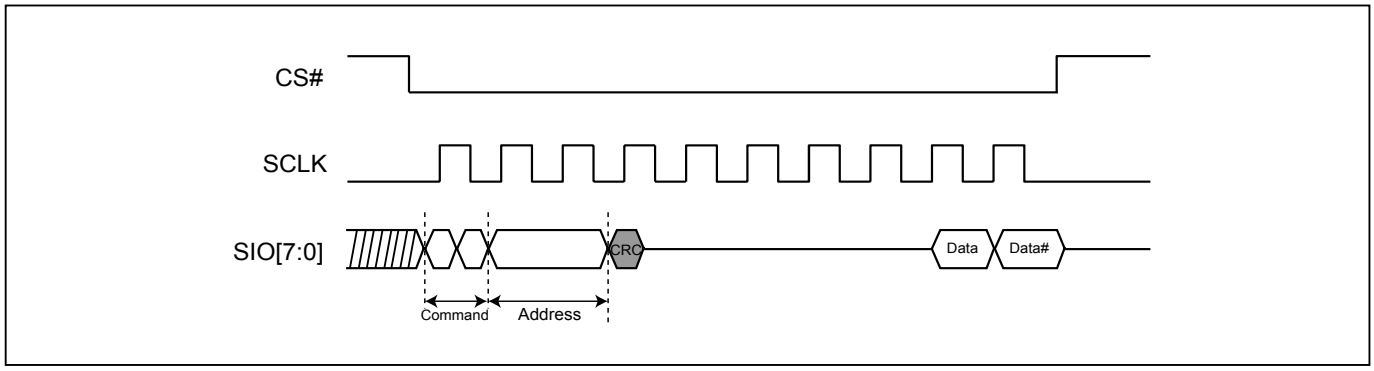


Figure 135. CRC Timing (Read register - example for 1byte data)



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Figure 136. CRC Timing (RDPASS)

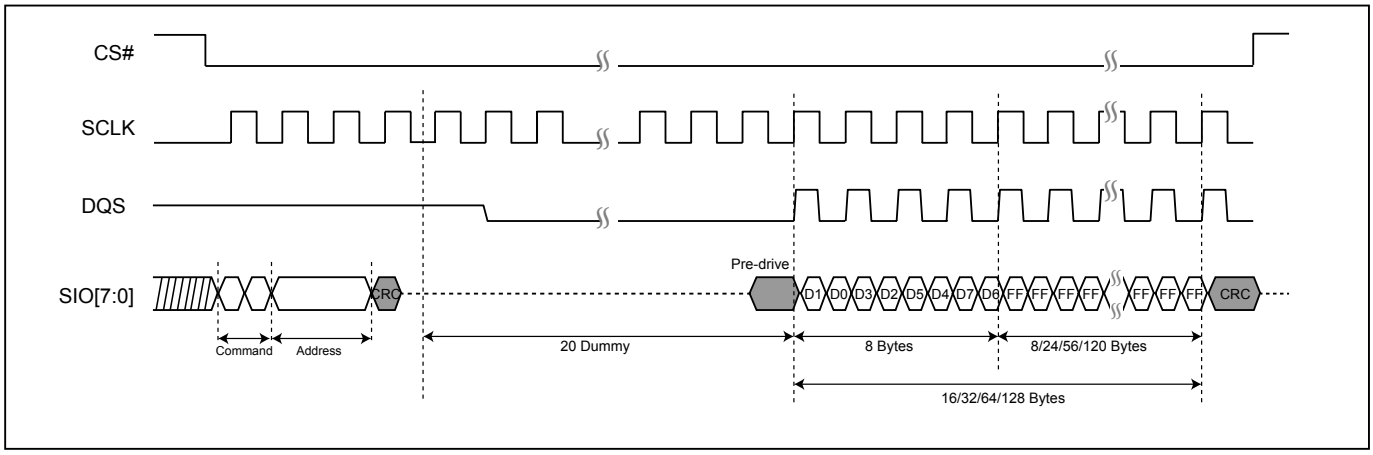


Figure 137. CRC Timing (WRPASS/PASSULK)

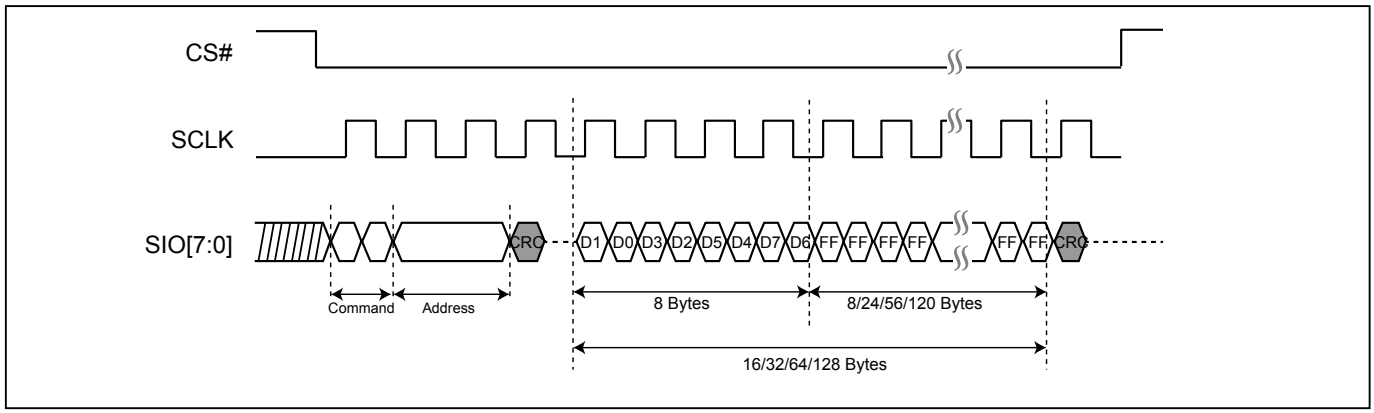
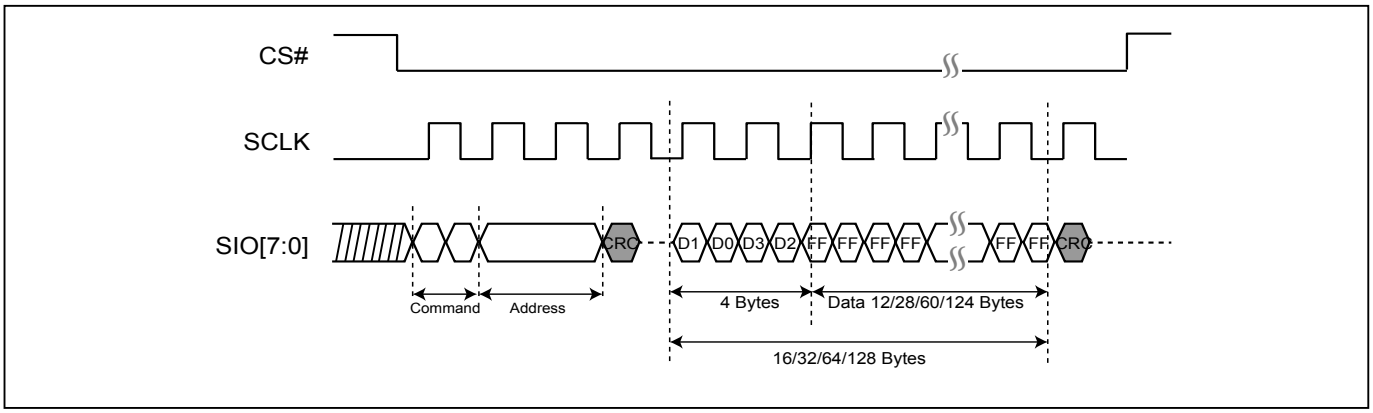


Figure 138. CRC Timing (WRFBR)



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13. RESET

Driving the RESET# pin low for a period of tRLRH or longer will reset the device. After reset cycle, the device is at the following states:
- Standby mode
- All the volatile bits such as WEL/WIP will return to the default status as power on.
- All the volatile bits in CR2 will return to the default status as power on.
- Fastboot read will be executed on first CS# pin goes low

If the device is under programming or erasing, driving the RESET# pin low will also terminate the operation and data could be lost. During the resetting cycle, the SIO data becomes high impedance and the current will be reduced to minimum.

Figure 139. RESET Timing

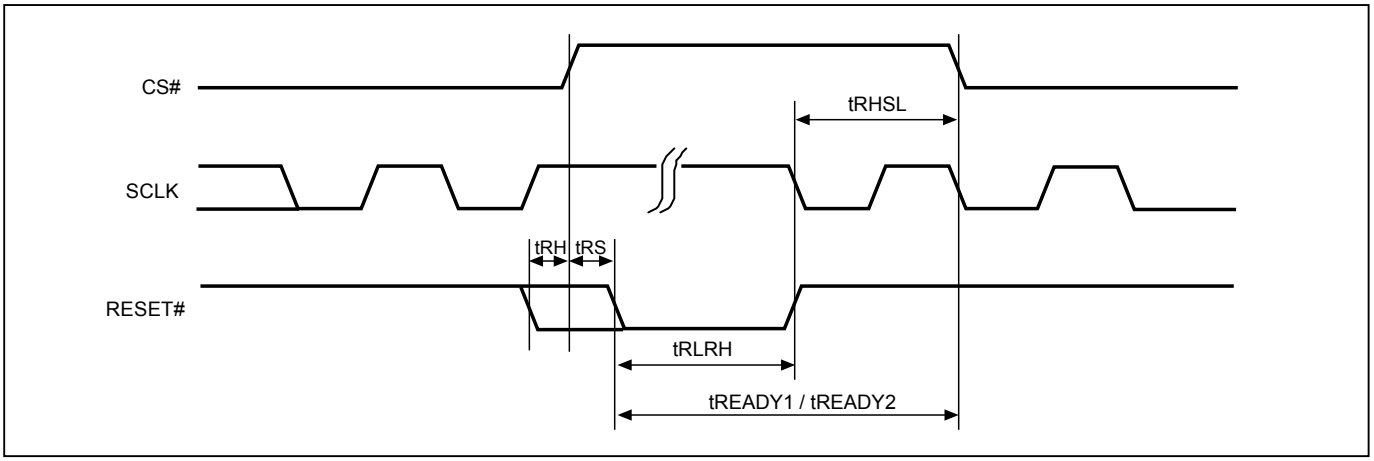


Table 14. Reset Timing-(Standby)

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRHSL	Reset# high before CS# low	10			us
tRS	Reset# setup time	15			ns
tRH	Reset# hold time	15			ns
tRLRH	Reset# low pulse width	10			us
tREADY1	Reset Recovery time	35			us

Table 15. Reset Timing-(Other Operation)

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRHSL	Reset# high before CS# low	10			us
tRS	Reset# setup time	15			ns
tRH	Reset# hold time	15			ns
tRLRH	Reset# low pulse width	10			us
tREADY2	Reset Recovery time (During instruction decoding)	40			us
	Reset Recovery time (for read operation)	40			us
	Reset Recovery time (for program operation)	310			us
	Reset Recovery time(for SE4KB operation)	12			ms
	Reset Recovery time (for BE64K operation)	25			ms
	Reset Recovery time (for Chip Erase operation)	100			ms
	Reset Recovery time (for WRSR operation)	40			ms

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14. POWER-ON STATE

The device is at below states when power-up:
- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level:
- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When VCC is lower than VWI (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The write, erase, and program command should be sent after the below time delay:
- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.
Please refer to the "*"Power-up Timing"*".

Note:
- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)
- At power-down stage, the VCC drops below VWI level, all operations are disable and device has no response to any command. The data corruption might occur during the stage while a write, program, erase cycle is in progress.
- To stabilize the VCCQ level, the VCCQ/VSSQ rail decoupled by a suitable capacitor close to package pins is recommended. One VCCQ pin connect to one capacitor.
- It is recommended VCC and VCCQ power are separated system supply with same supply voltage.

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15. ELECTRICAL SPECIFICATIONS

Table 16. ABSOLUTE MAXIMUM RATINGS

RATING		VALUE
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.5V to VCC+0.5V
Applied Output Voltage		-0.5V to VCC+0.5V
VCC to Ground Potential		-0.5V to 4.0V

NOTICE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot to VCC+1.0V or -1.0V for period up to 20ns.

Figure 140. Maximum Negative Overshoot Waveform

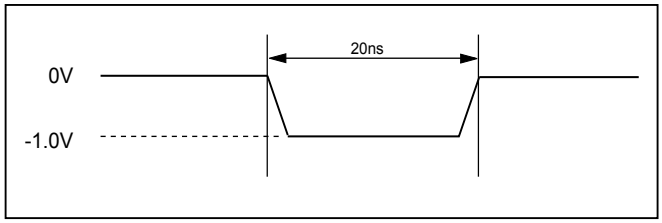


Figure 141. Maximum Positive Overshoot Waveform

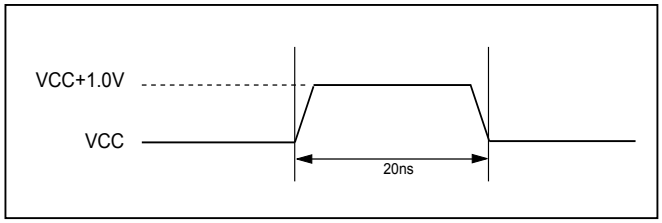


Table 17. CAPACITANCE TA = 25°C, f = 1.0 MHz

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			8	pF	VIN = 0V
COUT	Output Capacitance			12	pF	VOUT = 0V

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Figure 142. DATA INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL

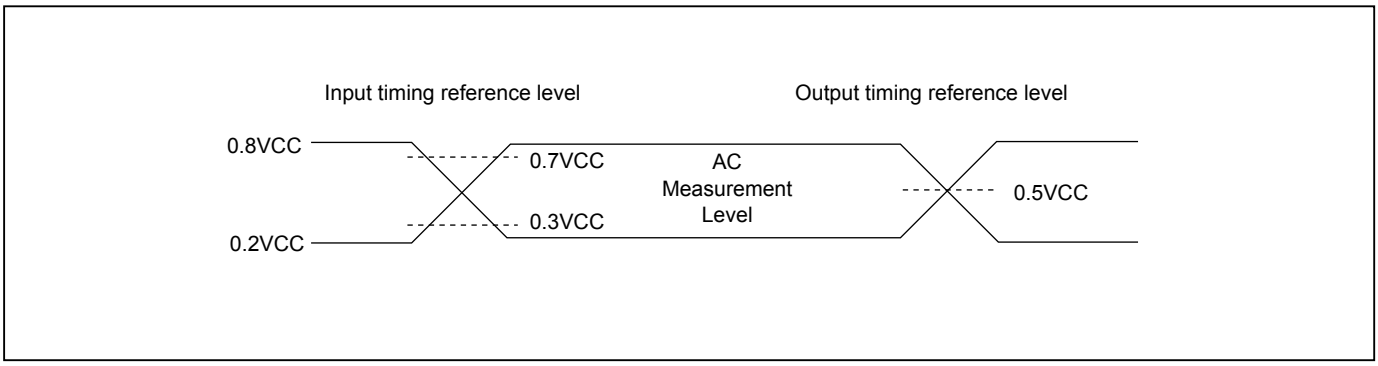
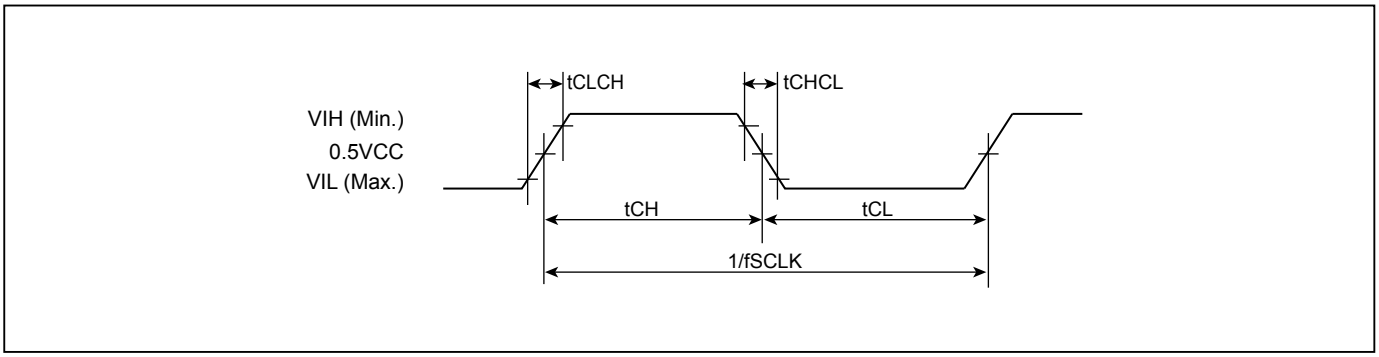


Figure 143. SCLK TIMING DEFINITION



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Table 18. DC CHARACTERISTICS

Temperature = -40°C to 85°C, VCC = 2.7V ~ 3.6V

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units	Test Conditions
ILI	Input Load Current	1			±2	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1			±2	uA	VCC = VCC Max, VOUT = VCC or GND
ISB1	VCC Standby Current	1		35	180	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			25	80	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1,3		20	40	mA	100MHz 8IO STR (SIO floating)
				30	45	mA	100MHz 8IO DTR (SIO floating)
				25	50	mA	133MHz 8IO STR (SIO floating)
				40	60	mA	133MHz 8IO DTR (SIO floating)
ICC2	VCC Program Current	1		30	40	mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current			20	40	mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector Erase Current (SE)	1		20	40	mA	Erase in Progress, CS#=VCC
ICC4	VCC Block Erase Current (BE)	1		30	40	mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		20	40	mA	Erase in Progress, CS#=VCC
ICC6	VCC Read While Write Current	1,3		50	80	mA	100MHz 8IO STR (SIO floating)
				60	85	mA	100MHz 8IO DTR (SIO floating)
				55	90	mA	133MHz 8IO STR (SIO floating)
				70	100	mA	133MHz 8IO DTR (SIO floating)
VIL	Input Low Voltage		-0.4		0.3VCC	V	
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.2	V	IOL=100uA
VOH	Output High Voltage		VCC-0.2			V	IOH=-100uA

Notes :
1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.
3. VCC current only; not include VCCQ current.

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Table 19. AC CHARACTERISTICS

Symbol	Alt.	Parameter		Min.	Typ.	Max.	Unit
fSCLK	fC	Clock frequency for SPI commands (except Read operation)				133	MHz
		Clock frequency for OPI commands				133	MHz
fRSCLK	fR	Clock Frequency for READ instructions				50	MHz
fTSCLK		Clock Frequency for FAST READ				133	MHz
		Clock Frequency for 8READ, 8DTRD		*"9-3-1. Dummy Cycle and Frequency Table (MHz)"*			MHz
tCH(1)	tCLH	Clock High Time		0.45*T			ns
tCL(1)	tCL	Clock Low Time		0.45*T			ns
tCLCH/ tCHCL		Clock Rise Time / Clock Fall Time	fSCLK ≤ 100MHz	1			V/ns
			fSCLK ≤ 133MHz	1.4			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)		4.5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)		3			ns
tSHSL	tCSH	CS# Deselect Time	From Read to next Read	10			ns
			From Write/Erase/Program to Read Status Register	40			ns
tDVCH	tDSU	Data In Setup Time (10)	STR	2			ns
tDVCH / tDVCL		Data setup time (9) (10)	DTR	1			ns
tCHDX	tDH	Data In Hold Time (10)	STR	2			ns
tCHDX / tCLDX		Data hold time (9) (10)	DTR	1			ns
tCHSH		CS# Active Hold Time (relative to SCLK)	STR	3			ns
tCLSH		CS# active hold time	DTR	3			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)	STR	3			ns
			DTR	3			ns
tSHQZ	tDIS	Output Disable Time				8	ns
tQSV		Clock transient to DQS valid time				9	ns
tCLQV / tCHQV	tV	Clock transient to Output Valid	Loading: 12pF	1.8		5.2	ns
			Loading: 15pF	1.8		5.3	
			Loading: 20pF	1.8		5.5	
			Loading: 30pF	1.8		5.8	
tCLQX	tHO	Output Hold Time		1		4.1	ns
tDQSQ		SIO valid skew related to DQS	Loading: 12pF(10)			0.7	ns
			Loading: 15pF(10)			0.75	
			Loading: 20pF(10)			0.8	
			Loading: 30pF(10)			0.9	
tQH		SIO hold time related to DQS		min(tCL,tCH)-tQHS			ns
tQHS		SIO hold skew factor	Loading: 12pF(10)			0.75	ns
			Loading: 15pF(10)			0.80	
			Loading: 20pF(10)			0.85	
			Loading: 30pF(10)			1	
tECSV		ECS go low time	Loading: 30pF(10)			10	ns

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AC CHARACTERISTICS - continued

Symbol	Alt.	Parameter	Min.	Typ.	Max.	Unit
tDP		CS# High to Deep Power-down Mode			10	us
tRES1		CS# High to Standby Mode			60	us
tCRDP		CS# Toggling Time before Release from Deep Power-Down Mode	20			ns
tW		Write Status/Configuration Register Cycle Time			40	ms
tW2V		Write Configuration Register 2 volatile bit		40		ns
tW2N(10)		Write Configuration Register 2 non-volatile bit			60	us
tESL(6)		Erase Suspend Latency			50	us
tPSL(6)		Program Suspend Latency			25	us
tPRS(7)		Latency between Program Resume and next Suspend	0.3	175		us
tERS(8)		Latency between Erase Resume and next Suspend	0.3	400		us

Symbol	Alt.	Parameter	Min.	Typ.	Max.	Unit
tPP(4)		Page Program Cycle Time		0.15	0.75	ms
tSE		Sector Erase Cycle Time		25	400	ms
tBE		Block Erase (64KB) Cycle Time		250	2000	ms
tCE		Chip Erase Cycle Time		150	300	s

Symbol	Alt.	Parameter		Min.
tDV		Data valid window	DTR	min(tCH,tCL) - max(tCLQV(max) - tCLQX(max), tCLQV(min) - tCLQX(min))
			STR	min(tSCLK) - max(tCLQV(max) - tCLQX(max), tCLQV(min) - tCLQX(min))

Notes:

1. tCH + tCL must be greater than or equal to 1/ Frequency.
2. Typical values given for TA=25°C. Not 100% tested.
3. Test condition is shown as *Figure 142*.
4. While programming consecutive bytes, Page Program instruction provides optimized timings by selecting to program the whole 256 bytes or only a few bytes between 1~256 bytes.
5. By default dummy cycle value. Please refer to the *"Table 1. Operating Frequency Comparison"*.
6. Latency time is required to complete Erase/Program Suspend operation until WIP bit is "0".
7. For tPRS, minimum timing must be observed before issuing the next program suspend command. However, a period equal to or longer than the typical timing is required in order for the program operation to make progress.
8. For tERS, minimum timing must be observed before issuing the next erase suspend command. However, a period equal to or longer than the typical timing is required in order for the erase operation to make progress.
9. tDVCH+tCHDX>1.5ns for each SIO; tDVCL+tCLDX>1.5ns for each SIO.
10. Sampled, not 100% tested.

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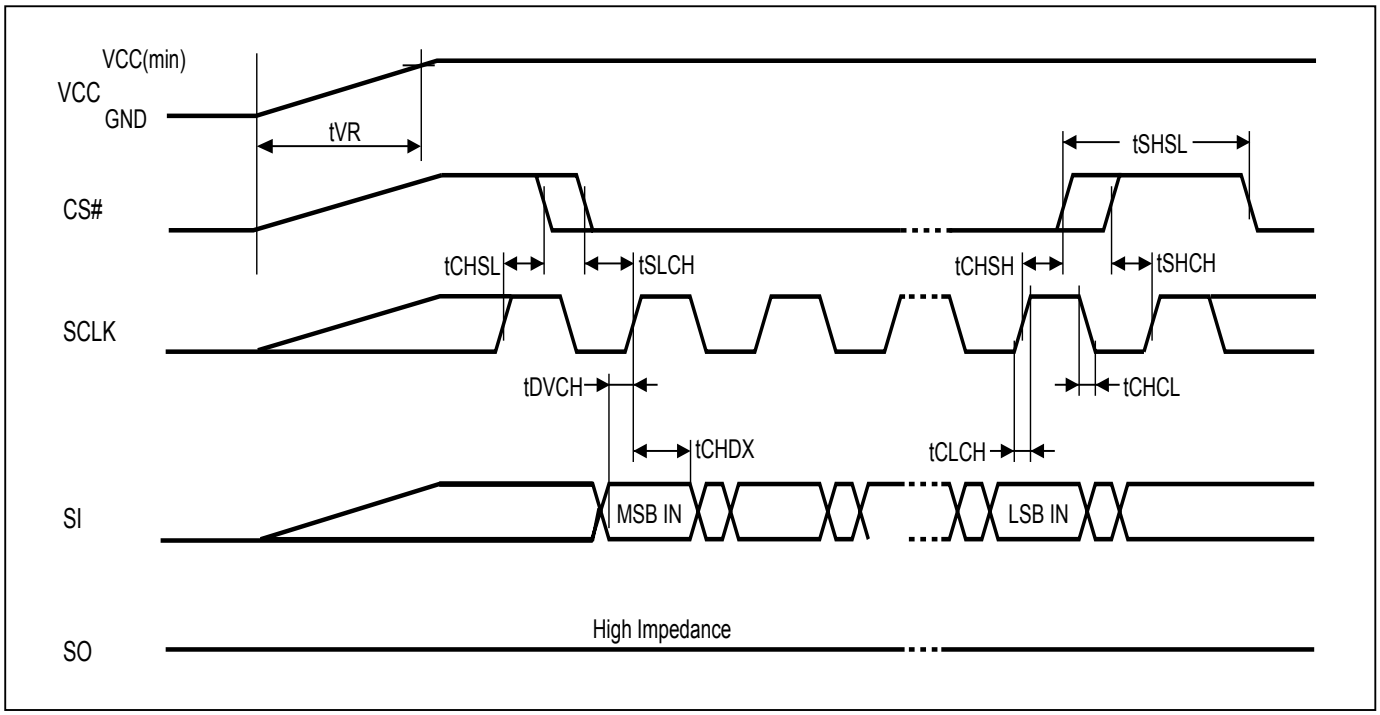
16. OPERATING CONDITIONS

At Device Power-Up and Power-Down

AC timing illustrated in *Figure 144* and *Figure 145* are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 144. AC Timing at Device Power-Up



Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1		500000	us/V

Notes :
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to *Table 19.* AC CHARACTERISTICS.

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Figure 145. Power-Down Sequence

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.

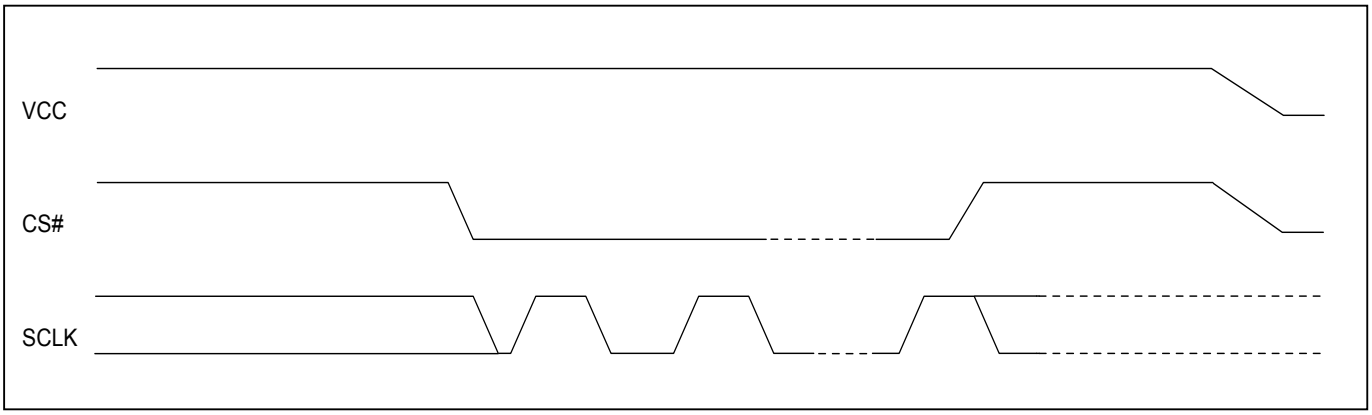
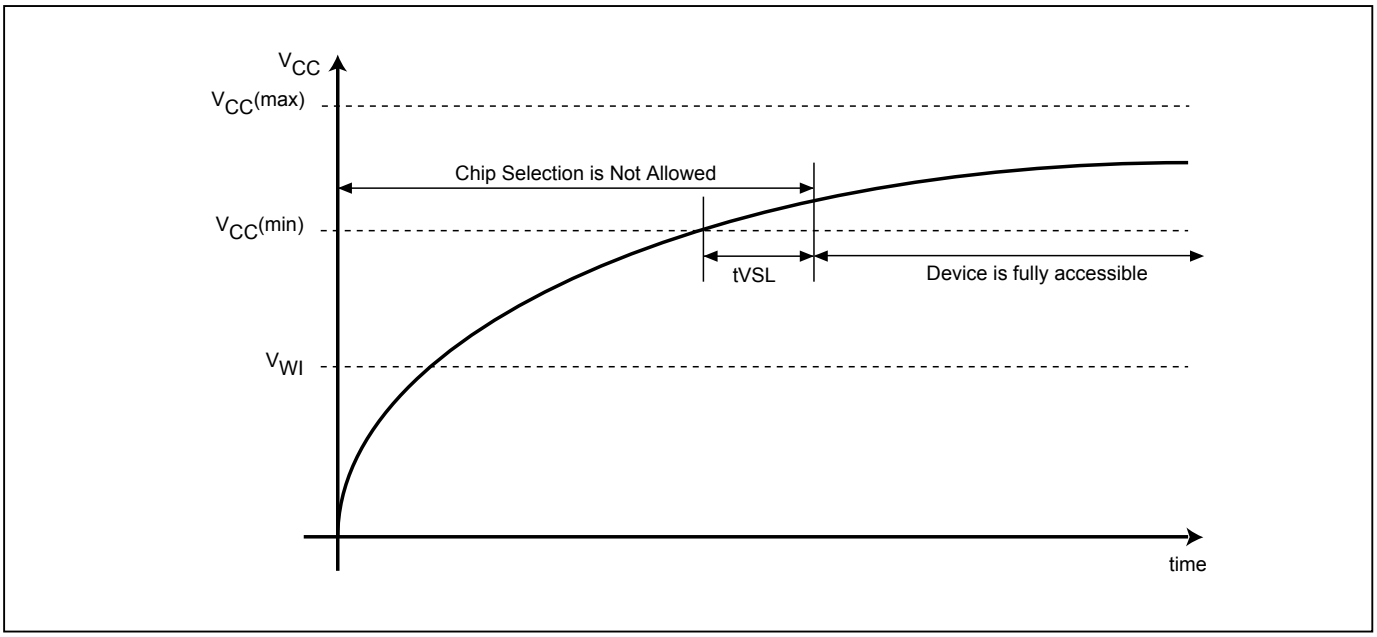


Figure 146. Power-up Timing



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Figure 147. Power Up/Down and Voltage Drop

When powering down the device, VCC must drop below V_{PWD} for at least tPWD to ensure the device will initialize correctly during power up. Please refer to *"Figure 147. Power Up/Down and Voltage Drop"* and *"Table 20. Power-Up/Down Voltage and Timing"* below for more details.

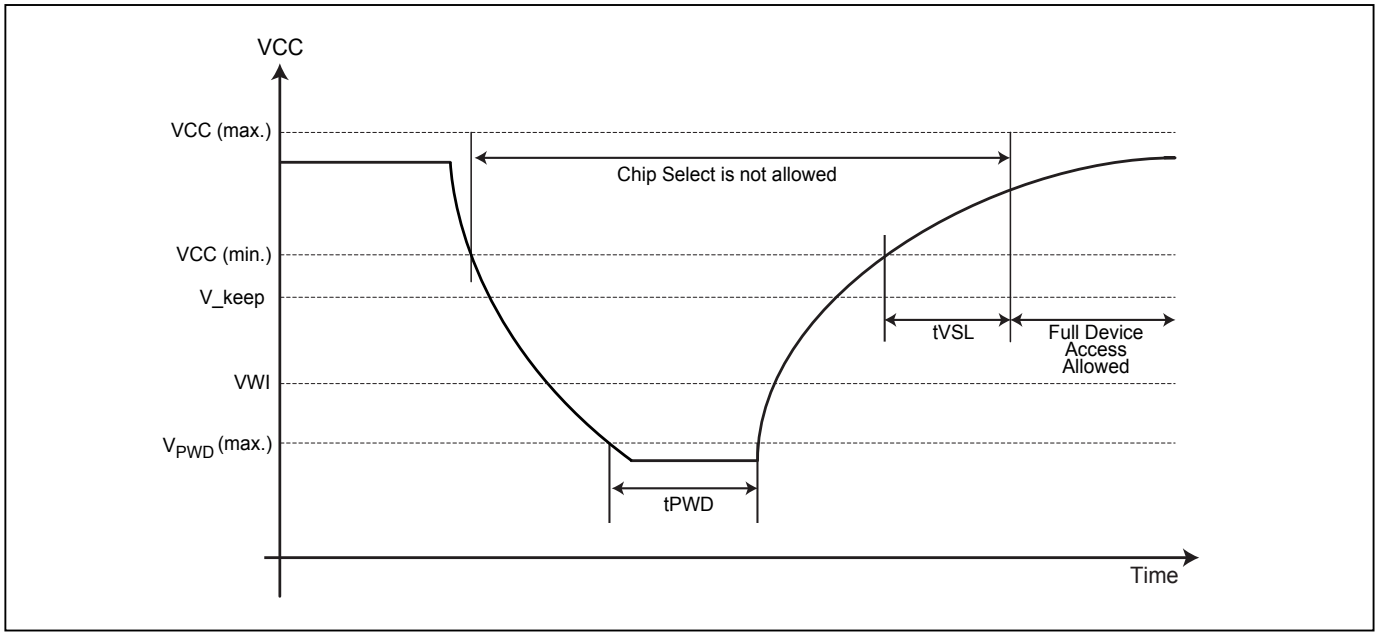


Table 20. Power-Up/Down Voltage and Timing

Symbol	Parameter	Min.	Max.	Unit
V_{PWD}	VCC voltage needed to below V_{PWD} for ensuring initialization will occur		0.9	V
V_keep	Voltage that a re-initialization is necessary if VDD drop below to VKEEP	2.4		V
tPWD	The minimum duration for ensuring initialization will occur	300		us
tVSL	VCC(min.) to device operation	1500		us
VCC	VCC Power Supply	2.7	3.6	V
VWI	Write Inhibit Voltage	2.0	2.3	V

Note: These parameters are characterized only.

16-1. INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0). DOPI# in CR2 depends on shipping device model.

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17. ERASE AND PROGRAMMING PERFORMANCE

Parameter	Min.	Typ. (1)	Max. (2)	Unit
Write Status Register Cycle Time			40	ms
Sector Erase Cycle Time (4KB)		25	400	ms
Block Erase Cycle Time (64KB)		250	2000	ms
Chip Erase Cycle Time		150	300	s
Page Program Time		0.15	0.75	ms
Erase/Program Cycle		100,000		cycles

Note:
1. Typical program and erase time assumes the following conditions: 25°C, 3V, and checkboard pattern.
2. Under worst conditions of 2.7V and the temperature of the worst case.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.

18. DATA RETENTION

Parameter	Condition	Min.	Max.	Unit
Data retention	55˚C	20		years

19. LATCH-UP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to GND on all power pins		1.5 VCCmax
Input current with respect to GND on all non-power pins	-100mA	+100mA
Test conditions are compliant to JEDEC JDESD78 standard		

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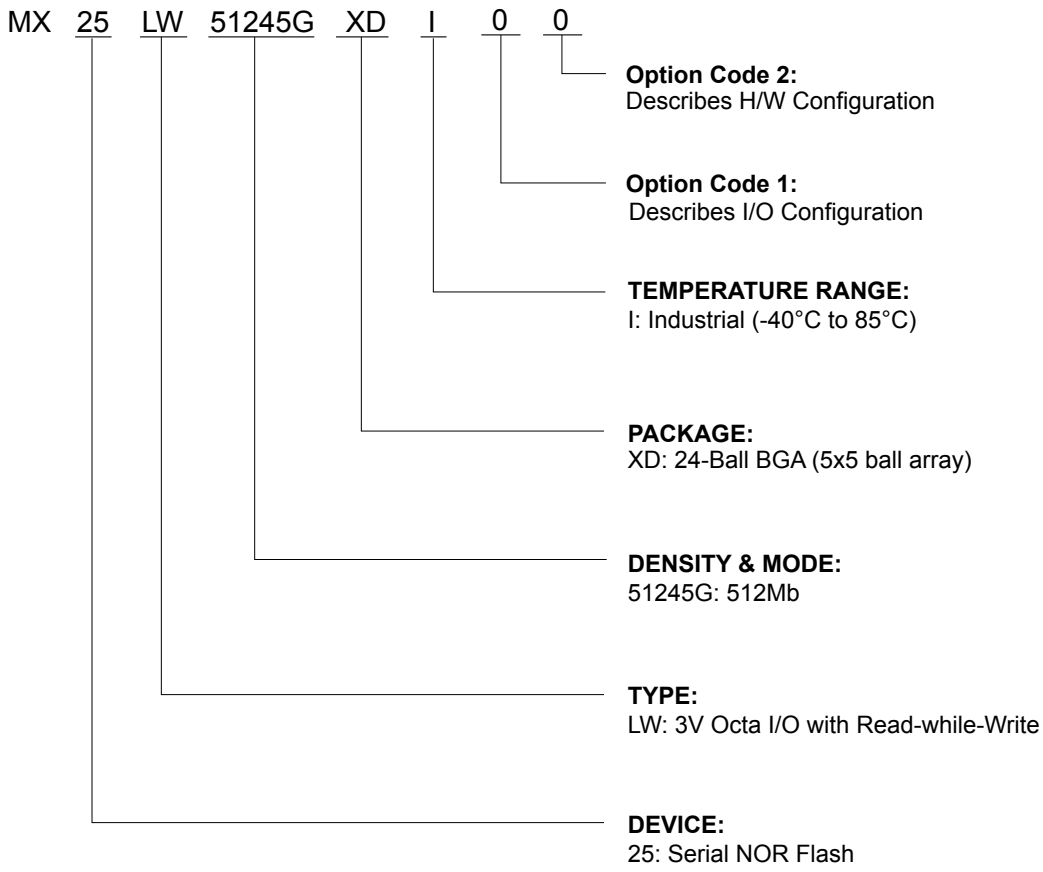
20. ORDERING INFORMATION

Please contact Macronix regional sales for the latest product selection and available form factors.

PART NO.	Package	Temp.	I/O Configuration		H/W Configuration		Remark
			Default I/O	Dummy Cycle	H/W Pin	Addressing	
MX25LW51245GXDI00	24-Ball BGA (5x5 ball array)	-40°C to 85°C	Standard	Standard	Reset#	Standard	

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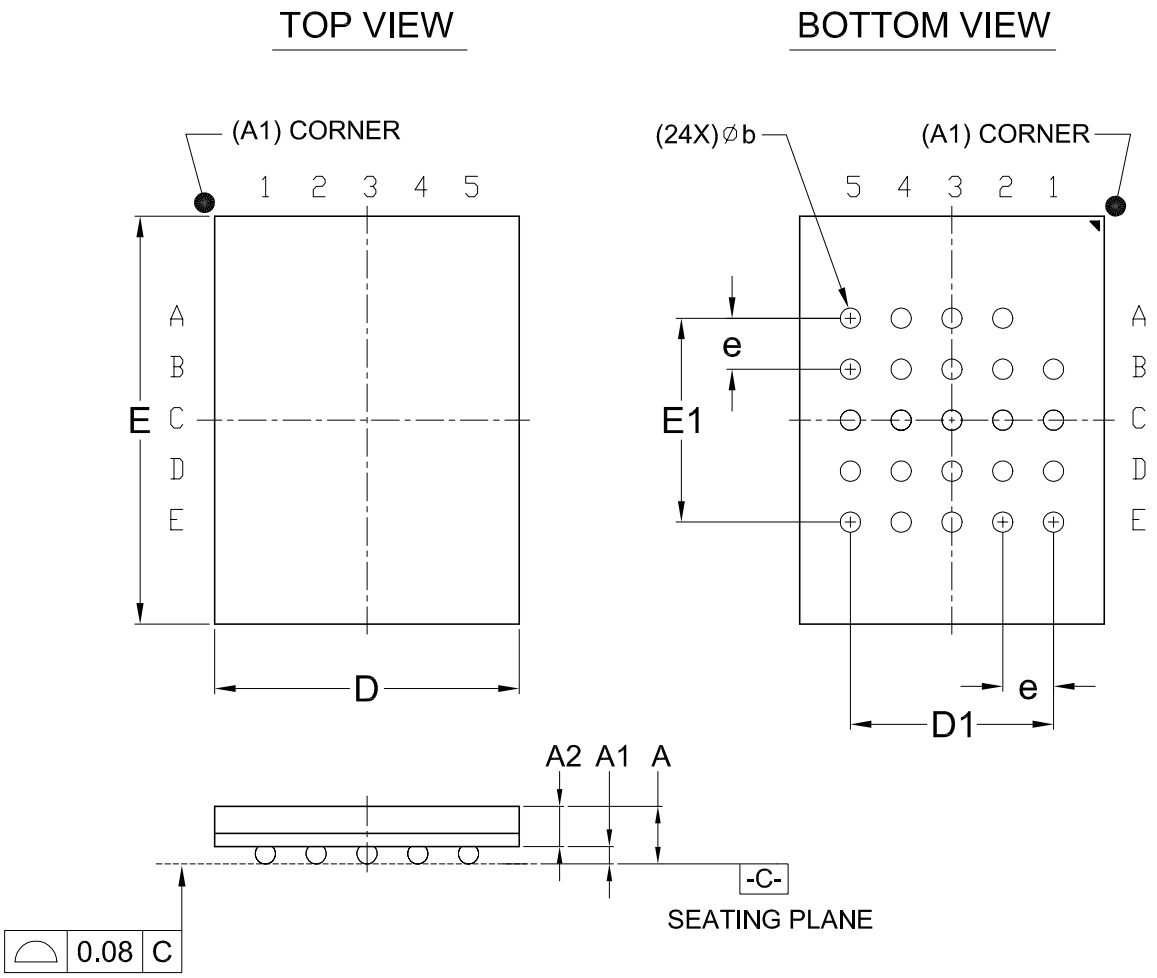
21. PART NAME DESCRIPTION



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22. PACKAGE INFORMATION

Doc. Title: Package Outline for CSP 24BALL (6x8x1.2MM, BALL PITCH 1.0MM, BALL DIAMETER 0.4MM, 5x5 BALL ARRAY)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.65	0.35	5.90	---	7.90	---	---
	Nom.	---	0.30	---	0.40	6.00	4.00	8.00	4.00	1.00
	Max.	1.20	0.35	---	0.45	6.10	---	8.10	---	---
Inch	Min.	---	0.010	0.026	0.014	0.232	---	0.311	---	---
	Nom.	---	0.012	---	0.016	0.236	0.157	0.315	0.157	0.039
	Max.	0.047	0.014	---	0.018	0.240	---	0.319	---	---

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