MX25L3255D

SECURE SERIAL FLASH SPECIFICATION

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Contents

FEATURES **5**
GENERAL DESCRIPTION **7**
Table 1. Additional Feature Comparison 7
PIN CONFIGURATIONS **8**
PIN DESCRIPTION **8**
BLOCK DIAGRAM **9**
DATA PROTECTION **10**
Table 2. 4K-bit Secured OTP Definition 11
Memory Organization **12**
Table 3. Memory Organization 12
DEVICE OPERATION **14**
Figure 1. Serial Modes Supported 14
COMMAND DESCRIPTION **15**
Table 4. Command Set 15
(1) Write Enable (WREN) 17
(2) Write Disable (WRDI) 17
(3) Read Identification (RDID) 17
(4) Read Status Register (RDSR) 17
(5) Block Write Lock Protection (BLOCKP) 18
(6) Read Block Write Lock status (RDBLOCK) 18
(7) Chip Unprotect (UNLOCK) 19
(8) Read Data Bytes (READ) 19
(9) Read Data Bytes at Higher Speed (FAST_READ) 19
(10) 2 x I/O Read Mode (2READ) 19
(11) Dual Read Mode (DREAD) 20
(12) 4 x I/O Read Mode (4READ) 20
(13) Quad Read Mode (QREAD) 20
(14) Sector Erase (SE) 21
(15) Block Erase (BE) 21
(16) Chip Erase (CE) 21
(17) Page Program (PP) 22
(18) 4 x I/O Page Program (4PP) 22
(19) Continuously program mode (CP mode) 22
(20) Deep Power-down (DP) 23
(21) Release from Deep Power-down (RDP), Read Electronic Signature (RES) 23
(22) Read Electronic Manufacturer ID & Device ID (REMS), (REMS2), (REMS4) 24
Table 5. ID Definitions 24
(23) Enter Secured OTP (ENSO) 25
(24) Exit Secured OTP (EXSO) 25

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(25) Read Security Register (RDSCUR) 25
Table 6. Security Register Definition 26
(26) Write Security Register (WRSCUR) 26
POWER-ON STATE 27
ELECTRICAL SPECIFICATIONS 28
ABSOLUTE MAXIMUM RATINGS 28
Figure 2.Maximum Negative Overshoot Waveform 28
CAPACITANCE TA = 25°C, f = 1.0 MHz 28
Figure 3. Maximum Positive Overshoot Waveform 28
Figure 4. INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL 29
Figure 5. OUTPUT LOADING 29
Table 7. DC CHARACTERISTICS (Temperature = -40°C to 85°C for Industrial grade, VCC = 2.7V ~ 3.6V) . 30
Table 8. AC CHARACTERISTICS (Temperature = -40°C to 85°C for Industrial grade, VCC = 2.7V ~ 3.6V) 31
Timing Analysis 32
Figure 6. Serial Input Timing 32
Figure 7. Output Timing 32
Figure 8. WP# Setup Timing and Hold Timing 33
Figure 9. Write Enable (WREN) Sequence (Command 06) 33
Figure 10. Write Disable (WRDI) Sequence (Command 04) 33
Figure 11. Read Identification (RDID) Sequence (Command 9F) 34
Figure 12. Read Status Register (RDSR) Sequence (Command 05) 34
Figure 13. Block Write Lock Protection (BLOCKP) Sequence (Command E2) 34
Figure 14. Chip Unprotect (UNLOCK) Sequence (Command F3) 35
Figure 15. Read Data Bytes (READ) Sequence (Command 03) 35
Figure 16. Read Block Protection Lock Status (RDBLOCK) Sequence (Command FB) 35
Figure 17. Read at Higher Speed (FAST_READ) Sequence (Command 0B) 36
Figure 18. 2 x I/O Read Mode Sequence (Command BB) 36
Figure 19. Dual Read Mode Sequence (Command 3B) 37
Figure 20. 4 x I/O Read Mode Sequence (Command EB) 37
Figure 21. 4 x I/O Read enhance performance Mode Sequence (Command EB) 38
Figure 22. Quad Read Mode Sequence (Command 6B) 39
Figure 23. Page Program (PP) Sequence (Command 02) 40
Figure 24. 4 x I/O Page Program (4PP) Sequence (Command 38) 40
Figure 25. Continously Program (CP) Mode Sequence with Hardware Detection (Command AD) 41
Figure 26. Sector Erase (SE) Sequence (Command 20) 41
Figure 27. Block Erase (BE) Sequence (Command D8) 41
Figure 28. Chip Erase (CE) Sequence (Command 60 or C7) 42
Figure 29. Deep Power-down (DP) Sequence (Command B9) 42
Figure 30. Release from Deep Power-down and Read Electronic Signature (RES) Sequence (Command AB) 42
Figure 31. Release from Deep Power-down (RDP) Sequence (Command AB) 43
Figure 32. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90 or EF or DF) 43

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Figure 33. Power-up Timing 44
Table 9. Power-Up Timing 44
INITIAL DELIVERY STATE 44
OPERATING CONDITIONS 45
Figure 34. AC Timing at Device Power-Up 45
Figure 35. Power-Down Sequence 46
ERASE AND PROGRAMMING PERFORMANCE 47
DATA RETENTION 47
LATCH-UP CHARACTERISTICS 47
ORDERING INFORMATION 48
PART NAME DESCRIPTION 49
PACKAGE INFORMATION 50
REVISION HISTORY 52

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32M-BIT [x 1/x 2/x4] CMOS MXSMIO™ (SERIAL MULTI I/O) FLASH MEMORY

FEATURES

GENERAL

- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 33,554,432 x 1 bit structure or 16,772,216 x 2 bits (two I/O read mode) structure or 8,388,608 x 4 bits (four I/O read mode) structure
- 1024 Equal Sectors with 4K byte each
  - Any Sector can be erased individually
- 64 Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V

PERFORMANCE

- High Performance
  - Fast read
    - 1 I/O: 104MHz with 8 dummy cycles
    - 4 I/O: 75MHz with 6 dummy cycles for 4READ; 75MHz with 8 dummy cycles for QREAD
    - 2 I/O: 75MHz with 4 dummy cycles for 2READ; 75MHz with 8 dummy cycles for DREAD
  - Fast access time: 104MHz serial clock
  - Serial clock of four I/O read mode : 75MHz, which is equivalent to 300MHz
  - Fast program time: 1.4ms(typ.) and 5ms(max.)/page (256-byte per page)
  - Byte program time: 9us (typical)
  - Continuously program mode (automatically increase address under word program mode)
  - Fast erase time: 60ms (typ.)/sector (4K-byte per sector) ; 0.7s(typ.) /block (64K-byte per block); 25s(typ.) /chip
- Low Power Consumption
  - Low active read current: 25mA(max.) at 104MHz, 20mA(max.) at 66MHz and 10mA(max.) at 33MHz
  - Low active programming current: 20mA (max.)
  - Low active erase current: 20mA (max.)
  - Low standby current: 20uA (max.)
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block Write Lock protection
  - Additional 4K-bit secured OTP for unique identifier
  - Permanent lock
  - Read protection function
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)

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• Status Register Feature
• Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - Both REMS,REMS2 and REMS4 commands for 1-byte manufacturer ID and 1-byte device ID

HARDWARE FEATURES

• SCLK Input
  - Serial clock input
• SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
• SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
• WP#/SIO2
  - Hardware write protection or serial data Input/Output for 4 x I/O read mode
• NC/SIO3
  - NC pin or serial data Input/Output for 4 x I/O read mode
• PACKAGE
  - 8-pin SOP (200mil)
  - 24-ball BGA
  - **All Pb-free devices are RoHS Compliant**

Please contact Macronix sales for specific information regarding this Advanced Security Features

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GENERAL DESCRIPTION

The MX25L3255D are 33,554,432 bit serial Flash memory, which is configured as 4,194,304 x 8 internally. When it is in two or four I/O read mode, the structure becomes 16,772,216 bits x 2 or 8,388,608 bits x 4. The MX25L3255D feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin, WP# pin and NC pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX25L3255D provides sequential read operation on whole chip.

After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis for Continuously program mode, and erase command is executes on sector (4K-byte), or block (64K-byte), or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please contact Macronix sales for more details.

When the device is not in operation and CS# is high, it is put in standby mode and draws less than 20uA DC current.

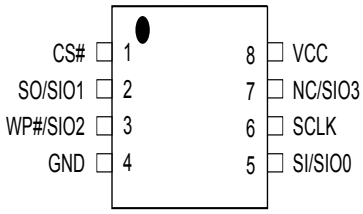
The MX25L3255D utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

Table 1. Additional Feature Comparison

Additional Features / Part Name	Protection and Security					Read Performance		Identifier		
	Permanent Lock	Each Block Protection	4K-bit secured OTP	WP# Hardware Protection	Read Protection	2 I/O Read (75 MHz)	4 I/O Read (75 MHz)	RES (command: 90 hex)	REMS/2/4 (command: 90/EF/0F hex)	RDID (command: 9F hex)
MX25L3255D	V	V	V	V	V	V	V	9E (hex)	C2 9E (hex)	C2 9E 16 (hex)
MX25L3235D			V	V		V	V	5E (hex)	C2 5E (hex)	C2 5E 16 (hex)

PIN CONFIGURATIONS

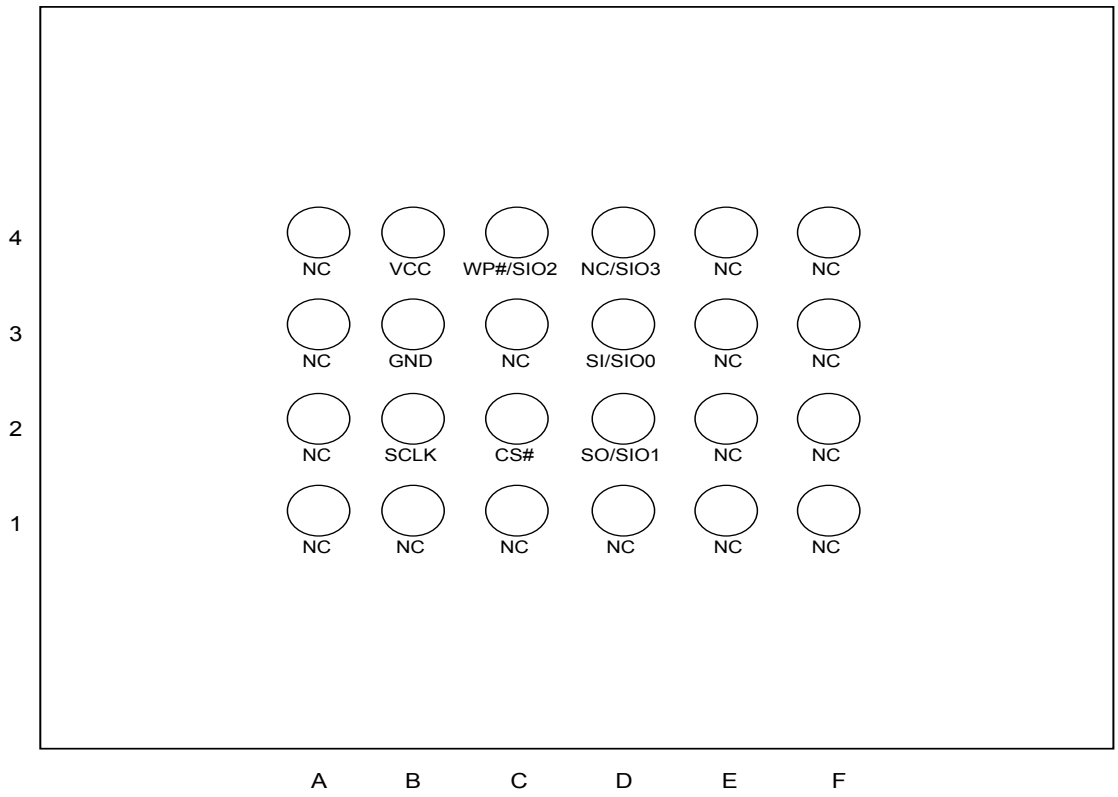
8-PIN SOP (200mil)



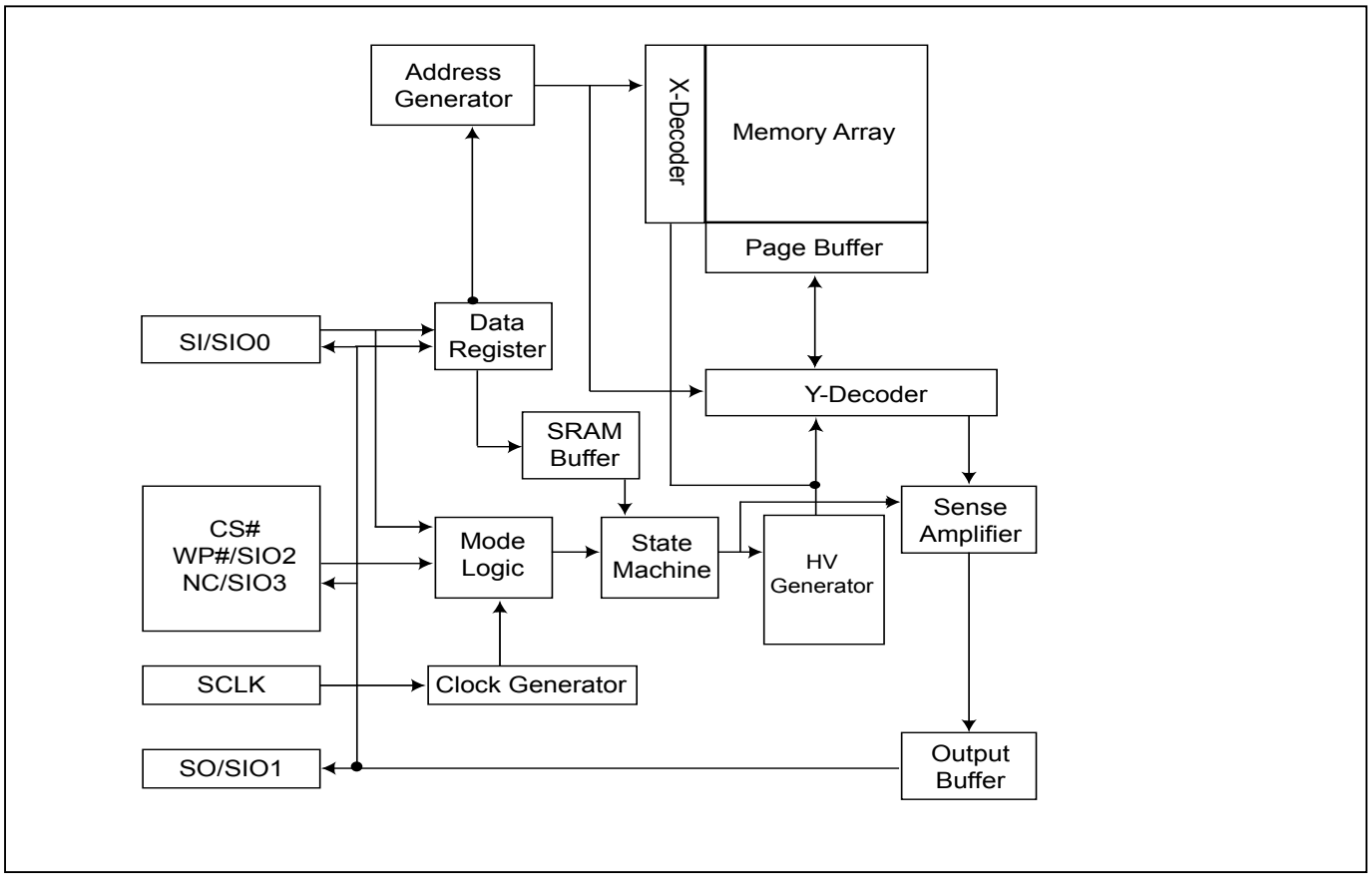
PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SCLK	Clock Input
WP#/SIO2	Write protection: connect to GND or Serial Data Input & Output (for 4xI/O read mode)
NC/SIO3	NC pin (Not connect) or Serial Data Input & Output (for 4xI/O read mode)
VCC	+ 3.3V Power Supply
GND	Ground

24-ball BGA



BLOCK DIAGRAM



DATA PROTECTION

MX25L3255D is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the standby mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.

- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data. The WEL bit will return to reset stage under following situation:
  - Power-up
  - Write Disable (WRDI) command completion
  - Page Program (PP) command completion
  - Continuously Program mode (CP) instruction completion
  - Sector Erase (SE) command completion
  - Block Erase (BE) command completion
  - Chip Erase (CE) command completion

- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES).

- Advanced Security Features: there are some protection and securuity features which protect content from inadvertent write and hostile access.

I. Block Write Lock protection

- The Software Protected Mode (SPM) use A23-A16 address bits to allow a block (64K Byte) of memory to be protected as read only through the Block Write Lock protection command (BLOCKP). This feature allows user to unprotect the entice chip through the chip unprotect command (UNLOCK).

- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the Block.
  If WP#/SIO2=VIL (input Low), all blocks of memory to be protected as read only.
  If WP#/SIO2=VIH (input High), all blocks depends on whether they were last Lock or Unlock. If the system goes into four I/O read mode, the feature of HPM will be disabled.

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II. **Additional 4K-bit secured OTP** for unique identifier: to provide 4K-bit one-time program area for setting device unique serial number - Which may be set by factory or system customer. Please refer to table 2. 4K-bit secured OTP definition.

- Security register bit 0 indicates whether the chip is locked by factory or not.

- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing EXSO command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to table of "security register definition" for security register bit definition and table of "4K-bit secured OTP definition" for address range definition.

- Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit secured OTP mode, array access is not allowed.

Table 2. 4K-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxx000~xxx00F	128-bit	ESN (electrical serial number)	Determined by customer
xxx010~xxx1FF	3968-bit	N/A	

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Memory Organization

Table 3. Memory Organization

Block	Sector	Address Range	
63	1023	3FF000h	3FFFFFh
	:	:	:
	1008	3F0000h	3F0FFFh
62	1007	3EF000h	3EFFFFh
	:	:	:
	992	3E0000h	3E0FFFh
61	991	3DF000h	3DFFFFh
	:	:	:
	976	3D0000h	3D0FFFh
60	975	3CF000h	3CFFFFh
	:	:	:
	960	3C0000h	3C0FFFh
59	959	3BF000h	3BFFFFh
	:	:	:
	944	3B0000h	3B0FFFh
58	943	3AF000h	3AFFFFh
	:	:	:
	928	3A0000h	3A0FFFh
57	927	39F000h	39FFFFh
	:	:	:
	912	390000h	390FFFh
56	911	38F000h	38FFFFh
	:	:	:
	896	380000h	380FFFh
55	895	37F000h	37FFFFh
	:	:	:
	880	370000h	370FFFh
54	879	36F000h	36FFFFh
	:	:	:
	864	360000h	360FFFh
53	863	35F000h	35FFFFh
	:	:	:
	848	350000h	350FFFh
52	847	34F000h	34FFFFh
	:	:	:
	832	340000h	340FFFh
51	831	33F000h	33FFFFh
	:	:	:
	816	330000h	330FFFh
50	815	32F000h	32FFFFh
	:	:	:
	800	320000h	320FFFh
49	799	31F000h	31FFFFh
	:	:	:
	784	310000h	310FFFh
48	783	30F000h	30FFFFh
	:	:	:
	768	300000h	300FFFh

Block	Sector	Address Range	
47	767	2FF000h	2FFFFFh
	:	:	:
	752	2F0000h	2F0FFFh
46	751	2EF000h	2EFFFFh
	:	:	:
	736	2E0000h	2E0FFFh
45	735	2DF000h	2DFFFFh
	:	:	:
	720	2D0000h	2D0FFFh
44	719	2CF000h	2CFFFFh
	:	:	:
	704	2C0000h	2C0FFFh
43	703	2BF000h	2BFFFFh
	:	:	:
	688	2B0000h	2B0FFFh
42	687	2AF000h	2AFFFFh
	:	:	:
	672	2A0000h	2A0FFFh
41	671	29F000h	29FFFFh
	:	:	:
	656	290000h	290FFFh
40	655	28F000h	28FFFFh
	:	:	:
	640	280000h	280FFFh
39	639	27F000h	27FFFFh
	:	:	:
	624	270000h	270FFFh
38	623	26F000h	26FFFFh
	:	:	:
	608	260000h	260FFFh
37	607	25F000h	25FFFFh
	:	:	:
	592	250000h	250FFFh
36	591	24F000h	24FFFFh
	:	:	:
	576	240000h	240FFFh
35	575	23F000h	23FFFFh
	:	:	:
	560	230000h	230FFFh
34	559	22F000h	22FFFFh
	:	:	:
	544	220000h	220FFFh
33	543	21F000h	21FFFFh
	:	:	:
	528	210000h	210FFFh
32	527	20F000h	20FFFFh
	:	:	:
	512	200000h	200FFFh

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Block	Sector	Address Range	
31	511	1FF000h	1FFFFFh
	:	:	:
	496	1F0000h	1F0FFFh
30	495	1EF000h	1EFFFFh
	:	:	:
	480	1E0000h	1E0FFFh
29	479	1DF000h	1DFFFFh
	:	:	:
	464	1D0000h	1D0FFFh
28	463	1CF000h	1CFFFFh
	:	:	:
	448	1C0000h	1C0FFFh
27	447	1BF000h	1BFFFFh
	:	:	:
	432	1B0000h	1B0FFFh
26	431	1AF000h	1AFFFFh
	:	:	:
	416	1A0000h	1A0FFFh
25	415	19F000h	19FFFFh
	:	:	:
	400	190000h	190FFFh
24	399	18F000h	18FFFFh
	:	:	:
	384	180000h	180FFFh
23	383	17F000h	17FFFFh
	:	:	:
	368	170000h	170FFFh
22	367	16F000h	16FFFFh
	:	:	:
	352	160000h	160FFFh
21	351	15F000h	15FFFFh
	:	:	:
	336	150000h	150FFFh
20	335	14F000h	14FFFFh
	:	:	:
	320	140000h	140FFFh
19	319	13F000h	13FFFFh
	:	:	:
	304	130000h	130FFFh
18	303	12F000h	12FFFFh
	:	:	:
	288	120000h	120FFFh
17	287	11F000h	11FFFFh
	:	:	:
	272	110000h	110FFFh
16	271	10F000h	10FFFFh
	:	:	:
	256	100000h	100FFFh
15	255	0FF000h	0FFFFFh
	:	:	:
	240	0F0000h	0F0FFFh

Block	Sector	Address Range	
14	239	0EF000h	0EFFFFh
	:	:	:
	224	0E0000h	0E0FFFh
13	223	0DF000h	0DFFFFh
	:	:	:
	208	0D0000h	0D0FFFh
12	207	0CF000h	0CFFFFh
	:	:	:
	192	0C0000h	0C0FFFh
11	191	0BF000h	0BFFFFh
	:	:	:
	176	0B0000h	0B0FFFh
10	175	0AF000h	0AFFFFh
	:	:	:
	160	0A0000h	0A0FFFh
9	159	09F000h	09FFFFh
	:	:	:
	144	090000h	090FFFh
8	143	08F000h	08FFFFh
	:	:	:
	128	080000h	080FFFh
7	127	07F000h	07FFFFh
	:	:	:
	112	070000h	070FFFh
6	111	06F000h	06FFFFh
	:	:	:
	96	060000h	060FFFh
5	95	05F000h	05FFFFh
	:	:	:
	80	050000h	050FFFh
4	79	04F000h	04FFFFh
	:	:	:
	64	040000h	040FFFh
3	63	03F000h	03FFFFh
	:	:	:
	48	030000h	030FFFh
2	47	02F000h	02FFFFh
	:	:	:
	32	020000h	020FFFh
1	31	01F000h	01FFFFh
	:	:	:
	16	010000h	010FFFh
0	15	00F000h	00FFFFh
	:	:	:
	3	003000h	003FFFh
	2	002000h	002FFFh
	1	001000h	001FFFh
	0	000000h	000FFFh

DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this LSI should be High-Z.

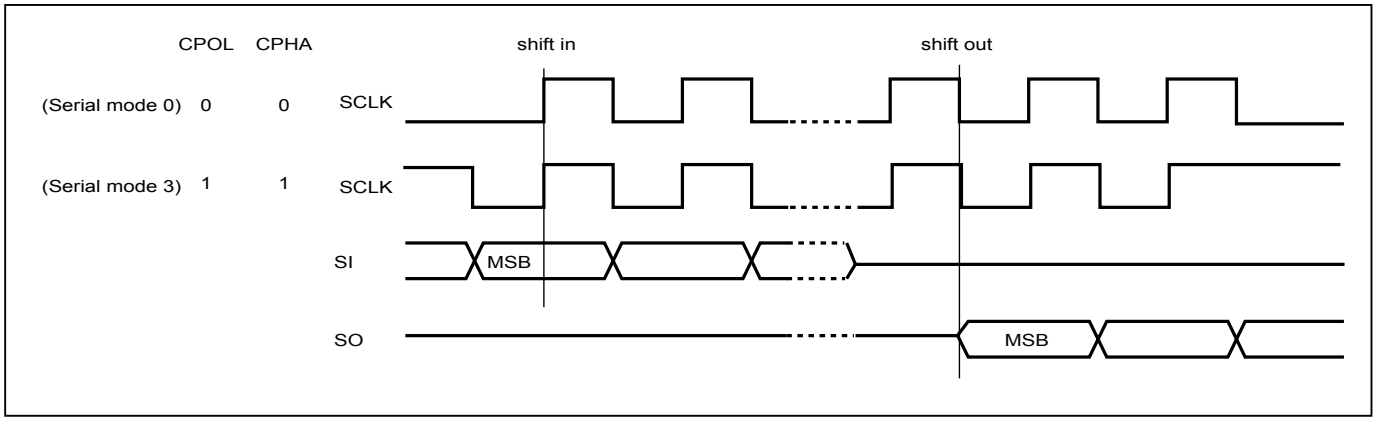
3. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock(SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as Figure 1.

5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, 2READ, DREAD, 4READ, QREAD, RDBLOCK, RDPLOCK, RES, REMS, REMS2 and REMS4 the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRLB, SE, BE, CE, PP, 4PP, CP, RDP, DP, BLOCKP, UNLOCK, ENSO, and EXSO, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported



Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

COMMAND DESCRIPTION

Table 4. Command Set

COMMAND (byte)	WREN (write enable)	WRDI (write disable)	RDID (read identification)	RDSR (read status register)	BLOCKP (Block Write Lock protection)	RDBLOCK (read Block Write Lock status)	UNLOCK (chip unprotect)	READ (read data)
1st byte	06 (hex)	04 (hex)	9F (hex)	05 (hex)	E2 (hex)	FB (hex)	F3 (hex)	03 (hex)
2nd byte					AD1	AD1		AD1 (A23-A16)
3rd byte					AD2	AD2		AD2 (A15-A8)
4th byte					AD3	AD3		AD3 (A7-A0)
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out the values of the status register	assign a block (64KB) to lock protection	read assigned Block Write Lock status	reset Block Write Lock protection bit whole chip	n bytes read out until CS# goes high

COMMAND (byte)	FAST READ (fast read data)	2READ (2 x I/O read command) Note1	DREAD (1I 2O read command)	4READ (4 x I/O read command)	QREAD (1I 4O read command)	Release Read Enhanced	4PP (quad page program)	SE (sector erase)
1st byte	0B (hex)	BB (hex)	3B (hex)	EB (hex)	6B (hex)	FF (hex)	38 (hex)	20 (hex)
2nd byte	AD1	ADD(2)	AD1	ADD(4) & Dummy(4)	AD1	x	AD1	AD1
3rd byte	AD2	ADD(2) & Dummy(2)	AD2	Dummy(4)	AD2	x		AD2
4th byte	AD3		AD3		AD3	x		AD3
5th byte	Dummy		Dummy		Dummy			
Action	n bytes read out until CS# goes high	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by Dual output until CS# goes high	n bytes read out by 4 x I/O until CS# goes high	n bytes read out by Quad output until CS# goes high	All these commands FFh,00h,AAh or 55h will escape the performance enhance mode	quad input to program the selected page	to erase the selected sector

COMMAND (byte)	BE (block erase)	CE (chip erase)	PP (Page program)	CP (Continuously program mode)	DP (Deep power down)	RDP (Release from deep power down)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)
1st byte	D8 (hex)	60 or C7 (hex)	02 (hex)	AD (hex)	B9 (hex)	AB (hex)	AB (hex)	90 (hex)
2nd byte	AD1		AD1	AD1			x	x
3rd byte	AD2		AD2	AD2			x	x
4th byte	AD3		AD3	AD3			x	ADD (Note 2)
Action	to erase the selected block	to erase whole chip	to program the selected page	continously program whole chip, the address is automatically increase	enters deep power down mode	release from deep power down mode	to read out 1-byte Device ID	output the Manufacturer ID & Device ID

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COMMAND (byte)	REMS2 (read ID for 2x I/O mode)	REMS4 (read ID for 4x I/O mode)	ENSO (enter secured OTP)	EXSO (exit secured OTP)	RDSCUR (read security register)	WRSCUR (write security register)	ESRY (enable SO to output RY/BY#)	DSRY (disable SO to output RY/BY#)
1st byte	EF (hex)	DF (hex)	B1 (hex)	C1 (hex)	2B (hex)	2F (hex)	70 (hex)	80 (hex)
2nd byte	x	x						
3rd byte	x	x						
4th byte	ADD (Note 2)	ADD (Note 2)						
Action	output the Manufacturer ID & Device ID	output the Manufact-urer ID & device ID	to enter the 4K-bit Secured OTP mode	to exit the 4K-bit Secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)	to enable SO to output RY/BY# during CP mode	to disable SO to output RY/BY# during CP mode

Note 1: The count base is 4-bit for ADD(2) and Dummy(2) because of 2 x I/O. And the MSB is on SI/SIO1 which is different from 1 x I/O condition.
Note 2: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.
Note 3: It is not allowed to adopt any other code which is not in the above command definition table.

(1) Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, BLOCKP, PLOCK, UNLOCK, CP, SE, BE, and CE which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→ sending WREN instruction code→ CS# goes high. (see Figure 9)

(2) Write Disable (WRDI)

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→ sending WRDI instruction code→ CS# goes high. (see Figure 10)

The WEL bit is reset by following situations:

- Power-up
- Write Disable (WRDI) instruction completion
- Page Program (PP) instruction completion
- Quad Page Program (4PP) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE) instruction completion
- Chip Erase (CE) instruction completion
- Continuously program mode (CP) instruction completion
- Block Write Lock Protection (BLOCKP) instruction completion
- Chip Unprotect (UNLOCK) instruction completion

(3) Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The MXIC Manufacturer ID is C2(hex), the memory type ID is 9E (hex) as the first-byte device ID, and the individual device ID of second-byte ID are listed as table of "ID Definitions". (see table 5)

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code → 24-bits ID data out on SO→ to end RDID operation can use CS# to high at any time during data out. (see Figure 11.)

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

(4) Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO (see Figure 12)

The definition of the status register bits is as below:

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WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored and not affect value of WEL bit if it is applied to a protected memory area.

Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
x	x	x	x	x	x	WEL (write enable latch)	WIP (write in progress bit)
reserved	reserved	reserved	reserved	reserved	reserved	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

(5) Block Write Lock Protection (BLOCKP)

The BLOCKP instruction is for write protection a specified block of memory, using A23-A16 (A15-A0 don't care) address bits to assign a 64Kbyte block to be protected as read only. This feature allows user to stop protecting the entire block through the chip unprotect command (UNLOCK).

The WREN (Write Enable) instruction is required before issuing BLOCKP instruction.

The sequence of issuing BLOCKP instruction is: CS# goes low→send BLOCKP (E2h) instruction → send 3 address bytes assign one block to be protected on SI pin → CS# goes high. (see Figure 13)

The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not be executed.

(6) Read Block Write Lock status (RDBLOCK)

The RDPLOCK instruction is for reading the status of permanent lock of a specified block, using A23-A16 (A15-A0 =0) address bits to assign a 64Kbyte block and read permanent lock status bit which the first byte of Read-out cycle. The first byte data out DQ0 is"1" to indicate that this block has be locked permanently, that user can read only but cannot write, program or erase this block permanently. The first byte data out DQ0 is "0" to indicate that this block hasn't be protected, and user can read and write this block.

The sequence of issuing RDBLOCK instruction is: CS# goes low→ send RDBLOCK (FBh) instruction→ send 3 address bytes to assign one block on SI pin→ read block's protection lock status bit on SO pin → CS# goes high. (see Figure 16)

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(7) Chip Unprotect (UNLOCK)

The UNLOCK instruction is for disabling the lock protection block of the whole chip.

The WREN (Write Enable) instruction is required before issuing UNLOCK instruction.
The sequence of issuing UNLOCK instruction is: CS# goes low → send UNLOCK (F3h) instruction → CS# goes high. (see Figure 14)

The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not be executed.

(8) Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→ sending READ instruction code→ 3-byte address on SI→ data out on SO→to end READ operation can use CS# to high at any time during data out. (see Figure 15)

(9) Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code-> 3-byte address on SI→ 1-dummy byte (default) address on SI→data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out. (see Figure 17)

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(10) 2 x I/O Read Mode (2READ)

The 2READ instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits(interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→ sending 2READ instruction→ 24-bit address interleave on SIO1 & SIO0→ 4-bit dummy cycle on SIO1 & SIO0→data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out (see Figure 18 for 2 x I/O Read Mode Timing Waveform).

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

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(11) Dual Read Mode (DREAD)

The DREAD instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits(interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing DREAD instruction is: CS# goes low→ sending DREAD instruction→3-byte address on SIO0→ 8-bit dummy cycle on SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out (see Figure 19 for Dual Read Mode Timing Waveform).

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(12) 4 x I/O Read Mode (4READ)

The 4READ instruction enable quad throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every four bits(interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing 4READ instruction is: CS# goes low→ sending 4READ instruction→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→ 6 dummy cycles → data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out (see Figure 20 for 4 x I/O Read Mode Timing Waveform).

Another sequence of issuing 4 READ instruction especially useful in random access is : CS# goes low→ sending 4 READ instruction→ 3-bytes address interleave on SIO3, SIO2, SIO1 & SIO0 → performance enhance toggling bit P[7:0]→ 4 dummy cycles → data out still CS# goes high → CS# goes low (reduce 4 Read instruction) → 24-bit random access address (see Figure 21 for 4x I/O read enhance performance mode timing waveform).

In the performance-enhancing mode, P[7:4] must be toggling with P[3:0] ; likewise P[7:0]=A5h,5Ah,F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh,00h,AAh or 55h. And afterwards CS# is raised or issuing FF command(CS# goes high -> CS# goes low -> sending 0xFF -> CS# goes high) instead of no toggling,the system then will escape from performance enhance mode and return to normal opertaion.In these cases,tSHSL=15ns(min) will be specified.

While Program/Erase cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase current cycle.

(13) Quad Read Mode (QREAD)

The QREAD instruction enable quad throughput of Serial Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before seding the QREAD instruction.The address is latched on rising edge of SCLK, and data of every four bits(interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address

after each byte data is shifted out, so the whole memory can be read out at a single QREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing QREAD instruction, the following data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing QREAD instruction is: CS# goes low→ sending QREAD instruction→ 24-bit address on SIO0→ 8 dummy cycles → data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end QREAD operation can use CS# to high at any time during data out (see Figure 22 for Quad Read Mode Timing Waveform).

While Program/Erase/Write Status Register cycle is in progress, QREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(14) Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see table 3) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low → sending SE instruction code→ 3-byte address on SI → CS# goes high. (see Figure 26)

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the sector is protected, the Sector Erase (SE) instruction will not be executed on the sector.

(15) Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (see table 3) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low →sending BE instruction code→ 3-byte address on SI →CS# goes high. (see Figure 27)

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected, the Block Erase (BE) instruction will not be executed on the block.

(16) Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go

high exactly at the byte boundary, otherwise the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→ sending CE instruction code→ CS# goes high. (see Figure 28)

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Chip Erase cycle is in progress. The WIP sets 1 during the tCE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

(17) Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. If the entire 256 data bytes are going to be programmed, A7-A0 (The eight least significant address bits) should be set to 0. If the eight least significant address bits (A7-A0) are not all 0, all transmitted data going beyond the end of the current page are programmed from the start address of the same page (from the address A7-A0 are all 0). If more than 256 bytes are sent to the device, the data of the last 256-byte is programmed at the request page and previous data will be disregarded. If less than 256 bytes are sent to the device, the data is programmed at the requested address of the page without effect on other address of the same page.

The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high. (see Figure 23)

The CS# must be kept to low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary (the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected, the Page Program (PP) instruction will not be executed.

(18) 4 x I/O Page Program (4PP)

The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit. The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3 as address and data input, which can improve programer performance and the effectiveness of application of lower clock less than 20MHz. For system with faster clock, the Quad page program cannot provide more actual favors, because the required internal page program time is far more than the time data flows in. Therefore, we suggest that while executing this command (especially during sending data), user can slow the clock speed down to 20MHz below. The other function descriptions are as same as standard page program.

The sequence of issuing 4PP instruction is: CS# goes low→ sending 4PP instruction code→ 3-byte address on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→ CS# goes high. (see Figure 24)

(19) Continuously program mode (CP mode)

The CP mode may enhance program performance by automatically increasing address to the next higher address after each byte data has been programmed.

The Continuously program (CP) instruction is for multiple byte program to Flash. A write Enable (WREN) instruction must execute to set the Write Enable Latch(WEL) bit before sending the Continuously program (CP) instruction. CS# requires to go high before CP instruction is executing. After CP instruction and address input, two bytes of data is input sequentially from MSB(bit7) to LSB(bit0). The first byte data will be programmed to the initial address range with A0=0 and second byte data with A0=1. If only one byte data is input, the CP mode will not process. If more than two bytes data are input, the additional data will be ignored and only two byte data are valid. The CP program instruction will be ignored and not affect the WEL bit if it is applied to a protected memory area. Any byte to be programmed should be in the erase state (FF) first. It will not roll over during the CP mode, once the last unprotected address has been reached, the chip will exit CP mode and reset write Enable Latch bit (WEL) as "0" and CP mode bit as "0". Please check the WIP bit status if it is not in write progress before entering next valid instruction. During CP mode, the valid commands are CP command (AD hex), WRDI command (04 hex), RDSR command (05 hex), and RDSCUR command (2B hex). And the WRDI command is valid after completion of a CP programming cycle, which means the WIP bit=0.

The sequence of issuing CP instruction is : CS# high to low→ sending CP instruction code→ 3-byte address on SI-> Data Byte on SI→CS# goes high to low→sending CP instruction.....→ last desired byte programmed or sending Write Disable (WRDI) instruction to end CP mode→ sending RDSR instruction to verify if CP mode is ended. (see Figure 25 of CP mode timing waveform)

Three methods to detect the completion of a program cycle during CP mode:
1) Software method-I: by checking WIP bit of Status Register to detect the completion of CP mode.
2) Software method-II: by waiting for a tBP time out to determine if it may load next valid command or not.
3) Hardware method: by writing ESRY (enable SO to output RY/BY#) instruction to detect the completion of a program cycle during CP mode. The ESRY instruction must be executed before CP mode execution. Once it is enable in CP mode, the CS# goes low will drive out the RY/BY# status on SO, "0" indicates busy stage, "1" indicates ready stage, SO pin outputs tri-state if CS# goes high. DSRY (disable SO to output RY/BY#) instruction to disable the SO to output RY/BY# and return to status register data output during CP mode. Please note that the ESRY/DSRY command are not accepted unless the completion of CP mode.

(20) Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (to entering the Deep Power-down mode), the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When CS# goes high, it's only in standby mode not deep power-down mode. It's different from Standby mode.

The sequence of issuing DP instruction is: CS# goes low→sending DP instruction code→ CS# goes high. (see Figure 29)

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction. (those instructions allow the ID being reading out). When Power-down, the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For RDP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode and reducing the current to ISB2.

(21) Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the

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Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and Chip Select (CS#) must remain High for at least tRES2(max), as specified in Table 8. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

The sequence is shown as Figure 30, 31.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

The RDP instruction is for releasing from Deep Power Down Mode.

(22) Read Electronic Manufacturer ID & Device ID (REMS), (REMS2), (REMS4)

The REMS, REMS2 & REMS4 instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The REMS, REMS2 & REMS4 instruction is very similar to the Release from Power-down/Device ID instruction. The instruction is initiated by driving the CS# pin low and shift the instruction code "90h" or "EFh" or "DFh"followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID for MXIC (C2h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure 32. The Device ID values are listed in Table of ID Definitions. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Table 5. ID Definitions

RDID Command	manufacturer ID	memory type	memory density
	C2	9E	16
RES Command	electronic ID		
	9E		
REMS/REMS2/REMS4/ Command	manufacturer ID	device ID	
	C2	9E	

(23) Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 4K-bit secured OTP mode. The additional 4K-bit secured OTP is independent from main array, which may use to store unique serial number for system identifier. After entering the Secured OTP mode, and then follow standard read or program, procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low→ sending ENSO instruction to enter Secured OTP mode→ CS# goes high.

Please note that WRSCUR commands is not acceptable during the access of secure OTP region, once security OTP is lock down, only read related commands are valid.

(24) Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 4K-bit secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low→ sending EXSO instruction to exit Secured OTP mode→ CS# goes high.

(25) Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write parameter register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low→ send ing RDSCUR instruction → Security Register data out on SO→ CS# goes high.

The definition of the Security Register bits is as below:

Secured OTP Indicator bit. The Secured OTP indicator bit shows the chip is locked by factory before ex- factory or not. When it is "0", it indicates non- factory lock; "1" indicates factory- lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 4K-bit Secured OTP area cannot be update any more. While it is in 4K-bit secured OTP mode, array access is not allowed.

Continuously Program Mode (CP mode) bit. The Continuously Program Mode bit indicates the status of CP mode, "0" indicates not in CP mode; "1" indicates in CP mode.

Table 6. Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
x	x	x	Continuously Program mode (CP mode)	x	x	LDSO (indicate if lock-down	Secured OTP indicator bit
reserved	reserved	reserved	0=normal Program mode 1=CP mode (default=0)	reserved	reserved	0 = not lock-down 1 = lock-down (cannot program/erase OTP)	0 = non-factory lock 1 = factory lock
volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	non-volatile bit	non-volatile bit

(26) Write Security Register (WRSCUR)

The WRSCUR instruction is for changing the values of Security Register Bits. The WREN instruction is not required before sending WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 4K-bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more.

The sequence of issuing WRSCUR instruction is :CS# goes low→ sending WRSCUR instruction → CS# goes high.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

POWER-ON STATE

The device is at below states when power-up:
- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level:
- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The read, write, erase, and program command should be sent after the time delay:
- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.

Please refer to the figure of "power-up timing".

Note:
- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

RATING		VALUE
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.5V to 4.6V
Applied Output Voltage		-0.5V to 4.6V
VCC to Ground Potential		-0.5V to 4.6V

NOTICE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot Vss to -2.0V and Vcc to +2.0V for periods up to 20ns, see Figure 2, 3.

Figure 2.Maximum Negative Overshoot Waveform

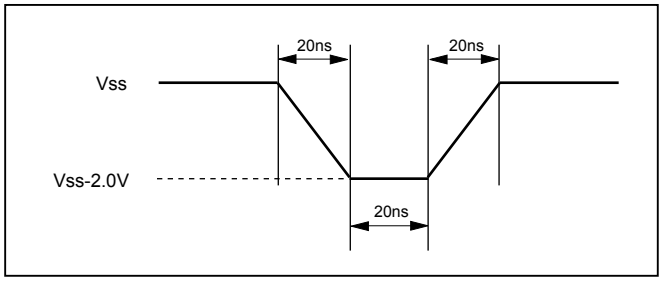
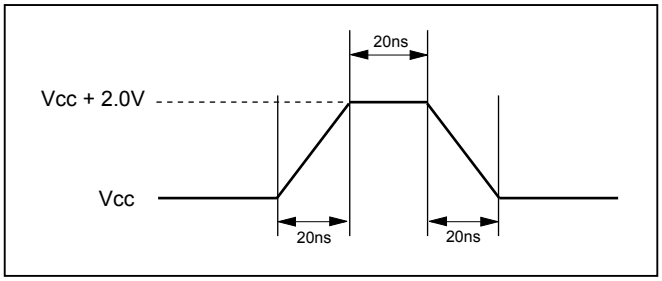


Figure 3. Maximum Positive Overshoot Waveform



CAPACITANCE TA = 25°C, f = 1.0 MHz

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			6	pF	VIN = 0V
COUT	Output Capacitance			8	pF	VOUT = 0V

Figure 4. INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL

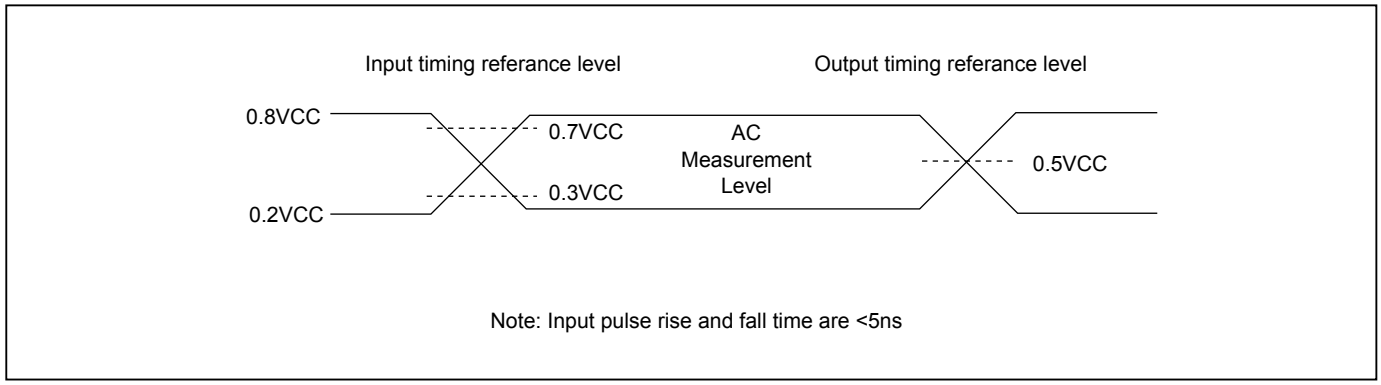
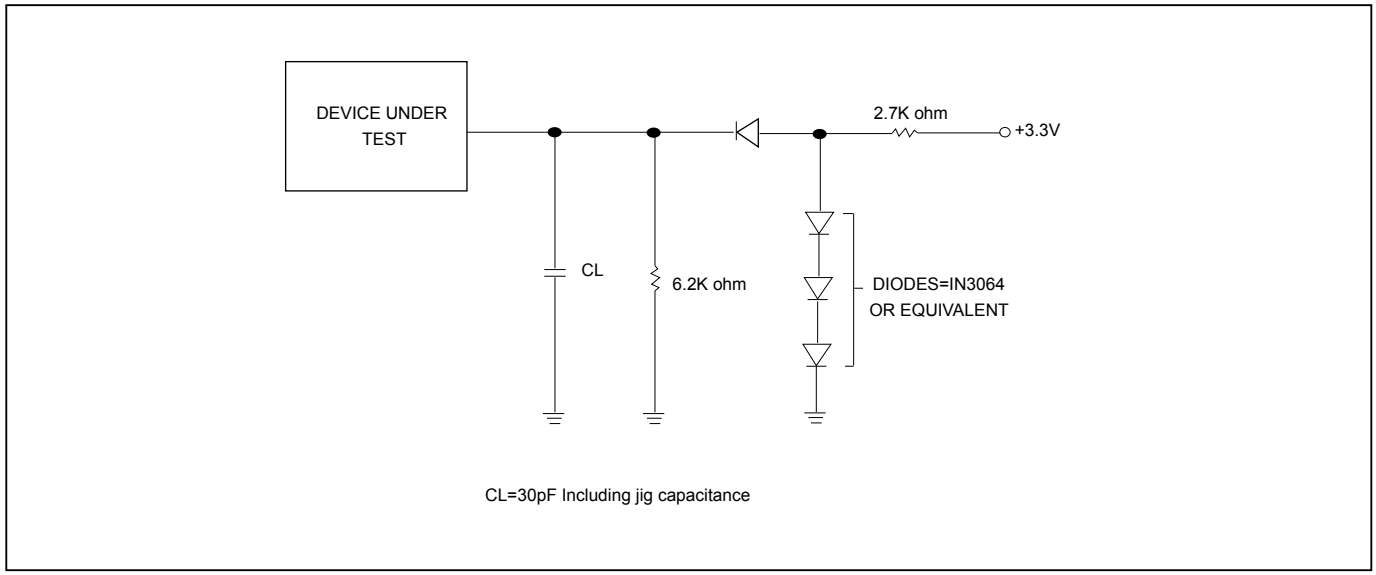


Figure 5. OUTPUT LOADING



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Table 7. DC CHARACTERISTICS (Temperature = -40°C to 85°C for Industrial grade, VCC = 2.7V ~ 3.6V)

SYMBOL	PARAMETER	NOTES	MIN.	MAX.	UNITS	TEST CONDITIONS
ILI	Input Load Current	1		± 2	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1		± 2	uA	VCC = VCC Max, VIN = VCC or GND
ISB1	VCC Standby Current	1		20	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			20	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1		25	mA	f=104MHz, fQ=75MHz (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
				20	mA	f=66MHz, fT=75MHz (2 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
				10	mA	f=33MHz, SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		20	mA	Program in Progress, CS# = VCC
ICC4	VCC Sector Erase Current (SE)	1		20	mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		20	mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage		-0.5	0.3VCC	V	
VIH	Input High Voltage		0.7VCC	VCC+0.4	V	
VOL	Output Low Voltage			0.4	V	IOL = 1.6mA
VOH	Output High Voltage		VCC-0.2		V	IOH = -100uA

Notes :
1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

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Table 8. AC CHARACTERISTICS (Temperature = -40°C to 85°C for Industrial grade, VCC = 2.7V ~ 3.6V)

Symbol	Alt.	Parameter		Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE, CE, DP, RES,RDP WREN, WRDI, RDID, RDSR, WRSR		D.C.		104	MHz
fRSCLK	fR	Clock Frequency for READ instructions				33	MHz
fTSCLK	fT	Clock Frequency for 2READ, DREAD instructions				75	MHz
	fQ	Clock Frequency for 4READ, QRAED instructions				75	MHz
fPSCLK	fP	Clock Frequency for 4PP operation				20	MHz
tCH(1)	tCLH	Clock High Time	fc=104MHz	4.7			ns
			fR=33MHz	13			ns
tCL(1)	tCLL	Clock Low Time	fc=104MHz	4.7			ns
			fR=33MHz	13			ns
tCLCH(2)		Clock Rise Time (3) (peak to peak)		0.1			V/ns
tCHCL(2)		Clock Fall Time (3) (peak to peak)		0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)		5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)		5			ns
tDVCH	tDSU	Data In Setup Time		2			ns
tCHDX	tDH	Data In Hold Time		5			ns
tCHSH		CS# Active Hold Time (relative to SCLK)		5			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)		5			ns
tSHSL(3)	tCSH	CS# Deselect Time	Read	15			ns
			Write/Erase/Program	50			ns
tSHQZ(2)	tDIS	Output Disable Time Loading: 30pF/15pF	2.7V-3.6V			10/8	ns
			3.0V-3.6V			8/6	ns
tCLQV	tV	Clock Low to Output Valid Loading: 30pF/15pF	2.7V-3.6V			10/8	ns
			3.0V-3.6V			8/6	ns
tCLQX	tHO	Output Hold Time		0			ns
tWHSL(4)		Write Protect Setup Time		20			ns
tSHWL(4)		Write Protect Hold Time		100			ns
tDP(2)		CS# High to Deep Power-down Mode				10	us
tRES1(2)		CS# High to Standby Mode without Electronic Signature Read				8.8	us
tRES2(2)		CS# High to Standby Mode with Electronic Signature Read				8.8	us
tU		Chip Unprotect Time			40	100	ms
tBP		Byte-Program			9	300	us
tPP		Page Program Cycle Time			1.4	5	ms
tSE		Sector Erase Cycle Time			60	300	ms
tBE		Block Erase Cycle Time			0.7	2	s
tCE		Chip Erase Cycle Time			25	50	s

Notes:
1. tCH + tCL must be greater than or equal to 1/ f (fC or fR).
2. Value guaranteed by characterization, not 100% tested in production.
3. tSHSL=15ns from read instruction, tSHSL=50ns from Write/Erase/Program instruction.
4. Test condition is shown as Figure 4, 5.

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Timing Analysis

Figure 6. Serial Input Timing

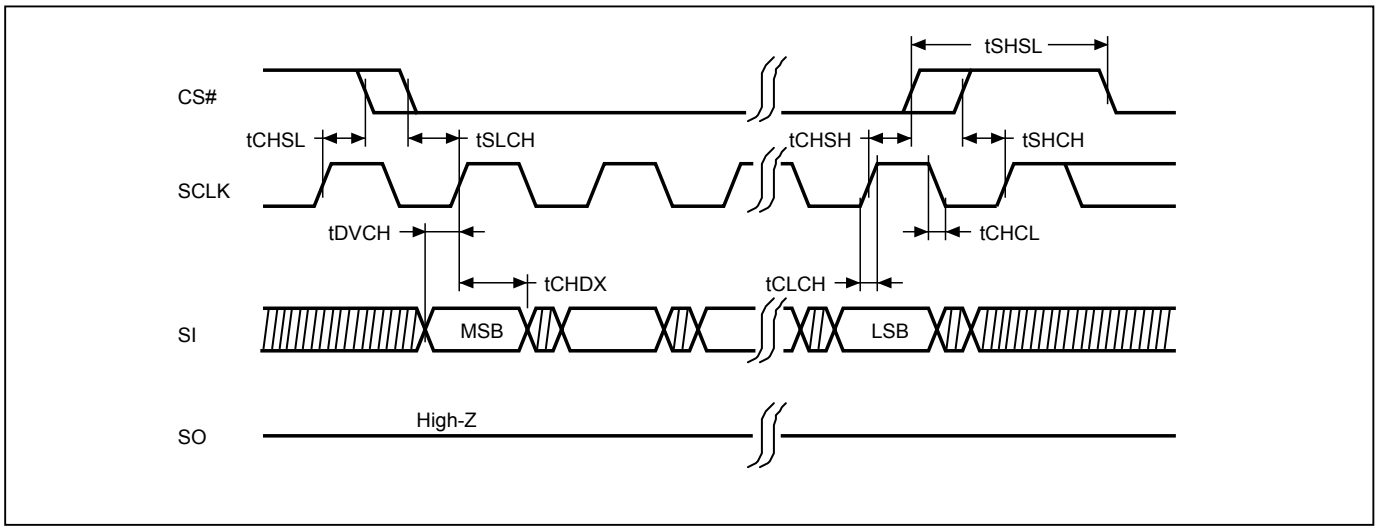


Figure 7. Output Timing

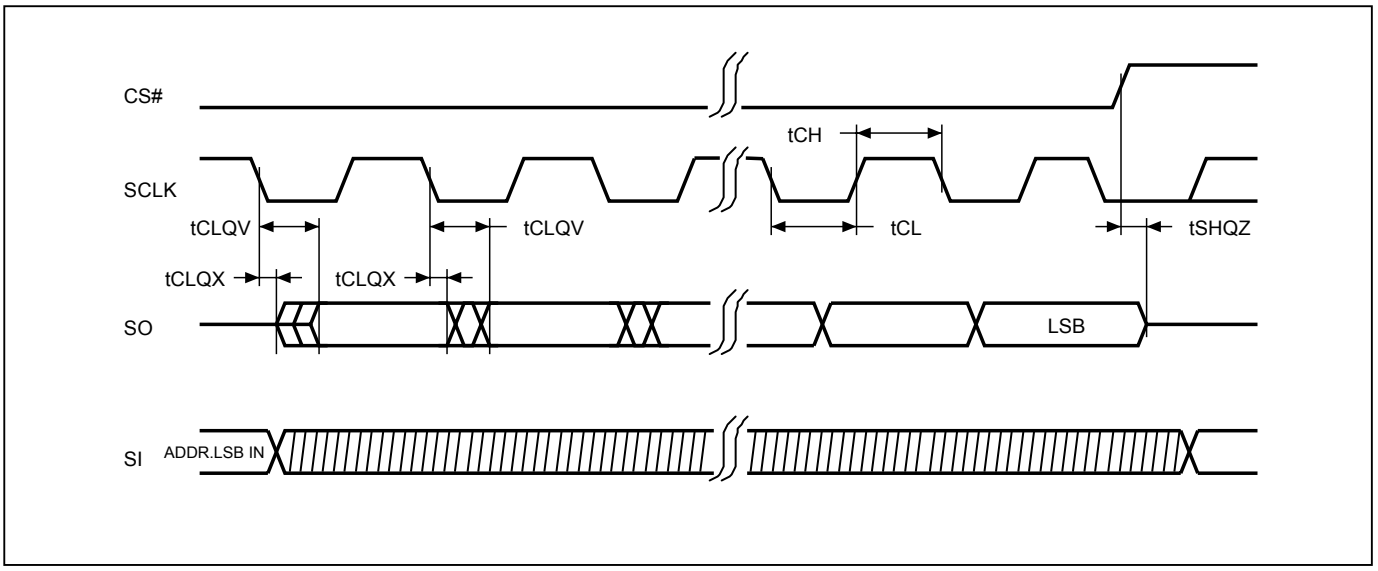


Figure 8. WP# Setup Timing and Hold Timing

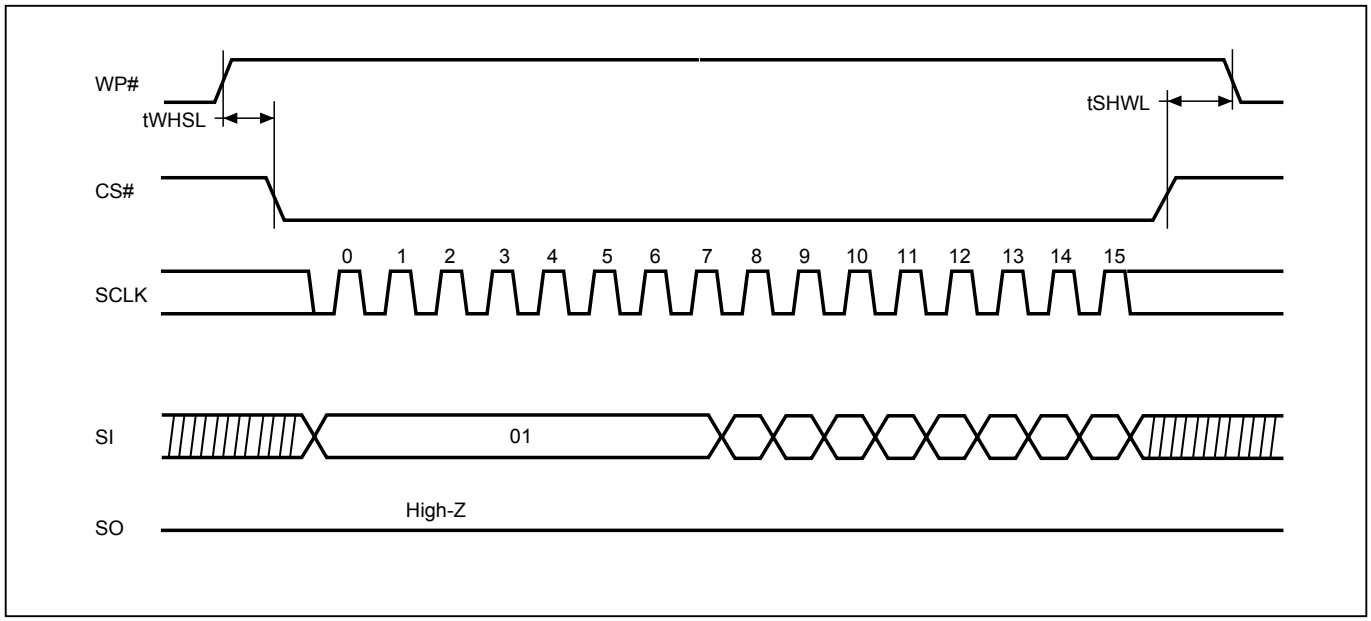


Figure 9. Write Enable (WREN) Sequence (Command 06)

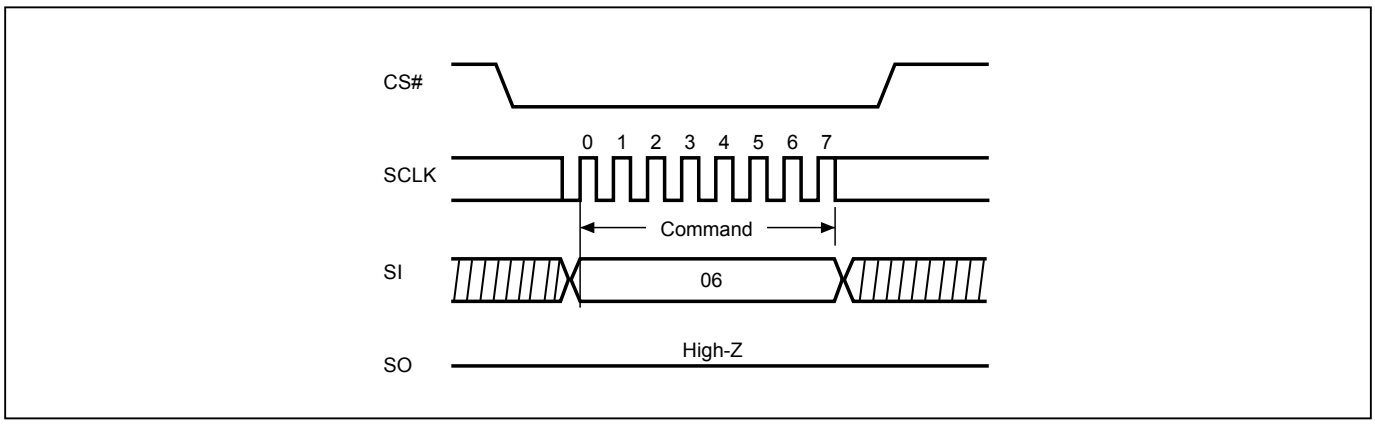


Figure 10. Write Disable (WRDI) Sequence (Command 04)

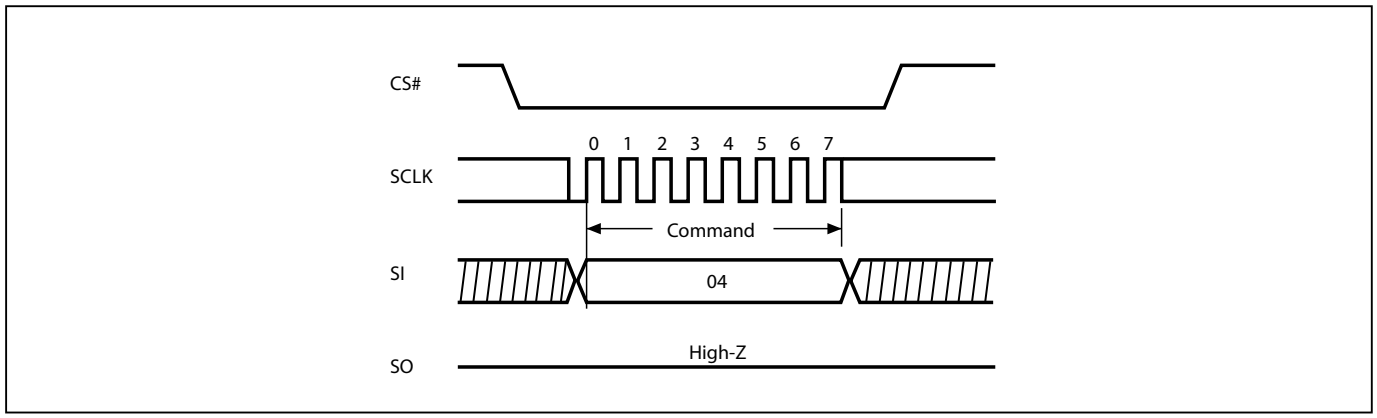


Figure 11. Read Identification (RDID) Sequence (Command 9F)

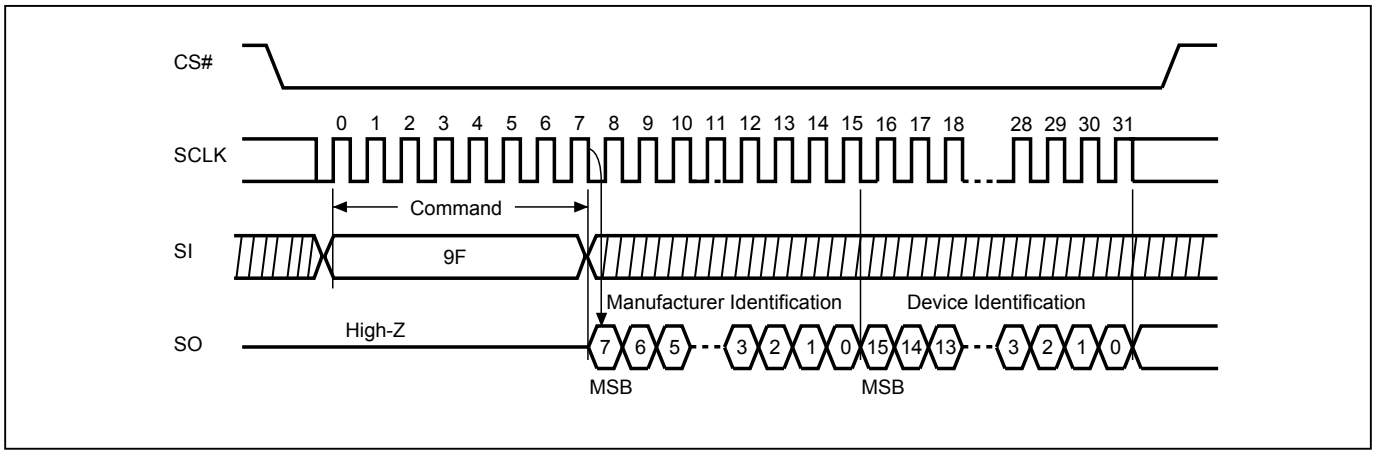


Figure 12. Read Status Register (RDSR) Sequence (Command 05)

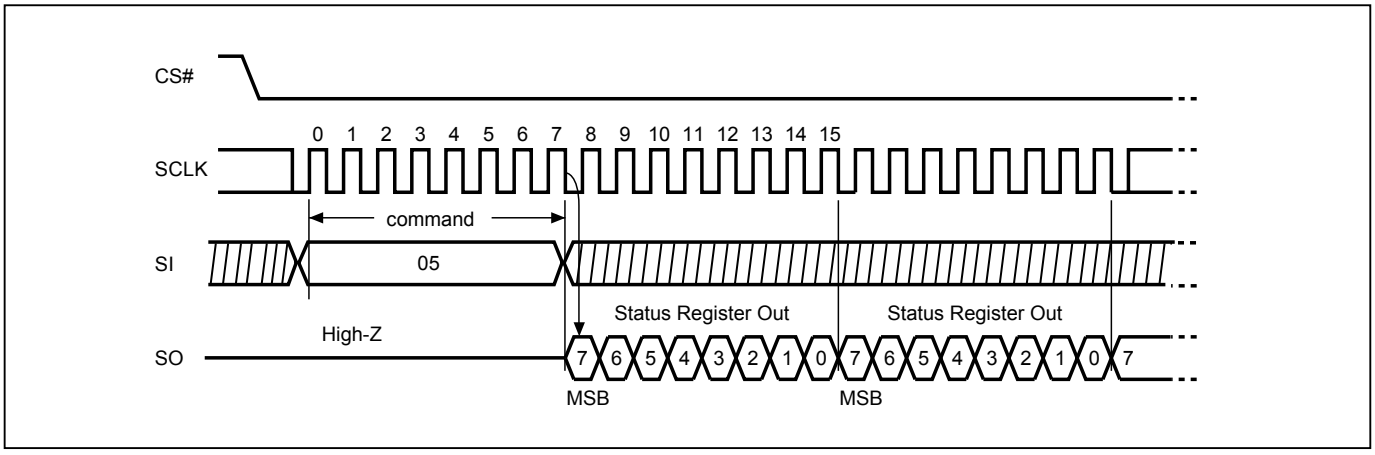


Figure 13. Block Write Lock Protection (BLOCKP) Sequence (Command E2)

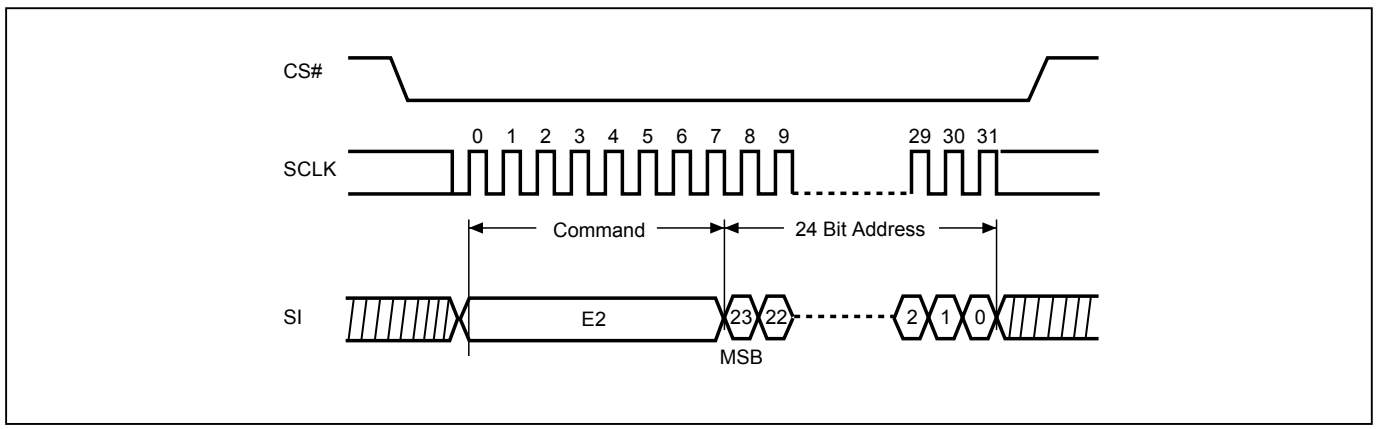


Figure 14. Chip Unprotect (UNLOCK) Sequence (Command F3)

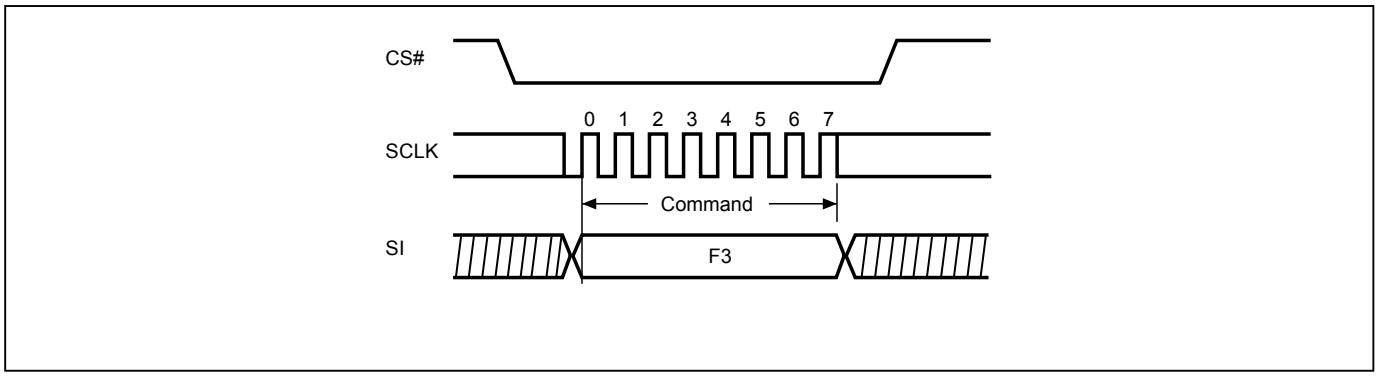


Figure 15. Read Data Bytes (READ) Sequence (Command 03)

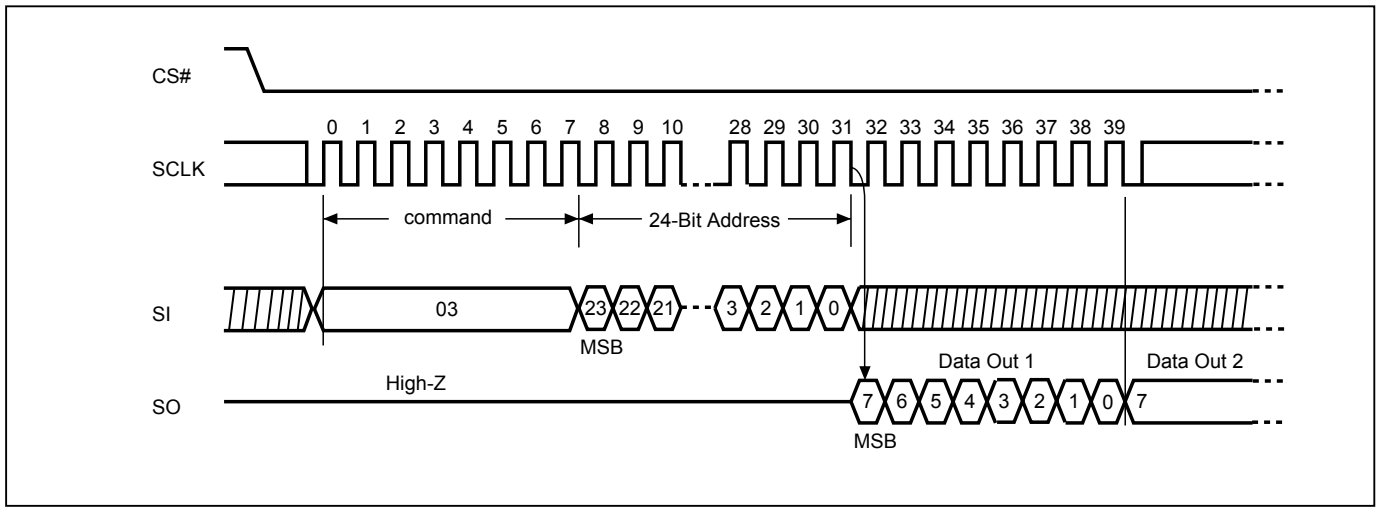


Figure 16. Read Block Protection Lock Status (RDBLOCK) Sequence (Command FB)

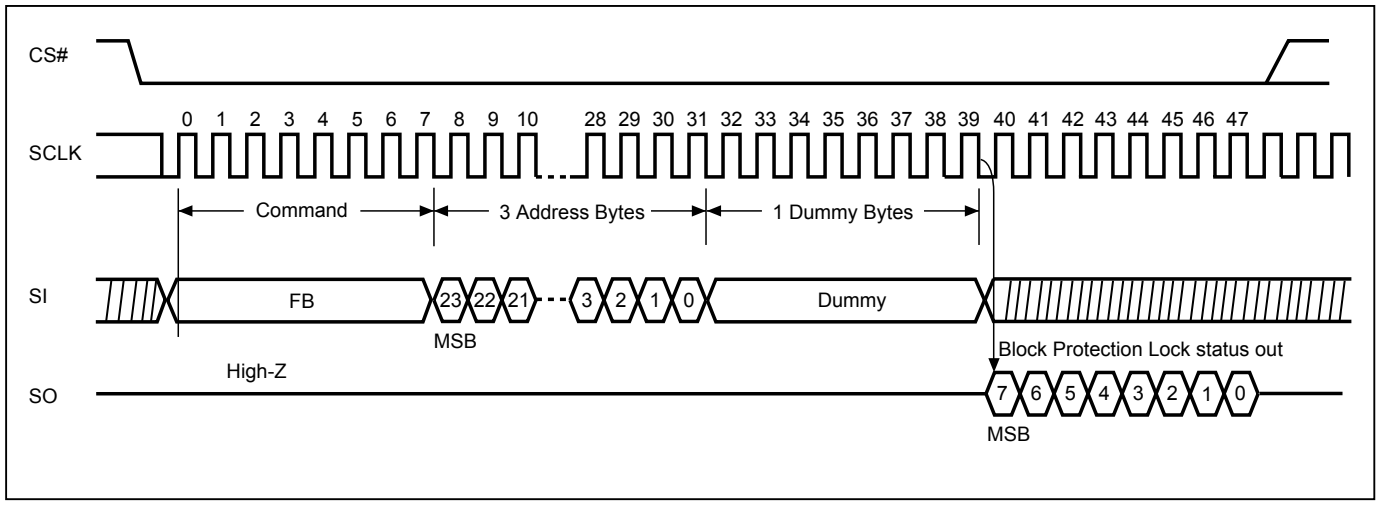


Figure 17. Read at Higher Speed (FAST_READ) Sequence (Command 0B)

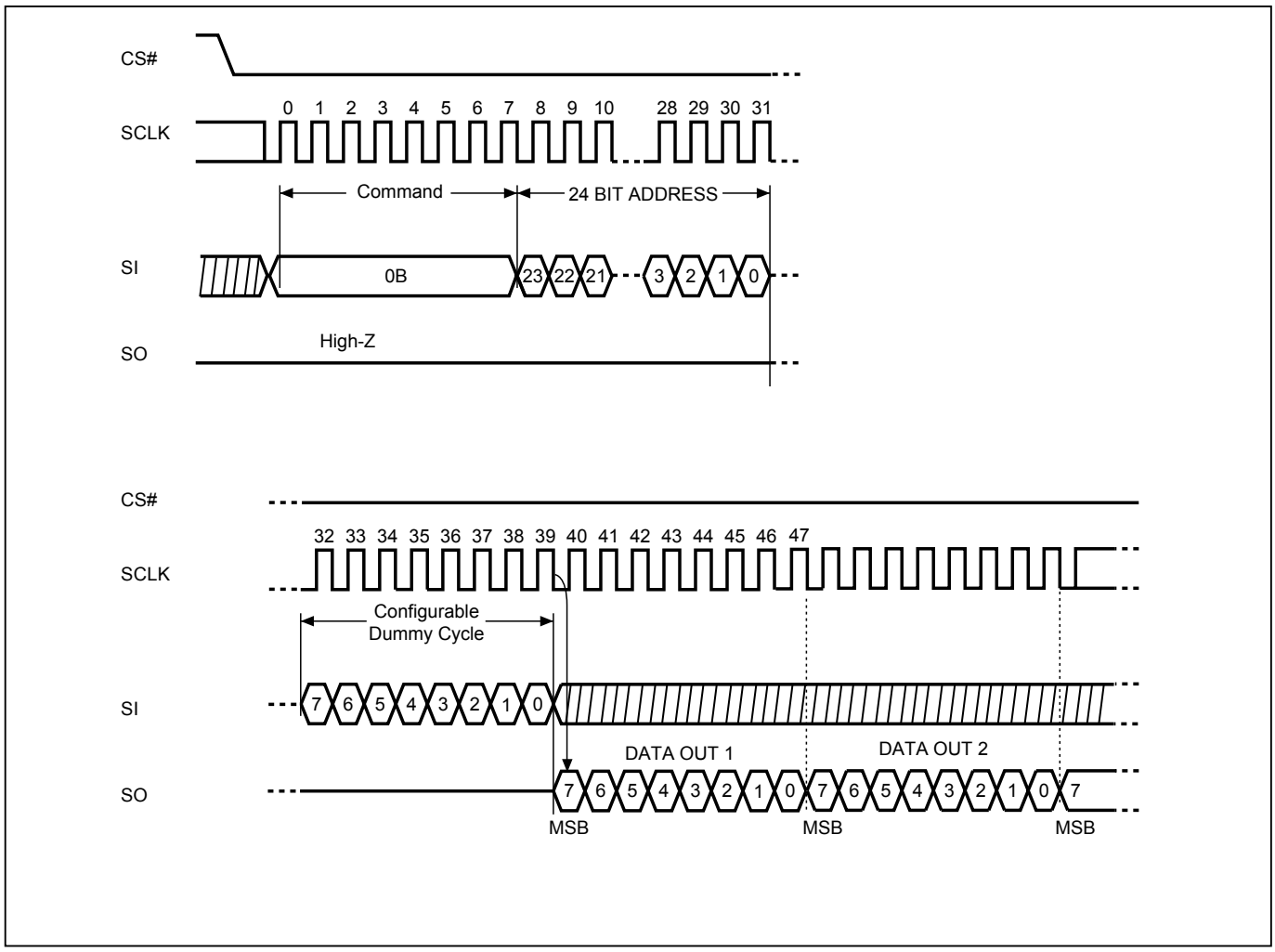


Figure 18. 2 x I/O Read Mode Sequence (Command BB)

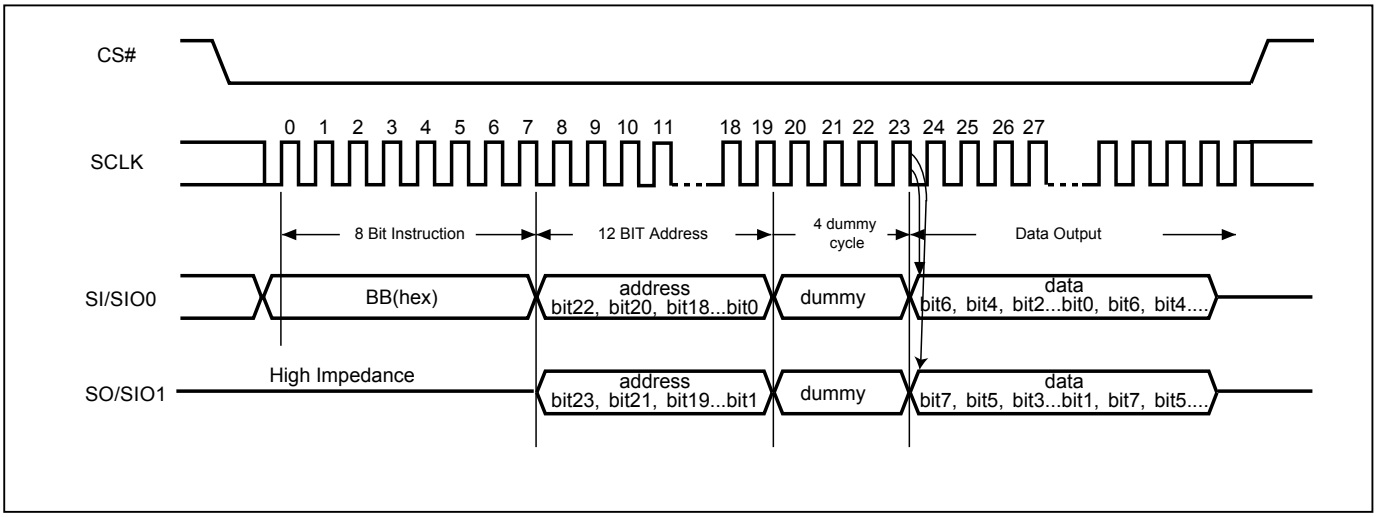


Figure 19. Dual Read Mode Sequence (Command 3B)

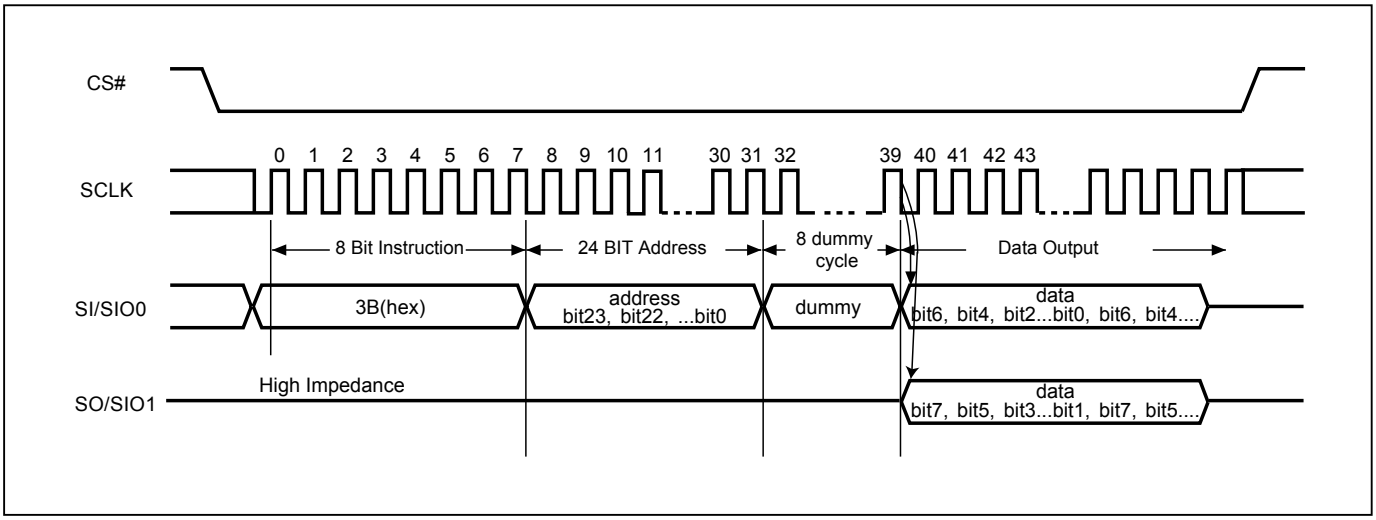
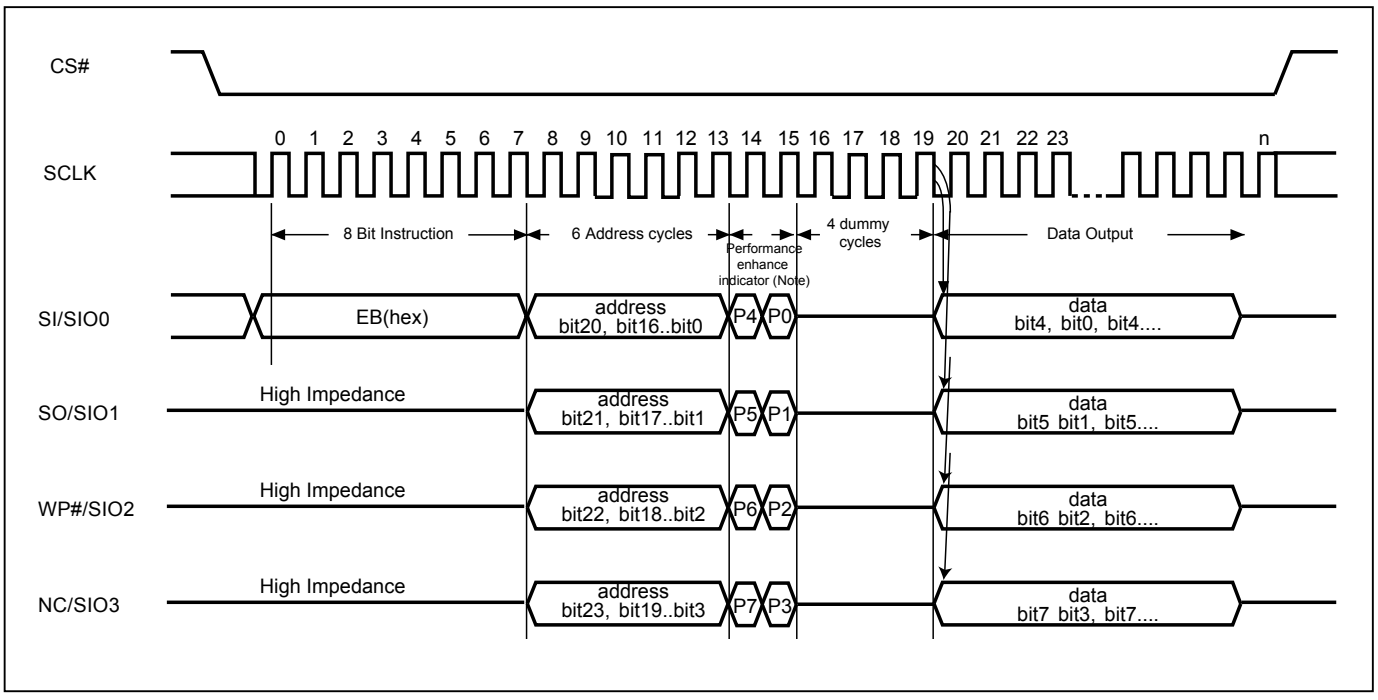
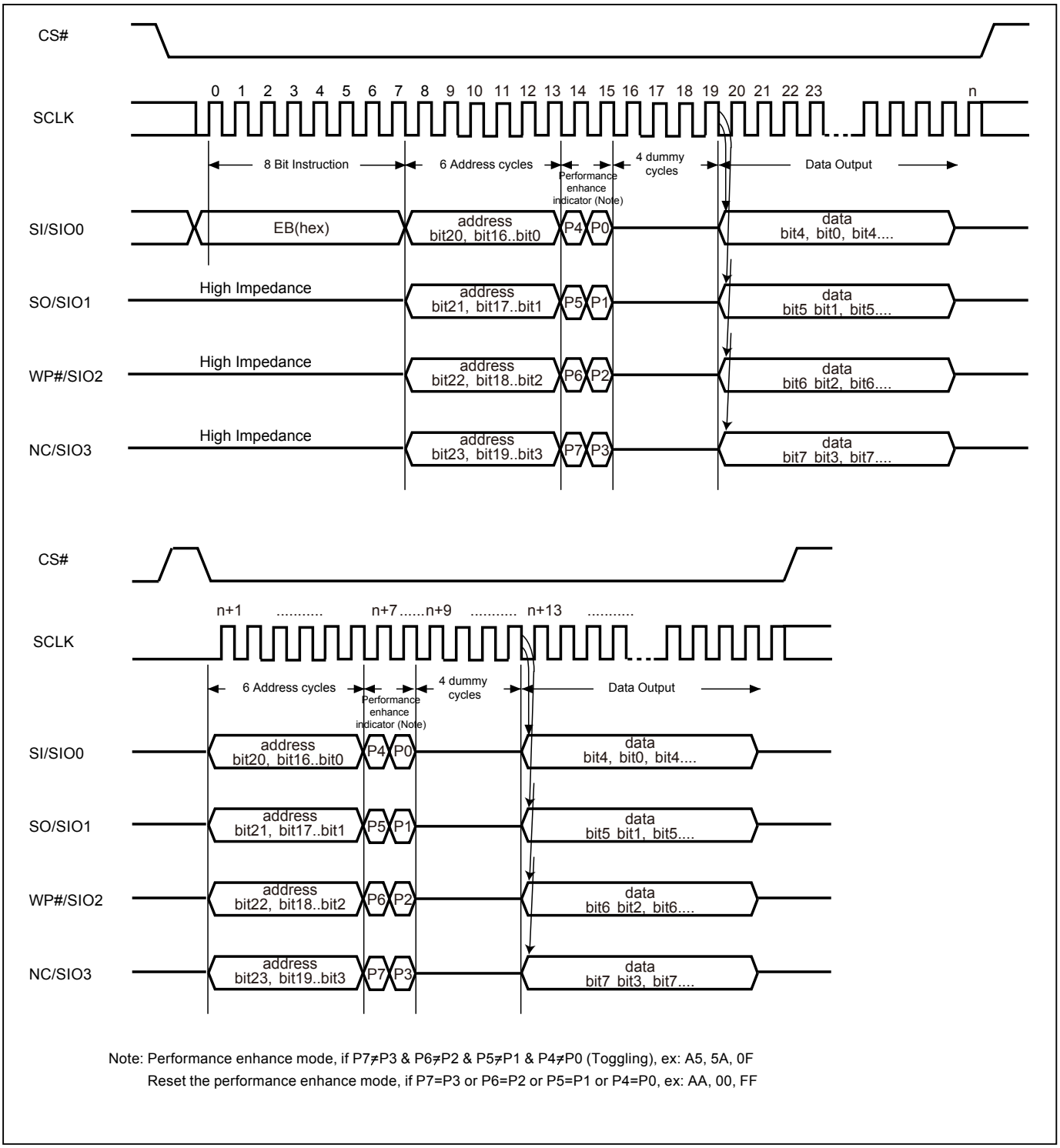


Figure 20. 4 x I/O Read Mode Sequence (Command EB)



Note:
1. Hi-impedance is inhibited for the two clock cycles.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) is inhibited.

Figure 21. 4 x I/O Read enhance performance Mode Sequence (Command EB)



Note: Performance enhance mode, if P7≠P3 & P6≠P2 & P5≠P1 & P4≠P0 (Toggling), ex: A5, 5A, 0F
Reset the performance enhance mode, if P7=P3 or P6=P2 or P5=P1 or P4=P0, ex: AA, 00, FF

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Figure 22. Quad Read Mode Sequence (Command 6B)

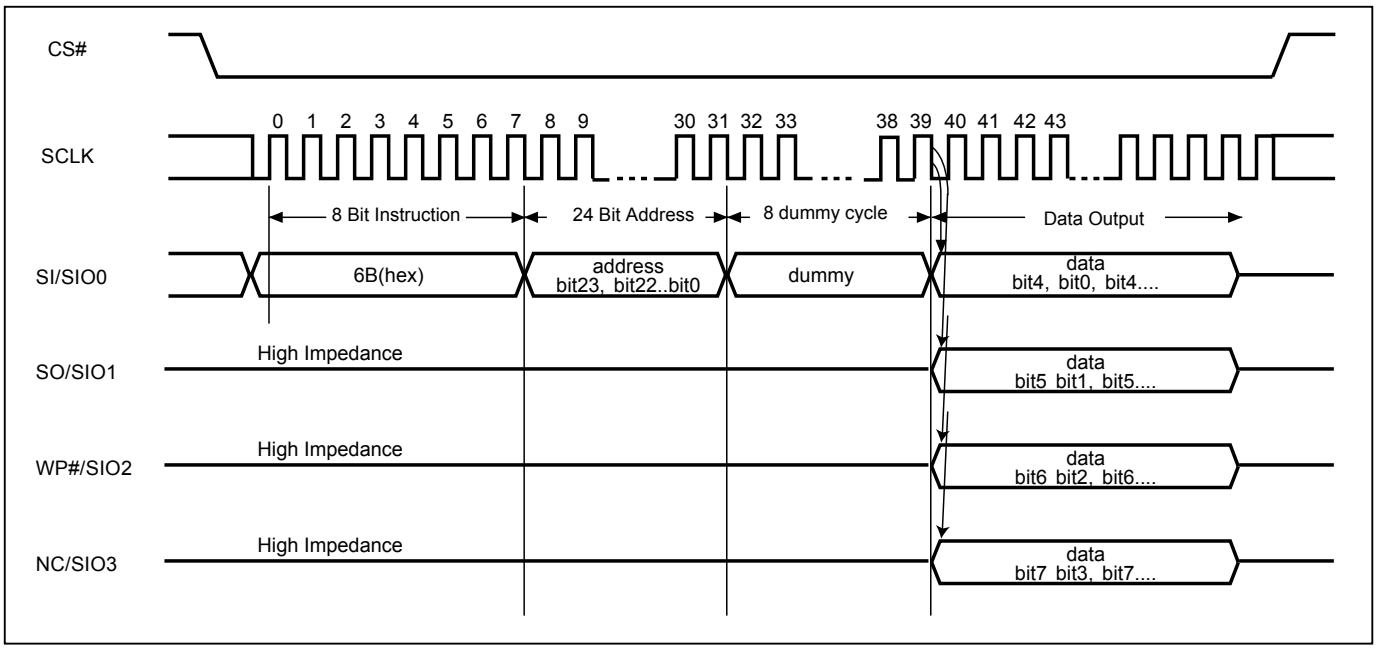


Figure 23. Page Program (PP) Sequence (Command 02)

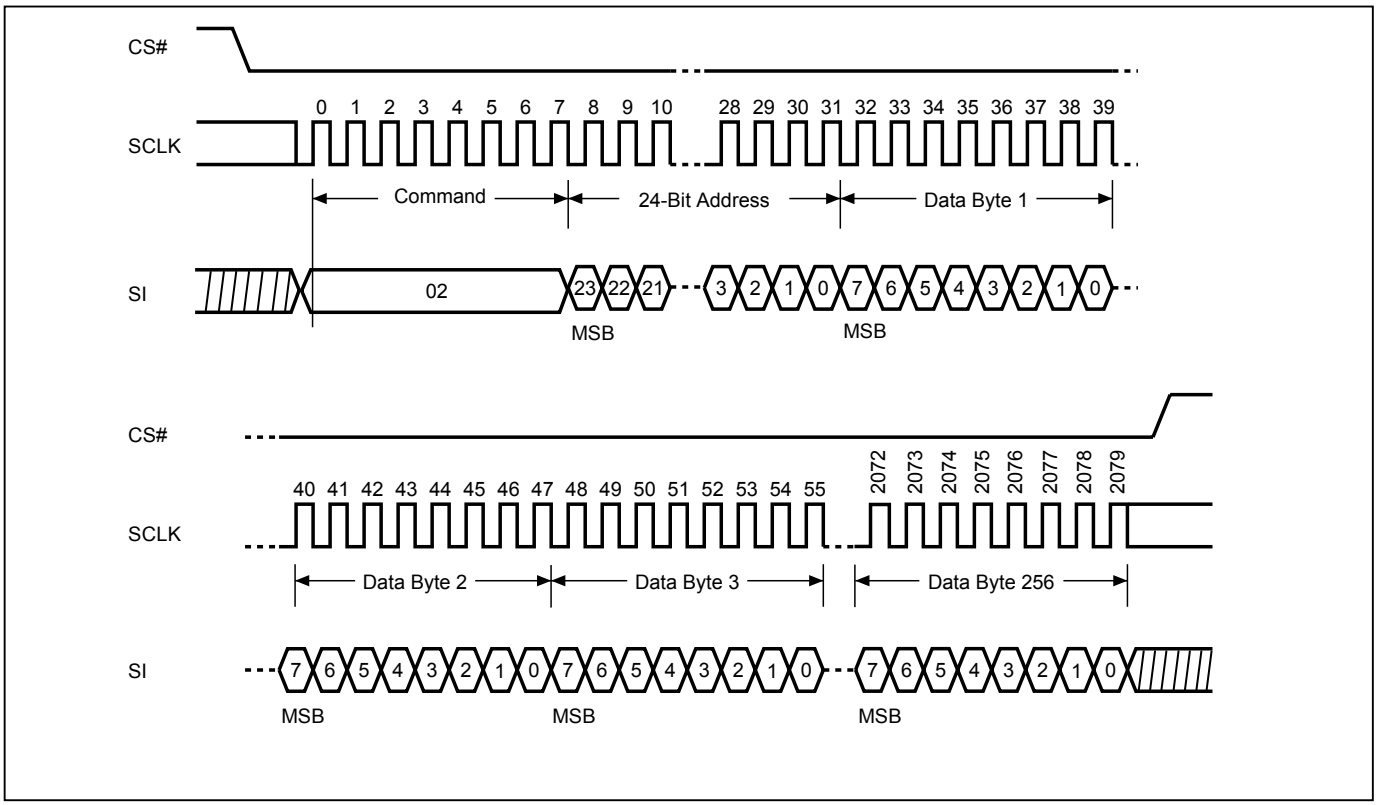


Figure 24. 4 x I/O Page Program (4PP) Sequence (Command 38)

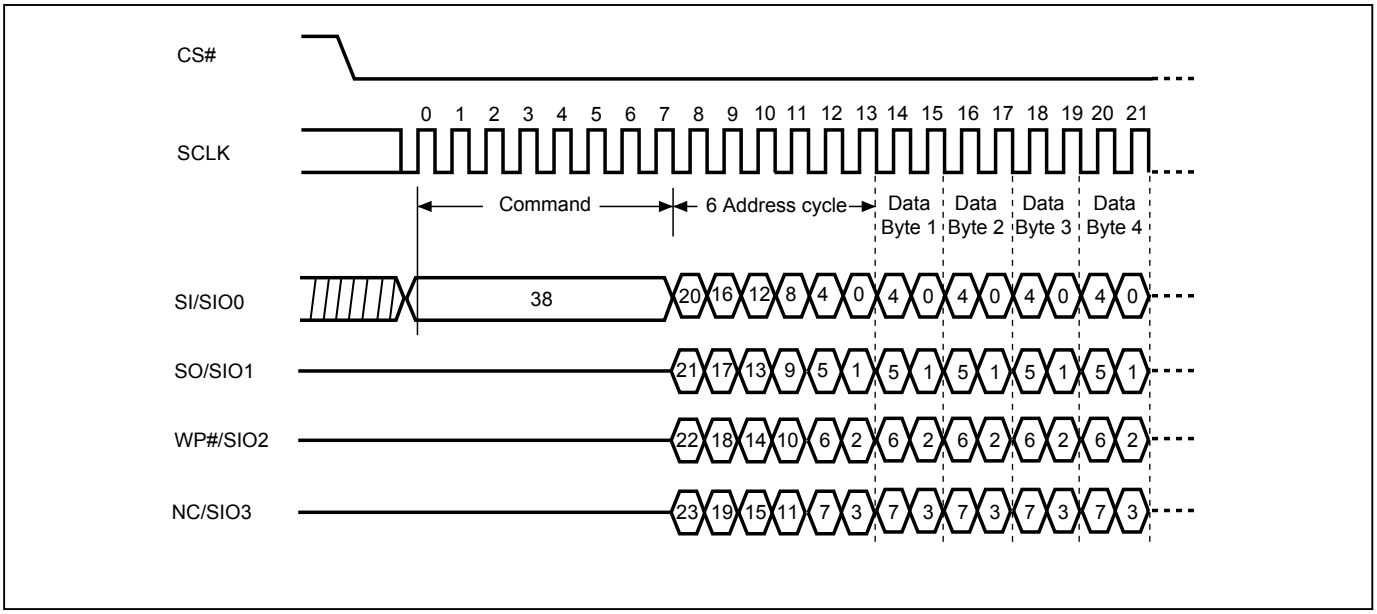
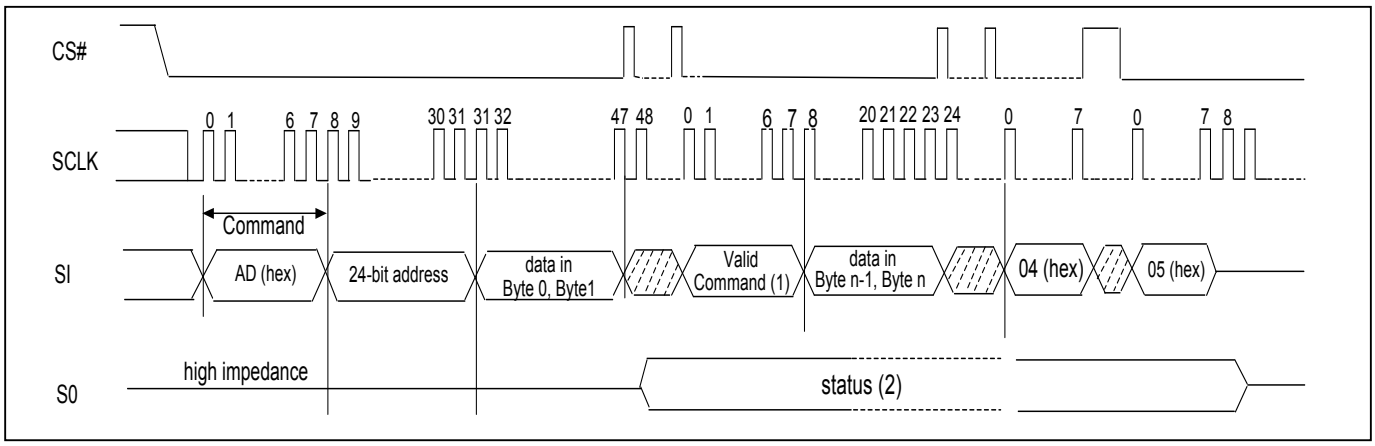
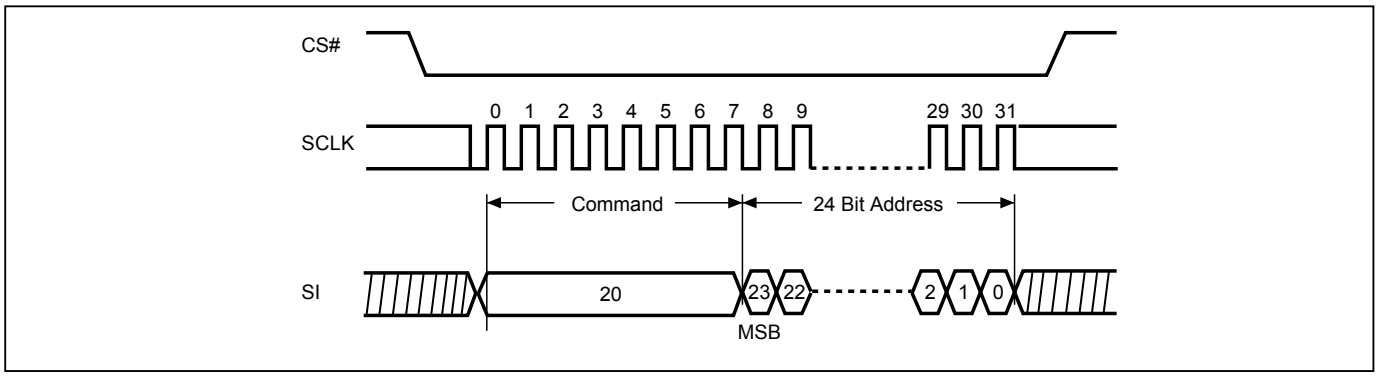


Figure 25. Continously Program (CP) Mode Sequence with Hardware Detection (Command AD)



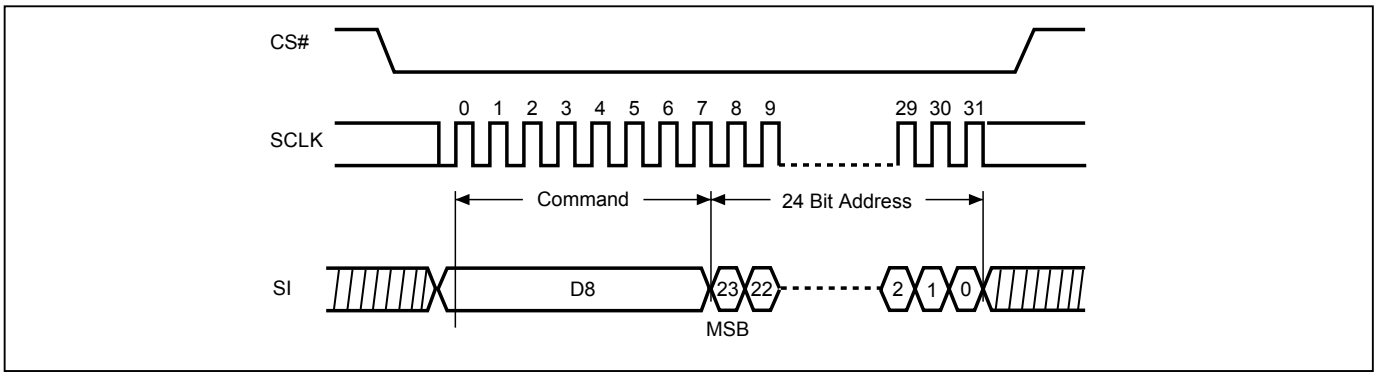
Note: (1) During CP mode, the valid commands are CP command (AD hex), WRDI command (04 hex), RDSR command (05 hex), and RDSCUR command (2B hex).
(2) Once an internal programming operation begins, CS# goes low will drive the status on the SO pin and CS# goes high will return the SO pin to tri-state.
(3) To end the CP mode, either reaching the highest unprotected address or sending Write Disable (WRDI) command (04 hex) may achieve it and then it is recommended to send RDSR command (05 hex) to verify if CP mode is ended.

Figure 26. Sector Erase (SE) Sequence (Command 20)



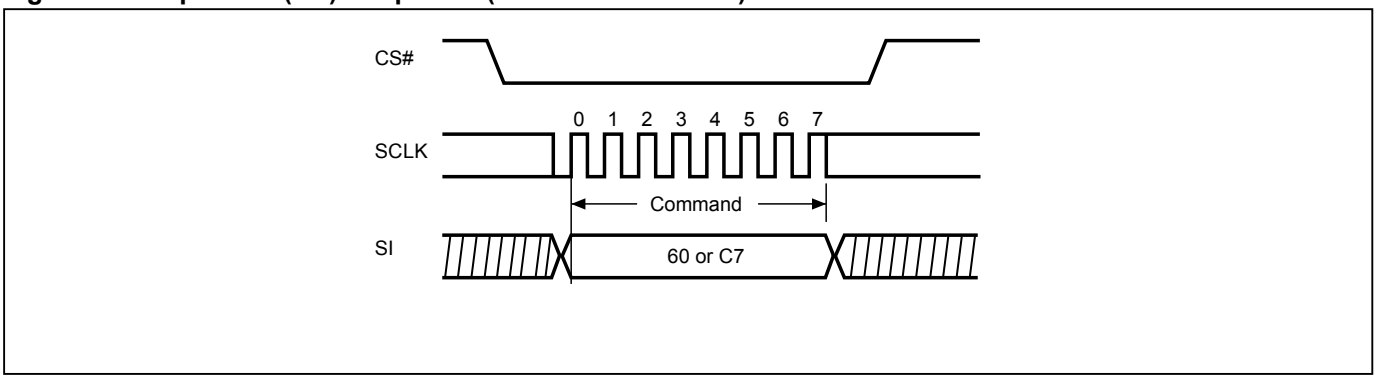
Note: SE command is 20(hex).

Figure 27. Block Erase (BE) Sequence (Command D8)



Note: BE command is D8(hex).

Figure 28. Chip Erase (CE) Sequence (Command 60 or C7)



Note: CE command is 60(hex) or C7(hex).

Figure 29. Deep Power-down (DP) Sequence (Command B9)

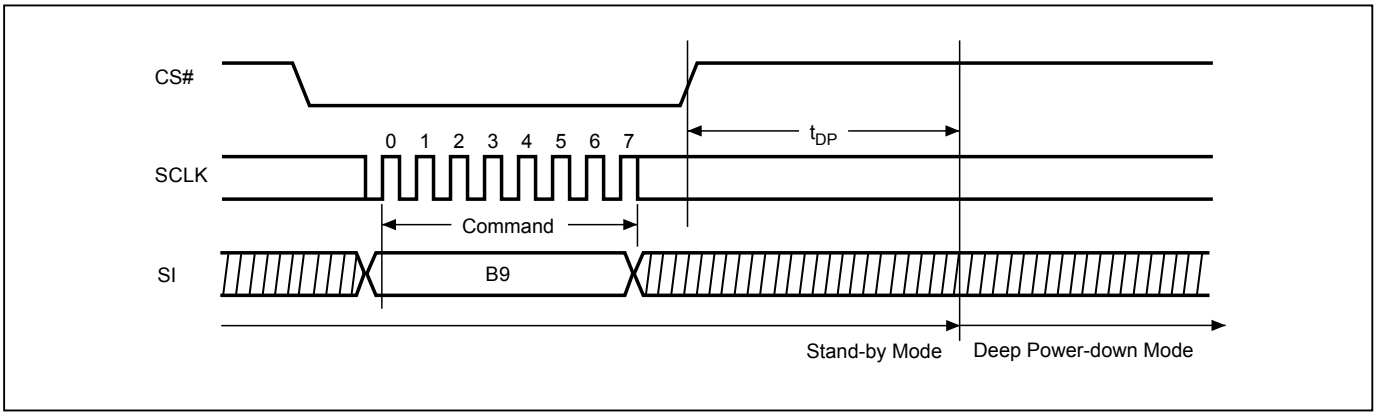
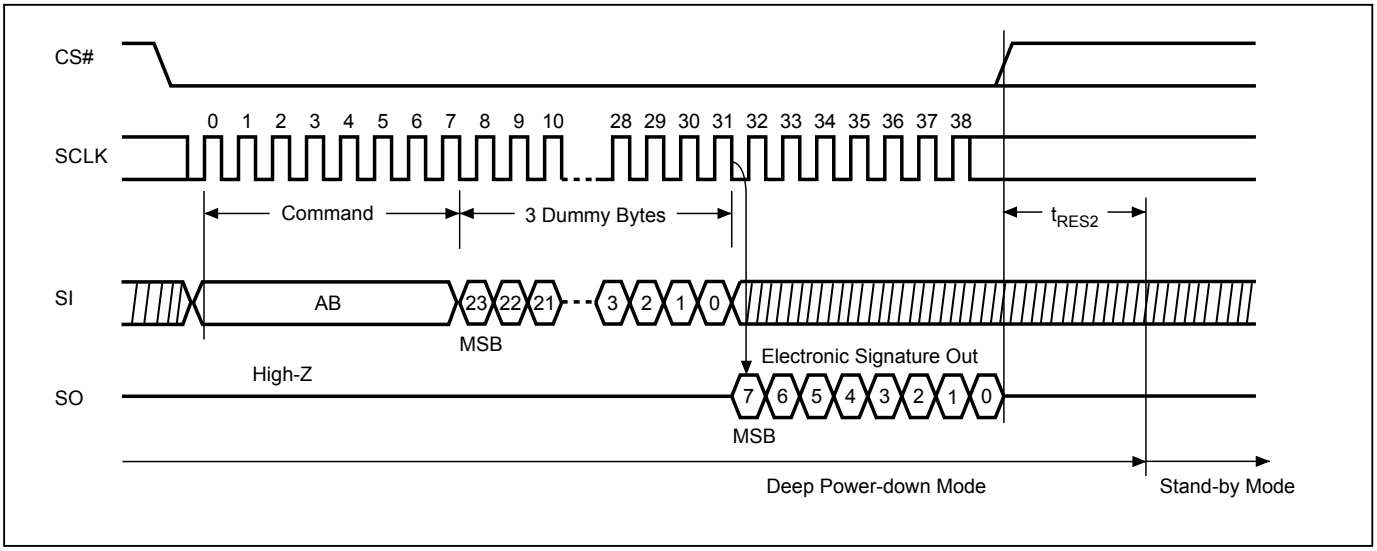


Figure 30. Release from Deep Power-down and Read Electronic Signature (RES) Sequence (Command AB)



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Figure 31. Release from Deep Power-down (RDP) Sequence (Command AB)

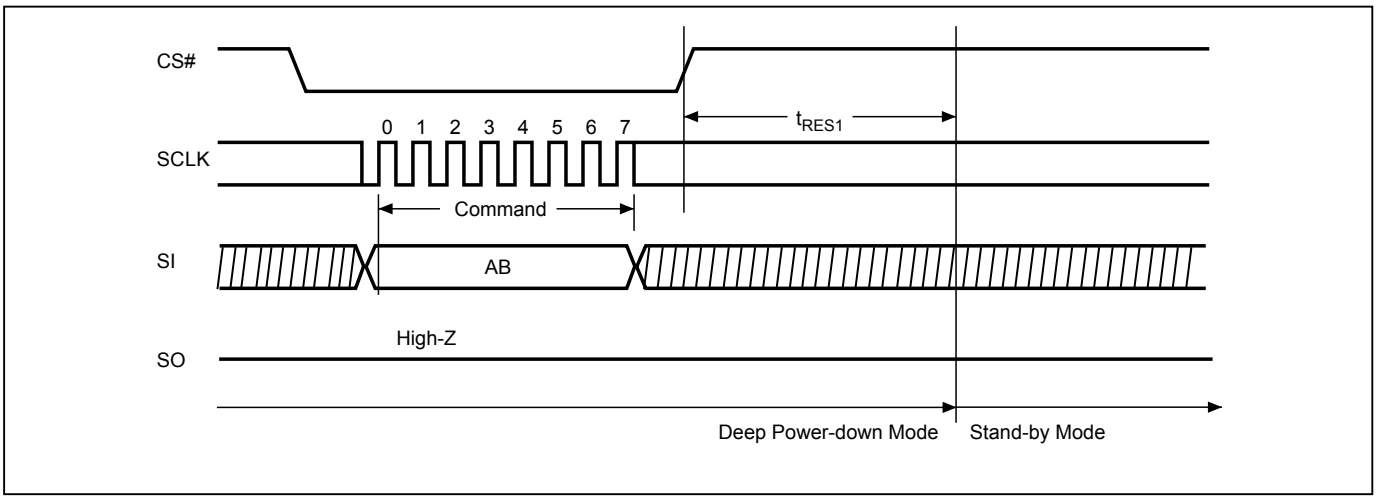
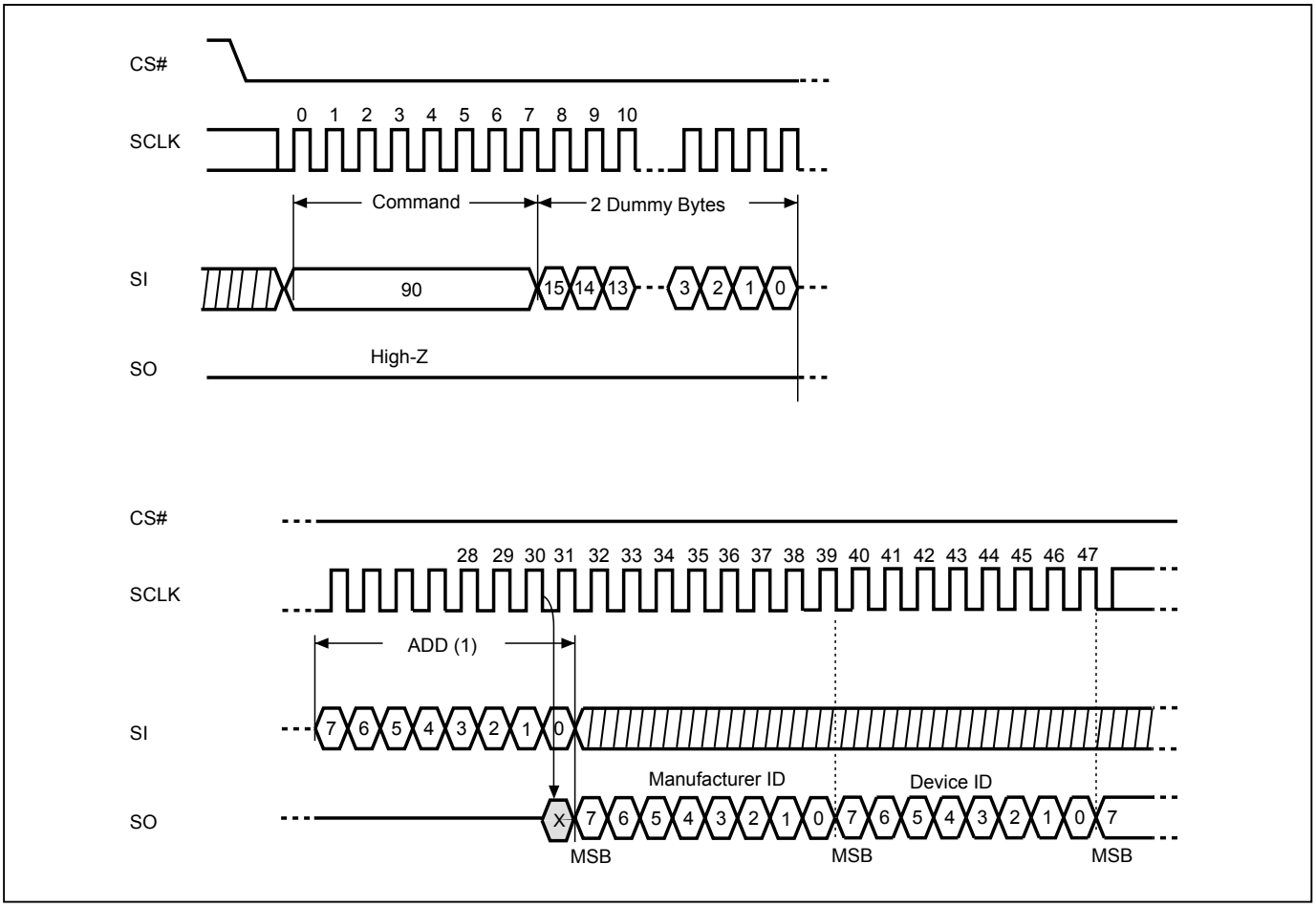


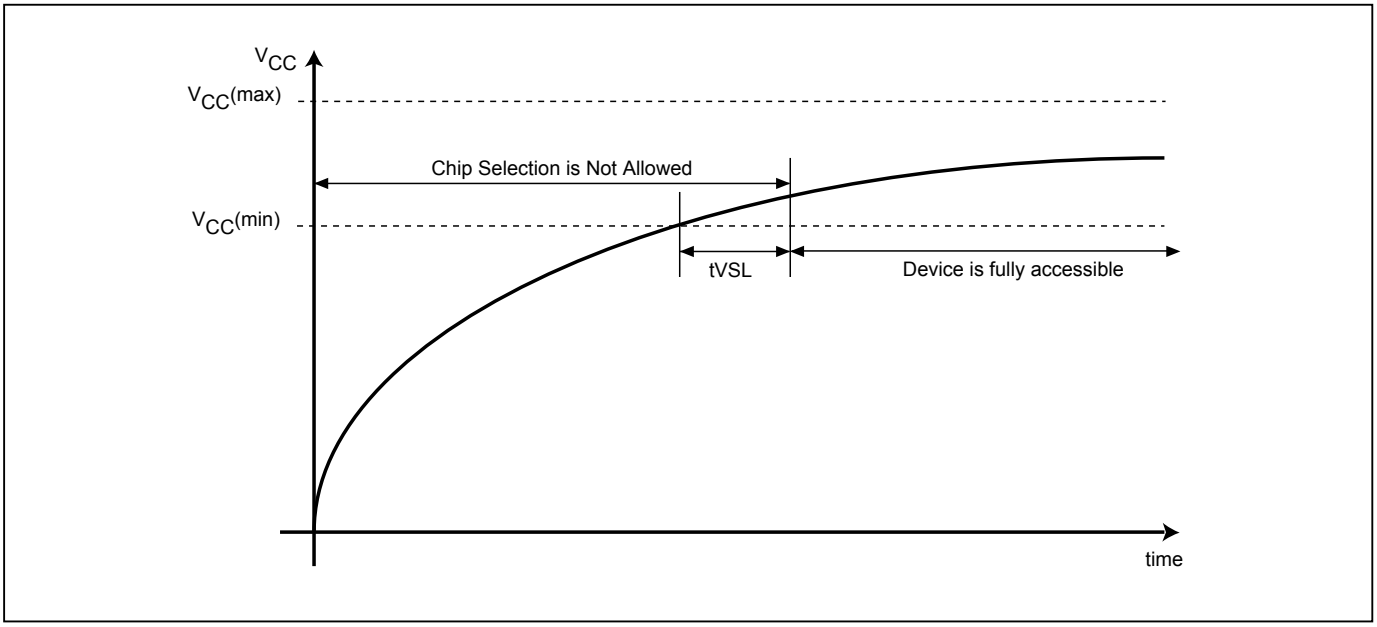
Figure 32. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90 or EF or DF)



Notes:
(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first
(2) Instruction is either 90(hex) or EF(hex) or DF(hex).

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Figure 33. Power-up Timing



Note: VCC (max.) is 3.6V and VCC (min.) is 2.7V.

Table 9. Power-Up Timing

Symbol	Parameter	Min.	Max.	Unit
tVSL(1)	VCC(min) to CS# low	200		us

Note: 1. The parameter is characterized only.

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

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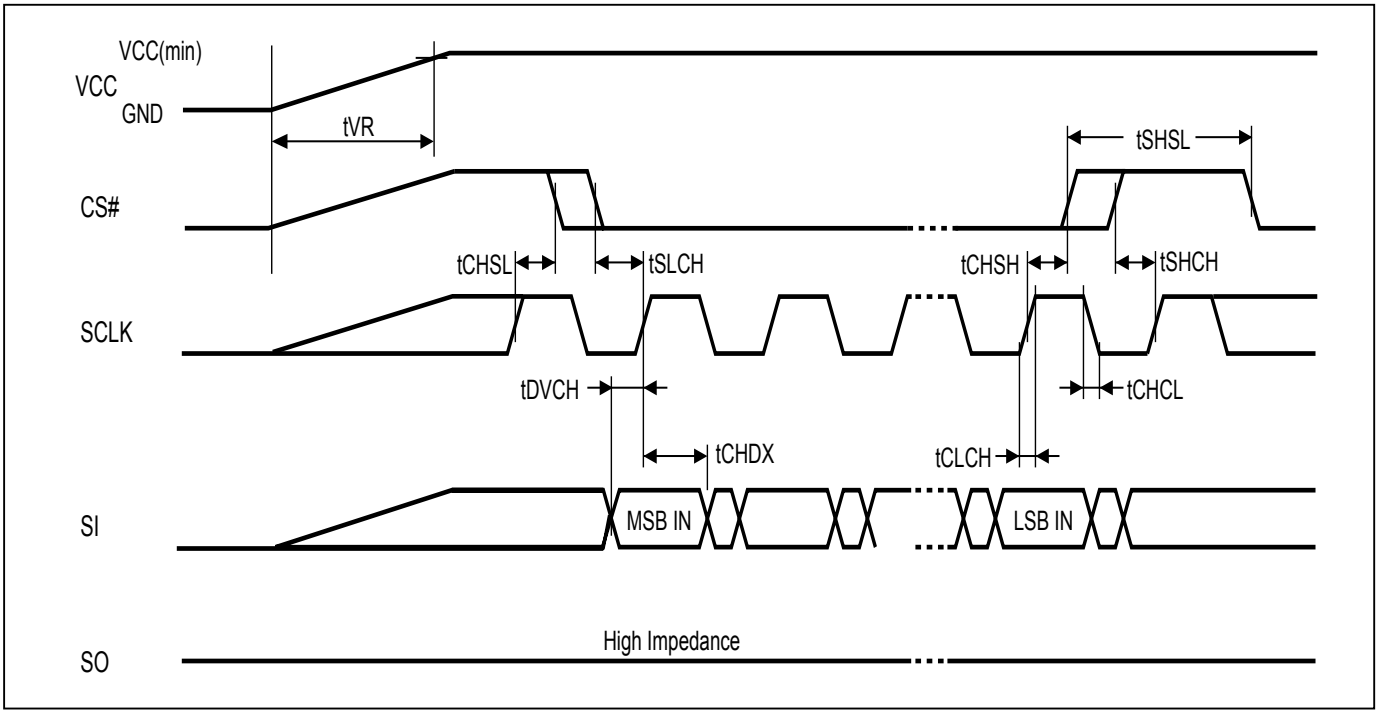
OPERATING CONDITIONS

At Device Power-Up and Power-Down

AC timing illustrated in Figure 34 and Figure 35 are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 34. AC Timing at Device Power-Up

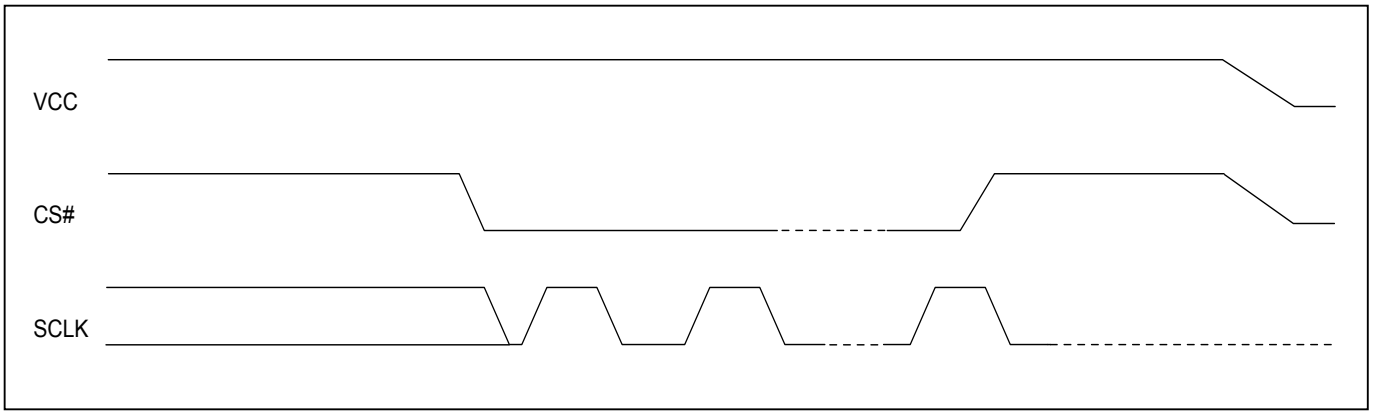


Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1	20	500000	us/V

Notes :
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to "AC CHARACTERISTICS" table.

Figure 35. Power-Down Sequence

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.



ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	Min.	TYP. (1)	Max. (2)	UNIT
Chip Unprotect		40	100	ms
Sector Erase Cycle Time		60	300	ms
Block Erase Cycle Time		0.7	2	s
Chip Erase Cycle Time		25	50	s
Byte Program Time (via page program command)		9	300	us
Page Program Cycle Time		1.4	5	ms
Erase/Program Cycle		100,000		cycles
Block Write Lock Protection		9	300	us

Note:
1. Typical program and erase time assumes the following conditions: 25°C, 3.3V, and checker board pattern.
2. Under worst conditions of 85°C and 2.7V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
4. Erase/Program cycles comply with JEDEC: JESD-47 & JESD22-A117 standard.

DATA RETENTION

PARAMETER	Condition	Min.	Max.	UNIT
Data retention	55˚C	20		years

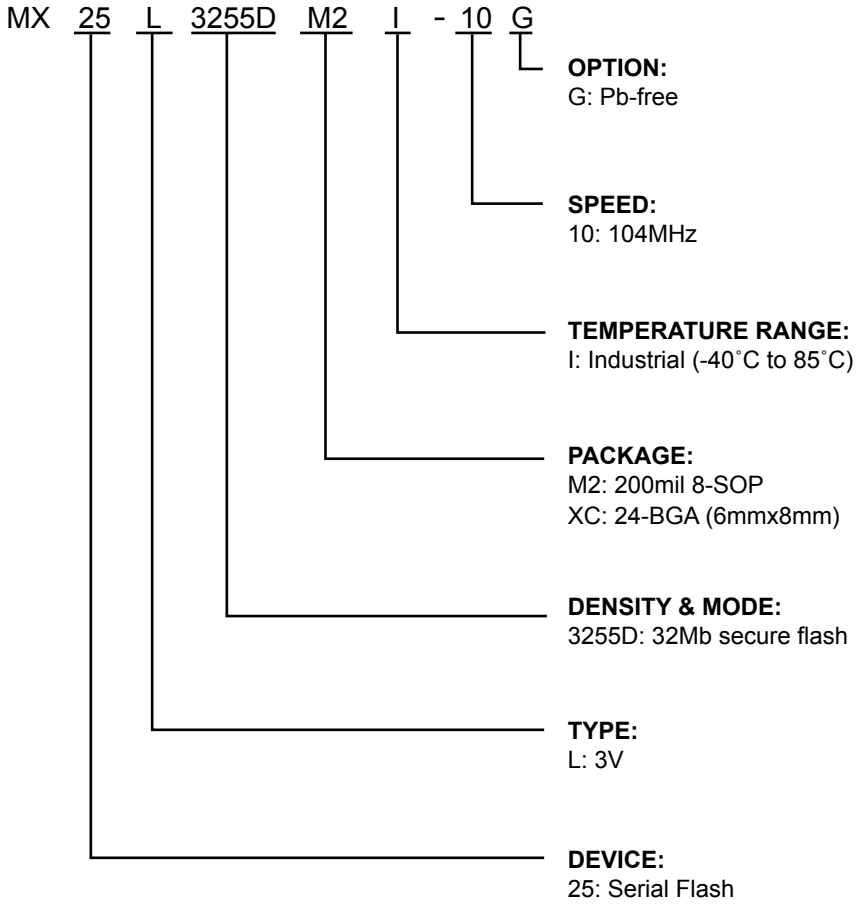
LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on all power pins, SI, CS#	-1.0V	2 VCCmax
Input Voltage with respect to GND on SO	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time.		

ORDERING INFORMATION

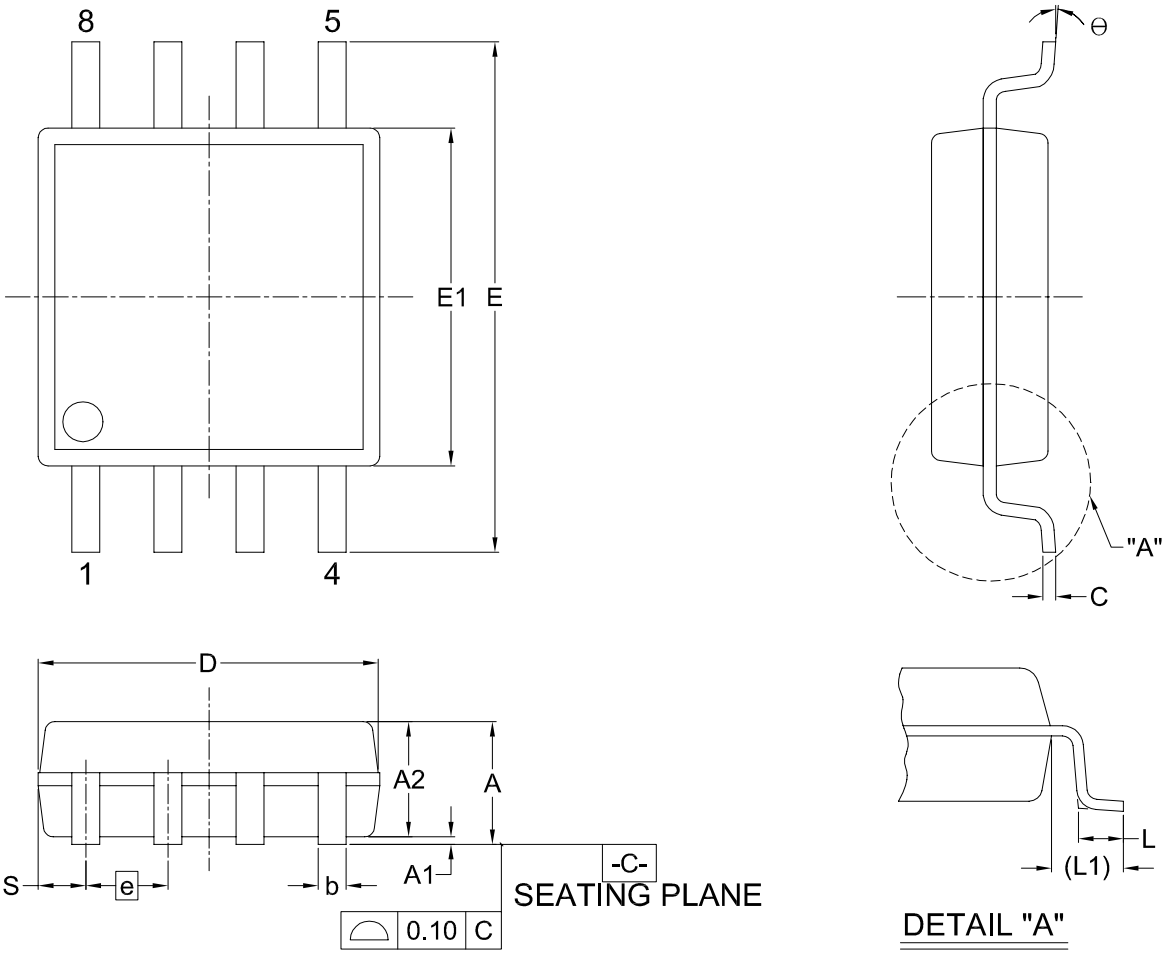
PART NO.	CLOCK (MHz)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (uA)	TEMPERATURE	PACKAGE	Remark
MX25L3255DM2I-10G	104	25	20	-40°C~85°C	8-SOP (200mil)	Pb-free
MX25L3255DXCI-10G	104	25	20	-40°C~85°C	24-BGA (6mmx8mm)	Pb-free

PART NAME DESCRIPTION



PACKAGE INFORMATION

Doc. Title: Package Outline for SOP 8L 200MIL (official name - 209MIL)

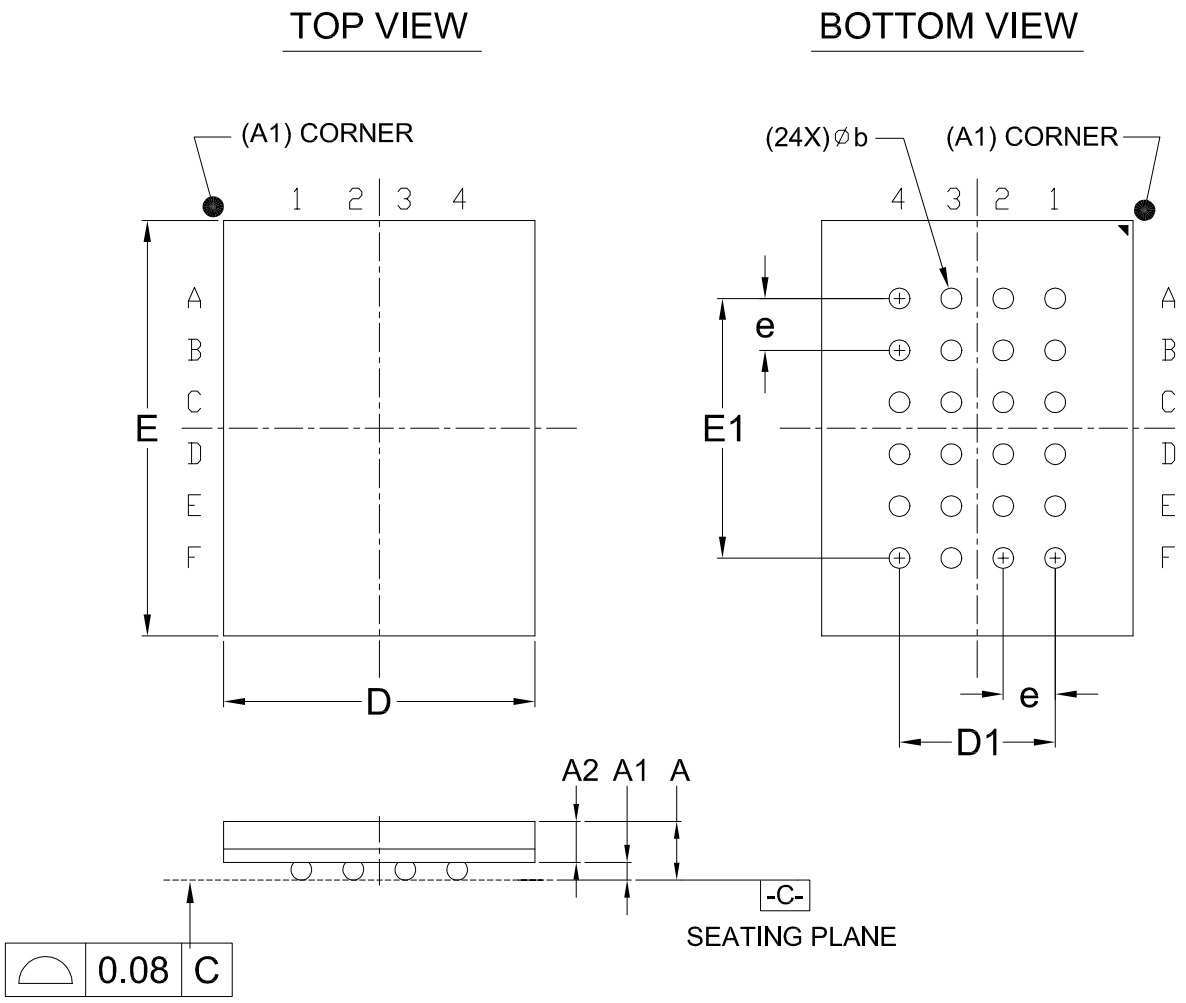


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.05	1.70	0.36	0.19	5.13	7.70	5.18	---	0.50	1.21	0.62	0
	Nom.	---	0.15	1.80	0.41	0.20	5.23	7.90	5.28	1.27	0.65	1.31	0.74	5
	Max.	2.16	0.20	1.91	0.51	0.25	5.33	8.10	5.38	---	0.80	1.41	0.88	8
Inch	Min.	---	0.002	0.067	0.014	0.007	0.202	0.303	0.204	---	0.020	0.048	0.024	0
	Nom.	---	0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050	0.026	0.052	0.029	5
	Max.	0.085	0.008	0.075	0.020	0.010	0.210	0.319	0.212	---	0.031	0.056	0.035	8

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-1406	2				

Doc. Title: Package Outline for CSP 24BALL (6x8x1.2MM, BALL PITCH 1.0MM, BALL DIAMETER 0.4MM)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	—	0.25	0.65	0.35	5.90	—	7.90	—	---
	Nom.	—	0.30	---	0.40	6.00	3.00	8.00	5.00	1.00
	Max.	1.20	0.35	---	0.45	6.10	—	8.10	—	---
Inch	Min.	—	0.010	0.026	0.014	0.232	—	0.311	—	---
	Nom.	—	0.012	---	0.016	0.236	0.120	0.315	0.200	0.039
	Max.	0.047	0.014	---	0.018	0.240	—	0.319	—	---

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-4257	1	MO-216			

REVISION HISTORY

Revision No.	Description	Page	Date
0.01	1. Added 24-ball BGA package	P6,8,45,46 P48	DEC/10/2008
	2. Added Read Block Write Lock status (RDBLOCK)	P16,18,34	
	3. Modified Figure 19. 4 x I/O Read Mode Sequence (Command EB)	P36	
0.02	1. Removed "Low Vcc write inhibit" function	P5,10,26, 47,51	MAR/11/2009
	2. Changed "ADVANCED INFORMATION" into "Preliminary"	P5	
	3. Revised Read Status Register and added QE/SRWD bit	P18	
	4. Revised AC charateristics: tCH (1) and tCL (1) 5/5 to 4.5/4.5	P30	
	5. Removed "Advanced information"	P45-46	
	6. Removed QE bit/SRWD bit status register information	P18,22	
	7. Removed ICC3	P29	
	8. Modified tCH/tCL from 4.5/4.5ns to 4.7/4.7ns	P30	
	9. Modified data retention from 10 years to 20 years	P5	
0.03	1. Aligned to complete version		MAR/13/2009
1.0	1. Removed "Preliminary"	P5	MAR/18/2010
	2. Corrected wrong memory type ID data	P17	
	3. Removed loading from clock rate	P5,28,30	
	4. Removed undefined spec: tQLQH and tQHQL	P31	
	5. Modified Figure 32. AC Timing at Device Power-Up	P43	
	6. Added Figure 33. Power-Down Sequence	P44	
1.1	1. Added DREAD mode/QREAD mode	P5,14,15,20 P21,37,39	SEP/09/2010
	2. Modified Storage Temperature from -55°C to 125°C to -65°C to 150°C	P28	
	3. Modified Figure 26	P41	
	4. Added table for DATA RETENTION	P47	

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