ROHM GROUP
LAPIS SEMICONDUCTOR

FEDD51V17400F-03
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MSM51V17400F

4,194,304-Word × 4-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

DESCRIPTION

The MSM51V17400F is a 4,194,304-word × 4-bit dynamic RAM fabricated in LAPIS Semiconductor's silicon-gate CMOS technology. The MSM51V17400F achieves high integration, high-speed operation, and low-power consumption because LAPIS Semiconductor manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM51V17400F is available in a 26/24-pin plastic TSOP.

FEATURES

· 4,194,304-word × 4-bit configuration
· Single 3.3V power supply, ±0.3V tolerance
· Input : LVTTL compatible, low input capacitance
· Output : LVTTL compatible, 3-state
· Refresh : 2048 cycles/32ms
· Fast page mode, read modify write capability
· CAS before RAS refresh, hidden refresh, RAS-only refresh capability
· Packages:
26/24-pin 300mil plastic TSOP (P-TSOP(2)26/24-300-1.27-Z3K)

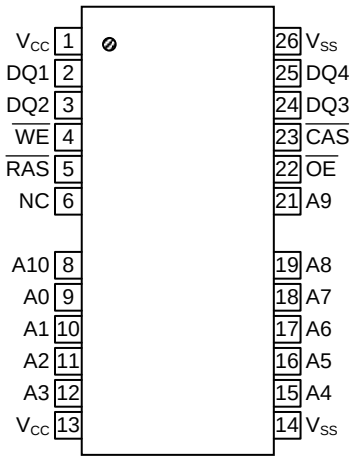
PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSM51V17400F-60	60ns	30ns	15ns	15ns	110ns	324mW	1.8mW

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PIN CONFIGURATION (TOP VIEW)



26/24-Pin Plastic TSOP
(K Type)

Pin Name	Function
A0–A10	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
DQ1–DQ4	Data Input/Data Output
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (3.3V)
V_{SS}	Ground (0V)
NC	No Connection

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

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ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–0.5 to V_{CC}+ 0.5	V
Voltage V_{CC} Supply relative to V_{SS}	V_{CC}	–0.5 to 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_{D*}	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	–55 to 150	°C

*: Ta = 25°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3[*1]	V
Input Low Voltage	V_{IL}	– 0.3[*2]	—	0.8	V

Notes: *1. The input voltage is V_{CC} + 1.0V when the pulse width is less than 20ns (the pulse width is with respect to the point at which V_{CC} is applied).

*2. The input voltage is V_{SS} – 1.0V when the pulse width is less than 20ns (the pulse width respect to the point at which V_{SS} is applied).

PIN CAPACITANCE

(Vcc = 3.3V ± 0.3V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Min.	Unit
Input Capacitance (A0 – A10)	C_{IN1}	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 – DQ4)	$C_{I/O}$	—	7	pF

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DC CHARACTERISTICS

(V_{CC} = 3.3V ± 0.3V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	MSM51V17400 F-60		Unit	Note
			Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} = –2.0mA	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA	0	0.4	V	
Input Leakage Current	I_{LI}	0V ≤ V_I ≤ V_{CC} +0.3V; All other pins not under test = 0V	– 10	10	µA	
Output Leakage Current	I_{LO}	DQ disable 0V ≤ V_O ≤ V_{CC}	– 10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min.	—	90	mA	1,2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	—	2	mA	1
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2V	—	0.5		
Average Power Supply Current ($\overline{RAS}$-only Refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = Min.	—	90	mA	1,2
Power Supply Current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, DQ = enable	—	5	mA	1
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ = cycling, $\overline{CAS}$ before $\overline{RAS}$	—	90	mA	1,2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = Min.	—	70	mA	1,3

Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. The address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. The address can be changed once or less while $\overline{CAS}$ = V_{IH}.

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AC CHARACTERISTICS (1/2)

(V_{CC} = 3.3V ± 0.3V, Ta = 0 to 70°C) Note1,2,3,11,12

Parameter	Symbol	MSM51V17400 F-60		Unit	Note
		Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	110	—	ns	
Read Modify Write Cycle Time	t_{RWC}	155	—	ns	
Fast Page Mode Cycle Time	t_{PC}	40	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRWC}	85	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	60	ns	4, 5, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	15	ns	4, 5
Access Time from Column Address	t_{AA}	—	30	ns	4, 6
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	35	ns	4
Access Time from $\overline{OE}$	t_{OEA}	—	15	ns	4
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	—	ns	4
$\overline{CAS}$ to Data Output Buffer Turn-off Delay Time	t_{OFF}	0	15	ns	7
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	15	ns	7
Transition Time	t_T	3	50	ns	3
Refresh Period	t_{REF}	—	32	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	100,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	ns	
$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	t_{ROH}	15	—	ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	ns	6
Row Address Set-up Time	t_{ASR}	0	—	ns	

AC CHARACTERISTICS (2/2)

(V_{CC} = 3.3V ± 0.3V ,Ta = 0 to 70°C) Note1,2,3,11,12

Parameter	Symbol	MSM51V17400 F-60		Unit	Note
		Min.	Max.		
Row Address Hold Time	t_{RAH}	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	ns	
Column Address Hold Time	t_{CAH}	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	ns	8
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	0	—	ns	8
Write Command Set-up Time	t_{WCS}	0	—	ns	9
Write Command Hold Time	t_{WCH}	10	—	ns	
Write Command Pulse Width	t_{WP}	10	—	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	ns	
Data-in Set-up Time	t_{DS}	0	—	ns	10
Data-in Hold Time	t_{DH}	10	—	ns	10
$\overline{OE}$ to Data-in Delay Time	t_{OED}	15	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	40	—	ns	9
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	55	—	ns	9
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	85	—	ns	9
$\overline{CAS}$ Precharge $\overline{WE}$ Delay Time	t_{CPWD}	60	—	ns	9
$\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge	t_{RPC}	5	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	10	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRP}	10	—	ns	
$\overline{WE}$ Hold Time from $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRH}	10	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Set-up Time (Test Mode)	t_{WTS}	10	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Hold Time (Test Mode)	t_{WTH}	10	—	ns	

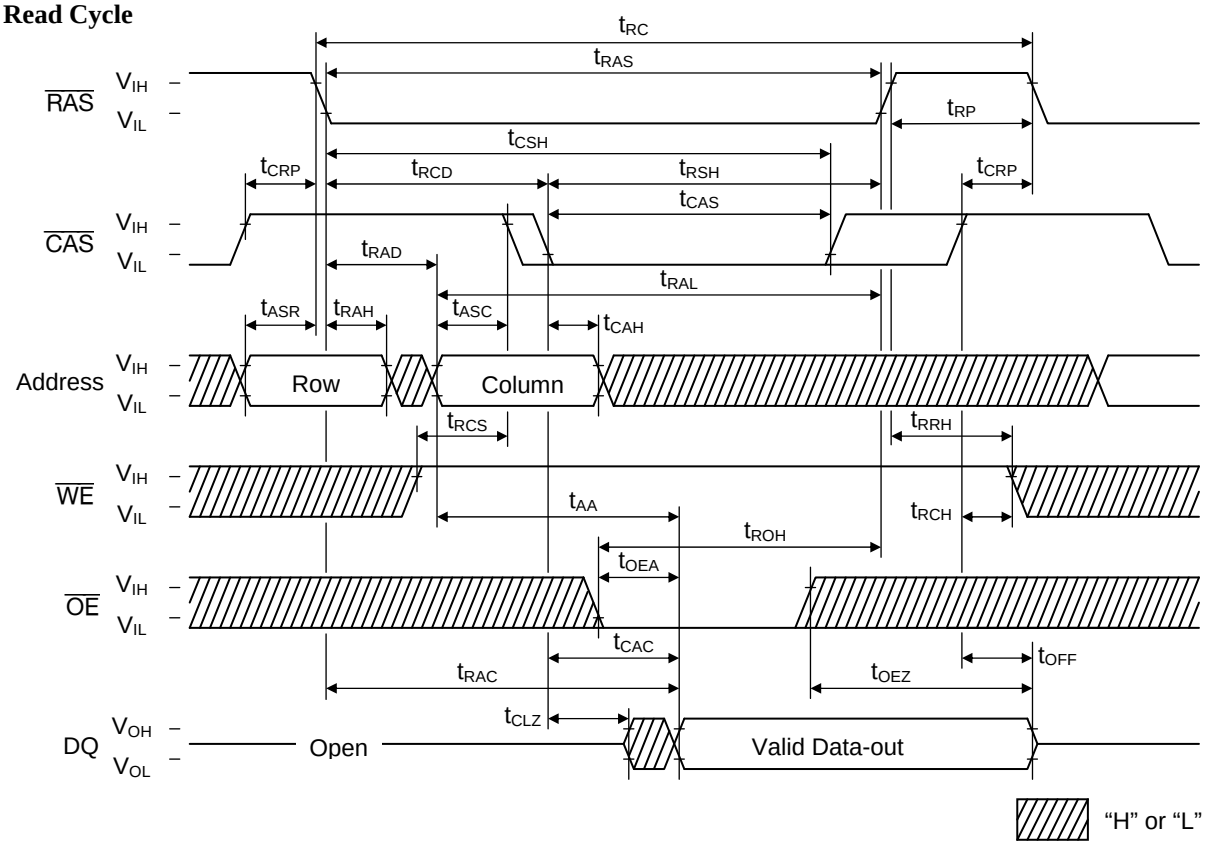
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Notes:
1. A start-up delay of 200μs is required after power-up, followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.
2. The AC characteristics assume t_T = 5ns.
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL}.
4. This parameter is measured with a load circuit equivalent to 1TTL load and 100pF.
5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC}.
6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA}.
7. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the output achieved the open circuit condition and are not referenced to output voltage levels.
8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$(Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
10. These parameters are referenced to the $\overline{CAS}$, leading edges in an early write cycle, and to the $\overline{WE}$ leading edge in an $\overline{OE}$ control write cycle, or a read modify write cycle.
11. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. In a test CA9 and CA10 are not used and each DQ pin now access 4-bit locations. Since all 4 DQ pins are used, a total 16 data bits can be written in parallel into the memory array. In a read cycle, if 4 data bits are equal, the DQ pin will indicate a high level. If the 4 data bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
12. In a test mode read cycle, the value of access time parameter is delayed for 5ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.

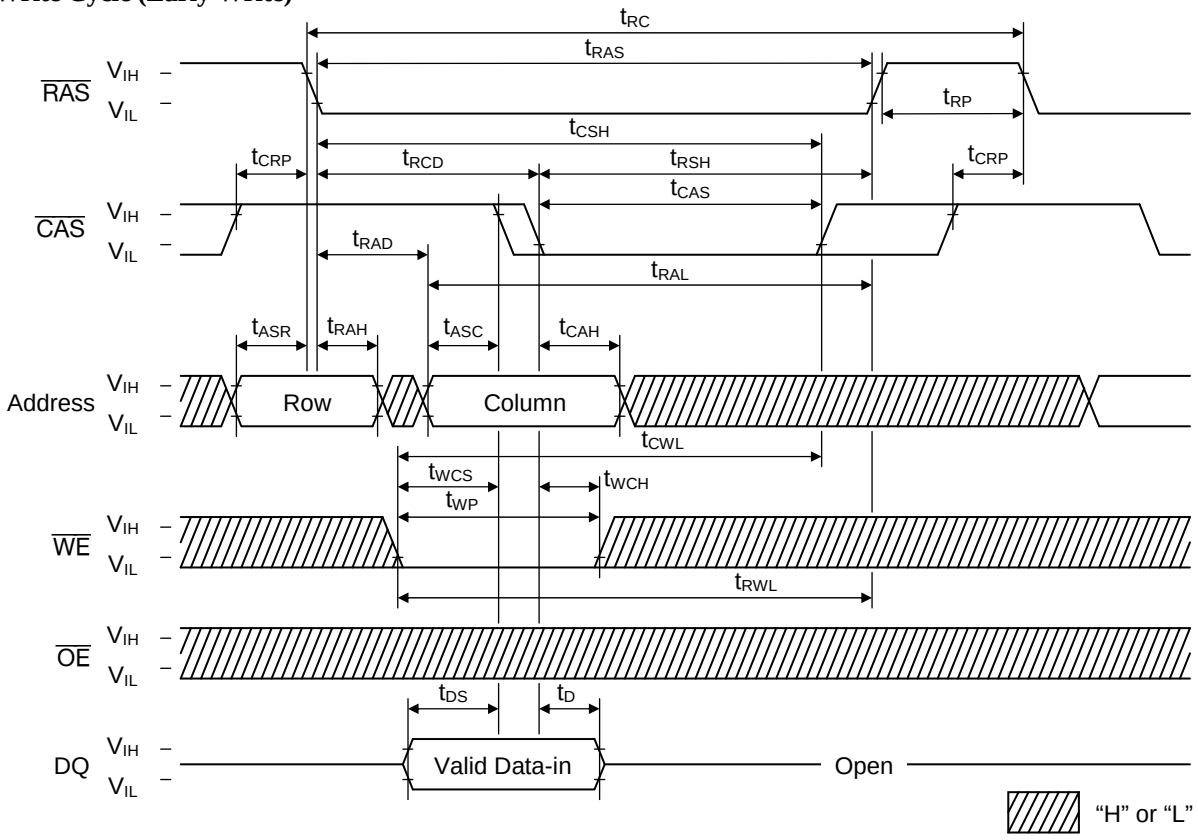
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TIMING CHART

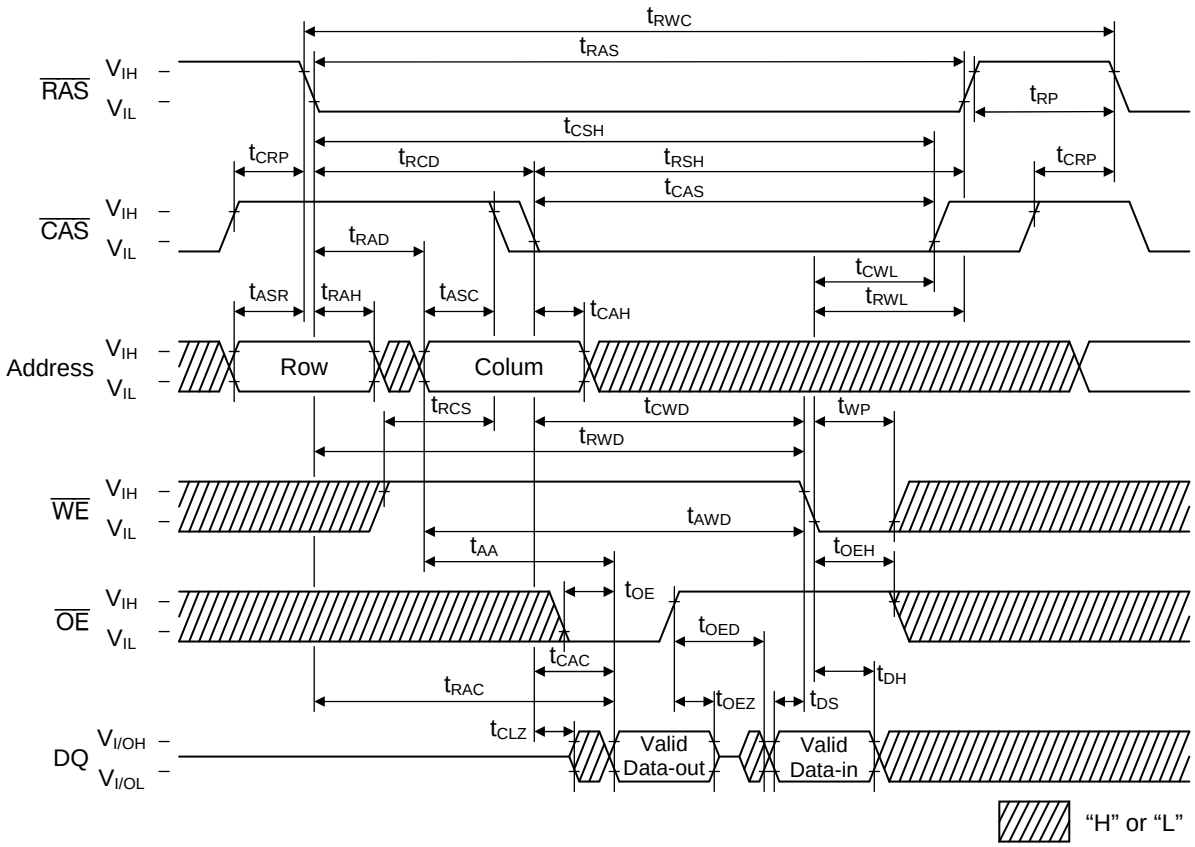
Read Cycle



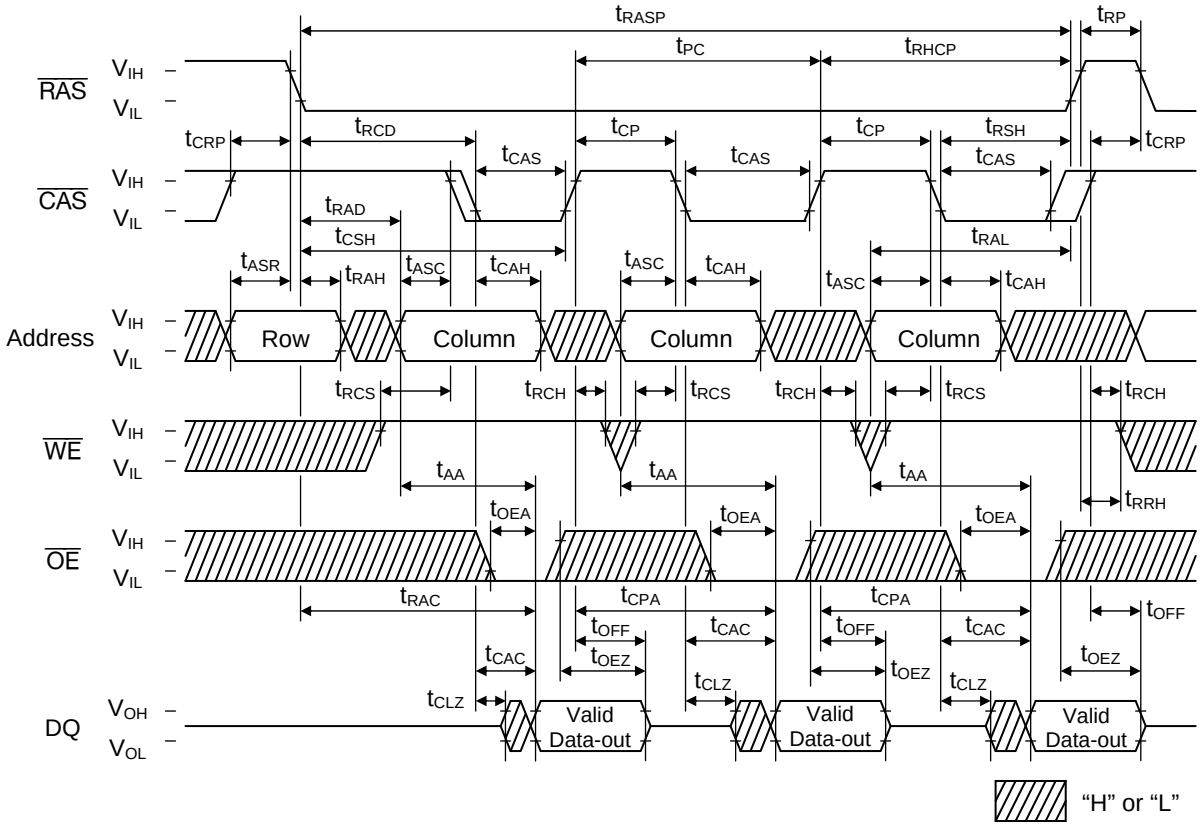
Write Cycle (Early Write)



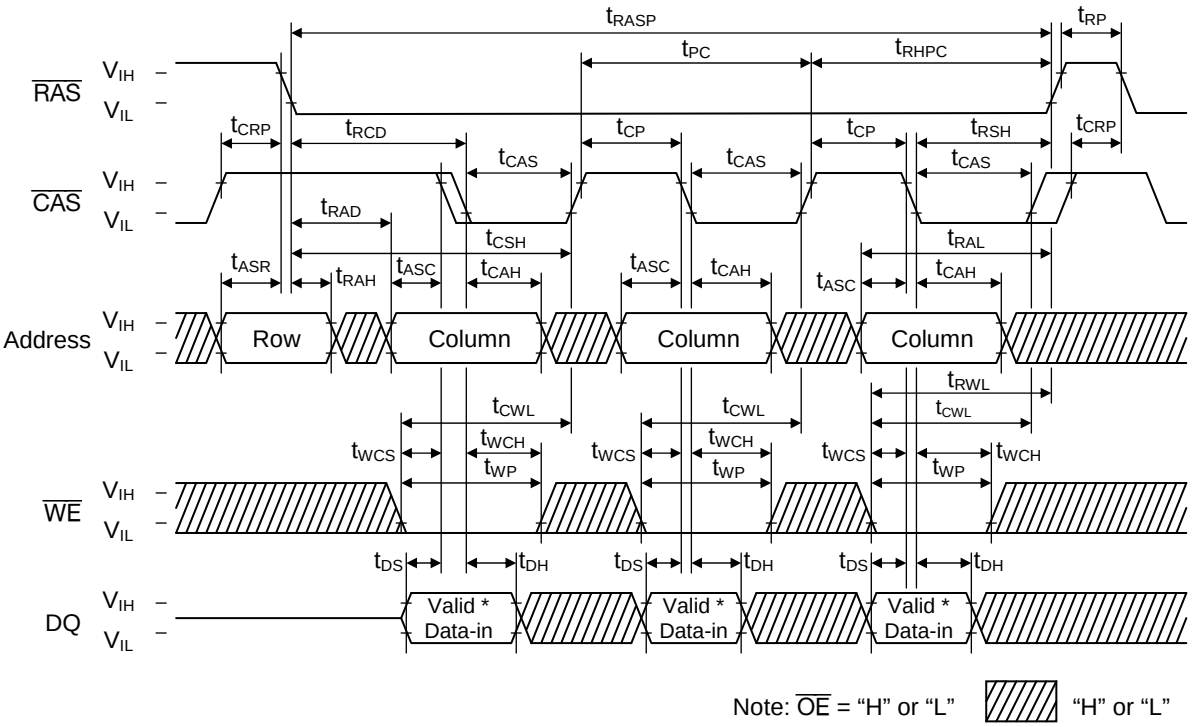
Read Modify Write Cycle



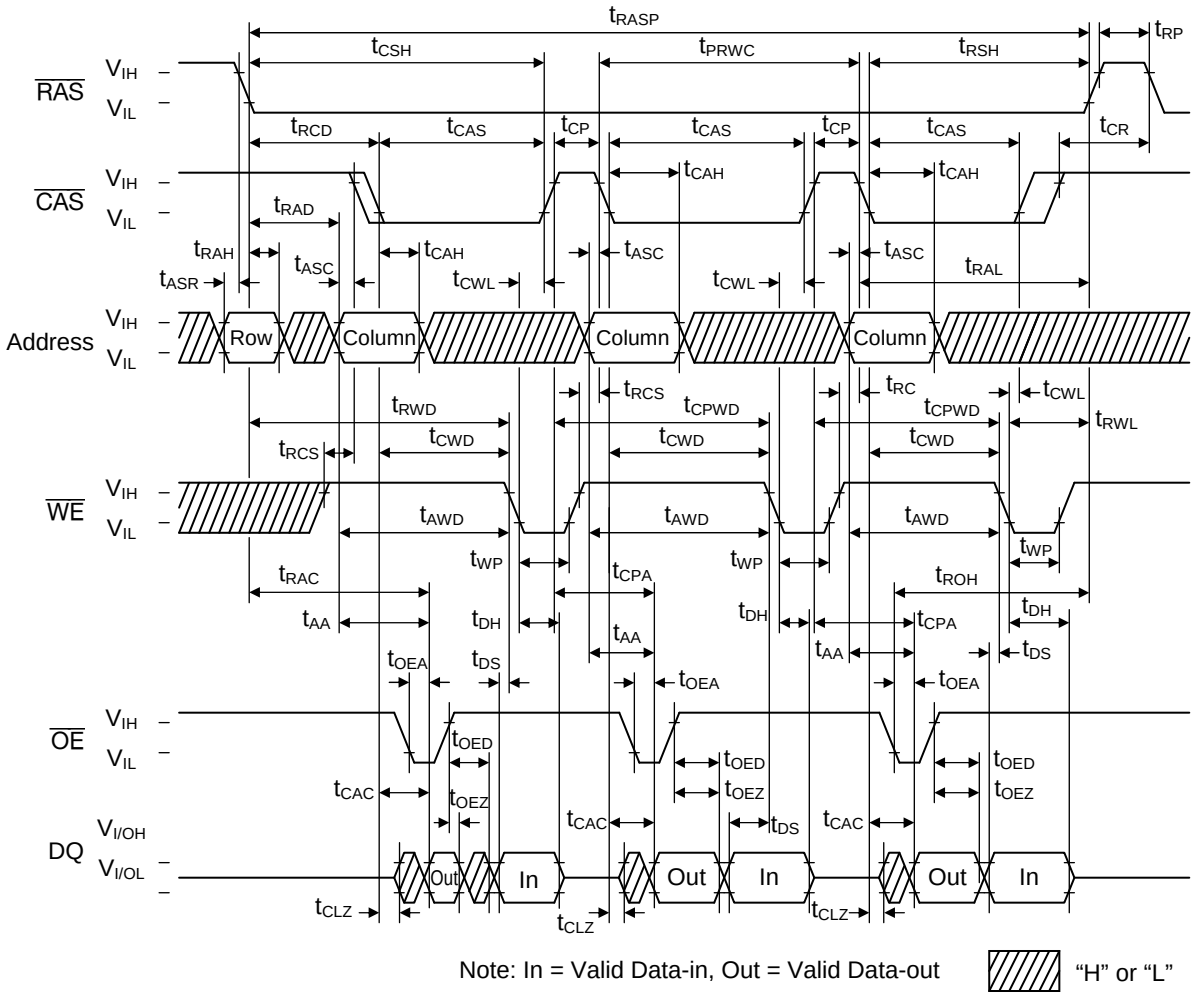
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle (Early Write)

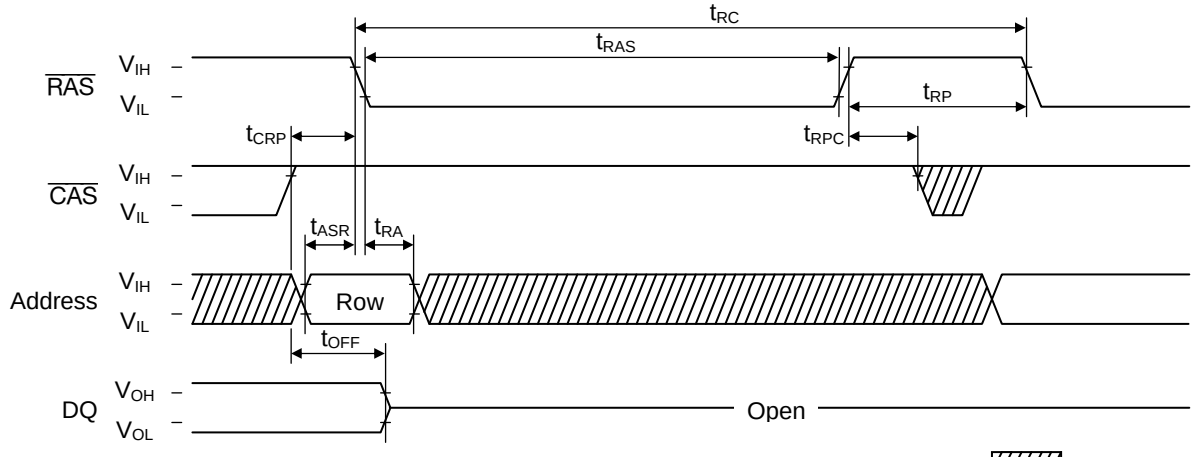


Fast Page Mode Read Modify Write Cycle



Note: In = Valid Data-in, Out = Valid Data-out "H" or "L"

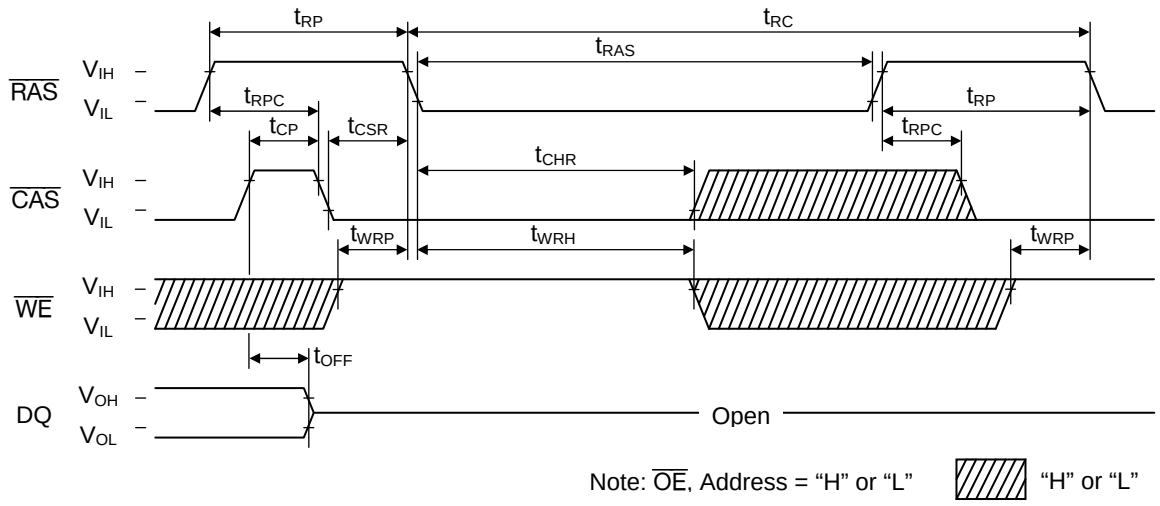
RAS-only Refresh Cycle



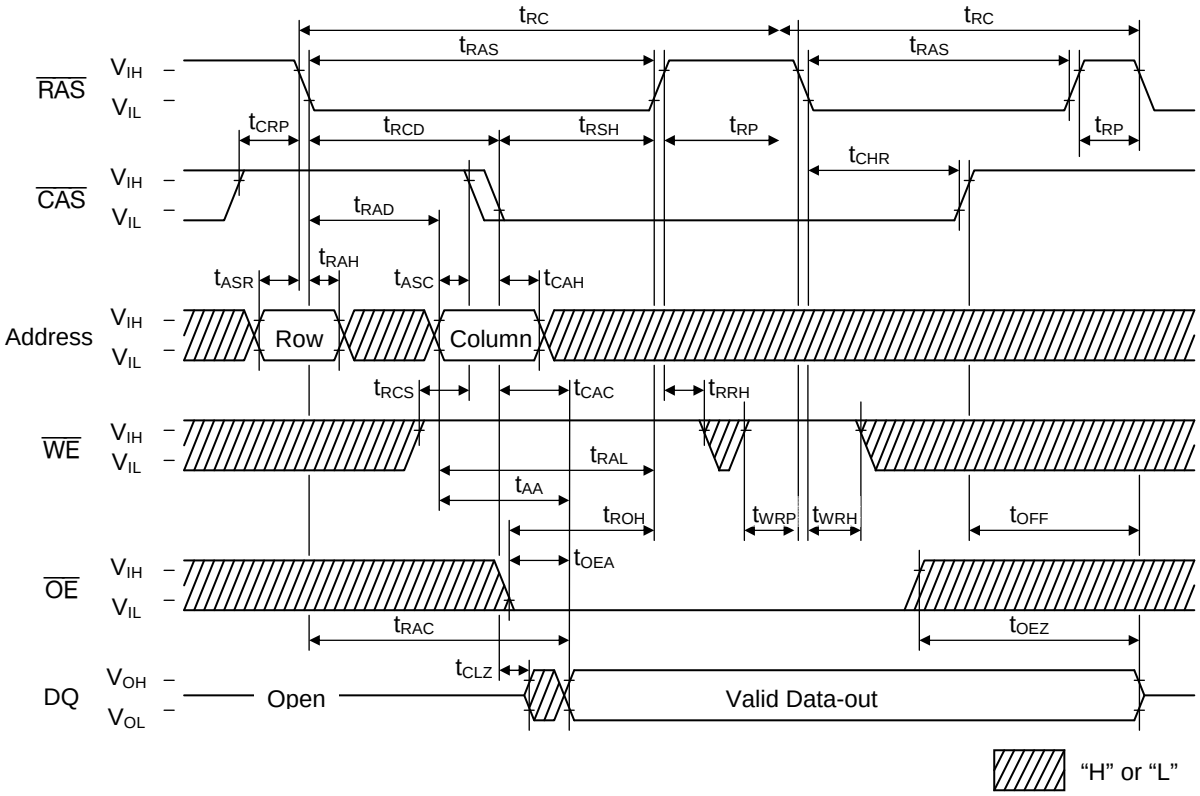
Note: WE, OE = "H" or "L" "H" or "L"

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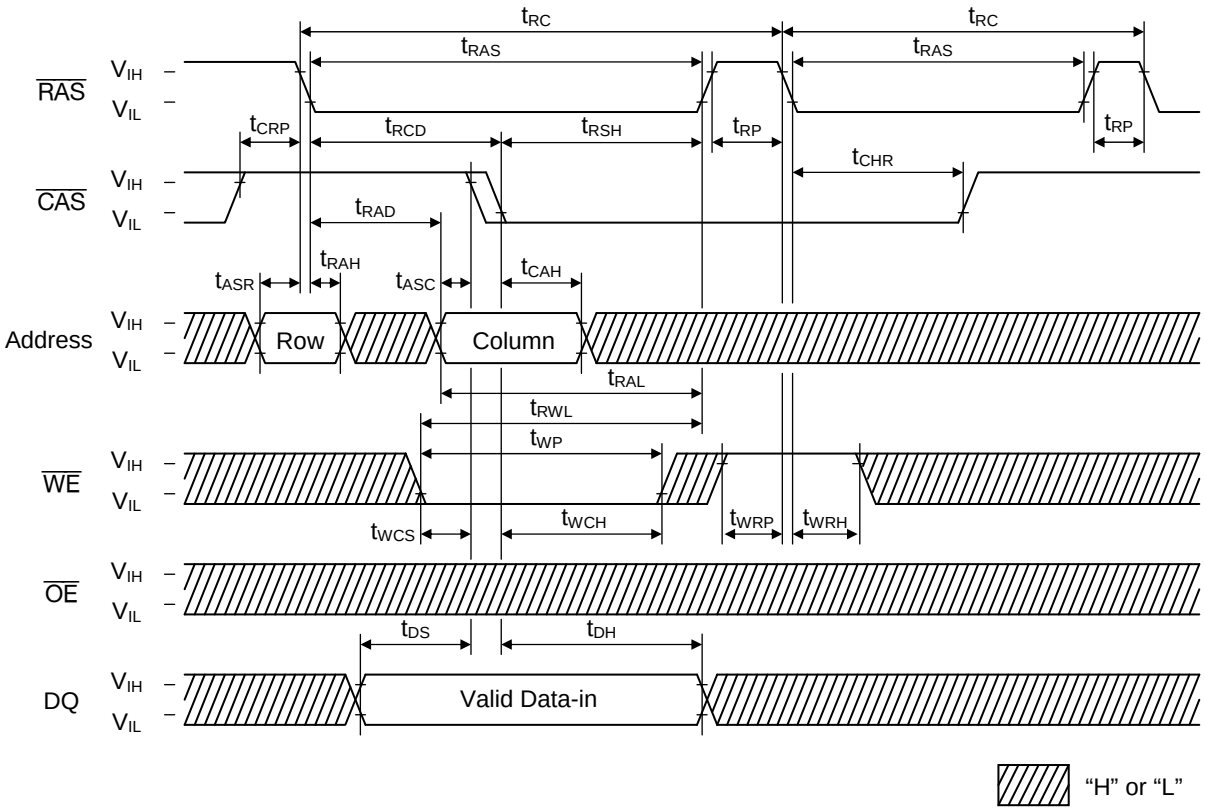
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



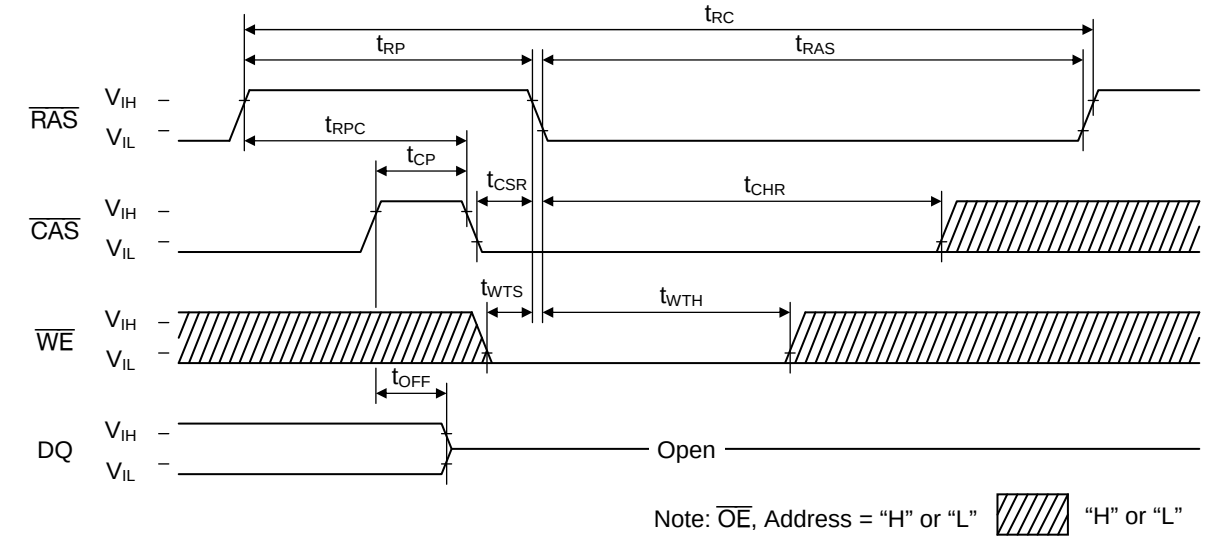
Hidden Refresh Read Cycle



Hidden Refresh Write Cycle



Test Mode-in Cycle



REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDD51V17400F-01	Mar.23, 2004	–	–	Final edition 1 from FEDD5117400F-04
FEDD51V17400F-02	Feb.01, 2012	1,2 1 3	1,2 1 –	Deleted SOJ26/24 Changed pb-free device name Deleted Block diagram
FEDD51V17400F-03	Nov. 27, 2014	1	1	Changed package code(Cu frame) Added ROHM logo mark Changed company Logo

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