# MR20H40 / MR25H40

**MR20H40 -** 50MHz/20ns $^{t}$SCK 4Mb SPI Interface MRAM
**MR25H40 -** 40MHz/25ns $^{t}$SCK 4Mb SPI Interface MRAM
For more information on product options, see **"Table 16 – Ordering Part Numbers" on page 25**.

## FEATURES

- No write delays
- Unlimited write endurance
- Data retention greater than 20 years
- Automatic data protection on power loss
- Fast, simple SPI interface, up to 50 MHz clock rate with MR20H40.
- 3.0 to 3.6 Volt power supply range
- Low-current sleep mode
- Commercial (0 to 70°C), Industrial (-40 to 85°C), Extended (-40 to 105°C), and AEC-Q100 Grade 1 (-40 to 125°C) temperature range options.
- Available in 8-pin DFN or 8-pin DFN Small Flag, RoHS-compliant packages.
- Direct replacement for serial EEPROM, Flash, and FeRAM
- MSL Level 3



8-DFN



8-DFN Small Flag

RoHS

## DESCRIPTION

MR2xH40 is a family of 4,194,304-bit magnetoresistive random access memory (MRAM) devices organized as 524,288 words of 8 bits. They are the ideal memory solution for applications that must store and retrieve data and programs quickly using a small number of I/O pins. They have serial EEPROM and serial Flash compatible read/write timing with no write delays and unlimited read/write endurance. Unlike other serial memories, with the MR2xH40 family both reads and writes can occur randomly in memory with no delay between writes.

The MR2xH40 family provides highly reliable data storage over a wide range of temperatures. The MR20H40 (50MHz) is offered with Industrial (-40° to 85 °C) range. The MR25H40 (40MHz) is offered with Commercial (0 to 70°C), Industrial (-40° to 85 °C), Extended (-40 to 105°C), and AEC-Q100 Grade 1 (-40°C to 125 °C) operating temperature range options.

Both are available in a 5 x 6mm, 8-pin DFN package. The pinout is compatible with serial SRAM, EEPROM, Flash, and FeRAM products.

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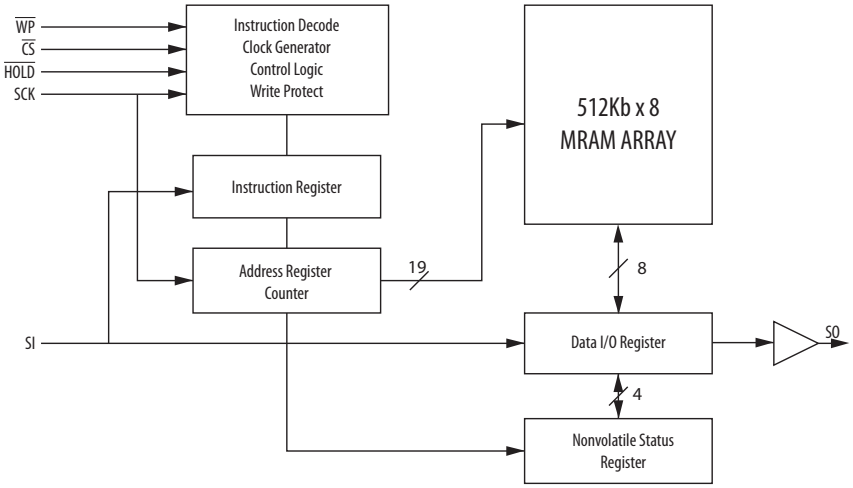


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## OVERVIEW

The MR2xH40 family is an SPI interface MRAM family with a memory array logically organized as 512Kx8 using the four pin interface of chip select ($\overline{CS}$), serial input (SI), serial output (SO) and serial clock (SCK) of the serial peripheral interface (SPI) bus. The MRAM implements a subset of commands common to SPI EEPROM and SPI Flash components. This allows the SPI MRAM to replace these components in the same socket and interoperate on a shared SPI bus. The SPI MRAM offers superior write speed, unlimited endurance, low standby & operating power, and simple, reliable data retention compared to other serial memory alternatives.

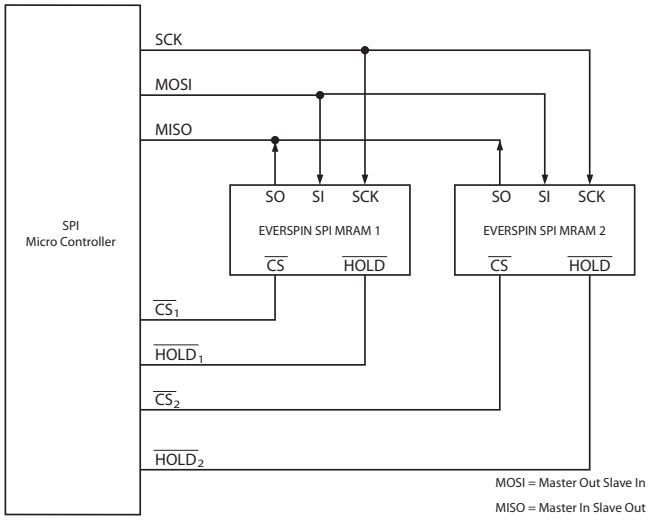
### Figure 1 – Block Diagram




## System Configuration

Single or multiple devices can be connected to the bus as shown in Figure 2. Pins SCK, SO and SI are common among devices. Each device requires $\overline{CS}$ and $\overline{HOLD}$ pins to be driven separately.

### Figure 2 – System Configuration

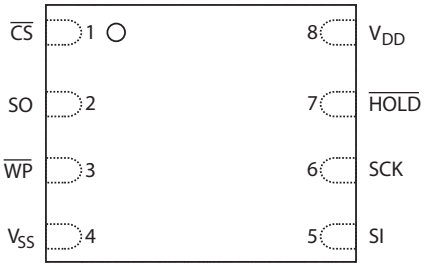





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## Pin Functions

### Figure 3 – DFN Package Pin Diagram (Top View)




### Table 1 – Pin Functions

| Signal Name | Pin | I/O | Function | Description |
|---|---|---|---|---|
| $\overline{CS}$ | 1 | Input | Chip Select | An active low chip select for the serial MRAM. When chip select is high, the memory is powered down to minimize standby power, inputs are ignored and the serial output pin is Hi-Z. Multiple serial memories can share a common set of data pins by using a unique chip select for each memory. |
| SO | 2 | Output | Serial Output | The data output pin is driven during a read operation and remains Hi-Z at all other times. SO is Hi-Z when HOLD is low. Data transitions on the data output occur on the falling edge of SCK. |
| $\overline{WP}$ | 3 | Input | Write Protect | A low on the write protect input prevents write operations to the Status Register. |
| $V_{SS}$ | 4 | Reference | Ground | Power supply ground pin. |
| SI | 5 | Input | Serial Input | All data is input to the device through this pin. This pin is sampled on the rising edge of SCK and ignored at other times. SI can be tied to SO to create a single bidirectional data bus if desired. |
| SCK | 6 | Input | Serial Clock | Synchronizes the operation of the MRAM. The clock can operate up to 50 MHz to shift commands, address, and data into the memory. Inputs are captured on the rising edge of clock. Data outputs from the MRAM occur on the falling edge of clock. The serial MRAM supports both SPI Mode 0 (CPOL=0, CPHA=0) and Mode 3 (CPOL=1, CPHA=1). In Mode 0, the clock is normally low. In Mode 3, the clock is normally high. Memory operation is static so the clock can be stopped at any time. |
| $\overline{HOLD}$ | 7 | Input | Hold | A low on the Hold pin interrupts a memory operation for another task. When $\overline{HOLD}$ is low, the current operation is suspended. The device will ignore transitions on the $\overline{CS}$ and SCK when $\overline{HOLD}$ is low. All transitions of $\overline{HOLD}$ must occur while $\overline{CS}$ is low. |
| $V_{DD}$ | 8 | Supply | Power Supply | Power supply voltage from +3.0 to +3.6 volts. |

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# SPI COMMUNICATIONS PROTOCOL

The MR2xH40 can be operated in either SPI Mode 0 (CPOL=0, CPHA =0) or SPI Mode 3 (CPOL=1, CPHA=1). For both modes, inputs are captured on the rising edge of the clock and data outputs occur on the falling edge of the clock. When not conveying data, SCK remains low for Mode 0; while in Mode 3, SCK is high. The memory determines the mode of operation (Mode 0 or Mode 3) based upon the state of the SCK when $\overline{CS}$ falls.

All memory transactions start when $\overline{CS}$ is brought low to the memory. The first byte is a command code. Depending upon the command, subsequent bytes of address are input. Data is either input or output. There is only one command performed per $\overline{CS}$ active period. $\overline{CS}$ must go inactive before another command can be accepted. To ensure proper part operation according to specifications, it is necessary to terminate each access by raising $\overline{CS}$ at the end of a byte (a multiple of 8 clock cycles from $\overline{CS}$ dropping) to avoid partial or aborted accesses.

## Command Codes

**Table 2 – Command Codes**

| Instruction | Description | Binary Code | Hex Code | Address Bytes | Data Bytes |
|---|---|---|---|---|---|
| WREN | Write Enable | 0000 0110 | 06h | 0 | 0 |
| WRDI | Write Disable | 0000 0100 | 04h | 0 | 0 |
| RDSR [1] | Read Status Register | 0000 0101 | 05h | 0 | 1 |
| WRSR | Write Status Register | 0000 0001 | 01h | 0 | 1 |
| READ | Read Data Bytes | 0000 0011 | 03h | 3 | 1 to ∞ |
| WRITE | Write Data Bytes | 0000 0010 | 02h | 3 | 1 to ∞ |
| SLEEP | Enter Sleep Mode | 1011 1001 | B9h | 0 | 0 |
| WAKE | Exit Sleep Mode | 1010 1011 | ABh | 0 | 0 |

Note:

1. An RDSR command cannot immediately follow a READ command. If an RDSR command immediately follows a READ command, the output data will not be correct. Any other sequence of commands is allowed. If an RDSR command is required immediately following a READ command, it is necessary that another command be inserted before the RDSR is executed. Alternatively, two successive RDSR commands can be issued following the READ command. The second RDSR will output the proper state of the Status Register.

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## Status Register, Memory Protection and Block Write Protection

The status register consists of the 8 bits listed in Table 3. As seen in Table 4, the Status Register Write Disable bit (SRWD) is used in conjunction with bit 1 (WEL) and the Write Protection pin ($\overline{WP}$) to provide hardware memory block protection. Bits BP0 and BP1 define the memory block arrays that are protected as described in Table 5. The fast writing speed of the MR2xH40 does not require write status bits. The state of bits 6,5,4, and 0 can be user modified and do not affect memory operation. All bits in the status register are pre-set from the factory in the "0" state.

**Table 3 – Status Register Bit Assignments**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| SRWD | Don't Care | Don't Care | Don't Care | BP1 | BP0 | WEL | Don't Care |

## Memory Protection Modes

When WEL is reset to 0, writes to all blocks and the status register are protected. When WEL is set to 1, BP0 and BP1 determine which memory blocks are protected. While SRWD is reset to 0 and WEL is set to 1, status register bits BP0 and BP1 can be modified. Once SRWD is set to 1, $\overline{WP}$ must be high to modify SRWD, BP0 and BP1.

**Table 4 – Memory Protection Modes**

| WEL | SRWD | $\overline{WP}$ | Protected Blocks | Unprotected Blocks | Status Register |
|---|---|---|---|---|---|
| 0 | X | X | Protected | Protected | Protected |
| 1 | 0 | X | Protected | Writable | Writable |
| 1 | 1 | Low | Protected | Writable | Protected |
| 1 | 1 | High | Protected | Writable | Writable |



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## Block Protection Modes

The memory enters hardware block protection when the $\overline{WP}$ input is low and the Status Register Write Disable (SRWD) bit is set to 1. The memory leaves hardware block protection only when the $\overline{WP}$ pin goes high. While $\overline{WP}$ is low, the write protection blocks for the memory are determined by the status register bits BP0 and BP1 and cannot be modified without taking the $\overline{WP}$ signal high again.

If the $\overline{WP}$ signal is high (independent of the status of SRWD bit), the memory is in software protection mode. This means that block write protection is controlled solely by the status register BP0 and BP1 block write protect bits and this information can be modified using the WRSR command.

### Table 5 – Block Memory Write Protection

| Status Register | | Memory Contents | |
|---|---|---|---|
| **BP1** | **BP0** | **Protected Area** | **Unprotected Area** |
| 0 | 0 | None | All Memory |
| 0 | 1 | Upper Quarter | Lower Three-Quarters |
| 1 | 0 | Upper Half | Lower Half |
| 1 | 1 | All | None |

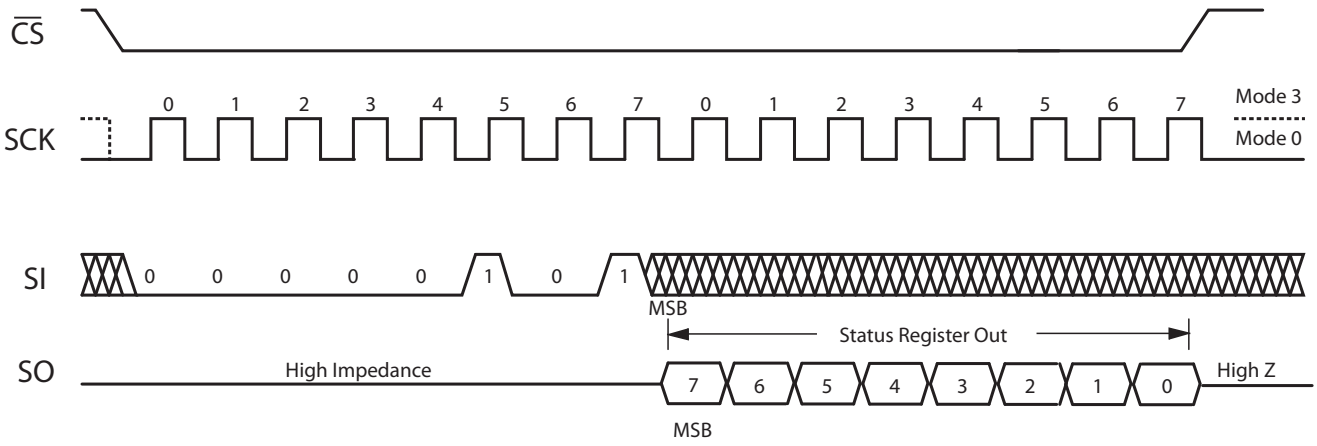


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## Read Status Register (RDSR)

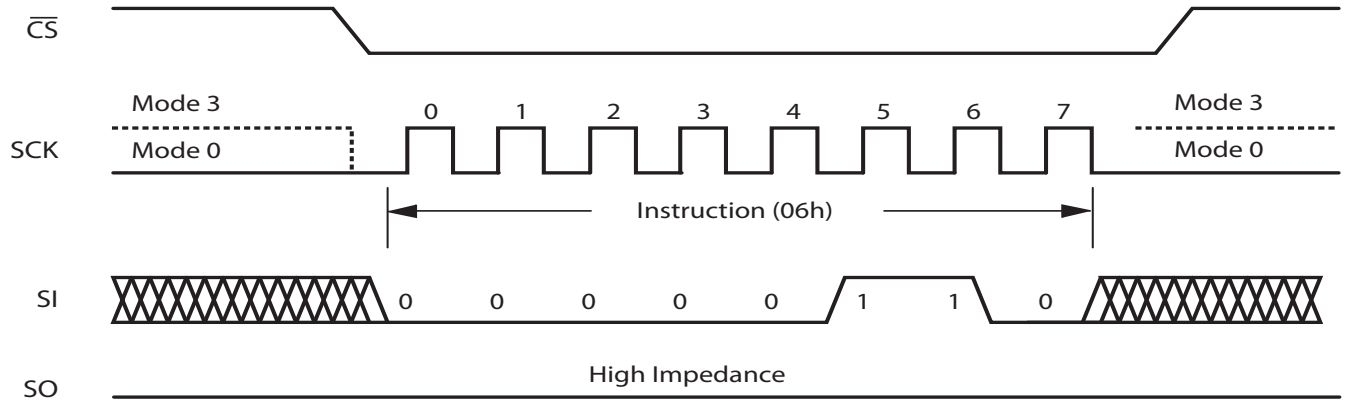
The Read Status Register (RDSR) command allows the Status Register to be read. The Status Register can be read to check the status of write enable latch bit, status register write protect bit, and block write protect bits. For MR2xH40, the write in progress bit (bit 0) is not written by the memory because there is no write delay. The RDSR command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high. An RDSR command cannot immediately follow a READ command. If an RDSR command immediately follows a READ command, the output data will not be correct. Any other sequence of commands is allowed. If an RDSR command is required immediately following a READ command, it is necessary that another command be inserted before the RDSR is executed. Alternatively, two successive RDSR commands can be issued following the READ command. The second RDSR will output the proper state of the Status Register.

**Figure 4 – Read Status Register (RDSR) Timing**




## Write Enable (WREN)

**Figure 5 – Write Enable (WREN) Timing**




The Write Enable (WREN) command sets the Write Enable Latch (WEL) bit in the status register (bit 1). The Write Enable Latch must be set prior to writing either bit in the status register or the memory. The WREN command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high.



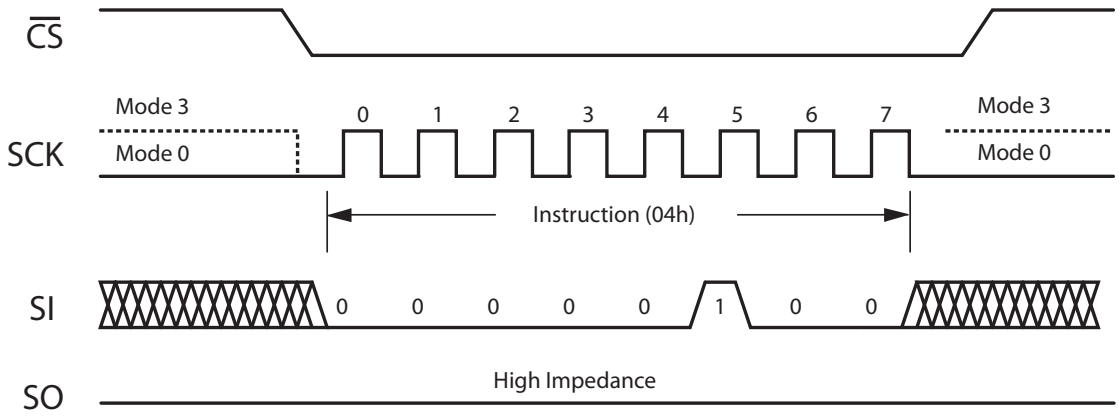
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## Write Disable (WRDI)

The Write Disable (WRDI) command resets the Write Enable Latch (WEL) bit in the status register (bit 1) to 0. This prevents writes to status register or memory. The WRDI command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high.

The Write Enable Latch (WEL) is reset to 0 on power-up or when the WRDI command is completed.

**Figure 6 – Write Disable (WRDI) Timing**

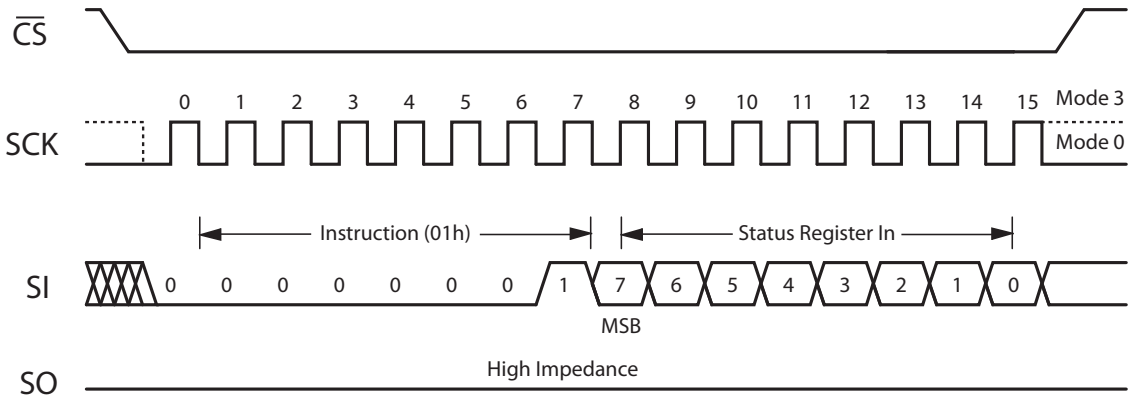



## Write Status Register (WRSR)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. The WRSR command is not executed unless the Write Enable Latch (WEL) has been set to 1 by executing a WREN command while pin $\overline{WP}$ and the Status Register SRWD (Bit 7) correspond to values that make the status register writable as seen in Table 4 on page 8. Status Register bits are non-volatile with the exception of the WEL which is reset to 0 upon power cycling.

The WRSR command is entered by driving $\overline{CS}$ low, sending the command code and status register write data byte, and then driving $\overline{CS}$ high.

**Figure 7 – Write Status Register (WRSR) Timing**





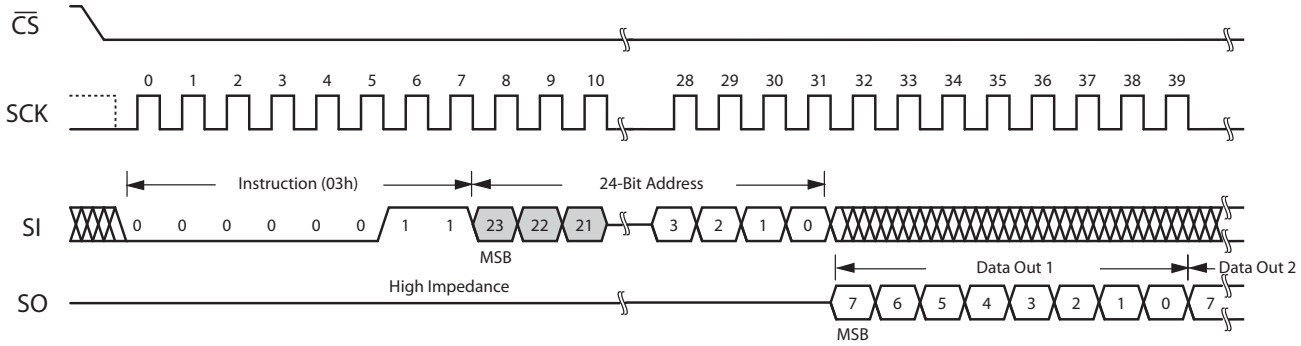

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## Read Data Bytes (READ)

The Read Data Bytes (READ) command allows data bytes to be read starting at an address specified by the 24-bit address. Only address bits 0-18 are decoded by the memory. The data bytes are read out sequentially from memory until the read operation is terminated by bringing $\overline{CS}$ high. The entire memory can be read in a single command. The address counter will roll over to 0000H when the address reaches the top of memory.

The READ command is entered by driving $\overline{CS}$ low and sending the command code. The memory drives the read data bytes on the SO pin. Reads continue as long as the memory is clocked. The command is terminated by bringing $\overline{CS}$ high.

**Figure 8 – Read Data Bytes (READ) Timing**




## Write Data Bytes (WRITE)

The Write Data Bytes (WRITE) command allows data bytes to be written starting at an address specified by the 24-bit address. Only address bits 0-18 are decoded by the memory. The data bytes are written sequentially in memory until the write operation is terminated by bringing $\overline{CS}$ high. The entire memory can be written in a single command. The address counter will roll over to 0000H when the address reaches the top of memory.

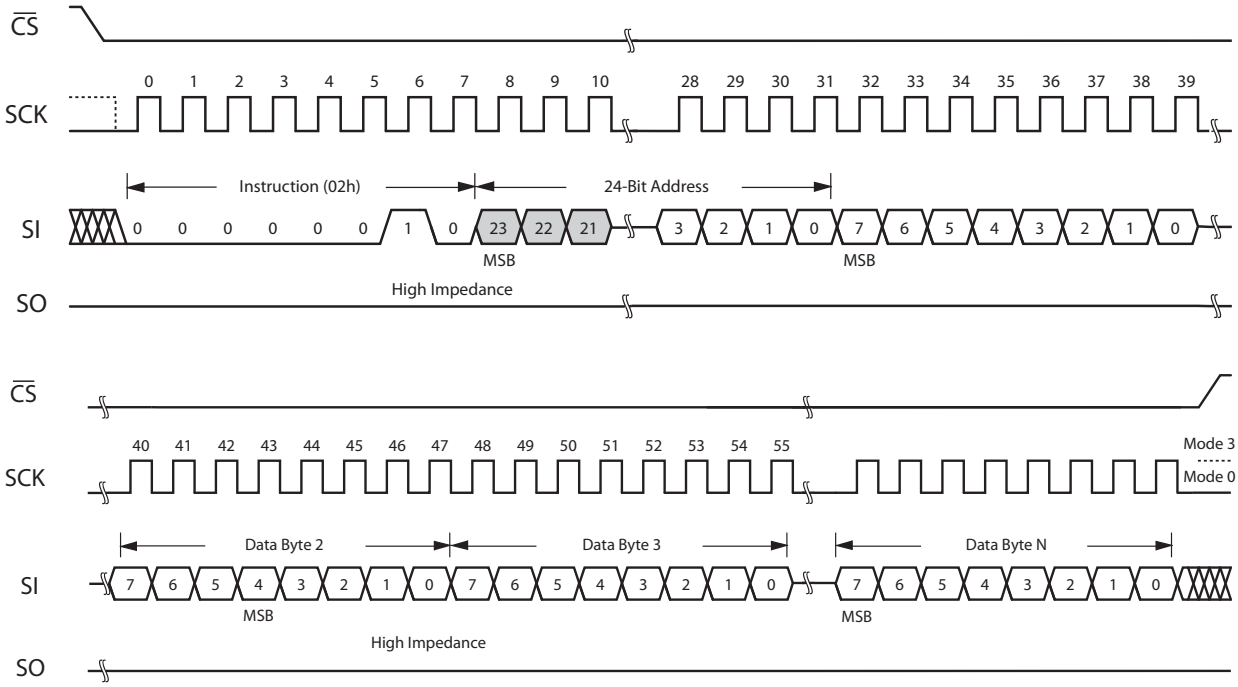
Unlike EEPROM or Flash Memory, MRAM can write data bytes continuously at its maximum rated clock speed without write delays or data polling. Back to back WRITE commands to any random location in memory can be executed without write delay. MRAM is a random access memory rather than a page, sector, or block organized memory so it is ideal for both program and data storage.

The WRITE command is entered by driving $\overline{CS}$ low, sending the command code, and then sequential write data bytes. Writes continue as long as the memory is clocked. The command is terminated by bringing $\overline{CS}$ high.

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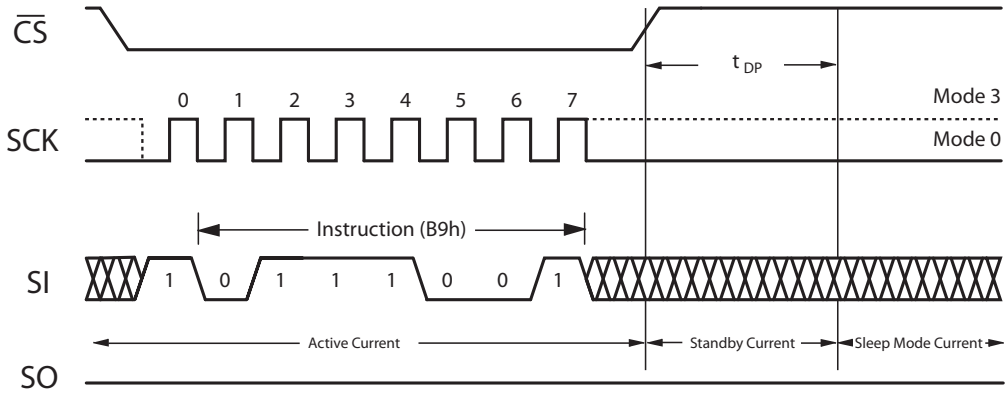
**Figure 9 – Write Data Bytes (WRITE) Timing**




## Enter Sleep Mode (SLEEP)

The Enter Sleep Mode (SLEEP) command turns off all MRAM power regulators in order to reduce the overall chip standby power to 15 µA typical. The SLEEP command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high. The standby current is achieved after time, $^{t}DP$. If power is removed when the part is in sleep mode, upon power restoration, the part enters normal standby. The only valid command following SLEEP mode entry is a WAKE command.

**Figure 10 – Enter Sleep Mode (SLEEP) Timing**



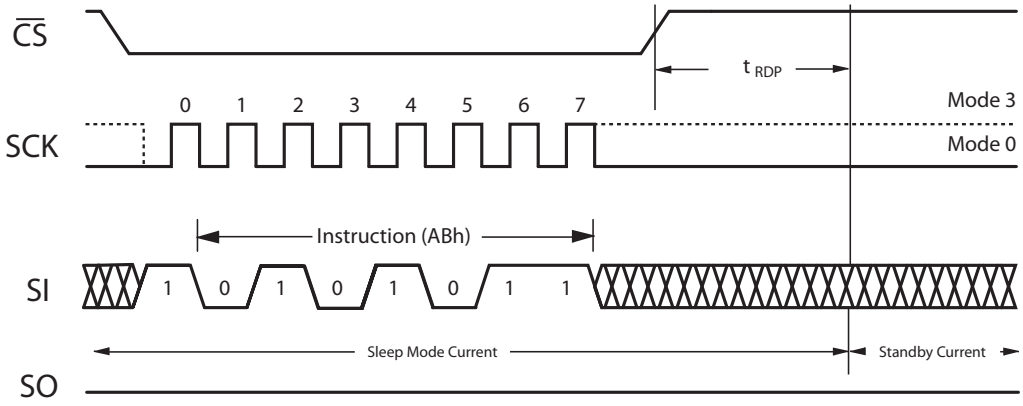



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## Exit Sleep Mode (WAKE)

The Exit Sleep Mode (WAKE) command turns on internal MRAM power regulators to allow normal operation. The WAKE command is entered by driving $\overline{CS}$ low, sending the command code, and then driving $\overline{CS}$ high. The memory returns to standby mode after $^{t}$RDP. The $\overline{CS}$ pin must remain high until the $^{t}$RDP period is over. WAKE must be executed after sleep mode entry and prior to any other command.

**Figure 11 – Exit Sleep Mode (WAKE) Timing**






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# ELECTRICAL SPECIFICATIONS

## Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

### Table 6 – Absolute Maximum Ratings

Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage [2] | | -0.5 to 4.0 | V |
| $V_{IN}$ | Voltage on any pin [2] | | -0.5 to $V_{DD}$ + 0.5 | V |
| $I_{OUT}$ | Output current per pin | | ±20 | mA |
| $P_D$ | Package power dissipation [3] | | 0.600 | W |
| $T_{BIAS}$ | Temperature under bias | Commercial | -10 to 85 | °C |
| | | Industrial | -45 to 95 | °C |
| | | Extended | -45 to 115 | °C |
| | | AEC-Q100 Grade 1 | -45 to 135 | °C |
| $T_{stg}$ | Storage Temperature | | -55 to 150 | °C |
| $T_{Lead}$ | Lead temperature during solder (3 minute max) | | 260 | °C |
| $H_{max_write}$ | Maximum magnetic field during write | Write | 12,000 | A/m |
| $H_{max_read}$ | Maximum magnetic field during read or standby | Read or Standby | 12,000 | A/m |

Notes:

1. All voltages are referenced to $V_{SS}$. The DC value of $V_{IN}$ must not exceed actual applied $V_{DD}$ by more than 0.5V. The AC value of $V_{IN}$ must not exceed applied $V_{DD}$ by more than 2V for 10ns with $I_{IN}$ limited to less than 20mA.
2. Power dissipation capability depends on package characteristics and use environment.

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## Table 7 – Operating Conditions

| Symbol | Parameter | Temp Grade | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | | 3.0 | 3.6 | V |
| $V_{IH}$ | Input high voltage | | 2.2 | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input low voltage | | -0.5 | 0.8 | V |
| $T_A$ | Ambient temperature under bias | Commercial | 0 | 70 | °C |
| | | Industrial | -40 | 85 | °C |
| | | Extended | -40 | 105 | °C |
| | | AEC-Q100 Grade 1 [1] | -40 | 125 | °C |

Notes:

1. AEC-Q100 Grade 1 temperature profile assumes 10 percent duty cycle at maximum temperature (2 years out of 20-year life.)

## Table 8 – DC Characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input leakage current | | - | ±1 | µA |
| $I_{LO}$ | Output leakage current | | - | ±1 | µA |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = +4 mA | - | 0.4 | V |
| | | $I_{OL}$ = +100 µA | - | $V_{SS}$ + 0.2v | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = -4 mA | 2.4 | - | V |
| | | $I_{OH}$ = -100 µA | $V_{DD}$ - 0.2 | - | V |



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## Table 9 – Power Supply Characteristics

| Symbol | Parameter | Conditions | Typical | Max | Unit |
|---|---|---|---|---|---|
| $I_{DDR}$ | Active Read Current | @ 1 MHz | 5.0 | 11 | mA |
| | | @ 40 MHz | 12 | 17 | mA |
| | | @ 50MHz | 13.8 | 18.5 | mA |
| $I_{DDW}$ | Active Write Current | @ 1 MHz | 9.0 | 25 | mA |
| | | @ 40 MHz | 28 | 42 | mA |
| | | @ 50 MHz | 33 | 46.5 | mA |
| $I_{SB1}$ | AC Standby Current (CS High) | @ 40 MHz | 250 | 400 | µA |
| | | @ 50 MHz | 650 | 750 | µA |
| $I_{SB2}$ | CMOS Standby Current (CS High) | | 90 | 180 | µA |
| $I_{ZZ}$ | Standby Sleep Mode Current (CS High) | | 15 | 40 | µA |

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# TIMING SPECIFICATIONS

## Capacitance

### Table 10 – Capacitance

| Symbol | Parameter | Typical | Max | Unit |
|---|---|---|---|---|
| $C_{In}$ | Control input capacitance [1] | - | 6 | pF |
| $C_{I/O}$ | Input/Output capacitance [1] | - | 8 | pF |

Notes:

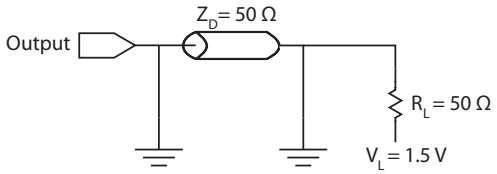
1. $f$ = 1.0 MHz, dV = 3.0 V, $T_A$ = 25 °C, periodically sampled rather than 100% tested.

## AC Measurement Conditions

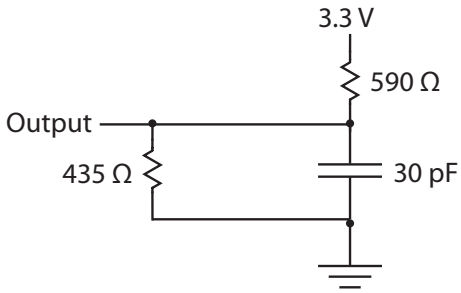
### Table 11 – AC Measurement Conditions

| Parameter | Value | Unit |
|---|---|---|
| Logic input timing measurement reference level | 1.5 | V |
| Logic output timing measurement reference level | 1.5 | V |
| Logic input pulse levels | 0 or 3.0 | V |
| Input rise/fall time | 2 | ns |
| Output load for low and high impedance parameters | See Figure 12 | |
| Output load for all other timing parameters | See Figure 13 | |

### Figure 12 – Output Load for Impedance Parameter Measurements




### Figure 13 – Output Load for all Other Parameter Measurements






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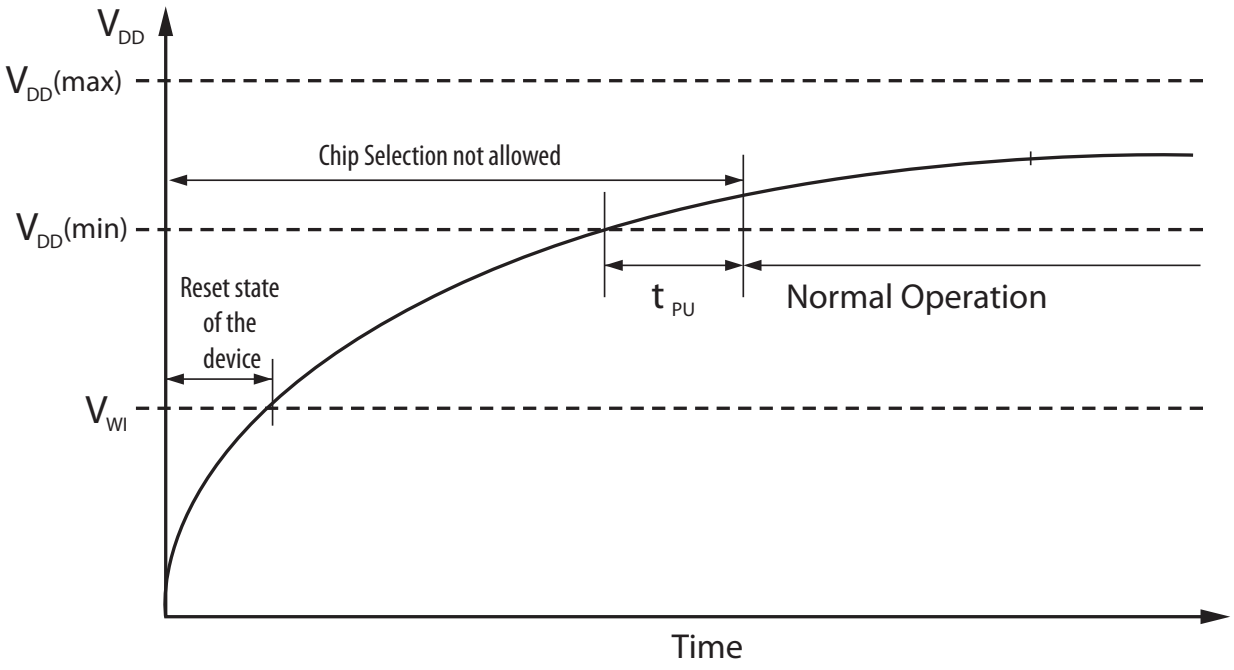
## Power Up Timing

The MR2xH40 is not accessible for a start-up time, $^{t}PU$= 400 µs after power up. Users must wait this time from the time when $V_{DD}$ (min) is reached until the first $\overline{CS}$ low to allow internal voltage references to become stable. The $\overline{CS}$ signal should be pulled up to $V_{DD}$ so that the signal tracks the power supply during power-up sequence.

**Table 12 – Power-Up Timing**

| Symbol | Parameter | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| $V_{WI}$ | Write Inhibit Voltage | 2.2 | - | - | V |
| $^{t}PU$ | Startup Time | 400 | - | - | µs |

**Figure 14 – Power-Up Timing**






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## AC Timing Parameters

### Table 13 – MR20H40 ($^{f}$SCK = 50MHz) AC Timing Parameters

Industrial Temperature Range, $V_{DD}$=3.0 to 3.6 V, $C_L$= 30 pF for all values.

| Symbol | Parameter | Temp Range | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| $^{f}$SCK | SCK Clock Frequency | Industrial | 0 | - | 50 | MHz |
| $^{t}$RI | Input Rise Time | Industrial | - | - | 50 | ns |
| $^{t}$RF | Input Fall Time | Industrial | - | - | 50 | ns |
| $^{t}$WH | SCK High Time | Industrial | 7 | - | - | ns |
| $^{t}$WL | SCK Low Time | Industrial | 7 | - | - | ns |
| **Synchronous Data Timing see Figure 15** | | | | | | |
| $^{t}$CS | CS High Time | Industrial | 40 | - | - | ns |
| $^{t}$CSS | CS Setup Time | Industrial | 5 | - | - | ns |
| $^{t}$CSH | CS Hold Time | Industrial | 5 | - | - | ns |
| $^{t}$SU | Data In Setup Time | Industrial | 2 | - | - | ns |
| $^{t}$H | Data In Hold Time | Industrial | 5 | - | - | ns |
| $^{t}$V | Output Valid | Industrial | 0 | - | 9 | ns |
| $^{t}$HO | Output Hold Time | Industrial | 0 | - | - | ns |
| **HOLD Timing see Figure 16** | | | | | | |
| $^{t}$HD | HOLD Setup Time | Industrial | 5 | - | - | ns |
| $^{t}$CD | HOLD Hold Time | Industrial | 5 | - | - | ns |
| $^{t}$LZ | HOLD to Output Low Impedance | Industrial | - | - | 20 | ns |
| $^{t}$HZ | HOLD to Output High Impedance | Industrial | - | - | 20 | ns |
| **Other Timing Specifications** | | | | | | |
| $^{t}$WPS | WP Setup To CS Low | Industrial | 5 | - | - | ns |
| $^{t}$WPH | WP Hold From CS High | Industrial | 5 | - | - | ns |
| $^{t}$DP | Sleep Mode Entry Time | Industrial | 3 | - | - | µs |
| $^{t}$RDP | Sleep Mode Exit Time | Industrial | 400 | - | - | µs |
| $^{t}$DIS | Output Disable Time | Industrial | 12 | - | - | ns |

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## Table 14 – MR25H40 ($^{f}$SCK = 40MHz) AC Timing Parameters

Commercial Industrial, Extended and AEC-Q100 Grade 1 Temperature Ranges, $V_{DD}$=3.0 to 3.6 V, $C_L$= 30 pF for all values.

| Symbol | Parameter | Temp Grade | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| $^{f}$SCK | SCK Clock Frequency | All | 0 | - | 40 | MHz |
| $^{t}$RI | Input Rise Time | All | - | - | 50 | ns |
| $^{t}$RF | Input Fall Time | All | - | - | 50 | ns |
| $^{t}$WH | SCK High Time | All | 11 | - | - | ns |
| $^{t}$WL | SCK Low Time | All | 11 | - | - | ns |
| **Synchronous Data Timing see Figure 15** | | | | | | |
| $^{t}$CS | CS High Time | All | 40 | - | - | ns |
| $^{t}$CSS | CS Setup Time | All | 10 | - | - | ns |
| $^{t}$CSH | CS Hold Time | All | 10 | - | - | ns |
| $^{t}$SU | Data In Setup Time | All | 5 | - | - | ns |
| $^{t}$H | Data In Hold Time | All | 5 | - | - | ns |
| $^{t}$V | Output Valid | Comm./Ind./Ext. | 0 | - | 9 | ns |
| | | AEC-Q100 Grade 1 | 0 | - | 10 | ns |
| $^{t}$HO | Output Hold Time | All | 0 | - | - | ns |

Table continues next page.

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## Table 14 (Cont'd) - MR25H40 ($^{f}$SCK = 40MHz) AC Timing Parameters

Commercial, Industrial, Extended and AEC-Q100 Grade 1 Temperature Ranges, $V_{DD}$=3.0 to 3.6 V, $C_L$= 30 pF for all values.

| **HOLD Timing see Figure 16** | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Temp Grade** | **Min** | **Typical** | **Max** | **Unit** |
| $^{t}$HD | HOLD Setup Time | All | 10 | - | - | ns |
| $^{t}$CD | HOLD Hold Time | All | 10 | - | - | ns |
| $^{t}$LZ | HOLD to Output Low Impedance | All | - | - | 20 | ns |
| $^{t}$HZ | HOLD to Output High Impedance | All | - | - | 20 | ns |
| **Other Timing Specifications** | | | | | | |
| $^{t}$WPS | WP Setup To CS Low | All | 5 | - | - | ns |
| $^{t}$WPH | WP Hold From CS High | All | 5 | - | - | ns |
| $^{t}$DP | Sleep Mode Entry Time | All | 3 | - | - | µs |
| $^{t}$RDP | Sleep Mode Exit Time | All | 400 | - | - | µs |
| $^{t}$DIS | Output Disable Time | All | 12 | - | - | ns |

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**Figure 15 – Synchronous Data Timing**

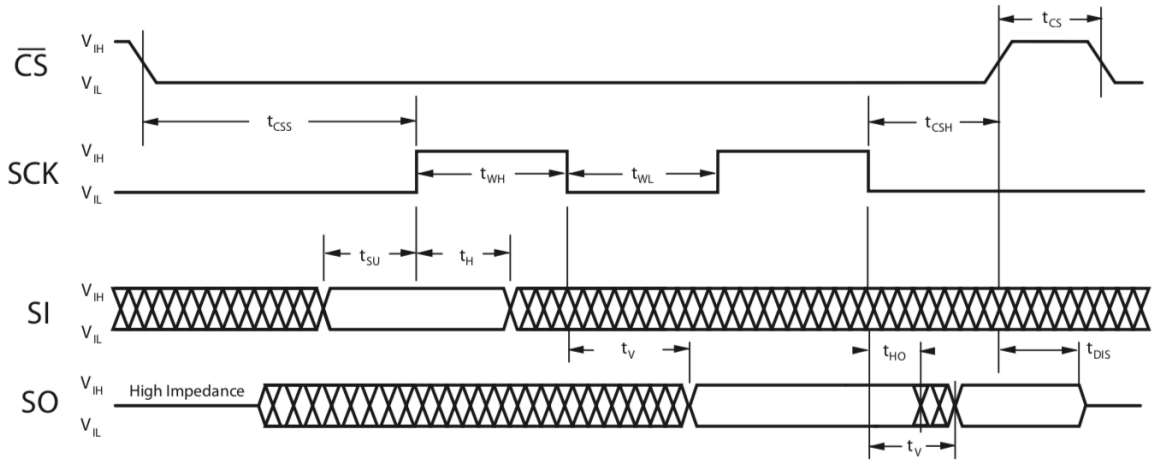
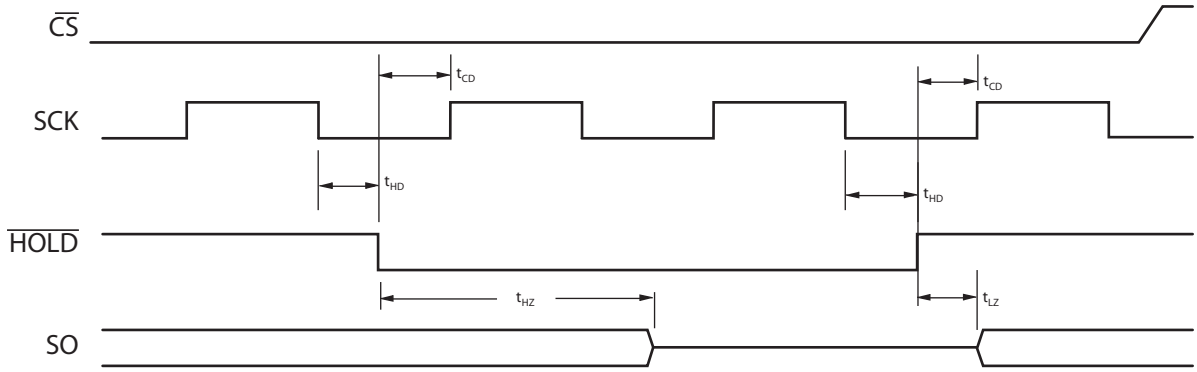



**Figure 16 – HOLD Timing**






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# PART NUMBERS AND ORDERING

## Table 15 – Part Numbering System

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Product Family Number** | | MR | 25H | 40 | | | | |
| | | **Memory** | **Interface** | **Density** | **Revision** | **Temp** | **Package** | **Grade** |
| **Ordering Part Number** | | MR | 25H | 40 | | C | DC | ES |
| MRAM | | MR | | | | | | |
| 50 MHz Serial Family | | 20H | | | | | | |
| 40 MHz Serial Family | | 25H | | | | | | |
| 256 Kb | | 256 | | | | | | |
| 512 Kb | | 512 | | | | | | |
| 1 Mb | | 10 | | | | | | |
| 4 Mb | | 40 | | | | | | |
| No Revision | | Blank | | | | | | |
| Revision A | | A | | | | | | |
| Revision B | | B | | | | | | |
| Commercial | 0 to 70°C | Blank | | | | | | |
| Industrial | -40 to 85°C | C | | | | | | |
| Extended | -40 to 105°C | V | | | | | | |
| AEC Q-100 Grade 1 | -40 to 125°C | M | | | | | | |
| 8-pin DFN in Tray | | DC | | | | | | |
| 8-pin DFN Tape and Reel | | DCR | | | | | | |
| 8-pin DFN (small flag) in Tray | | DF | | | | | | |
| 8-pin DFN (small flag) Tape and Reel | | DFR | | | | | | |
| Engineering Samples | | ES | | | | | | |
| Customer Samples | | Blank | | | | | | |
| Mass Production | | Blank | | | | | | |

Product Family Number and Ordering Part Number given are for illustration only.



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## Table 16 – Ordering Part Numbers

| Speed Grade | Temp Grade | Tempera-ture | Package | Shipping Con-tainer | Order Part Number |
|---|---|---|---|---|---|
| 50MHz | Industrial | -40 to +85 C | 8-DFN Small Flag | Trays | MR20H40CDF |
| | | | | Tape and Reel | MR20H40CDFR |
| 40 MHz | Commercial | 0 to +70 C | 8-DFN Small Flag | Trays | MR25H40DF |
| | | | | Tape and Reel | MR25H40DFR |
| | Industrial | -40 to +85 C | 8-DFN [1] | Trays | MR25H40CDC [1] |
| | | | | Tape and Reel | MR25H40CDCR [1] |
| | | | 8-DFN Small Flag | Trays | MR25H40CDF |
| | | | | Tape and Reel | MR25H40CDFR |
| | Extended | -40 to +105 C | 8-DFN Small Flag | Trays | MR25H40VDF |
| | | | | Tape and Reel | MR25H40VDFR |
| | AEC-Q100 Grade 1 | -40 to +125 C | 8-DFN Small Flag | Trays | MR25H40MDF |
| | | | | Tape and Reel | MR25H40MDFR |

Note:

1. The DC pckage option (8-DFN) is not recommended for new designs. Please select the DF (8-DFN small flag) option for new designs.

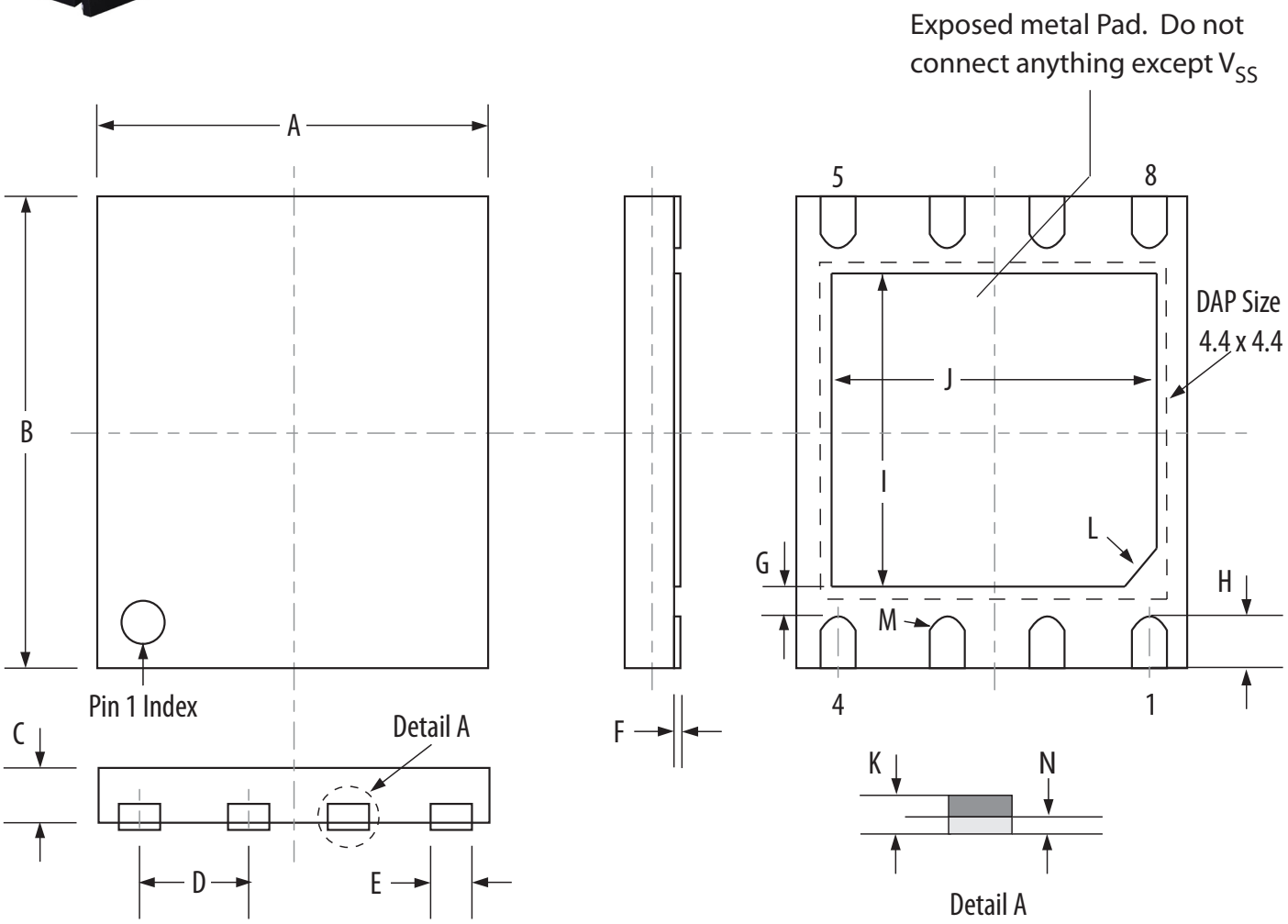
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## PACKAGE OUTLINE DRAWINGS



### Figure 17 – DFN Package Outline




| Dimension | A | B | C | D | E | F | G | H | I | J | K | L | M | N |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Max. | 5.10 | 6.10 | 1.00 | 1.27 | 0.45 | 0.05 | 0.35 | 0.70 | 4.20 | 4.20 | 0.261 | C0.35 | R0.20 | 0.05 |
| Min. | 4.90 | 5.90 | 0.90 | BSC | 0.35 | 0.00 | Ref. | 0.50 | 4.00 | 4.00 | 0.195 | | | 0.00 |

Notes:

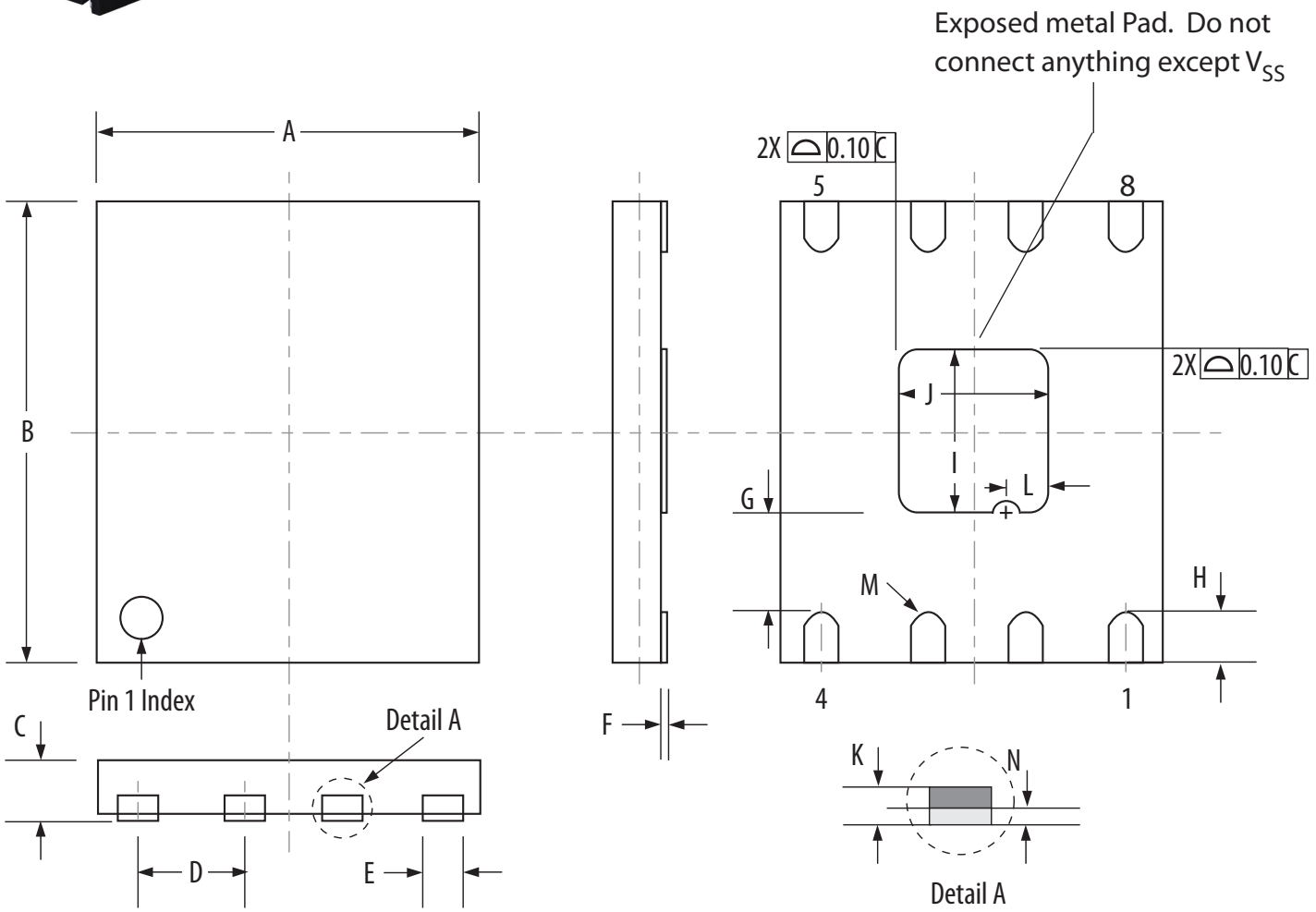
1. Reference JEDEC MO-229.
2. All dimensions are in mm. Angles in degrees.
3. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall be within 0.08 mm.
4. Warpage shall not exceed 0.10 mm.

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## Figure 18 – DFN Small Flag Package




| Dimension | A | B | C | D | E | F | G | H | I | J | K | L | M | N |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Max. | 5.10 | 6.10 | 0.90 | 1.27 BSC | 0.45 | 0.05 | 1.60 | 0.70 | 2.10 | 2.10 | .210 | C0.45 | R0.20 | 0.05 |
| Min. | 4.90 | 5.90 | 0.80 | | 0.35 | 0.00 | 1.20 | 0.50 | 1.90 | 1.90 | .196 | | | 0.00 |

Notes:

1. Reference JEDEC MO-229.
2. All dimensions are in mm. Angles in degrees.
3. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall be within 0.08 mm.
4. Warpage shall not exceed 0.10 mm.

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## REVISION HISTORY

| Revision | Date | Description of Change |
|---|---|---|
| 0 | Jan 15, 2010 | Product Concept Release |
| 0 .1 | Feb. 23, 2010 | Fixed typos in text. |
| 1 | May 5, 2010 | Removed commercial specifications. All parts meet industrial specifications. |
| 2 | Jan 11, 2011 | Preliminary Product Release. Updated description of status register non-volatility, WAKE command, Table 3.4. |
| 3 | Apr 25, 2011 | Removed DIP package part to seperate datasheet. Added inset detail for mechanical package drawings. |
| 4 | September 22, 2011 | Added AEC-Q100 Grade 1 ordering option. Revised Table 3.1, Table 3.2, Table 3.4, Table 4.4 revised and Note 2 deleted, revised Figure 5.1 and Table 5.1. |
| 5 | Nov 18, 2011 | Corrected $V_{OL}$ in Table 3.3 to read $V_{OL}$ Max = $V_{SS}$ + 0.2v. Corrected SI waveform in Figure 2.8. New Small Flag DFN package option added to Page 1 Features and available parts Table 5.1. DFN Small Flag drawing and dimensions table added as Figure 6.2. Figure 6.1, DFN Package, cleaned up with better quality drawing and dimension table. No specifications were changed in Figure 6.1. |
| 6 | August 23, 2012 | CDF and CDFR options changed to Preliminary. Added Small Flag DFN illustrations. Reformatted all parametric tables. Revised 8-DFN package drawing to show correct proportion for flag and package. Added MR20H40 as 50MHz speed option. Deleted large flag DFN ordering option for AEC-Q100 products. Corrected errors in DFN package outline drawings. |
| 7 | January 17, 2013 | Removed Preliminary status from MR25H40CDF, CDFR. |
| 8 | May 24, 2013 | Removed Preliminary status from MR20H40CDF(R), and from MR20H40DF(R). |
| 9 | March 28, 2014 | Removed Preliminary status from 25H40MDF(R). $V_{WI}$ max to unspecified from TBD. Added MSL-3 status to the Features list. |
| 10 | July 11, 2014 | MR20H40DF and MR20H40DFR withdrawn from sales status. |
| 11 | August 13, 2014 | Added Extended temperature grade offering. |
| 11.1 | May 19, 2015 | Revised Everspin contact information. |
| 11.2 | June 11, 2015 | Corrected Japan Sales Office telephone number. |
| 12.0 | December 9, 2015 | Clarification of RDSR command operation. |
| 12.1 | December 18, 2015 | Minor edits to the revised RDSR command operation. Corrected wrong bit number for the WEL in the WRDI command description. Clarification of SRWD bit location in the Status Register within the WRSR command description. Condensed Note 1 in Table 2, referring to RDSR operation after a READ command. |

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## REVISION HISTORY - Cont'd

| Revision | Date | Description of Change |
|---|---|---|
| 12.2 | December 13, 2016 | Change all large flag DFN options to "The DC pckage option (8-DFN) is not recommended for new designs. Please select the DF (8-DFN small flag) option for new designs." |
| 12.3 | February 2, 2017 | Added $^{t}$HO and $^{t}$V relationship to Synchronous Data Timing |
| 12.4 | March 23, 2018 | Updated the Contact Us table |
| 12.5 | December 16, 2019 | Corrected sentence in Block Protection Modes section on page 9 to "The memory enters hardware block protection when the WP input is low and the Status Register Write Disable (SRWD) bit is set to 1". |
| 12.6 | August 7, 2020 | Added a Commercial temperature range product option to MR25H40 family. |

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