DDR SDRAM

4M x 16 Bit x 4 Banks Double Data Rate SDRAM

Features

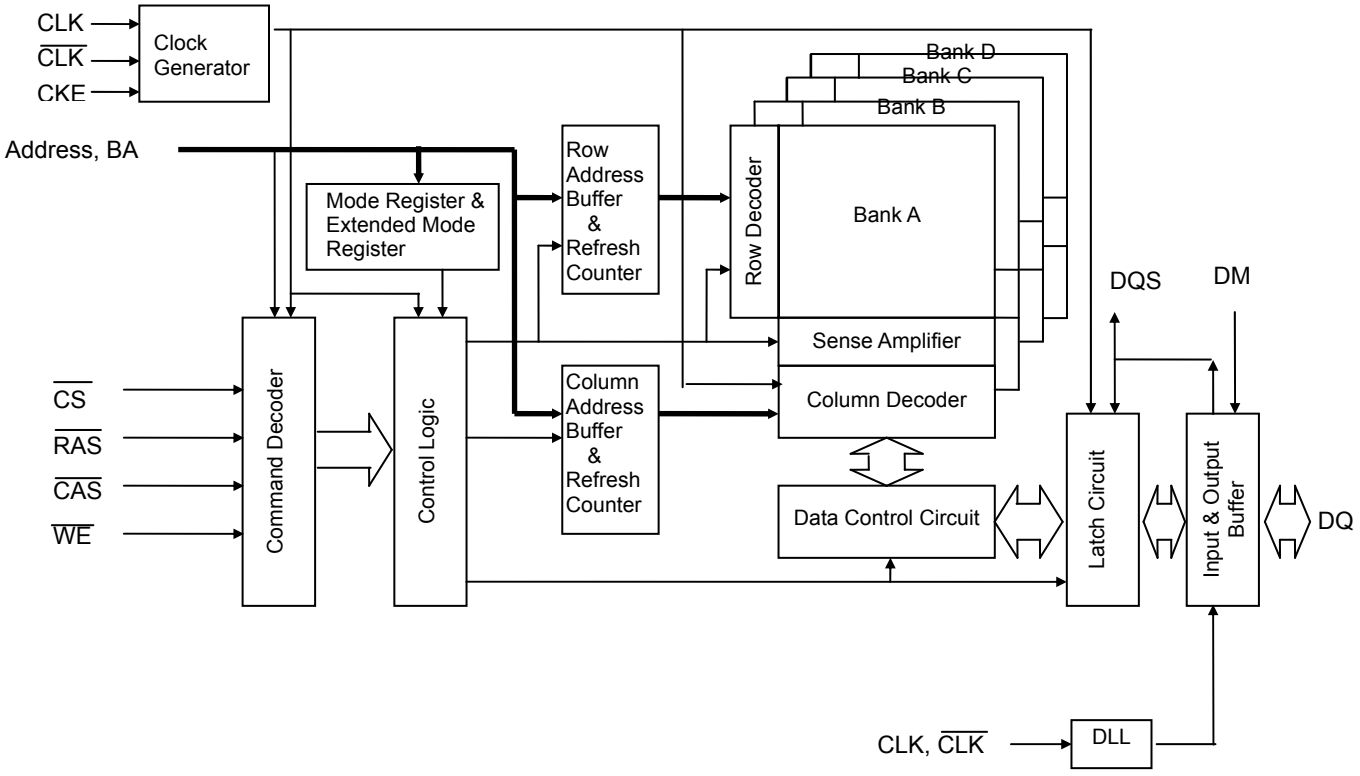
- Double-data-rate architecture, two data transfers per clock cycle
- Bi-directional data strobe (DQS)
- Differential clock inputs (CLK and $\overline{CLK}$)
- DLL aligns DQ and DQS transition with CLK transition
- Four bank operation
- CAS Latency : 2.5, 3, 4
- Burst Type : Sequential and Interleave
- Burst Length : 2, 4, 8
- All inputs except data & DM are sampled at the rising edge of the system clock (CLK)
- Data I/O transitions on both edges of data strobe (DQS)
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Data mask (DM) for write masking only
- V_{DD} = 2.5V ± 0.2V, V_{DDQ} = 2.5V ± 0.2V
- 7.8us refresh interval
- Auto & Self refresh
- 2.5V I/O (SSTL_2 compatible)

Ordering Information

Product ID	Max Freq.	V_{DD}	Package	Comments
M13S2561616A -5TG2S	200MHz (DDR400)	2.5V	66 pin TSOPII	Pb-free
M13S2561616A -6TG2S	166MHz (DDR333)			
M13S2561616A -5BG2S	200MHz (DDR400)		60 Ball BGA	
M13S2561616A -6BG2S	166MHz (DDR333)			

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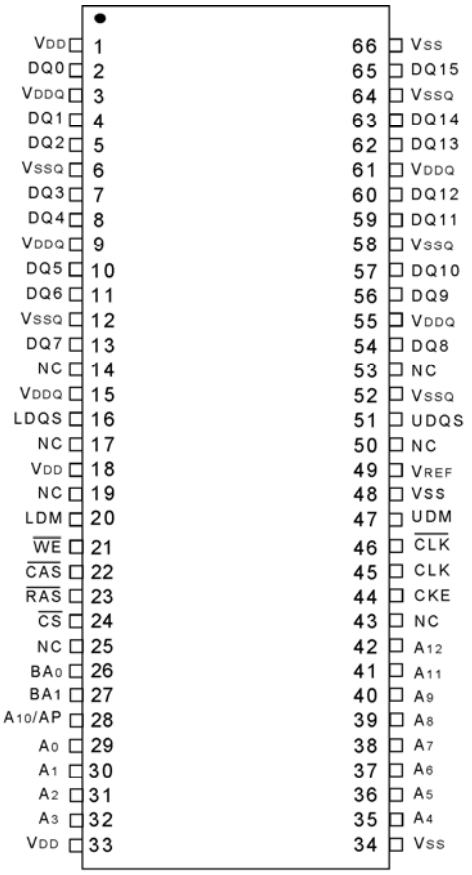
Functional Block Diagram



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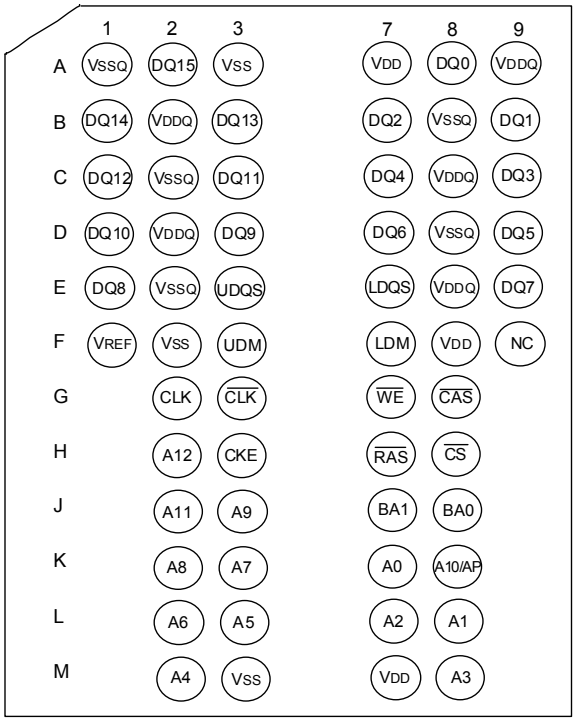
PIN CONFIGURATION (TOP VIEW)

(TSOPII 66L, 400milX875mil Body, 0.65mm Pin Pitch)



BALL CONFIGURATION (TOP VIEW)

(BGA60, 8mmX13mmX1.0mm Body, 0.8mm Ball Pitch)



Pin Description

Pin Name	Function	Pin Name	Function
A0~A12, BA0, BA1	Address inputs - Row address A0~A12 - Column address A0~A8 A10/AP: AUTO Precharge BA0, BA1: Bank selects (4 Banks)	LDM, UDM	DM is an input mask signal for write data. LDM corresponds to the data on DQ0~DQ7; UDM correspond to the data on DQ8~DQ15.
DQ0~DQ15	Data-in/Data-out	CLK, $\overline{CLK}$	Clock input
$\overline{RAS}$	Row address strobe	CKE	Clock enable
$\overline{CAS}$	Column address strobe	$\overline{CS}$	Chip select
$\overline{WE}$	Write enable	V_{DDQ}	Supply Voltage for DQ
V_{SS}	Ground	V_{SSQ}	Ground for DQ
V_{DD}	Power	V_{REF}	Reference Voltage for SSTL_2
LDQS, UDQS	Bi-directional Data Strobe. LDQS corresponds to the data on DQ0~DQ7; UDQS correspond to the data on DQ8~DQ15.	NC	No connection

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Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Voltage on V_{DD} & V_{DDQ} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 3.6	V
Voltage on inputs relative to V_{SS}	V_{INPUT}	-1.0 ~ 3.6	V
Voltage on I/O pins relative to V_{SS}	V_{IO}	-0.5 ~ V_{DDQ}+0.5	V
Operating ambient temperature	T_A	0 ~ +70	°C
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommend operation condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operation Conditions & Specifications

DC Operation Conditions

Recommended operating conditions (Voltage reference to V_{SS} = 0V)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{DD}	2.3	2.7	V	
I/O Supply voltage	V_{DDQ}	2.3	2.7	V	
I/O Reference voltage	V_{REF}	0.49*V_{DDQ}	0.51*V_{DDQ}	V	1
I/O Termination voltage (system)	V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V	2
Input logic high voltage	V_{IH} (DC)	V_{REF} + 0.15	V_{DDQ} + 0.3	V	
Input logic low voltage	V_{IL} (DC)	-0.3	V_{REF} - 0.15	V	
Input Voltage Level, CLK and $\overline{CLK}$ inputs	V_{IN} (DC)	-0.3	V_{DDQ} + 0.3	V	
Input Differential Voltage, CLK and $\overline{CLK}$ inputs	V_{ID} (DC)	0.36	V_{DDQ} + 0.6	V	3
V–I Matching: Pullup to Pulldown Current Ratio	VI (Ratio)	0.71	1.4	-	4
Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not tested under = 0V)	I_L	-2	2	μA	
Output leakage current (DQs are disable; 0V ≤ V_{OUT} ≤ V_{DDQ})	I_{OZ}	-5	5	μA	

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DC Operation Conditions - continued

Parameter	Symbol	Min	Max	Unit	Note
Output High Current (Full strength driver – Normal) (V_{OUT} =V_{DDQ}-0.373V, min V_{REF}, min V_{TT})	I_{OH}	-15		mA	5, 7
Output Low Current (Full strength driver – Normal) (V_{OUT} = 0.373V, max V_{REF}, max V_{TT})	I_{OL}	+15		mA	5, 7
Output High Current (Reduced strength driver –Weak) (V_{OUT} = V_{DDQ}-0.763V, min V_{REF}, min V_{TT})	I_{OH}	-9		mA	6
Output Low Current (Reduced strength driver – Weak) (V_{OUT} = 0.763V, max V_{REF}, max V_{TT})	I_{OL}	+9		mA	6
Output High Current (Reduced strength driver – Matched impedance) (V_{OUT} = V_{DDQ}-1.056V, min V_{REF}, min V_{TT})	I_{OH}	-4.5		mA	6
Output Low Current (Reduced strength driver – Matched impedance) (V_{OUT} = 1.056V, max V_{REF}, max V_{TT})	I_{OL}	+4.5		mA	6

Notes:

1. V_{REF} is expected to be equal to 0.5* V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
2. V_{TT} is not applied directly to the device. V_{TT} is system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
3. V_{ID} is the magnitude of the difference between the input level on CLK and the input level on $\overline{CLK}$.
4. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25 V to 1.0 V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7 for device drain to source voltages from 0.1 to 1.0.
5. V_{OH} = 1.95V, V_{OL} =0.35V.
6. V_{OH} = 1.9V, V_{OL} =0.4V.
7. The values of I_{OH}(DC) is based on V_{DDQ} = 2.3V and V_{TT} = 1.19V.
   The values of I_{OL}(DC) is based on V_{DDQ} = 2.3V and V_{TT} = 1.11V.

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IDD Parameters and Test Conditions

Test Condition	Symbol	Note
Operating Current (one bank Active - Precharge): t_{RC} = t_{RC} (min); t_{CK} = t_{CK} (min); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles; $\overline{CS}$ = high between valid commands.	IDD0	
Operating Current (one bank Active - Read - Precharge): One bank open; BL = 4; t_{RC} = t_{RC} (min); t_{CK} = t_{CK} (min); I_{OUT} = 0mA; Address and control inputs changing once per deselect cycle; $\overline{CS}$ = high between valid commands	IDD1	2
Precharge Power-down Standby Current: All banks idle; Power-down mode; t_{CK} = t_{CK} (min); CKE ≤ V_{IL}(max); V_{IN} = V_{REF} for DQ, DQS and DM.	IDD2P	
Precharge Floating Standby Current: $\overline{CS}$ ≥ V_{IH}(min); All banks idle; CKE ≥ V_{IH}(min); t_{CK} = t_{CK} (min); Address and other control inputs changing once per clock cycle; V_{IN} = V_{REF} for DQ, DQS, and DM.	IDD2F	
Precharge Quiet Standby Current: $\overline{CS}$ ≥ V_{IH}(min); All banks idle; CKE ≥ V_{IH}(min); t_{CK} = t_{CK} (min); Address and other control inputs stable at ≥ V_{IH}(min) or ≤ V_{IL}(max); V_{IN} = V_{REF} for DQ, DQS, and DM.	IDD2Q	
Active Power-down Standby Current: One bank active; Power-down mode; CKE ≤ V_{IL}(max); t_{CK} = t_{CK} (min); V_{IN} = V_{REF} for DQ, DQS, and DM.	IDD3P	
Active Standby Current: $\overline{CS}$ ≥ V_{IH}(min); CKE ≥ V_{IH}(min); One bank active; t_{RC} = t_{RAS} (max); t_{CK} = t_{CK} (min); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	IDD3N	
Operating Current (burst read): BL = 2; Continuous burst reads; One bank active; Address and control inputs changing once per clock cycle; t_{CK} = t_{CK} (min); I_{OUT} = 0mA; 50% of data changing on every transfer.	IDD4R	
Operating Current (burst write): BL = 2; Continuous burst writes; One bank active; Address and control inputs changing once per clock cycle; t_{CK} = t_{CK} (min); DQ, DM, and DQS inputs changing twice per clock cycle; 50% of input data changing at every transfer.	IDD4W	
Auto Refresh Current: t_{RC} = t_{RFC}(min)	IDD5	
Self Refresh Current: CKE ≤ 0.2V; external clock on; t_{CK} = t_{CK} (min)	IDD6	1
Operating Current (Four bank operation): Four-bank interleaving READs (burst = 4) with auto precharge; t_{RC} = t_{RC} (min); t_{CK} = t_{CK} (min); Address and control inputs change only during ACTIVE, READ, or WRITE commands; I_{OUT} = 0mA.	IDD7	2

Notes:

1. Enable on-chip refresh and address counters.
2. Random address is changing; 50% of data is changing at every transfer.

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IDD Specifications

Symbol	Version		Unit
	-5	-6	
IDD0	80	70	mA
IDD1	110	100	mA
IDD2P	4	4	mA
IDD2F	30	30	mA
IDD2Q	30	30	mA
IDD3P	25	20	mA
IDD3N	55	50	mA
IDD4R	130	120	mA
IDD4W	130	120	mA
IDD5	140	130	mA
IDD6	3	3	mA
IDD7	220	210	mA

Input / Output Capacitance

Parameter	Package	Symbol	Min	Max	Delta Cap (max)	Unit	Note
Input capacitance (A0~A12, BA0~BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	TSOP	C_{IN1}	2	5	0.5	pF	1,4
	BGA		TBD	TBD		pF	
Input capacitance (CLK, $\overline{CLK}$)	TSOP	C_{IN2}	2	4	0.25	pF	1,4
	BGA		TBD	TBD		pF	
Data & DQS input/output capacitance	TSOP	C_{OUT}	1	4	0.5	pF	1,2,3,4
	BGA		TBD	TBD		pF	
Input capacitance (DM)	TSOP	C_{IN3}	1	4	0.5	pF	1,2,3,4
	BGA		TBD	TBD		pF	

Notes:

1. These values are guaranteed by design and are tested on a sample basis only.
2. Although DM is an input -only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match signal propagation times of DQ, DQS, and DM in the system.
3. Unused pins are tied to ground.
4. This parameter is sampled. V_{DDQ} = 2.5V ± 0.2V, V_{DD} = 2.5V ± 0.2V. f=100MHz, T_A =25°C, V_{OUT}(DC) = V_{DDQ}/2, V_{OUT} (peak to peak) = 0.2V. DM inputs are grouped with I/O pins - reflecting the fact that they are matched in loading (to facilitate trace matching at the board level).

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AC Operation Conditions & Timing Specifications

AC Operation Conditions

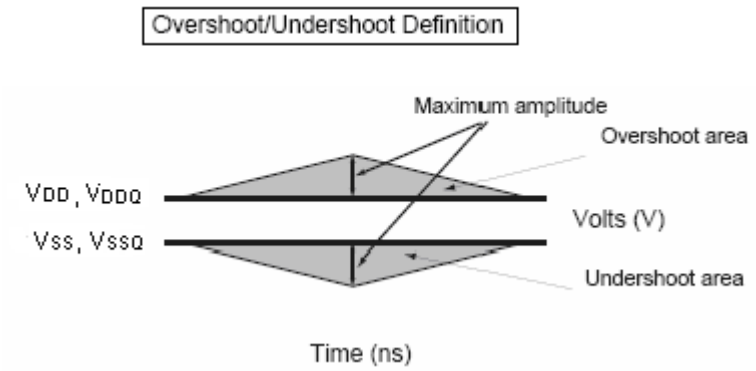
Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	V_{IH}(AC)	V_{REF} + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	V_{IL}(AC)		V_{REF} - 0.31	V	
Input Differential Voltage, CLK and $\overline{CLK}$ inputs	V_{ID}(AC)	0.7	V_{DDQ}+0.6	V	1
Input Crossing Point Voltage, CLK and $\overline{CLK}$ inputs	V_{IX}(AC)	0.5*V_{DDQ}-0.2	0.5*V_{DDQ}+0.2	V	2

Notes:

1. V_{ID} is the magnitude of the difference between the input level on CLK and the input on $\overline{CLK}$.
2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

AC Overshoot / Undershoot Specification

Parameter	Pin	Value	Unit
		-5 / -6	
Maximum peak amplitude allowed for overshoot	Address, Control	1.5	V
	Data, Strobe, Mask	1.2	V
Maximum peak amplitude allowed for undershoot	Address, Control	1.5	V
	Data, Strobe, Mask	1.2	V
Maximum overshoot area above V_{DD}	Address, Control	4.5	V-ns
	Data, Strobe, Mask	2.4	V-ns
Maximum undershoot area below V_{SS}	Address, Control	4.5	V-ns
	Data, Strobe, Mask	2.4	V-ns



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AC Timing Parameter & Specifications (Note: 1~6, 9~10)

Parameter		Symbol	-5		-6		Unit	Note
			min	max	min	max		
Clock period	CL2.5	t_{CK}	5	12	6	12	ns	
	CL3		5	12	6	12		
	CL4		5	12	6	12		
DQ output access time from CLK/ $\overline{CLK}$		t_{AC}	-0.7	+0.7	-0.7	+0.7	ns	
CLK high-level width		t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	
CLK low-level width		t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	
DQS output access time from CLK/ $\overline{CLK}$		t_{DQSCK}	-0.6	+0.6	-0.6	+0.6	ns	
Clock to first rising edge of DQS delay		t_{DQSS}	0.72	1.25	0.72	1.25	t_{CK}	
DQ and DM input setup time (to DQS)		t_{DS}	0.4		0.4		ns	
DQ and DM input hold time (to DQS)		t_{DH}	0.4		0.4		ns	
DQ and DM input pulse width (for each input)		t_{DIPW}	1.75		1.75		ns	18
Address and Control input setup time (fast)		t_{IS}	0.6		0.6		ns	15, 17~19
Address and Control input hold time (fast)		t_{IH}	0.6		0.6		ns	15, 17~19
Address and Control input setup time (slow)		t_{IS}	0.8		0.8		ns	16~19
Address and Control input hold time (slow)		t_{IH}	0.8		0.8		ns	16~19
Control and Address input pulse width (for each input)		t_{IPW}	2.2		2.2		ns	18
DQS input high pulse width		t_{DQSH}	0.35		0.35		t_{CK}	
DQS input low pulse width		t_{DQSL}	0.35		0.35		t_{CK}	
DQS falling edge to CLK setup time		t_{DSS}	0.2		0.2		t_{CK}	
DQS falling edge hold time from CLK		t_{DSH}	0.2		0.2		t_{CK}	
Data strobe edge to output data edge		t_{DQSQ}		0.4		0.4	ns	22
Data-out high-impedance time from CLK/ $\overline{CLK}$		t_{HZ}		+0.7		+0.7	ns	11
Data-out low-impedance time from CLK/ $\overline{CLK}$		t_{LZ}	-0.7	+0.7	-0.7	+0.7	ns	11
Clock half period		t_{HP}	t_{CL}min or t_{CH}min		t_{CL}min or t_{CH}min		ns	20,21
DQ/DQS output hold time from DQS		t_{QH}	t_{HP}- t_{QHS}		t_{HP}- t_{QHS}		ns	21
Data hold skew factor		t_{QHS}		0.5		0.5	ns	

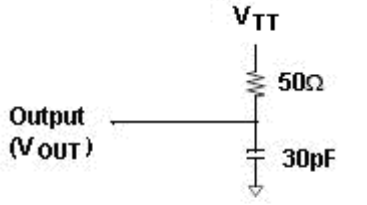
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AC Timing Parameter & Specifications – continued

Parameter	Symbol	-5		-6		Unit	Note
		min	max	min	max		
Active to Precharge command	t_{RAS}	40	70K	42	70K	ns	
Active to Active / Auto Refresh command period	t_{RC}	55		60		ns	
Auto Refresh to Active / Auto Refresh command period	t_{RFC}	70		72		ns	
Active to Read, Write delay	t_{RCD}	15		18		ns	
Precharge command period	t_{RP}	15		18		ns	
Active to Read with Auto Precharge command	t_{RAP}	15		18		ns	
Active bank A to Active bank B command	t_{RRD}	10		12		ns	
Write recovery time	t_{WR}	15		15		ns	
Write data in to Read command delay	t_{WTR}	2		2		t_{CK}	
Average periodic refresh interval	t_{REFI}		7.8		7.8	us	14
Write preamble	t_{WPRE}	0.25		0.25		t_{CK}	
Write postamble	t_{WPST}	0.4	0.6	0.4	0.6	t_{CK}	12
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	
Read postamble	t_{RPST}	0.4	0.6	0.4	0.6	t_{CK}	
Clock to DQS write preamble setup time	t_{WPRES}	0		0		ns	13
Mode Register Set command cycle time	t_{MRD}	2		2		t_{CK}	
Exit self refresh to Read command	t_{XSRD}	200		200		t_{CK}	
Exit self refresh to non-Read command	t_{XSNR}	75		75		ns	
Auto Precharge write recovery+precharge time	t_{DAL}	(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		t_{CK}	23

Notes:

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, IDD, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. The below figure represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).



Time Reference Load

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4. AC timing and IDD tests may use a V_{IL} to V_{IH} swing of up to 1.5 V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CLK/ $\overline{CLK}$), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1 V/ns in the range between V_{IL}(AC) and V_{IH}(AC).
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.
6. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE ≤ $0.2V_{DDQ}$ is recognized as LOW.
7. Enables on-chip refresh and address counters.
8. IDD specifications are tested after the device is properly initialized.
9. The CLK/ $\overline{CLK}$ input reference level (for timing referenced to CLK/ $\overline{CLK}$) is the point at which CLK and $\overline{CLK}$ cross; the input reference level for signals other than CLK/ $\overline{CLK}$, is V_{REF}.
10. The output timing reference voltage level is V_{TT}.
11. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (t_{HZ}), or begins driving (t_{LZ}).
12. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
13. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CLK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High- Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
14. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
15. For command/address input slew rate ≥ 1.0 V/ns
16. For command/address input slew rate ≥ 0.5 V/ns and < 1.0 V/ns
17. For CLK & $\overline{CLK}$ slew rate ≥ 1.0 V/ns
18. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
19. Slew Rate is measured between V_{OH}(AC) and V_{OL}(AC).
20. Min (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).....For example, t_{CL} and t_{CH} are = 50% of the period, less the half period jitter (t_{JIT}(HP)) of the clock source, and less the half period jitter due to crosstalk (t_{JIT}(crosstalk)) into the clock traces.
21. $t_{QH} = t_{HP} - t_{QHS}$, where:
t_{HP} = minimum half clock period for any given cycle and is defined by clock high or clock low (t_{CH}, t_{CL}). t_{QHS} accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
22. t_{DQSQ} Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
23. For each of the terms above, if not already an integer, round to the next highest integer.

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Command Truth Table

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DM	BA0, BA1	A10/AP	A12~A11, A9~A0	Note
Register	Extended MRS		H	X	L	L	L	L	X	OP CODE			1,2
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	V	L	Column Address (A0~A8)	4,8
	Auto Precharge Enable										H		4,6,8
Burst Terminate			H	X	L	H	H	L	X	X			7
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		5
Active Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	H	H	H					
Deselect (NOP)			H	X	H	X	X	X	X	X			
No Operation (NOP)					L	H	H	H					

(V = Valid, X = Don't Care, H = Logic High, L = Logic Low)

Notes:

1. OP Code: Operand Code. A0~A12 & BA0~BA1: Program keys. (@EMRS/MRS)
2. EMRS/MRS can be issued only at all banks precharge state.
   A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA0~BA1: Bank select addresses.
   If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after end of burst.
7. Burst Terminate command is valid at every burst length.
8. DM and Data-in are sampled at the rising and falling edges of the DQS. Data-in byte are masked if the corresponding and coincident DM is "High". (Write DM latency is 0).

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Basic Functionality

Power-Up and Initialization Sequence

DDR SDRAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. No power sequencing is specified during power up and power down given the following criteria:

- V_{DD} and V_{DDQ} are driven from a single power converter output, AND
- V_{TT} is limited to 1.35 V, AND
- V_{REF} tracks V_{DDQ} /2

OR, the following relationships must be followed:

- V_{DDQ} is driven after or with V_{DD} such that $V_{DDQ} < V_{DD} + 0.3$ V, AND
- V_{TT} is driven after or with V_{DDQ} such that $V_{TT} < V_{DDQ} + 0.3$ V, AND
- V_{REF} is driven after or with V_{DDQ} such that $V_{REF} < V_{DDQ} + 0.3$ V.

At least one of these two conditions must be met.

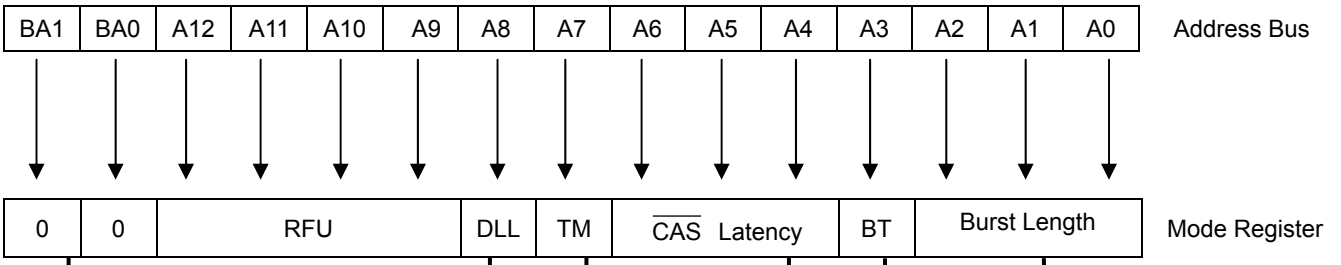
Except for CKE, inputs are not recognized as valid until after V_{REF} is applied. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after V_{DD} is applied. Maintaining an LVCMOS LOW level on CKE during power-up is required to guarantee that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access).
After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200 µs delay prior to applying an executable command. Once the 200 µs delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH.
Following the NOP command, a PRECHARGE ALL command should be applied. Next a MODE REGISTER SET command should be issued for the Extended Mode Register, to enable the DLL, and then a MODE REGISTER SET command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any executable command. A PRECHARGE ALL command should be applied, placing the device in the ”all banks idle” state.
Once in the idle state, two AUTO refresh cycles must be performed. Additionally, a MODE REGISTER SET command for the Mode Register, with the reset DLL bit deactivated (i.e., to program operating parameters without resetting the DLL) must be performed.
Following these cycles, the DDR SDRAM is ready for normal operation.

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Mode Register Definition

Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs $\overline{CAS}$ latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for variety of different applications. The default value of the register is not defined, therefore the mode register must be written after EMRS setting for proper DDR SDRAM operation. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and BA0~BA1 (The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register). The state of address pins A0~A12 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and BA0~BA1 going low is written in the mode register. Two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0~A2, addressing mode uses A3, $\overline{CAS}$ latency (read latency from column address) uses A4~A6. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and $\overline{CAS}$ latencies.



A8	DLL Reset
0	No
1	Yes

A7	Mode
0	Normal
1	Test

A3	Burst Type
0	Sequential
1	Interleave

BA1	BA0	Operating Mode
0	0	MRS Cycle
0	1	EMRS Cycle

$\overline{CAS}$ Latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	4
1	1	0	2.5
1	1	1	Reserved

Burst Length

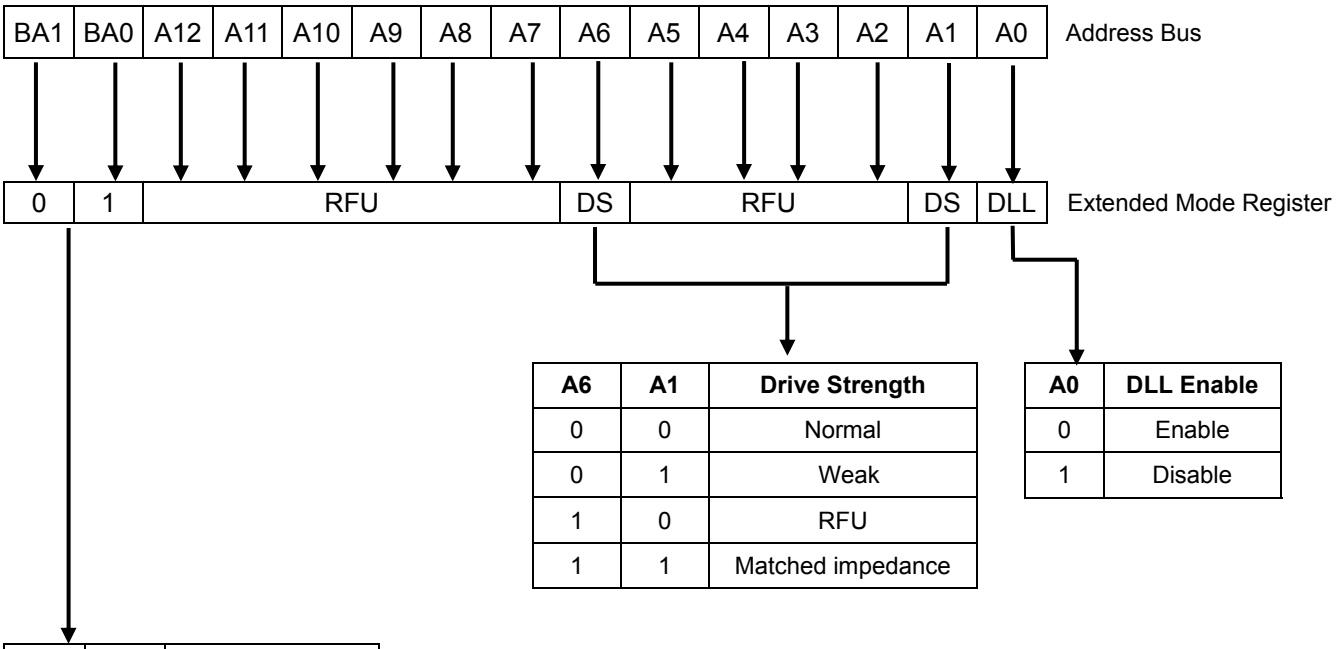
A2	A1	A0	Length	
			Sequential	Interleave
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

Note: RFU (Reserved for future use) must stay “0” during MRS cycle.

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Extended Mode Register Set (EMRS)

The extended mode register stores the data enabling or disabling DLL, and selecting output drive strength. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA0 (The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0~A12 and BA0~BA1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is written in the extended mode register. Two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. A1 and A6 are used for selecting output drive strength. "High" on BA0 is used for EMRS. All the other address pins except A0~A1, A6 and BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.



A6	A1	Drive Strength
0	0	Normal
0	1	Weak
1	0	RFU
1	1	Matched impedance

A0	DLL Enable
0	Enable
1	Disable

BA1	BA0	Operating Mode
0	0	MRS Cycle
0	1	EMRS Cycle

Note: RFU (Reserved for future use) must stay "0" during EMRS cycle.

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Burst Address Ordering for Burst Length

Burst Length	Starting Address (A2, A1, A0)	Sequential Mode	Interleave Mode
2	xx0	0, 1	0, 1
	xx1	1, 0	1, 0
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

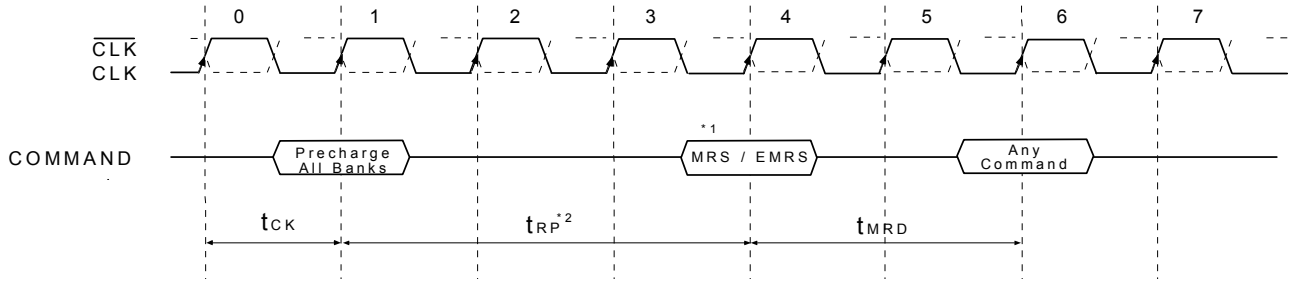
DLL Enable / Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation (upon exiting Self Refresh Mode, the DLL is enabled automatically). Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Output Drive Strength

The normal drive strength for all outputs is specified to be SSTL_2, Class II. The device also support reduced drive strength options, intended for lighter load and/or point-to-point environments.

Mode Register



*1: MRS/EMRS can be issued only at all banks precharge state.
*2: Minimum t_{RP} is required to issue MRS/EMRS command.

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Precharge

The precharge command is used to precharge or close a bank that has activated. The precharge command is issued when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The precharge command can be used to precharge each bank respectively or all banks simultaneously. The bank select addresses (BA0, BA1) are used to define which bank is precharged when the command is initiated. For write cycle, t_{WR}(min) must be satisfied until the precharge command can be issued. After t_{RP} from the precharge, an active command to the same bank can be initiated.

Burst Selection for Precharge by bank address bits

A10/AP	BA1	BA0	Precharge
0	0	0	Bank A Only
0	0	1	Bank B Only
0	1	0	Bank C Only
0	1	1	Bank D Only
1	X	X	All Banks

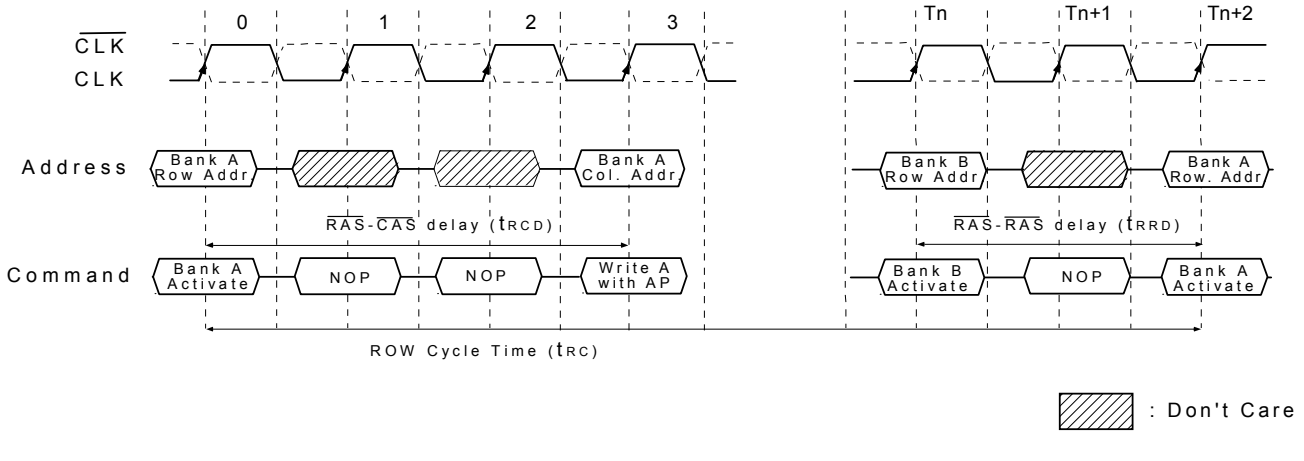
No Operation & Device Deselect

The device should be deselected by deactivating the $\overline{CS}$ signal. In this mode DDR SDRAM should ignore all the control inputs. The DDR SDRAMs are put in NOP mode when $\overline{CS}$ is active and by deactivating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$. For both Deselect and NOP the device should finish the current operation when this command is issued.

Bank / Row Active

The Bank Activation command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock (CLK). The DDR SDRAM has four independent banks, so Bank Select addresses (BA0, BA1) are required. The Bank Activation command must be applied before any Read or Write operation is executed. The Bank Activation command to the first Read or Write command must meet or exceed the minimum of $\overline{RAS}$ to $\overline{CAS}$ delay time (t_{RCD} min). Once a bank has been activated, it must be precharged before another Bank Activation command can be applied to the same bank. The minimum time interval between interleaved Bank Activation command (Bank A to Bank B and vice versa) is the Bank to Bank delay time (t_{RRD} min).

Bank Activation Command Cycle ($\overline{CAS}$ Latency = 3)



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Read

This command is used after the row activate command to initiate the burst read of data. The read command is initiated by activating $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and deasserting $\overline{WE}$ at the same clock rising edge as described in the command truth table. The length of the burst and the CAS latency time will be determined by the values programmed during the MRS command.

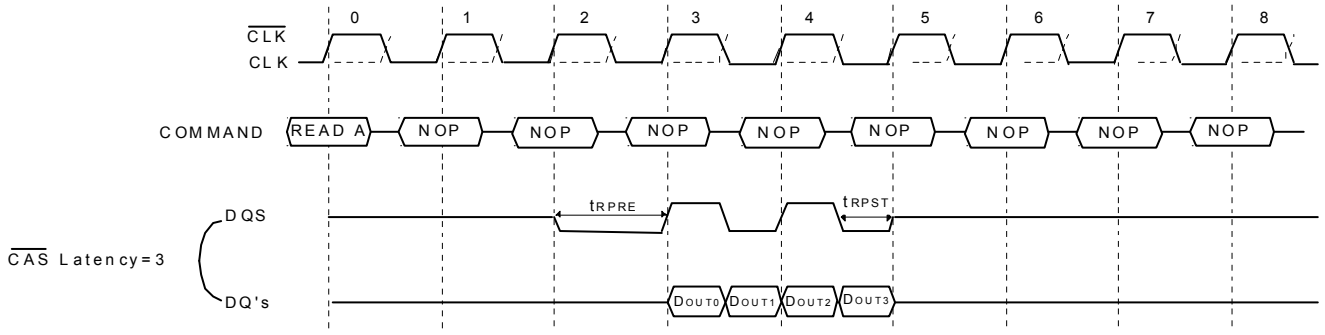
Write

This command is used after the row activate command to initiate the burst write of data. The write command is initiated by activating $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ at the same clock rising edge as describe in the command truth table. The length of the burst will be determined by the values programmed during the MRS command.

Burst Read Operation

Burst Read operation in DDR SDRAM is in the same manner as the current SDRAM such that the Burst read command is issued by asserting $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock (CLK) after t_{RCD} from the bank activation. The address inputs determine the starting address for the Burst. The Mode Register sets type of burst (Sequential or interleave) and burst length (2, 4, 8). The first output data is available after the $\overline{CAS}$ Latency from the READ command, and the consecutive data are presented on the falling and rising edge of Data Strobe (DQS) adopted by DDR SDRAM until the burst length is completed.

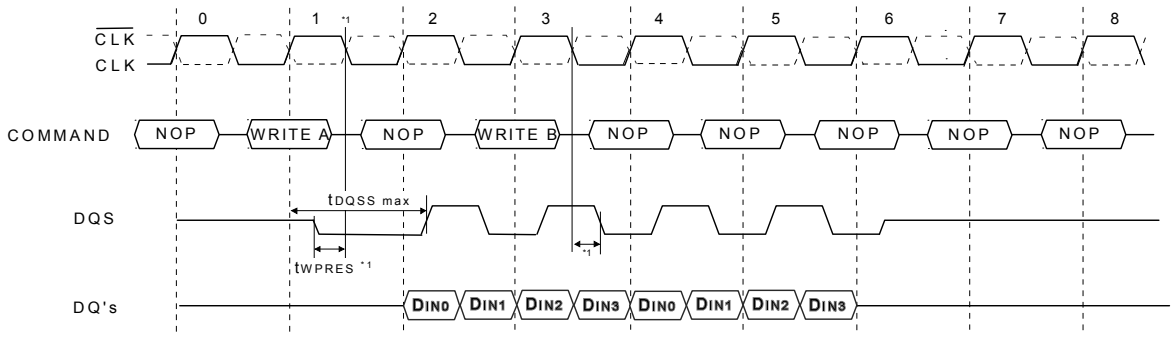
<Burst Length = 4, $\overline{CAS}$ Latency = 3>



Burst Write Operation

The Burst Write command is issued by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock (CLK). The address inputs determine the starting column address. There is no write latency relative to DQS required for burst write cycle. The first data of a burst write cycle must be applied on the DQ pins t_{DS} prior to data strobe edge enabled after t_{DQSS} from the rising edge of the clock (CLK) that the write command is issued. The remaining data inputs must be supplied on each subsequent falling and rising edge of Data Strobe until the burst length is completed. When the burst has been finished, any additional data supplied to the DQ pins will be ignored.

<Burst Length = 4>

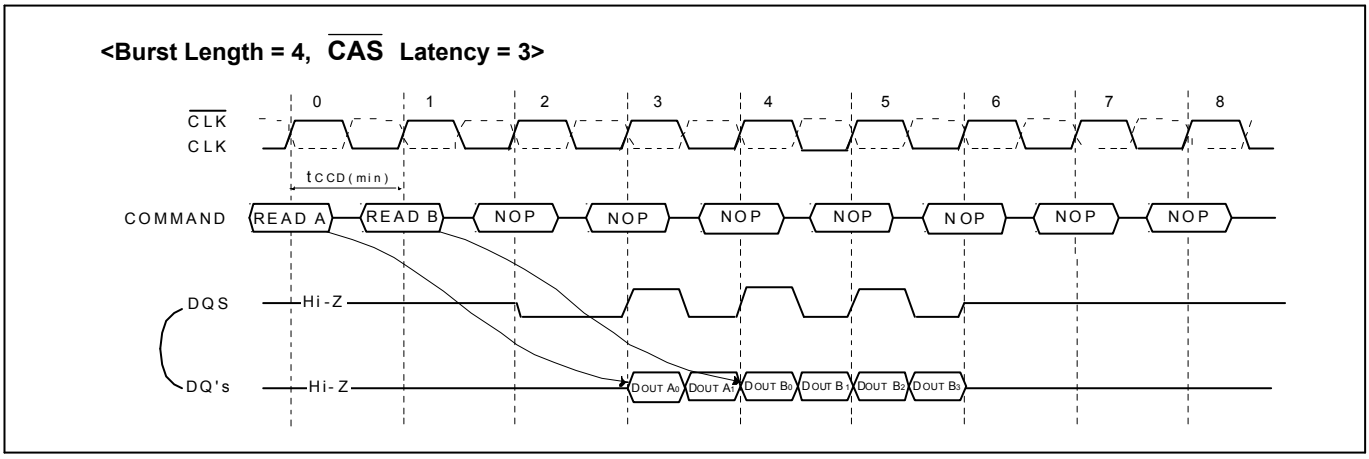


Note * 1: The specific requirement is that DQS be valid (High or Low) on or before this CLK edge. The case shown (DQS going from High-Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on t_{DQSS}.

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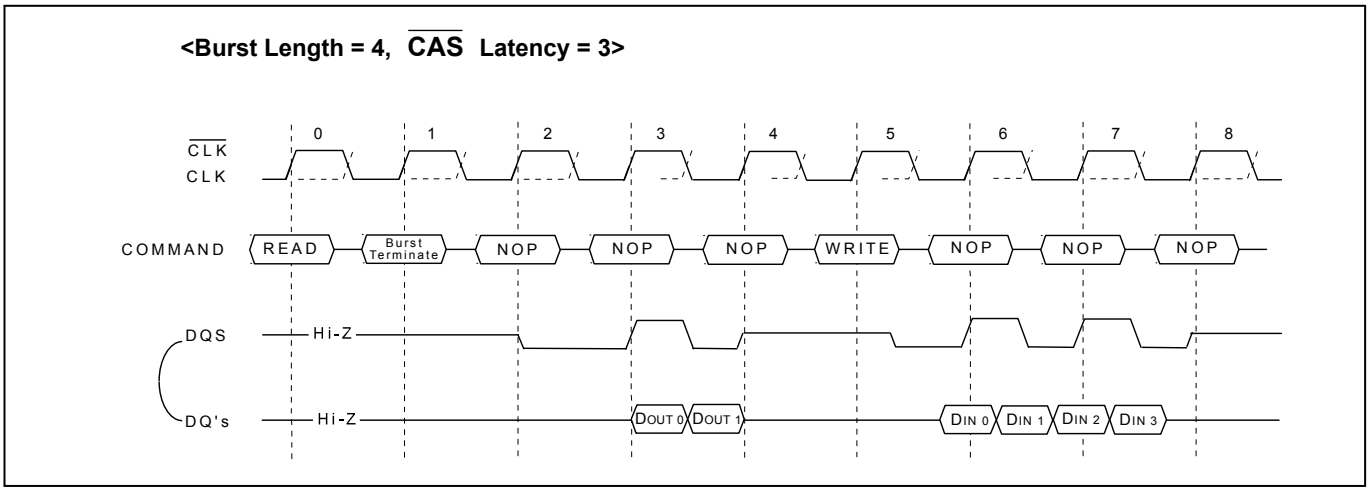
Read Interrupted by a Read

A Burst Read can be interrupted before completion of the burst by new Read command of any bank. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. The data from the first Read command continues to appear on the outputs until the $\overline{CAS}$ latency from the interrupting Read command is satisfied. At this point the data from the interrupting Read command appears. Read to Read interval is t_{CCD}(min).



Read Interrupted by a Write & Burst Terminate

To interrupt a burst read with a write command, Burst Terminate command must be asserted to avoid data contention on the I/O bus by placing the DQ's (Output drivers) in a high impedance state. To insure the DQ's are tri-stated one cycle before the beginning the write operation, Burt stop command must be applied at least RU(CL) clocks [RU mean round up to the nearest integer] before the Write command.



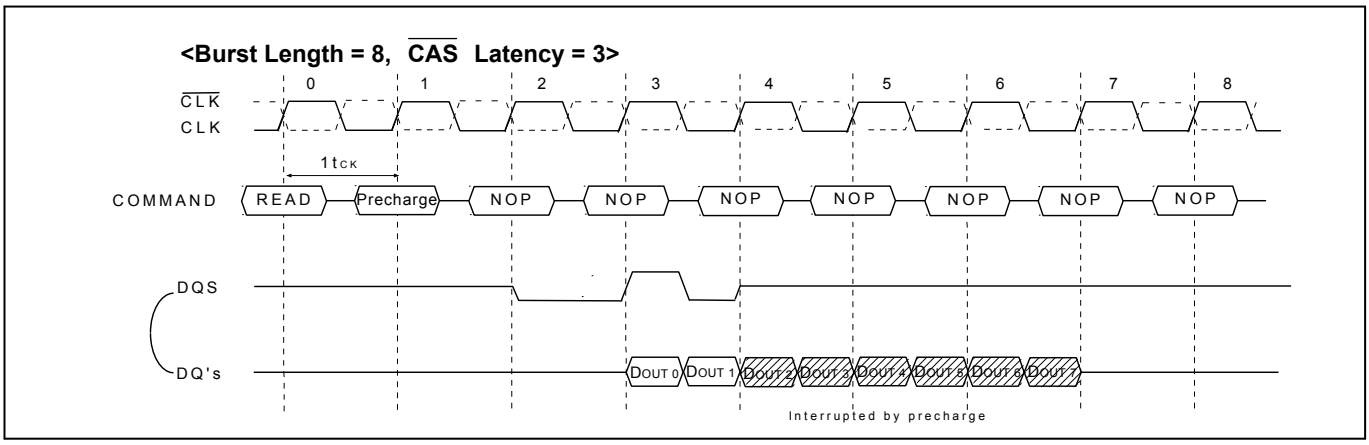
The following functionality establishes how a Write command may interrupt a Read burst.

1. For Write commands interrupting a Read burst, a Burst Terminate command is required to stop the read burst and tristate the DQ bus prior to valid input write data. Once the Burst Terminate command has been issued, the minimum delay to a Write command = RU(CL) [CL is the $\overline{CAS}$ Latency and RU means round up to the nearest integer].
2. It is illegal for a Write and Burst Terminate command to interrupt a Read with auto precharge command.

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Read Interrupted by a Precharge

A Burst Read operation can be interrupted by precharge of the same bank. The minimum 1 clock is required for the read to precharge intervals. A precharge command to output disable latency is equivalent to the $\overline{CAS}$ latency.



When a burst Read command is issued to a DDR SDRAM, a Precharge command may be issued to the same bank before the Read burst is complete. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

1. For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be given on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the $\overline{CAS}$ Latency. A new Bank Activate command may be issued to the same bank after t_{RP} (RAS precharge time).
2. When a Precharge command interrupts a Read burst operation, the Precharge command may be given on the rising clock edge which is CL clock cycles before the last data from the interrupted Read burst where CL is the $\overline{CAS}$ Latency. Once the last data word has been output, the output buffers are tristated. A new Bank Activate command may be issued to the same bank after t_{RP}.
3. For a Read with auto precharge command, a new Bank Activate command may be issued to the same bank after t_{RP} where t_{RP} begins on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the $\overline{CAS}$ Latency. During Read with auto precharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command would initiate a precharge operation without interrupting the Read burst as described in 1 above.
4. For all cases above, t_{RP} is an analog delay that needs to be converted into clock cycles. The number of clock cycles between a Precharge command and a new Bank Activate command to the same bank equals t_{RP} / t_{CK} (where t_{CK} is the clock cycle time) with the result rounded up to the nearest integer number of clock cycles.

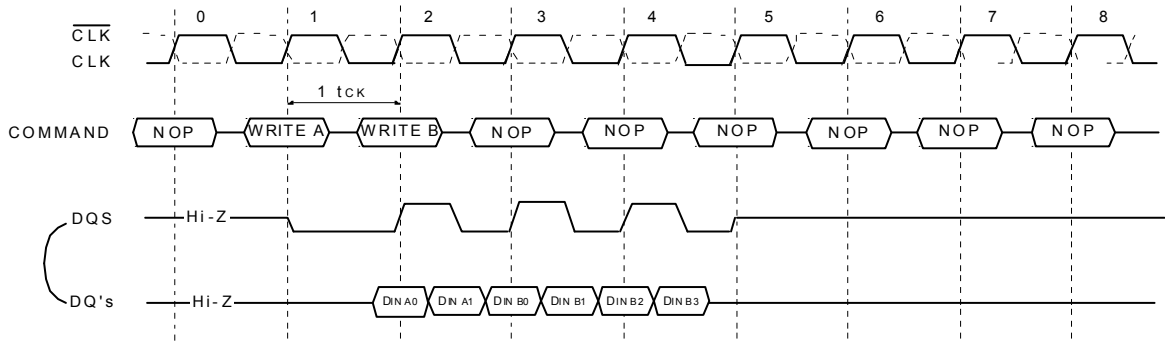
In all cases, a Precharge operation cannot be initiated unless t_{RAS} (min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Read with auto precharge commands where t_{RAS} (min) must still be satisfied such that a Read with auto precharge command has the same timing as a Read command followed by the earliest possible Precharge command which does not interrupt the burst.

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Write Interrupted by a Write

A Burst Write can be interrupted before completion of the burst by a new Write command, with the only restriction that the interval that separates the commands must be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

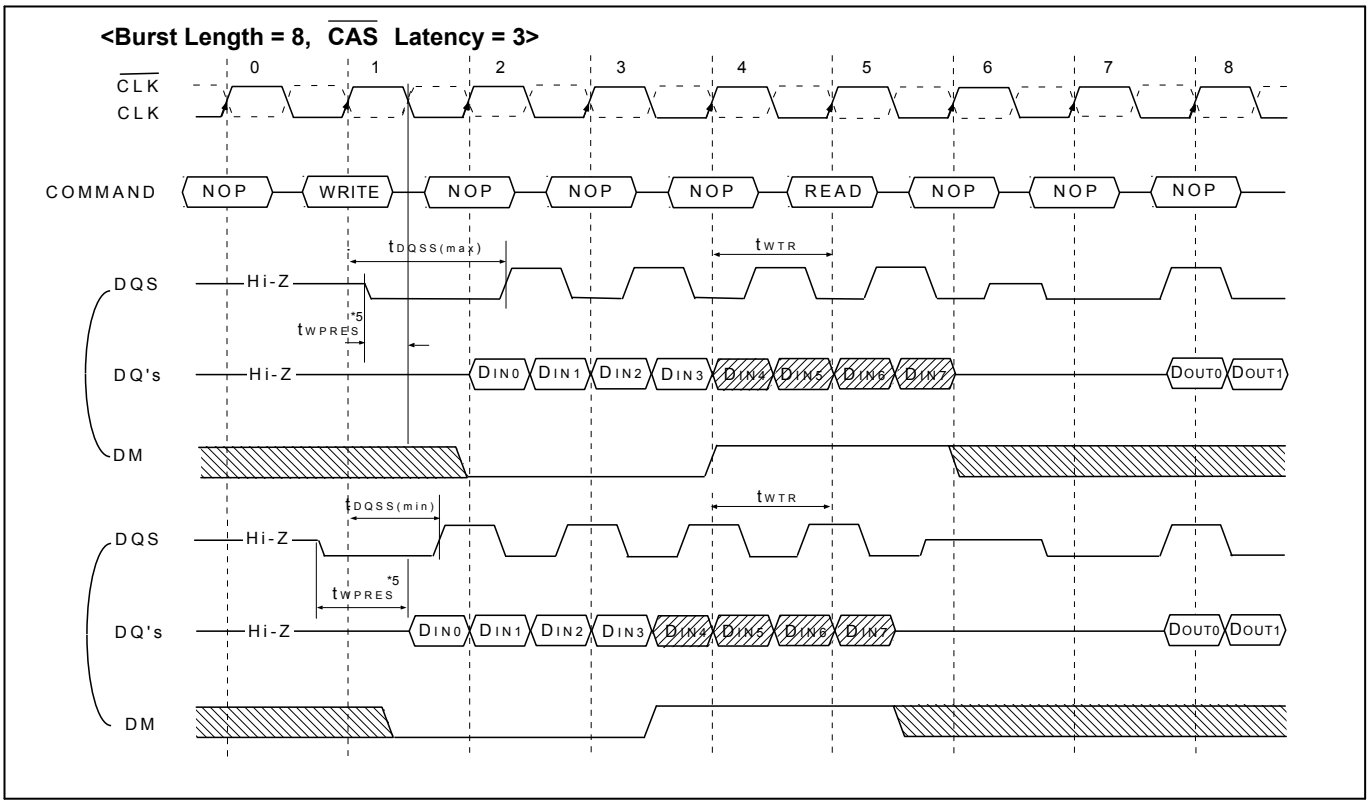
<Burst Length = 4>



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Write Interrupted by a Read & DM

A burst write can be interrupted by a read command of any bank. The DQ's must be in the high impedance state at least one clock cycle before the interrupting read data appear on the outputs to avoid data contention. When the read command is registered, any residual data from the burst write cycle must be masked by DM. The delay from the last data to read command (t_{WTR}) is required to avoid the data contention DRAM inside. Data that are presented on the DQ pins before the read command is initiated will actually be written to the memory. Read command interrupting write can not be issued at the next clock edge of that of write command.



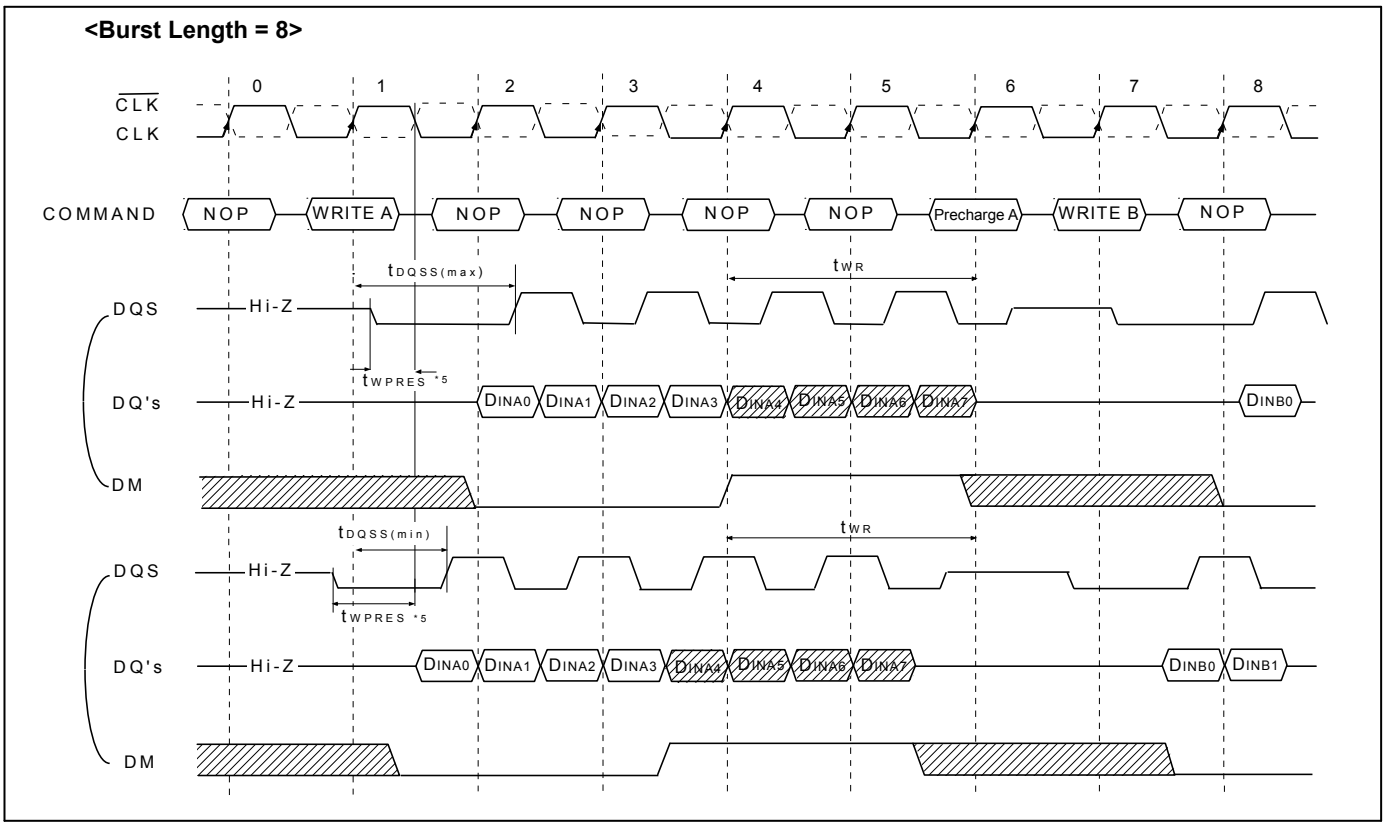
The following functionality established how a Read command may interrupt a Write burst and which input data is not written into the memory.

1. For Read commands interrupting a Write burst, the minimum Write to Read command delay is 2 clock cycles. The case where the Write to Read delay is 1 clock cycle is disallowed.
2. For read commands interrupting a Write burst, the DM pin must be used to mask the input data words which immediately precede the interrupting Read operation and the input data word which immediately follows the interrupting Read operation.
3. For all cases of a Read interrupting a Write, the DQ and DQS buses must be released by the driving chip (i.e., the memory controller) in time to allow the buses to turn around before the SDRAM drives them during a read operation.
4. If input Write data is masked by the Read command, the DQS inputs are ignored by the DDR SDRAM.
5. Refer to "Burst write operation"

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Write Interrupted by a Precharge & DM

A burst write operation can be interrupted before completion of the burst by a precharge of the same bank. Random column access is allowed. A write recovery time (t_{WR}) is required from the last data to precharge command. When precharge command is asserted, any residual data from the burst write cycle must be masked by DM.



Precharge timing for Write operations in DRAMs requires enough time to allow "write recovery" which is the time required by a DRAM core to properly store a full "0" or "1" level before a Precharge operation. For DDR SDRAM, a timing parameter, t_{WR}, is used to indicate the required of time between the last valid write operation and a Precharge command to the same bank.

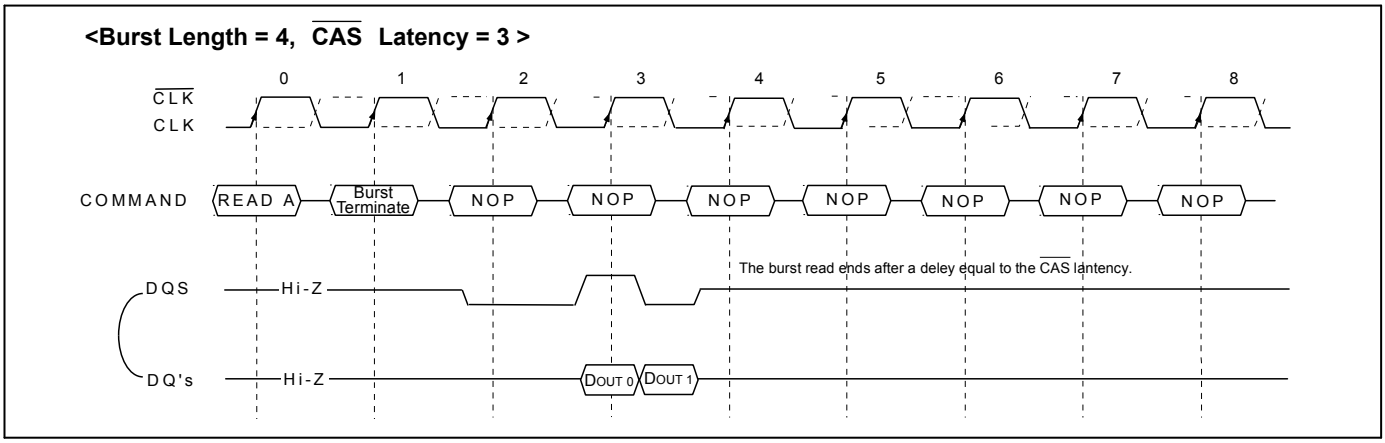
t_{WR} starts on the rising clock edge after the last possible DQS edge that strobed in the last valid and ends on the rising clock edge that strobes in the precharge command.

1. For the earliest possible Precharge command following a Write burst without interrupting the burst, the minimum time for write recovery is defined by t_{WR}.
2. When a precharge command interrupts a Write burst operation, the data mask pin, DM, is used to mask input data during the time between the last valid write data and the rising clock edge in which the Precharge command is given. During this time, the DQS input is still required to strobe in the state of DM. The minimum time for write recovery is defined by t_{WR}.
3. For a Write with auto precharge command, a new Bank Activate command may be issued to the same bank after $t_{WR} + t_{RP}$ where $t_{WR} + t_{RP}$ starts on the falling DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the Bank Activate commands. During write with auto precharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command without interrupting the Write burst as described in 1 above.
4. In all cases, a Precharge operation cannot be initiated unless t_{RAS}(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Write with auto precharge commands where t_{RAS}(min) must still be satisfied such that a Write with auto precharge command has the same timing as a Write command followed by the earliest possible Precharge command which does not interrupt the burst.
5. Refer to "Burst write operation"

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Burst Terminate

The burst terminate command is initiated by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock (CLK). The burst terminate command has the fewest restrictions making it the easiest method to use when terminating a burst read operation before it has been completed. When the burst terminate command is issued during a burst read cycle, the pair of data and DQS (Data Strobe) go to a high impedance state after a delay which is equal to the $\overline{CAS}$ latency set in the mode register. The burst terminate command, however, is not supported during a write burst operation.



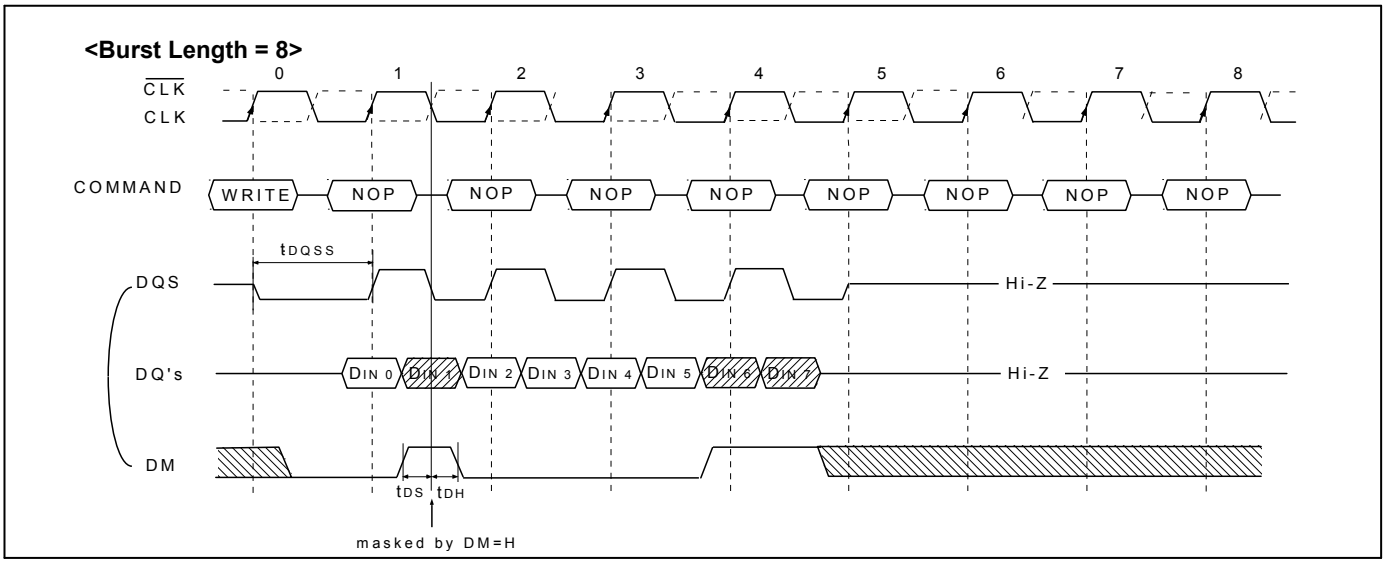
The Burst Terminate command is a mandatory feature for DDR SDRAMs. The following functionality is required.

1. The BST command may only be issued on the rising edge of the input clock, CLK.
2. BST is only a valid command during Read burst.
3. BST during a Write burst is undefined and shall not be used.
4. BST applies to all burst lengths.
5. BST is an undefined command during Read with auto precharge and shall not be used.
6. When terminating a burst Read command, the BST command must be issued L_{BST} ("BST Latency") clock cycles before the clock edge at which the output buffers are tristated, where L_{BST} equals the $\overline{CAS}$ latency for read operations.
7. When the burst terminates, the DQ and DQS pins are tristated.

The BST command is not byte controllable and applies to all bits in the DQ data word and the (all) DQS pin(s).

DM masking

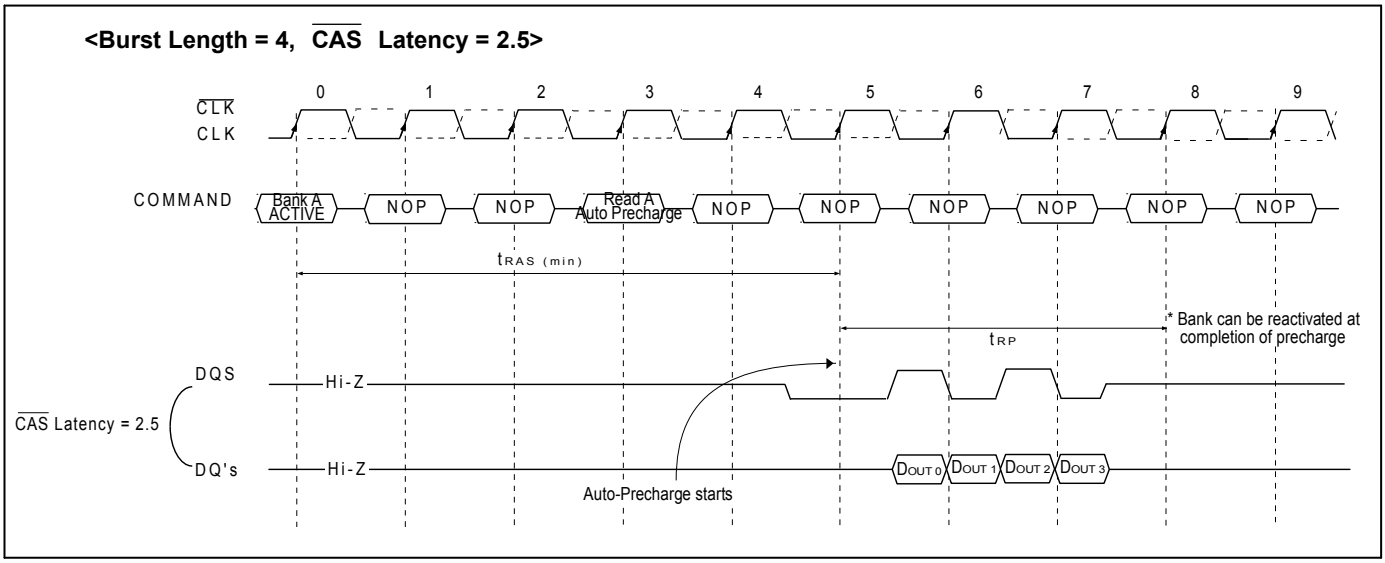
The DDR SDRAM has a data mask function that can be used in conjunction with data write cycle. Not read cycle. When the data mask is activated (DM high) during write operation, DDR SDRAM does not accept the corresponding data. (DM to data-mask latency is zero) DM must be issued at the rising or falling edge of data strobe.



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Read With Auto Precharge

If a read with auto precharge command is initiated, the DDR SDRAM automatically enters the precharge operation BL/2 clock later from a read with auto precharge command when t_{RAS} (min) is satisfied. If not, the start point of precharge operation will be delayed until t_{RAS} (min) is satisfied. Once the precharge operation has started the bank cannot be reactivated and the new command can not be asserted until the precharge time (t_{RP}) has been satisfied.



When the Read with Auto Precharge command is issued, new command can be asserted at 4, 5 and 6 respectively as follow.

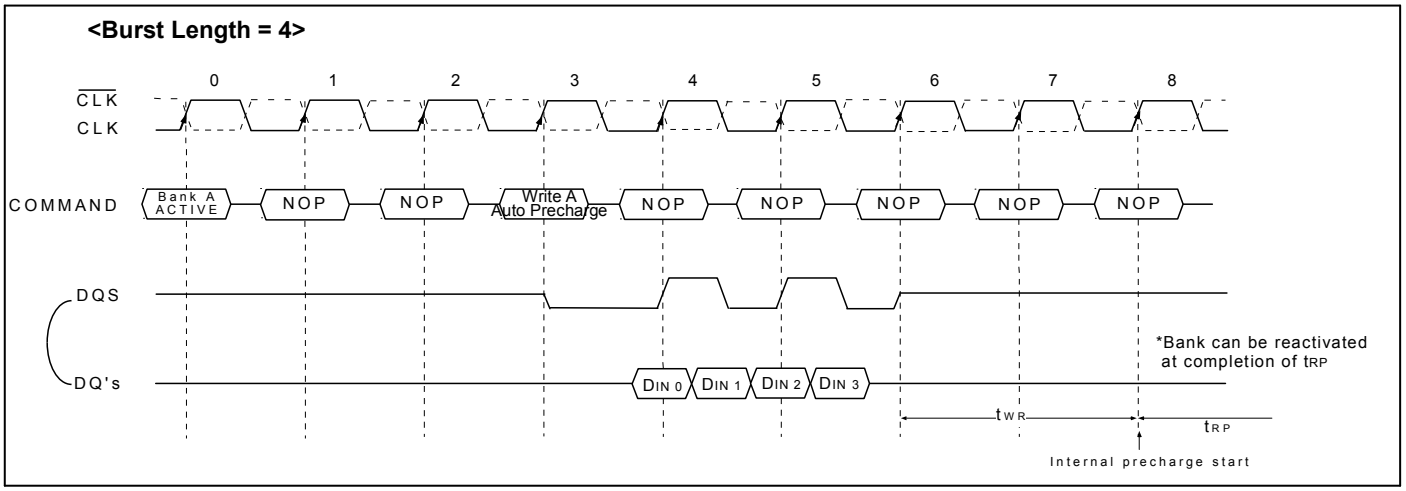
Asserted Command	For the same bank			For the different bank		
	4	5	6	4	5	6
READ	READ	Illegal	Illegal	Legal	Legal	Legal
READ with AP[*1]	READ with AP	Illegal	Illegal	Legal	Legal	Legal
Active	Illegal	Illegal	Illegal	Legal	Legal	Legal
Precharge	Legal	Legal	Illegal	Legal	Legal	Legal

Note 1: AP = Auto Precharge

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Write with Auto Precharge

If A10 is high when write command is issued, the write with auto-precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins at the rising edge of the CLK with the t_{WR} delay after the last data-in.



At burst read / write with auto precharge, $\overline{CAS}$ interrupt of the same bank is illegal.

Asserted Command	For the same bank					For the different bank				
	4	5	6	7	8	4	5	6	7	8
WRITE	WRITE	WRITE	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
WRITE with AP*1	WRITE with AP	WRITE with AP	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
READ	Illegal	READ + DM*2	READ+ DM	READ	Illegal	Illegal	Illegal	Illegal	Legal	Legal
READ with AP	Illegal	READ with AP+ DM	READ with AP+ DM	READ with AP	Illegal	Illegal	Illegal	Illegal	Legal	Legal
Active	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
Precharge	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal

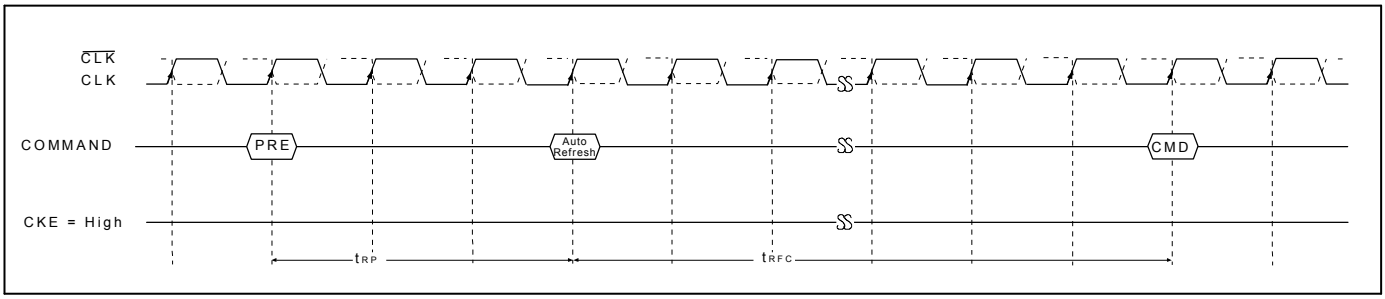
Note: 1. AP = Auto Precharge
2. DM: Refer to “Write Interrupted by a Read & DM“

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Auto Refresh & Self Refresh

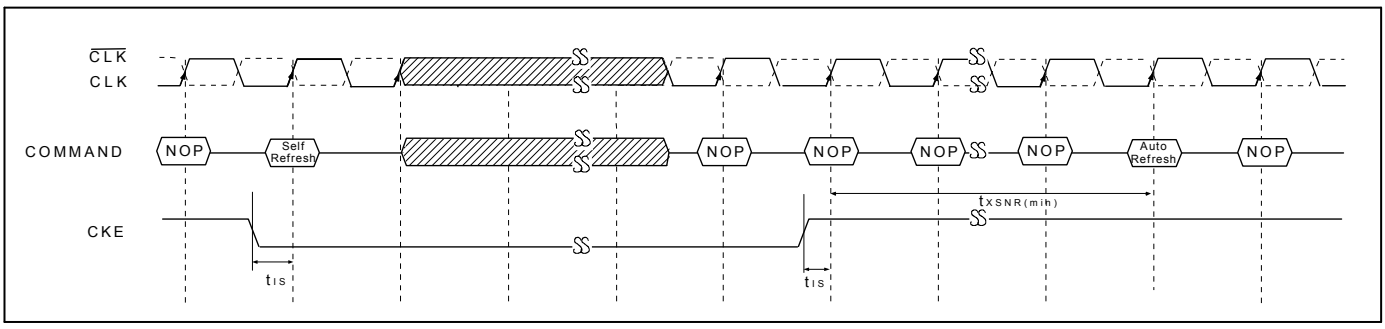
Auto Refresh

An auto refresh command is issued by having $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ held low with CKE and $\overline{WE}$ high at the rising edge of the clock (CLK). All banks must be precharged and idle for t_{RP}(min) before the auto refresh command is applied. No control of the external address pins is requires once this cycle has started because of the internal address counter. When the refresh cycle has completed, all banks will be in the idle state. A delay between the auto refresh command and the next activate command or subsequent auto refresh command must be greater than or equal to the t_{RFC}(min).
A maximum of eight consecutive AUTO REFRESH commands (with t_{RFC}(min)) can be posted to any given DDR SDRAM meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8 x t_{REFI} .



Self Refresh

A self refresh command is defines by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock (CLK). Once the self refresh command is initiated, CKE must be held low to keep the device in self refresh mode. During the self refresh operation, all inputs except CKE are ignored. Since CKE is an SSTL_2 input, V_{REF} must be maintained during self refresh. The clock is internally disabled during self refresh operation to reduce power consumption. The self refresh is exited by supplying stable clock input before returning CKE high, asserting deselect or NOP command and then asserting CKE high for longer than t_{XSRD} for locking of DLL.



Note: After self refresh exit, input an auto refresh command immediately.

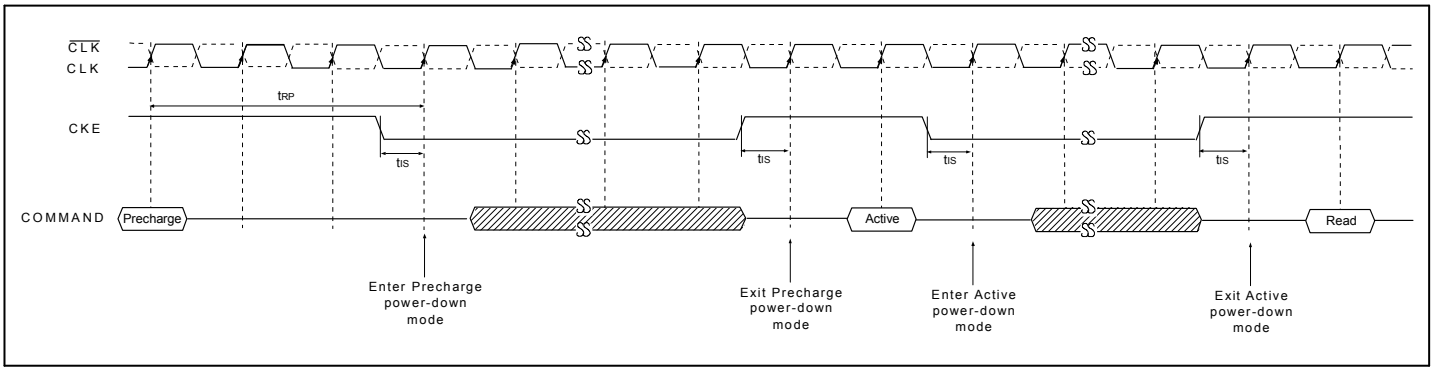
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Power down

Power down is entered when CKE is registered Low (no accesses can be in progress). If power down occurs when all banks are idle, this mode is referred to as precharge power-down; if power down occurs when there is a row active in any bank, this mode is referred to as active power-down.

Entering power down deactivates the input and output buffers, excluding CLK, $\overline{CLK}$ and CKE. In power down mode, CKE Low must be maintained, and all other input signals are "Don't Care". The minimum power down duration is at least 1 t_{CK} + t_{IS}. However, power down duration is limited by the refresh requirements of the device.

The power down state is synchronously exited when CKE is registered High (along with a NOP or DESELECT command). A valid command may be applied 1 t_{CK} + t_{IS} after exit from power down.



Functional Truth Table

Truth Table – CKE [Note 1~4, 6]

CKE n-1	CKE n	Current State	COMMAND n	ACTION n	NOTE
L	L	Power Down	X	Maintain Power Down	
L	L	Self Refresh	X	Maintain Self Refresh	7
L	H	Power Down	NOP or DESELECT	Exit Power Down	
L	H	Self Refresh	NOP or DESELECT	Exit Self Refresh	5, 7
H	L	All Banks Idle	NOP or DESELECT	Precharge Power Down Entry	
H	L	Bank(s) Active	NOP or DESELECT	Active Power Down Entry	
H	L	All Banks Idle	AUTO REFRESH	Self Refresh Entry	
H	H	See the Truth Tables as follow			

Notes:

1. CKE n is the logic state of CKE at clock edge n; CKE n-1 was the state of CKE at the previous clock edge.
2. Current state is the state of DDR SDRAM immediately prior to clock edge n.
3. COMMAND n is the command registered at clock edge n, and ACTION n is the result of COMMAND n.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT and NOP DESELECT or NOP commands should be issued on any clock edges occurring during the t_{XSNR} or t_{XSRD} period. A minimum of 200 clock cycles is needed before applying any executable command, for the DLL to lock.
6. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
7. V_{REF} must be maintained during Self Refresh operation.

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Truth Table – Current State Bank n

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND / ACTION	NOTE
Command to Bank n [Note 1~6,13]						
Any	H	X	X	X	DESELECT (NOP / continue previous operation)	
	L	H	H	H	No Operation (NOP / continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	MODE REGISTER SET	7
Row Active	L	H	L	H	READ (select column & start read burst)	10
	L	H	L	L	WRITE (select column & start write burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (Auto Precharge Disabled)	L	H	L	H	READ (select column & start new read burst)	10
	L	H	L	L	WRITE (select column & start write burst)	10, 12
	L	L	H	L	PRECHARGE (truncate read burst, start precharge)	8
	L	H	H	L	BURST TERMINATE	9
Write (Auto Precharge Disabled)	L	H	L	H	READ (select column & start read burst)	10, 11
	L	H	L	L	WRITE (select column & start new write burst)	10
	L	L	H	L	PRECHARGE (truncate write burst, start precharge)	8, 11
Command to Bank m [Note 1~3, 6,13~15]						
Any	H	X	X	X	DESELECT (NOP / continue previous operation)	
	L	H	H	H	No Operation (NOP / continue previous operation)	
Idle	X	X	X	X	Any command allowed to bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start read burst)	10
	L	H	L	L	WRITE (select column & start write burst)	10
	L	L	H	L	PRECHARGE	
Read (Auto Precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start new read burst)	10
	L	H	L	L	WRITE (select column & start write burst)	10, 12
	L	L	H	L	PRECHARGE	
Write (Auto Precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start read burst)	10, 11
	L	H	L	L	WRITE (select column & start new write burst)	10
	L	L	H	L	PRECHARGE	
Read with Auto Precharge	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start new read burst)	3a, 10
	L	H	L	L	WRITE (select column & start write burst)	3a, 10, 12
	L	L	H	L	PRECHARGE	
Write with Auto Precharge	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column & start read burst)	3a, 10
	L	H	L	L	WRITE (select column & start new write burst)	3a, 10
	L	L	H	L	PRECHARGE	

Notes:

1. This table applies when CKEn-1 was HIGH and CKEn is HIGH and after t_{XSNR} or t_{XSRD} has been met (if the previous state was self refresh).

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2. This table is bank - specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and t_{RP} has been met.
   Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   Read / Write: A READ / WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
   Read / Write with Auto Precharge Enabled: See following text, notes 3a, 3b:

   3a. For devices which do not support the optional “concurrent auto precharge” feature, the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states can each be broken into two parts: the access period and the precharge period. For Read with Auto Precharge, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For Write with Auto Precharge, the precharge period begins when t_{WR} ends, with t_{WR} measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or t_{RP}) begins. During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other bank may be applied. In either case, all other related limitations apply (e.g., contention between READ data and WRITE data must be avoided).

   3b. For devices which do support the optional “concurrent auto precharge” feature, a read with auto precharge enabled, or a write with auto precharge enabled, may be followed by any command to the other banks, as long as that command does not interrupt the read or write data transfer, and all other related limitations apply (e.g., contention between READ data and WRITE data must be avoided.)
4. The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table.

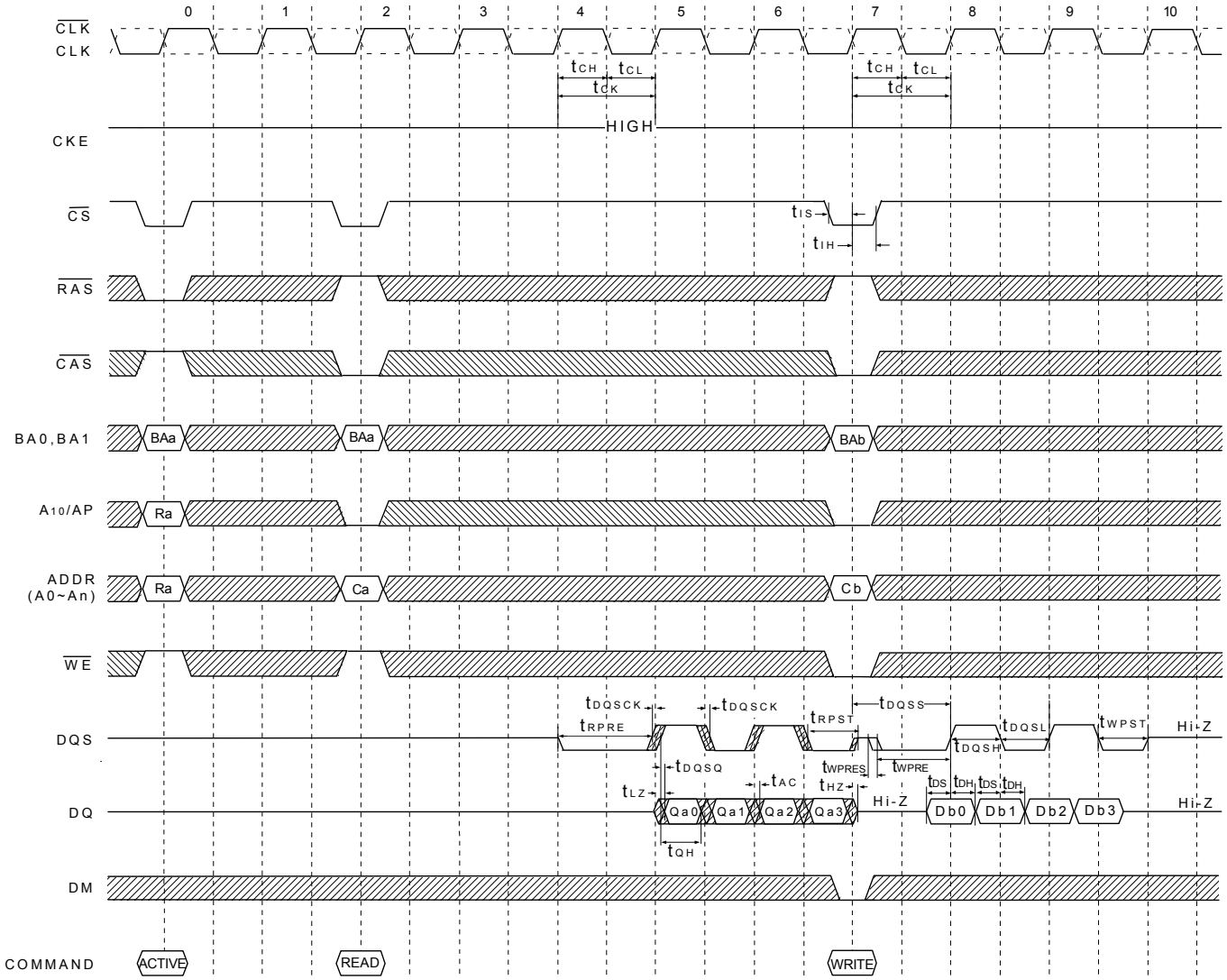
   Precharging: Starts with registration of a PRECHARGE command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.
   Row Activating: Starts with registration of an ACTIVE command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank will be in the ”row active” state.
   Read/ Write with Auto -
   Precharge Enabled: Starts with registration of a READ / WRITE command with AUTO PRECHARGE enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.
5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an AUTO REFRESH command and ends when t_{RC} is met. Once t_{RFC} is met, the DDR SDRAM will be in the ”all banks idle” state.
   Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when t_{MRD} has been met. Once t_{MRD} is met, the DDR SDRAM will be in the ”all banks idle” state.
   Precharging All: Starts with registration of a PRECHARGE ALL command and ends when t_{RP} is met. Once t_{RP} is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank - specific; requires that all banks are idle and no bursts are in progress.
8. May or may not be bank - specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. Not bank - specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
10. Reads or Writes listed in the Command/Action column include Reads or Writes with AUTO PRECHARGE enabled and Reads or Writes with AUTO PRECHARGE disabled.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of the READ burst; otherwise, a Burst Terminate must be used to end the READ prior to asserting a WRITE command,
13. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
14. AUTO REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.
15. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.

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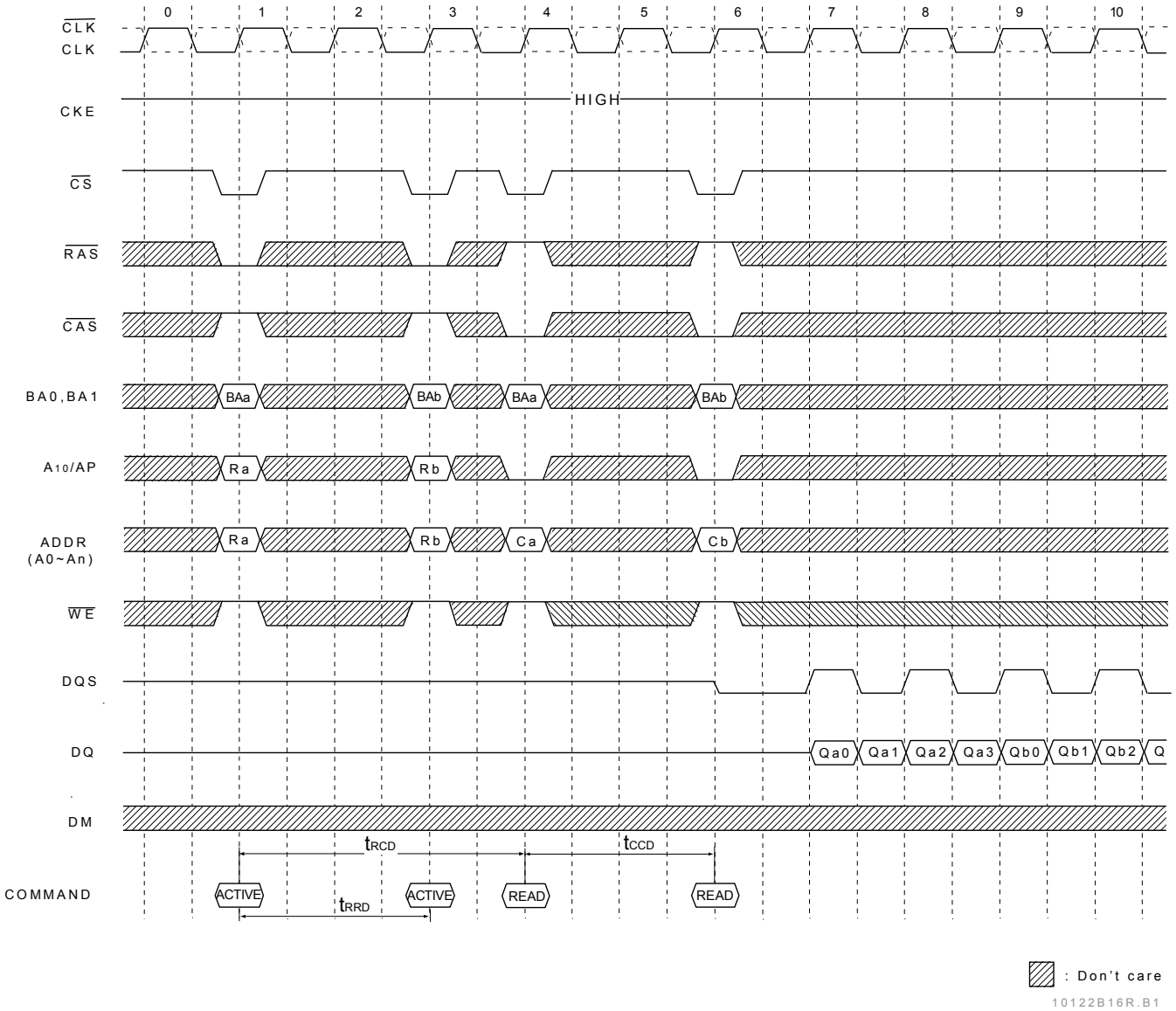
Timing Diagram

Basic Timing (Setup, Hold and Access Time @ BL=4, CL=3)



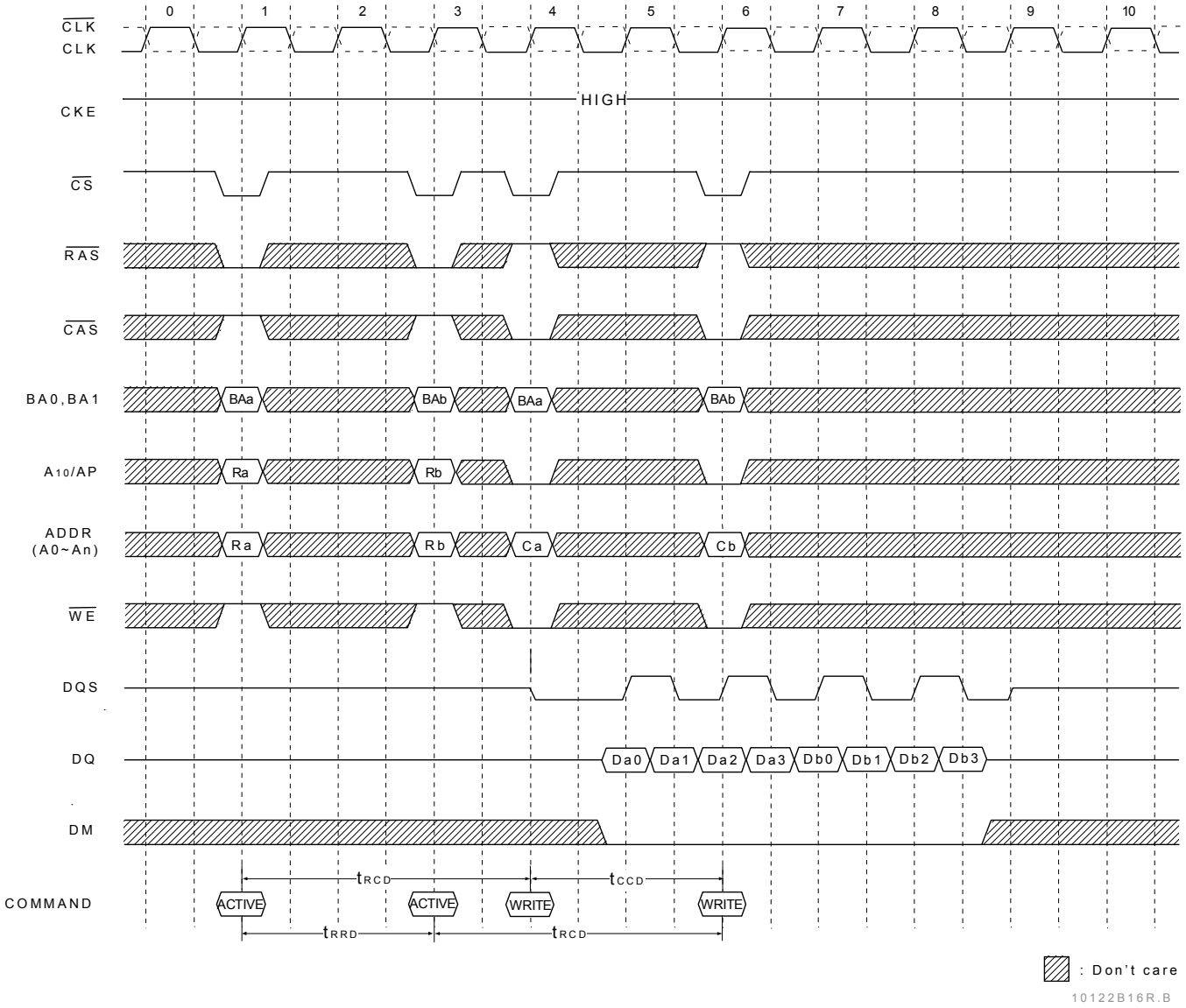
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Multi Bank Interleaving READ (@ BL=4, CL=3)



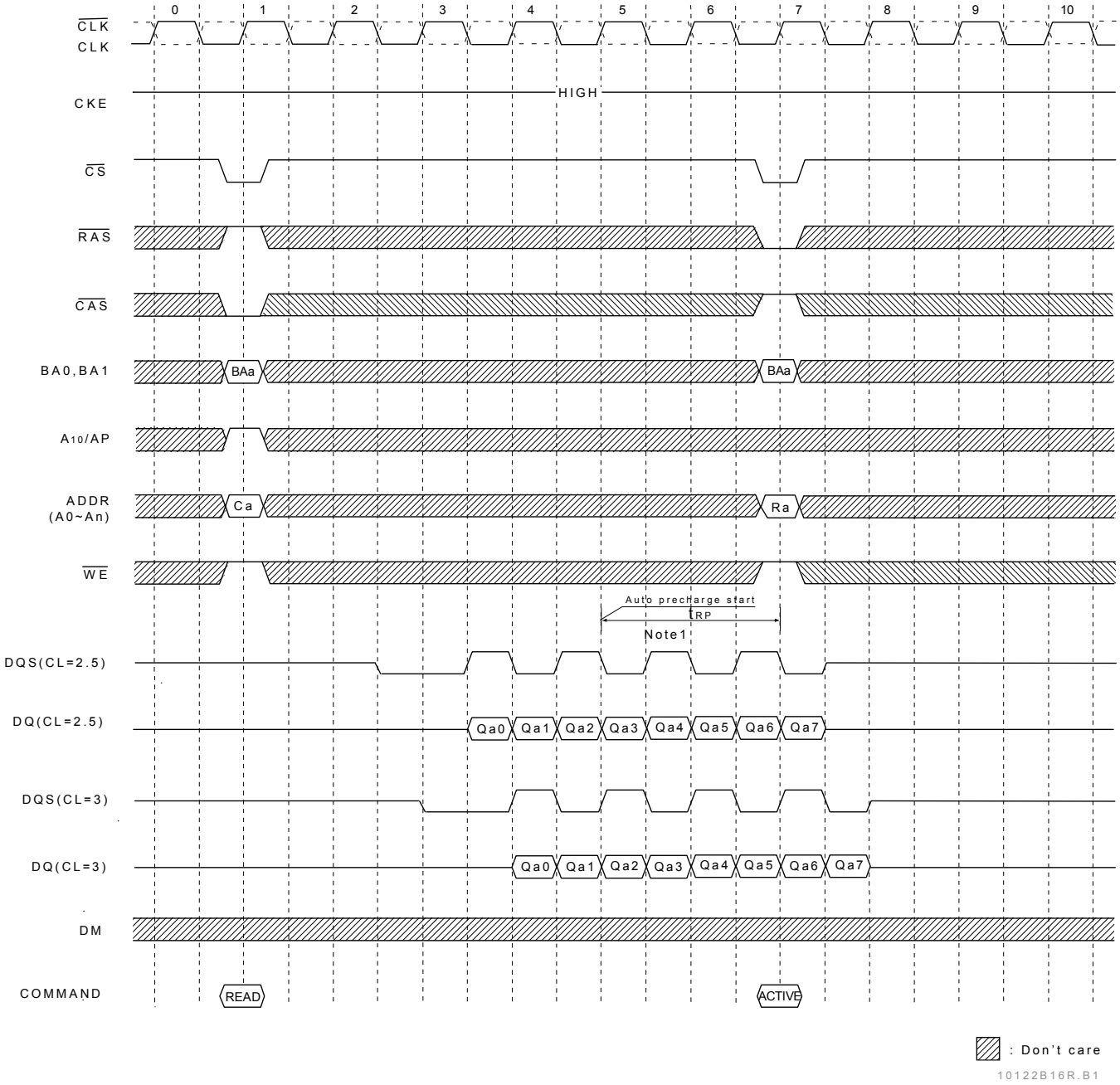
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Multi Bank Interleaving WRITE (@ BL=4)



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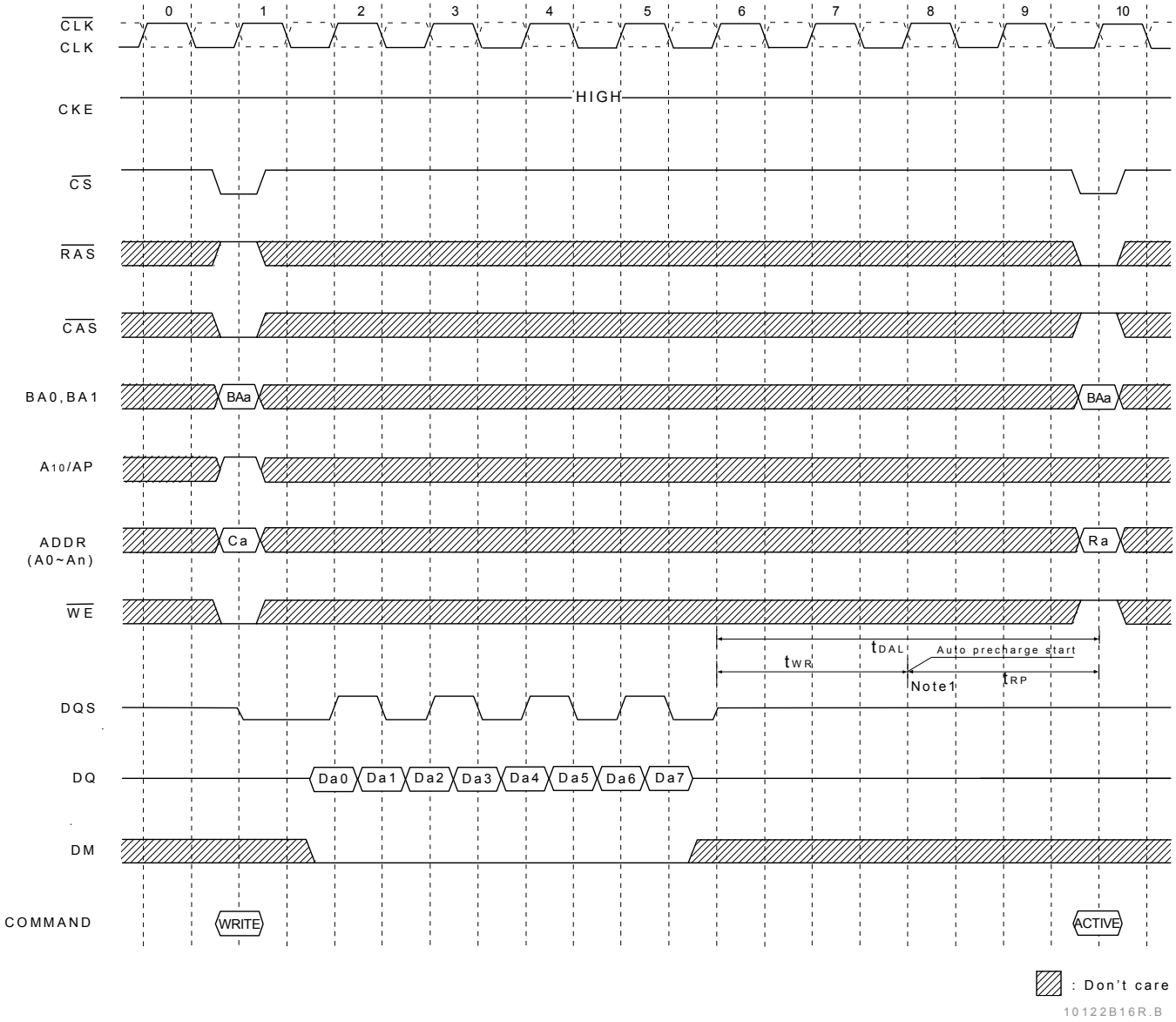
Read with Auto Precharge (@ BL=8)



Note: 1. The row active command of the precharge bank can be issued after t_{RP} from this point.
The new read/write command of another activated bank can be issued from this point.
At burst read/write with auto precharge, $\overline{CAS}$ interrupt of the same/another bank is illegal.

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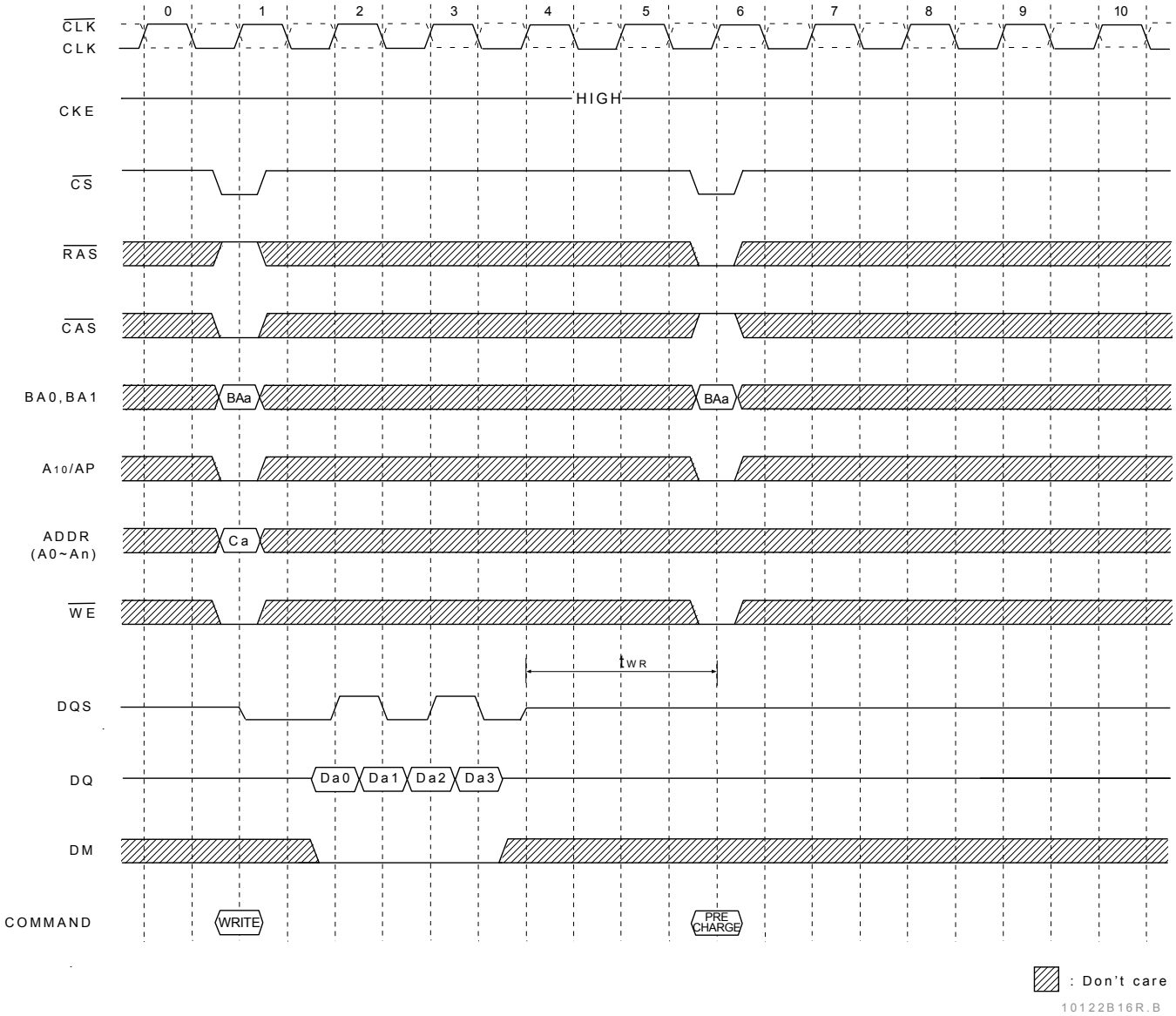
Write with Auto Precharge (@ BL=8)



Note: 1. The row active command of the precharge bank can be issued after t_{RP} from this point.
The new read/write command of another activated bank can be issued from this point.
At burst read/write with auto precharge, $\overline{CAS}$ interrupt of the same/another bank is illegal.

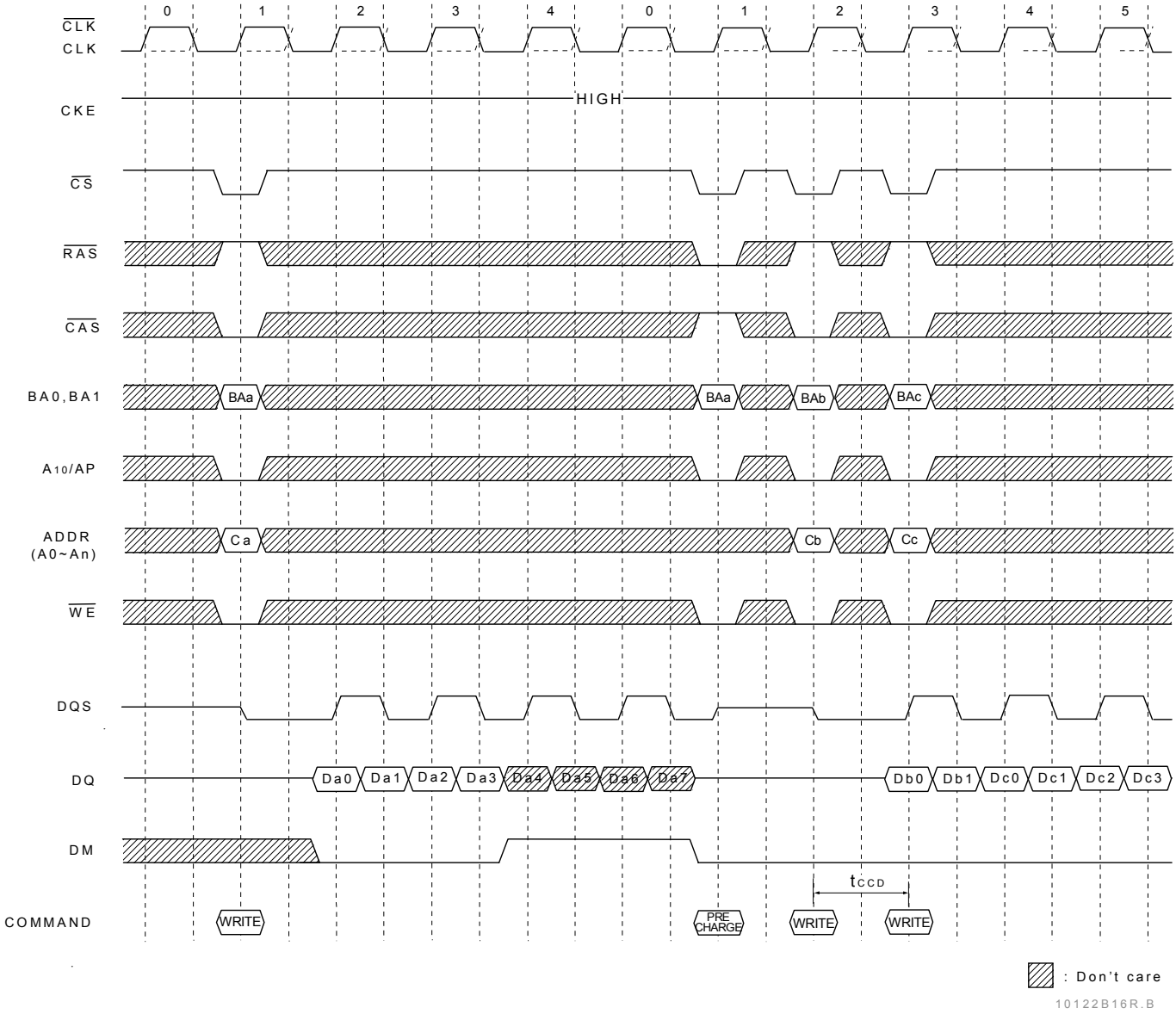
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Write followed by Precharge (@ BL=4)



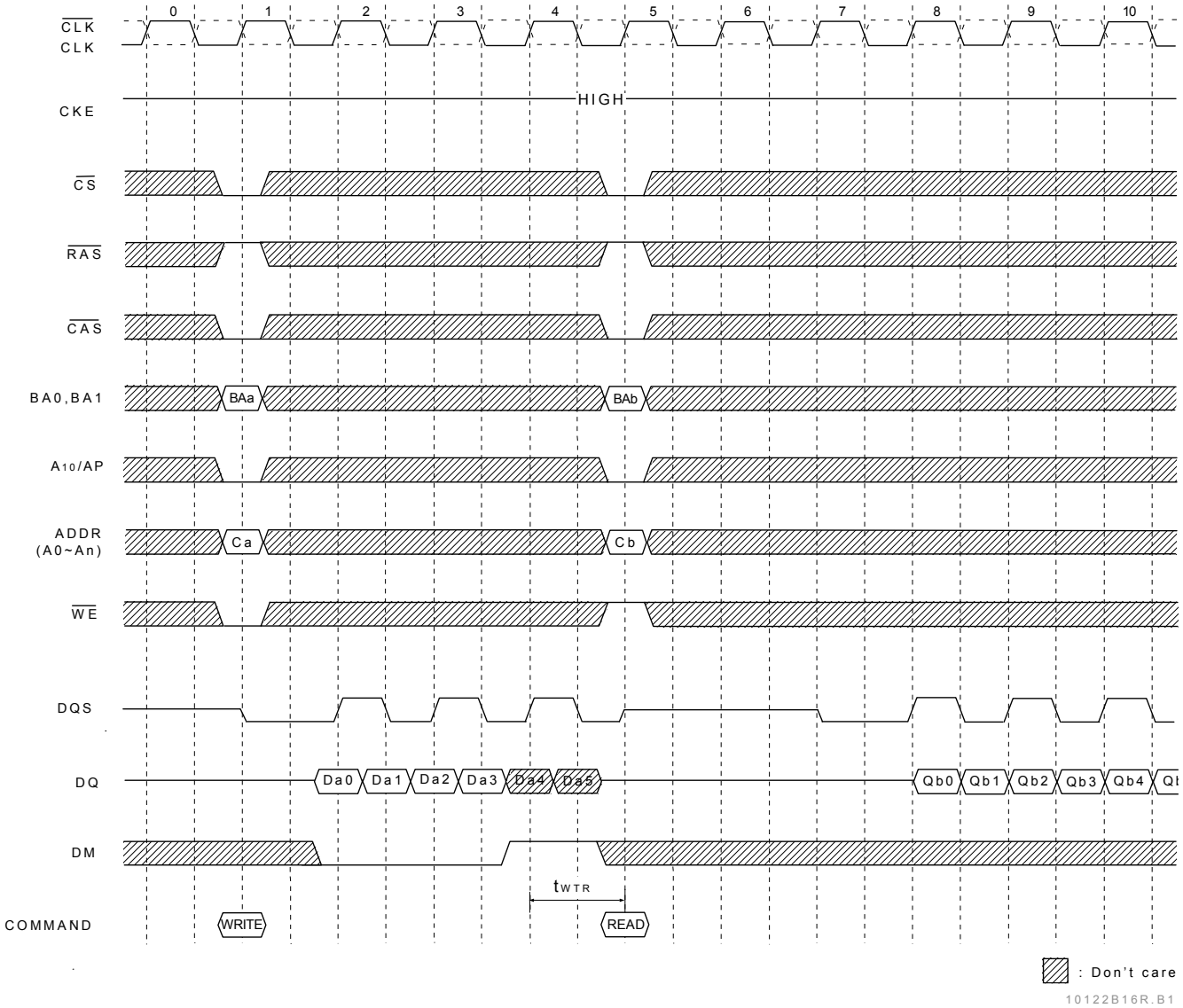
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Write Interrupted by Precharge & DM (@ BL=8)



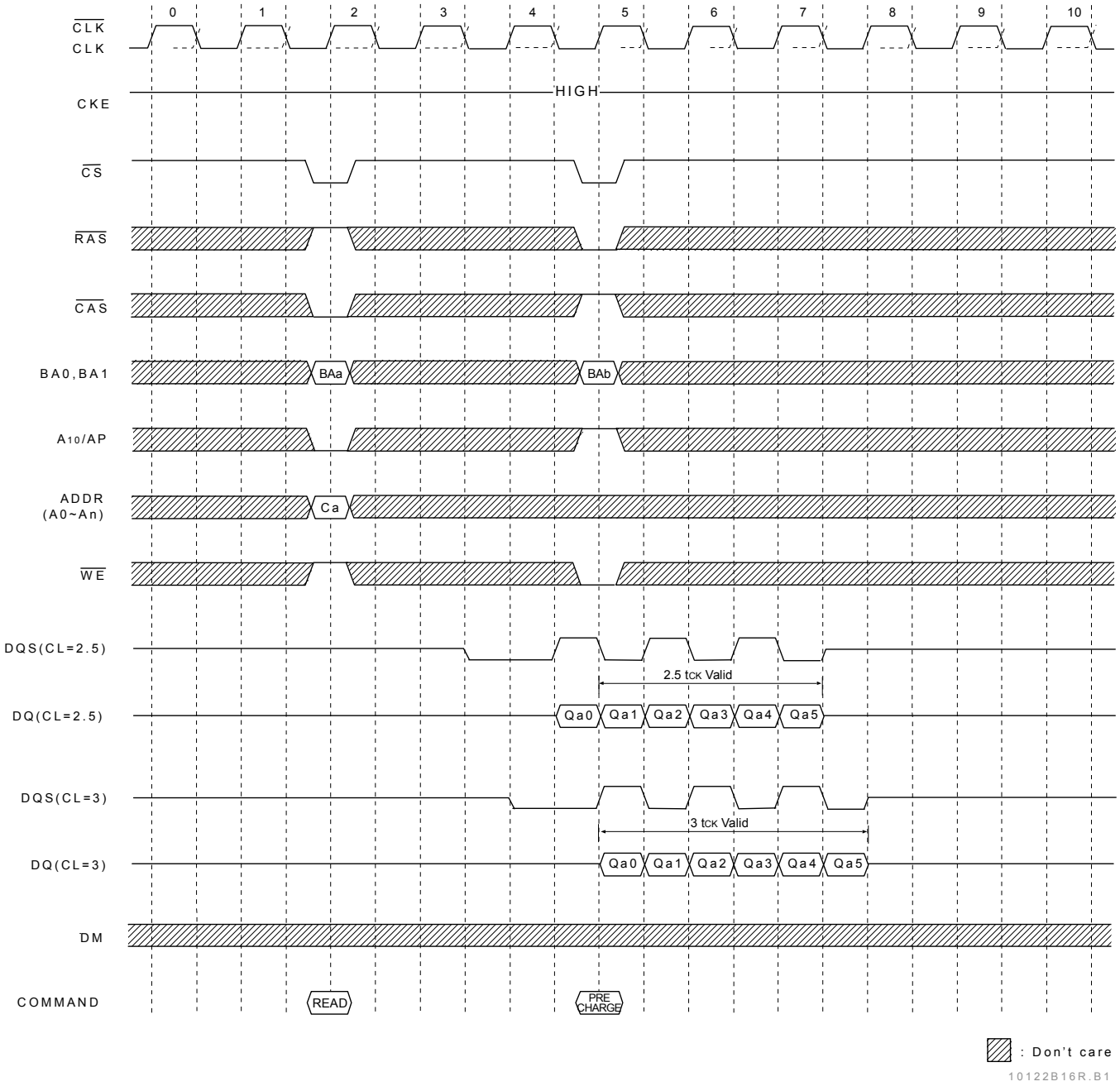
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Write Interrupted by a Read (@ BL=8, CL= 3)



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Read Interrupted by Precharge (@ BL=8)

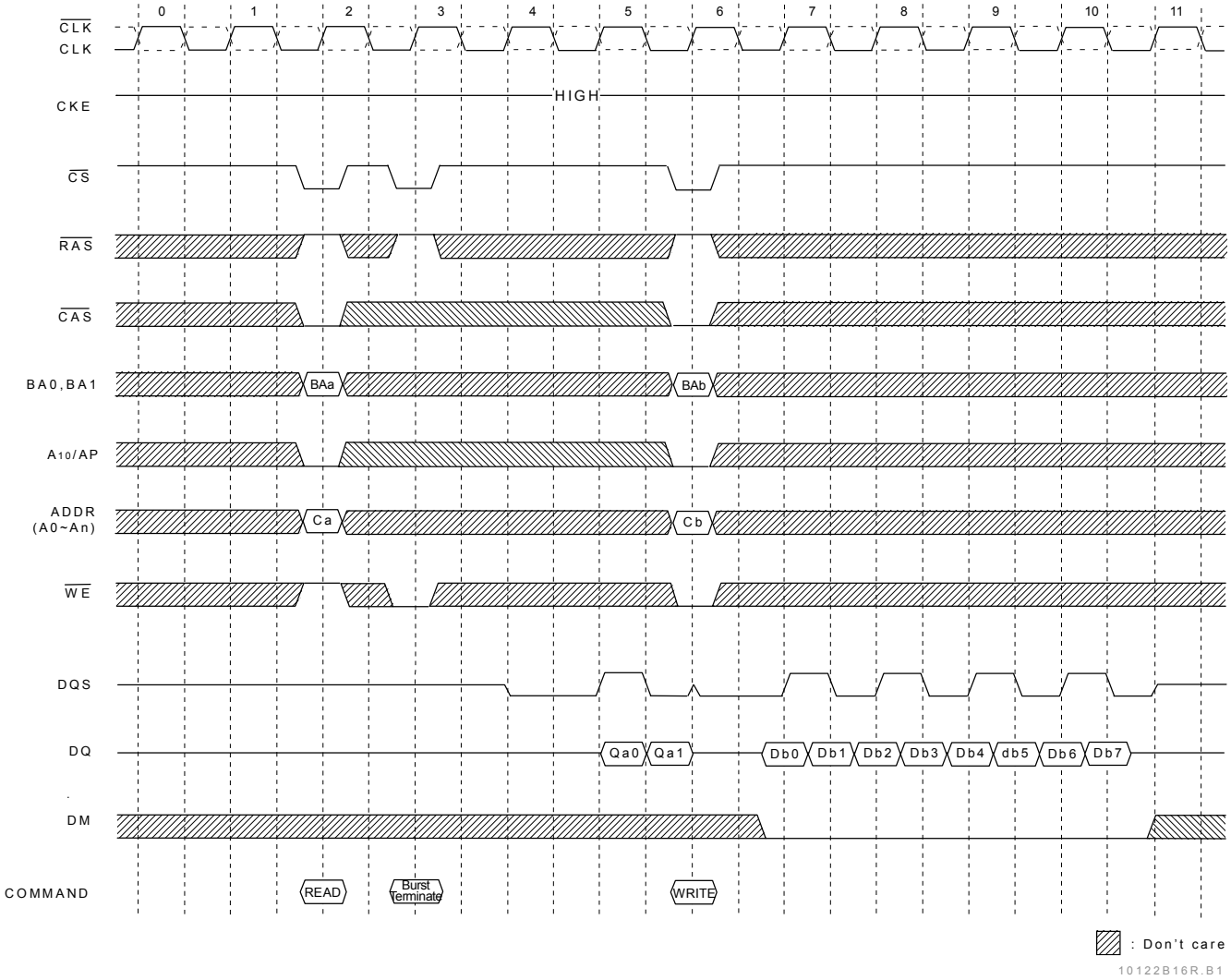


When a burst Read command is issued to a DDR SDRAM, a Precharge command may be issued to the same bank before the Read burst is complete. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

1. For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be given on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the CAS Latency. A new Bank Activate command may be issued to the same bank after t_{RP} (RAS Precharge time).
2. When a Precharge command interrupts a Read burst operation, the Precharge command may be given on the rising clock edge which is CL clock cycles before the last data from the interrupted Read burst where CL is the CAS Latency. Once the last data word has been output, the output buffers are tri-stated. A new Bank Activate command may be issued to the same bank after t_{RP}.

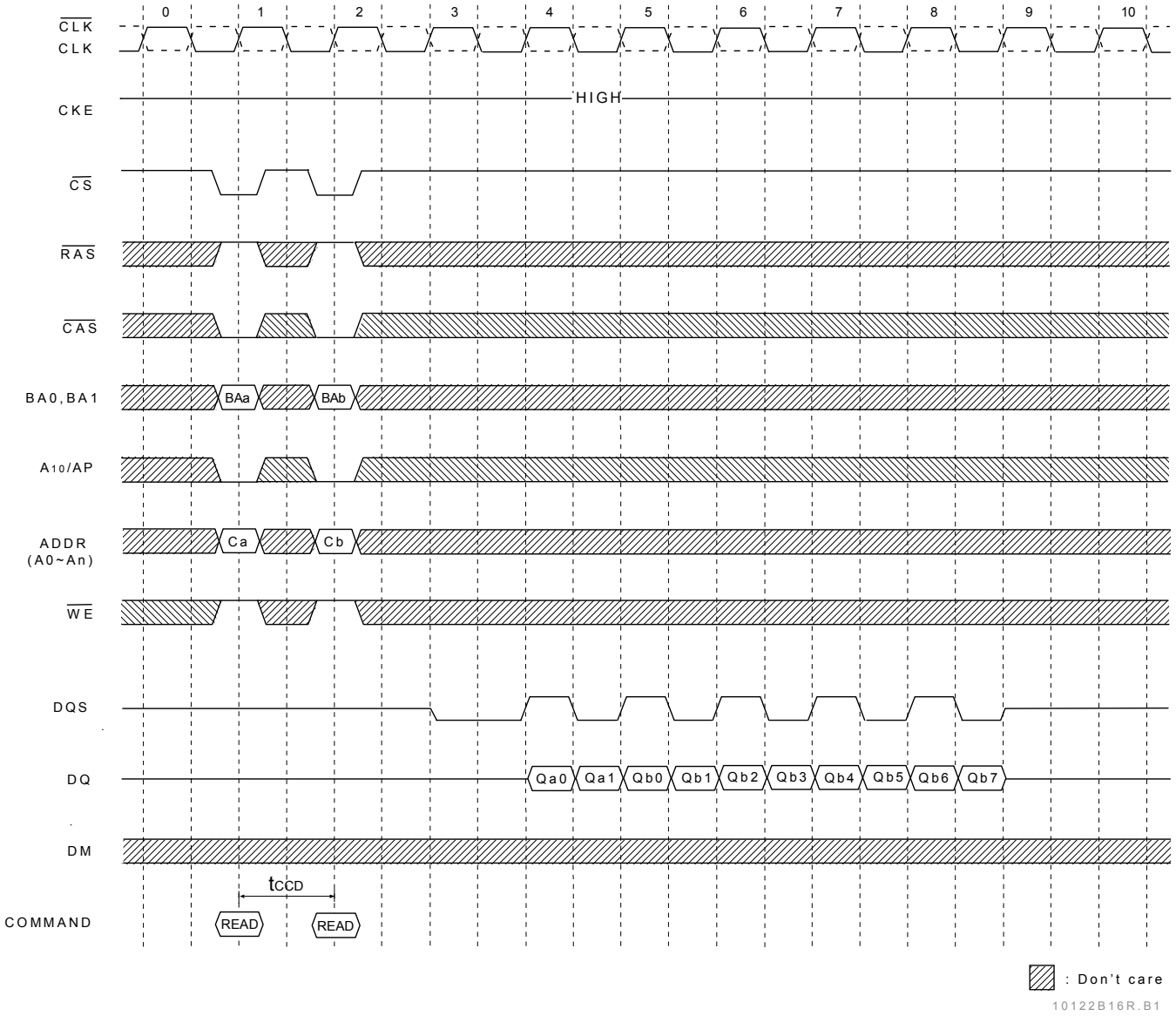
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Read Interrupted by a Write & Burst Terminate (@ BL=8, CL=3)



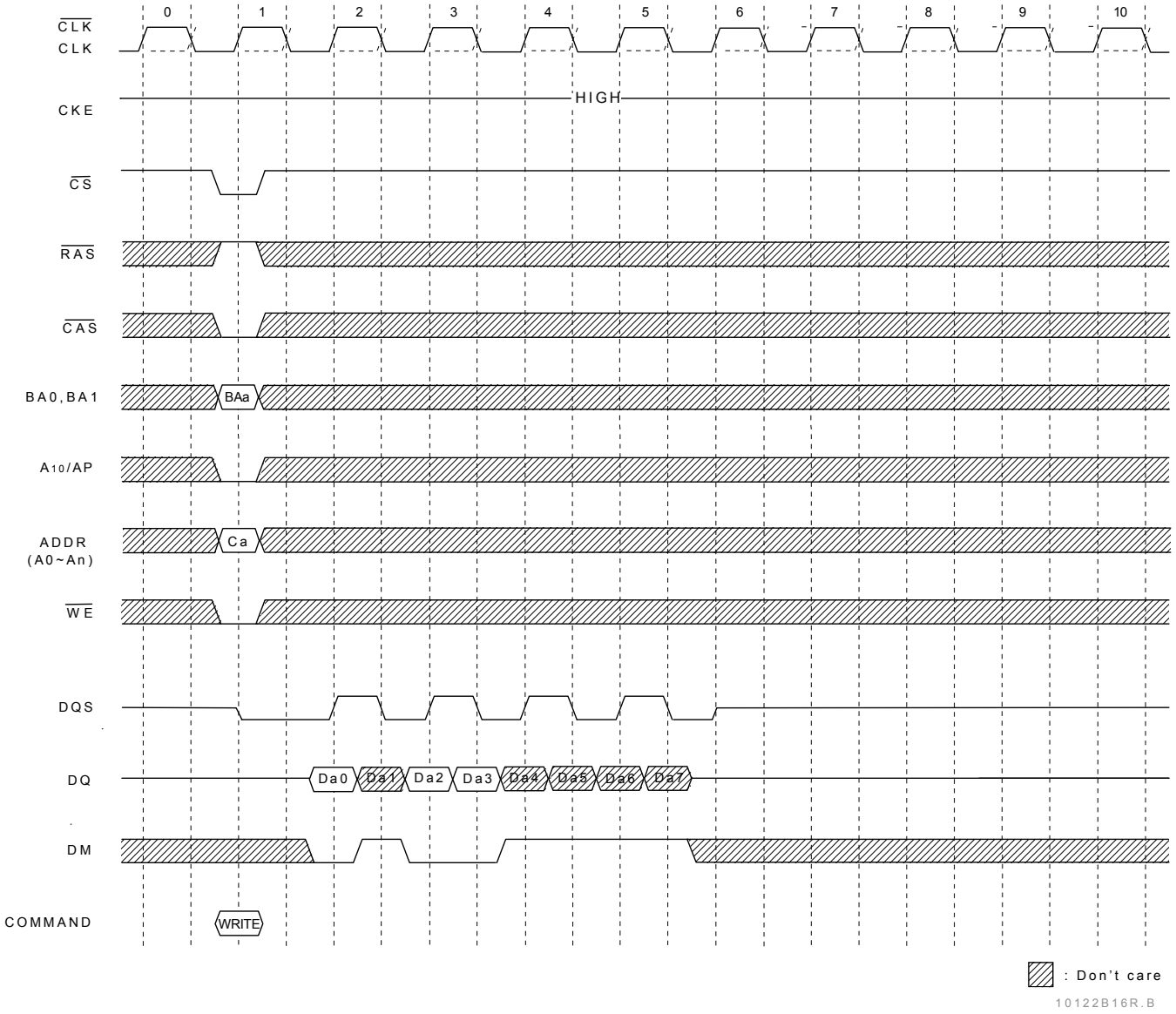
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Read Interrupted by a Read (@ BL=8, CL=3)



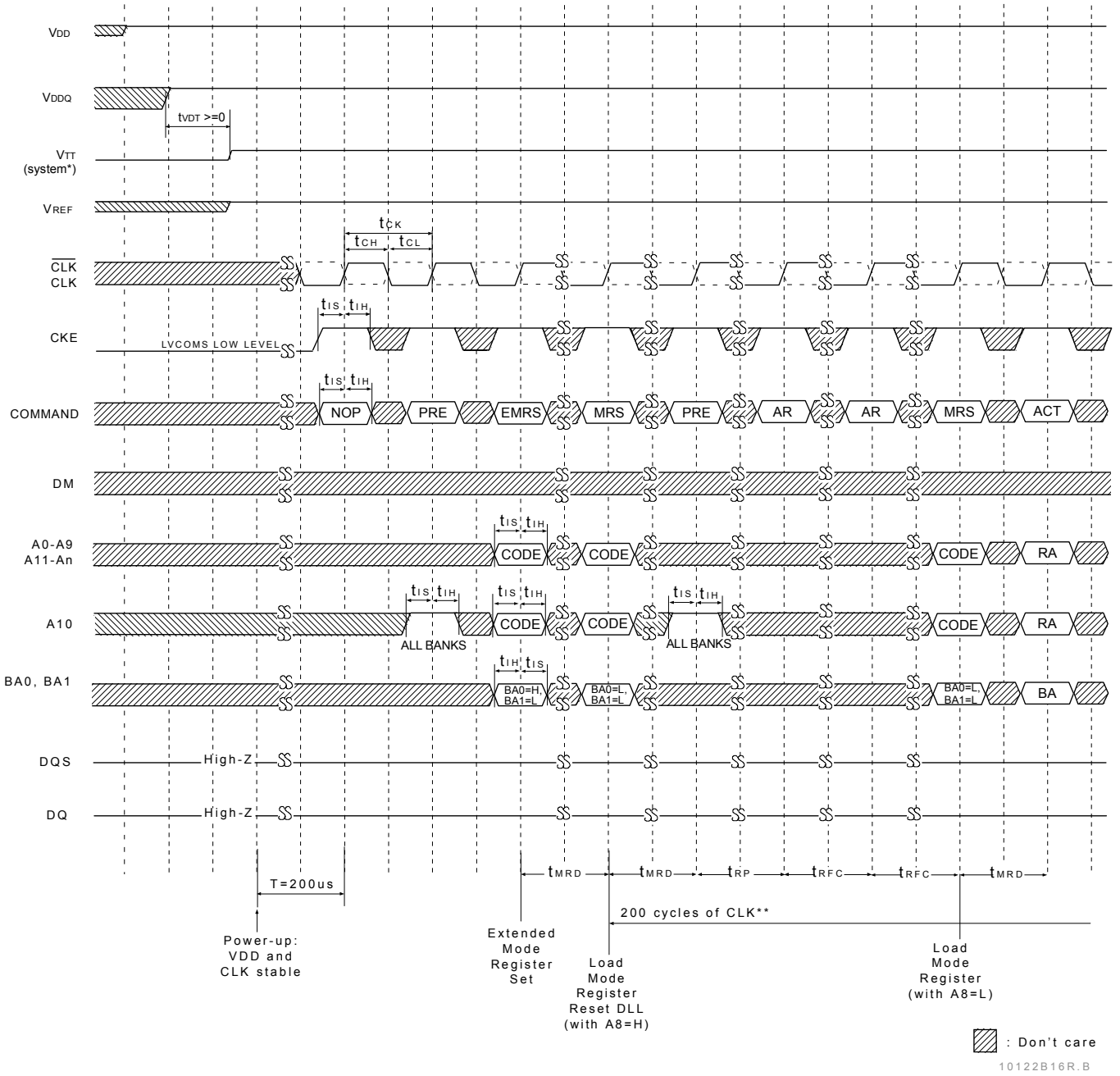
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DM Function (@ BL=8) only for write



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Power up & Initialization Sequence (based on DDR400)



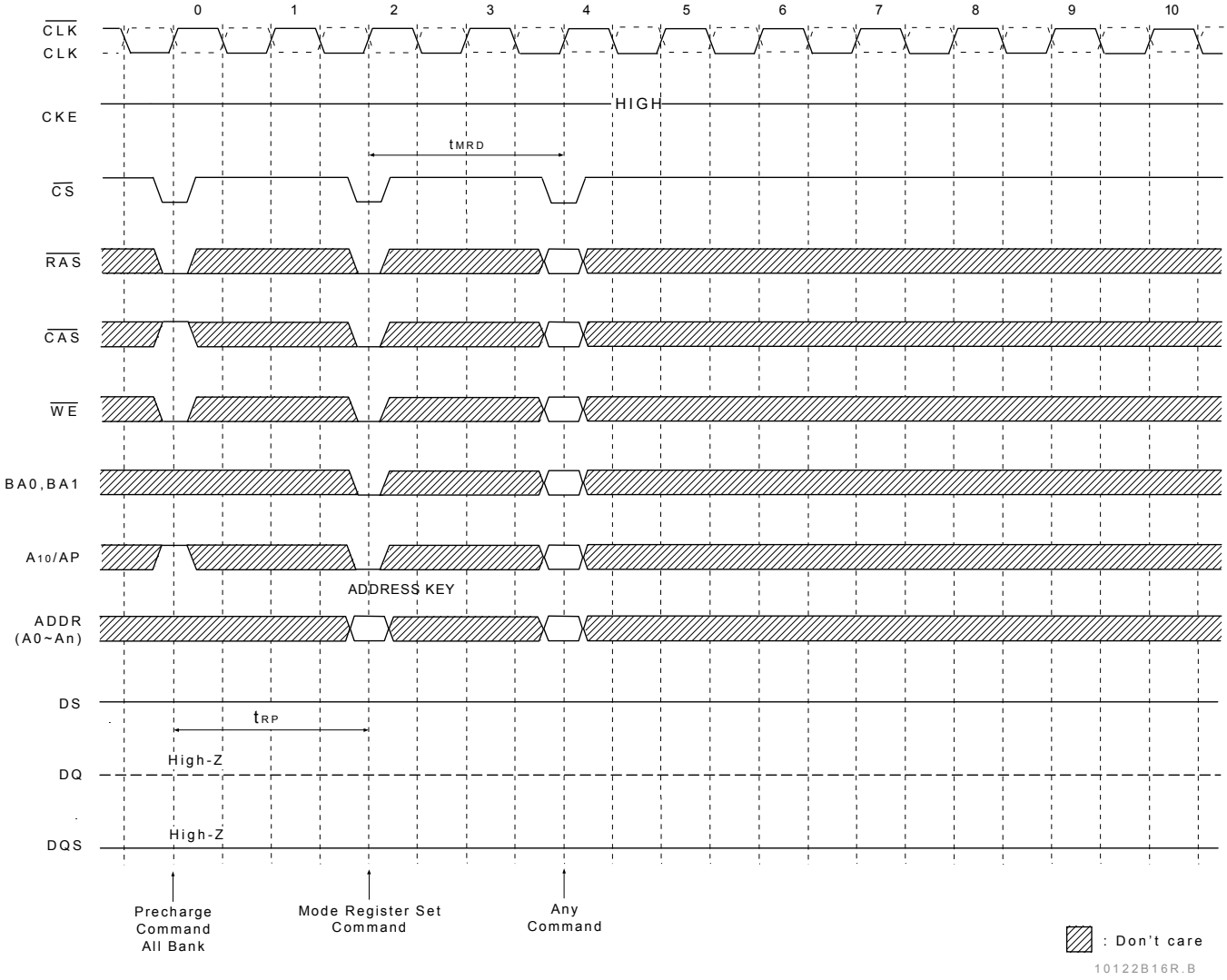
Notes:

* = V_{TT} is not applied directly to the device, however t_{VTD} must be greater than or equal to zero to avoid device latch-up.

** = t_{MRD} is required before any command can be applied, and 200 cycles of CLK are required before an executable command can be applied. The two Auto Refresh commands may be moved to follow the first MRS but precede the second PRECHARGE ALL command.

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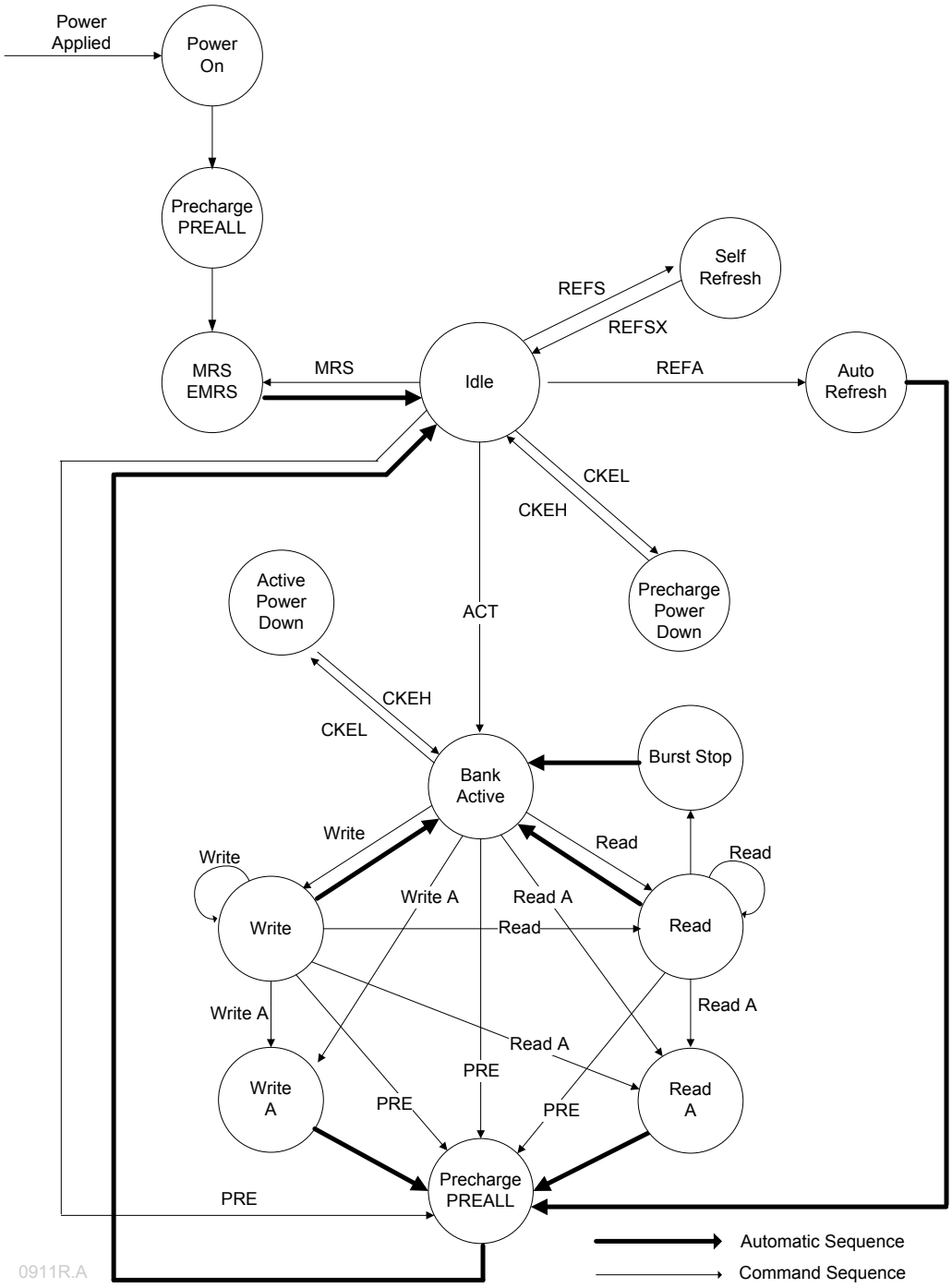
Mode Register Set



Note: Power & Clock must be stable for 200us before precharge all banks.

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Simplified State Diagram



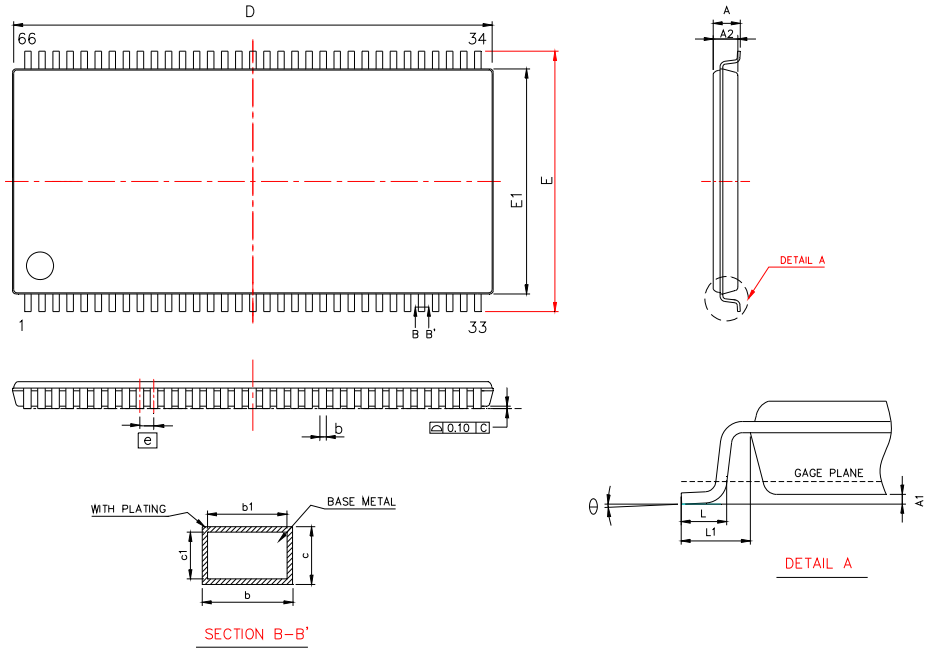
PREALL = Precharge All Banks
MRS = Mode Register Set
EMRS = Extended Mode Register Set
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
REFA = Auto Refresh

CKEL = Enter Power Down
CKEH = Exit Power Down
ACT = Active
Write A = Write with Autoprecharge
Read A = Read with Autoprecharge
PRE = Precharge

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PACKING DIMENSIONS

66-LEAD TSOP(II) DDR DRAM(400mil)

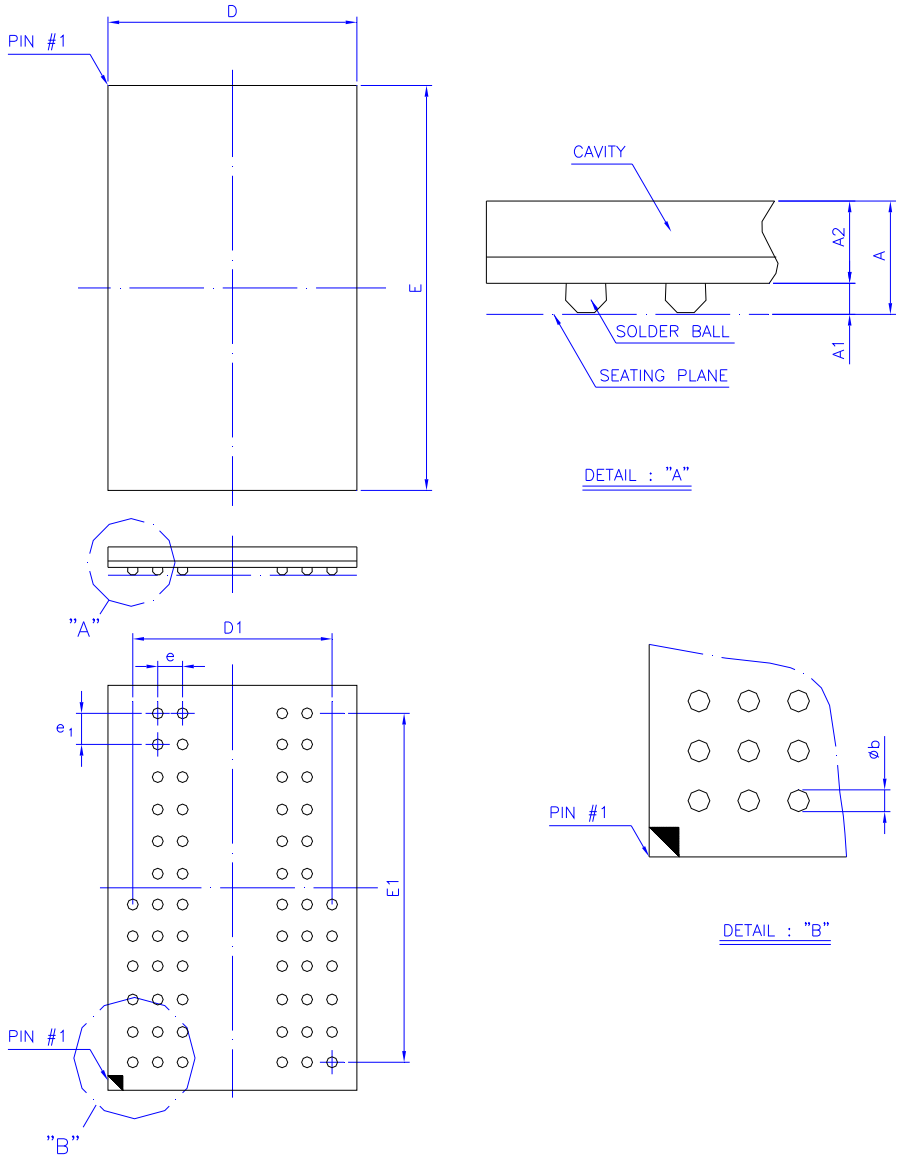


Symbol	Dimension in inch			Dimension in mm		
	Min	Norm	Max	Min	Norm	Max
A			0.047			1.2
A1	0.002	0.004	0.006	0.05	0.1	0.15
A2	0.037	0.039	0.041	0.95	1	1.05
b	0.009		0.015	0.22		0.38
b1	0.009	0.012	0.013	0.22	0.3	0.33
c	0.005		0.008	0.12		0.21
c1	0.0047	0.005	0.006	0.12	0.127	0.16
D	0.875 BSC			22.22 BSC		
ZD	0.028 REF			0.71 REF		
E	0.455	0.463	0.471	11.56	11.76	11.96
E1	0.400 BSC			10.16 BSC		
e	0.026 BSC			0.65 BSC		
L	0.016	0.02	0.024	0.4	0.5	0.6
L1	0.031 REF			0.80 REF		
θ°	0°		8°	0°		8°
θ1°	10°	15°	20°	10°	15°	20°

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PACKING DIMENSIONS

60-BALL DDR SDRAM (8x13 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A			1.00			0.039
A_1	0.20	0.25	0.30	0.008	0.010	0.012
A_2			0.71			0.028
Φ_b	0.30	0.35	0.40	0.012	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
E	12.90	13.00	13.10	0.508	0.512	0.516
D_1		6.40			0.252	
E_1		11.0			0.433	
e		0.80			0.031	
e_1		1.00			0.039	

Controlling dimension : Millimeter.

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Revision History

Revision	Date	Description
0.1	2012.12.26	Original
0.2	2013.11.27	1. Delete CAS Latency: 2 2. Modify the figure of burst write operation
1.0	2014.04.29	1. Delete "Preliminary" 2. Modify Input / Output Capacitance of TSOP package 3. Delete speed grade -4

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