1.8/3.3V 4M-BIT

SERIAL NOR FLASH WITH DUAL SPI

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扫码查规格书

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FEATURES

- **Low power supply operation**
  - Single 1.65V-3.6V supply
- **4M bit Serial Flash**
  - 4 M-bit/512K-byte/2,048 pages
  - 256 bytes per programmable page
  - Uniform 4K-byte Sectors, 32K/64K-byte Blocks
- **New Family of SpiFlash Memories**
  - Standard SPI: CLK, CS#, DI, DO, WP#
  - Dual SPI: CLK, CS#, DI, DO, WP#
  - Auto-increment Read capability
- **Temperature Ranges**
  - Industrial (-40°C to 85°C)
  - Industrial (-40°C to 105°C)
  - Industrial (-40°C to 125°C)
- **Low power consumption**
  - 0.5/1 uA typical standby current
  - 0.5/1 uA typical power down current
- **Flexible Architecture with 4KB sectors**
  - Sector Erase (4K-bytes)
  - Block Erase (32K/64K-bytes)
  - Page Program up to 256 bytes
  - More than 100K erase/program cycles
  - More than 20-year data retention
- **Advanced Security Feature**
  - Software and Hardware Write-Protect
  - 128-Bit Unique ID for each device
- **High performance program/erase speed**
  - Page program time: 1.2ms typical
  - Sector erase time: 75ms typical
  - Block erase time: 0.35s typical
  - Chip erase time: 2.3s typical
- **Package Options**
  - SOP8 - 150mil/208mil
  - TFBGA24
  - TSSOP8 - 173mil
  - DFN8 (1.5*1.5*0.45mm)
  - DFN8 (2*3*0.55mm)
  - All Pb-free packages are RoHS compliant

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GENERAL DESCRIPTION

The HT25WD40A of non-volatile flash memory device supports the standard Serial Peripheral Interface (SPI). Traditional SPI single bit serial input and output (Single I/O or SIO) is supported as well as optional two bit (Dual I/O or DIO) serial protocols. This multiple width interface is called SPI Multi-I/O or MIO.

The SPI protocols use only 4 signals:

◆ Chip Select (CS#)

◆ Serial Clock (CLK)

◆ Serial Data

- IO0 (DI)
- O1 (DO)

The HT25WD40A support the standard Serial Peripheral Interface (SPI) and Dual Output SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), O1 (DO). SPI clock frequencies of up to 100MHz are supported allowing equivalent clock rates of 200MHz (100MHz x 2) for Dual Output when using the Fast Read Dual Output. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories.

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1. BLOCK DIAGRAM

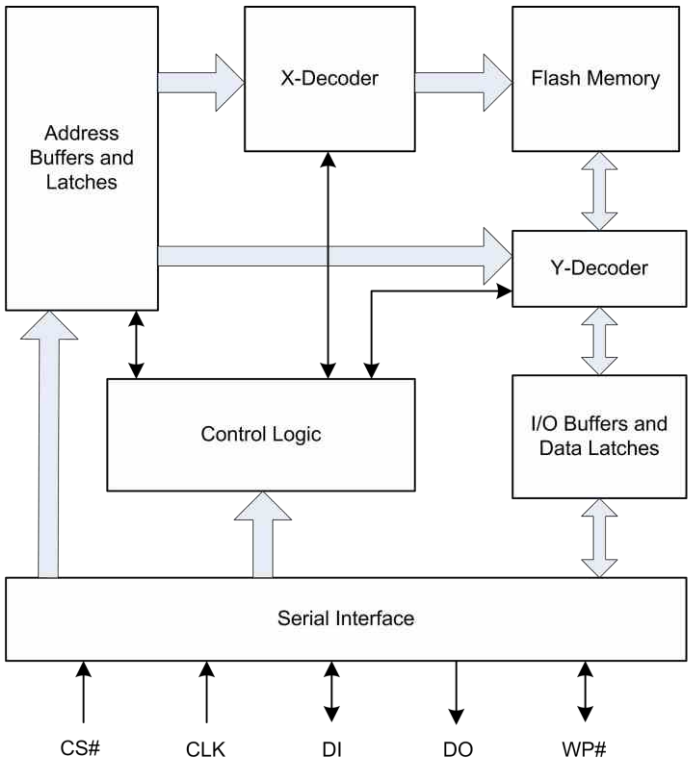


Figure 2.1 Block Diagram

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2. CONNECTION DIAGRAMS

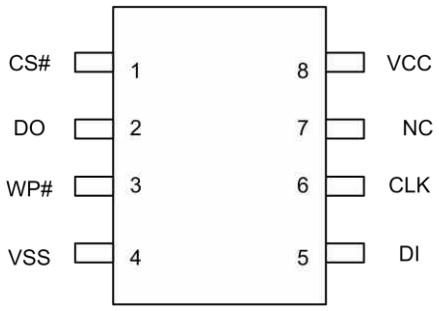


Figure 3.1 SOP8 (150/208mil)/ DIP8 (300mil)

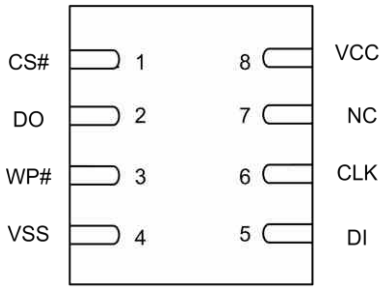


Figure 3.2 DFN8

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3. SIGNAL DESCRIPTIONS

Table 4.1 Pin Descriptions

Symbol	Pin Name
CLK	Serial Clock Input
DI(IO0)	Serial Data Input(Data input output 0) (1)
DO(O1)	Serial Data Output(Data output 1) (1)
CS#	Chip Enable
WP#	Write Protect
NC	No Connection
V_{CC}	Power Supply (1.65-3.6V)
V_{SS}	Ground

Notes:
(1) IO0 and O1 are used for Standard and Dual SPI instructions.

4.1. Serial Data Input (DI) / IO0

The SPI Serial Data Input (DI) pin is used to transfer data serially into the device. It receives instructions, address and data to be programmed. Data is latched on the rising edge of the Serial Clock (CLK) input pin. The DI pin becomes IO0 - an input and output during Dual commands for receiving instructions, address, and data to be programmed (values latched on rising edge of serial CLK clock signal) as well as shifting out data (on the falling edge of CLK).

4.2. Serial Data Output (DO) / O1

The SPI Serial Data Output (DO) pin is used to transfer data serially out of the device. Data is shifted out on the falling edge of the Serial Clock (CLK) input pin. DO becomes O1 - an output during Dual commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial CLK clock signal) as well as shifting out data (on the falling edge of CLK).

4.3. Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Mode")

4.4. Chip Select (CS#)

The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high the device is deselected and the Serial Data Output pins are at high impedance.

When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When CS# is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

4.5. Write Protect (WP#)

The Write Protect (WP#) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (BP0, BP1 and BP2) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected.

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4. MEMORY ORGANIZATION

5.1. Flash Memory Array

The HT25WD40A memory is organized as:
- 524,288bytes
- Uniform Sector Architecture 8 blocks of 64-Kbyte
- 128 sectors of 4-Kbyte
- 2, 048 pages (256 bytes each)

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector, Block or Chip Erasable but not Page Erasable.

Table 5.1(1) Memory Organization(HT25WD40A)

Block	Sector	Address range	
Block 7	127	07F000H	07FFFFH
	.....	.....	.....
	112	070000H	070FFFH
Block 6	111	06F000H	06FFFFH
	.....	.....	.....
	96	060000H	060FFFH
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
Block 2	47	02F000H	02FFFFH
	.....	.....	.....
	32	020000H	020FFFH
Block 1	31	01F000H	01FFFFH
	.....	.....	.....
	16	010000H	010FFFH
Block 0	15	00F000H	00FFFFH
	.....	.....	.....
	0	000000H	000FFFH

Notes:
(1) These are condensed tables that use a couple of sectors as references. There are address ranges that are not explicitly listed. All 4-kB sectors have the pattern XXX000h-XXXFFFh.

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5. FUNCTION DESCRIPTION

6.1 SPI Operations

6.1.1 SPI Modes

The HT25WD40A can be driven by an embedded microcontroller (bus master) in either of the two following clocking modes.

◆**Mode 0** with Clock Polarity (CPOL) = 0 and, Clock Phase (CPHA) = 0

◆**Mode 3** with CPOL = 1 and, CPHA = 1

For these two modes, input data is always latched in on the rising edge of the CLK signal and the output data is always available on the falling edge of the CLK clock signal.

The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring any data.

◆CLK will stay at logic low state with CPOL = 0, CPHA = 0

◆CLK will stay at logic high state with CPOL = 1, CPHA = 1

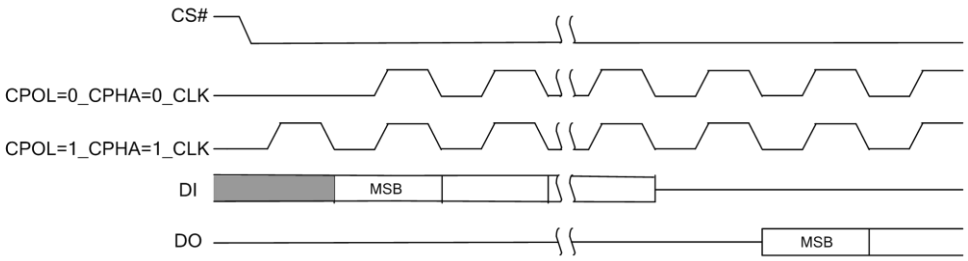


Figure 6.1 SPI Modes

Timing diagrams throughout the rest of the document are generally shown as both mode 0 and 3 by showing CLK as both high and low at the fall of CS#. In some cases a timing diagram may show only mode 0 with CLK low at the fall of CS#. In such case, mode 3 timing simply means clock is high at the fall of CS# so no CLK rising edge set up or hold time to the falling edge of CS# is needed for mode 3.

CLK cycles are measured (counted) from one falling edge of CLK to the next falling edge of CLK. In mode 0 the beginning of the first CLK cycle in a command is measured from the falling edge of CS# to the first falling edge of CLK because CLK is already low at the beginning of a command.

6.1.2 Dual SPI Modes

The HT25WD40A supports Dual SPI Operation when using the Fast Read Dual Output (3Bh) instruction. These features allow data to be transferred from the device at twice the rate possible with the standard SPI. These instructions are ideal for quickly downloading code to RAM upon Power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI commands, the DI and DO pins become bidirectional I/O pins: IO0 and O1.

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6.2. Status Register

The Read and Write Status Registers commands can be used to provide status and control of the flash memory device.

Status Register (SR) can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection.

SR contain non-volatile bits in locations SR[7:2] that control sector protection, Status Register Protection. Bits located in SR[1], and SR[0] are read only volatile bits for write enable, and busy status. These are updated by the memory control logic. The SR[1] write enable bit is set only by the Write Enable (06h) command and cleared by the memory control logic when an embedded operation is completed.

Write access to the non-volatile Status Register bits is controlled by the state of the non-volatile Status Register Protect bits SR[7] (SRP), the Write Enable command (06h) preceding a Write Status Registers command, the WP# pin.

Table 6.1 Status Register (SR)

Bits	Field	Function	Type	Default State	Description
7	SRP	Status Register Protect	Non-volatile	0	0 = WP# input has no effect or Power Supply Lock Down mode 1 = WP# input can protect the Status Register
6	Reserved			0	
5	Reserved			0	
4	BP2	Block Protect Bits	Non-volatile	0	000b = No protection
3	BP1			0	
2	BP0			0	
1	WEL	Write Enable Latch	Read only	0	0 = Not Write Enabled, no embedded operation can start 1 = Write Enabled, embedded operation can start
0	BUSY	Embedded Operation Status	Read only	0	0 = Not Busy, no embedded operation in progress 1 = Busy, embedded operation in progress

6.2.1 BUSY

BUSY is a read only bit in the status register (SR[0]) which is set to a “1” state when the device is executing a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction. During this time the device will ignore further instructions except for the Read Status Register instruction (see t_W, t_{PP}, t_{SE}, t_{BE}, and t_{CE} in AC Characteristics). When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a “0” state indicating the device is ready for further instructions.

6.2.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (SR[1]) which is set to a 1 after executing a Write Enable Instruction. The WEL status bit is cleared to a 0 when the device is written disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register.

6.2.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read / write bits in the Status Register (SR[4:2]) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Registers Command (see t_W in Section 8.5). All, none or a portion of the memory array can be protected from Program

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and Erase commands (see Section 6.3.2, Block Protection Maps). The factory default setting for the Block Protection Bits is 0 (none of the array is protected.)

6.2.4 The Status Register Protect (SRP)

The Status Register Protect (SRP) bit operates in conjunction with the Write Protect (WP#) signal. The Status Register Write Protect (SRP) bit and Write Protect (WP#) signal set the device to the Hardware Protected mode. When the Status Register Protect (SRP) bit is set to 1, and Write Protect (WP#) is driven Low. In this mode, the non-volatile bits of the Status Register(SRP, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is not execution. The default value of SRP is 0.

Notes:
1. Busy and WEL(SR1[1:0]) are volatile read only status bits that are never affected by the Write Status Registers command.
2. The non-volatile version of SRP and BP2-BP0 (SR1[7] and SR1[4:2]) bits are not writable when protected by the SRP bits and WP# as shown in the table. The non-volatile version of these Status Register bits is selected for writing when the Write Enable (06h) command precedes the Write Status Registers (01h) command.

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6.3. Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern the HT25WD40A provides the following data protection mechanisms:

6.3.1 Write Protect Features

◆ Device resets when V_{CC} is below threshold

◆ Time delay write disable after Power-Up

◆ Write enable / disable commands and automatic write disable after erase or program

◆ Command length protection

- All commands that Write, Program or Erase must complete on a byte boundary (CS# driven high after a full 8 bits have been clocked) otherwise the command will be ignored.

◆ Software and Hardware write protection using Status Register control

- WP# input protection
- Lock Down write protection until next power-up or Software Reset

◆ Write Protection using the Deep Power-Down command

Upon power-up or at power-down, the HT25WD40A will maintain a reset condition while V_{CC} is below the threshold value of VWI, (see Figure 8.1). While reset, all operations are disabled and no commands are recognized. During power-up and after the V_{CC} voltage exceeds VWI, all program and erase related commands are further disabled for a time delay of tPUW. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Registers commands. Note that the chip select pin (CS#) must track the V_{CC} supply level at power-up until the V_{CC}-min level and tVSL time delay is reached. If needed a pull-up resistor on CS# can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable command must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Registers command will be accepted. After completing a program, erase or write command the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled main flash array write protection is facilitated using the Write Status Registers command to write the Status Register (SR) and Block Protect (BP2, BP1 and BP0) bits.

The BP method allows a portion as small as 4-kB sector or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (WP#) pin, changes to the Status Register can be enabled or disabled under hardware control. See the Table 6.2 for further information.

Additionally, the Deep Power-Down (DPD) command offers an alternative means of data protection as all commands are ignored during the DPD state, except for the Release from Deep-Power-Down (RES ABh) command. Thus, preventing any program or erase during the DPD state.

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6.3.2 Block Protection Maps

Table 6.2 HT25WD40A Block Protection

Status Register			HT25WD40A(4 Mbit) Block Protection			
BP2	BP1	BP0	Protected Block(s)	Protected Addresses	Protected Density	Protected Portion
0	0	0	None	None	None	None
0	0	1	0 thru 7	000000h – 07DFFFh	504 kB	Lower 63/64
0	1	0	0 thru 7	000000h – 07BFFFh	496 kB	Lower 31/32
0	1	1	0 thru 7	000000h – 077FFFh	480 kB	Lower 15/16
1	0	0	0 thru 6	000000h – 06FFFFh	448 kB	Lower 7/8
1	0	1	0 thru 5	000000h – 05FFFFh	384 kB	Lower 3/4
1	1	0	0 thru 3	000000h – 03FFFFh	256 kB	Lower 1/2
1	1	1	0 thru 7	000000h – 07FFFFh	512 kB	All

Notes:
1. X = don't care.

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6.4. Page Program

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration t_{PP}). To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0), provided that they lie in consecutive addresses on the same page of memory.

6.5. Sector Erase, Block Erase and Chip Erase

The Page Program (PP) instruction allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to be erased to all 1s (FFh). This can be achieved a sector at a time, using the Sector Erase (SE) instruction, a block at a time using the Block Erase (BE) instruction or throughout the entire memory, using the Chip Erase (CE) instruction. This starts an internal Erase cycle (of duration t_{SE} t_{BE} or t_{CE}). The Erase instruction must be preceded by a Write Enable (WREN) instruction.

6.6. Polling during a Write, Program or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program (PP) or Erase (SE, BE or CE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{SE}, t_{BE} or t_{CE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

6.7. Active Power, Stand-by Power and Deep Power-Down Modes

When Chip Select (CS#) is Low, the device is enabled, and in the Active Power mode. When Chip Select (CS#) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write Status Register). The device then goes into the Standby Power mode. The device consumption drops to ICC1.

The Deep Power-down mode is entered when the specific instruction (the Enter Deep Power-down Mode (DP) instruction) is executed. The device consumption drops further to ICC2. The device remains in this mode until another specific instruction (the Release from Deep Power-down Mode and Read Device ID (RDI) instruction) is executed.

All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Program or Erase instructions.

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7. INSTRUCTIONS

The instruction set of the HT25WD40A consists of several basic instructions that are fully controlled through the SPI bus. Instructions are initiated with the falling edge of Chip Select (CS#). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge CS#. Clock relative timing diagrams for each instruction are included in figures 7.1 through 7.17. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle completes.

Table 7.1 Command Set (Configuration, Status, Erase, Program Instructions (1), SPI Mode)

Command Name	BYTE 1 (Instruction)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Read Status Register	05h	SR[7:0](2)				
Write Enable	06h					
Write Disable	04h					
Write Status Registers	01h	SR[7:0]				
Page Program	02h	A23—A16	A15—A8	A7—A0	D7—D0	
Sector Erase (4 KB)	20h	A23—A16	A15—A8	A7—A0		
Block Erase (32 KB)	52h	A23—A16	A15—A8	A7—A0		
Block Erase (64 KB)	D8h	A23—A16	A15—A8	A7—A0		
Chip Erase	C7h/60h					
Read Unique ID Number	4Bh	A23—A16	A15—A8	A7—A0	dummy	(ID127—ID0)

Notes:
1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "()" indicate data being read from the device on the DO pin.
2. Status Register contents will repeat continuously until CS# terminates the command.

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Table 7.2 Command Set (Read Instructions [1])

Command Name	BYTE 1 (Instruction)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Read Data	03h	A23—A16	A15—A8	A7—A0	(D7—D0,…)	
Fast Read	0Bh	A23—A16	A15—A8	A7—A0	dummy	(D7—D0,…)
Fast Read Dual Output	3Bh	A23—A16	A15—A8	A7—A0	dummy	(D7—D0,…)[1]

Notes:
1. Dual Output data
   IO0 = (D6, D4, D2, D0)
   O1 = (D7, D5, D3, D1)

Table 7.3 Command Set (Read ID, SPI Mode)

Command Name	BYTE 1 (Instruction)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Deep Power-down	B9h					
Release Power down / Device ID	ABh	dummy	dummy	dummy	Device ID[1]	
Manufacturer/ Device ID[2]	90h	dummy	dummy	00h	Manufacturer	Device ID
JEDEC ID	9Fh	Manufacturer	Memory Type	Capacity		

Notes:
1. The Device ID will repeat continuously until CS# terminates the command.
2. Legacy Device Identification Commands on page 24 for Device ID information. The 90h instruction is followed by an address. Address = 0 selects Manufacturer ID as the first returned data as shown in the table. Address = 1 selects Device ID as the first returned data followed by Manufacturer ID.

Table 7.4[1] Manufacturer and Device Identification(HT25WD40A)

OP Code	Data1	Data2	Data3
ABh	Device ID = 12h	-	-
90h	Manufacturer ID = 5E	Device ID = 12h	-
9Fh	Manufacturer ID = 5E	Memory Type =32h	Capacity = 13h

Notes:
(1) Please contact sales for more information

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7.1 Configuration and Status Commands

7.1.1 Read Status Register (05h)

The Read Status Register commands allow the 8-bit Status Registers to be read. The command is entered by driving CS# low and shifting the instruction code “05h” for Status Register into the DI pin on the rising edge of CLK. The Status Register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7.1. The Status Register bits are shown in Section 6.2, Status Registers.

The Read Status Register (05h) command may be used at any time, even during a Program, Erase, or Write Status Registers cycle. This allows the BUSY status bit to be checked to determine when the operation is complete and if the device can accept another command.

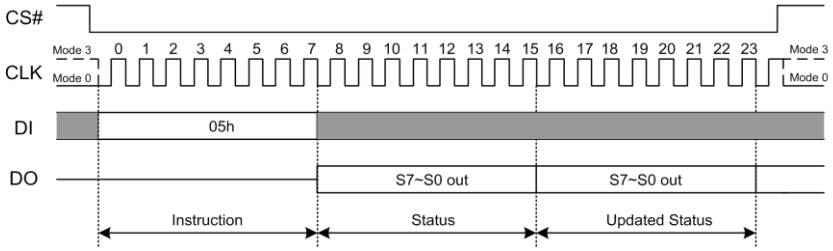


Figure 7.1 Read Status Register Instruction

7.1.2 Write Enable (06h)

The Write Enable instruction (Figure 7.2) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register instruction. The Write Enable instruction is entered by driving CS# low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

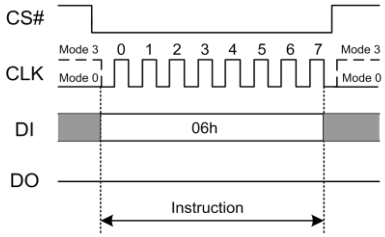


Figure 7.2 Write Enable Instruction

7.1.3 Write Disable (04h)

The Write Disable instruction (Figure 7.3) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving CS# low, shifting the instruction code “04h” into the DI pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase instructions.

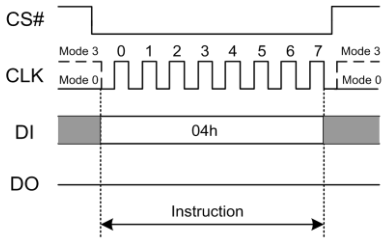


Figure 7.3 Write Disable Instruction

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7.1.4 Write Status Register (01h)

The Write Status Registers command allows the Status Registers to be written. Only non-volatile Status Register bits SRP, BP2, BP1, BP0 (SR[7], SR[4:2]) can be written. All other Status Register bit locations are read-only and will not be affected by the Write Status Registers command. The Status Register bits are shown in Section 6.2, Status Registers. Any reserved bits should only be written to their default value.

To write non-volatile Status Register bits, a standard Write Enable (06h) command must previously have been executed for the device to accept the Write Status Registers Command (Status Register bit WEL must equal 1). Once write enabled, the command is entered by driving CS# low, sending the instruction code “01h”, and then writing the Status Register data bytes as illustrated in Figure 7.4.

To complete the Write Status Registers command, the CS# pin must be driven high after the eighth bit of a data value is clocked in (CS# must be driven high on an 8-bit boundary). If this is not done the Write Status Registers command will not be executed.

The Write Status Register instruction allows the Status Register to be written. A Write Enable instruction must previously have been executed for the device to accept the Write Status Register Instruction (Status Register bit WEL must equal to 1). Once write enabled, the instruction is entered by driving CS# low, sending the instruction code “01h”, and then writing the status register data byte as illustrated in Figure 7.4.

During non-volatile Status Register write operation (06h combined with 01h), after CS# is driven high, the self-timed Write Status Register cycle will commence for a time duration of t_W (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

If CS# is driven high after the eighth clock, the Write Status Register (01h) instruction will only program the Status Register.

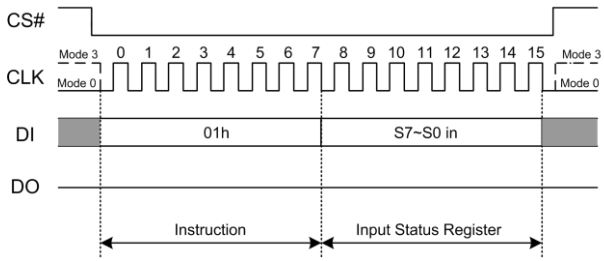


Figure 7.4 Write Status Register Instruction

7.2 Program and Erase Commands

7.2.1 Page Program (PP) (02h)

The Page Program instruction allows up to 256 bytes of data to be programmed at previously erased to all 1s (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 7.5.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more

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than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After CS# is driven high, the self-timed Page Program instruction will commence for a time duration of t_{pp} (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

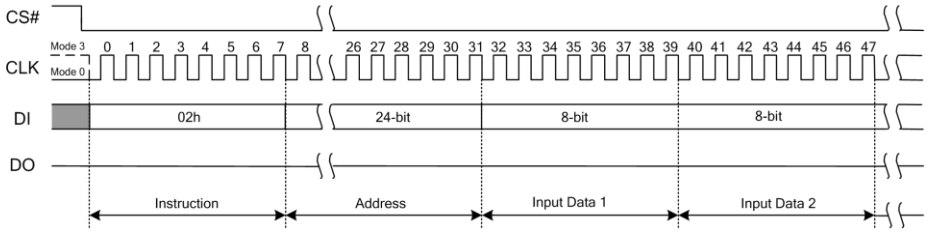


Figure 7.5 Page Program Instruction

7.2.2 Sector Erase (SE) (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0). The Sector Erase instruction sequence is shown in Figure 7.6.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After CS# is driven high, the self-timed Sector Erase instruction will commence for a time duration of t_{SE} (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

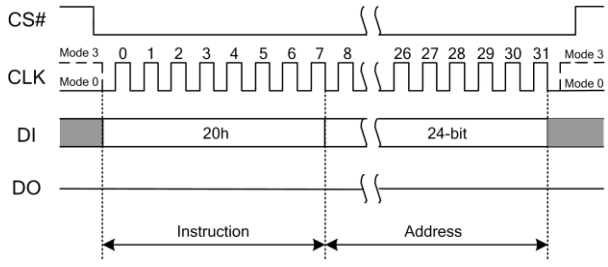


Figure 7.6 Sector Erase Instruction

7.2.3 Block Erase (BE) (D8h) and Half Block Erase (52h)

The Block Erase instruction sets all memory within a specified block (64K-bytes) or half block (32K- bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “D8h” or “52h” followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in Figure 7.7.

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The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After CS# is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

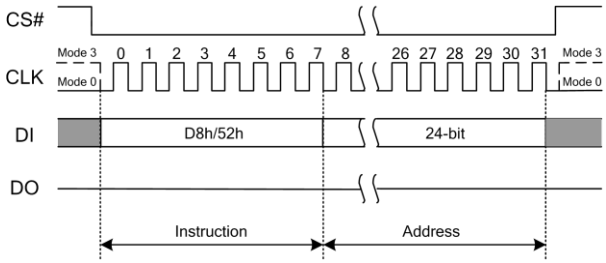


Figure 7.7 Block Erase Instruction

7.2.4 Chip Erase (CE) (C7h or 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 7.8.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After CS# is driven high, the self-timed Chip Erase instruction will commence for a time duration of t_{CE} (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

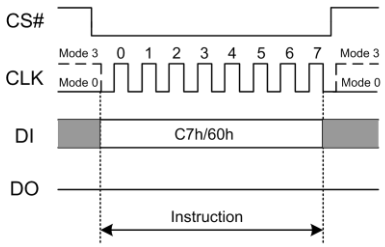


Figure 7.8 Chip Erase Instruction

7.3 Read Commands

7.3.1 Read Data (03h)

The Read Data instruction allows one more data bytes to be sequentially read from the memory. The instruction is initiated by driving the CS# pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving CS# high.

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The Read Data instruction sequence is shown in Figure 7.9. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics).

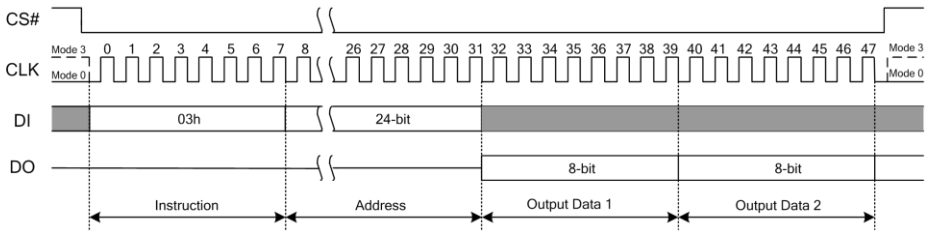


Figure 7.9 Read Data Instruction

7.3.2 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 7.10. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DI pin is a “don’t care”.

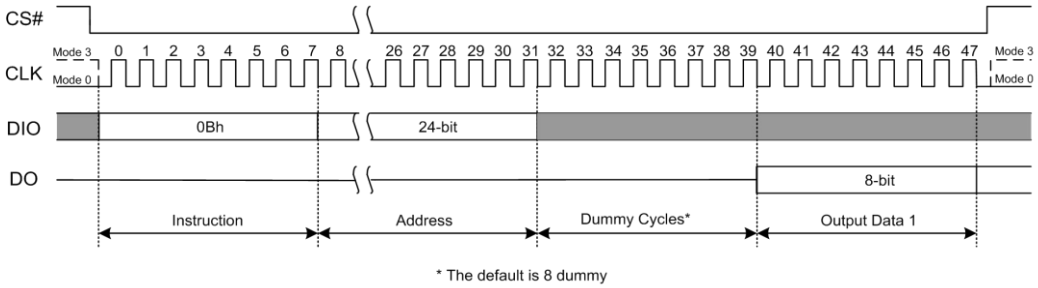


Figure 7.10 Fast Read Instruction

7.3.3 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins, DO and DI, instead of just DO. This allows data to be transferred from the HT25WD40A at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 7.11. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the DI pin should be high-impedance prior to the falling edge of the first data out clock.

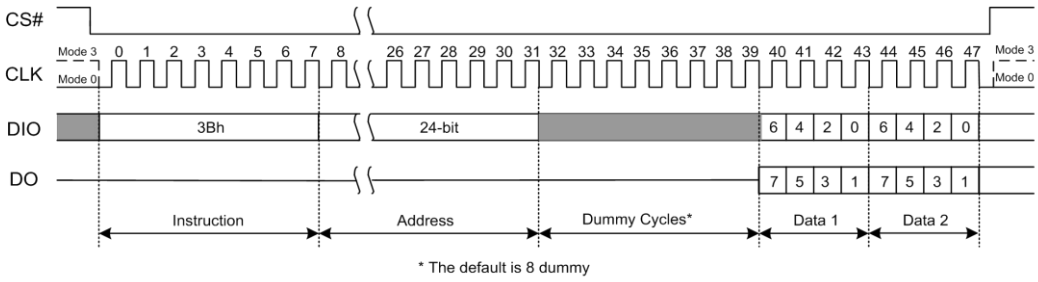


Figure 7.11 Fast Read Dual Output Instruction Sequence Diagram

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7.4 ID and Security Commands

7.4.1 Deep Power-down (DP) (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power- down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the CS# pin low and shifting the instruction code “B9h” as shown in Figure 7.12.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done, the Power-down instruction will not be executed. After CS# is driven high, the power-down state will enter within the time duration of t_{DP} (See AC Characteristics). While in the power-down state only the Release from Power-down / Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

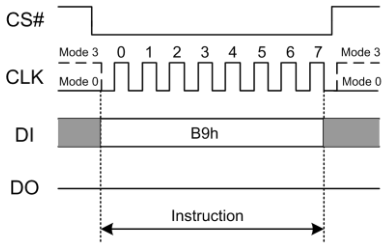


Figure 7.12 Deep Power-down Instruction

7.4.2 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, obtain the devices electronic identification (ID) number or both.

To release the device from the power-down state, the instruction is issued by driving the CS# pin low, shifting the instruction code “ABh” and driving CS# high as shown in Figure 7.13. After the time duration of t_{RES1} (See AC Characteristics) the device will resume normal operation and other instructions will be accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID during the non-power-down state, the instruction is initiated by driving the CS# pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits will then be shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7.14. The Device ID value for the HT25WD40A is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving CS# high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in Figure 7.14, except that after CS# is driven high it must remain high for a time duration of t_{RES2} (See AC Characteristics). After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from Power-down / Device ID instruction is issued within Erase, Program or Write cycle (when BUSY equals 1), the instruction is ignored and will not have any effects on the current cycle.

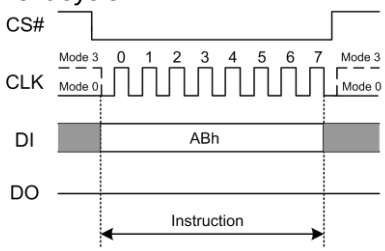


Figure 7.13 Release Power-down Instruction

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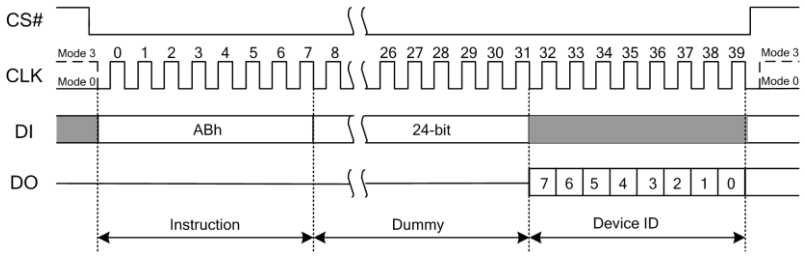


Figure 7.14 Release Power-down / Device ID

7.4.3 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7.15. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The command is completed by driving CS# high.

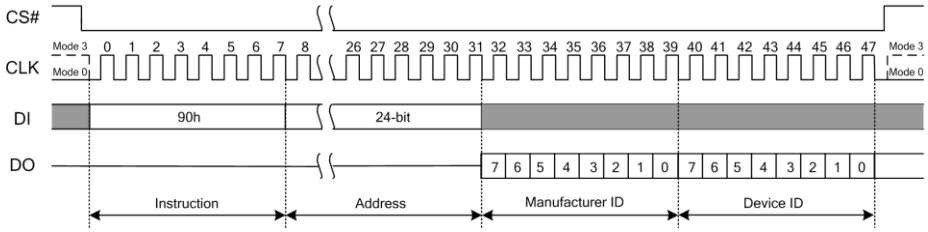


Figure 7.15 Read Manufacturer/Device ID

7.4.4 Read Identification (RDID) (9Fh)

For compatibility reasons, the HT25WD40A provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003.

The instruction is initiated by driving the CS# pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7.16. For memory type and capacity values, refer to Manufacturer and Device Identification table.

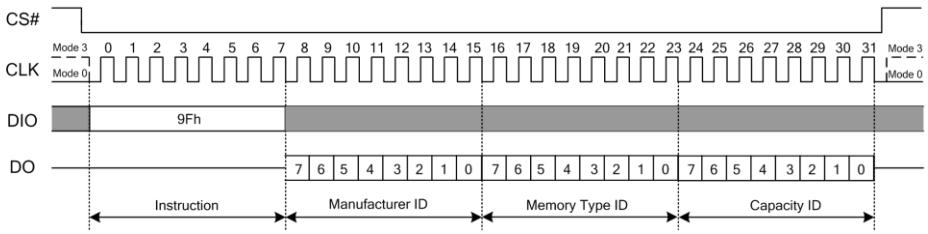


Figure 7.16 Read JEDEC ID

7.4.5 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 128-bit number which is unique

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to each HT25WD40A device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the CS# pin low and shifting the instruction code "4Bh" followed by a 24-bit address(A23-A0) of 000000h and one byte dummy clock. After that, the 128-bit ID is shifted out on the falling edge of CLK as shown in Figure 7.17.

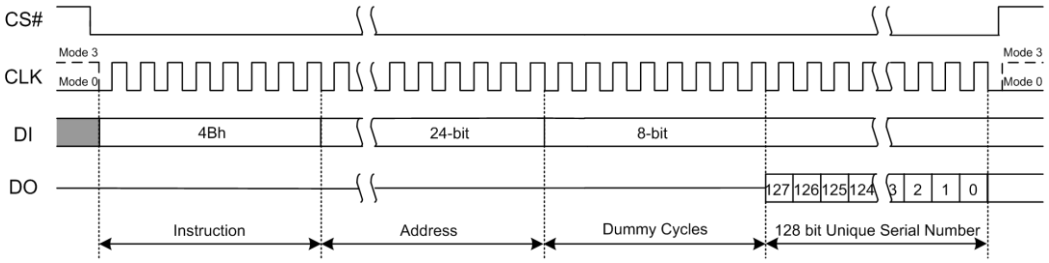


Figure 7.17 Read unique ID Number Instruction

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8. ELECTRICAL CHARACTERISTIC

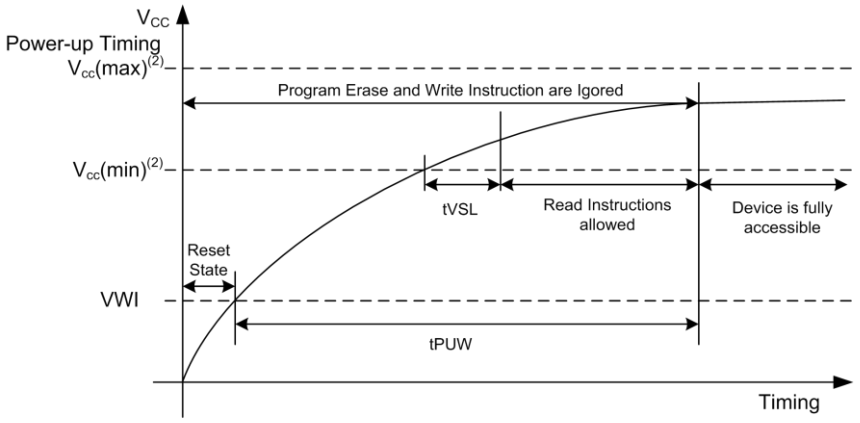


Figure 8.1 Power-up Timing

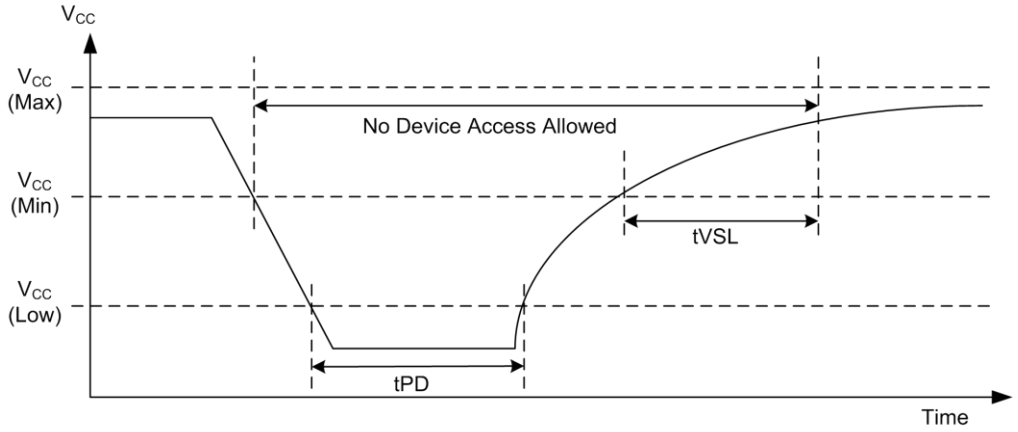


Figure 8.2 Power-Down and Voltage Drop

Table 8.1 Power-up and power-down Timing

PARAMETER	SYMBOL	TYPE		UNIT
		MIN	MAX	
Vcc(minimum operation voltage)	Vcc(min)	1.65	-	V
Vcc(low voltage for initialization to occur)	Vcc(low)	-	0.5	V
Vcc (min) to CS# Low	tVSL(1)	0.3	-	ms
Time Delay Before Write Instruction	tPUW(1)	1	10	ms
The minimum duration for ensuring initialization will occur	tPD	300	-	μs
Write Inhibit Threshold Voltage	VWI(1)	1	1.5	V

Notes:
(1) The parameters are characterized only.
(2) V_{CC} (max.) is 3.6V and V_{CC} (min.) is 1.65V.

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8.1. Absolute Maximum Ratings

Stresses above the values mentioned as following may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values.

Table 8.2(1) Absolute Maximum Rating

PARAMETERS(2)	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	V_{CC}		-0.6 to +4.2	V
Voltage applied on any pin	V_{IO}	Relative to Ground	-0.6 to VCC+0.4	V
Transient Voltage on any Pin	V_{IOT}	<20ns Transient Relative to Ground	-2.0 to VCC+2.0	V
Storage Temperature	T_{STG}		-65 to +150	℃
Lead Temperature	T_{LEAD}		See Note(3)	℃
Electrostatic Discharge Voltage	V_{ESD}	Human Body Model(4)	-2000 to +2000	V

Notes:
(1) Specification for HT25WD40A is preliminary. See preliminary designation at the end of this document.
(2) This device has been designed and tested for the specified operation ranges. Proper operation outside these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
(3) Compatible to JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
(4) JEDEC Std. JESD22-A114A (C1=100 pF, R1=1500 ohms, R2=500 ohms).

8.2. Recommended Operating Ranges

Table 8.3 Recommended Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	V_{CC}(1)	F_R=100MHz,f_R=80MHz(2)	1.65	3.6	V
Ambient Temperature, Operating	T_A	Industrial	-40	125	℃

Notes:
(1) Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.
(2) See details Table 8.6 AC Electrical Characteristics.

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8.3. DC Characteristics

Table 8.4a DC Characteristics

(T = -40°C ~ 85°C, VCC = 1.65 ~ 3.6V)

SYMBOL	PARAMETER	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
CIN(1)	Input Capacitance	VIN = 0V(2)			6	pF
COUT(1)	Output Capacitance	VOUT = 0V(2)			8	pF
ILI	Input Leakage				±3	uA
ILO	I/O Leakage				±2	uA
ICC1	Standby Current,	CS# = V_{CC}, VIN=V_{CC} / V_{SS}		0.5/1	5	uA
ICC2	Deep Power-down Current	CS# = V_{CC}, VIN=V_{CC} / V_{SS}		0.5/1	5	uA
ICC3	Current Read Data / Dual 10MHz(2)	C = 0.1 V_{CC} / 0.9 V_{CC} DO = Open		1.2	4	mA
ICC3	Current Read Data / Dual 50MHz(2)	C = 0.1 V_{CC} / 0.9 V_{CC} DO = Open		1.8	5	mA
ICC3	Current Read Data / Dual 80MHz(2)	C = 0.1 V_{CC} / 0.9 V_{CC} DO = Open		2.5	7	mA
ICC3	Current Read Data 100MHz(2)	C = 0.1 V_{CC} / 0.9 V_{CC} DO = Open		2.9	8	mA
ICC4	Current Page Program	CS# = V_{CC}		3	9	mA
ICC5	Current Write Status Register	CS# = V_{CC}		3	9	mA
ICC6	Current Sector Erase	CS# = V_{CC}		3	9	mA
ICC7	Current Block/Chip Erase	CS# = V_{CC}		3	9	mA
VIL	Input Low Voltage		-0.5		V_{CC}×0.2	V
VIH	Input High Voltage		V_{CC}×0.7		V_{CC} +0.4	V
VOL	Output Low Voltage	IOL = 100 uA			0.4	V
VOH	Output High Voltage	IOH = - 100 uA	V_{CC} - 0.2			V

Notes:
(1) Tested on sample basis and specified through design and characterization data. T=25°C, V_{CC}=3V.
(2) Checker Board Pattern.

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Table 8.4b DC Characteristics

(T = -40°C ~ 105°C, VCC = 1.65 ~ 3.6V)

SYMBOL	PARAMETER	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
CIN(1)	Input Capacitance	VIN = 0V(2)			6	pF
COUT(1)	Output Capacitance	VOUT = 0V(2)			8	pF
ILI	Input Leakage				±3	uA
ILO	I/O Leakage				±2	uA
ICC1	Standby Current,	CS# = V_{CC}, VIN=V_{CC} / V_{SS}		0.5/2	10	uA
ICC2	Deep Power-down Current	CS# = V_{CC}, VIN=V_{CC} / V_{SS}		0.5/2	10	uA
ICC3	Current Read Data / Dual 10MHz(2)	C = 0.1 V_{CC} / 0.9 V_{CC} DO = Open		1.2	5.5	mA
ICC3	Current Read Data / Dual 50MHz(2)	C = 0.1 V_{CC} / 0.9 V_{CC} DO = Open		1.8	7	mA
ICC3	Current Read Data / Dual 80MHz(2)	C = 0.1 V_{CC} / 0.9 V_{CC} DO = Open		2.5	12	mA
ICC3	Current Read Data 100MHz(2)	C = 0.1 V_{CC} / 0.9 V_{CC} DO = Open		2.9	15	mA
ICC4	Current Page Program	CS# = V_{CC}		3	15	mA
ICC5	Current Write Status Register	CS# = V_{CC}		3	15	mA
ICC6	Current Sector Erase	CS# = V_{CC}		3	15	mA
ICC7	Current Block/Chip Erase	CS# = V_{CC}		3	15	mA
VIL	Input Low Voltage		-0.5		V_{CC}×0.2	V
VIH	Input High Voltage		V_{CC}×0.7		V_{CC} +0.4	V
VOL	Output Low Voltage	IOL = 100 uA			0.4	V
VOH	Output High Voltage	IOH = - 100 uA	V_{CC} - 0.2			V

Notes:

(1)Tested on sample basis and specified through design and characterization data. T=25°C, V_{CC}=3V.

(2)Checker Board Pattern.

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Table 8.4c DC Characteristics

(T = -40°C ~ 125°C, VCC = 1.65 ~ 3.6V)

SYMBOL	PARAMETER	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
CIN(1)	Input Capacitance	VIN = 0V(2)			6	pF
COUT(1)	Output Capacitance	VOUT = 0V(2)			8	pF
ILI	Input Leakage				±3	uA
ILO	I/O Leakage				±2	uA
ICC1	Standby Current,	CS# = V_{CC}, VIN=V_{CC} / V_{SS}		0.5/2	15	uA
ICC2	Deep Power-down Current	CS# = V_{CC}, VIN=V_{CC} / V_{SS}		0.5/2	15	uA
ICC3	Current Read Data / Dual 10MHz(2)	C = 0.1 V_{CC} / 0.9 V_{CC} DO = Open		1.2	7	mA
ICC3	Current Read Data / Dual 50MHz(2)	C = 0.1 V_{CC} / 0.9 V_{CC} DO = Open		1.8	15	mA
ICC3	Current Read Data / Dual 80MHz(2)	C = 0.1 V_{CC} / 0.9 V_{CC} DO = Open		2.5	20	mA
ICC3	Current Read Data 100MHz(2)	C = 0.1 V_{CC} / 0.9 V_{CC} DO = Open		2.9	22	mA
ICC4	Current Page Program	CS# = V_{CC}		3	20	mA
ICC5	Current Write Status Register	CS# = V_{CC}		3	20	mA
ICC6	Current Sector Erase	CS# = V_{CC}		3	20	mA
ICC7	Current Block/Chip Erase	CS# = V_{CC}		3	20	mA
VIL	Input Low Voltage		-0.5		V_{CC}×0.2	V
VIH	Input High Voltage		V_{CC}×0.7		V_{CC} +0.4	V
VOL	Output Low Voltage	IOL = 100 uA			0.4	V
VOH	Output High Voltage	IOH = - 100 uA	V_{CC} - 0.2			V

Notes:
(1)Tested on sample basis and specified through design and characterization data. T=25°C, V_{CC}=3V.
(2)Checker Board Pattern.

8.4. AC Measurement Conditions

Table 8.5 AC Measurement Conditions

Symbol	PARAMETER	Min.	Max.	Unit
CL	Load Capacitance		30	pF
TR, TF	Input Rise and Fall Times		5	ns
VIN	Input Pulse Voltages	0.1V_{CC} to 0.8V_{CC}		V
VtIN	Input Timing Reference Voltages	0.2V_{CC} to 0.7V_{CC}		V
VtON	Output Timing Reference Voltages	0.5 V_{CC}		V

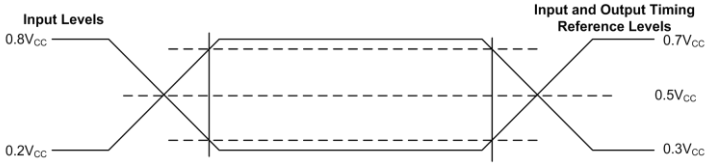


Figure 8.3 AC Measurement I/O Waveform

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8.5. AC Electrical Characteristics

Table 8.6a AC Electrical Characteristics

(T = -40°C ~ 85°C, VCC = 1.65 ~ 3.6V, C_L = 30pf)

SYMBOL	ALT	Parameter	SPEC			UNIT
			MIN	TYP	MAX	
F_{R1}	f_{C1}	Clock frequency for Fast Read (0Bh) , Vcc=2.3V-3.6V	D.C.		100	MHz
F_{R2}	f_{C2}	Clock frequency for Fast Read (0Bh) , Vcc=1.65V-2.3V(1)	D.C.		50	MHz
f_{R1}		Clock frequency for Read (03h) , Dual Output (3Bh) , Vcc=2.3V-3.6V	D.C.		80	MHz
f_{R2}		Clock frequency for Read (03h) , Dual Output (3Bh) , Vcc=1.65V-2.3V(1)	D.C.		40	MHz
t_{CLH}, t_{CLL}(1)		Clock High, Low Time for all instructions	4			ns
t_{CLCH}(2)		Clock Rise Time peak to peak	0.1			V/ns
t_{CHCL}(2)		Clock Fall Time peak to peak	0.1			V/ns
t_{SLCH}	t_{CSS}	CS# Active Setup Time relative to CLK	10			ns
t_{CHSL}		CS# Not Active Hold Time relative to CLK	10			ns
t_{DVCH}	t_{DSU}	Data In Setup Time	4			ns
t_{CHDX}	t_{DH}	Data In Hold Time	4			ns
t_{CHSH}		CS# Active Hold Time relative to CLK	10			ns
t_{SHCH}		CS# Not Active Setup Time relative to CLK	10			ns
t_{SHSL}	t_{CSH}	CS# Deselect Time (SPI)	40			ns
t_{SHQZ}(2)	t_{DIS}	Output Disable Time			12	ns
t_{CLQV}	t_V	Clock Low to Output Valid, Vcc=2.3V-3.6V		4	7	ns
t_{CLQV}	t_V	Clock Low to Output Valid, Vcc=1.65V-2.3V		6	12	ns
t_{CLQX}	t_{HO}	Output Hold Time	2			ns
t_{WHSL}(3)		Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}(3)		Write Protect Hold Time After CS# High	100			ns
t_{DP}(2)		CS# High to Power-down Mode			0.1	µs
t_{RES1}(2)		CS# High to Standby Mode without Electronic Signature Read			0.1	µs
t_{RES2}(2)		CS# High to Standby Mode with Electronic Signature Read			0.1	µs
t_W		Write Status Register Time		5	40	ms
t_{PP}		Page Program Time		1.2	6	ms
t_{SE}		Sector Erase Time (4KB)		75	500	ms
t_{BE1}		Block Erase Time (32KB)		0.2	2	s
t_{BE2}		Block Erase Time (64KB)		0.35	3	s
t_{CE}		Chip Erase Time (HT25WD40A)		2.3	15	s

Notes:

(1) Clock high + Clock low must be less than or equal to $1/f_C$.

(2) Value guaranteed by design and/or characterization, not 100% tested in production.

(3) Only applicable as a constraint for a Write Status Register instruction when SRP=1.

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Table 8.6b AC Electrical Characteristics

(T = -40°C ~ 105°C, VCC = 1.65 ~ 3.6V, C_L = 30pf)

SYMBOL	ALT	Parameter	SPEC			UNIT
			MIN	TYP	MAX	
F_{R1}	f_{C1}	Clock frequency for Fast Read (0Bh) , Vcc=2.3V-3.6V	D.C.		100	MHz
F_{R2}	f_{C2}	Clock frequency for Fast Read (0Bh) , Vcc=1.65V-2.3V(1)	D.C.		50	MHz
f_{R1}		Clock frequency for Read (03h) , Dual Output (3Bh) , Vcc=2.3V-3.6V	D.C.		80	MHz
f_{R2}		Clock frequency for Read (03h) , Dual Output (3Bh) , Vcc=1.65V-2.3V(1)	D.C.		40	MHz
t_{CLH}, t_{CLL}(1)		Clock High, Low Time for all instructions	4			ns
t_{CLCH}(2)		Clock Rise Time peak to peak	0.1			V/ns
t_{CHCL}(2)		Clock Fall Time peak to peak	0.1			V/ns
t_{SLCH}	t_{CSS}	CS# Active Setup Time relative to CLK	10			ns
t_{CHSL}		CS# Not Active Hold Time relative to CLK	10			ns
t_{DVCH}	t_{DSU}	Data In Setup Time	4			ns
t_{CHDX}	t_{DH}	Data In Hold Time	4			ns
t_{CHSH}		CS# Active Hold Time relative to CLK	10			ns
t_{SHCH}		CS# Not Active Setup Time relative to CLK	10			ns
t_{SHSL}	t_{CSH}	CS# Deselect Time (SPI)	40			ns
t_{SHQZ}(2)	t_{DIS}	Output Disable Time			12	ns
t_{CLQV}	t_V	Clock Low to Output Valid			12	ns
t_{CLQX}	t_{HO}	Output Hold Time	2			ns
t_{WHSL}(3)		Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}(3)		Write Protect Hold Time After CS# High	100			ns
t_{DP}(2)		CS# High to Power-down Mode			0.1	μs
t_{RES1}(2)		CS# High to Standby Mode without Electronic Signature Read			0.1	μs
t_{RES2}(2)		CS# High to Standby Mode with Electronic Signature Read			0.1	μs
t_W		Write Status Register Time		5	40	ms
t_{PP}		Page Program Time		1.2	6	ms
t_{SE}		Sector Erase Time (4KB)		75	550	ms
t_{BE1}		Block Erase Time (32KB)		0.2	2.2	s
t_{BE2}		Block Erase Time (64KB)		0.35	3.5	s
t_{CE}		Chip Erase Time (HT25WD40A)		2.3	18	s

Notes:

(1) Clock high + Clock low must be less than or equal to $1/f_C$.

(2) Value guaranteed by design and/or characterization, not 100% tested in production.

(3) Only applicable as a constraint for a Write Status Register instruction when SRP=1.

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Table 8.6c AC Electrical Characteristics

(T = -40°C ~ 125°C, VCC = 1.65 ~ 3.6V, C_L = 30pf)

SYMBOL	ALT	Parameter	SPEC			UNIT
			MIN	TYP	MAX	
F_{R1}	f_{C1}	Clock frequency for Fast Read (0Bh) , Vcc=2.3V-3.6V	D.C.		100	MHz
F_{R2}	f_{C2}	Clock frequency for Fast Read (0Bh) , Vcc=1.65V-2.3V(1)	D.C.		50	MHz
f_{R1}		Clock frequency for Read (03h) , Dual Output (3Bh) , Vcc=2.3V-3.6V	D.C.		80	MHz
f_{R2}		Clock frequency for Read (03h) , Dual Output (3Bh) , Vcc=1.65V-2.3V(1)	D.C.		40	MHz
t_{CLH}, t_{CLL}(1)		Clock High, Low Time for all instructions	4			ns
t_{CLCH}(2)		Clock Rise Time peak to peak	0.1			V/ns
t_{CHCL}(2)		Clock Fall Time peak to peak	0.1			V/ns
t_{SLCH}	t_{CSS}	CS# Active Setup Time relative to CLK	10			ns
t_{CHSL}		CS# Not Active Hold Time relative to CLK	10			ns
t_{DVCH}	t_{DSU}	Data In Setup Time	4			ns
t_{CHDX}	t_{DH}	Data In Hold Time	4			ns
t_{CHSH}		CS# Active Hold Time relative to CLK	10			ns
t_{SHCH}		CS# Not Active Setup Time relative to CLK	10			ns
t_{SHSL}	t_{CSH}	CS# Deselect Time (SPI)	40			ns
t_{SHQZ}(2)	t_{DIS}	Output Disable Time			12	ns
t_{CLQV}	t_V	Clock Low to Output Valid			12	ns
t_{CLQX}	t_{HO}	Output Hold Time	2			ns
t_{WHSL}(3)		Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}(3)		Write Protect Hold Time After CS# High	100			ns
t_{DP}(2)		CS# High to Power-down Mode			0.1	µs
t_{RES1}(2)		CS# High to Standby Mode without Electronic Signature Read			0.1	µs
t_{RES2}(2)		CS# High to Standby Mode with Electronic Signature Read			0.1	µs
t_W		Write Status Register Time		5	40	ms
t_{PP}		Page Program Time		1.2	6	ms
t_{SE}		Sector Erase Time (4KB)		75	600	ms
t_{BE1}		Block Erase Time (32KB)		0.2	2.5	s
t_{BE2}		Block Erase Time (64KB)		0.35	4	s
t_{CE1}		Chip Erase Time (HT25WD40A)		2.3	20	s

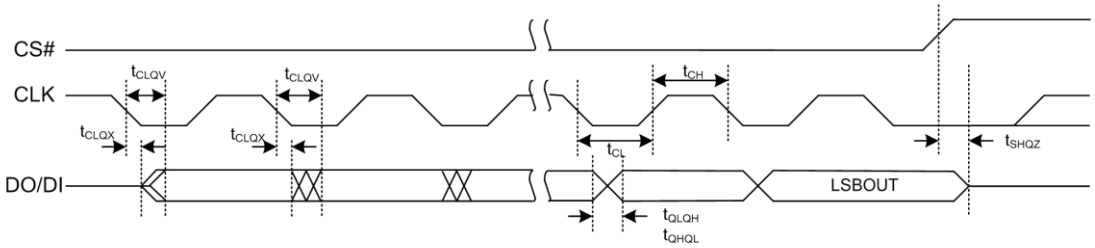
Notes:

(1) Clock high + Clock low must be less than or equal to $1/f_C$.

(2) Value guaranteed by design and/or characterization, not 100% tested in production.

(3) Only applicable as a constraint for a Write Status Register instruction when SRP=1.

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*DIO IS AN OUTPUT ONLY FOR THE FAST READ DUAL OUTPUT INSTRUCTIONS (3BH)

Figure 8.4 Serial Output Timing

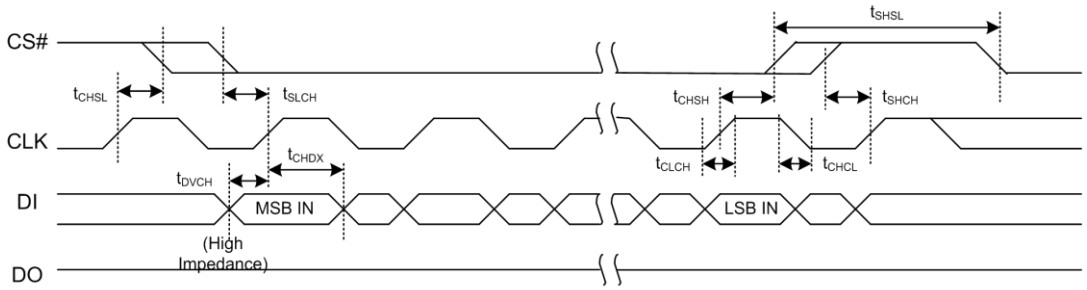
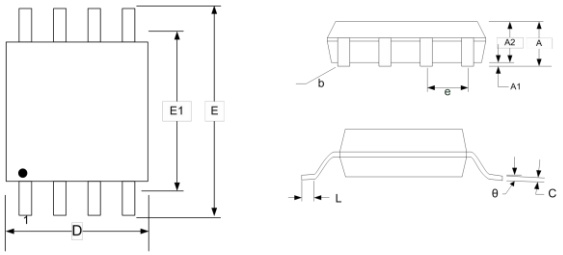


Figure 8.5 Input Timing

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9. PACKAGE MECHANICAL

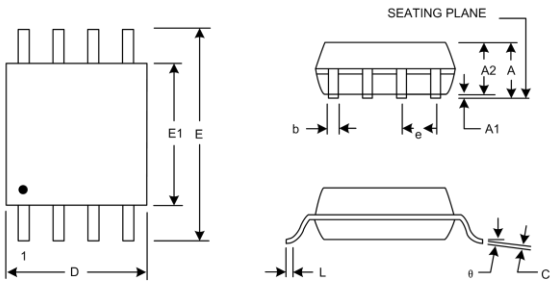
9.1. SOP8 - 150mil



SYMBOL	MILIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A	---	---	1.75	---	---	0.069
A1	0.05	0.15	0.25	0.002	0.006	0.010
A2	1.25	1.40	1.55	0.049	0.055	0.061
b	0.31	0.41	0.51	0.012	0.016	0.020
C	0.15	0.20	0.25	0.006	0.008	0.010
D	4.80	4.90	5.00	0.1890	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	---	1.27BSC	---	---	0.05BSC	---
L	0.40	---	0.80	0.016	---	0.031
θ	0°	---	8°	---	---	---

Note:
1. Both the package length and width do not include the mold flash.
2. Seating plane: Max. 0.1mm.

9.2. SOP8 - 208mil

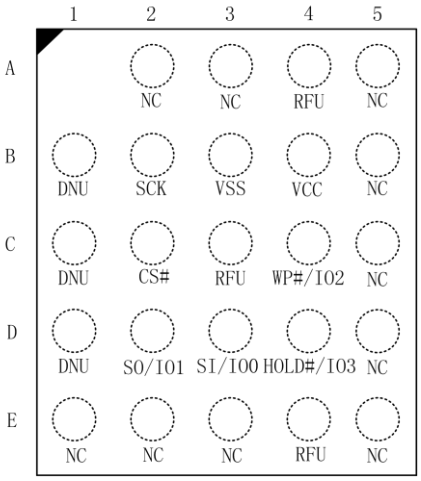


SYMBOL	MILIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A	---	---	2.15	---	---	0.085
A1	0.05	0.15	0.25	0.002	0.006	0.010
A2	1.70	1.80	1.91	0.067	0.071	0.075
b	0.31	0.41	0.51	0.012	0.016	0.020
C	0.15	0.20	0.25	0.006	0.008	0.010
D	5.13	5.23	5.33	0.202	0.206	0.210
E	7.70	7.90	8.10	0.303	0.311	0.319
E1	5.18	5.28	5.38	0.204	0.208	0.212
e	---	1.27BSC	---	---	0.05BSC	---
L	0.50	0.65	0.80	0.020	0.03	0.031
θ	0°	---	8°	0°	---	8°

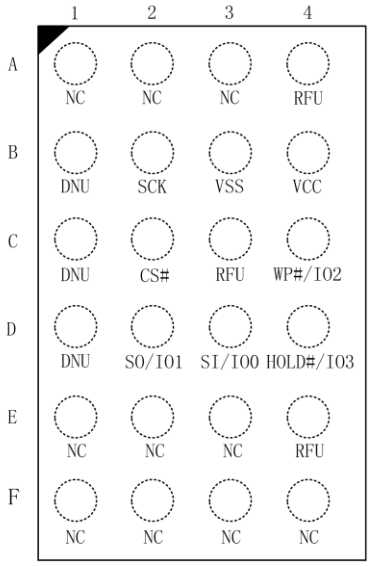
Note:
1. Both the package length and width do not include the mold flash.
2. Seating plane: Max. 0.1mm.

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9.3. TFBGA24 (5*5 Ball Array)

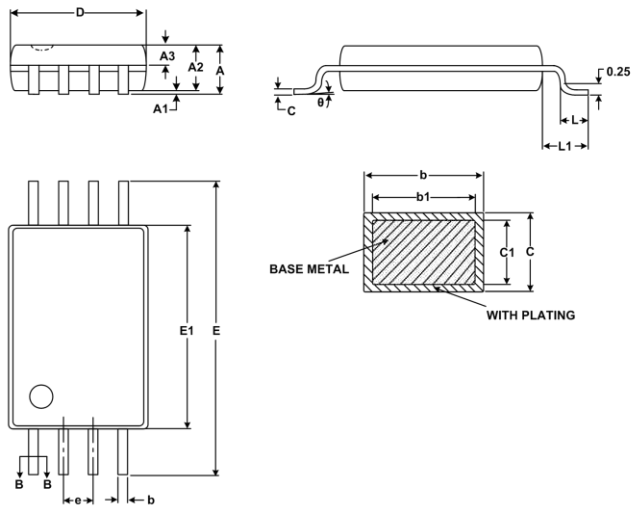


9.4. TFBGA24 (6*4 Ball Array)



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9.5. TSSOP8 - 173mil

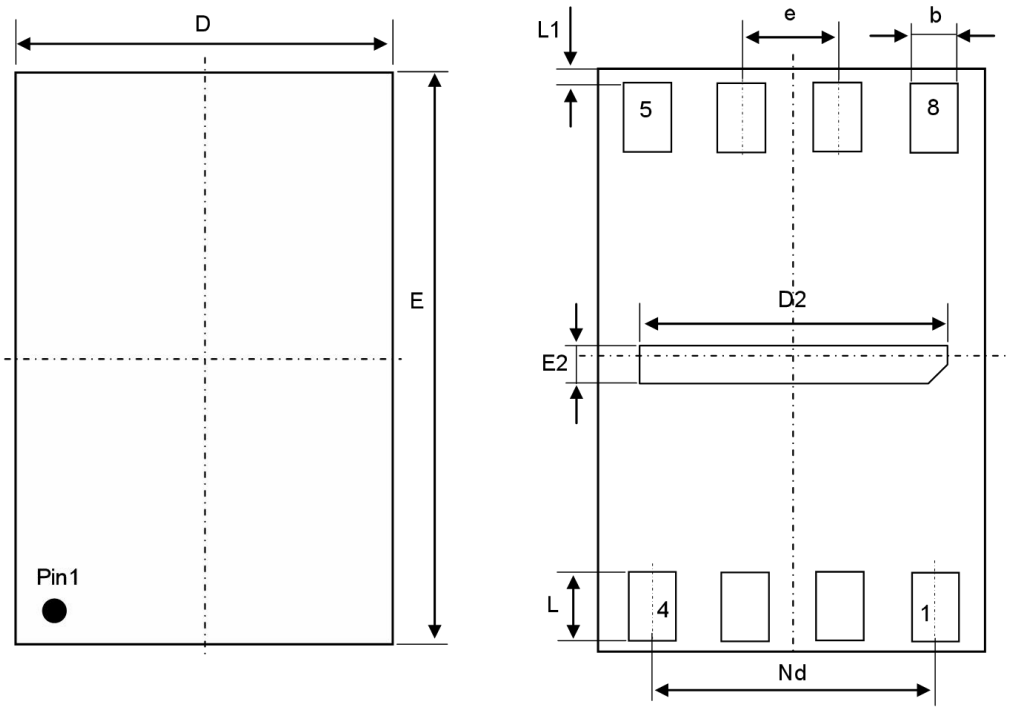


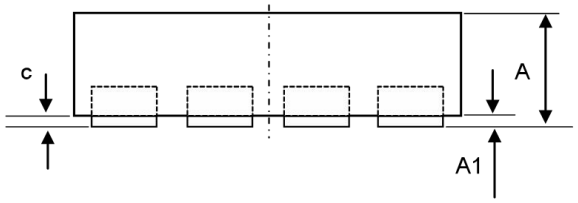
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	–	0.28
b1	0.19	0.22	0.25
c	0.13	–	0.17
c1	0.12	0.13	0.14
D	2.90	3.00	3.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	–	0.75
L1	1.00REF		
θ	0	–	8°

Note:
1. Both the package length and width do not include the mold flash.
2. Seating plane: Max. 0.1mm.

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9.6. DFN8 (2*3*0.55mm)





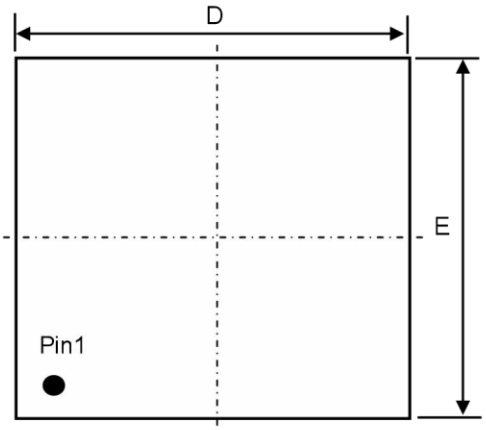
Dimensions :

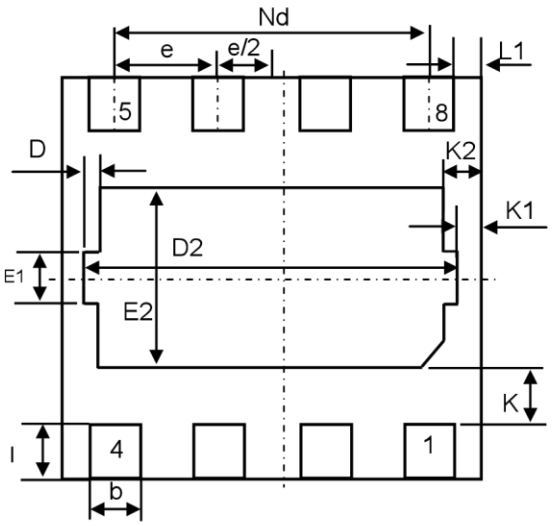
Symbol / Unit		A	A1	b	c	D	D2	e	Nd	E	E2	L	L1
Min	mm	0.50	0	0.18	0.10	1.90	1.50	0.50 REF	1.50 REF	2.90	0.10	0.30	0.05
Nom		0.55	0.02	0.25	0.15	2.00	1.60			3.00	0.20	0.35	0.10
Max		0.60	0.05	0.30	0.20	2.10	1.70			3.10	0.30	0.40	0.15

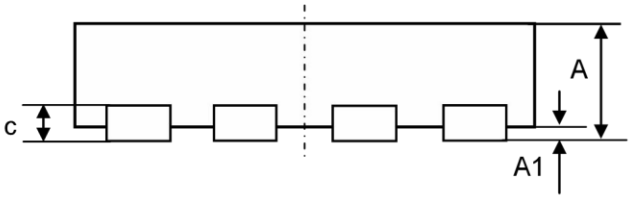
Note:
1. Both the package length and width do not include the mold flash.
2. The exposed metal pad area on the bottom of the package is floating.
3. Coplanarity ≤ 0.08mm.Package edge tolerance ≤ 0.10mm.
4. The lead shape may be of little difference according to different package factories. These lead shapes are compatible with each other.

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9.7. DFN8 (1.5*1.5*0.45mm)







Dimensions：

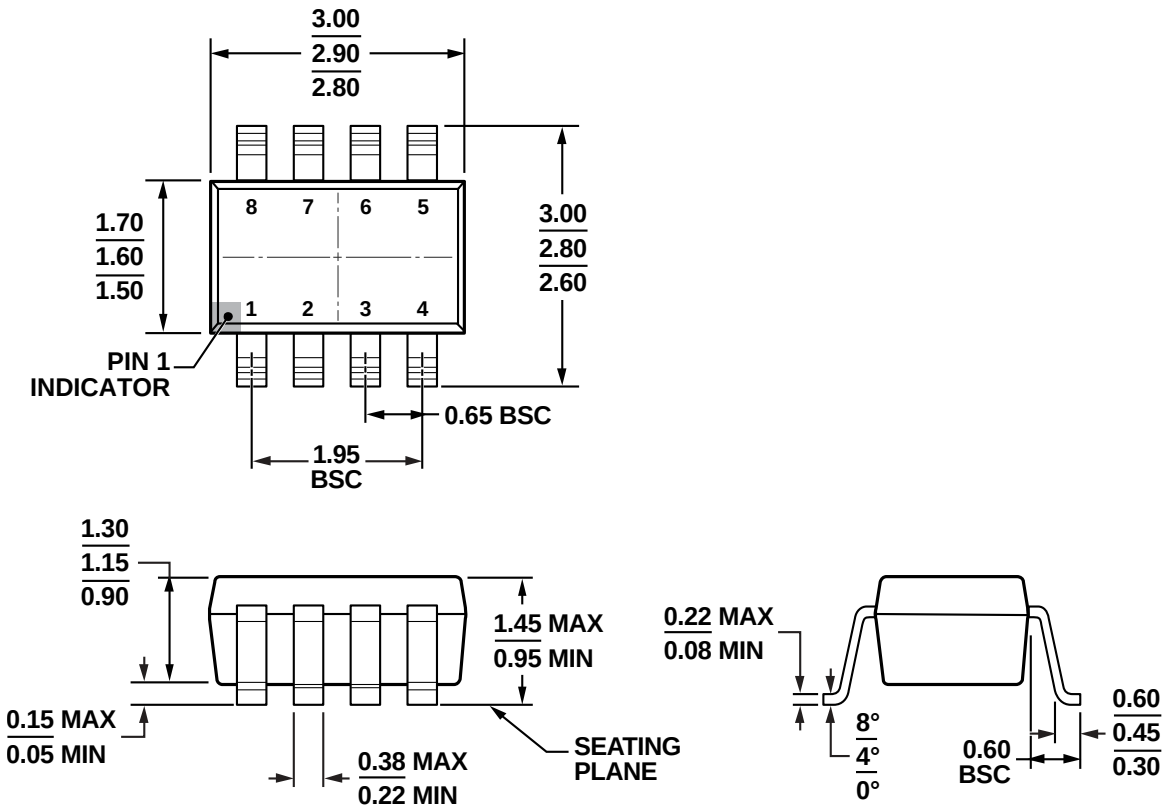
Symbol / Unit		A	A1	b	c	D	D1	D2	e	Nd	E	E1	E2	L	L1	K	K1	K2
Min	mm	0.40	0.00	0.13	0.15 REF	1.45	0.05 REF	1.20	0.40 REF	1.20 REF	1.45	0.20 REF	0.60	0.15	0.06 REF	0.20 REF	0.10 REF	0.15 REF
Nom		0.45	0.02	0.18		1.50		1.30			1.50		0.70	0.20				
Max		0.50	0.05	0.23		1.55		1.40			1.55		0.80	0.25				

Note:

1. Both the package length and width do not include the mold flash.
2. The exposed metal pad area on the bottom of the package is floating.
3. Coplanarity ≤ 0.08mm.Package edge tolerance ≤ 0.10mm.
4. The lead shape may be of little difference according to different package factories. These lead shapes are compatible with each other.

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9.8. SOT23-8 (1.5*1.5*0.45mm)



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