GDQ2BFAA

DATASHEET

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1 FEATURES

- Power supply : VDD = VDDQ = 1.2V (1.14V to 1.26V); VPP = 2.5V (2.375V to 2.75V)
- JEDEC standard package: x16 96-ball FBGA
- Array Configuration : 8 banks (x16) 2 groups of 4 banks
- 8n-bit prefetch architecture
- Burst Length (BL): 8 and 4 with Burst Chop (BC)
- Programmable CAS Latency (CL)
- Programmable CAS Write Latency (CWL)
- Internal generated Vref for data inputs
- On-Die Termination (ODT) : Support Nominal, Park and Dynamic ODT
- Differential clock and data strobe inputs (CK_t ,CK_c; DQS_t, DQS_c)
- Interface: 1.2V Pseudo Open Drain (POD) IO
- Per DRAM Addressability (PDA)
- Data Bus Inversion (DBI)
- Data Mask (DM) for write data
- Maximum Power Saving Mode (MPSM)
- Asynchronous reset for power up
- Precharge: Auto precharge option for each burst access
- Operating case temperature :-40°C ≤ TCase ≤95°C
- Support auto-refresh and self-refresh mode
- Average Refresh Period:
  - 7.8μs at -40°C ≤ TCase ≤ 85°C
  - 3.9μs at 85°C < TCase ≤ 95°C
- Fine granularity refresh 2x, 4x mode for smaller tRFC
- Programmable data strobe preambles
- Command Address (CA) Parity is supported
- Write Cyclic Redundancy Code (CRC) is supported
- Connectivity test mode (TEN) is supported
- Gear Down Mode
- Output driver calibration through ZQ pin (RZQ: 240ohm ± 1%)
- JEDEC JESD-79-4 compliant
- RoHS compliant

Note:

The functionality described and the timing specifications included in this datasheet are for the DLL Enabled mode of operation (normal operation), unless specifically stated otherwise.

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1.1 Speed Bins

Speed	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	Unit
	11-11-11	13-13-13	15-15-15	17-17-17	19-19-19	22-22-22	
tCK (min)	1.25	1.071	0.937	0.833	0.75	0.625	ns
CAS Latency	11	13	15	17	19	22	nCK
tRCD (min)	13.75	13.92	14.06	14.16	14.25	13.75	ns
tRP (min)	13.75	13.92	14.06	14.16	14.25	13.75	ns
tRAS (min)	35	34	33	32	32	33	ns
tRC (min)	48.75	47.92	47.06	46.16	46.25	46.75	ns

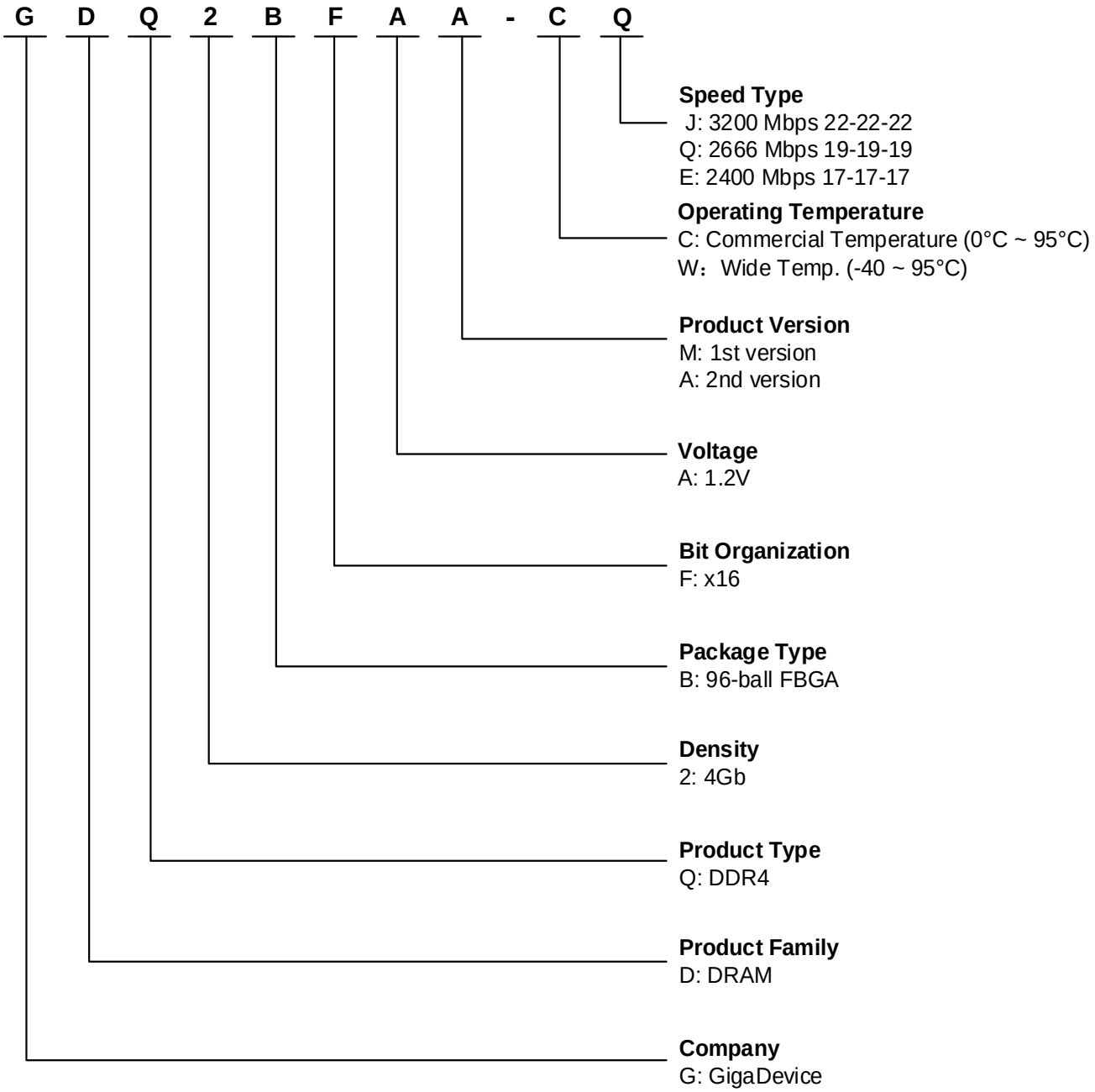
1.2 Address Table

Parameter	256 Mb x16
Number of Bank Groups	2
Number of Banks per Bank Group	4
Bank Group Address	BG0
Bank Address per Bank Group	BA0~BA1
Row Address	A0~A14
Column Address	A0~A9
Page Size	2KB

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2 ORDERING INFORMATION

2.1 Part Number Decoding



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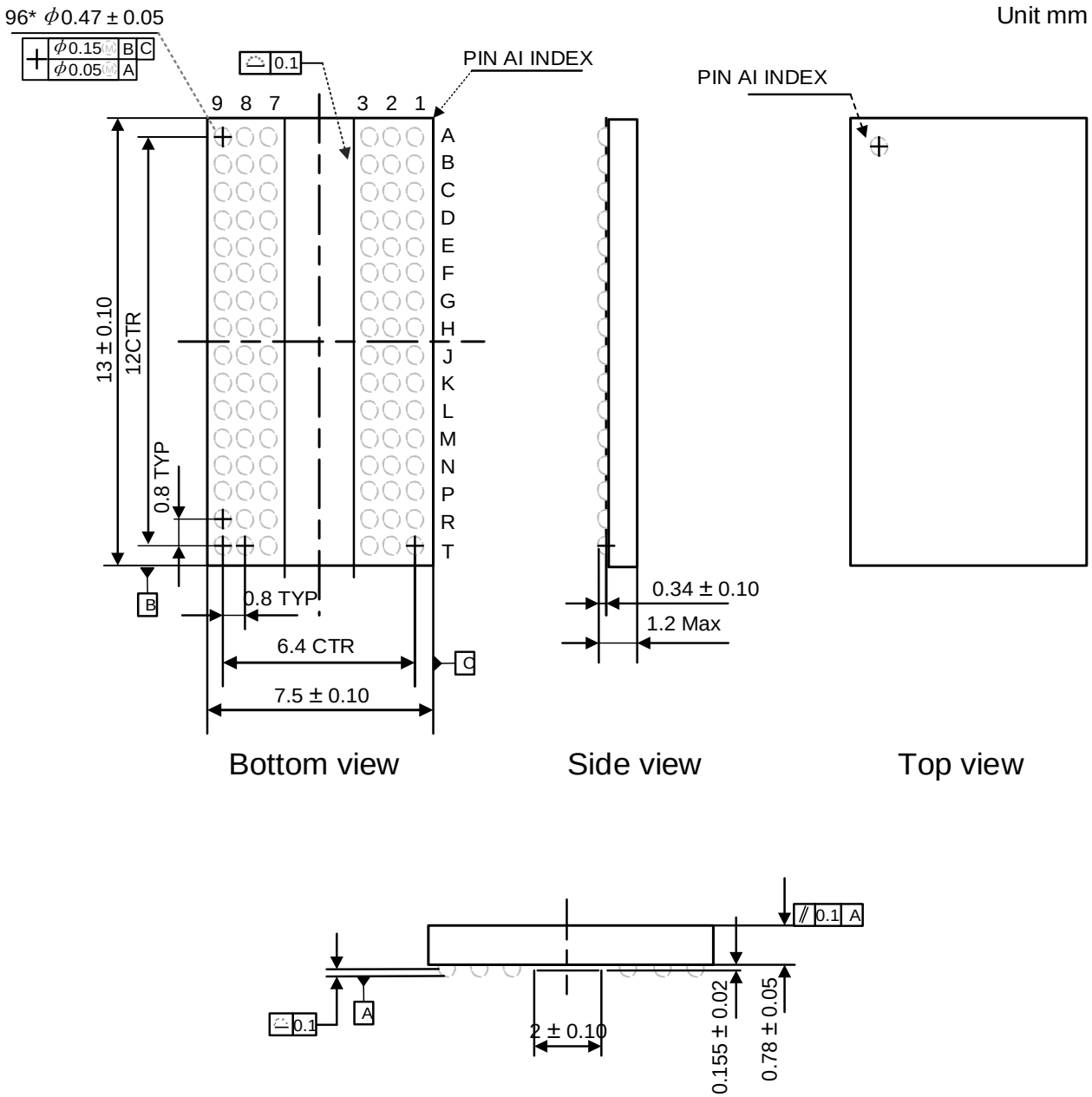
2.2 Valid Part Numbers

Part Number	Organization	Data Rate	CL-tRCD-tRP
GDQ2BFAA-CE	256 Mb x 16	2400 Mbps	17-17-17
GDQ2BFAA-CQ	256 Mb x 16	2666 Mbps	19-19-19
GDQ2BFAA-CJ	256 Mb x 16	3200 Mbps	22-22-22
GDQ2BFAA-WQ	256 Mb x 16	2666 Mbps	19-19-19
GDQ2BFAA-WJ	256 Mb x 16	3200 Mbps	22-22-22

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3 PACKAGE INFORMATION

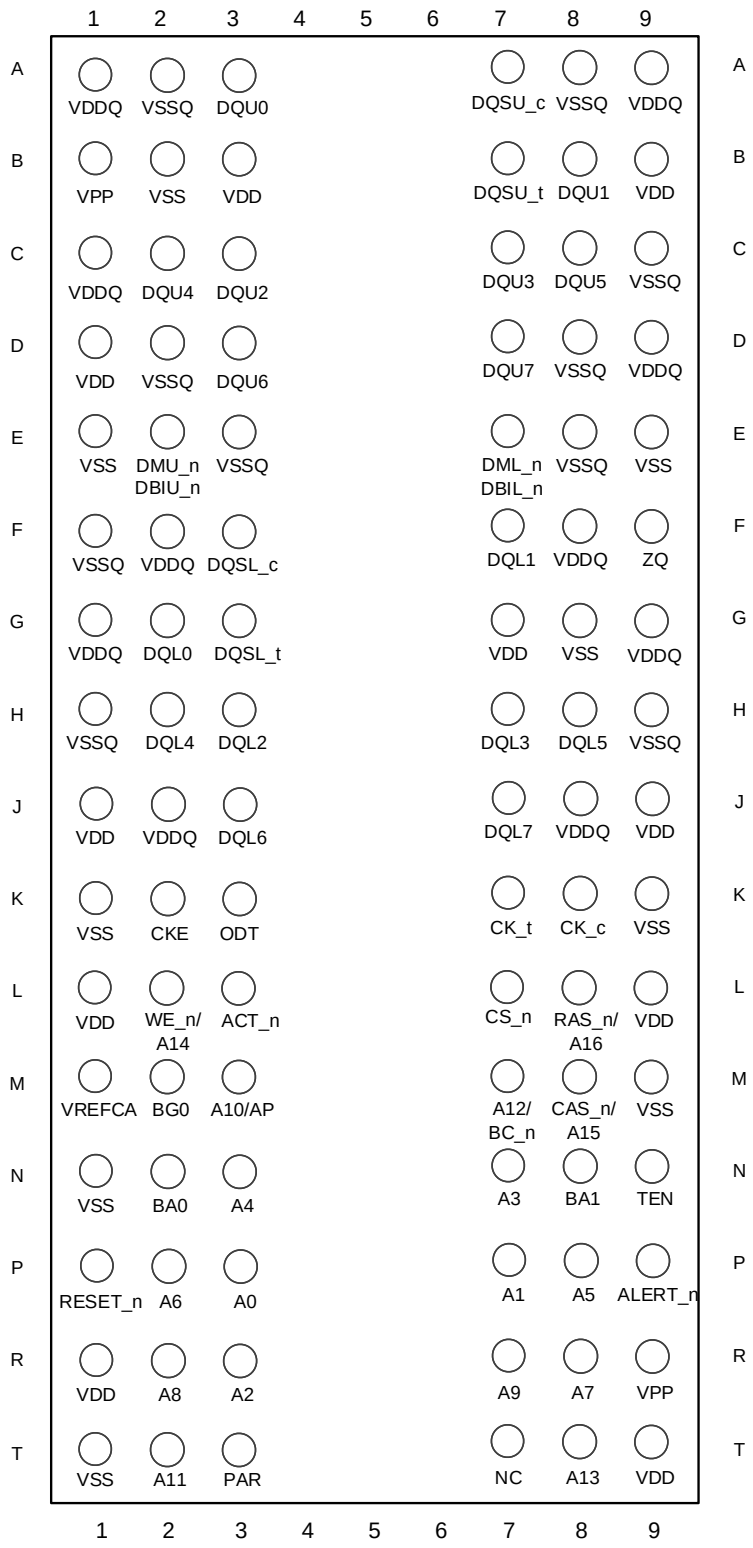
3.1 Package 96-Ball FBGA (x16)



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4 BALL ASSIGNMENTS

4.1 96-Ball FBGA (x16) ball assignments



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4.2 Ball Description

Symbol	Type	Function
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE	Input	**Clock Enable:** CKE High activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power- Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout Read and Write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self- Refresh.
CS_n	Input	**Chip Select:** All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
ODT	Input	**On Die Termination:** ODT (registered High) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	**Activation Command Input:** ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/ A14 will be considered as Row Address A16, A15 and A14.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	**Command Inputs:** RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. These balls have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table.
DM_n, DBI_n (DMU_n, DBIU_n DML_n, DBIL_n)	I/O	**Input Data Mask and Data Bus Inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8.
BG0-BG1	Input	**Bank Group Inputs:** BG0-BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/x8 have BG0 and BG1, but x16 has only BG0.

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Symbol	Type	Function
BA0-BA1	Input	**Bank Address Inputs:** BA0-BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0-A16	Input	**Address Inputs:** Provide the row address for ACTIVATE commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.
A10/AP	Input	**Auto-precharge:** A10 is sampled during Read/Write commands to determine whether Auto-precharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Auto-precharge; LOW: no Auto-precharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12/BC_n	Input	**Burst Chop:** A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See “Command Truth Table” of Operation Guide for details.
RESET_n	Input	**Active Low Asynchronous Reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
DQ	I/O	**Data Input/Output:** Bi-directional data bus. If CRC is enabled via mode register, then CRC code is added at the end of Data Burst. Any DQ from DQ3~DQ0 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	I/O	**Data Strobe:** Output with Read data, input with Write data. Edge-aligned with Read data, centered-aligned with Write data. For x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during Reads and Writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	**Termination Data Strobe:** TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11, A12, A10 and TDQS_c is not used. x4/ x16 DRAMs must dis able the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	**Command and Address Parity Input:** DDR4 Supports Even Parity Check in DRAMs with MR setting. Once it is enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A0-A16. Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is low

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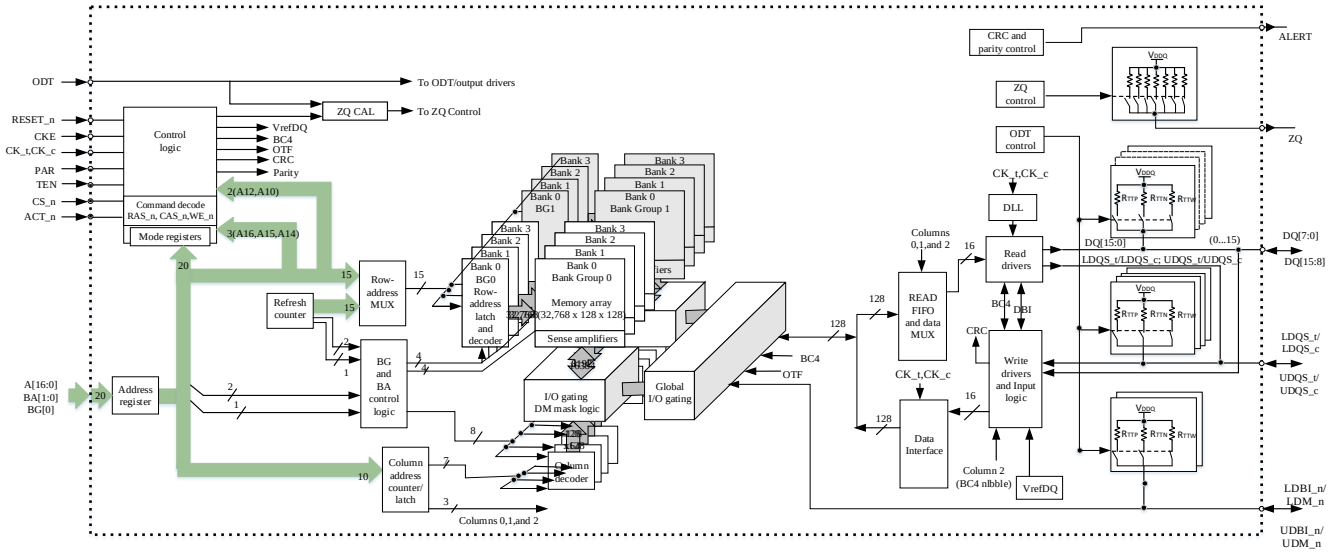
Symbol	Type	Function
ALERT_n	I/O	**ALERT:** It has multi functions such as CRC error flag, Command and Address Parity error flag as output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as an input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n pin must be bounded to VDD on board.
TEN	Input	**Connectivity Test Mode Enable:** Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. High in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on system. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		**No Connect:** No internal electrical connection is present.
VDDQ	Supply	**DQ Power Supply:** 1.2 V +/- 0.06 V
VSSQ	Supply	**DQ Ground**
VDD	Supply	**Power Supply:** 1.2 V +/- 0.06 V
VSS	Supply	**Ground**
VPP	Supply	**DRAM Activating Power Supply:** 2.5V (2.375V min, 2.75V max)
VREFCA	Supply	**Reference voltage for CA**
ZQ	Supply	**Reference Pin for ZQ calibration**

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5 Functional Block Diagram

DDR4 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 16-bank (4-banks per Bank Group) DRAM.

Figure 5-1. 256 Meg x 16 Functional Block Diagram



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6 ABSOLUTE MAXIMUM RATINGS

6.1 Absolute Maximum DC Ratings

Table 6-1. Absolute Maximum DC Ratings

Symbol	Parameter	Min	Max	Unit	Note
VDD	Voltage on VDD pin relative to Vss	-0.3	1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3	1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3	3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VrefCA relative to Vss	-0.3	1.5	V	1,3,5
T_{STG}	Storage Temperature	-55	100	°C	1,2

Note:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV.
4. VPP must be equal or greater than VDD/VDDQ at all times.
5. Overshoot area above 1.5V is specified in Section 7.3.5 and Section 7.3.6.

6.2 Recommended DC Operating Conditions

Table 6-2. Recommended DC Operating Conditions

Symbol	Parameter	Ratings			Unit	Note
		Min	Typ.	Max		
VDD	Supply voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply voltage for output	1.14	1.2	1.26	V	1,2,3
VPP	Wordline supply voltage	2.375	2.5	2.75	V	3

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

6.3 DRAM Component Operating Temperature Range

Table 6-3. Operating Temperature Range

Symbol	Parameter	Rating	Unit	Note
T_{OPER}	Normal Temperature Range	-40~85	°C	1,2
	Extended Temperature Range	85~95	°C	1,3

Note:

1. Operating Temperature TOPER is the case surface temperature on the center/top side of the DRAM. For measurement

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conditions, please refer to the JEDEC document JESD51-2.

2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85°C under all operating conditions for the commercial offering; The industrial and automotive temperature offerings allow the case temperature to go below 0°C to -40°C.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability.
   - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0 and MR2 A7 = 1) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1 and MR2 A7 = 1).

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7 AC AND DC INPUT MEASUREMENT LEVELS

7.1 AC and DC Logic Input Levels for Single-ended Signals

Table 7-1. Single-ended AC and DC Input Levels for Command and Address

Symbol	Parameter	1600/1866/2133/2400		2666/3200		Unit	Note
		Min	Max	Min	Max		
VIH.CA(DC75)	DC input logic high	VREFCA + 0.075	VDD	-	-	V	
VIL.CA(DC75)	DC input logic low	VSS	VREFCA - 0.075	-	-	V	
VIH.CA(DC65)	DC input logic high	-	-	VREFCA + 0.065	VDD	V	
VIL.CA(DC65)	DC input logic low	-	-	VSS	VREFCA - 0.065	V	
VIH.CA(AC100)	AC input logic high	VREF + 0.1	Note 2	-	-	V	1
VIL.CA(AC100)	AC input logic low	Note 2	VREF - 0.1	-	-	V	1
VIH.CA(AC90)	AC input logic high	-	-	VREF + 0.09	Note 2	V	1
VIL.CA(AC90)	AC input logic low	-	-	Note 2	VREF - 0.09	V	1
VREFCA(DC)	Reference voltage for ADD, CMD inputs	0.49*VDD	0.51*VDD	0.49*VDD	0.51*VDD	V	2,3

Note:

1. See “Overshoot and Undershoot Specifications”
2. The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1%VDD (for reference: approx. ± 12mV)
3. For reference: approx. VDD/2 ± 12 mV

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7.2 AC and DC Logic Input Measurement Levels: Vref Tolerances

The DC-tolerance limits and AC-noise limits for the reference voltages VrefCA is illustrated in the Figure 7-1 below. It shows a valid reference voltage Vref(t) as a function of time. (Vref stands for VrefCA).

Vref(DC) is the linear average of Vref(t) over a very long period of time (for example, 1 second). This average has to meet the min/max requirement in Figure 7-1. Furthermore Vref(t) may temporarily deviate from Vref(DC) by no more than ± 1% VDD

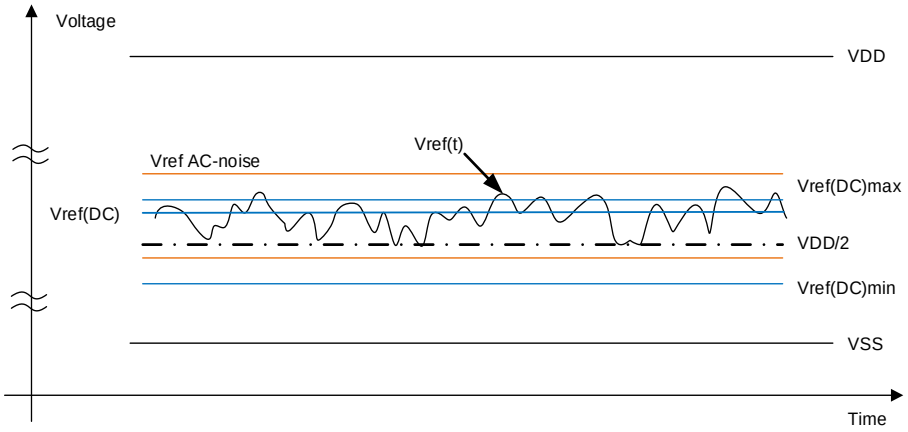


Figure 7-1. Illustration of Vref(DC) Tolerance and Vref AC-noise Limits

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on Vref.

"Vref" should be understood as Vref(DC)

This clarifies that DC-variations of Vref affect the absolute voltage a signal has to reach to achieve a valid high or low level, and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for Vref(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with Vref AC-noise. Timing and voltage effects due to AC-noise on Vref up to the specified limit (± 1% of VDD) are included in DRAM timings and their associated deratings.

7.3 AC and DC Logic Input Levels for Differential Signals

7.3.1 AC and DC Logic Input Levels for Differential Signals

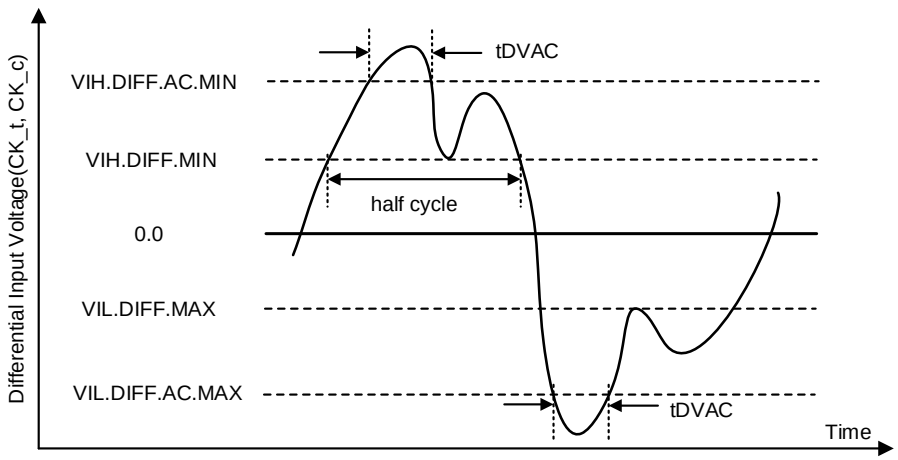


Figure 7-2. Definition of Differential AC-Swing and "Time above AC-Level" tDVAC

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Note:

1. Differential signal rising edge from VIL.DIFF.MAX to VIH.DIFF.MIN must be monotonic slope.
2. Differential signal falling edge from VIH.DIFF.MIN to VIL.DIFF.MAX must be monotonic slope.

7.3.2 Differential Swing Requirements for Clock (CK_t - CK_c)

Table 7-2. Differential Input Levels Requirements for CK_t - CK_c

Symbol	Parameter	1600/1866/2133		2400/2666		3200		Unit	Note
		Min	Max	Min	Max	Min	Max		
VIHdiff	differential input high	+ 0.150	Note 3	+ 0.135	Note 3	+ 0.110	Note 3	V	1
VILdiff	differential input low	Note 3	- 0.150	Note 3	- 0.135	Note 3	- 0.110	V	1
VIHdiff(AC)	differential input high ad	2 x (VIH(AC) - VREF	Note 3	2 x (VIH(AC) - VREF	Note 3	2 x (VIH(AC) - VREF	Note 3	V	2
VILdiff(AC)	differential input low ac	Note 3	2 x (VIL(AC) - VREF	Note 3	2 x (VIL(AC) - VREF	Note 3	2 x (VIL(AC) - VREF	V	2

Note:

1. Used to define a differential signal slew-rate.
2. for CK_t - CK_c use VIH.CA/VIL.CA(AC) of ADD/CMD and VREFCA;
3. These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits (VIH.CA(DC) max, VIL.CA(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

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Table 7-3. Allowed Time before Ringback (tDVAC) for CK_t - CK_c

Slew Rate [V/ns]	tDVAC [ps] @ |VIH/Ldiff(AC)| = 200mV		tDVAC [ps] @ |VIH/Ldiff(AC)| = TBDmV	
	Min	Max	Min	Max
> 4.0	120	-	TBD	-
4.0	115	-	TBD	-
3.0	110	-	TBD	-
2.0	105	-	TBD	-
1.8	100	-	TBD	-
1.6	95	-	TBD	-
1.4	90	-	TBD	-
1.2	85	-	TBD	-
1.0	80	-	TBD	-
<1.0	80	-	TBD	-

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7.3.3 Differential Swing Requirements for Clock (CK_t - CK_c)

Each individual component of a differential signal (CK_t, CK_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c have to approximately reach VSEHmin/VSELmax (approximately equal to the ac-levels (VIH.CA(ac)/VIL.CA(ac)) for ADD/CMD signals) in every half-cycle.

Note that the applicable ac-levels for ADD/CMD might be different per speed-bin etc. E.g., if different value than VIH.CA(AC100)/VIL.CA(AC100) is used for ADD/CMD signals, then these ac- levels apply also for the single-ended signals CK_t and CK_c.

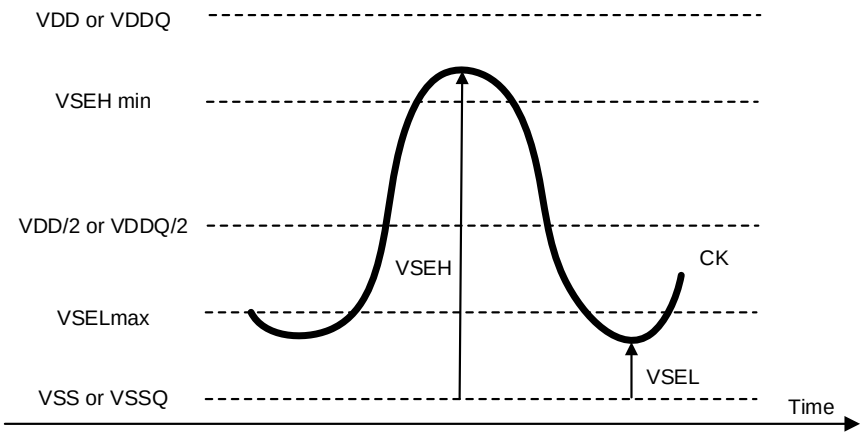


Figure 7-3. Single-ended Requirement for CK

Note that, while ADD/CMD signal requirements are with respect to VrefCA, the single-ended components of differential signals have a requirement with respect to VDD/2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 7-4. Single-ended Levels Requirements for CK_t, CK_c

Symbol	Parameter	1600/1866/2133		2400/2666		3200		Unit	Note
		Min	Max	Min	Max	Min	Max		
VSEH	Single-ended high-level for CK_t / CK_c	VDD/2 + 0.1	Note 3	VDD/2 + 0.095	Note 3	VDD/2 + 0.085	Note 3	V	1,2
VSEL	Single-ended low-level for CK_t / CK_c	Note 3	VDD/2 - 0.1	Note 3	VDD/2 - 0.095	Note 3	VDD/2 - 0.085	V	1,2

Note

1. For CK_t-CK_c use VIH.CA/VIL.CA(AC) of ADD/CMD.
2. VIH(AC)/VIL(AC) for ADD/CMD is based on VREFCA.
3. These values are not defined, however the single-ended signals CK_t, CK_c need to be within the respective limits (VIH.CA(DC) max, VIL.CA(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

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7.3.4 Address, Command, and Control Overshoot/Undershoot Specifications

Table 7-5. AC Overshoot/Undershoot Specification for Address, Command, and Control Pins

Parameter	Symbol	1600/1866/2133/2400				2666/3200	Unit	Note
Maximum peak amplitude above V_{AOS}	V_{AOSP}	0.06					V	
Upper boundary of overshoot area A_{AOS1}	V_{AOS}	VDD + 0.24					V	1
Maximum peak amplitude allowed for undershoot	VAUS	0.3					V	
Maximum overshoot area per 1tCK Above V_{AOS}	A_{AOS2}	0.0083	0.0071	0.0062	0.0055	0.0055	V-ns	
Maximum overshoot area per 1tCK Between VDD and V_{AOS}	A_{AOS1}	0.255	0.2185	0.1914	0.1699	0.1699	V-ns	
Maximum undershoot area per 1tCK Below VSS	A_{AUS}	0.2644	0.2265	0.1984	0.1762	0.1762	V-ns	
(A0-A13,A17,BG0-BG1,BA0-BA1,ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,CS_n,CKE,ODT,C2-C0)								

Note:

1. The value of VAOS matches VDD absolute max as defined in Table 6-1 if VDD equals VDD max as defined in Table 6-1. If VDD is above the recommended operating conditions, VAOS remains at VDD absolute max as defined in Table 6-1.

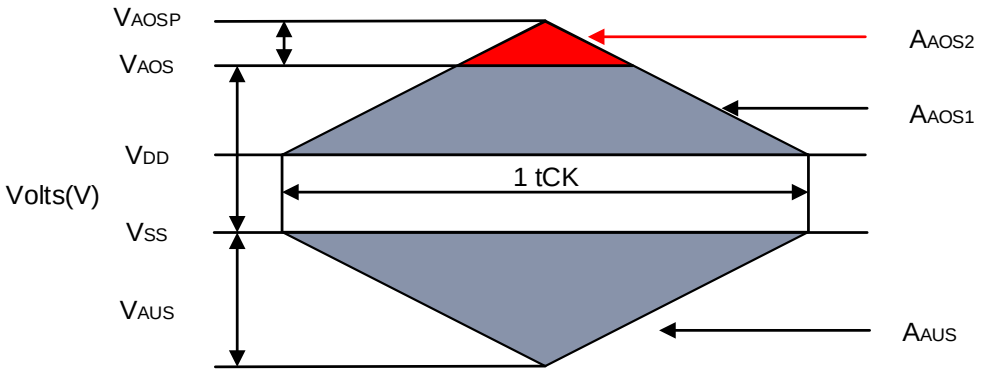


Figure 7-4. Address, Command, and Control Overshoot and Undershoot Definition

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7.3.5 Address, Command, and Control Overshoot/Undershoot Specifications

Table 7-6. AC Overshoot/Undershoot Specification for Clock

Parameter	Symbol	1600/1866/2133/2400/2666/3200						Unit	Note
Maximum peak amplitude above V_{COS}	V_{COSP}	0.06						V	
Upper boundary of overshoot area A_{COS1}	V_{COS}	VDD + 0.24						V	1
Maximum peak amplitude allowed for undershoot	V_{CUS}	0.3						V	
Maximum overshoot area per UI Above V_{COS}	A_{COS2}	0.0038	0.0032	0.0028	0.0025	0.0025	0.0025	V-ns	
Maximum overshoot area per 1tCK Between VDD and V_{COS}	A_{COS1}	0.1125	0.0964	0.0844	0.075	0.075	0.075	V-ns	
Maximum undershoot area per UI Below VSS	A_{CUS}	0.1144	0.098	0.0858	0.0762	0.0762	0.0762	V-ns	
(CK_t, CK_c)									

Note:

The value of VAOS matches VDD absolute max as defined in Table 6-1 if VDD equals VDD max as defined in Table 6-2. If VDD is above the recommended operating conditions, VAOS remains at VDD absolute max as defined in Table 6-1.

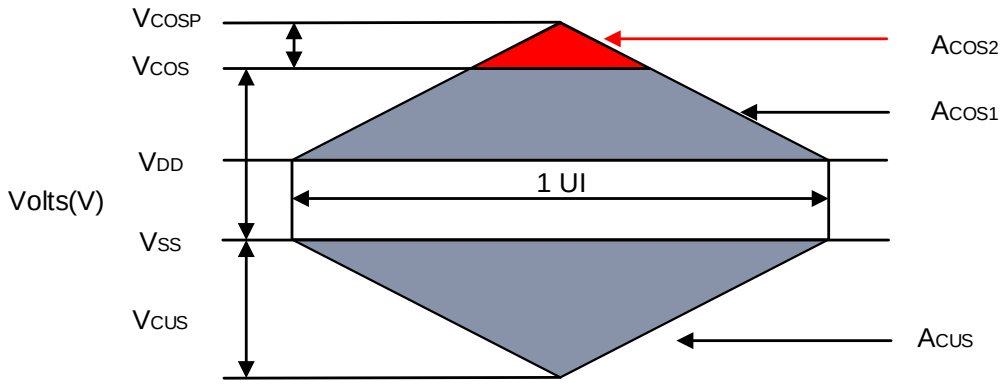


Figure 7-5. Clock Overshoot and Undershoot Definition

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7.3.6 Data, Strobe and Mask Overshoot/Undershoot Specifications

Table 7-7. AC Overshoot/Undershoot Specification for Clock

Parameter	Symbol	1600/1866/2133/2400/2666/3200						Unit	Note
Maximum peak amplitude above V_{DOS}	V_{DOSP}	0.16						V	
Upper boundary of overshoot area A_{DOS1}	V_{DOS}	VDD + 0.24						V	1
Lower boundary of undershoot area A_{DUS1}	V_{DUS}	0.3						V	2
Maximum peak amplitude below V_{DUS}	A_{DUSP}	0.1						V-ns	
Maximum overshoot area per UI Above V_{DOS}	A_{DOS2}	0.0150	0.0129	0.0113	0.0100	0.0100	0.0100	V-ns	
Maximum overshoot area per 1UI Between VDDQ and V_{DOS}	A_{DOS1}	0.1050	0.0900	0.0788	0.0700	0.0700	0.0700	V-ns	
Maximum undershoot area per UI Between VSSQ and A_{DUS1}	A_{DUS1}	0.1050	0.0900	0.0788	0.0700	0.0700	0.0700	V-ns	
Maximum undershoot area per 1 UI below VDUS	A_{DUS2}	0.0150	0.0129	0.0113	0.0100	0.100	0.100	V-ns	
(DQ, DQS_t, DQS_c, DM_n, DBI_n, TDQS_t, TDQS_c)									

Note:

1. The value of VDOS matches (VIN, VOUT) max as defined in Table 6-1 if VDDQ equals VDDQ max as defined Table 6-2. If VDDQ is above the recommended operating conditions, VDOS remains at (VIN, VOUT) max as defined in Table 6-1.
2. The value of VDUS matches (VIN, VOUT) min as defined in Table 6-1.

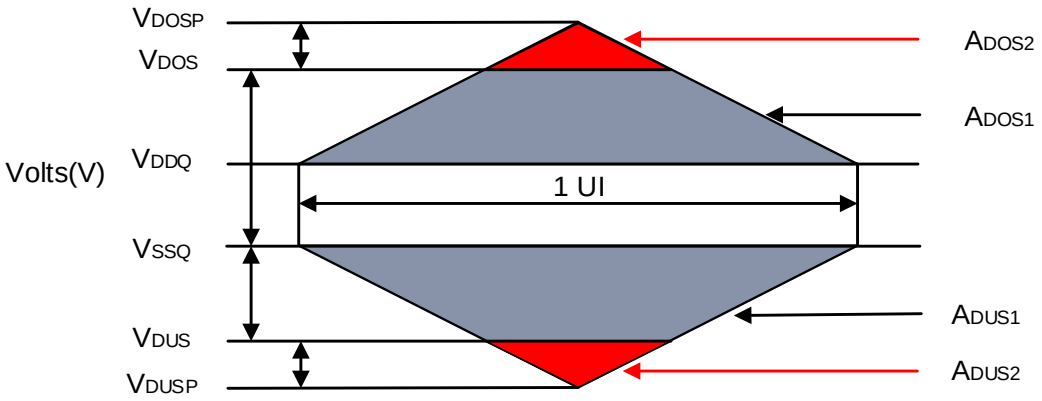


Figure 7-6. Data, Strobe and Mask Overshoot and Undershoot Definition

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7.4 Slew Rate Definitions for Differential Input Signals

7.4.1 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Table 7-8 andFigure 7-7.

Table 7-8. CK Differential Input Slew Rate Definition

Description	From	To	Defined by
Differential input slew rate for rising edge (CK_t-CK_c)	VILdiffmax	VIHdiffmin	[VIHdiffmin-VILdiffmax]/DeltaTRdiff
Differential input slew rate for falling edge (CK_t-CK_c)	VIHdiffmin	VILdiffmax	[VIHdiffmin -VILdiffmax]/DeltaTFdiff

Note:

1. The differential signal (i, e., CK_t-CK_c) must be linear between these thresholds.

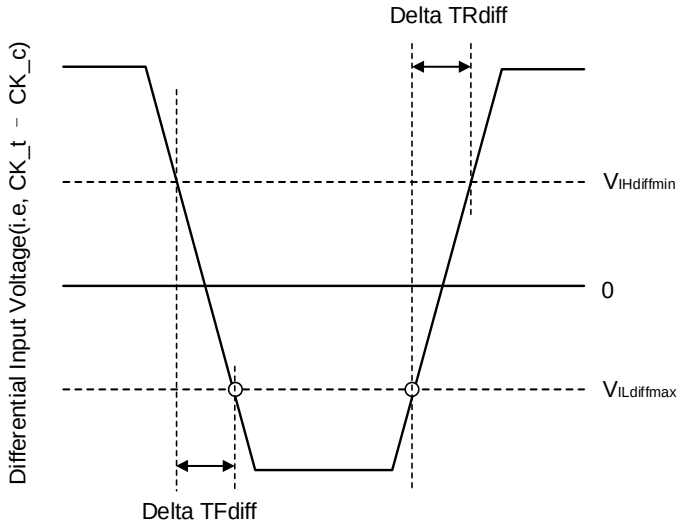
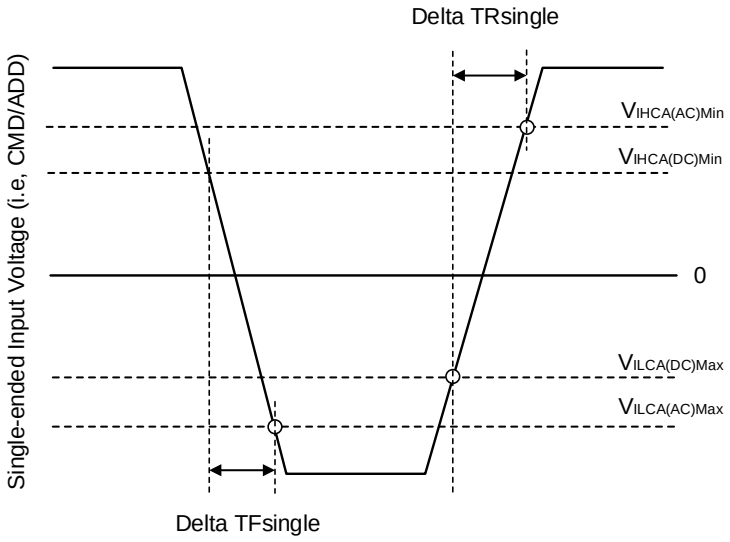


Figure 7-7. Differential Input Slew Rate Definition for CK_t, CK_c

7.4.2 Slew Rate Definitions for Differential Input Signals (CMD/ADD)



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Figure 7-8. Single-ended Input Slew Rate Definition for CMD and ADD

Note:

1. Single-ended input slew rate for rising edge = {VIHCA(AC)Min - VILCA(DC)Max} / Delta TR single.
2. Single-ended input slew rate for falling edge = {VIHCA(DC)Min - VILCA(AC)Max} / Delta TF single.
3. Single-ended signal rising edge from VILCA(DC)Max to VIHCA(DC)Min must be monotonic slope.
4. Single-ended signal falling edge from VIHCA(DC)Min to VILCA(DC)Max must be monotonic slope.

7.5 CK Differential Input Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in. The differential input cross point voltage Vix is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

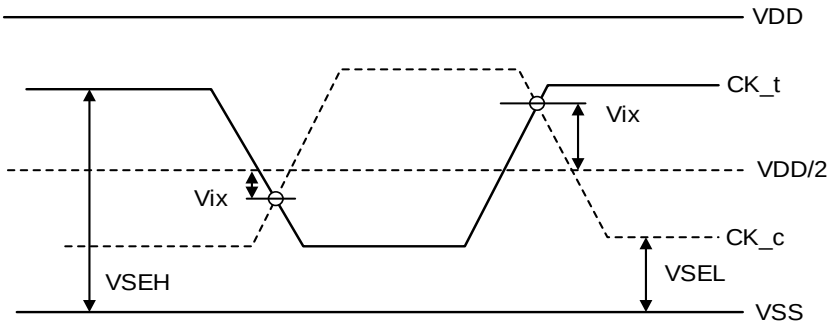


Figure 7-9. Vix Definition (CK)

Table 7-9. Cross Point Voltage for CK Differential Input Signals at DDR4-1666 through DDR4-2400

Symbol	Parameter	Input Level	DDR4 – 1666/1866/2133/2400	
			Min	Max
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	VSEH > VDD/2 + 145 mV	N/A	120mV
		VDD/2 + 100mV ≤ VSEH ≤ VDD/2 + 145 mV	N/A	(VSEH-VDD/2) – 25mV
		VDD/2 - 145 mV ≤ VSEL ≤ VDD/2 – 100 mV	- (VDD/2-VSEL) + 25mV	N/A
		VSEL < VDD/2 - 145mV	-120mV	N/A

Table 7-10. Cross Point Voltage for CK Differential Input Signals at DDR4-2666

Symbol	Parameter	Input Level	DDR4 – 2666/3200	
			Min	Max
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	VSEH > VDD/2 + 145 mV	N/A	110mV
		VDD/2 + 90mV ≤ VSEH ≤ VDD/2 + 145 mV	N/A	(VSEH-VDD/2) – 30mV
		VDD/2 - 145 mV ≤ VSEL ≤ VDD/2 – 90 mV	- (VDD/2-VSEL) + 30mV	N/A
		VSEL < VDD/2 - 145mV	-110mV	N/A

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7.6 CMOS Rail to Rail Input Levels for RESET_n

Table 7-11. CMOS Rail to Rail Input Levels for RESET_n

Parameter	Symbol	Min	Max	Unit	Note
AC Input High Voltage	VIH(AC)_RESET	0.8*VDD	VDD	V	6
DC Input High Voltage	VIH(DC)_RESET	0.7*VDD	VDD	V	2
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2VDD	V	7
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3VDD	V	1
Rising Time	TR_RESET	-	1.0	μs	4
RESET Pulse Width	tPW_RESET	1.0	-	μs	3,5

Note:

1. After RESET_n is registered Low, RESET_n level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, SDRAM may not be reset.
2. Once RESET_n is registered High, RESET_n level must be maintained above VIH(DC)_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET_n signal Low.
3. RESET is destructive to data contents.
4. No slope reversal (ringback) requirement during its level transition from Low to High.
5. This definition is applied only “Reset Procedure at Power Stable”.
6. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
7. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

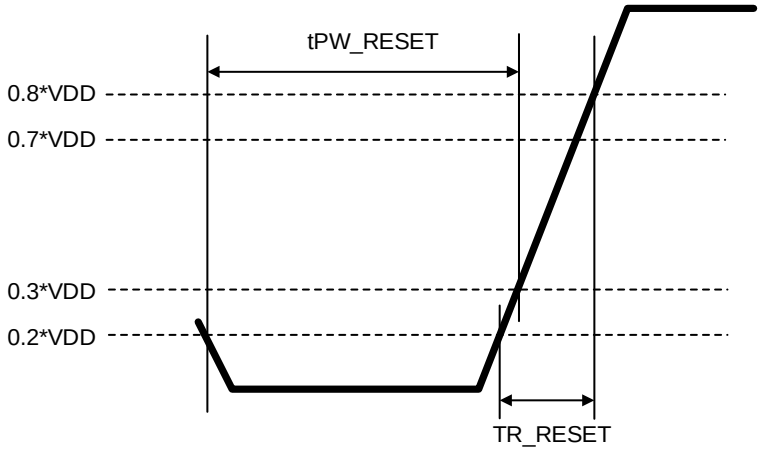


Figure 7-10. RESET_n Input Slew Rate Definition

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7.7 AC&DC Logic Input Levels for DQS Signals

7.7.1 Differential Signal Definition

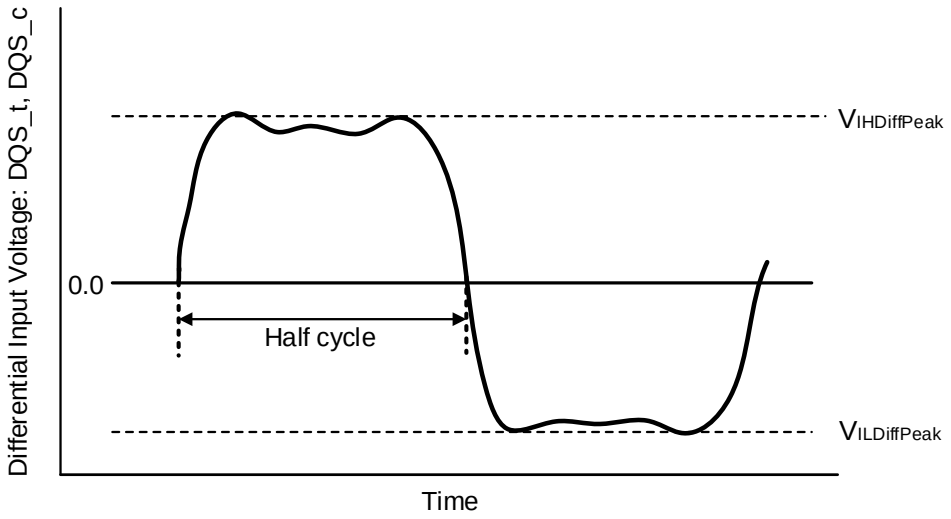


Figure 7-11 DQS Differential Input Signal AC-swing Level

7.7.2 Differential Swing Requirements for DQS (DQS_t – DQS_c)

Table 7-12. Differential Input Swing Requirements for DQS

Symbol	Parameter	1600/1866/2133		2400		2666		3200		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
VIHDiffPeak	VIH.DIFF.Peak Voltage	186	Note2	160	Note2	150	Note2	140	Note2	mV	1
VILDiffPeak	VIL.DIFF.Peak Voltage	Note2	-186	Note2	-160	Note2	-150	Note2	-140	mV	1

Note:

1. Used to define a differential signal slew-rate.
2. These values are not defined; however, the differential signals DQS_t - DQS_c, need to be within the respective limits of Overshoot, Undershoot Specification for single-ended signals.

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7.7.3 Peak Voltage Calculation Method

The peak voltage of Differential DQS signals are calculated in a following equation.

VIH.DIFF.Peak Voltage = Max(f(t))

VIL.DIFF.Peak Voltage = Min(f(t))

f(t) = VDQS_t - VDQS_c

The Max(f(t)) or Min(f(t)) used to determine the midpoint which to reference the +/-35% window of the exempt non-monotonic signaling shall be the smallest peak voltage observed in all UI's.

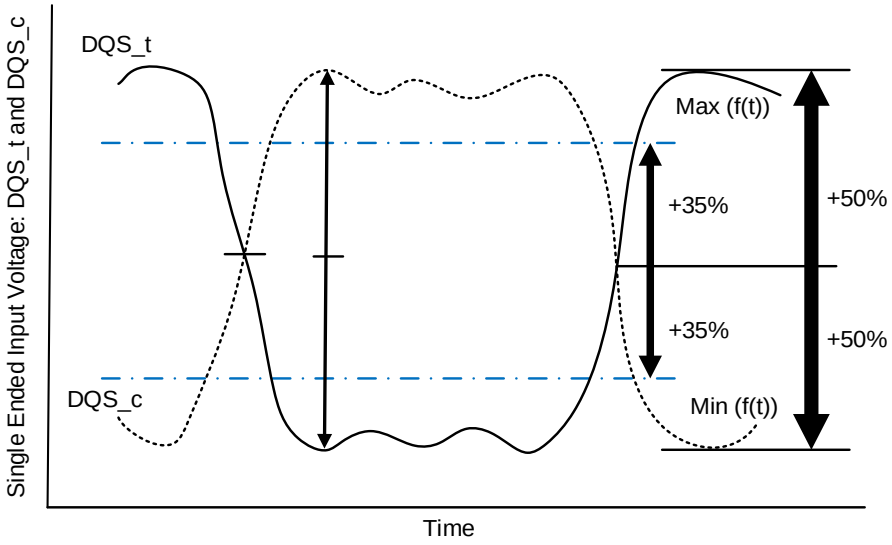


Figure 7-12. Definition of Differential DQS Peak Voltage and Range of Exempt Nonmonotonic Signaling

7.7.4 Differential Input Cross Point Voltage

To achieve tight RxMask input requirements as well as output skew parameters with respect to strobe, the cross point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in Table 7-13. The differential input cross point voltage VIX_DQS (VIX_DQS_FR and VIX_DQS_RF) is measured from the actual cross point of DQS_t, DQS_c relative to the VDQSmid of the DQS_t and DQS_c signals.

VDQSmid is the midpoint of the minimum levels achieved by the transitioning DQS_t and DQS_c signals, and noted by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.

A nonmonotonic transitioning signal's ledge is exempt or not used in determination of a horizontal tangent provided the said ledge occurs within +/- 35% of the midpoint of either VIH.DIFF. Peak Voltage (DQS_t rising) or VIL.DIFF.Peak Voltage (DQS_c rising), refer to Figure 7-12. A secondary horizontal tangent resulting from a ring-back transition is also exempt in determination of a horizontal tangent. That is, a falling transition's horizontal tangent is derived from its negative slope to zero slope transition (point A in Figure 7-13) and a ring-back's horizontal tangent derived from its positive slope to zero slope transition (point B in Figure 7-13) is not a valid horizontal tangent; and a rising transition's horizontal tangent is derived from its positive slope to zero slope transition (point C in Figure 7-13) and a ring-back's horizontal tangent derived from its negative slope to zero slope transition (point D in Figure 7-13) is not a valid horizontal tangent.

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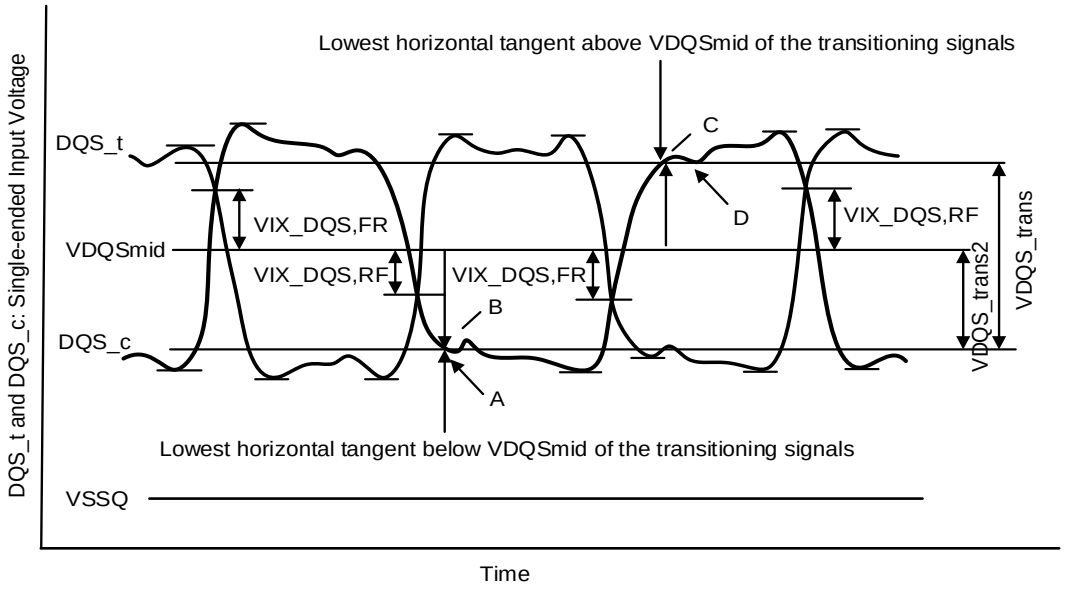


Figure 7-13. Vix Definition (DQS)

Table 7-13. Cross Point Voltage for DQS Differential Input Signals

Symbol	Parameter	1600/1866/2133/2400/2666/3200		Unit	Note
		Min	Max		
Vix_DQS_ratio	DQS Differential input crosspoint voltage ratio	-	25	%	1,2
VDQSmid_to_Vcent	VDQSmid offset relative to Vcent_DQ(midpoint)	-	min(VIHdiff,50)	mV	3,4,5

Note:

1. Vix_DQS_Ratio is DQS Vix crossing (Vix_DQS_FR or Vix_DQS_RF) divided by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.
2. VDQSmid will be similar to the VREFDQ internal setting value obtained during Vref Training if the DQS and DQs drivers and paths are matched.
3. The maximum limit shall not exceed the smaller of VIHdiff minimum limit or 50mV.
4. Vix measurements are only applicable for transitioning DQS_t and DQS_c signals when toggling data, preamble and high-z states are not applicable conditions.
5 The parameter VDQSmid is defined for simulation and ATE testing purposes, it is not expected to be tested in a system.

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7.7.5 Differential Input Slew Rate Definition

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown in Figure 7-14 and Table 7-14.

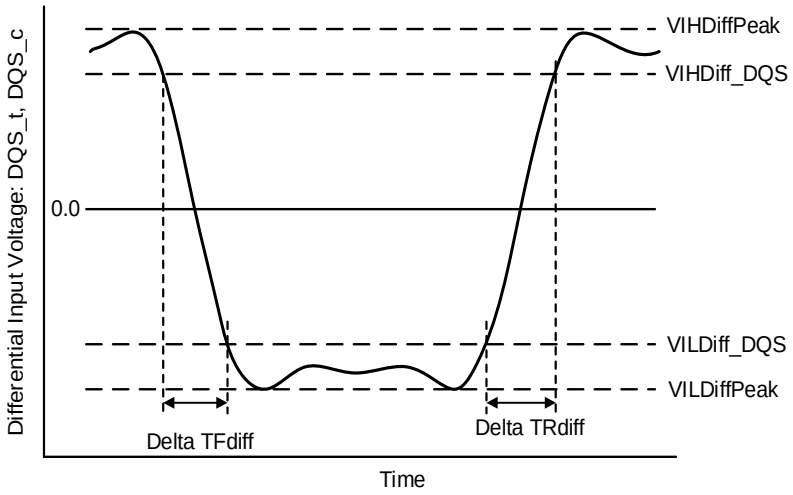


Figure 7-14. Differential Input Slew Rate Definition for DQS_t, DQS_c

Note:

1. Differential signal rising edge from VILDiff_DQS to VIHDiff_DQS must be monotonic slope.
2. Differential signal falling edge from VIHDiff_DQS to VILDiff_DQS must be monotonic slope.

Table 7-14. Differential Input Slew Rate Definition for DQS_t, DQS_c

Description	From	To	Defined by
Differential input slew rate for rising edge(DQS_t – DQS_c)	VILdiff_DQS	VIHdiff_DQS	|VILDiff_DQS - VIHDiff_DQS|/DeltaTRdiff
Differential input slew rate for falling edge(DQS_t – DQS_c)	VIHdiff_DQS	VILdiff_DQS	|VILDiff_DQS - VIHDiff_DQS|/DeltaTRdiff

Table 7-15. Differential Input Level for DQS_t, DQS_c

Symbol	Parameter	1600/1866/2133		2400/2666		Unit
		Min	Max	Min	Max	
VIHdiff_DQS	DC input logic high	136	-	130	-	mV
VILdiff_DQS	DC input logic low	-	-136	-	-130	mV

Table 7-16. Differential Input Slew Rate for DQS_t, DQS_c

Symbol	Parameter	1600/1866/2133/2400		2666/3200		Unit
		Min	Max	Min	Max	
SRIdiff	Differential input slew rate	3	18	2.5	18	V/ns

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8 AC&DC OUTPUT MEASUREMENT LEVELS

8.1 Output Driver DC Electronic Characteristics

The DDR4 driver supports two different RON values. These RON values are referred as strong (low RON) and weak mode (high RON). A functional representation of the output buffer is shown in Figure 8-1 below. Output driver impedance RON is defined as the individual pull-up and pull- down resistors (RON_{Pu} and RON_{Pd}).

$RON_{Pu} = \frac{VDDQ-Vout}{|Iout|}$ under the condition that RON_{Pd} is off

$RON_{Pd} = \frac{Vout}{|Iout|}$ under the condition that RON_{Pu} is off.

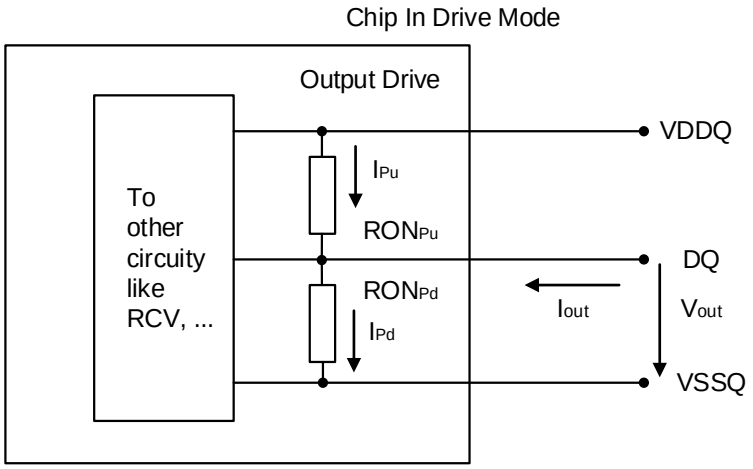


Figure 8-1. Output Driver

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Table 8-1. Output Driver DC Electronical Characteristics, Assuming RZQ = 240ohm; Entire Operating Temperature Range; after Proper ZQ Calibration

RONNOM	Resistor	Vout	Min	Nom	Max	Unit	Note
34Ω	RON34Pd	VOLdc=0.5*VDDQ	0.73	1.0	1.1	RZQ/7	1,2
		VOMdc=0.8*VDDQ	0.83	1.0	1.1	RZQ/7	1,2
		VOHdc=1.1*VDDQ	0.83	1.0	1.25	RZQ/7	1,2
	RON34Pu	VOLdc=0.5*VDDQ	0.9	1.0	1.25	RZQ/7	1,2
		VOMdc=0.8*VDDQ	0.9	1.0	1.1	RZQ/7	1,2
		VOHdc=1.1*VDDQ	0.8	1.0	1.1	RZQ/7	1,2
48Ω	RON48Pd	VOLdc=0.5*VDDQ	0.73	1.0	1.1	RZQ/5	1,2
		VOMdc=0.8*VDDQ	0.83	1.0	1.1	RZQ/5	1,2
		VOHdc=1.1*VDDQ	0.83	1.0	1.25	RZQ/5	1,2
	RON48Pu	VOLdc=0.5*VDDQ	0.9	1.0	1.25	RZQ/5	1,2
		VOMdc=0.8*VDDQ	0.9	1.0	1.1	RZQ/5	1,2
		VOHdc=1.1*VDDQ	0.8	1.0	1.1	RZQ/5	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc=0.8*VDDQ	-10		17	%	1,2,3,4
Mismatch DQ-DQ within byte variation pull-up, MMPudd		VOMdc=0.8*VDDQ			10	%	1,2,4
Mismatch DQ-DQ within byte variation pull-up, MMPddd		VOMdc=0.8*VDDQ			10	%	1,2,4

Note:

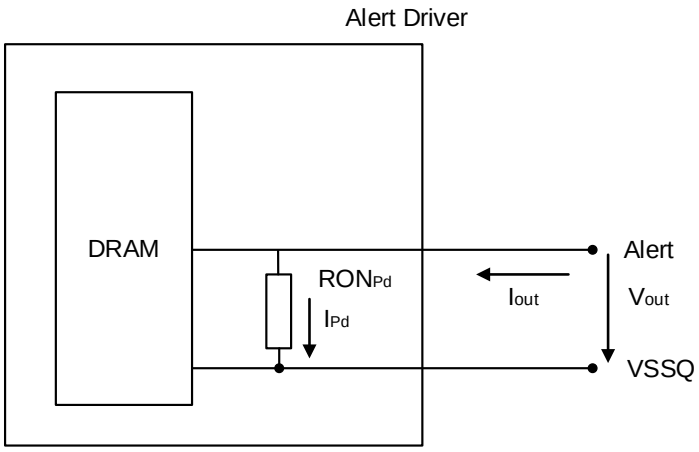
1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity (TBD).
2. Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5*VDDQ and 1.1*VDDQ.
3. Measurement definition for mismatch between pull-up and pull-down, MMPuPd: Measure RONPu and RONPD both at 0.8*VDD separately; RONnom is the nominal RON value.
4. MMPuPdd =[(RONPu–RONPd/RONNOM)] * 100
5. RON variance range ratio to RON Nominal value in a given component, including DQS_t and DQS_c.
6. MMPuPdd =[(RONPuMax–RONPuMin/RONNOM)] * 100
7. MMPdPdd =[(RONPdMax–RONPdMin/RONNOM)] * 100
8. This parameter of x16 device is specified for Upper byte and Lower byte.

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8.1.1 Alert_n Output Driver Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

$RON_{Pd} = \frac{Vout}{|Iout|}$ under the condition that RON_{Pu} is off.



Resister	Vout	Min	Max	Unit	Note
RON_{Pd}	VOL_{dc}=0.1*VDDQ	0.3	1.2	34Ω	1
	VOM_{dc}=0.8*VDDQ	0.4	1.2	34Ω	1
	VOH_{dc}=1.1*VDDQ	0.4	1.4	34Ω	1

Note:

VDDQ voltage is at VDDQ DC. VDDQ DC definition is TBD.

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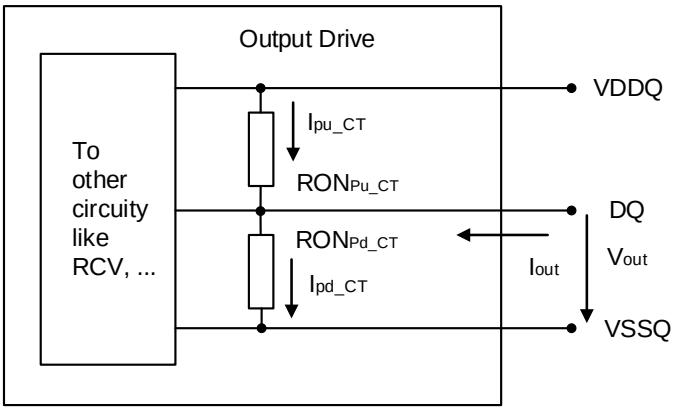
8.1.2 Output Driver Characteristic of Connectivity Test (CT) Mode

Following output driver impedance RON will be applied Test Output Pin during Connectivity Test (CT) Mode. The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows:

$$RON_{Pu_CT} = \frac{VDDQ\text{-}Vout}{|\,Iout\,|}$$

$$RON_{Pd_CT} = \frac{Vout}{|\,Iout\,|}$$

Chip In Drive Mode



RON_{NOM_CT}	Resister	Vout	Max	Unit
34Ω	RON_{Pd_CT}	$VOB_{dc}=0.2*V_{DDQ}$	1.9	34Ω
		$VOL_{dc}=0.5*V_{DDQ}$	2.0	34Ω
		$VOM_{dc}=0.8*V_{DDQ}$	2.2	34Ω
		$VOH_{dc}=1.1*V_{DDQ}$	2.5	34Ω
	RON_{Pu_CT}	$VOB_{dc}=0.2*V_{DDQ}$	2.5	34Ω
		$VOL_{dc}=0.5*V_{DDQ}$	2.2	34Ω
		$VOM_{dc}=0.8*V_{DDQ}$	2.0	34Ω
		$VOH_{dc}=1.1*V_{DDQ}$	1.9	34Ω

Note:

Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.

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8.2 Single-ended AC& DC Output Levels

Table 8-2. Single-ended AC&DC Output Levels

Symbol	Parameter	DDR4-1600 to DDR4-3200	Unit
V_{OH}(DC)	DC output high measurement level (for IV curve linearity)	1.1 x V_{DDQ}	V
V_{OM}(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V
V_{OL}(DC)	DC output low measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V
V_{OH}(AC)	AC output high measurement level (for output SR)	(0.7+0.15) x V_{DDQ}	V
V_{OL}(AC)	AC output low measurement level (for output SR)	(0.7-0.15) x V_{DDQ}	V

Note:

The swing of ± 0.15 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ.

8.3 Differential AC&DC Output Levels

Table 8-3. Differential AC&DC Output Levels

Symbol	Parameter	DDR4-1600 to DDR4-3200	Unit
V_{OHdiff}(AC)	AC differential output high measurement level (for output SR)	+ 0.3 x V_{DDQ}	V
V_{OLdiff}(AC)	AC differential output low measurement level (for output SR)	-0.3 x V_{DDQ}	V

Note:

The swing of ± 0.3 × V_{DDQ} is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V_{TT} = V_{DDQ} at each of the differential outputs.

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8.4 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OL}(AC) and V_{OH}(AC) for single ended signals as shown in Table 8-4 and Figure 8-2.

Table 8-4. Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	V_{OL}(AC)	V_{OH}(AC)	[V_{OH}(AC)- V_{OL}(AC)]/Delta TRse
Single ended output slew rate for falling edge	V_{OH}(AC)	V_{OL}(AC)	[V_{OH}(AC)- V_{OL}(AC)]/Delta TFse

Note:

Output slew rate is verified by designed and characterization, and may not be subject to production test.

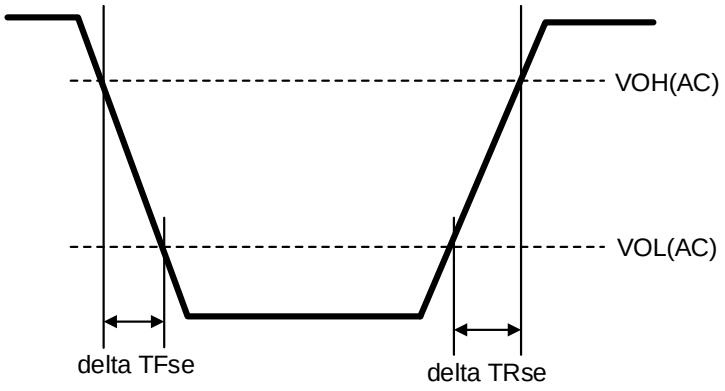


Figure 8-2. Single-ended Output Slew Rate Definition

Table 8-5. Single-ended Output Slew Rate

Parameter	Symbol	DDR4-1600 to DDR4-3200		Unit
		Min	Max	
Single ended output slew rate	SRQse	4	9	V/ns

Description:

SR: Slew Rate; Q: Query Output (like in DQ, which stands for Data-in, Query-Output) se: Single-ended Singnals; For RON = RZQ/7 setting

Note:

In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.

- Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).
- Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies).

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8.5 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 8-6 and Figure 8-3.

Table 8-6. Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	V_{OLdiff}(AC)	V_{OHdiff}(AC)	[V_{OHdiff}(AC)- V_{OLdiff}(AC)]/Delta TRdiff
Differential output slew rate for falling edge	V_{OHdiff}(AC)	V_{OLdiff}(AC)	[V_{OHdiff}(AC)- V_{OLdiff}(AC)]/Delta TFdiff

Note:

Output slew rate is verified by design and characterization, and may not be subject to production test.

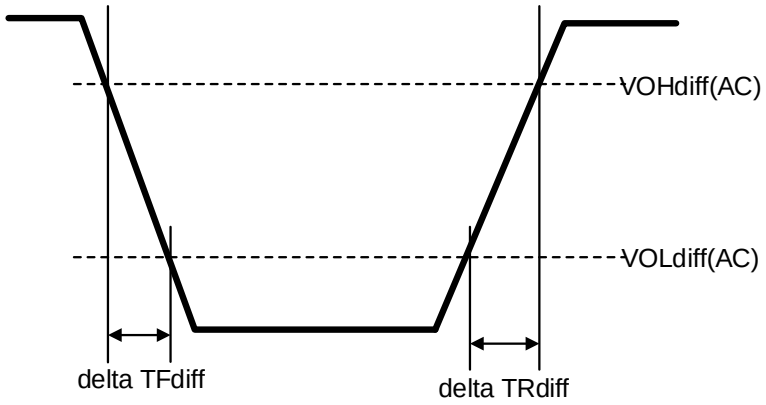


Figure 8-3. Differential Output Slew Rate Definition

Table 8-7. Differential Output Slew Rate

Parameter	Symbol	DDR4-1600 to DDR4-3200		Unit
		Min	Max	
Differential output slew rate	SRQdiff	8	18	V/ns

Description:

SR: Slew Rate; Q: Query Output (like in DQ, which stands for Data-in, Query-Output);

Diff: Differential Singnals; For RON = RZQ/7 setting

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8.6 Single-ended AC& DC Output Levels of Connectivity Test Mode

Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

Table 8-8. Single-ended AC&DC Output Level of Connectivity Test Mode

Symbol	Parameter	DDR4-1600 to DDR4-3200	Unit	Note
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	1.1 x V_{DDQ}	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
$V_{OB(DC)}$	DC output below measurement level (for IV curve linearity)	0.2 x V_{DDQ}	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	V_{TT} + (0.1 x V_{DDQ})	V	1
$V_{OL(AC)}$	AC output below measurement level (for output SR)	V_{TT} - (0.1 x V_{DDQ})	V	1

Note:

The effective test load is 50Ω terminated by VTT = 0.5*V_{DDQ}.

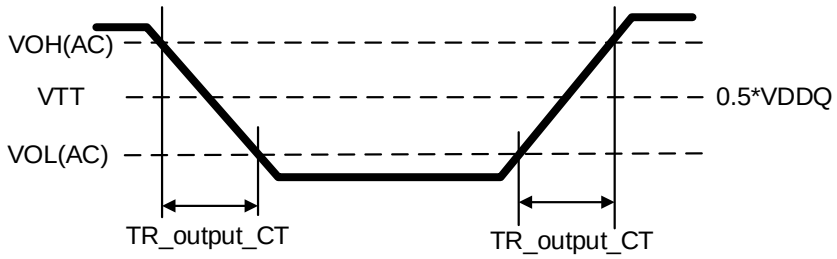


Figure 8-4. Output Slew Rate Definition of Connectivity Test Mode

Table 8-9. Single-ended Output Slew Rate of Connectivity Test Mode

Parameter	Symbol	DDR4-1600 to DDR4-3200		Unit
		Min	Max	
Output signal Falling time	TF_output_CT	-	10	ns/V
Output signal Rising time	TR_output_CT	-	10	ns/V

8.7 Reference Load for Connectivity Test Mode Timing

The reference load for ODT timings is defined in Figure 8-5.

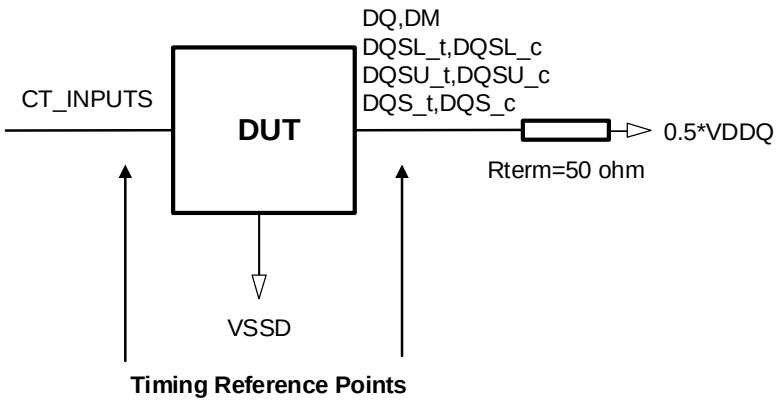


Figure 8-5. Connectivity Test Mode Timing Reference Load

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9 SPEED BIN

9.1 DDR4-1600 Speed Bins and Operations

Table 9-1. DDR4-1600 Speed Bins and Operations

Speed Bin				DDR4-1600		Unit	Note
CL-nRCD-nRP				11-11-11			
Parameter			Symbol	Min	Max		
Internal Read command to first data			tAA	13.75[13] (13.50)[5,11]	18	ns	11
Internal Read command to first data with Read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(max) + 2nCK	ns	11
ACT to internal Read or write delay time			tRCD	13.75[13] (13.50)[5,11]	-	ns	11
PRE command period			tRP	13.75 (13.50)[5,11]	-	ns	11
ACT to PRE command period			tRAS	35	9 x tREFI	ns	11
ACT to ACT or REF command period			tRC	48.75 (48.50)[5,11]	-	ns	11
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	1.5 (Optional)[5]	1.6	ns	1,2,3,4,10,13
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,10
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3
Supported CL Settings				(9),11,12		nCK	12,13
Supported CL Settings with Read DBI				(11),13,14		nCK	12
Supported CWL Settings				9,11		nCK	

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9.2 DDR4-1866 Speed Bins and Operations

Table 9-2. DDR4-1866 Speed Bins and Operations

Speed Bin				DDR4-1866		Unit	Note
CL-nRCD-nRP				13-13-13			
Parameter			Symbol	Min	Max		
Internal Read command to first data			tAA	13.92[13] (13.50)[5,11]	18	ns	11
Internal Read command to first data with Read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(max) + 2nCK	ns	11
ACT to internal Read or write delay time			tRCD	13.92 (13.50)[5,11]	-	ns	11
PRE command period			tRP	13.92 (13.50)[5,11]	-	ns	11
ACT to PRE command period			tRAS	34	9 x tREFI	ns	11
ACT to ACT or REF command period			tRC	47.92 (47.50)[5,11]	-	ns	11
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	1.5 (Optional)[5]	1.6	ns	1,2,3,4,10,13
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,10
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25 (Optional)[5,11]	<1.5	ns	1,2,3,4,6
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3
Supported CL Settings				(9), (11),12,13,14		nCK	12,13
Supported CL Settings with Read DBI				(11), (13),14,15,16		nCK	12
Supported CWL Settings				9,10,11,12		nCK	

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9.3 DDR4-2133 Speed Bins and Operations

Table 9-3. DDR4-2133 Speed Bins and Operations

Speed Bin				DDR4-2133		Unit	Note
CL-nRCD-nRP				15-15-15			
Parameter			Symbol	Min	Max		
Internal Read command to first data			tAA	14.06[13] (13.50)[5,11]	18	ns	12
Internal Read command to first data with Read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	12
ACT to internal Read or Write delay time			tRCD	14.06 (13.50)[5,11]	-	ns	12
PRE command period			tRP	14.06 (13.50)[5,11]	-	ns	12
ACT to PRE command period			tRAS	33	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	47.06 (46.50)[5,11]	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	1.5 (Optional)[5]	1.6	ns	1,2,3,4,11,14
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,11
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,7
	CL = 12	CL = 14	tCK(AVG)	(Optional)[5,11]			
				1.25	<1.5	ns	1,2,3,7
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,7
				(Optional)[5,11]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,7
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3
Supported CL Settings				(9),(11),12,(13),14,15,16		nCK	13,14
Supported CL Settings with Read DBI				(11),(13),14,(15),16,18,19		nCK	
Supported CWL Settings				9,10,11,12,14		nCK	

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9.4 DDR4-2400 Speed Bins and Operations

Table 9-4. DDR4-2400 Speed Bins and Operations

Speed Bin				DDR4-2400		Unit	Note
CL-nRCD-nRP				17-17-17			
Parameter			Symbol	Min	Max		
Internal Read command to first data			tAA	14.16 (13.75)[5,11]	18	ns	12
Internal Read command to first data with Read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	12
ACT to internal Read or write delay time			tRCD	14.16 (13.75)[5,11]	-	ns	12
PRE command period			tRP	14.16 (13.75)[5,11]	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	46.16 (45.75)[5,11]	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	Reserved / 1.5	1.6	ns	1,2,3,4,8,11
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,8,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved	(Optional)[5,11]	ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25 / (Optional)[5,11]	<1.5	ns	1,2,3,4,8
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071 / (Optional)[5,11]	<1.25	ns	1,2,3,4,8
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937 / (Optional)[5,11]	<1.071	ns	1,2,3,4,8
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
Supported CL Settings				10,(11),12,(13),14,(15),16,17,18		nCK	13
Supported CL Settings with Read DBI				12,(13),14,(15),16,(18),19,20,21		nCK	
Supported CWL Settings				9,10,11,12,14,16		nCK	

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9.5 DDR4-2666 Speed Bins and Operations

Table 9-5. DDR4-2666 Speed Bins and Operations

Speed Bin				DDR4-2666		Unit	Note
CL-nRCD-nRP				19-19-19			
Parameter			Symbol	Min	Max		
Internal Read command to first data			tAA	14.25 (13.75)[5,11]	18	ns	12
Internal Read command to first data with Read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	12
ACT to internal Read or Write delay time			tRCD	14.25 (13.75)[5,11]	-	ns	12
PRE command period			tRP	14.25 (13.75)[5,11]	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	46.25 (13.75)[5,11]	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9,11
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,9,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,9
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,9
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,9
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,9
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,9
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,9
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,9
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3,9
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3
Supported CL Settings				10,(11),12,(13),14,(15),16,(17),18,19,20		nCK	13
Supported CL Settings with Read DBI				12,(13),14,(15),16,(18),19,(20),21,22,23		nCK	
Supported CWL Settings				9,10,11,12,14,16,18		nCK	

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9.6 DDR4-3200 Speed Bins and Operations

Table 9-6. DDR4-3200 Speed Bins and Operations

Speed Bin				DDR4-3200		Unit	Note
CL-nRCD-nRP				22-22-22			
Parameter			Symbol	Min	Max		
Internal Read command to first data			tAA	13.75	18.00	ns	12
Internal Read command to first data with Read DBI enabled			tAA_DBI	tAA(min) + 4nCK	tAA(max) + 4nCK	ns	12
ACT to internal Read or Write delay time			tRCD	13.75	-	ns	12
PRE command period			tRP	13.75	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	45.75	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9,11
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,9,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,9
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,9
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,9
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,9
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,9
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,9
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,9
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3,9
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3
CWL = 16,20	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 22	CL = 26	tCK(AVG)	0.625	<0.75	ns	1,2,3,4
	CL = 24	CL = 28	tCK(AVG)	0.625	<0.75	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18,19,20,22,24		nCK	13
Supported CL Settings with Read DBI				12,13,14,15,16,18,19,20,21,22,23,24,26,28		nCK	
Supported CWL Settings				9,10,11,12,14,16,18,20		nCK	

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Speed Bin Table Note

Absolute Specifications

- VDDQ = VDD = 1.20V ± 0.06 V
- VPP = 2.5V (2.375V min, 2.75V max)
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133, 2400, 2666 and 3200 Speed Bin Tables are valid only when Gear Down Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL-all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following rounding algorithm defined in JEDEC-79C Section 13.5.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.937 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the corresponding table which are not subject to Production Tests but verified by Design/ Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the corresponding table which are not subject to Production Tests but verified by Design/ Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the corresponding table which are not subject to Production Tests but verified by Design/ Characterization.
9. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the corresponding table which are not subject to Production Tests but verified by Design/ Characterization.
10. Any DDR4-3200 speed bin also supports functional operation at lower frequencies as shown in the corresponding table which are not subject to Production Tests but verified by Design/ Characterization.
11. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
12. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
13. CL number in parentheses, it means that these numbers are optional.
14. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
15. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

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9.7 tREFI and tRFC Parameters

Table 9-7. tREFI and tRFC Parameters

Refresh Mode	Parameter		4Gb	Unit
	tREFI(base)		7.8	μs
1 x mode	tREFI1	-40 °C ≤ TCASE ≤ 85 °C	tREFI(base)	μs
		85 °C < TCASE ≤ 95 °C	tREFI(base)/2	μs
		tRFC1(min)	260	ns
2 x mode	tREFI2	-40 °C ≤ TCASE ≤ 85 °C	tREFI(base)/2	μs
		85 °C < TCASE ≤ 95 °C	tREFI(base)/4	μs
		tRFC2(min)	160	ns
4 x mode	tREFI4	-40 °C ≤ TCASE ≤ 85 °C	tREFI(base)/4	μs
		85 °C < TCASE ≤ 95 °C	tREFI(base)/8	μs
		tRFC4(min)	110	ns

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10 IDD AND IDDQ SPECIFICATION PARAMETERS AND TEST CONDITIONS

10.1 IDD, IPP and IDDQ Measurement Conditions

Figure 10-1 shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDD0A, IDD1, IDD1A, IDD2N, IDD2NA, IDD2NL, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3NA, IDD3P, IDD4R, IDD4RA, IDD4W, IDD4WA, IDD5B, IDD5F2, IDD5F4, IDD6N, IDD6E, IDD6R, IDD6A, IDD7 and IDD8) are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
- IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Attention: IDDQ values cannot be directly used to calculate IO power of the DDR4 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 10-2. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- “0” and “Low” is defined as VIN <= VILAC(max).
- “1” and “High” is defined as VIN >= VIHAC(min).
- “MID-LEVEL” is defined as inputs are VREF = VDD / 2.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in Table 10-2.
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in Table 10-3.
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting
  RON = RZQ/7 (34 Ohm in MR1);
  RTT_NOM = RZQ/6 (40 Ohm in MR1);
  RTT_WR = RZQ/2 (120 Ohm in MR2);
  RTT_PARK = Disable;
  Qoff = 0B (Output Buffer enabled) in MR1;
  TDQS_t disabled in MR1;
  CRC disabled in MR2;
  CA parity feature disabled in MR5;
  Gear down mode disabled in MR3;
  Read/Write DBI disabled in MR5;
  DM disabled in MR5
- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {CS_n, ACT_n, RAS_n, CAS_n, WE_n}: = {High, Low, Low, Low, Low}
- Define D# = {CS_n, ACT_n, RAS_n, CAS_n, WE_n}: = {High, High, High, High, High}; apply invert of BG/BA changes when directed above.

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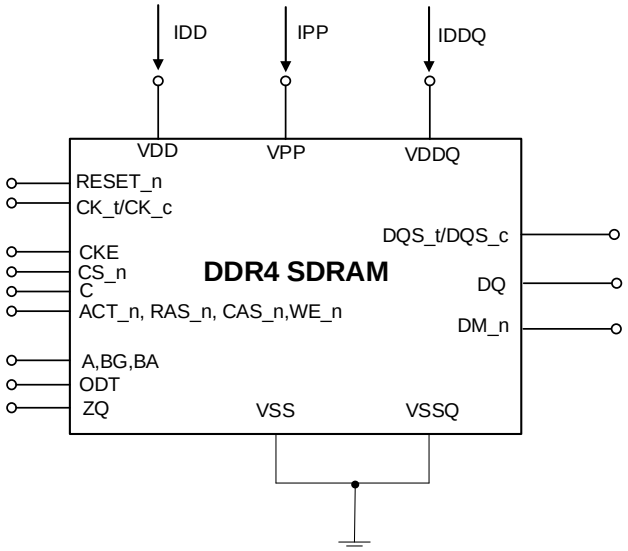


Figure 10-1. Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

Note:

DIMM level Output test load condition may be different from above

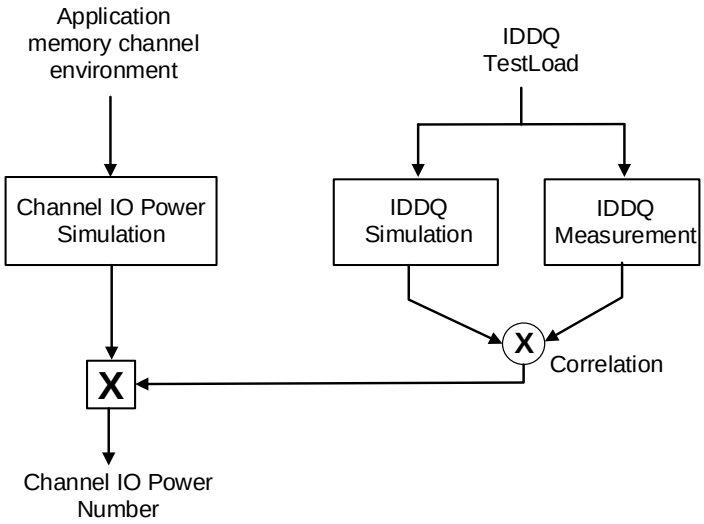


Figure 10-2. Correlation from Simulated Channel IO Power to Actual Channel IO Power Supported by IDDQ Measurement.

Table 10-1. Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns

Symbol	DDR4-1600			DDR4-1866			DDR4-2133			DDR4-2400				Unit
	10-10-10	11-11-11	12-12-12	12-12-12	13-13-13	14-14-14	14-14-14	15-15-15	16-16-16	15-15-15	16-16-16	17-17-17	18-18-18	
tCK	1.25			1.071			0.937			0.833				ns
CL	10	11	12	12	13	14	14	15	16	15	16	17	18	nCK
CWL	9	11	11	10	12	12	11	14	14	12	16	16	16	nCK
nRCD	10	11	12	12	13	14	14	15	16	15	16	17	18	nCK
nRC	38	39	40	44	45	46	50	51	52	54	55	56	57	nCK
nRAS	28			32			36			39				nCK
nRP	10	11	12	12	13	14	14	15	16	15	16	17	18	nCK

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Symbol		DDR4-1600			DDR4-1866			DDR4-2133			DDR4-2400				Unit
		10-10-10	11-11-11	12-12-12	12-12-12	13-13-13	14-14-14	14-14-14	15-15-15	16-16-16	15-15-15	16-16-16	17-17-17	18-18-18	
nFAW	X4	16			16			16			16				nCK
	X8	20			22			23			26				nCK
	X16	28			28			32			36				nCK
nRRDS	X4	4			4			4			4				nCK
	X8	4			4			4			4				nCK
	X16	5			6			6			7				nCK
nRRDL	X4	5			5			6			6				nCK
	X8	5			5			6			6				nCK
	X16	6			6			7			8				nCK
tCCD_S		4			4			4			4				nCK
tCCD_L		5			5			6			6				nCK
tWTR_S		2			3			3			3				nCK
tWTR_L		6			7			8			9				nCK
nRFC 2Gb		128			150			171			193				nCK
nRFC 4Gb		208			243			278			313				nCK
nRFC 8Gb		280			327			374			421				nCK
nRFC 16Gb		440			514			587			661				nCK

Symbol		DDR4-2666				DDR4-2933				DDR4-3200			Unit
		17-17-17	18-18-18	19-19-19	20-20-20	19-19-19	20-20-20	21-21-21	22-22-22	20-20-20	22-22-22	24-24-24	
tCK		0.75				0.682				0.625			ns
CL		17	18	19	20	19	20	21	22	20	22	24	nCK
CWL		16	16	18	18	18	18	20	20	18	20	20	nCK
nRCD		17	18	19	20	19	20	21	22	20	22	24	nCK
nRC		60	61	62	63	66	67	68	69	72	74	76	nCK
nRAS		43				47				52			nCK
nRP		17	18	19	20	19	20	21	22	20	22	24	nCK
nFAW	X4	16				16				16			nCK
	X8	28				31				34			nCK
	X16	40				44				48			nCK
nRRDS	X4	4				4				4			nCK
	X8	4				4				4			nCK
	X16	8				8				9			nCK
nRRDL	X4	7				8				8			nCK
	X8	7				8				8			nCK
	X16	9				10				11			nCK
tCCD_S		4				4				4			nCK
tCCD_L		7				8				8			nCK
tWTR_S		4				4				4			nCK

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Symbol	DDR4-2666				DDR4-2933				DDR4-3200			Unit
	17-17-17	18-18-18	19-19-19	20-20-20	19-19-19	20-20-20	21-21-21	22-22-22	20-20-20	22-22-22	24-24-24	
tWTR_L	10				11				12			nCK
nRFC 2Gb	214				235				256			nCK
nRFC 4Gb	347				382				416			nCK
nRFC 8Gb	467				514				560			nCK
nRFC 16Gb	734				807				880			nCK

Table 10-2. Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL** **BL:** 8[1]; **AL:** 0; **CS_n:** High between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 10-3. **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 10-3); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 10-3.
IDDA	**Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions:** see IDD0
IPP0	**Operating One Bank Active-Precharge IPP Current** Same condition with IDD0
IDD1	**Operating One Bank Active-Read-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL** **BL:** 8[1]; **AL:** 0; **CS_n**: High between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data IO:** partially toggling according to Table 10-4. **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 10-4) ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 10-4.
IDD1A	**Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions**: see IDD1
IPP1	**Operating One Bank Active-Read-Precharge IPP Current** Same condition with IDD1

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Symbol	Description
IDD2N	**Precharge Standby Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, CL** **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 10-5. **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 10-5
IDD2NA	**Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions:** see IDD2N
IPP2N	**Precharge Standby IPP Current** Same condition with IDD2N
IDD2NT	**Precharge Standby ODT Current** **CKE:** High; **External clock:** On; **tCK, CL** **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 10-6. **Data IO:** VSSQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:**oggling according to Table 10-6 **Pattern Details:** Table 10-6
IDDQ2NT (Optional)	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2NL	**Precharge Standby Current with CAL enabled** Same definition like for IDD2N, CAL enabled[3]
IDD2NG	**Precharge Standby Current with Gear Down mode enabled** Same definition like for IDD2N, Gear Down mode enabled[3,5]
IDD2ND	**Precharge Standby Current with DLL disabled** Same definition like for IDD2N, DLL disabled[3]
IDD2N_par	**Precharge Standby Current with CA parity enabled** Same definition like for IDD2N, CA parity enabled[3]

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Symbol	Description
IDD2P	**Precharge Power-Down Current CKE:** Low; **External clock:** On; **tCK, CL** **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IPP2P	**Precharge Power-Down IPP Current** Same condition with IDD2P
IDD2Q	**Precharge Quiet Standby Current** **CKE**: High; **External clock:** On; **tCK, CL** **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IDD3N	**Active Standby Current** **CKE:** High; **External clock:** On; **tCK, CL** **BL:** 8[1]; **AL:** 0; **CS_n:** stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 10-5. **Data IO**: VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 10-5
IDD3NA	**Active Standby Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD3N
IPP3N	**Active Standby IPP Current** **Same condition with IDD3N**

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Symbol	Description
IDD3P	**Active Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL** **BL:** 8[1]; **AL:** 0; **CS_n:** stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT**: Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IPP3P	**Active Power-Down IPP Current** Same condition with IDD3P
IDD4R	**Operating Burst Read Current** **CKE:** High; **External clock:** On; **tCK, CL** **BL:** 8[2]; **AL:** 0; **CS_n**: High between RD; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 10-7. **Data IO**: seamless Read data burst with different data between one burst and the next one according to Table 10-7. **DM_n:** stable at 1; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 10-7) **Output Buffer and RTT**: Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 10-7
IDD4RA	**Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions:** see IDD4R
IDD4RB	**Operating Burst Read Current with Read DBI** **Read DBI enabled[3], Other conditions:** see IDD4R
IPP4R	**Operating Burst Read IPP Current** **Same condition with IDD4R**
IDDQ4R (Optional)	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDDQ4RB (Optional)	**Operating Burst Read IDDQ Current with Read DBI** Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current

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Symbol	Description
IDD4W	**Operating Burst Write Current** **CKE:** High; **External clock:** On; **tCK, CL** **BL:** 8[1]; **AL:** 0; **CS_n:** High between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 10-8; **Data IO**: seamless Write data burst with different data between one burst and the next one according to Table 10-8 **DM_n:** stable at 1; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (Table 10-8); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at High; **Pattern Details:** see Table 10-8
IDD4WA	**Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions:** see IDD4W
IDD4WB	**Operating Burst Write Current with Write DBI** **Write DBI enabled3, Other conditions:** see IDD4W
IDD4WC	**Operating Burst Write Current with Write CRC** **Write CRC enabled3, Other conditions:** see IDD4W
IDD4W_par	**Operating Burst Write Current with CA Parity** **CA Parity enabled3, Other conditions:** see IDD4W
IPP4W	**Operating Burst Write IPP Current** **Same condition with IDD4W**
IDD5B	**Burst Refresh Current (1X REF)** **CKE:** High; **External clock:** On; **tCK, CL nRFC** **BL:** 8[1]; **AL:** 0; **CS_n:** High between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 10-10. **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC (see Table 10-10); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details**: see Table 10-10
IPP5B	**Burst Refresh Write IPP Current (1X REF) Same condition with IDD5B**
IDD5F2	**Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions:** see IDD5B
IPP5F2	**Burst Refresh Write IPP Current (2X REF) Same condition with IDD5F2**
IDD5F4	**Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions:** see IDD5B
IPP5F4	**Burst Refresh Write IPP Current (4X REF) Same condition with IDD5F4**

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Symbol	Description
IDD6N	**Self Refresh Current: Normal Temperature Range** ***T*CASE: 0 - 85°C;** **Low Power Array Self Refresh (LP ASR)**: Normal[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: Low; **CL** **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6N	**Self Refresh IPP Current: Normal Temperature Range Same condition with IDD6N**
IDD6E	**Self-Refresh Current: Extended Temperature Range)** ***T*CASE: 0 - 95°C;** **Low Power Array Self Refresh (LP ASR)**: Extended[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: Low; **CL** **BL:** 8[1] **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**: stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6E	**Self Refresh IPP Current: Extended Temperature Range Same condition with IDD6E**
IDD6R	**Self-Refresh Current: Reduced Temperature Range** ***T*CASE: 0 - TBD (~35-45) °C;** **Low Power Array Self Refresh (LP ASR)**: Reduced[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: Low; **CL** **BL:** 8[1] **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**: stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6R	**Self Refresh IPP Current: Reduced Temperature Range Same condition with IDD6R**

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Symbol	Description
IDD6A	**Auto Self-Refresh Current** ***T*CASE: 0 - 95°C;** **Low Power Array Self Refresh (LP ASR)**: Auto[4]; **Partial Array Self-Refresh (PASR)**: Full Array; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: Low; **CL** **BL:** 8[1] **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**: stable at 1; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6A	**Auto Self-Refresh IPP Current** **Same condition with IDD6A**
IDD7	**Operating Bank Interleave Read** **Current CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD,** **nFAW, CL BL:** 8[1]; **AL:** CL-1; **CS_n**: High between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 10-11; **Data IO:** Read data bursts with different data between one burst and the next one according to Table 10-11; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 10-11; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 10-11.
IPP7	**Operating Bank Interleave Read IPP Current** **Same condition with IDD7**
IDD8	**Maximum Power Down Current TBD**
IPP8	**Maximum Power Down IPP Current Same condition with IDD8**

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10.1.1 IDD0, IDD0A and IPP0 Measurement-Loop Pattern

Table 10-3. IDD0, IDD0A and IPP0 Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3,4	D_#,D_#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			...	repeat pattern 1…4 unit nRAS -1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			…	repeat pattern 1…4 unit nRC -1, truncate if necessary																
		1	1*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 1 instead																
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2instead																
		3	3*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead																
		5	5*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 2 instead																
		6	6*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
		7	7*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
		8	8*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	9*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 1 instead																
		10	10*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
		11	11*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 3 instead																
		12	12*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead																
		13	13*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
		14	14*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
		15	15*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 0 instead																

Note:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is Don't Care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ.

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10.1.2 IDD1, IDD1A and IPP1 Measurement-Loop Pattern

Table 10-4. IDD1, IDD1A and IPP1 Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1,2	D,D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3,4	D_#,D_#	1	1	1	1	1	0	0	3[b]	3	0	0	0	7	F	0	-
			...	repeat pattern 1…4 unit nRCD – AL - 1, truncate if necessary																
			nRCD -AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			…	repeat pattern 1…4 unit nRAS -1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			…	repeat pattern nRC + 1…4 unit 1*nRC + nRAS -1, truncate if necessary																
		1	1*nRC + 0	ACT	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	-
			1*nRC + 1,2	D,D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1*nRC + 3,4	D_#, D_#	1	1	1	1	1	0	0	3[b]	3	0	0	0	7	F	0	-
			…	repeat pattern nRC + 1…4 unit 1*nRC + nRAS -1, truncate if necessary																
			1*nRC + nRCD – AL	RD	0	1	1	0	1	0	0	1	1	0	0	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			…	repeat pattern 1…4 unit nRAS -1, truncate if necessary																
			1*nRC + nRAS	PRE	0	1	0	1	0	0	0	1	1	0	0	0	0	0	0	-
			…	repeat nRC + 1…4 unit 2*nRC -1, truncate if necessary																
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead																
		3	3*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead																
		5	5*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead																
		6	6*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
		8	7*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
		9	9*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 2, BA[1:0] = 0 instead																For x4 and x8 only

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CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
		10	10*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 1 instead															
		11	11*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 2, BA[1:0] = 2 instead															
		12	12*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 3 instead															
		13	13*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 2, BA[1:0] = 1 instead															
		14	14*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 2 instead															
		15	15*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 2, BA[1:0] = 3 instead															
		16	16*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 0 instead															

Note:

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
2. BG1 is Don’t Care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

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10.1.3 IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2, IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern

Table 10-5. IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2, IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	D,D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			1	D,D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			2	D_#,D_#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	0
			3	D_#,D_#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	0
		1	4-7	repeat Sub-Loop 0, use BG[1:0] = 1, BA[1:0] = 1 instead																
		2	8-11	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 2 nstead																
		3	12-15	repeat Sub-Loop 0, use BG[1:0] = 1, BA[1:0] = 3 instead																
		4	16-19	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 1 instead																
		5	20-23	repeat Sub-Loop 0, use BG[1:0] = 1, BA[1:0] = 2 instead																
		6	24-27	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 3 instead																
		7	28-31	repeat Sub-Loop 0, use BG[1:0] = 1, BA[1:0] = 0 instead																
		8	32-35	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 0 instead																
		9	36-39	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 1 instead																
		10	40-43	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 2 instead																
		11	44-47	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 3 instead																
		12	48-51	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 1 instead																
		13	52-55	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 2 instead																
		14	56-59	repeat Sub-Loop 0, use BG[1:0] = 2, BA[1:0] = 3 instead																
		15	60-63	repeat Sub-Loop 0, use BG[1:0] = 3, BA[1:0] = 0 instead																

Note:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is Don’t Care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ.

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10.1.4 IDD2NT and IDDQ2NT Measurement-Loop Pattern

Table 10-6. IDD2NT and IDDQ2NT Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	D,D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1	D,D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	D_#,D_#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	-
			3	D_#,D_#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 1, BA[1:0] = 1 instead																
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 0, BA[1:0] = 2 instead																
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 0, BA[1:0] = 1 instead																
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 1, BA[1:0] = 2 instead																
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 0, BA[1:0] = 3 instead																
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 1, BA[1:0] = 0 instead																
		8	32-35	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 3, BA[1:0] = 1 instead																
		10	40-43	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 2, BA[1:0] = 2 instead																
		11	44-47	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 3, BA[1:0] = 3 instead																
		12	48-51	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 2, BA[1:0] = 1 instead																
		13	52-55	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 3, BA[1:0] = 2 instead																
		14	56-59	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 2, BA[1:0] = 3 instead																
		15	60-63	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 3, BA[1:0] = 0 instead																

Note:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is Don’t Care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ.

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10.1.5 IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern[1]

Table 10-7. IDD4R, IDDR4RA, IDDR4RB and IDDQ4R Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2,3	D_#,D_#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
		1	4	RD	0	1	1	0	1	0	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			6,7	D_#,D_#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
		2	8-11	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead															
		3	12-15	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead															
		4	16-19	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead															
		5	20-23	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead															
		6	24-27	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead															
		7	28-31	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead															
		8	32-35	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead															For x4 and x8 only
		9	36-39	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 1 instead															
		10	40-43	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead															
		11	44-47	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 3 instead															
		12	48-51	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead															
		13	52-55	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 2 instead															
		14	56-59	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead															
		15	60-63	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 0 instead															

Note:

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
2. BG1 is Don't Care for x16 device
3. C[2:0] are used only for 3DS device

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4. Burst Sequence driven on each DQ signal by Read Command.

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10.1.6 IDD4W, IDDR4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern

Table 10-8. IDD4W, IDDR4WA, IDDR4WB and IDD4W_par Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			1	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	
			2,3	D_#,D_#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	
		1	4	WR	0	1	1	0	0	1	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			5	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	
			6,7	D_#,D_#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	
		2	8-11	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead																
		3	12-15	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	16-19	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead																
		5	20-23	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead																
		6	24-27	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
		7	28-31	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
		8	32-35	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 1 instead																
		10	40-43	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
		11	44-47	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 3 instead																
		12	48-51	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead																
		13	52-55	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
		14	56-59	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
		15	60-63	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 0 instead																

Note:

1. DQS_t, DQS_c are used according to WR Commands, otherwise VDDQ.
2. BG1 is Don’t Care for x16 device
3. C[2:0] are used only for 3DS device

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4. Burst Sequence driven on each DQ signal by Write Command.

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10.1.7 IDD4WC Measurement-Loop Pattern

Table 10-9. IDD4WC Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC
			1,2	D,D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			3,4	D_#,D_#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
			5	WR	0	1	1	0	0	1	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC
			6,7	D,D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			8,9	D_#,D_#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
		2	10-14	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead															
		3	15-19	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead															
		4	20-24	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead															
		5	25-29	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead															
		6	30-34	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead															
		7	35-39	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead															
		8	40-44	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead															For x4 and x8 only
		9	45-49	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 1 instead															
		10	50-54	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead															
		11	55-59	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 3 instead															
		12	60-64	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead															
		13	65-69	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 2 instead															
		14	70-74	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead															
		15	75-79	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 0 instead															

Note:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is Don't Care for x16 device

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3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Write Command.

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10.1.8 IDD5B Measurement-Loop Pattern

Table 10-10. IDD5B Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	REF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3	D_#,D_#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			4	D_#,D_#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			4-7	repeat pattern 1…4, use BG[1:0][2]= 1, BA[1:0] = 1 instead.																
			8-11	repeat pattern 1…4, use BG[1:0][2]= 0, BA[1:0] = 2 instead.																
			12-15	repeat pattern 1…4, use BG[1:0][2]= 1, BA[1:0] = 3 instead.																
			16-19	repeat pattern 1…4, use BG[1:0][2]= 0, BA[1:0] = 1 instead.																
			20-23	repeat pattern 1…4, use BG[1:0][2]= 1, BA[1:0] = 2 instead.																
			24-27	repeat pattern 1…4, use BG[1:0][2]= 0, BA[1:0] = 3 instead.																
			28-31	repeat pattern 1…4, use BG[1:0][2]= 1, BA[1:0] = 0 instead.																
			32-35	repeat pattern 1…4, use BG[1:0][2]= 2, BA[1:0] = 0 instead.																For x4 and x8 only
			36-39	repeat pattern 1…4, use BG[1:0][2]= 3, BA[1:0] = 1 instead.																
			40-43	repeat pattern 1…4, use BG[1:0][2]= 2, BA[1:0] = 2 instead.																
			44-47	repeat pattern 1…4, use BG[1:0][2]= 3, BA[1:0] = 3 instead.																
			48-51	repeat pattern 1…4, use BG[1:0][2]= 2, BA[1:0] = 1 instead.																
			52-55	repeat pattern 1…4, use BG[1:0][2]= 3, BA[1:0] = 2 instead.																
			56-59	repeat pattern 1…4, use BG[1:0][2]= 2, BA[1:0] = 3 instead.																
			60-63	repeat pattern 1…4, use BG[1:0][2]= 3, BA[1:0] = 0 instead.																
		2	64… nRFC -1	repeat Sub-Loop 1, Truncate, if necessary																

Note:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is Don’t Care for x16 device
3. C[2:0] are used only for 3DS device

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4. DQ signals are VDDQ.

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10.1.9 IDD7 Measurement-Loop Pattern

Table 10-11. IDD7 Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1	RDA	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
			3	D_#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	
			…	repeat pattern 2…3, until nRRD – 1, if nRRD > 4. Truncate if necessary.																
		1	nRRD	ACT	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	
			nRRD + 1	RDA	0	1	1	0	1	0		1	1	0	0	1	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			…	repeat pattern 2…3, until 2*nRRD – 1, if nRRD > 4. Truncate if necessary.																
		2	2*nRRD	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead.																
		3	3*nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead.																
		4	4*nRRD	repeat pattern 2…3, until nFAW – 1, if nFAW > 4*nRRD. Truncate if necessary.																
		5	nFAW	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead.																
		6	nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead.																
		7	nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead.																
		8	nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead.																
		9	nFAW + 4*nRRD	repeat Sub-Loop 4																
		10	2*nFAW	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead.																For x4 and x8 only
		11	2*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 2 instead.																
		12	2*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead.																
		13	2*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 0 instead.																
		14	2*nFAW + 4*nRRD	repeat Sub-Loop 4																
		15	3*nFAW	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead.																

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CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
		16	3*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 2 instead.																
		17	3*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead.																
		18	3*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 0 instead.																
		19	3*nFAW + 4*nRRD	repeat Sub-Loop 4																
		20	4*nFAW	repeat pattern 2…3, until nRC – 1, if nRC > 4*nFAW. Truncate if necessary.																

Note:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is Don’t Care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

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10.2 IDD Specifications

IDD and IPP values are for full operation range of voltage and temperature unless otherwise noted.

Table 10-12. IDD and IDDQ Specifications (Rev. B)

Symbol	Width	2400	2666	3200	Unit
IDD0	x16	90	93	101	mA
IDD0A	x16	90	94	102	mA
IDD1	x16	97	101	109	mA
IDD1A	x16	100	103	112	mA
IDD2N	x16	54	55	61	mA
IDD2NA	x16	54	56	61	mA
IDD2NT	x16	60	62	69	mA
IDD2P	x16	32	36	39	mA
IDD2Q	x16	52	52	57	mA
IDD3P	x16	44	45	48	mA
IDD3N	x16	85	88	98	mA
IDD4R	x16	166	178	209	mA
IDD4W	x16	192	208	242	mA
IDD5B	x16	177	180	187	mA
IDD5R	x16	58	60	65	mA
IDD6A	x16	32	32	32	mA
IDD6E	x16	33	33	33	mA
IDD6N	x16	28	28	28	mA
IDD6R	x16	25	25	25	mA
IDD7	x16	183	223	233	mA
IDD8	x16	24	24	24	mA
IDDQ2NT	x16	70	70	70	mA

Note:

1. Maximum limits are specified.
2. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR4 SDRAM devices support the following options or requirements referred to in this material.

Table 10-13. IPP Specifications (Rev. B)

Symbol	Width	2400	2666	3200	Unit
IPP0	x16	7	7	7	mA
IPP1	x16	7	7	7	mA
IPP2N	x16	4	4	4	mA
IPP3N	x16	5	5	5	mA
IPP5B	x16	22	22	22	mA
IPP5R	x16	5	5	5	mA
IPP6N	x16	3	3	3	mA
IPP7	x16	20	24	24	mA

Note:

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1. Maximum limits are specified.
2. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR4 SDRAM devices support the following options or requirements referred to in this material.

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11 INPUT/OUTPUT CAPACITANCE

Table 11-1. Silicon Pad I/O Capacitance

Symbol	Parameter	1600/1866/2133		2400/2666		3200		Unit	Note
		Min	Max	Min	Max	Min	Max		
C_{IO}	Input/output capacitance	0.55	1.4	0.55	1.15	0.55	1.00	pF	1,2,3
C_{DIO}	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,3,11
C_{DDQS}	Input/output capacitance delta DQS_t and DQS_c	-	0.05	-	0.05	-	0.05	pF	1,2,3,5
C_{CK}	Input capacitance, CK_t and CK_c	0.2	0.8	0.2	0.7	0.2	0.7	pF	1,3
C_{DCK}	Input capacitance delta CK_t and CK_c	-	0.05	-	0.05	-	0.05	pF	1,3,4
C_I	Input capacitance (CTRL, ADD, CMD pins only)	0.2	0.8	0.2	0.7	0.2	0.55	pF	1,3,6
C_{DI_CTRL}	Input capacitance delta (All CTRL pins only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
$C_{DI_ADD_CMD}$	Input capacitance delta (All ADD/ CMD pins only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
C_{ALERT}	Input/output capacitance of ALERT	0.5	1.5	0.5	1.5	0.5	1.5	pF	1,3
C_{ZQ}	Input/output capacitance of ZQ	-	2.3	-	2.3	-	2.3	pF	1,3,12
C_{TEN}	Input capacitance OF TEN	0.2	2.3	0.2	2.3	0.2	2.3	pF	1,3,13

Note:

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by deembedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure TBD.
2. DQ, DM_n, DQS_T, DQS_C, TDQS_T, TDQS_C. Although the DM, TDQS_T and TDQS_C pins have different functions, the loading matches DQ and DQS.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
4. Absolute value CK_T - CK_C.
5. Absolute value of CIO(DQS_T) - CIO(DQS_C).
6. CI applies to ODT, CS_n, CKE, A0 - A17, BA0 - BA1, BG0 - BG1, RAS_n / A16, CAS_n / A15, WE_n / A14, ACT_n and PAR.
7. $C_{DI\ CTRL}$ applies to ODT, CS_n and CKE.
8. $C_{DI_CTRL} = C_I(CTRL) - 0.5*(C_I(CLK_T) + C_I(CLK_C))$.
9. $C_{DI_ADD_CMD}$ applies to, A0 - A17, BA0 - BA1, BG0 - BG1, RAS_n / A16, CAS_n / A15, WE_n / A14, ACT_n and PAR.
10. $C_{DI_ADD_CMD} = C_I(ADD_CMD) - 0.5*(C_I(CLK_T) + C_I(CLK_C))$.
11. $C_{DIO} = C_{IO}(DQ, DM) - 0.5*(C_{IO}(DQS_T) + C_{IO}(DQS_C))$.
12. Maximum external load capacitance on ZQ pin: tbd pF.
13. TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.

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Table 11-2. DRAM Package Electrical Specifications (x16)

Symbol	Parameter	1600/1866/2133		2400/2666/3200		Unit	Note
		Min	Max	Min	Max		
Z_{IO}	Input/output Zpkg	45	85	45	85	Ω	1
T_{DIO}	Input/output Pkg Delay	14	45	14	45	ps	1
L_{iO}	Input/output Lpkg	-	3.4	-	3.4	nH	1,2
C_{iO}	Input/output Cpkg	-	0.82	-	0.82	pF	1,3
$Z_{IO\ DQS}$	DQS_t and DQS_c Zpkg	45	85	45	85	Ω	1
$Td_{IO\ DQS}$	DQS_t and DQS_c Pkg Delay	14	45	14	45	ps	1
$L_{iO\ DQS}$	DQS Lpkg	-	3.4	-	3.4	nH	1,2
$C_{iO\ DQS}$	DQS Cpkg	-	0.82	-	0.82	pF	1,3
$DZ_{DIO\ DQS}$	Delta Zpkg DQSU_t, DQSU_c	-	10	-	10	Ω	-
	Delta Zpkg DQSL_t, DQSU_c	-	10	-	10	Ω	-
$D_{TdDIO\ DQS}$	Delta Delay DQSU_t, DQSU_c	-	5	-	5	ps	-
	Delta Delay DQSL_t, DQSU_c	-	5	-	5	ps	-
$Z_{I\ CTRL}$	Input-CTRL pins Zpkg	50	90	50	90	Ω	1
Td_{IADD_CMD}	Input-CTRL pins Pkg Delay	14	42	14	42	ps	1
$L_{i\ CTRL}$	Input CTRL Lpkg	-	3.4	-	3.4	nH	1,2
$C_{i\ CTRL}$	Input CTRL Cpkg	-	0.7	-	0.7	pF	1,3
Z_{IADD_CMD}	Input-CMD ADD pins Zpkg	50	90	50	90	Ω	1
Td_{IADD_CMD}	Input-CMD ADD pins Pkg Delay	14	52	14	52	ps	1
L_{iADD_CMD}	Input-CMD ADD Lpkg	-	3.9	-	3.9	nH	1,2
C_{iADD_CMD}	Input-CMD ADD Cpkg	-	0.86	-	0.86	pF	1,3

Table 11-3. DRAM Package Electrical Specifications (x16) (cont'd)

Symbol	Parameter	1600/1866/2133		2400/2666/3200		Unit	Note
		Min	Max	Min	Max		
Z_{CK}	CLK_t and CLK_c Zpkg	50	90	50	90	Ω	-
Td_{CK}	CLK_t and CLK_c Pkg Delay	14	42	14	42	ps	-
$L_{i\ CLK}$	Input CLK Lpkg	-	3.4	-	3.4	nH	-
$C_{i\ CLK}$	Input CLK Cpkg	-	0.7	-	0.7	pF	-
DZ_{DCK}	Delta Zpkg CK_t and CK_c	-	10	-	10	Ω	-
D_{TdCK}	Delta Delay CK_t and CK_c	-	5	-	5	ps	-
Z_{OZQ}	ZQ Zpkg	-	100	-	100	Ω	-
$Td_{O\ ZQ}$	ZQ Delay	20	90	20	90	ps	-
$Z_{O\ ALERT}$	ALERT Zpkg	40	100	40	100	Ω	-
$Td_{O\ ALERT}$	ALERT Delay	20	55	20	55	ps	-

Note:

1. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum value shown.
2. It is assumed that Lpkg can be approximated as Lpkg = Zo*Td.
3. It is assumed that Cpkg can be approximated as Cpkg = Td/Zo.

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12 ELECTRICAL CHARACTERISTICS & AC TIMING

12.1 Reference Load for AC Timing and Output Slew Rate

Figure 12-1 represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

RON nominal of DQ, DQS_t and DQS_c drivers uses 34 ohms to specify the relevant AC timing parameter values of the device.

- The maximum DC High level of Output signal = 1.0*VDDQ
- The minimum DC Low level of Output signal = {34 / (34 + 50)}*VDDQ = 0.4*VDDQ
- The nominal reference level of an Output signal can be approximated by the following:
- The center of maximum DC High and minimum DC Low = {(1 + 0.4) / 2}*VDDQ = 0.7* VDDQ

The actual reference level of Output signal might vary with driver RON and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye. Prior to measuring AC parameters, the reference level of the verification tool should be set to an appropriate level.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

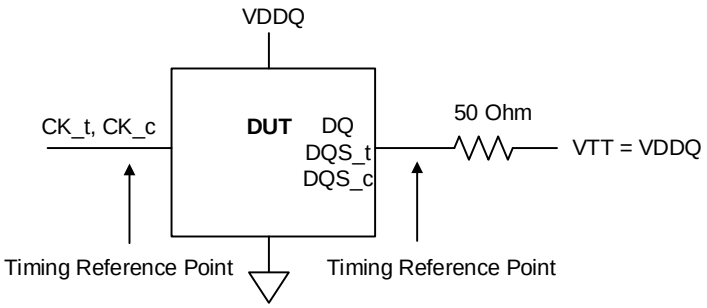


Figure 12-1. Reference Load for AC Timing and Output Slew Rate

12.2 tREFI

Average periodic Refresh interval (tREFI) of DDR4 SDRAM is defined as shown in Table 12-1 below.

Table 12-1. tREFI by Device Density

Parameter	Symbol		4Gb	Unit
Average periodic refresh interval	tREFI	0 °C ≤ TCASE ≤ 85 °C	7.8	µs
		85 °C ≤ TCASE ≤ 95 °C	3.9	µs

12.3 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR4 SDRAM device.

12.3.1 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.

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12.3.2 Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg)=(\sum_{j=1}^{N} tCK(abs)j) / N \quad N=200$$

12.3.3 Definition for tCH(avg) and Tcl(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg)=(\sum_{j=1}^{N} tCHj) / (N \times tCK(avg)) \quad N=200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg)=(\sum_{j=1}^{N} tCLj) / (N \times tCK(avg)) \quad N=200$$

12.3.4 Definition for tERR(nper)

tERR is defined as the cumulative error across n consecutive cycles of n x tCK(avg). tERR is not subject to production test.

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12.4 Timing Parameters by Speed Grade

12.4.1 Timing Parameters by Speed Bin for DDR4-1600 to 2400

Table 12-2. Timing Parameters by Speed Bin for DDR4_1600 to 2400

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing											
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	8	20	ns	
Average Clock Period	tCK (avg)	1.25	<1.5	1.071	<1.25	0.937	<1.071	0.833	<0.937	ns	35,36
Average high pulse width	tCH (avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK (avg)	
Average low pulse width	tCL (avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK (avg)	
Absolute Clock Period	tCK (abs)	Min : tCK(avg)min + tJIT(per)min_tot								tCK (avg)	
		Max : tCK(avg)max + tJIT(per)max_tot									
Absolute clock HIGH pulse width	tCH (abs)	0.45	-	0.45	-	0.45	-	0.45	-		23
Absolute clock LOW pulse width	tCL (abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK (avg)	24
Clock Period Jitter- total	JIT (per)_tot	-63	63	-54	54	-47	47	-42	42	ps	25
Clock Period Jitter- deterministic	JIT (per)_dj	-31	31	-27	27	-23	23	-21	21	ps	26
Clock Period Jitter during DLL locking period	tJIT (per, lck)	-50	50	-43	43	-38	38	-33	33	ps	
Cycle to Cycle Period Jitter	tJIT (cc)	-	125	-	107	-	94	-	83	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT (cc, lck)	-	100	-	86	-	75	-	67	ps	
Cumulative error across 2 cycles	tERR (2per)	-92	92	-79	79	-69	69	-61	61	ps	
Cumulative error across 3 cycles	tERR (3per)	-109	109	-94	94	-82	82	-73	73	ps	
Cumulative error across 4 cycles	tERR (4per)	-121	121	-104	104	-91	91	-81	81	ps	
Cumulative error across 5 cycles	tERR (5per)	-131	131	-112	112	-98	98	-87	87	ps	
Cumulative error across 6 cycles	tERR (6per)	-139	139	-119	119	-104	104	-92	92	ps	
Cumulative error across 7 cycles	tERR (7per)	-145	145	-124	124	-109	109	-97	97	ps	

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Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Cumulative error across 8 cycles	tERR (8per)	-151	151	-129	129	-113	113	-101	101	ps	
Cumulative error across 9 cycles	tERR (9per)	-156	156	-134	134	-117	117	-104	104	ps	
Cumulative error across 10 cycles	tERR (10per)	-160	160	-137	137	-120	120	-107	107	ps	
Cumulative error across 11 cycles	tERR (11per)	-164	164	-141	141	-123	123	-110	110	ps	
Cumulative error across 12 cycles	tERR (12per)	-168	168	-144	144	-126	126	-112	112	ps	
Cumulative error across 13 cycles	tERR (13per)	-172	172	-147	147	-129	129	-114	114	ps	
Cumulative error across 14 cycles	tERR (14per)	-175	175	-150	150	-131	131	-116	116	ps	
Cumulative error across 15 cycles	tERR (15per)	-178	178	-152	152	-133	133	-118	118	ps	
Cumulative error across 16 cycles	tERR (16per)	-180	189	-155	155	-135	135	-120	120	ps	
Cumulative error across 17 cycles	tERR (17per)	-183	183	-157	157	-137	137	-122	122	ps	
Cumulative error across 18 cycles	tERR (18per)	-185	185	-159	159	-139	139	-124	124	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR (nper)	tERR (nper)min = ((1 + 0.68ln(n)) *tJIT (per)_total min) tERR (nper)max = ((1 + 0.68ln(n)) *tJIT (per)_total max)								ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS (base)	115	-	100	-	80	-	62	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS (Vref)	215	-	200	-	180	-	162	-	ps	
Command and Address hold time to CK_t,CK_c referenced to Vih(dc) / Vil(dc) levels	tIH (base)	140	-	125	-	105	-	87	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH (Vref)	215	-	200	-	180	-	162	-	ps	
Control and Address Input pulse width for each input	tIPW	600	-	525	-	460	-	410	-	ps	
Command and Address Timing											
CAS_n to CAS_n command delay for same bank	tCCD_L	Max	-	Max	-	Max	-	Max	-	nCK	34

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Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
group		(5nCK, 6.250 ns)		(5nCK, 5.355 ns)		(5nCK, 5.355 ns)		(5nCK, 5 ns)			
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S (2K)	Max (4nCK, 6 ns)	-	Max (4nCK, 5.3 ns)	-	Max (4nCK, 5.3 ns)	-	Max (4nCK, 5.3 ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	tRRD_S (1K)	Max (4nCK, 5 ns)	-	Max (4nCK, 4.2 ns)	-	Max (4nCK, 3.7 ns)	-	Max (4nCK, 3.3 ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/ 2KB page size	tRRD_S (1/2K)	Max (4nCK, 5.0 ns)	-	Max (4nCK, 4.2 ns)	-	Max (4nCK, 3.7 ns)	-	Max (4nCK, 3.3 ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L (2K)	Max (4nCK, 7.5 ns)	-	Max (4nCK, 6.4 ns)	-	Max (4nCK, 6.4 ns)	-	Max (4nCK, 6.4 ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L (1K)	Max (4nCK, 6.0 ns)	-	Max (4nCK, 5.3 ns)	-	Max (4nCK, 5.3 ns)	-	Max (4nCK, 4.9 ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/ 2KB page size	tRRD_L (1/2K)	Max (4nCK, 6.0 ns)	-	Max (4nCK, 5.3 ns)	-	Max (4nCK, 5.3 ns)	-	Max (4nCK, 4.9 ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max (28nCK, 35 ns)	-	Max (28nCK, 30 ns)	-	Max (28nCK, 30 ns)	-	Max (28nCK, 30 ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max (20nCK, 25 ns)	-	Max (20nCK, 23 ns)	-	Max (20nCK, 21 ns)	-	Max (20nCK, 21 ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max (16nCK, 20 ns)	-	Max (16nCK, 17 ns)	-	Max (16nCK, 15 ns)	-	Max (16nCK, 13 ns)	-	ns	34
Delay from start of internal Write transaction to internal read command for different bank group	tWTR_S	Max (2nCK, 2.5 ns)	-	Max (2nCK, 2.5 ns)	-	Max (2nCK, 2.5 ns)	-	Max (2nCK, 2.5 ns)	-	ns	1, 2, 34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	Max (4nCK, 7.5 ns)	-	Max (4nCK, 7.5 ns)	-	Max (4nCK, 7.5 ns)	-	Max (4nCK, 7.5 ns)	-	ns	1, 34

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Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Internal READ Command to PRECHARGE Command delay	tRTP	Max (4nCK, 7.5 ns)	-	Max (4nCK, 7.5 ns)	-	Max (4nCK, 7.5 ns)	-	Max (4nCK, 7.5 ns)	-	ns	
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR + max (4nCK, 3.75 ns)		tWR + max (5nCK, 3.75 ns)		tWR + max (5nCK, 3.75 ns)		tWR + max(5nCK, 3.75 ns)		ns	1, 28
Delay from start of internal Write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S + max (4nCK, 3.75 ns)		tWTR_S + max (5nCK, 3.75 ns)		tWTR_S + max (5nCK, 3.75 ns)		tWTR_S + max (5nCK, 3.75 ns)		ns	2,,29, 34
Delay from start of internal Write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L + max (4nCK, 3.75 ns)		tWTR_L + max (5nCK, 3.75 ns)		tWTR_L + max (5nCK, 3.75 ns)		tWTR_L + max (5nCK, 3.75 ns)		ns	3, 30, 34
DDL locking time	tDLLK	597	-	597	-	768	-	768	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	Max (24nCK, 15 ns)	-	Max (24nCK, 15 ns)	-	Max (24nCK, 15 ns)	-	Max (24nCK, 15 ns)	-	nCK	50
Mult-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	nCK	33
Mult-Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) +AL + PL	-	tMOD (min) +AL + PL	-	tMOD (min) +AL + PL	-	tMOD (min) +AL + PL	-	ns	
Auto precharge write recovery + precharge time	tDAL (min)	Programmed WR + roundup (tRP / tCK(avg))								nCK	
DQ0 or DQL0 driven to set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	0.5	-	UI	45, 47
DQ0 or DQL0 driven to hold time from last DQS falling edge	tPDA_H	0.5	-	0.5	-	0.5	-	0.5	-	UI	46, 47

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Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
CS_n to Command Address Latency											
CS_n to Command Address Latency	tCAL	Max (3nCK, 3.748 ns)	-	Max (3nCK, 3.748 ns)	-	Max (3nCK, 3.748 ns)	-	Max (3nCK, 3.748 ns)	-	nCK	
Mode Register Set command cycle time in CAL mode	tMRD_tCAL	tMOD + tCAL	-	tMOD + tCAL	-	tMOD + tCAL	-	tMOD + tCAL	-	nCK	
Mode Register Set update delay in CAL mode	tMOD_tCAL	tMOD + tCAL	-	tMOD + tCAL	-	tMOD + tCAL	-	tMOD + tCAL	-	nCK	
DRAM Data Timing											
DQS_t,DQS_c to DQ skew, per group, per acces	tDQSQ	-	0.16	-	0.16	-	0.16	-	0.17	tCK (avg)/2	13,18,39 ,49
DQ output hold time from DQS_t, DQS_c	tQH	0.76	-	0.76	-	0.76	-	0.74	-	tCK (avg)/2	13,17,18 ,39,49
Data Valid Window per device per UI: (tQH - tDQSQ) of each UI on a given DRAM	tDVWd	0.63	-	0.63	-	0.64	-	0.64	-	UI	17,18,39 ,49
Data Valid Window per pin per UI: (tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.66	-	0.66	-	0.69	-	0.72	-	UI	17,18,39 ,49
DQ low impedance time from CK_t, CK_c	tLZ (DQ)	-450	225	-390	195	-360	180	-330	175	ps	39
DQ high impedance time from CK_t, CK_c	tHZ (DQ)	-	225	-	195	-	180	-	175	ps	39
Data Strobe Timing											
DQS_t, DQS_c differential READ Preamble (1 clock preamble)	tRPRE	0.9	Note 44	0.9	Note 44	0.9	Note 44	0.9	Note 44	nCK	39,40
DQS_t, DQS_c differential READ Preamble (2 clock preamble)	tRPRE2	NA	NA	NA	NA	NA	NA	1.8	Note 44	tCK	39,41
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	Note 45	0.33	Note 45	0.33	Note 45	0.33	Note 45	tCK	39
DQS_t, DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	tCK	21,39

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Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
DQS_t, DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	tCK	20,39
DQS_t, DQS_c differential WRITE Preamble (1 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK	42
DQS_t, DQS_c differential WRITE Preamble (2 clock preamble)	tWPRE2	NA	NA	NA	NA	NA	NA	1.8	-	tCK	43
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ (DQS)	-450	225	-390	195	-360	180	-330	175	ps	39
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ (DQS)	-	225	-	195	-	180	-	175	ps	39
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble)	tDQSS2	NA	NA	NA	NA	NA	NA	-0.5	0.5		43
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)	-	370	-	330	-	310	-	290	ps	37,38,39
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c with DDL on mode	tDQSCK (DLL On)	-225	225	-195	195	-180	180	-175	175	ps	37,38,39
MPSM Timing											

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Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Command path disable delay upon MPSM entry	tMPED	tMOD (min) + tCPDED (min)								tCK	
Valid clock requirement after MPSM entry	tCKMPE	tMOD (min) + tCPDED (min)								tCK	
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX (min)								tCK	
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS (min)								tCK	
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP (min) + tXSDLL (min)								tCK	
CS setup time to CKE	tMPX_S	tISmin + tIHmin								ns	
Calibration Timing											
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	nCK	
Normal operation short calibration Short calibration time	tZQCS	128	-	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing											
Exit Reset from CKE HIGH to a valid command	tXPR	Max (5nCK, tRFC(min) + 10 ns)	-	Max (5nCK, tRFC(min) + 10 ns)	-	Max (5nCK, tRFC(min) + 10 ns)	-	Max (5nCK, tRFC(min) + 10 ns)	-	nCK	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC4 (min) + 10ns	-	tRFC4 (min) + 10 ns	-	tRFC4 (min) + 10 ns	-	tRFC4 (min) + 10 ns	-	nCK	
SRX to Commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT(min)	tRFC4 (min) + 10ns	-	tRFC4 (min) + 10 ns	-	tRFC4 (min) + 10 ns	-	tRFC4 (min) + 10 ns	-	nCK	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST(min)	tRFC4 (min) + 10ns	-	tRFC4 (min) + 10 ns	-	tRFC4 (min) + 10 ns	-	tRFC4 (min) + 10 ns	-	nCK	
Exit Self Refresh to commands requiring a locked	tXSDLL	tDLLK (min)	-	tDLLK (min)	-	tDLLK (min)	-	tDLLK (min)	-	nCK	

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Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
DLL											
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE (min) + 1nCK	-	tCKE (min) + 1nCK	-	tCKE (min) + 1nCK	-	tCKE (min) + 1nCK	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE (min) + 1nCK + PL	-	tCKE (min) + 1nCK + PL	-	tCKE (min) + 1nCK + PL	-	tCKE (min) + 1nCK + PL	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	Max (5nCK, 10 ns)	-	Max (5nCK, 10 ns)	-	Max (5nCK, 10 ns)	-	Max (5nCK, 10 ns)	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	Tcksre_PAR	Max (5nCK, 10 ns) + PL	-	Max (5nCK, 10 ns) + PL	-	Max (5nCK, 10 ns) + PL	-	Max (5nCK, 10 ns) + PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power Down Exit (PDX) or Reset Exit	tCKSRX	Max (5nCK, 10 ns)	-	Max (5nCK, 10 ns)	-	Max (5nCK, 10 ns)	-	Max (5nCK, 10 ns)	-	nCK	
Power Down Timing											
Exit Power Down with DLL on to any valid command, Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	Max (4nCK, 6ns)	-	Max (4nCK, 6ns)	-	Max (4nCK, 6ns)	-	Max (4nCK, 6ns)	-	nCK	
CKE minimum pulse width	tCKE	Max (3nCK, 5ns)	-	Max (3nCK, 5ns)	-	Max (3nCK, 5ns)	-	Max (3nCK, 5ns)	-	nCK	31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE (min)	9*tREFI	tCKE (min)	9*tREFI	tCKE (min)	9*tREFI	tCKE (min)	9*tREFI	nCK	6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL + 4 + (tWR/tCK(avg))	-	WL + 4 + (tWR/tCK(avg))	-	WL + 4 + (tWR/tCK(avg))	-	WL + 4 + (tWR/tCK(avg))	-	nCK	4

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Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL + 2 + (tWR/tCK(avg))	-	WL + 2 + (tWR/tCK(avg))	-	WL + 2 + (tWR/tCK(avg))	-	WL + 2 + (tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD (min)	-	tMOD (min)	-	tMOD (min)	-	tMOD (min)	-	nCK	
PDA Timing											
Mode Register Set command cycle time in PDA mode	tMRD_PDA	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD		nCK	
ODT Timing											
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1	9	1	9	1	9	1	9	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1	9	1	9	1	9	1	9	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	
Write Leveling Timing											
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is	tWLDQSEN	25	-	25	-	25	-	25	-	nCK	12

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Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
programmed											
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE							0	2	ns	
CA Parity Timing											
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	-	PL	nCK	
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL + 6ns	-	PL + 6ns	-	PL + 6ns	-	PL + 6ns	nCK	
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	48	96	56	112	64	128	72	144	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	43	-	50	-	57	-	64	nCK	
Parity Latency	PL	4		4		4		5		nCK	
CRC Error Reporting											
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	6	10	nCK	
tREFI											
tRFC1 (min)	4Gb	260	-	260	-	260	-	260	-	ns	34
tRFC2 (min)	4Gb	160	-	160	-	160	-	160	-	ns	34
tRFC4 (min)	4Gb	110	-	110	-	110	-	110	-	ns	34

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12.4.2 Timing Parameters by Speed Bin for DDR4-2666 to 3200

Table 12-3. Timing Parameters by Speed Bin for DDR4_2666 to 3200

Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	ns	
Average Clock Period	tCK (avg)	0.75	<0.800	0.682	<0.750	0.625	<0.682	ns	35,36
Average high pulse width	tCH (avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK (avg)	
Average low pulse width	tCL (avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK (avg)	
Absolute Clock Period	tCK (abs)	Min = tCK(avg)min + tJIT(per)min_tot						tCK (avg)	
		Max = tCK(avg)max + tJIT(per)max_tot							
Absolute clock HIGH pulse width	tCH (abs)	0.45	-	0.45	-	0.45	-	tCK (avg)	23
Absolute clock LOW pulse width	tCL (abs)	0.45	-	0.45	-	0.45	-	tCK (avg)	24
Clock Period Jitter- total	JIT (per)_tot	-38	38	-34	34	-32	32	ps	25
Clock Period Jitter- deterministic	JIT (per)_dj	-19	19	-17	17	-16	16	ps	26
Clock Period Jitter during DLL locking period	tJIT (per, lck)	-30	30	-27	27	-25	25	ps	
Cycle to Cycle Period Jitter	tJIT (cc)	-	75	-	68	-	62	ps	25
Cycle to Cycle Period Jitter during DLL locking period	tJIT (cc, lck)	-	60	-	55	-	50	ps	
Cumulative error across 2 cycles	tERR (2per)	-55	55	-50	50	-46	46	ps	
Cumulative error across 3 cycles	tERR (3per)	-66	66	-60	60	-55	55	ps	
Cumulative error across 4 cycles	tERR (4per)	-73	73	-66	66	-61	61	ps	
Cumulative error across 5 cycles	tERR (5per)	-78	78	-71	71	-65	65	ps	
Cumulative error across 6 cycles	tERR (6per)	-83	83	-75	75	-69	69	ps	
Cumulative error across 7 cycles	tERR (7per)	-87	87	-79	79	-73	73	ps	
Cumulative error across 8 cycles	tERR (8per)	-91	91	-83	83	-76	76	ps	
Cumulative error across 9 cycles	tERR (9per)	-94	94	-85	85	-78	78	ps	

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Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Cumulative error across 10 cycles	tERR (10per)	-96	96	-88	88	-80	80	ps	
Cumulative error across 11 cycles	tERR (11per)	-99	99	-90	90	-83	83	ps	
Cumulative error across 12 cycles	tERR (12per)	-101	101	-92	92	-84	84	ps	
Cumulative error across 13 cycles	tERR (13per)	-103	103	-93	93	-86	86	ps	
Cumulative error across 14 cycles	tERR (14per)	-104	104	-95	95	-87	87	ps	
Cumulative error across 15 cycles	tERR (15per)	-106	106	-97	97	-89	89	ps	
Cumulative error across 16 cycles	tERR (16per)	-108	108	-98	98	-90	90	ps	
Cumulative error across 17 cycles	tERR (17per)	-110	110	-100	100	-92	92	ps	
Cumulative error across 18 cycles	tERR (18per)	-112	112	-101	101	-93	93	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR (nper)	tERR (nper)min = ((1 + 0.68ln(n)) *tJIT (per)_total min)						ps	
		tERR (nper)max = ((1 + 0.68ln(n)) *tJIT (per)_total max)							
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS (base)	55	-	48	-	40	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS (Vref)	145	-	138	-	130	-	ps	
Command and Address hold time to CK_t,CK_c referenced to Vih(dc) / Vil(dc) levels	tIH (base)	80	-	73	-	65	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH (Vref)	145	-	138	-	130	-	ps	
Control and Address Input pulse width for each input	tIPW	385	-	365	-	340	-	ps	
Command and Address Timing									
CAS_n to CAS_n command delay for same bank group	tCCD_L	Min = Max (5nCK, 5 ns)						nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different	tRRD_S (2K)	Min = Max (4nCK, 5.3 ns)						nCK	34

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Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
bank group for 2KB page size									
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	tRRD_S (1K)	Min = Max (4nCK, 3.0 ns)		Min = Max (4nCK, 2.7 ns)		Min = Max (4nCK, 2.5 ns)		nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/ 2KB page size	tRRD_S (1/2K)	Min = Max (4nCK, 3.0 ns)		Min = Max (4nCK, 2.7 ns)		Min = Max (4nCK, 2.5 ns)		nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L (2K)	Min = Max (4nCK, 6.4 ns)		Min = Max (4nCK, 6.4 ns)		Min = Max (4nCK, 6.4 ns)		nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L (1K)	Min = Max (4nCK, 4.9 ns)		Min = Max (4nCK, 4.9 ns)		Min = Max (4nCK, 4.9 ns)		nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/ 2KB page size	tRRD_L (1/2K)	Min = Max (4nCK, 3.0 ns)		Min = Max (4nCK, 2.7 ns)		Min = Max (4nCK, 2.5 ns)		nCK	34
Four activate window for 2KB page size	tFAW_2K	Min = Max (28nCK, 30 ns)		Min = Max (28nCK, 30 ns)		Min = Max (28nCK, 30 ns)		ns	34
Four activate window for 1KB page size	tFAW_1K	Min = Max (20nCK, 21 ns)		Min = Max (20nCK, 21 ns)		Min = Max (20nCK, 21 ns)		ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Min = Max (16nCK, 12 ns)		Min = Max (16nCK, 10.875 ns)		Min = Max (16nCK, 10 ns)		ns	34
Delay from start of internal Write transaction to internal Read command for different bank group	tWTR_S	Min = Max (2nCK, 2.5 ns)		Min = Max (2nCK, 2.5 ns)		Min = Max (2nCK, 2.5 ns)		ns	1, 2, 34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	Min = Max (4nCK, 7.5 ns)		Min = Max (4nCK, 7.5 ns)		Min = Max (4nCK, 7.5 ns)		ns	1, 34
Internal READ Command to PRE - CHARGE Command delay	tRTP	Min = Max (4nCK, 7.5 ns)		Min = Max (4nCK, 7.5 ns)		Min = Max (4nCK, 7.5 ns)		ns	
WRITE recovery time	tWR	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	Min = tWR + max(5nCK, 3.75 ns)						ns	1, 28
Delay from start of internal Write transaction to internal	tWTR_S_CRC_DM	Min = tWTR_S + max(5nCK, 3.75 ns)						ns	2,,29, 34

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Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
read command for different bank group with both CRC and DM enabled									
Delay from start of internal Write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	Min = tWTR_L + max(5nCK, 3.75 ns)						ns	3, 30, 34
DDL locking time	tDLLK	1024	-	1024	-	1024	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	Min = Max (24nCK, 15 ns) -						nCK	
Mult-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK	33
Mult-Purpose Register Write Recovery Time	tWR_MPR	Min = tMOD (min) + AL + PL						nCK	
Auto precharge write recovery + precharge time	tDAL (min)	Programmed WR +roundup (tRP / tCK(avg))						nCK	
DQ0 or DQL0 driven to set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	UI	45, 47
DQ0 or DQL0 driven to hold time from last DQS falling edge	tPDA_H	0.5	-	0.5	-	0.5	-	UI	46, 47
CS_n to Command Address Latency									
CS_n to Command Address Latency	tCAL	Max (3nCK, 3.748 ns)	-	Max (3nCK, 3.748 ns)	-	Max (3nCK, 3.748 ns)	-	nCK	
Mode Register Set command cycle time in CAL mode	tMRD_tCAL	tMOD + tCAL	-	tMOD + tCAL	-	tMOD + tCAL	-	nCK	
Mode Register Set update delay in CAL mode	tMOD_tCAL	tMOD + tCAL	-	tMOD + tCAL	-	tMOD + tCAL	-	nCK	
DRAM Data Timing									
DQS_t,DQS_c to DQ skew, per group, per acces	tDQSQ	-	0.18	-	0.19	-	TBD	tCK	13,18,39,49

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Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
								(avg)/2	
DQ output hold time from DQS_t, DQS_c	tQH	0.74	-	0.72	-	TBD	-	tCK (avg)/2	17,18,39,49
Data Valid Window per device per UI: (tQH - tDQSQ) of each UI on a given DRAM	tDVWd	0.64	-	TBD	-	TBD	-		
Data Valid Window per pin per UI: (tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.72	-	TBD	-	0.72	-		
DQ low impedance time from CK_t, CK_c	tLZ (DQ)	-310	170	-280	165	-250	160		
DQ high impedance time from CK_t, CK_c	tHZ (DQ)	-	170	-	165	-	160		
Data Strobe Timing									
DQS_t, DQS_c differential READ Preamble (1 clock preamble)	tRPRE	0.9	Note 44	0.9	Note 44	0.9	Note 44	tCK	
DQS_t, DQS_c differential READ Preamble (2 clock preamble)	tRPRE2	1.8	Note 44	1.8	Note 44	1.8	Note 44	tCK	
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	Note 45	0.33	Note 45	0.33	Note 45	tCK	
DQS_t, DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	tCK	21,39
DQS_t, DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	tCK	20,39
DQS_t, DQS_c differential WRITE Preamble (1 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	tCK	42
DQS_t, DQS_c differential WRITE Preamble (2 clock preamble)	tWPRE2	1.8	-	1.8	-	1.8	-	tCK	43
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ (DQS)	-310	170	-280	165	-250	160	ps	39
DQS_t and DQS_c high-impedance time (Referenced	tHZ (DQS)	-	170	-	165	-	160	ps	39

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Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
from RL+BL/2)									
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble)	tDQSS2	-0.5	0.5	TBD	TBD	TBD	TBD		43
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-		
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)	-	270	-	265	-	260	ps	37,38,39
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c with DDL on mode	tDQSCK	-170	170	-165	165	-160	160	ps	37,38,39
MPSM Timing									
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tCK	
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tCK	
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	tCK	
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-	tXS(min)	-	tXS(min)	-	tCK	
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tCK	
CS setup time to CKE	tMPX_S	tISmin + tIHmin	-	tISmin + tIHmin	-	tISmin + tIHmin	-	ns	

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Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Calibration Timing									
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing									
Exit Reset from CKE HIGH to a valid command	tXPR	Min = Max(5nCK, tRFC(min) + 10 ns)							
Exit Self Refresh to commands not requiring a locked DLL	tXS	Min = tRFC (min) + 10ns							
SRX to Commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT(min)	Min = tRFC4 (min) + 10ns							
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST(min)	Min = tRFC4 (min) + 10ns							
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK (min)	-	tDLLK (min)	-	tDLLK (min)	-		
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE (min) + 1nCK	-	tCKE (min) + 1nCK	-	tCKE (min) + 1nCK	-		
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE (min) + 1nCK + PL	-	tCKE (min) + 1nCK + PL	-	tCKE (min) + 1nCK + PL	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	Max (5nCK, 10 ns)	-	Max (5nCK, 10 ns)	-	Max (5nCK, 10 ns)	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	Tcksre_PAR	Max (5nCK, 10 ns) + PL	-	Max (5nCK, 10 ns) + PL	-	Max (5nCK, 10 ns) + PL	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power Down Exit (PDX) or Reset Exit	tCKSRX	Max (5nCK, 10 ns)	-	Max (5nCK, 10 ns)	-	Max (5nCK, 10 ns)	-		

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Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Power Down Timing									
Exit Power Down with DLL on to any valid command, Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	Max (4nCK, 6ns)	-	Max (4nCK, 6ns)	-	Max (4nCK, 6ns)	-		
CKE minimum pulse width	tCKE	Max (3nCK, 5ns)	-	Max (3nCK, 5ns)	-	Max (3nCK, 5ns)	-		31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE (min)	9*tREFI	tCKE (min)	9*tREFI	tCKE (min)	9*tREFI		6
Timing of ACT command to Power Down entry	tACTPDEN	2	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	Min = RL + 4 + 1						nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	Min = WL + 4 + (tWR/tCK(avg))						nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	Min = WL + 4 + WR + 1						nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	Min = WL + 2 + (tWR/tCK(avg))						nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	Min = WL + 2 + WR + 1						nCK	5
Timing of REF command to Power Down entry	tREFPDEN	2	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD (min)	-	tMOD (min)	-	tMOD (min)	-		
Mode Register Set command cycle time in PDA mode	tMRD_PDA	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-		
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD			
Asynchronous RTT turn-on delay (Power-Down with DLL	tAONAS	1	9	1	9	1	9	ns	

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Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
frozen)									
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1	9	1	9	1	9	ns	
RTT dynamic change skew	tADC	0.28	0.72	0.26	0.74	0.26	0.74	tCK(avg)	
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_crossing	tWLH	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	0.95	0	0.95	0	9.5	ns	
Write leveling output error	tWLOE	-	2	-	2	-	2	ns	
CA Parity Timing									
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	nCK	
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL + 6ns	-	PL + 6ns	-	PL + 6ns	nCK	
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	80	160	88	176	96	192	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	71	-	78	-	85	nCK	
Parity Latency	PL	5		6		6		nCK	
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	nCK	
Gear Down Timing									

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Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR	tXPR	-	tXPR	-	tXPR	-		
CKE High Assert to Gear Down Enable time (T2/CKE)	tXS_GEAR	tXS	-	tXS	-	tXS	-		
MRS command to Sync pulse time(T3)	tSYNC_GEAR	tMOD +4nCK	-	tMOD +4nCK	-	tMOD +4nCK	-		27
Sync pulse to First valid command(T4)	tCMD_GEAR	tMOD	-	tMOD	-	tMOD	-		27
Geardown setup time	tGEAR setup	2	-		-	2	-	nCK	
Geardown hold time	tGEAR hold	2	-		-	2	-	nCK	
tREFI									
tRFC1 (min)	4Gb	260	-	260	-	260	-	ns	34
tRFC2 (min)	4Gb	160	-	160	-	160	-	ns	34
tRFC4 (min)	4Gb	110	-	110	-	110	-	ns	34

Note:

1. Start of internal Write transaction is defined as follows:
   - For BL8 (Fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.
   - For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.
   - For BC4 (Fixed by MRS): Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from Write to Read when CRC and DM are simultaneously enabled.
3. Commands requiring a locked DLL are Read (and Read Auto Precharge) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK following rouding algorithm defined in Section 12.5.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on $T_{OPER.}$
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied.

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9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10. When CRC and DM are both enabled, tWTR_S_CRC_DM is used in place of tWTR_S.
11. When CRC and DM are both enabled, tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max value are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement.
14. The deterministic component of the total timing. Measurement method TBD.
15. DQ to DQ static offset relative to strobe per group. Measurement method TBD.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example TBD.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.
21. tQSL describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI.
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are TBD.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27. This parameter has to be even number of clocks.
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered Low, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered High, CKE signal level shall be maintained above VIHDC for tCKE specification (High pulse width).
33. Defined between end of MPR Read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the “Speed Bin”.
35. This parameter must keep consistency with “Speed Bin”.

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36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate. UI=tCK(avg)min/2.
37. Applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM.
39. Value is only valid for RONNOM = 34Ω.
40. 1tCK toggle mode with setting MR4:A11 to 0.
41. 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
42. 1tCK mode with setting MR4:A12 to 0.
43. 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
44. The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. See “Clock to Data Strobe Relationship" of DDR4 Operation Guide Boundary of DQS Low-Z occur one cycle earlier in 2tCK toggle mode which is illustrated in “Read Preamble“.
45. DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point.
46. Last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High
47. VerfDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.
48. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See “Clock to Data Strobe Relationship" of DDR4 Operation Guide.
49. Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately 0.7 * VDDQ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to VTT = VDDQ.
50. For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.

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12.5 Rounding Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 933.33 MHz, or a clock period of 1.0714 ns. Similarly, a system with a memory clock frequency of 1066.66 MHz yields mathematically a clock period of 0.9375 ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be done because the DDR4 SDRAM specification establishes a minimum granularity for timing parameters of 1 ps.

Rules for rounding must be defined to allow optimization of device performance without violating device parameters. These algorithms rely on results that are within correction factors on device testing and specification to avoid losing performance due to rounding errors.

These rules are:

- Clock periods such as tCKAVGmin are defined to 1 ps of accuracy; for example, 0.9375... ns is defined as 937 ps and 1.0714 ns is defined as 1071 ps.
- Using real math, parameters like tAAmin, tRCDmin, etc. which are programmed in systems in numbers of clocks (nCK) but expressed in units of time (in ns) are divided by the clock period (in ns) yielding a unitless ratio, a correction factor of 2.5% is subtracted, then the result is set to the next higher integer number of clocks:
  nCK = ceiling [(parameter_in_ns / application_tCK_ in_ns) - 0.025]
- Alternatively, programmers may prefer to use integer math instead of real math by expressing timing in ps, scaling the desired parameter value by 1000, dividing by the application clock period, adding an inverse correction factor of 97.4%, dividing the result by 1000, then truncating down to the next lower integer value:
  nCK = truncate [{(parameter_in_ps x 1000) / (application_tCK_in_ps) + 974} / 1000]
- Either algorithm yields identical results. In case of conflict between results, the preferred algorithm is the integer math algorithm.
- This algorithm applies to all timing parameters documented in a Serial Presence Detect(SPD) when converting from ns to nCK. Other timing parameters may use a simpler algorithm:
  nCK = ceiling (parameter_in_ns ÷ application_tCK_in_ns).

12.6 The DQ Input Receiver Compliance Mask for Voltage and Timing

The DQ input receiver compliance mask for voltage and timing is shown in Figure 12-2 below. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DRAM input receiver to be able to successfully capture a valid input signal with BER of 1e-16; Any input signal encroaching within the Rx Mask is subject to being invalid data. The Rx Mask is the receiver property for each DQ input pin and it is not the valid data-eye.

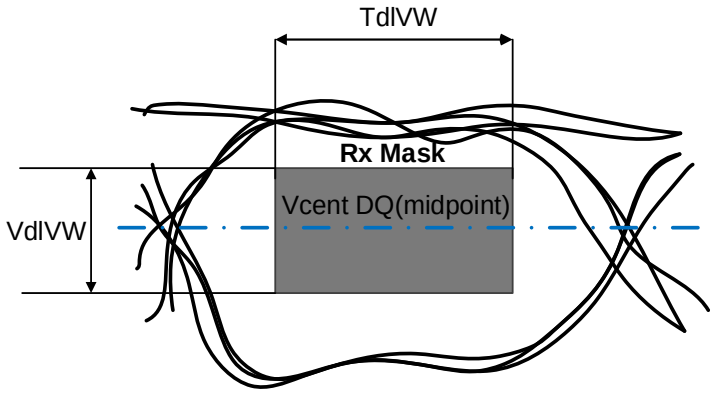


Figure 12-2. DQ Receiver(Rx) Compliance mask

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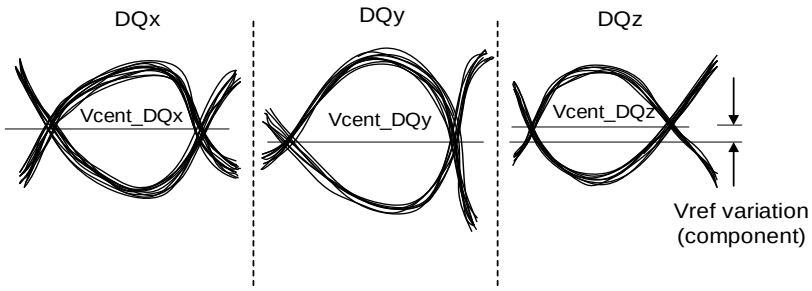


Figure 12-3. Across Pin Vref DQ Voltage Variation

The Vref_DQ voltage is an internal reference voltage level that shall be set to the properly trained setting, which is generally Vcent_DQ(midpoint), in order to have valid Rx Mask values.

Vcent_DQ(pin avg) is defined as the midpoint between the largest Vref_DQ voltage level and the smallest Vref_DQ voltage level across all DQ pins for a given DRAM component. Each DQ pin Vref level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 12-3. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level Vref will be set by the system to account for RON and ODT settings.

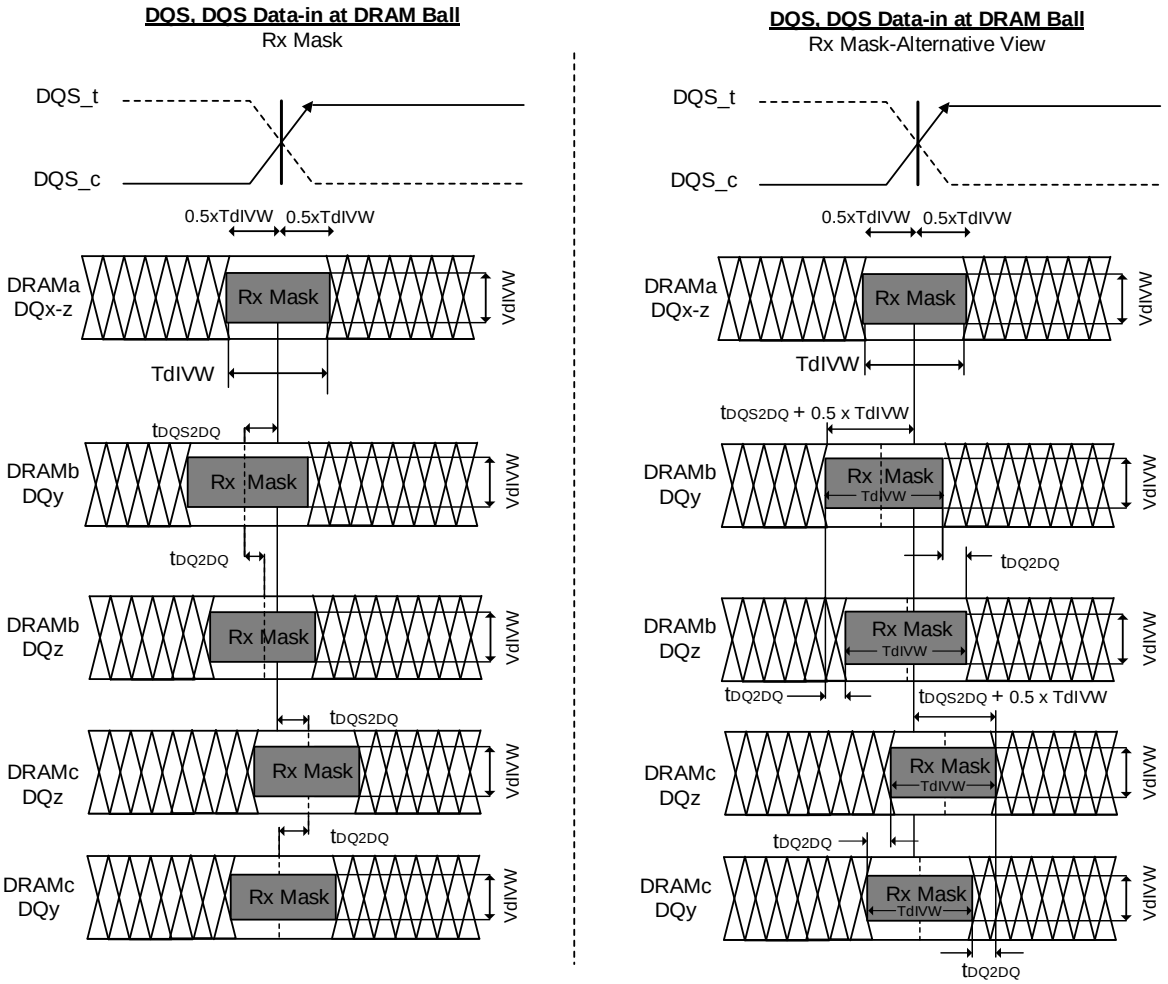


Figure 12-4. DQS to DQ and DQ to DQ Timings at DRAM Balls

Note:

- DQx represents an optimally centered mask.
- DQy represents earliest valid mask.
- DQz represents lasted valid mask.

Note:

- DRAMa represents a DRAM without any DQS/DQ skews.
- DRAMb represents a DRAM with early skews (negative t_{DQS2DQ}).
- DRAMc represents a DRAM with delayed skews (positive t_{DQS2DQ}).

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Note:

1. Figures show skew allowed between DRAM to DRAM and DQ to DQ for a DRAM. Signals assume data centered aligned at DRAM Latch.
2. TdiPW is not shown; composite data-eyes shown would violate TdiPW.
3. VCENT DQ(midpoint) is not shown but is assumed to be midpoint of VdiVW.

All of the timing term in

are measured at the VdiVW voltage levels centered around

Vcent_DQ(midpoint) and are referenced to the DQS_t/DQS_c center aligned to the DQ per pin.

The rising edge slew rates are defined by srr1 and srr2. The slew rate measurement points for a rising edge are shown in Figure 12- below: A low to high transition tr1 is measured from 0.5*VdiVW(max) below Vcent_DQ(midpoint) to the last transition through 0.5*VdiVW(max) above Vcent_DQ(midpoint) to the first transition through the 0.5*VIHL_AC(min) above Vcent_DQ(midpoint).

Rising edge slew rate equations:

- srr1 = VdIVW(max) / tr1
- srr2 = (VIHL_AC(min) – VdIVW(max)) / (2*tr2)

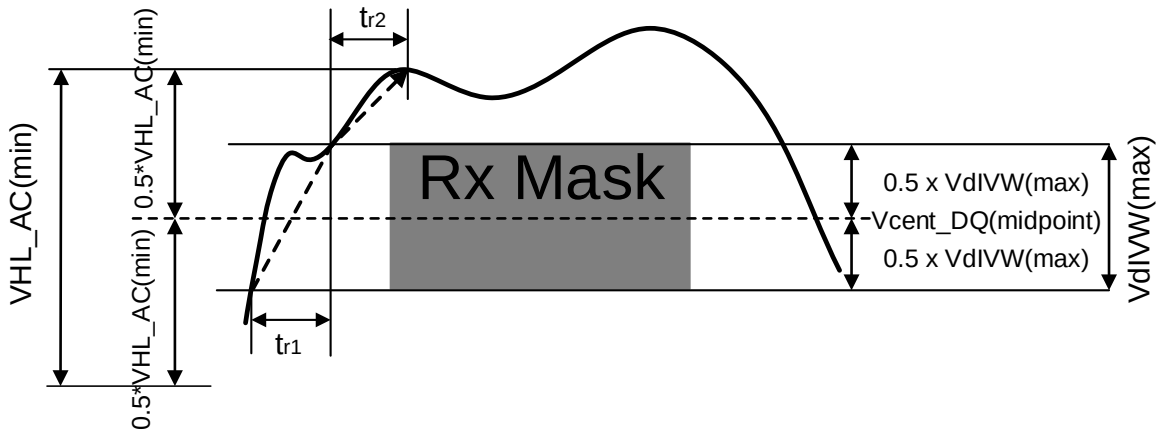


Figure 12-5. Slew Rate Conditions for Rising Transition

The falling edge slew rates are defined by srf1 and srf2. The slew rate measurement points for a falling edge are shown in Figure 12- below: A high to low transition tf1 is measured from 0.5*VdiVW(max) above Vcent_DQ(midpoint) to the last transition through 0.5*VdiVW(max) below Vcent_DQ(midpoint) while tf2 is measured from the last transition through 0.5*VdiVW(max) below Vcent_DQ(midpoint) to the first transition through the 0.5*VIHL_AC(min) below Vcent_DQ(pin mid).

Falling edge slew rate equations:

- srf1 = VdIVW(max) / tf1
- srf2 = (VIHL_AC(min) – VdIVW(max)) / (2*tf2)

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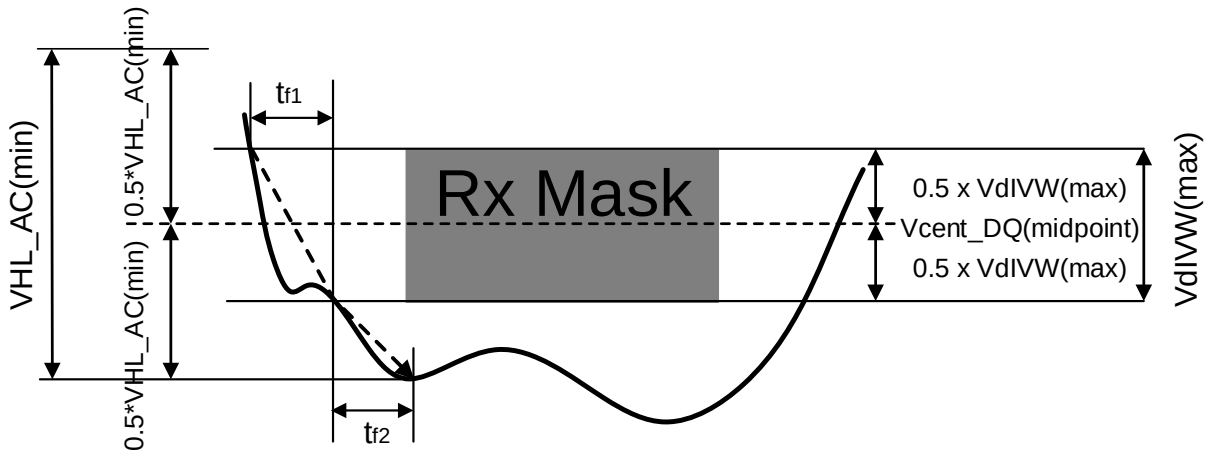


Figure 12-6. Slew Rate Conditions for Falling Transition

Table 12-4. DRAM DQS in Receive Mode; * UI=tck(avg)min/2

Symbol	Parameter	1600/1866/2133		2400		2666		Unit	Note
		Min	Max	Min	Max	Min	Max		
VdIVW	Rx Mask voltage – pK-pK	-	136	-	130	-	120	mV	1,2,10
TdIVW	Rx timing window	-	0.2	-	0.2	-	0.22	UI*	1,2,10
VIHL_AC	DQ AC input swing pk-pk	186	-	160	-	150	-	mV	3,4,10
TdIPW	DQ input pulse width	0.58	-	0.58	-	0.58	-	UI*	5,10
tDQS2DQ	Rx Mask DQS to DQ offset	-0.17	0.17	-0.17	0.17	-0.19	0.19	UI*	6,10
tDQ2DQ	Rx Mask DQ to DQ offset	-	TBD	-	TBD	-	0.105	UI*	7
srr1	Input Slew Rate over VdIVW if tCK >=0.937ns	1.0	9	1.0	9	1	9	V/ns	8,10,
srf1	Input Slew Rate over VdIVW if 0.937ns > tCK >= 0.625ns	-	-	1.25	9	1.25	9	V/ns	8,10,
srr2	Rising Input Slew Rate over 1/2 VIHL_AC	0.2*srr1	9	0.2*srr1	9	0.2*srr1	9	V/ns	9,10,
srf2	Falling Input Slew Rate over 1/2 VIHL_AC	0.2*srf1	9	0.2*srr1	9	0.2*srr1	9	V/ns	9,10,

Note:

1. Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ (midpoint) after VrefDQ training is completed. The data Rx mask is applied per bit and should include voltage and temperature drift terms. The input buffer design specification is to achieve at least a BER = e-16 when the Rx mask is not violated. The BER will be characterized and extrapolated if necessary using a dual dirac method from a higher BER(tbd)
2. Defined over the DQ internal Vref range 1.

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3. Overshoot and Undershoot Specifications see “AC Overshoot Specification for Data, Strobe and Mask”
4. DQ input pulse signal swing into the receiver must meet or exceed VIHL AC(min). VIHL_AC(min) is to be achieved on an UI basis when a rising and falling edge occur in the same UI, i.e. a valid TdiPW.
5. DQ minimum input pulse width defined at the Vcent_DQ(midpoint).
6. DQS to DQ offset is skew between DQS and DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls over process, voltage, and temperature.
7. DQ to DQ offset is skew between DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls for a given component over process, voltage, and temperature.
8. Input slew rate over VdIVW Mask centered at Vcent_DQ(midpoint). Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within 1.7 V/ns of each other.
9. Input slew rate between VdIVW Mask edge and VIHL_AC(min) points.
10. All Rx Mask specifications must be satisfied for each UI. For example, if the minimum input pulse width is violated when satisfying TdiVW(min), VdiVW(max), and minimum slew rate limits, then either TdiVW(min) or minimum slew rates would have to be increased to the point where the minimum input pulse width would no longer be violated.

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12.7 Command, Control, and Address Setup, Hold, and Derating

The total tIS (setup time) and tIH (hold time) required is calculated to account for slew rate variation by adding the data sheet tIS (base) values, the VIL(AC)/VIH(AC) points, and tIH (base) values, the VIL(DC)/VIH(DC) points; to the ΔtIS and ΔtIH derating values, respectively. The base values are derived with single-end signals at 1V/ns and differential clock at 2V/ns. Example: tIS (total setup time) = tIS (base) + ΔtIS. For a valid transition, the input signal has to remain above/ below VIH(AC)/VIL(AC) for the time defined by tVAC.

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached VIH(AC)/VIL(AC) at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach VIH(AC)/VIL(AC). For slew rates that fall between the values listed in derating tables, the derating values may be obtained by linear interpolation.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VIH(AC)min that does not ring back below VIH(DC)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VIL(AC)max that does not ring back above VIL(DC)max. Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VIH(AC)min that does not ring back below VIH(DC)min.

Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VIL(AC)min that does not ring back above VIL(DC)max.

Table 12-5. Command, Address, Control Setup and Hold Values

DDR4	1600	1866	2133	2400	2666	2933	3200	Unit	Reference
tIS(base, AC100)	115	100	80	62	-	-	-	ps	VIH/L(ac)
tIH(base, DC75)	140	125	105	87	-	-	-	ps	VIH/L(dc)
tIS(base, AC90)	-	-	-	-	55	TBD	TBD	ps	VIH/L(ac)
tIH(base, DC65)	-	-	-	-	80	TBD	TBD	ps	VIH/L(dc)
tIS/Tih@ VREF	215	200	180	162	145	TBD	TBD	ps	

Note:

1. Base ac/dc referenced for 1 V/ns slew rate and 2 V/ns clock slew rate.
2. Values listed are referenced only; applicable limits are defined elsewhere.

Table 12-6. Command, Address, Control Input Voltage Values

DDR4	1600	1866	2133	2400	2666	2933	3200	Unit	Reference
VIH. CA(AC)min	100	100	100	100	90	TBD	TBD	mV	VIH/L(ac)
VIH. CA(DC)min	75	75	75	75	65	TBD	TBD	mV	VIH/L(dc)
VIL. CA(DC)max	-75	-75	-75	-75	-65	TBD	TBD	mV	VIH/L(ac)
VIL. CA(AC)max	-100	-100	-100	-100	-90	TBD	TBD	mV	VIH/L(dc)

Note:

1. Command, Address, Control input levels relative to VREFCA.
2. Values listed are referenced only; applicable limits are defined elsewhere.

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Table 12-7. Derating Values DDR4-1600/1866/2133/2400 tIS/tIH-ac/dc Based

△ tIS, △ tIH derating in [ps] AC/DC Based[1]																	
		CK_t, CK_c Differential Slew Rate															
		10.0 V/ns		8.0 V/ns		6.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.5 V/ns		1.0 V/ns	
		tIS	tIH	tIS	tIH	tIS	tIH	tIS	tIH	tIS	tIH	tIS	tIH	tIS	tIH	tIS	tIH
ADDR, CNTL Input Slew Rate V/ns	7	76	54	76	55	77	56	79	58	82	60	86	64	94	73	111	89
	6	73	53	74	53	75	54	77	56	79	58	83	63	92	71	108	88
	5	70	50	71	51	72	52	74	54	76	56	80	60	88	68	105	85
	4	65	46	66	47	67	48	69	50	71	52	75	56	83	65	100	81
	3	57	40	57	41	58	42	60	44	63	46	67	50	75	58	92	75
	2	40	28	41	28	42	29	44	31	46	33	50	38	58	46	75	63
	1.5	23	15	24	16	25	17	27	19	29	21	33	25	42	33	58	50
	1	-10	-10	-9	-9	-8	-8	-6	-6	-4	-4	0	0	8	8	25	25
	0.9	-17	-14	-16	-14	-15	-13	-13	-10	-11	-8	-7	-4	1	4	18	21
	0.8	-26	-19	-25	-19	-24	-18	-22	-16	-20	-14	-16	-9	-7	-1	9	16
	0.7	-37	-26	-36	-25	-35	-24	-33	-22	-31	-20	-27	-16	-18	-8	-2	9
	0.6	-52	-35	-51	-34	-50	-33	-48	-31	-46	-29	-42	-25	-33	-17	-17	0
	0.5	-73	-48	-72	-47	-71	-46	-69	-44	-67	-42	-63	-38	-54	-29	-38	-13
	0.4	-104	-66	-103	-66	-102	-65	-100	-63	-98	-60	-94	-56	-85-	-48	-69	-31

Note:

1. VIH/L(ac) = ± 100mV, VIH/L(dc) = ± 75mV; relative to VREFCA.

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Table 12-8. Derating Values DDR4-2666/2933/3200 tIS/tIH-ac/dc Based

△ tIS, △ tIH derating in [ps] AC/DC Based[1]																	
		CK_t, CK_c Differential Slew Rate															
		10.0 V/ns		8.0 V/ns		6.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.5 V/ns		1.0 V/ns	
		tIS	tIH	tIS	tIH	tIS	tIH	tIS	tIH	tIS	tIH	tIS	tIH	tIS	tIH	tIS	tIH
ADDR, CNTL Input Slew Rate V/ns	7	68	47	69	47	70	48	72	50	73	52	77	56	85	63	100	78
	6	66	45	67	46	68	47	69	49	71	50	75	54	83	62	98	77
	5	63	43	64	44	65	45	66	46	68	48	72	52	80	60	95	75
	4	59	40	59	40	60	41	62	43	64	45	68	49	75	56	90	71
	3	51	34	52	35	53	36	54	38	56	40	60	43	68	51	83	66
	2	36	24	37	24	38	25	39	27	41	29	45	33	53	40	68	55
	1.5	21	13	22	13	23	14	24	16	26	18	30	22	38	29	53	44
	1	-9	-9	-8	-8	-8	-8	-6	-6	-4	-4	0	0	8	8	23	23
	0.9	-15	-13	-15	-12	-14	-11	-12	-9	-10	-7	-6	-4	1	4	16	19
	0.8	-23	-17	-23	-17	-22	-16	-20	-14	-18	-12	-14	-8	-7	-1	8	14
	0.7	-34	-23	-33	-22	-32	-21	-30	-20	-28	-18	-25	-14	-17	-6	-2	9
	0.6	-47	-31	-47	-30	-46	-29	-44	-27	-42	-25	-38	-22	-31	-14	-16	1
	0.5	-67	-42	-66	-41	-65	-40	-63	-38	-61	-36	-58	-33	-50	-25	-35	-10
	0.4	-95	-58	-95	-57	-94	-56	-92	-54	-90	-53	-86	-49	-79	-41	-64	-26

Note:

1. VIH/L(ac) = ± tbd mV, VIH/L(dc) = ± tbd mV; relative to VREFCA.

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13 REVISION HISTORY

Version No	Description	Page	Date
1.0	Initial release	All	2021-4-28
1.1	Update Pad name description and extend the operating temperature from -40 to 95 ℃	5/14/46	2021-7-21
1.2	Update the IDD, IDDQ and IPP Specifications of DDR4-2400/2666/3200 speed grade	72/73	2021-9-13
1.3	Update functional block diagram	14	2021-11-2
1.4	Update some details about speed bins and operations; Update some details about Measurement-Loop Pattern Update some details about input/output capacitance; Update some details about timing parameters by speed bin.	P41/P42/P43/P44 P59/P65 P75/P76 P80/P81/P86	2022-3-9

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