GD5F2GM7xExxG

DATASHEET

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1 FEATURE

◆ 2Gb SLC NAND Flash

◆ Page Size
- Internal ECC On (ECC_EN=1, default):
Page Size：2048-Byte+64-Byte
- Internal ECC Off (ECC_EN=0):
Page Size：2048-Byte+128-Byte

◆ Standard, Dual, Quad SPI,DTR
- Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
- Dual SPI: SCLK, CS#, SIO0, SIO1, WP#, HOLD#
- Quad SPI: SCLK, CS#, SIO0, SIO1, SIO2, SIO3
- DTR(Double Transfer Rate) Read : SCLK, CS#, SIO0, SIO1, SIO2, SIO3

◆ High Speed Clock Frequency
- 3.3V:
133MHz for Standard/Dual/Quad SPI
104MHz for DTR Quad SPI
- 1.8V:
104MHz for Standard/Dual/Quad SPI
80MHz for DTR Quad SPI

◆ Software/Hardware Write Protection
- Write protect all/portion of memory via software
- Register protection with WP# Pin
- Power Lock Down Protection

◆ Single Power Supply Voltage
- Full voltage range for 1.8V: 1.7V ~ 2.0V
- Full voltage range for 3.3V: 2.7V ~ 3.6V

◆ Advanced security Features
- 20K-Byte OTP Region

◆ Program/Erase/Read Speed
- Page Program time: 320us typical
- Block Erase time: 3ms typical
- Page read time: 120us maximum

◆ Low Power Consumption
- 30mA maximum active current
- 50uA maximum standby current

◆ Enhanced access performance
- 2Kbyte cache for fast random read

◆ Advanced Feature for NAND
- Factory good block0
- Deep Power Down (1.8V only)

◆ Reliability
- P/E cycles with ECC: Typical 80K(2)
- Data retention: 10 Years

◆ Internal ECC
- 8bits /528byte

Note:1. ECC is On as default, and it can be disabled by the user.
2. The P/E cycles with ECC will be 60K at 105℃ operation temperature.

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2 GENERAL DESCRIPTION

SPI (Serial Peripheral Interface) NAND Flash provides an ultra-cost effective while high density non-volatile memory storage solution for embedded systems, based on an industry-standard NAND Flash memory core. It is an attractive alternative to SPI-NOR and standard parallel NAND Flash, with advanced features.

- Total pin count is 8, including VCC and GND
- Density is 2Gb
- Superior write performance and cost per bit over SPI-NOR
- Significant low cost than parallel NAND

This low-pin-count NAND Flash memory follows the industry-standard serial peripheral interface, and always remains the same pin out from one density to another. The command sets resemble common SPI-NOR command sets, modified to handle NAND specific functions and added new features. GigaDevice SPI NAND is an easy-to-integrate NAND Flash memory, with specified designed features to ease host management:

- **User-selectable internal ECC**. ECC parity is generated internally during a page program operation. When a page is read to the cache register, the ECC parity is detected and corrects the errors when necessary. The 64-bytes spare area is available even when internal ECC enabled. The device outputs corrected data and returns an ECC error status.
- **Internal data move or copy back with internal ECC**. The device can be easily refreshed and manage garbage collection task, without need of shift in and out of data. This command string can only be used on blocks with the same parity attribute.
- **Power on Read with internal ECC**. The device will automatically read first page of fist block to cache after power on, then host can directly read data from cache for easy boot. Also the data is promised correct by internal ECC when ECC enabled.

It is programmed and read in page-based operations, and erased in block-based operations. Data is transferred to or from the NAND Flash memory array, page by page, to a data register and a cache register. The cache register is closest to I/O control circuits and acts as a data buffer for the I/O data; the data register is closest to the memory array and acts as a data buffer for the NAND Flash memory array operation. The cache register functions as the buffer memory to enable page and random data READ/WRITE and copy back operations. These devices also use a SPI status register that reports the status of device operation.

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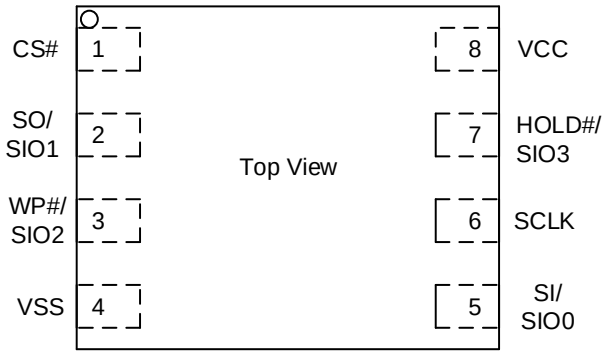
2.1 VALID PART NUMBERS

Please contact GigaDevice regional sales for the latest product selection and available form factors

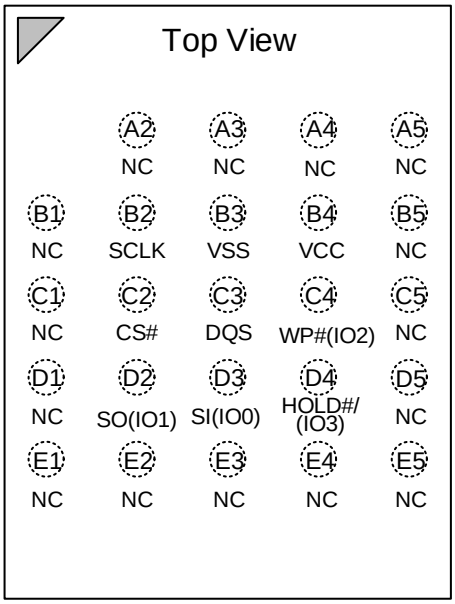
Product Number	Density	Voltage	Package Type	Temperature
GD5F2GM7REYIG	2Gbit	1.7V to 2.0V	WSON8(8*6mm)	-40℃ to 85℃
GD5F2GM7REBIG			TFBGA24(5*5 Ball Array)	-40℃ to 85℃
GD5F2GM7REWIG			WSON8(6*5mm)	-40℃ to 85℃
GD5F2GM7UEYIG		2.7V to 3.6V	WSON8(8*6mm)	-40℃ to 85℃
GD5F2GM7UEBIG			TFBGA24(5*5 Ball Array)	-40℃ to 85℃
GD5F2GM7UEWIG			WSON8(6*5mm)	-40℃ to 85℃
GD5F2GM7REYJG	2Gbit	1.7V to 2.0V	WSON8(8*6mm)	-40℃ to 105℃
GD5F2GM7UEYJG	2Gbit	2.7V to 3.6V	WSON8(8*6mm)	-40℃ to 105℃

2.2 CONNECTION DIAGRAM

Figure 2-1. Connect Diagram



8 - LEAD WSON



24-BALL TFBGA (5x5 ball array)

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2.3 PIN DESCRIPTION

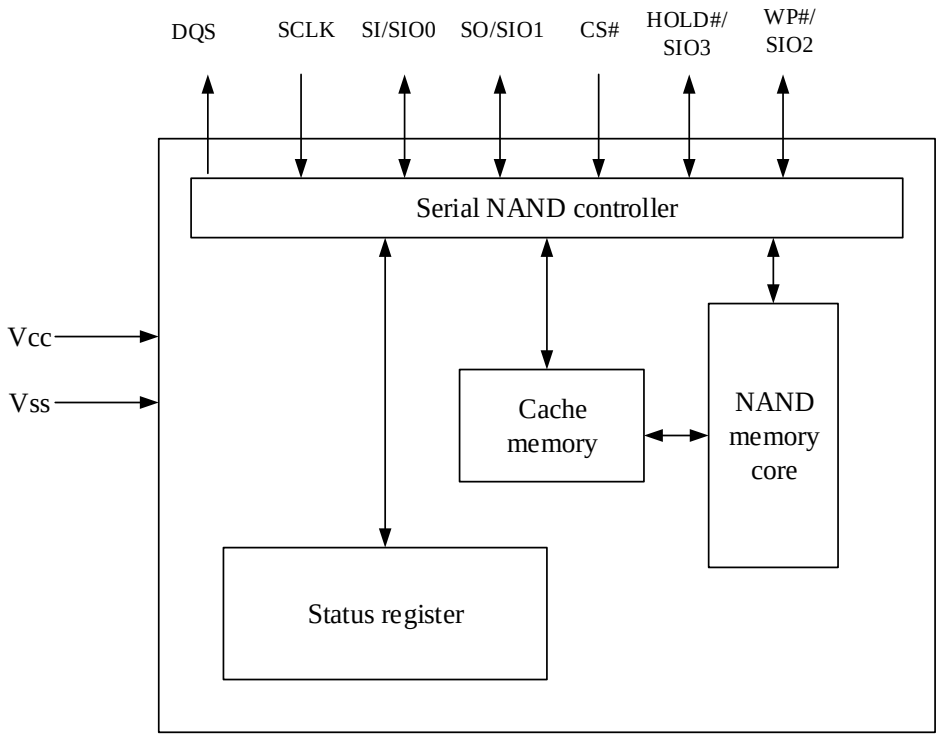
Pin Name	I/O	Description
CS#	**I**	Chip Select input, active low
SO/SIO1	**I/O**	Serial Data Output / Serial Data Input Output 1
WP#/SIO2	**I/O**	Write Protect, active low / Serial Data Input Output 2
VSS	**Ground**	Ground
SI/SIO0	**I/O**	Serial Data Input / Serial Data Input Output 0
SCLK	**I**	Serial Clock input
HOLD# /SIO3	**I/O**	Hold Input/Serial Data Input Output 3
VCC	**Supply**	Power Supply
NC		Not Connect, Not internal connection; can be driven or floated.
DQS (only for BGA24)	**O**	Data Strobe Signal Output

Note：

1. CS# must be driven high if chip is not selected. Please don't leave CS# floating any time after power is on.
2. If the DQS Function is not used, this pin must be floating.
3. If WP# and HOLD# are unused, they must be driven high by the host, or an external pull-up resistor must be placed on the PCB in order to avoid allowing WP# and HOLD# input to float.

2.4 BLOCK DIAGRAM

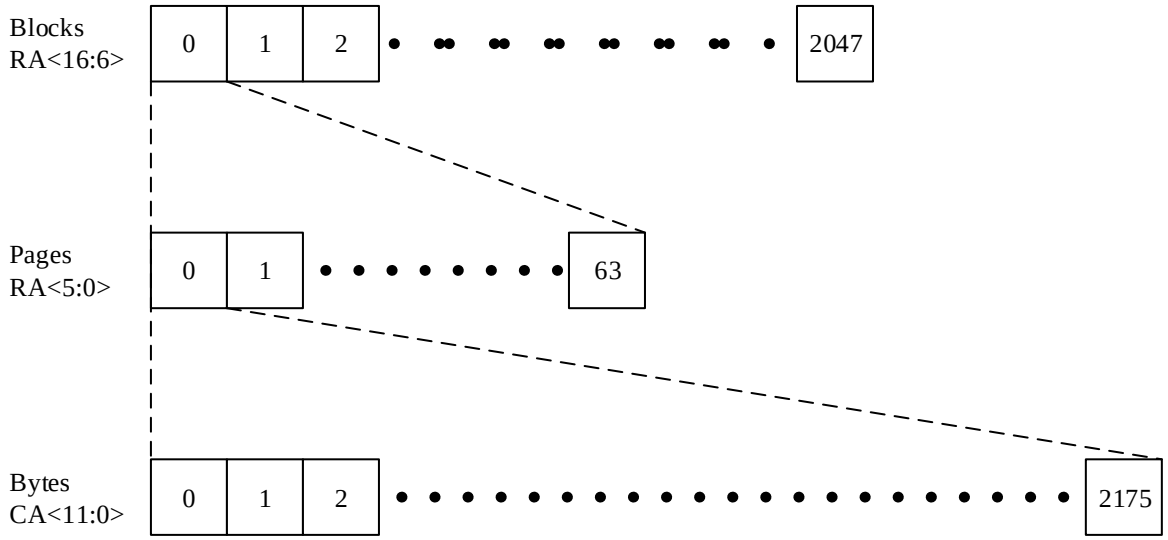
Figure 2-2. Block Diagram



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3 MEMORY MAPPING

For 2G



Note:

1. CA: Column Address. The 12-bit address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2175/2111 are valid. Bytes 2176/2112 through 4095 of each page are “out of bounds,” do not exist in the device, and cannot be addressed.
2. RA: Row Address. RA<5:0>selects a page inside a block, and RA<16:6>selects a block.

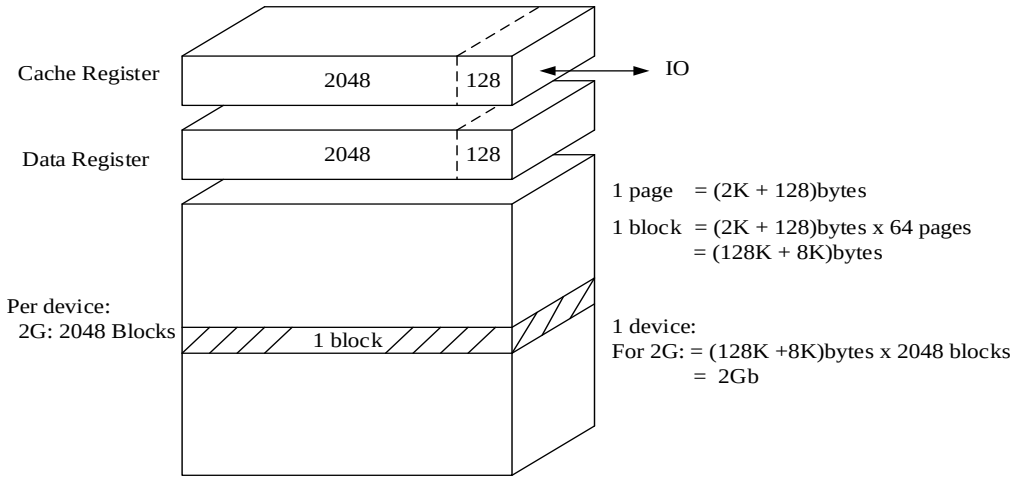
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4 ARRAY ORGANIZATION

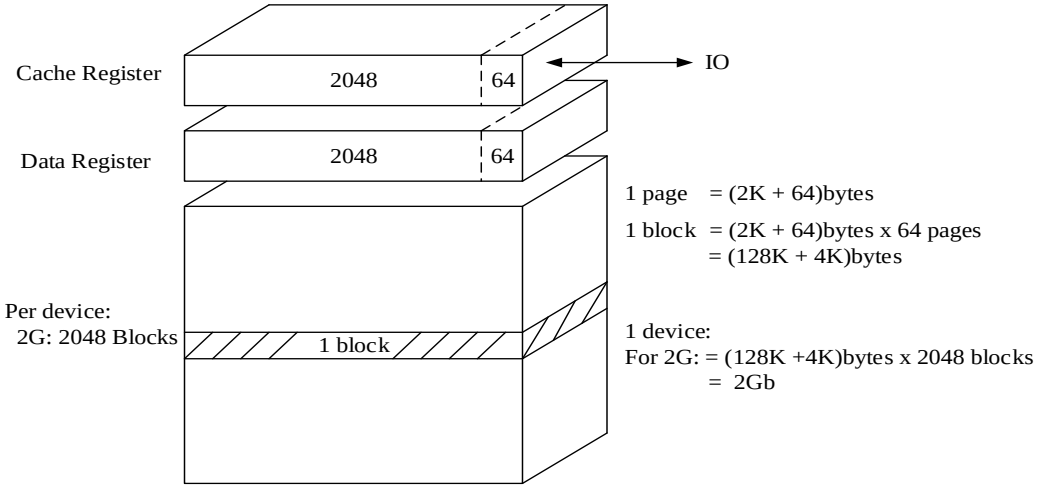
Table 4. Array Organization

Each device has	Each block has	Each page has	
2Gb			
256M+16M	128K+8K	2K+128	bytes
2048 x 64	64	-	pages
2048	-	-	blocks

Figure 4. Array Organization



Internal ECC = OFF



Internal ECC = ON

Note:

1.When Internal ECC is enabled，user can program the first 64 bytes of the entire 128 bytes spare area and the last 64 bytes of the whole spare area cannot be programed，user can read the entire 128 Byte spare area.

2.When Internal ECC is disabled，user can read and program the entire 128 bytes spare area.

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5 DEVICE OPERATION

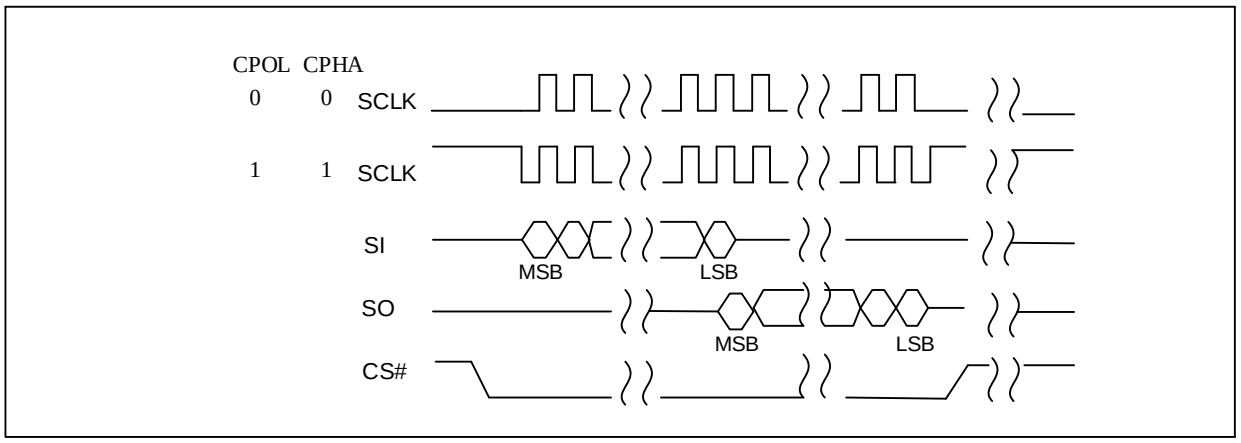
5.1 SPI Modes

SPI NAND supports two SPI modes:

- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK for both modes. All timing diagrams shown in this data sheet are mode 0. See Figure 5-1 for more details.

Figure 5-1. SPI Modes Sequence Diagram



Note: While CS# is HIGH, keep SCLK at VCC or GND (determined by mode 0 or mode 3). Do not toggle SCLK until CS# is driven LOW.

We recommend that the user pull CS# to high when user don't use SPI flash, otherwise the flash is always in the read state, which is damage for flash.

When CS# is high and SCLK at VCC or GND state, the device is in idle state.

Standard SPI

SPI NAND Flash features a standard serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO).

Dual SPI

SPI NAND Flash supports Dual SPI operation when using the x2 and dual IO commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1.

Quad SPI

SPI NAND Flash supports Quad SPI operation when using the x4 and Quad IO commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1, and WP# and HOLD# pins become SIO2 and SIO3.

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DTR Quad SPI

The device supports DTR Quad SPI operation when using the “DTR Quad I/O Fast Read” command.

These command allow data to be transferred to or from the device at eight times the rate of the standard SPI, and data output will be latched on both rising and falling edges of the serial clock. When using the DTR Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3. DTR Quad SPI commands require the Quad Enable bit (QE) in Status Register to be enable.

5.2 HOLD Mode

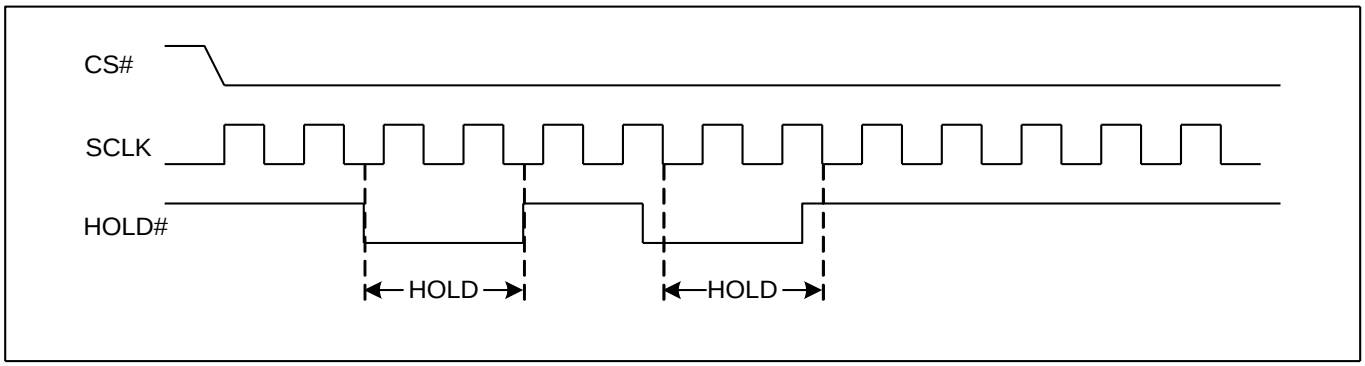
The HOLD# function is only available when QE=0, If QE=1, The HOLD# functions is disabled, the pin acts as dedicated data I/O pin.

The HOLD# signal goes low to stop any serial communications with the device, but doesn’t stop the operation of reading, programming, or erasing in progress.

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

The SO is high impedance, both SI and SCLK don’t care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

Figure 5-2. Hold Condition



5.3 Write Protection

SPI NAND provides Hardware Protection Mode besides the Software Mode. Write Protect (WP#) prevents the block lock bits (BP0, BP1, BP2 and INV, CMP) from being over written. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits cannot be altered.

To enable the Write Protection, the Quad Enable bit (QE) of feature (B0[0]) must be set to 0.

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5.4 Power Off Timing

Please do not turn off the power before Write/Erase operation is completed. Avoid using the device when the battery is low. Power shortage and/or power failure before Write/Erase operation is complete will cause loss of data and/or damage to data.

5.5 Data Strobe (DQS) signal (BGA24 only)

The DQS signal is an active output pin for the Data Strobe (DQS) signal during Read operations. The DQS signal is typically used in high speed applications to indicate when the output data is ready to be fetched by the controllers. To achieve such high frequency for specific DTR command, DQS pin is enabled on BGA24 package of this device. DQS is only available in EEh command.

DQS signal is driven to ground once EEh command is accepted, and will start to toggle when the output data is ready on the I/O pins under DTR mode. The toggling frequency is the same as the CLK frequency. For DTR Read operations, the data should be latched on both rising edge and falling edge of the DQS signal.

If the DQS Function is not used, this pin must be floating.

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6 COMMANDS DESCRIPTION

Table 6-1. Commands Set

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte 7
Write Enable	06h						
Write Disable	04h						
Get Features	0Fh	A7-A0	D7-D0	Wrap(7)			
Set Feature	1Fh	A7-A0	D7-D0				
Page Read (to cache)	13h	A23-A16	A15-A8	A7-A0			
Read From Cache	03h/0Bh(8)	A15-A8	A7-A0(2)	Dummy(1)	D7-D0		
Read From Cache x 2	3Bh(8)	A15-A8	A7-A0(2)	Dummy(1)	D7-D0		
Read From Cache x 4	6Bh(8)	A15-A8	A7-A0(2)	Dummy(1)	D7-D0		
Read From Cache Dual IO	BBh	A15-A8	A7-A0(2)	Dummy(1)	D7-D0		
Read From Cache Quad IO	EBh	A15-A8	A7-A0(2)	Dummyx2(1)	D7-D0		
Read From Cache Quad I/O DTR	EEh	A31-A24	A23-A16	A15-A8	A7-A0(2)	Dummy x8(1)	D7-D0
Read ID(4)	9Fh	Dummy	MID	DID			
Read parameter page(9)	13h	00h	00h	01h			
Read UID(9)	13h	00h	00h	00h			
Program Load	02h	A15-A8	A7-A0(3)	D7-D0	Next byte		
Program Load x4	32h	A15-A8	A7-A0(3)	D7-D0	Next byte		
Program Execute	10h	A23-A16	A15-A8	A7-A0			
Program Load Random Data	84h	A15-A8	A7-A0(3)	D7-D0	Next byte		
Program Load Random Data x4	C4h/34h	A15-A8	A7-A0(3)	D7-D0	Next byte		
Block Erase(128K)	D8h	A23-A16	A15-A8	A7-A0			
Reset(5)	FFh						
Enable Power on Reset	66h						
Power on Reset(6)	99h						
Deep Power Down(1.8V only)	B9h						
Release Deep Power Down(1.8V only)	ABh						

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Note:

1. 03h/0Bh/3Bh/6Bh has 8 clock, 1 byte dummy.
   BBh has 4 clock, 1 byte dummy.
   EBh has 4 clock, 2 bytes dummy.
   EEh has 8 clock, 8 bytes dummy.
2. The A15-A0 (03h/0Bh/3Bh/6Bh) has 16 clock, include 4 clock dummy.
   The A15-A0 (BBh) has 8 clock, include 2 clock dummy.
   The A15-A0 (EBh) has 4 clock, include 1 clock dummy.
   The A31-A0 (EEh) has 4 clock, include 2.5 clock dummy.
3. The A15-A0 has 16 clock, include 4 clock dummy.
4. MID is Manufacture ID (C8h for GigaDevice), DID is Device ID.
5. Reset command:

• Reset will reset PAGE READ/PROGRAM/ERASE operation.
• Reset will reset status register bits P_FAIL/E_FAIL/WEL/OIP/ECCS/ECCSE.

6. Power on reset:
   Retrieve status register and data in cache to power on status.
7. The output would be updated by real-time, until CS# is driven high.
8. Read UID/parameter page are same as page read to cache.

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7 WRITE OPERATIONS

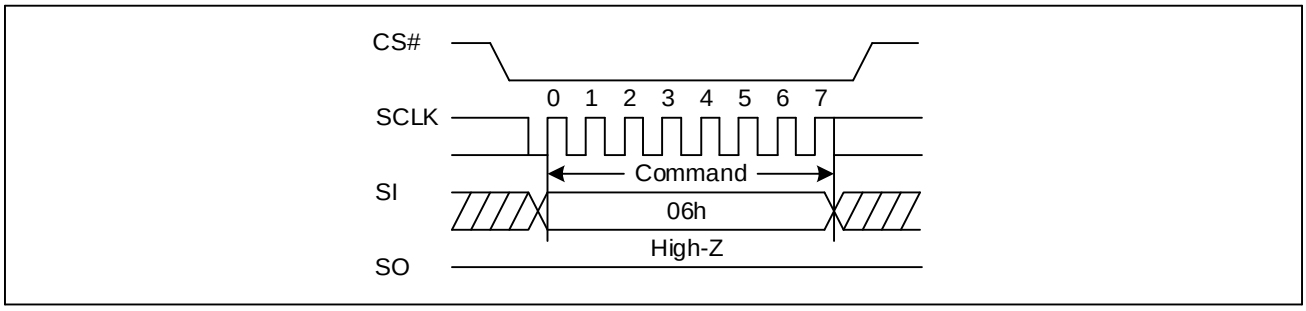
7.1 Write Enable (WREN) (06h)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to following operations that change the contents of the memory array:

- Page program
- OTP program/OTP protection
- Block erase

The WEL bit can be cleared after a reset command.

Figure 7-1. Write Enable Sequence Diagram

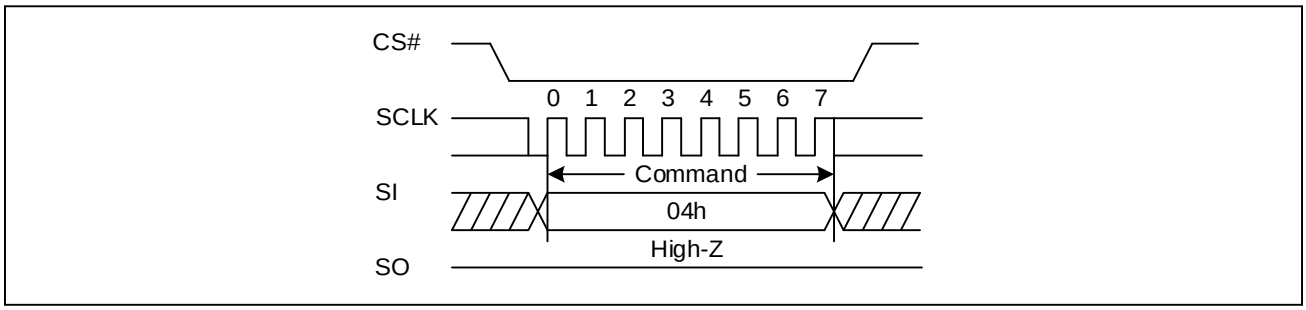


7.2 Write Disable (WRDI) (04h)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The WEL bit is reset by following condition:

- Page program
- OTP program/OTP protection
- Block erase

Figure 7-2. Write Disable Sequence Diagram



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8 READ OPERATIONS

8.1 Page Read

The PAGE READ (13h) command transfers the data from the NAND Flash array to the cache register. The command sequence is as follows:

- 13h (PAGE READ to cache)
- 0Fh (GET FEATURES command to read the status)
- 03h or 0Bh (Read from cache)/3Bh (Read from cache x2)/6Bh (Read from cache x4)/BBh (Read from cache dual IO)/EBh (Read from cache Quad IO)/EEh (Read from cache Quad IO DTR)

The PAGE READ command requires a 24-bit address. After the block/page addresses are registered, the device starts the transfer from the main array to the cache register, and is busy for tRD time. During this time, the GET FEATURE (0Fh) command can be issued to monitor the status. Followed the page read operation, the RANDOM DATA READ (03h/0Bh/3Bh/6Bh/BBh/EBh/EEh) command must be issued in order to read out the data from cache. The output data starts at the initial address specified in the command, once it reaches the ending boundary of whole page section, the output will wrap around from the beginning boundary until CS# is pulled high to terminate this operation. Refer waveforms to view the entire READ operation.

Note:(1) The command 6Bh (Read from cache x4)/EBh (Read from cache Quad IO)/EEh (Read from cache Quad IO DTR) is only available with the QE enable.

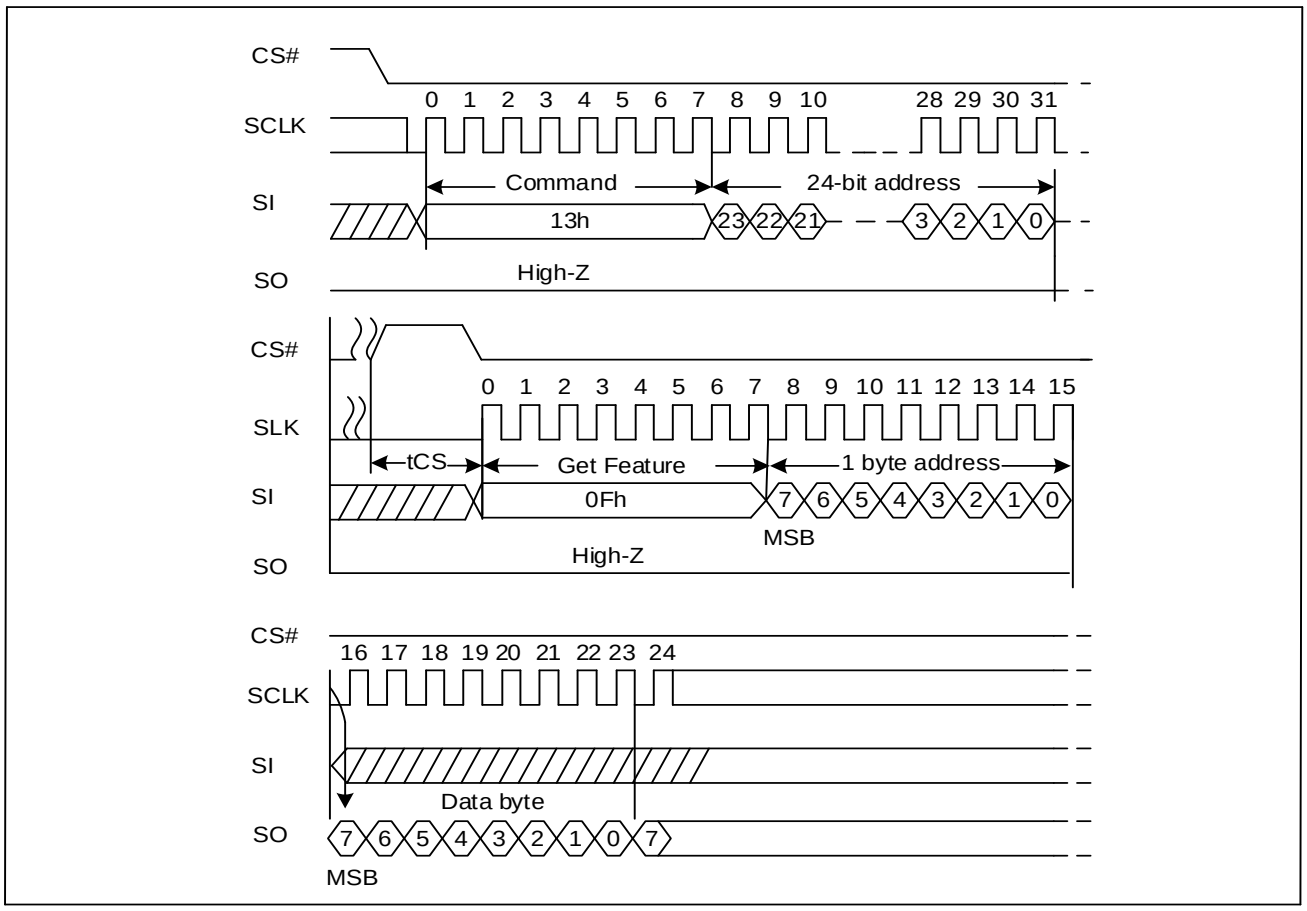
(2) When user read to the end of 64-Byte spare area, it won't wrap around from the beginning boundary and an additional 64Byte ECC code will be read. (Internal ECC enabled)

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8.2 Page Read to Cache (13h)

The command page read to cache is read the data from flash array to cache register.

Figure 8-1. Page Read to cache Sequence Diagram

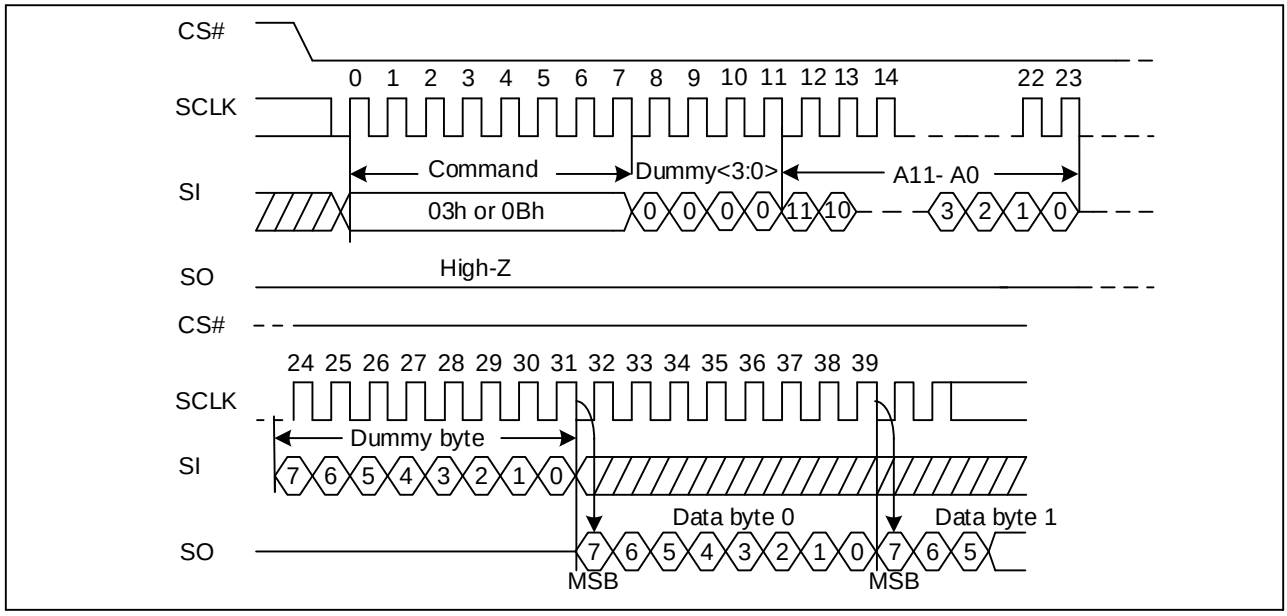


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8.3 Read From Cache (03h or 0Bh)

The command sequence is shown below.

Figure 8-2. Read From Cache Sequence Diagram

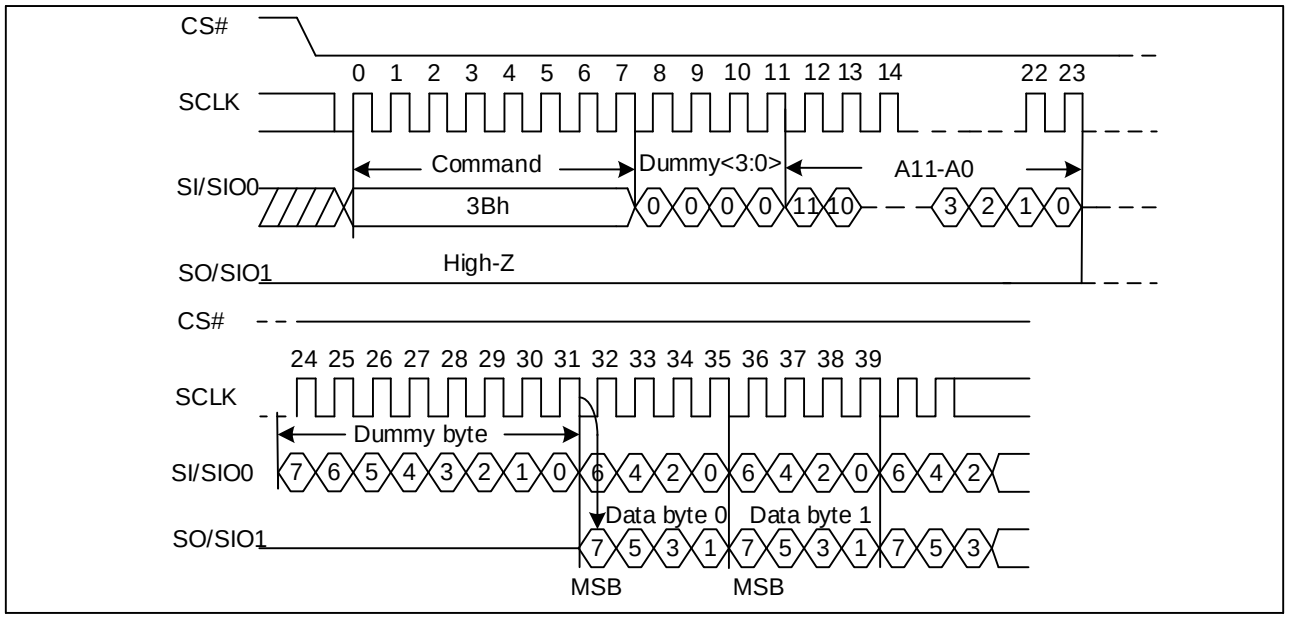


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8.4 Read From Cache x2 (3Bh)

The command sequence is shown below.

Figure 8-3. Read From Cache x2 Sequence Diagram

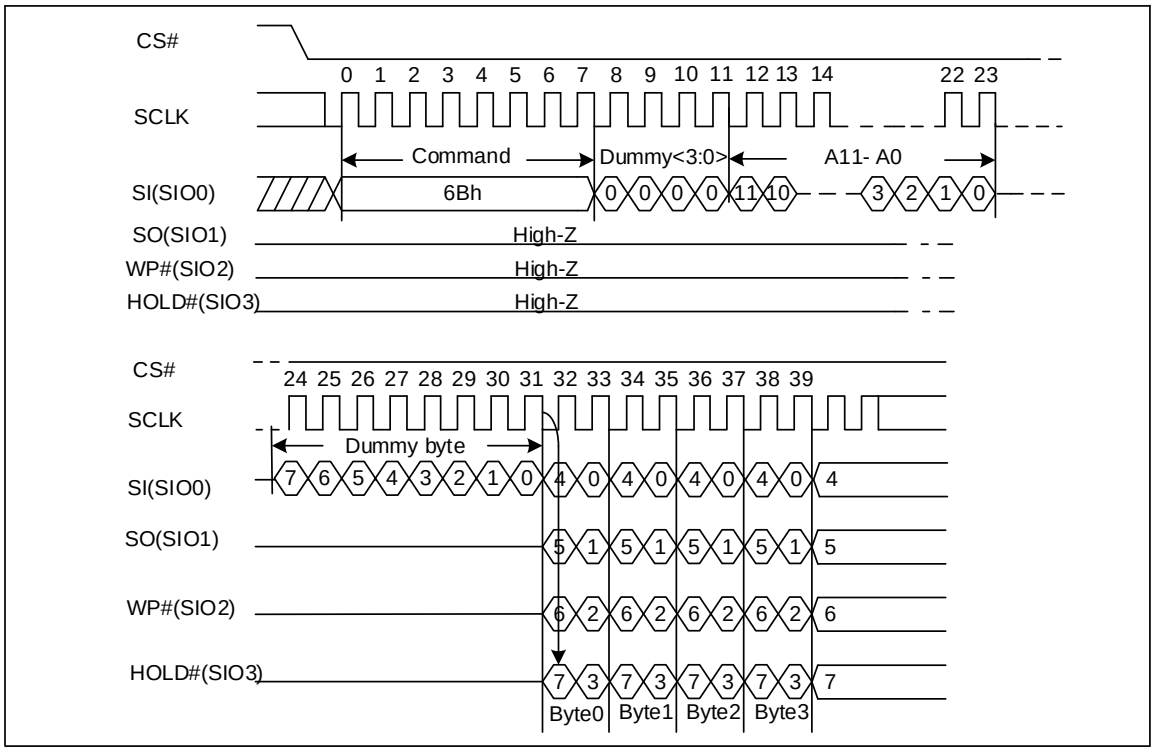


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8.5 Read From Cache x4 (6Bh)

The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the read from cache x4 command. The command sequence is shown below.

Figure 8-4. Read From Cache x4 Sequence Diagram

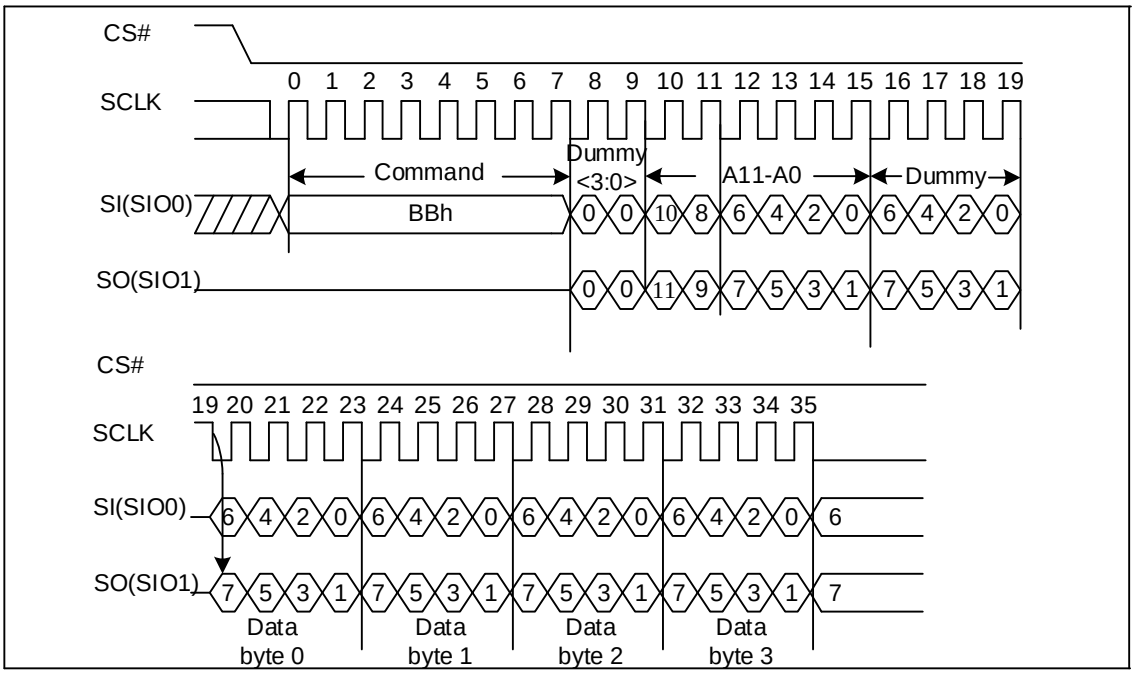


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8.6 Read From Cache Dual IO (BBh)

The Read from Cache Dual I/O command (BBh) is similar to the Read form Cache x2 command (3Bh) but with the capability to input the 4 Dummy bits, followed by a 12-bit column address for the starting byte address and 4 clock dummy by SIO0 and SIO1, each bit being latched in during the rising edge of SCLK, then the cache contents are shifted out 2-bit per clock cycle from SIO0 and SIO1. The first address byte can be at any location. The address increments automatically to the next higher address after each byte of data shifted out until the boundary wrap bit.

Figure 8-5. Read From Cache Dual IO Sequence Diagram

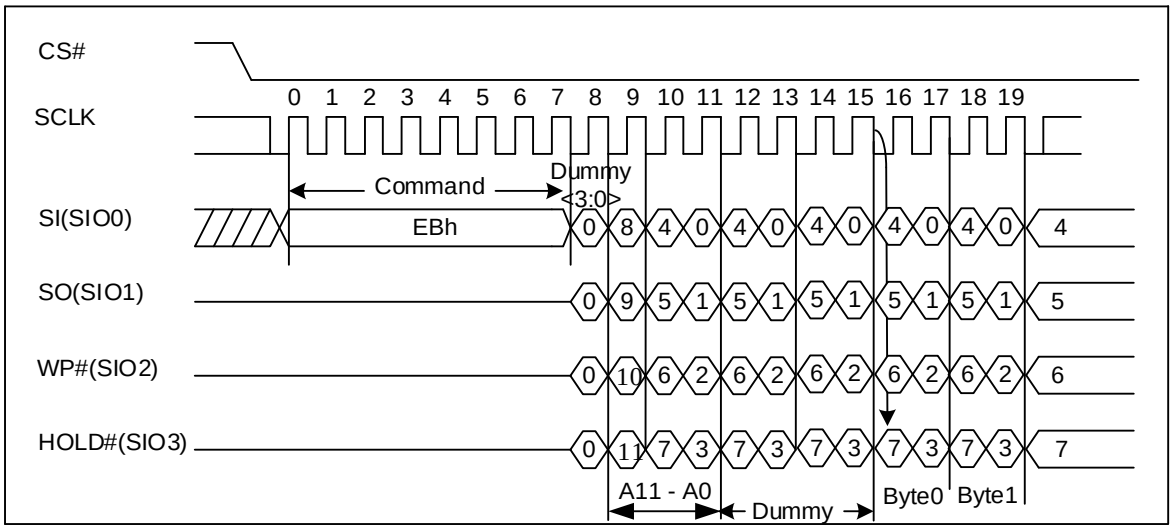


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8.7 Read From Cache Quad IO (EBh)

The Read from Cache Quad IO command is similar to the Read from Cache x4 command but with the capability to input the 4 dummy bits, followed a 12-bit column address for the starting byte address and a dummy byte by SIO0, SIO1, SIO3, SIO4, each bit being latched in during the rising edge of SCLK, then the cache contents are shifted out 4-bit per clock cycle from SIO0, SIO1, SIO2, SIO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out until the boundary wrap bit. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the read from cache quad IO command.

Figure 8-6. Read From Cache Quad IO Sequence Diagram



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8.8 Read From Cache Quad I/O DTR (EEh)

The DTR Quad IO command enables Double Transfer Rate throughput on quad I/O of Serial Flash in read mode. A Quad Enable (QE) bit of status Register must be set to “1” before sending the DTR Quad IO command. The address (interleave on 4 I/O pins) is latched on both rising and falling edge of SCLK, and data (interleave on 4 I/O pins) shift out on both rising and falling edge of SCLK. The 8-bit address can be latched-in at one clock, and 8-bit data can be read out at one clock, which means four bits at rising edge of clock, the other four bits at falling edge of clock.

The first address Byte can be at any location. The address is automatically increased to the next higher address after each Byte data is shifted out, so the whole page can be read out at a single DTR Quad IO command. The address counter rolls over to 0 when the highest address has been reached.

Figure 8-7.a Read From Cache Quad I/O DTR Sequence Diagram

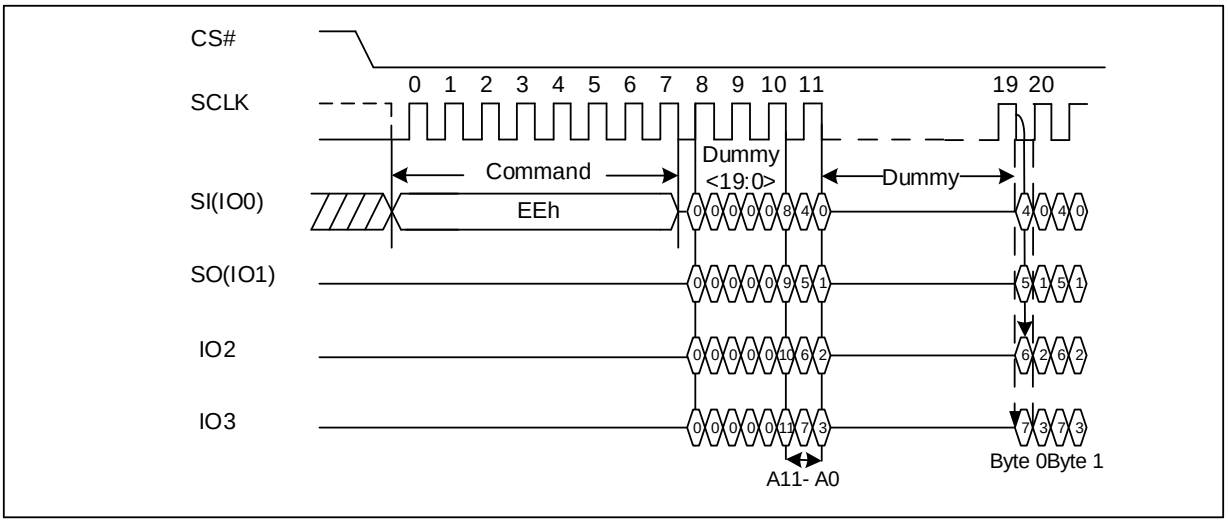
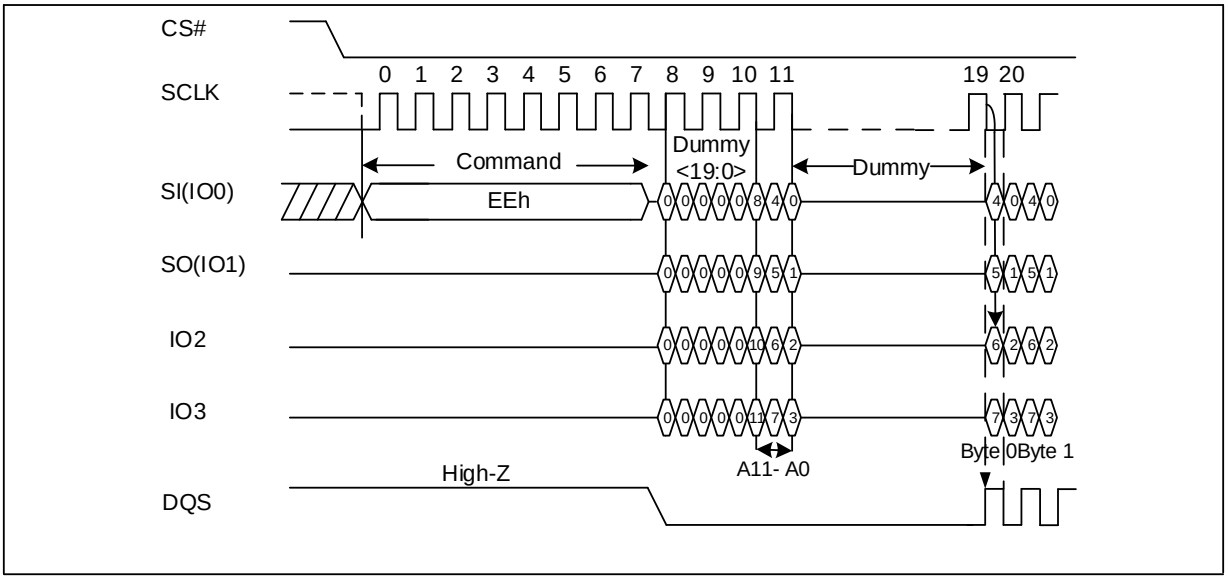


Figure 8-7.b Read From Cache Quad I/O DTR with DQS Sequence Diagram



Note:

Please contact GigaDevice when there is a need to use the EEh command for DTR.

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8.9 Read ID (9Fh)

The READ ID command is used to identify the NAND Flash device.

• The READ ID command outputs the Manufacturer ID and the device ID. See Table 8-1 for details.

Figure 8-8. Read ID Sequence Diagram

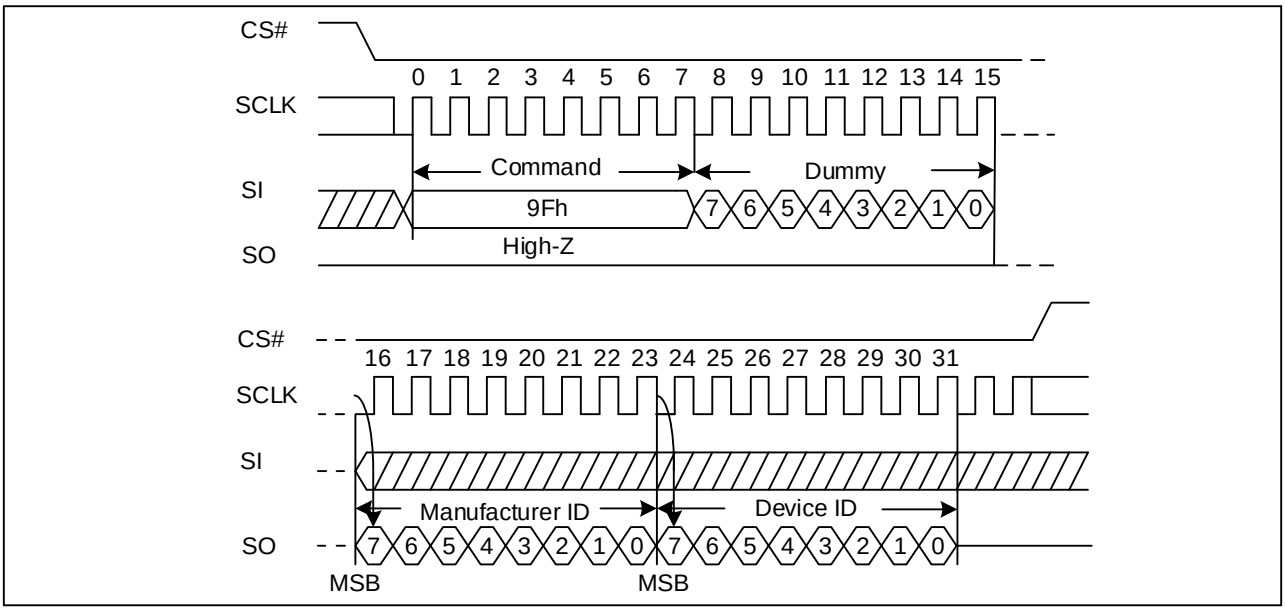


Table 8-1. READ ID Table

Part No	MID	DID1
GD5F2GM7UExxG	C8h	92h
GD5F2GM7RExxG	C8h	82h

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8.10 Read UID

The Read Unique ID function is used to retrieve the 16 bytes unique ID (UID) for the device. The unique ID when combined with the device manufacturer shall be unique.

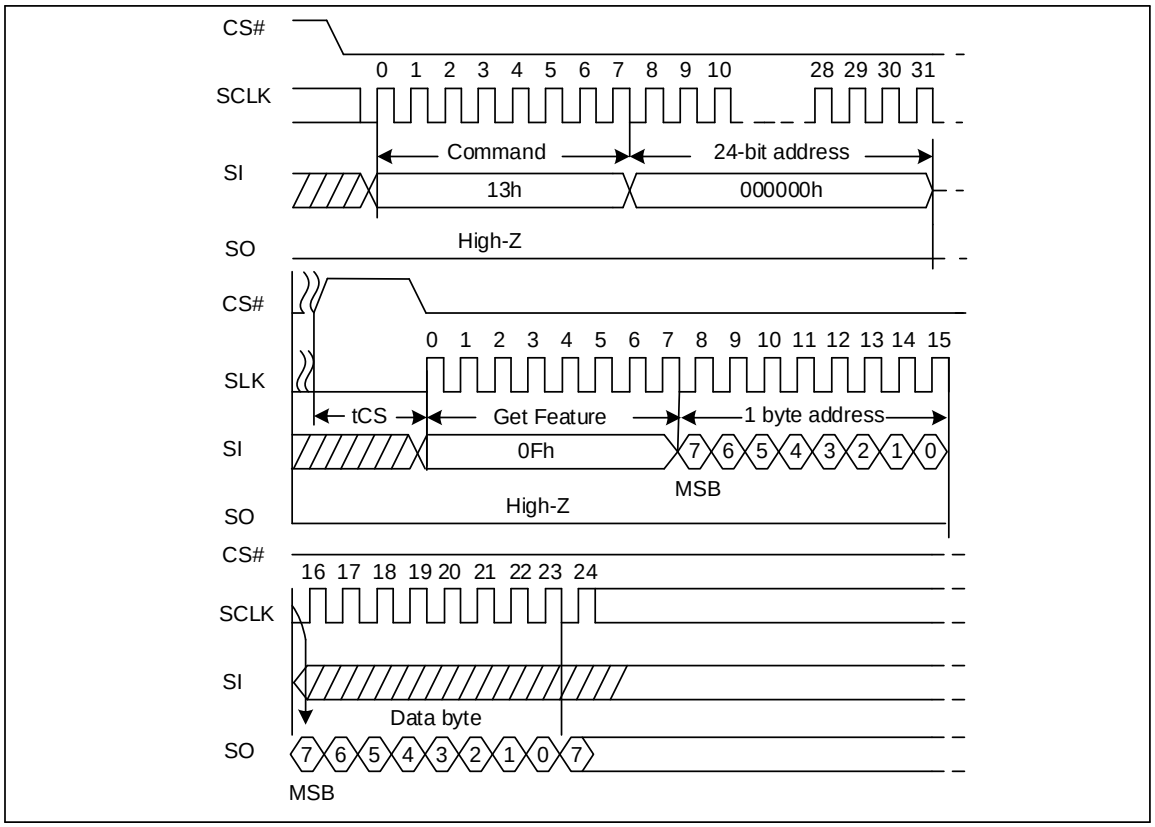
The UID data may be stored within the Flash array. To allow the host to determine if the UID is without bit errors, the UID is returned with its complement. If the XOR of the UID and its bit-wise complement is all ones, then the UID is valid. To accommodate robust retrieval of the UID in the case of bit errors, sixteen copies of the UID and the corresponding complement are stored by the target. For example, reading bytes 32-63 returns to the host another copies of the UID and its complement.

Bytes	Value
0-15	UID
16-31	UID complement (bit-wise)

Sequence is as follows:

1. Use Set Feature command to set B0 register, to enable OTP_EN.
2. Use Get Feature command to get data from B0 register and check if the OTP_EN is enable.
3. Use page read to cache (13h) command with address 24'h000000h, read data from array to cache.
4. Use 0Fh (GET FEATURES command) read the status.
5. User can use Read from cache command (03h/0Bh), read 16 bytes UID from cache.

Figure 8-9. Read UID to cache and Get Feature Command Sequence Diagram



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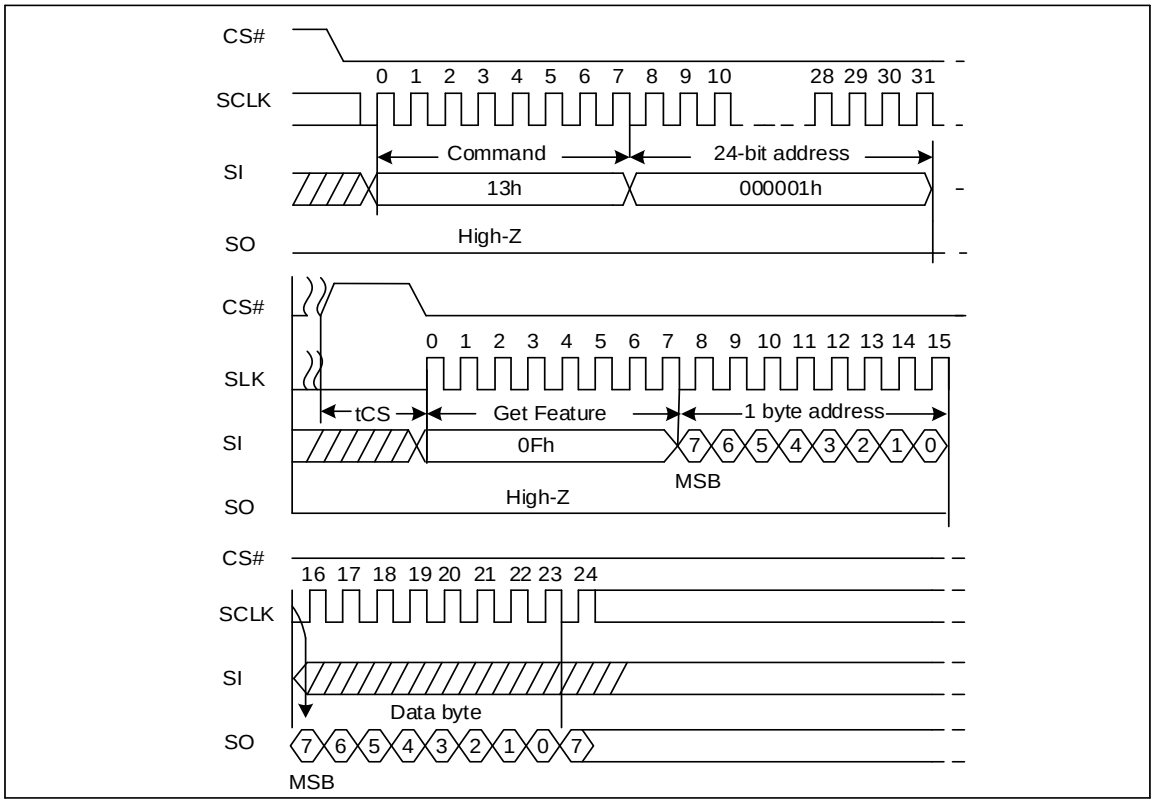
8.11 Read Parameter Page

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timing and other behavioral parameters. This data structure enables the host processor to automatically recognize the SPI-NAND Flash configuration of a device. The whole data structure is repeated at least three times. The Read from Cache command can be issued during execution of the read parameter page to read specific portion-soft the parameter page.

Sequence is as follows:

1. Use Set Feature command to set B0 register, to enable OTP_EN.
2. Use Get Feature command to get data from B0 register and check if the OTP_EN is enable.
3. Use Page Read to Cache (13h) command with address 24'h000001h. Load parameter page from array to cache.
4. Use 0Fh (GET FEATURES command) read the status
5. User can use Read from cache command (03h/0Bh), read parameter page from cache.

Figure 8-10. Read parameter page to cache and Get Feature Command Sequence Diagram



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Parameter page table as follow

<table>
<tr><th>Byte</th><th>O/M</th><th>Description</th><th>3.3V/1.8V</th></tr>
<tr><td>0-3</td><td>M</td><td>Parameter page signature
Byte 0: 4Fh, “O”
Byte 1: 4Eh, “N”
Byte 2: 46h, “F”
Byte 3: 49h, “I”</td><td>4Fh
4Eh
46h
49h</td></tr>
<tr><td>4-5</td><td>M</td><td>Revision number
0-15 Reserved (0)</td><td>00h
00h</td></tr>
<tr><td>6-7</td><td>M</td><td>Features supported
0-15 Reserved (0)</td><td>00h
00h</td></tr>
<tr><td>8-9</td><td>M</td><td>Reserved (0)</td><td>00h
00h</td></tr>
<tr><td>10-31</td><td></td><td>Reserved (0)</td><td>00h
…
00h</td></tr>
<tr><td></td><td></td><td>Manufacturer Information block</td><td></td></tr>
<tr><td>32-43</td><td>M</td><td>Device manufacturer (12 ASCII characters)“GIGADEVICE ”</td><td>47h
49h
47h
41h
44h
45h
56h
49h
43h
45h
20h
20h</td></tr>
<tr><td>44-63</td><td>M</td><td>Device model (20 ASCII characters)
<table>
<tr><th>Device Model</th><th>ORGANIZATION</th><th>VCC RANGE</th></tr>
<tr><td>“GD5F2GM7U”</td><td>X4</td><td>2.7v ~ 3.6v</td></tr>
<tr><td>“GD5F2GM7R”</td><td>X4</td><td>1.7v ~ 2.0v</td></tr>
</table></td><td>47h
44h
35h
46h
32h
47h
4Dh
37h
55h/52h
20h
20h
20h
20h
20h
20h</td></tr>
</table>

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			20h 20h 20h 20h 20h
64	M	JEDEC manufacturer ID“C8”	C8h
65-66	O	Date code	00h 00h
67-79		Reserved	00h 00h 00h
		Memory organization block	
80-83	M	Number of data bytes per page	00h 08h 00h 00h
84-85	M	Number of spare bytes per page	80h 00h
86-89	M	Number of data bytes per partial page	00h 02h 00h 00h
90-91	M	Number of spare bytes per partial page	20h 00h
92-95	M	Number of pages per block	40h 00h 00h 00h
96-99	M	Number of blocks per logical unit (LUN)	00h 08h 00h 00h
100	M	Number of logical units (LUNs)	01h
101	M	Reserved	00h
102	M	Number of bits per cell	01h
103-104	M	Bad blocks maximum	28h 00h
105-106	M	Block endurance	05h 04h
107	M	Guaranteed valid blocks at beginning of target	01h
108-109	M	Block endurance for guaranteed valid blocks	00h 00h

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110	M	Number of programs per page	04h
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints	00h
112	M	Number of bits ECC correctability	00h
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits	00h
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support	00h
115-127		Reserved	00h … 00h
		Electrical parameters block	
128	M	I/O capacitance	08h
129-130	M	IO clock support	00h 00h
131-132	O	Reserved (0)	00h 00h
133-134	M	tPROG Maximum page program time (us)	58h 02h
135-136	M	tBERS Maximum block erase time (us)	10h 27h
137-138	M	tR Maximum page read time (us)	78h 00h
139-140	M	Reserved	00h 00h
141-163		Reserved	00h
		Vendor block	
164-165	M	Vendor specific Revision number	00h
166-253		Vendor specific	00h
254-255	M	Integrity CRC	Set on test
		Redundant parameter pages	
256-511	M	Value of bytes 0-255	
512-767	M	Value of bytes 0-255	
768+	O	Additional redundant parameter pages	

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Notes:

1. “O” Stands for Optional, “M” for Mandatory
2. The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host. Please refer to ONFI 1.0 specifications for details. The CRC shall be calculated using the following 16-bit generator polynomial: $G(X) = X^{16} + X^{15} + X^2 + 1$， This polynomial in hex may be represented as 8005h.

3．The CRC value shall be initialized with a value of 4F4Eh before the calculation begins. There is no XOR applied to the final CRC value after it is calculated. There is no reversal of the data bytes or the CRC calculated value.

Device Model	ORGANIZATION	VCC RANGE	CRC value B254/B255
“GD5F2GM7UxxxG”	X4	2.7v ~ 3.6v	9Bh/55h
“GD5F2GM7RxxxG”	X4	1.7v ~ 2.0v	43h/98h

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9 PROGRAM OPERATIONS

9.1 Page Program

The PAGE PROGRAM operation sequence programs 1 byte to whole page bytes of data within a page. The page program sequence is as follows:

- 02h (PROGRAM LOAD)/32h (PROGRAM LOAD x4)
- 06h (WRITE ENABLE)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

Firstly, a PROGRAM LOAD (02h/32h) command is issued. PROGRAM LOAD consists of an 8-bit Op code, followed by 4 dummy bits and a 12-bit column address, then the data bytes to be programmed. The Program address should be in sequential order in a block. The data bytes are loaded into a cache register that is whole page long. If more than one page data are loaded, then those additional bytes are ignored by the cache register. The command sequence ends when CS# goes from LOW to HIGH. Figure 9-1 shows the PROGRAM LOAD operation. Secondly, prior to performing the PROGRAM EXECUTE operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE must be executed in order to set the WEL bit. If this command is not issued, then the rest of the program sequence is ignored.

Note:

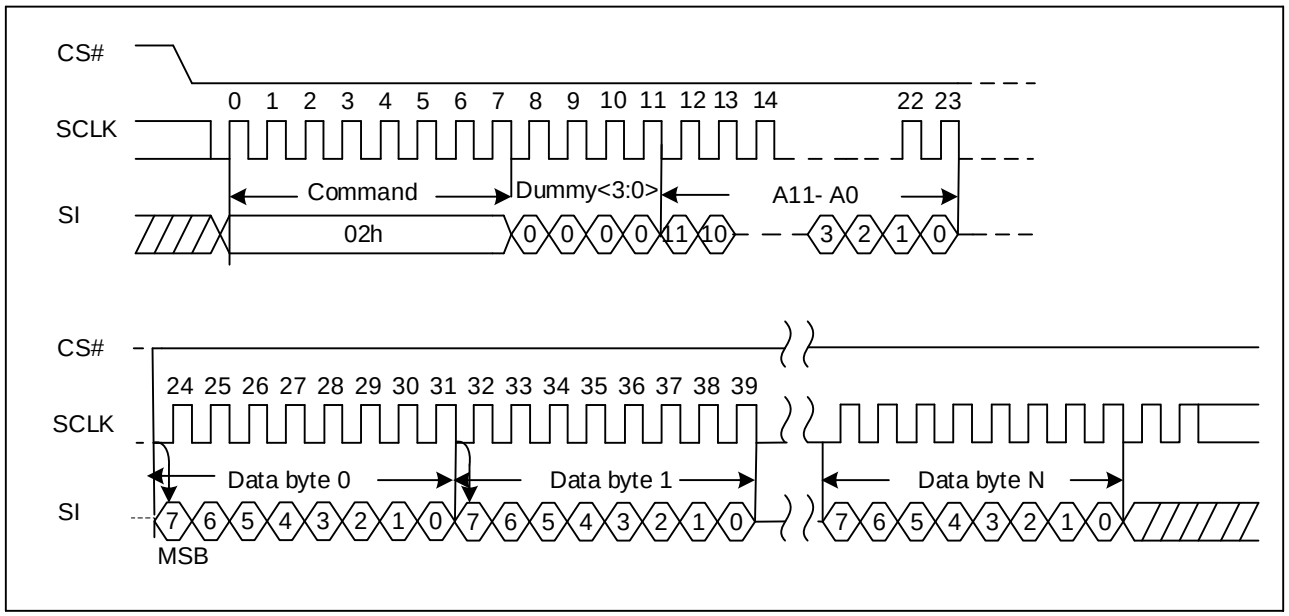
1. The contents of Cache Register don’t reset when Program Random Load (84h/C4h/34h) command and RESET (FFh) command.
2. When Program Execute (10h) command was issued just after Program Load (02h/32h) command, the 0xFF is output to the address that data was not loaded by Program Load (02h/32h) command.
3. When Program Execute (10h) command was issued just after Program Load Random Data (84h/C4h/34h) command, the contents of Cache Register are output to the NAND.
4. The Program address should be in sequential order in a block.
5. Program Load x4 is only available with the QE enable.

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9.2 Program Load (PL) (02h)

The command sequence is shown below.

Figure 9-1. Program Load Sequence Diagram



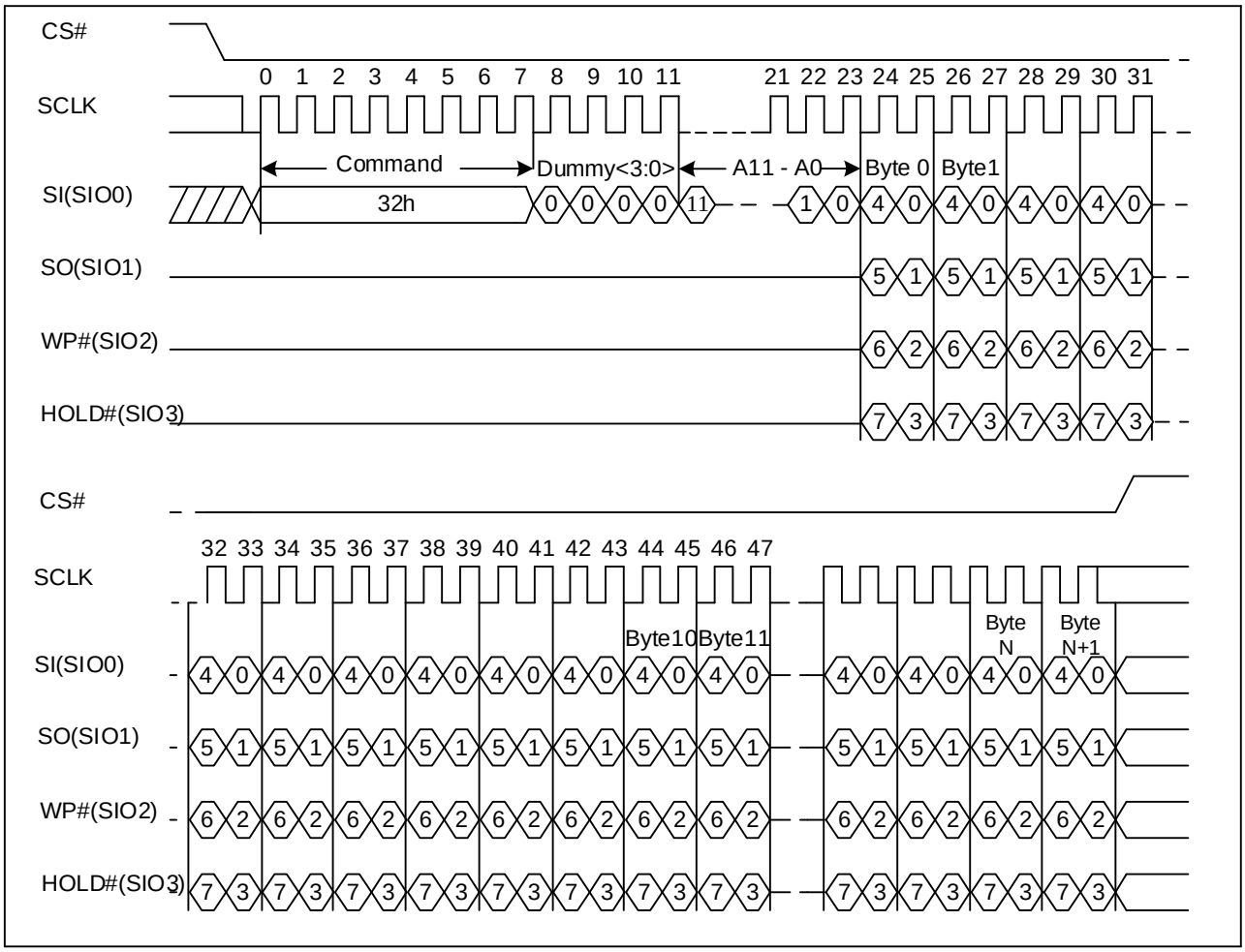
Note: When internal ECC disabled the Data Byte is 2176, when internal ECC enabled the Data Byte is 2112.

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9.3 Program Load x4 (PL x4) (32h)

The Program Load x4 command (32h) is similar to the Program Load command (02h) but with the capability to input the data bytes by four pins: SIO0, SIO1, SIO2, and SIO3. The command sequence is shown below. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the program load x4 command.

Figure 9-2. Program Load x4 Sequence Diagram



Note: When internal ECC disabled the Data Byte is 2176, when internal ECC enabled the Data Byte is 2112.

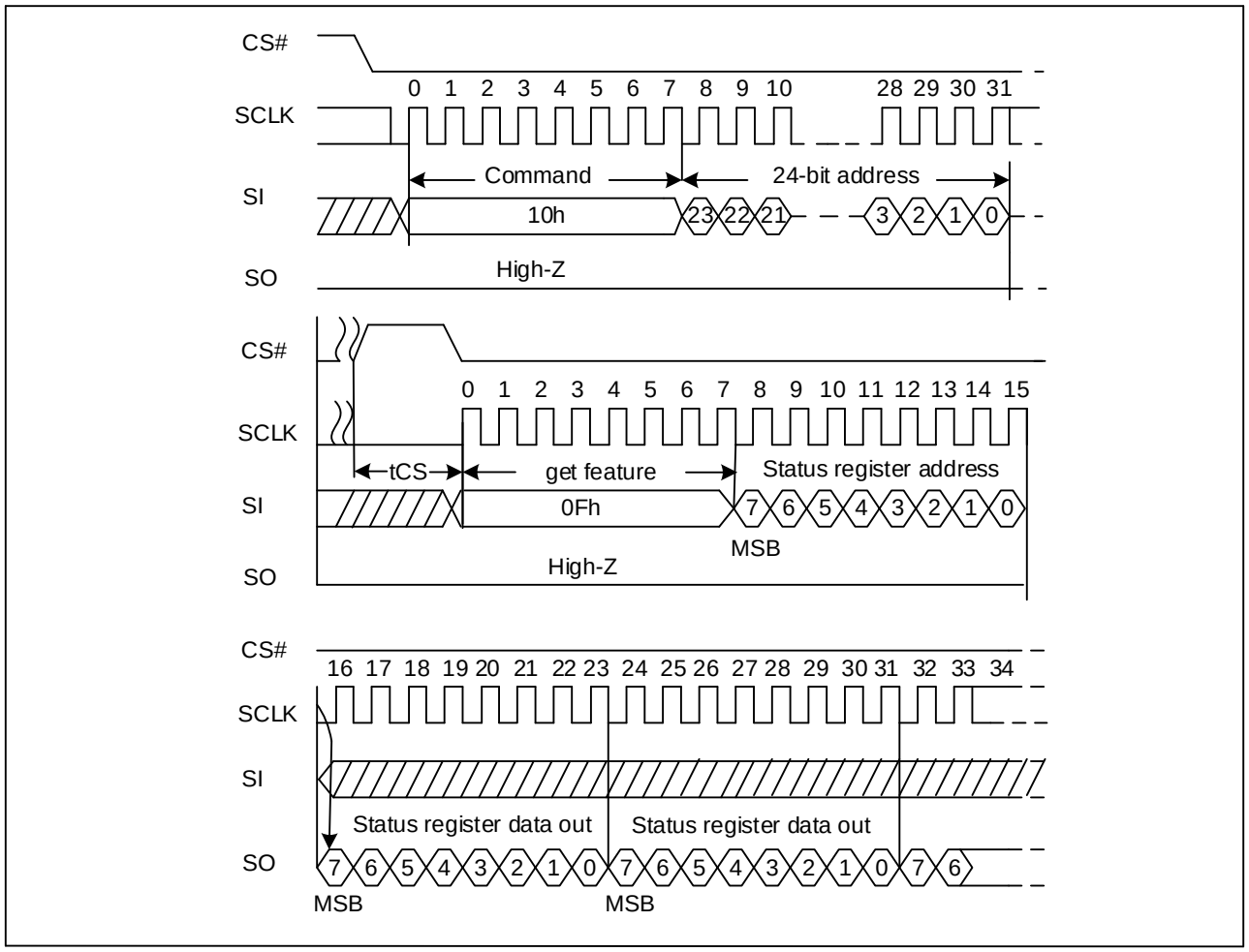
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9.4 Program Execute (PE) (10h)

After the data is loaded, a PROGRAM EXECUTE (10h) command must be issued to initiate the transfer of data from the cache register to the main array. PROGRAM EXECUTE consists of an 8-bit Op code, followed by a 24-bit address. After the page/block address is registered, the memory device starts the transfer from the cache register to the main array, and is busy for tPROG time. This operation shown in Figure 9-3. During this busy time, the status register can be polled to monitor the status of the operation (refer to Status Register). When the operation completes successfully, the next series of data can be loaded with the PROGRAM LOAD command. The command sequence is shown below.

Note: After the Program Execute (10h) command is issued, the data in cache register are no longer valid.

Figure 9-3. Program Execute Sequence Diagram



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9.5 Internal Data Move

The INTERNAL DATA MOVE command sequence programs or replaces data in a page with existing data. The INTERNAL DATA MOVE command sequence is as follows:

- 13h (PAGE READ to cache)
- Optional 84h/C4h/34h(PROGRAM LOAD RANDOM DATA)
- 06h (WRITE ENABLE)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

Prior to performing an internal data move operation, the target page content must be read out into the cache register by issuing a PAGE READ (13h) command. The PROGRAM LOAD RANDOM DATA (84h/C4h) command can be issued, if user wants to update bytes of data in the page. New data is loaded in the 12-bit column address. If the random data is not sequential, another PROGRAM LOAD RANDOM DATA (84h/C4h) command must be issued with the new column address. After the data is loaded, the WRITE ENABLE command must be issued, and then PROGRAMEXECUTE (10h) command can be issued to start the programming operation.

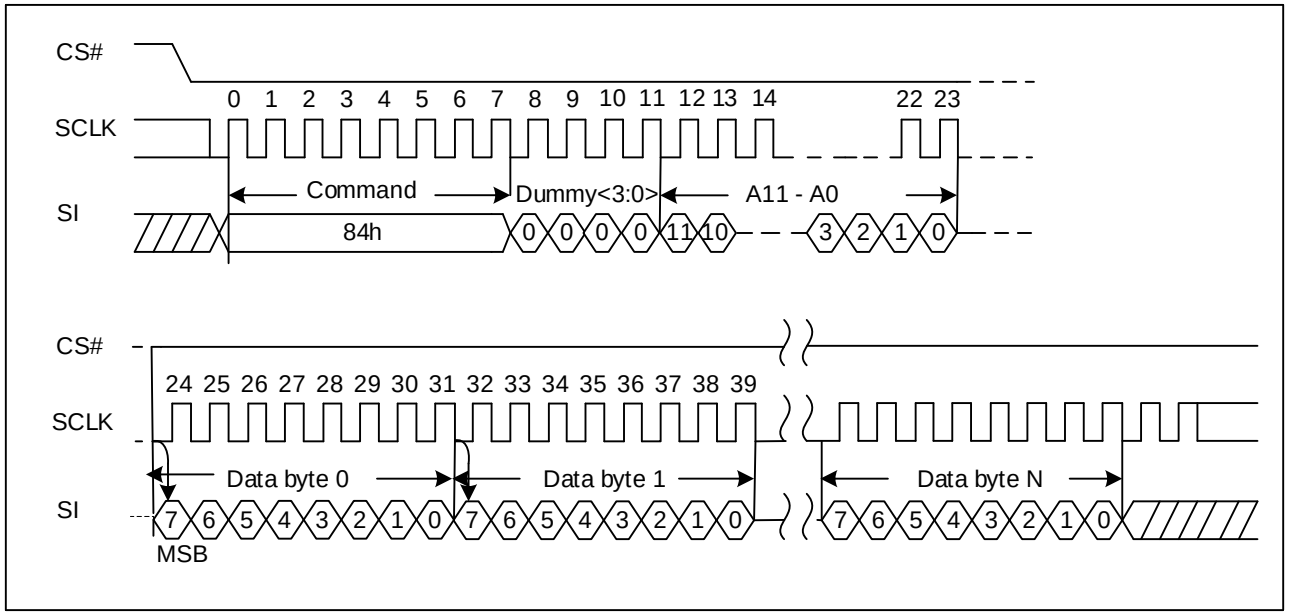
Note: Only the block with the same parity attribute can use the command. Internal Data Move command can’t move the data between two different parity blocks.

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9.6 Program Load Random Data (84h)

The Program Load Random Data command programs or replaces data in a page with existing data. This command consists of an 8-bit Op code, followed by 4 dummy bits, and a 12-bit column address. New data is loaded in the column address provided with the 12 bits. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA (84h) command must be issued with a new column address, see Figure 9-4 for details.

Figure 9-4. Program Load Random Data Sequence Diagram

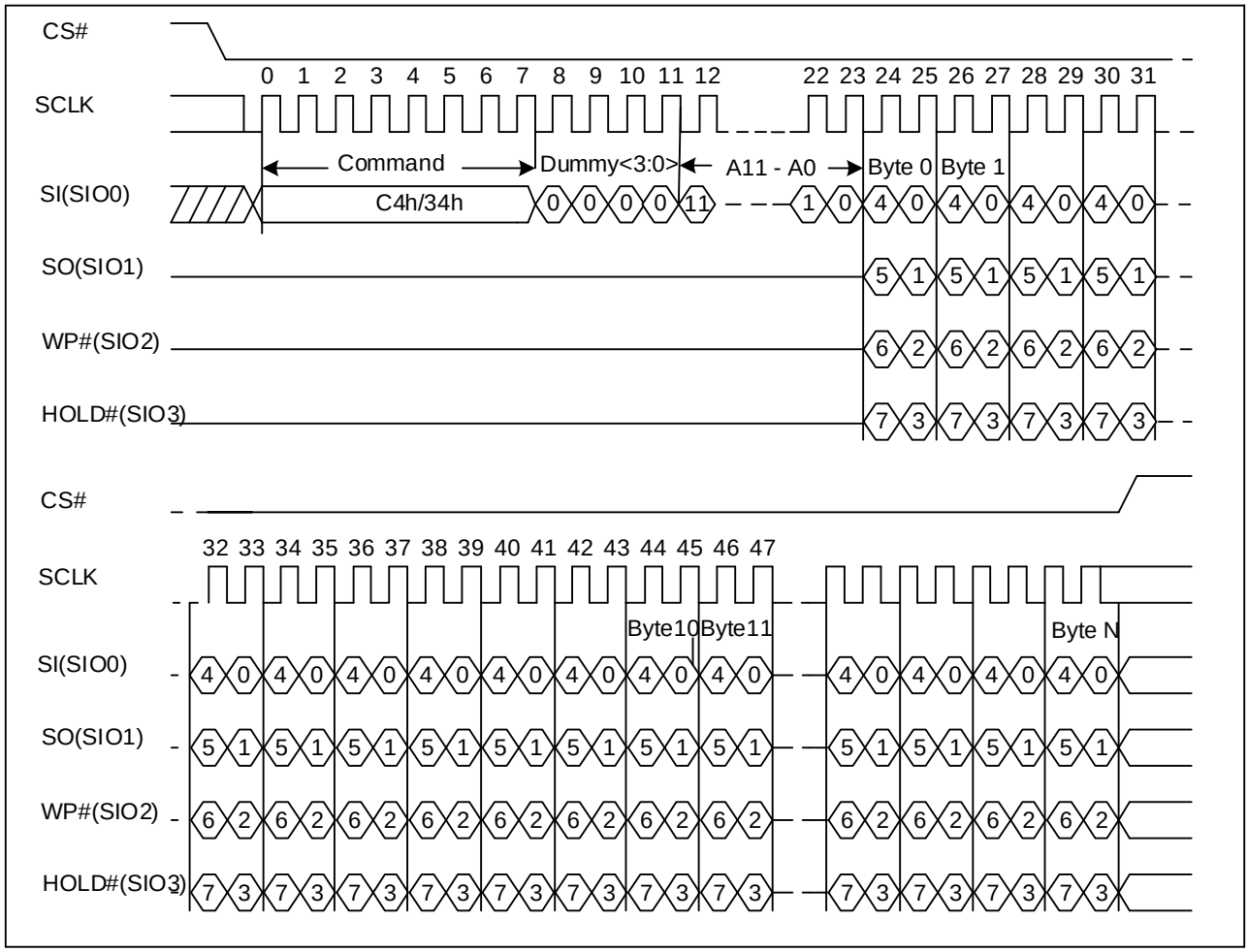


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9.7 Program Load Random Data x4 (C4h/34h)

The Program Load Random Data x4 command (C4h/34h) is similar to the Program Load Random Data command (84h) but with the capability to input the data bytes by four pins: SIO0, SIO1, SIO2, and SIO3. The command sequence is shown below. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable for the program load random data x4 command. See Figure 9-5 for details.

Figure 9-5. Program Load Random Data x4 Sequence Diagram



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10 ERASE OPERATIONS

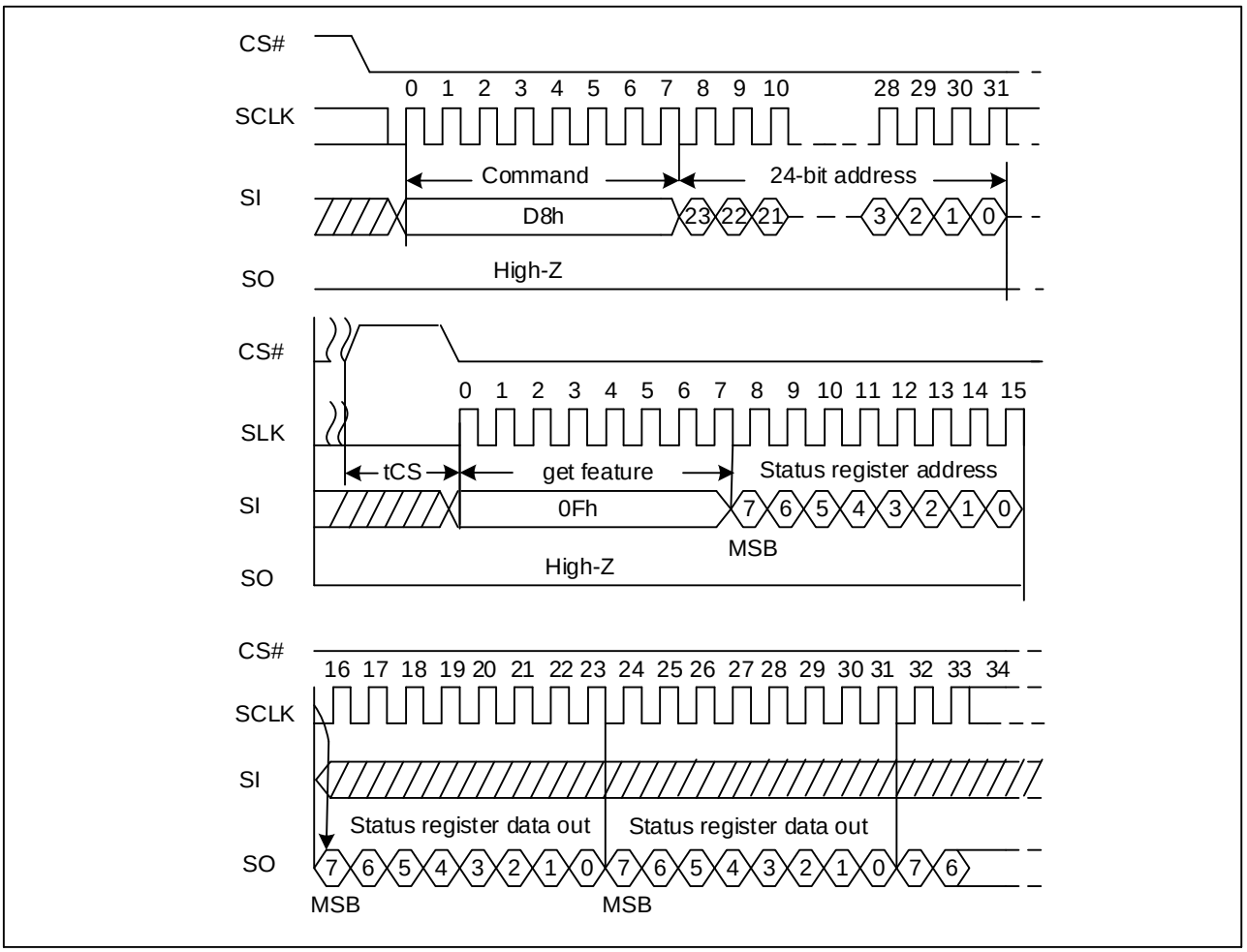
10.1 Block Erase (D8h)

The BLOCK ERASE (D8h) command is used to erase at the block level. The BLOCK ERASE command (D8h) operates on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:

- 06h (WRITE ENBALE command)
- D8h (BLOCK ERASE command)
- 0Fh (GET FEATURES command to read the status register)

Prior to performing the BLOCK ERASE operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed in order to set the WEL bit. If the WRITE ENABLE command is not issued, then the rest of the erase sequence is ignored. A WRITE ENABLE command must be followed by a BLOCK ERASE (D8h) command. This command requires a 24-bit address. After the row address is registered, the control logic automatically controls timing and erase-verify operations. The device is busy for tBERS time during the BLOCK ERASE operation. The GET FEATURES (0Fh) command can be used to monitor the status of the operation.

Figure 10-1. Block Erase Sequence Diagram



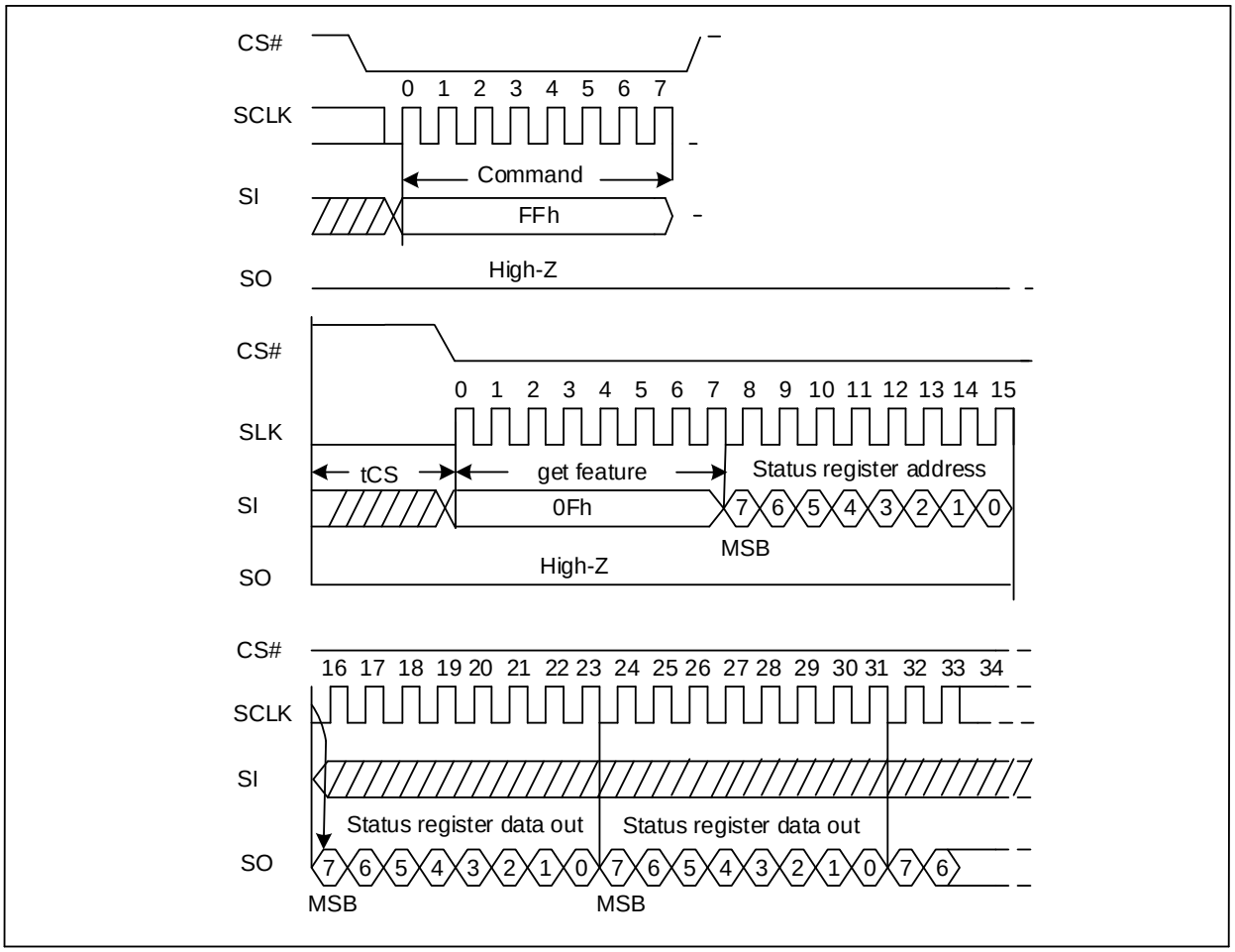
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11 RESET OPERATIONS

11.1 Soft Reset (FFh)

The RESET (FFh) command stops all operations and the status. For example, in case of a program or erase or read operation, the reset command can make the device enter the idle state.

Figure 11-1. Reset Sequence Diagram



Note: The Register bit value after soft reset refers to Table 12-2. Register bit Descriptions.

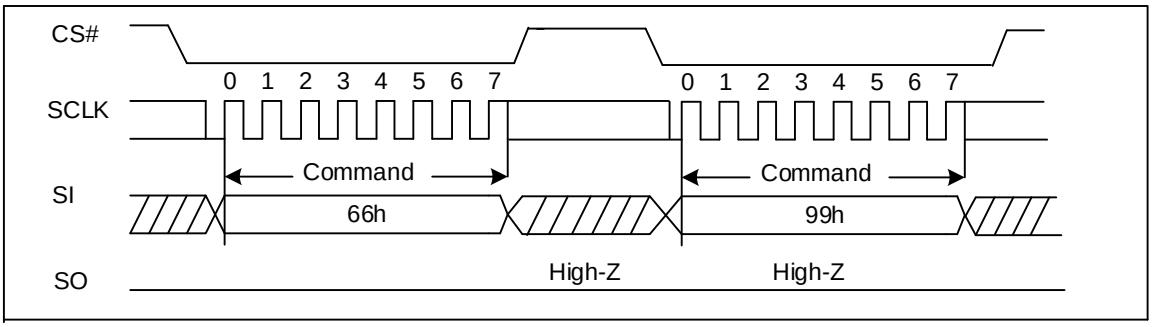
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11.2 Enable Power on Reset (66h) and Power on Reset (99h)

If the Power on Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current feature settings.

The “Enable Reset (66h)” and the “Reset (99h)” commands can be issued in SPI mode. The “Reset (99h)” command sequence as follow: CS# goes low -> Sending Enable Reset command ->CS# goes high ->CS# goes low.->Sending Reset command ->CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tVSL to reset. During this period, no command will be accepted. It is recommended to check the OIP bit in Status Register before issuing any other command sequence. The contents of the memory location being programmed or the block being erased are no longer valid.

Figure 11-2. Reset Sequence Diagram



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12 FEATURE OPERATIONS

12.1 Get Features (0Fh) and Set Features (1Fh)

The GET FEATURES (0Fh) and SET FEATURES (1Fh) commands are used to monitor the device status and alter the device behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Feature such as OTP can be enabled or disabled by setting specific feature bits (shown in the below table). The status register is mostly read, except WEL, which is a writable bit with the WRITE ENABLE (06h) command.

When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified in the following table, once the device is set, it remains set, even if a RESET (FFh) command is issued.

Table 12-1. Features Settings

Register	Addr.	7	6	5	4	3	2	1	0
Protection	A0h	BRWD	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
Feature	B0h	OTP_PRT	OTP_EN	Reserved	ECC_EN	BPL	Reserved	Reserved	QE
Status	C0h	Reserved	Reserved	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP
Feature	D0h	Reserved	DS_S1	DS_S0	Reserved	Reserved	Reserved	Reserved	Reserved
Status	F0h	Reserved	Reserved	ECCSE1	ECCSE0	BPS	Reserved	Reserved	Reserved

Note: 1. If BRWD is enabled and WP# is LOW, then the block lock register cannot be changed.
2. If QE is enabled, the quad IO operations can be executed.
3. All the reserved bits must be held low when the feature is set.
4. These registers A0h/B0h/D0h are write/read type, and Registers C0h/F0h are read only.
5. The OTP_PRT is non-volatile, others bits are volatile.
6. The Register Bit default value after power-up refers to Table 12-2. Register Bit Descriptions.

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Table 12-2. Status Register Bit Descriptions

Bit	Bit Name	After Power up or Power on Reset(66h-99h)	After Reset command (FFh)	Description
BRWD	Block register write disable	0	No Change	Which is used combined with WP#, If BRWD is high enabled and WP# is LOW, then the Protection register cannot be changed
BP2 BP1 BP0 INV CMP	Block Protection bits	1 1 1 0 0	No Change	used combination, refer to chapter Block Protection
OTP_PRT OTP_EN	OTP Region bits	0 0 Before OTP Set	No Change	used combination, refer to chapter OTP Region
ECC_EN	ECC Enable Latch	1	No Change	The device offers data corruption protection by offering optional internal ECC. READs and PROGRAMs with internal ECC can be enabled or disabled by setting feature bit ECC_EN. ECC is enabled by default when device powered on, so the default READ and PROGRAM commands operate with internal ECC in the “active” state when ECC enable.
BPL	Block Protection Lock register	0	No Change	BPL is for Power Lock Down Protection. Once the BPL bit sets as 1, the rest of the protection bits BP[0,2] , INV , CMP , BRWD can’t be changed until next power cycle. By default BPL is 0 after power-on-reset and this bit default is Power Lock Down Protection disable.
QE	The Quad Enable bit	0	No Change	This bit indicates that whether the quad IO operations can be executed. If QE is set to 1, the quad IO operations can be executed.
ECCS1 ECCS0 ECCSE1 ECCSE0	ECC Status	Page 0 Status	0 0 0 0	ECCS provides ECC status as the following table. ECCS and ECCSE are set to 00b either following a RESET, or at the beginning of the READ. They are then updated after the device completes a valid READ operation. ECCS and ECCSE are invalid if internal ECC is disabled (via a SET FEATURES command to reset ECC_EN to 0). After power-on RESET, ECC status is set to reflect the contents of block 0, page 0.

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P_FAIL	Program Fail	0	0	This bit indicates that a program failure has occurred (P_FAIL set to 1). It will also be set if the user attempts to program a protected region, including the OTP area. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command (P_FAIL = 0).
E_FAIL	Erase Fail	0	0	This bit indicates that an erase failure has occurred (E_FAIL set to 1). It will also be set if the user attempts to erase a locked region. This bit is cleared (E_FAIL = 0) at the start of the BLOCK ERASE command sequence or the RESET command.
WEL	Write Enable Latch	0	0	This bit indicates the current status of the write enable latch (WEL) and must be set (WEL = 1), prior to issuing a PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing the WRITE ENABLE command. WEL can also be disabled (WEL = 0), by issuing the WRITE DISABLE command.
OIP	Operation In Progress	0	0	This bit is set (OIP = 1) when a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, or RESET command is executing, indicating the device is busy. When the bit is 0, the interface is in the ready state.
DS_IO[1] DS_IO[0]	Driven Strength register	0 0	No Change	IO driver strength setting. Default is 00b.
BPS	Block Protection Status	1	No Change	Block protection status BPS is 1, selected block is protected BPS is 0, selected block is unprotected.

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Figure 12-1. Get Features Sequence Diagram

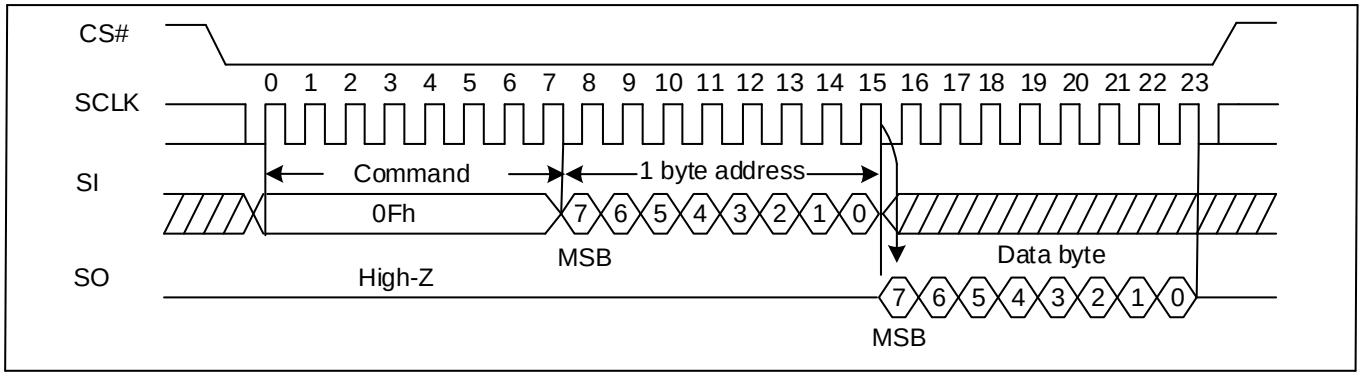
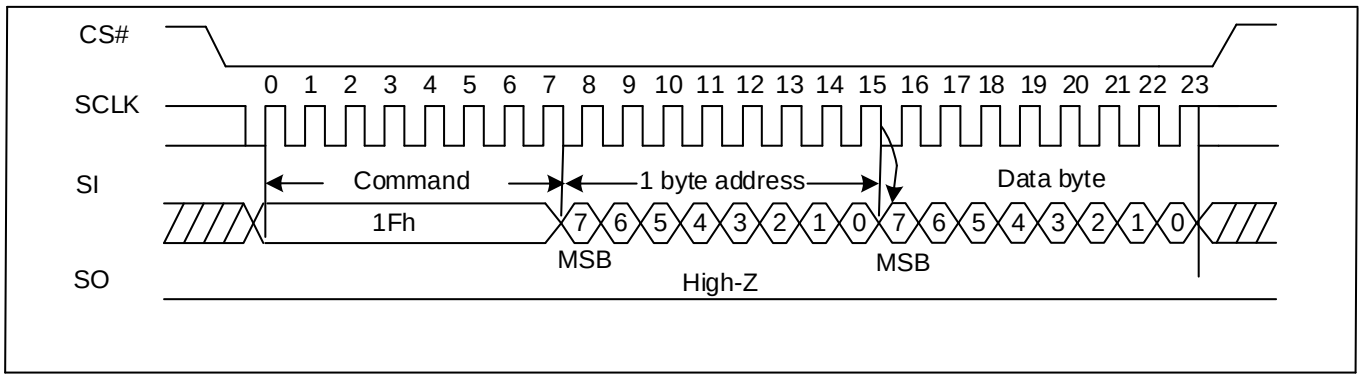


Figure 12-2. Set Features Sequence Diagram



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12.2 Status Register and Driver Register

The NAND Flash device has the status registers (C0h/F0h) that software can read during the device operation for operation state query. The status register can be read by issuing the GET FEATURES (0Fh) command, followed by the feature address C0h or F0h(see FEATURE OPERATION). The Output Driver Register can be set and read by issuing the SET FEATURE (0Fh) and GET FEATURE command followed by the feature address D0h (see FEATURE OPERATION).

Table 12-3. ECC Error Bits Descriptions

ECCS1	ECCS0	ECCSE1	ECCSE0	Description
0	0	x	x	No bit errors were detected during the previous read algorithm
0	1	0	0	Bit errors(≤4) were detected and corrected
0	1	0	1	Bit errors (=5) were detected and corrected.
0	1	1	0	Bit errors (=6) were detected and corrected.
0	1	1	1	Bit errors (=7) were detected and corrected.
1	1	x	x	Bit errors (=8) were detected and corrected.
1	0	x	x	Bit errors greater than ECC capability(8 bits) and not corrected

Table 12-4. Driver Register Bits Descriptions by Design Trim

DS_IO[1]	DS_IO[0]	Driver Strength
0	0	100%(Default)
0	1	75%
1	0	50%
1	1	25%

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12.3 OTP Region

The serial device offers a protected, One-Time Programmable NAND Flash memory area. 10 full pages are available on the device. Customers can use the OTP area any way they want, like programming serial numbers, or other data, for permanent storage. When delivered from factory, feature bit OTP_PRT is 0. To access the OTP feature, the user must set feature bits OTP_EN/OTP_PRT by SET FEATURES command. When the OTP is ready for access, pages 02h–0Bh can be programmed in sequential order by PROGRAM LOAD (02h) and PROGRAM EXECUTE (10h) commands (when not yet protected), and read out by PAGE READ (13h) command and output data by READ from CACHE (03h/0Bh/3Bh/6Bh/BBh/EBh).

When ECC is enabled, data written in the OTP area is ECC protected.

Table 12-5. OTP States

OTP_PRT	OTP_EN	State
x	0	Normal Operation
0	1	Access OTP region, read and program data
1	1	1. When the device power on state OTP_PRT is 0, user can set feature bit OTP_PRT and OTP_EN to 1, then issue PROGRAM EXECUTE (10h) to lock OTP, and after that OTP_PRT will permanently remain 1. 2. When the device power on state OTP_PRT is 1, user can only read the OTP region data

Note: The OTP space cannot be erased and after it has been protected, it cannot be programmed again, please use this function carefully.

Access to OTP data

- Issue the SET FEATURES command (1Fh)
- Set feature bit OTP_EN
- Issue the PAGE PROGRAM (only when OTP_PRT is 0) or PAGE READ command

Protect OTP region

Only when the following steps are completed, the OTP_PRT will be set and users can get this feature out with 0Fh command.

- Issue the SET FEATURES command (1Fh)
- Set feature bit OTP_EN and OTP_PRT
- 06h (WRITE ENABLE)
- Issue the PROGRAM EXECUTE (10h) command.

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12.4 Assistant Bad Block Management

As a NAND Flash, the device may have blocks that are invalid when shipped from the factory, and a minimum number of valid blocks (NVB) of the total available blocks are specified. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms, which ensure data integrity. Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by programming the Bad Block Mark (00h) to the first spare area location in each bad block. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the bad-block mark.

System software should initially check the first spare area location for non-FFh data on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

To simplify the system requirement and guard the data integration, GigaDevice SPI NAND provides assistant Management options as below.

Table 12-6. Bad Block Mark information (2Gb)

Description	Requirement
Minimum number of valid blocks (NVB)	2008
Total available blocks per die	2048
First spare area location	Byte 2048
Bad-block mark	00h(use non FFh to check)

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12.5 Block Protection

The block lock feature provides the ability to protect the entire device, or ranges of blocks, from the PROGRAM and ERASE operations. After power-up, the device is in the “locked” state, i.e., feature bits BP0, BP1and BP2 are set to 1, INV, CMP and BRWD are set to 0. To unlock all the blocks, or a range of blocks, the SET FEATURES command must be issued to alter the state of protection feature bits. When BRWD is set and WP# is LOW, none of the writable protection feature bits can be set. Also, when a PROGRAM/ERASE command is issued to a locked block, status bit OIP remains 0. When an ERASE command is issued to a locked block, the erase failure, status bit E_FAIL set to 1. When a PROGRAM command is issued to a locked block, program failure, status bit P_FAIL set to 1.

To enable the Write Protection (WP#), the Quad Enable bit (QE) of feature (B0[0]) must be set to 0.

Table 12-7. Block Lock Register Block Protect Bits (2Gb)

CMP	INV	BP2	BP1	BP0	Protect Row Address	Protect Rows
					2G	
x	x	0	0	0	NONE	None—all unlocked
0	0	0	0	1	1F800h ~ 1FFFFh	Upper 1/64 locked
0	0	0	1	0	1F000h ~ 1FFFFh	Upper 1/32 locked
0	0	0	1	1	1E000h ~ 1FFFFh	Upper 1/16 locked
0	0	1	0	0	1C000h ~ 1FFFFh	Upper 1/8 locked
0	0	1	0	1	18000h ~ 1FFFFh	Upper 1/4 locked
0	0	1	1	0	10000h ~ 1FFFFh	Upper 1/2 locked
x	x	1	1	1	0000h ~ 1FFFFh	All locked (default)
0	1	0	0	1	0000h ~7FFh	Lower 1/64 locked
0	1	0	1	0	0000h ~FFFh	Lower 1/32 locked
0	1	0	1	1	0000h ~ 1FFFh	Lower 1/16 locked
0	1	1	0	0	0000h ~ 3FFFh	Lower 1/8 locked
0	1	1	0	1	0000h ~ 7FFFh	Lower 1/4 locked
0	1	1	1	0	0000h ~ FFFFh	Lower 1/2 locked
1	0	0	0	1	0000h ~ 1F7FFh	Lower 63/64 locked
1	0	0	1	0	0000h ~ 1EFFFh	Lower31/32 locked
1	0	0	1	1	0000h ~ 1DFFFh	Lower 15/16 locked
1	0	1	0	0	0000h ~ 1BFFFh	Lower7/8 locked
1	0	1	0	1	0000h ~ 17FFFh	Lower3/4 locked
1	0	1	1	0	0000h ~ 003Fh	Block0
1	1	0	0	1	0800h ~ 1FFFFh	Upper 63/64 locked
1	1	0	1	0	1000h ~ 1FFFFh	Upper31/32 locked
1	1	0	1	1	2000h ~ 1FFFFh	Upper 15/16 locked
1	1	1	0	0	4000h ~ 1FFFFh	Upper7/8 locked
1	1	1	0	1	8000h ~ 1FFFFh	Upper3/4 locked
1	1	1	1	0	0000h ~ 003Fh	Block0

When WP# is not LOW, user can issue bellows commands to alter the protection states as want.

- Issue SET FEATURES register write (1Fh)
- Issue the feature bit address (A0h) and the feature bits combination as the table

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12.6 Power Lock Down Protection

The Power lock down protection prevent the block protection state from software modifications. After it is enabled, this protection cannot be disabled by a software command. Also, BP[0,2] , INV , CMP and BRWD bits are protected from further software change. Only another power cycle can disable the Power Lock Down Protection.

When the Hardware Protection is disabled during quad or x4 mode, Power Lock Down Protection can be used to prevent a block protection state change.

To enable the Power Lock Down Protection, perform the following command sequence:

- Issue the SET FEATURES command (with address B0h) to set the feature bit BPL to 1:

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12.7 Internal ECC

The device offers data corruption protection by offering optional internal ECC. READs and PROGRAMs with internal ECC can be enabled or disabled by setting feature bit ECC_EN. ECC is enabled by default when device powered on, so the default READ and PROGRAM commands operate with internal ECC in the “active” state when ECC enable.

To enable/disable ECC, perform the following command sequence:

- Issue the SET FEATURES command (1Fh) to set the feature bit ECC_EN:
  1. To enable ECC, Set ECC_EN to 1.
  2. To disable ECC, Clear ECC_EN to 0.

During a PROGRAM operation, the device calculates an ECC code on the 2k page in the cache register, before the page is written to the NAND Flash array.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If error bits are detected, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status bit indicates whether or not the error correction was successful. The ECC Protection table below shows the ECC protection scheme used throughout a page.

There are two ECC protection formats as follow:

- all data in main area and spare areas data are protected.

Any data wrote to the ECC parity data area are ignored when ECC enabled.

Table 12-8. The Distribution of ECC Segment and Spare Area in a Page

Main Area(2KB)				Spare Area(128B)							
User data				User meta data				ECC Parity Data			
Main0	Main1	Main2	Main3	Spare0	Spare1	Spare2	Spare3	Spare0	Spare1	Spare2	Spare3
(512B)	(512B)	(512B)	(512B)	(16B)	(16B)	(16B)	(16B)	(16B)	(16B)	(16B)	(16B)

Table 12-9. ECC Protection and Spare Area E Version

Max Byte Address	Min Byte Address	ECC Protected	Area	Description
1FFh	000h	Yes	Main 0	User data 0
3FFh	200h	Yes	Main 1	User data 1
5FFh	400h	Yes	Main 2	User data 2
7FFh	600h	Yes	Main 3	User data 3
80Fh	800h	Yes	Spare 0	User meta data 0(1)
81Fh	810h	Yes	Spare 1	User meta data 1
82Fh	820h	Yes	Spare 2	User meta data 2
83Fh	830h	Yes	Spare 3	User meta data 3
87Fh	840h	Yes	Spare Area	Internal ECC parity data

Note

1. 800h is reserved for initial bad block mark.
2. When ECC is on, the ECC for main/spare area (840h-87Fh) is prohibited for user, but user can read the Address 840h~87Fh.
3. When ECC is off, the whole page area is open for user.

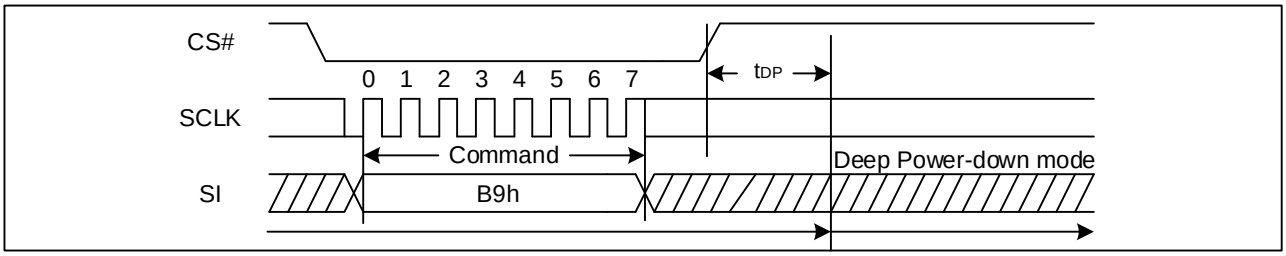
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12.8 Deep Power-Down (B9h)(1.8V Only)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down (ABh), Soft Reset(FFh) or Enable Reset (66h) and Reset (99h) commands. These commands can release the device from this mode. The Release from Deep Power-Down command releases the device from deep power down mode.

The Deep Power-Down Mode automatically stops at Power-Down, and the device is in the Standby Mode after Power-Up. The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of tDP before the supply current is reduced to $I_{CC1\text{-}DPD}$ and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Read Operation is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 12-3. Deep Power-Down Sequence Diagram



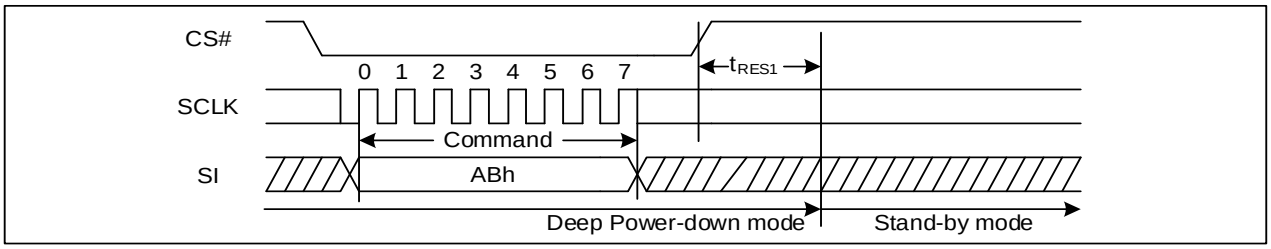
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12.9 Release from Deep Power-Down (ABh)(1.8V Only)

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code “ABh” and driving CS# high. Release from Power-Down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the tRES1 time duration.

When used to release the device from the Power-Down state, the command is the same as previously described, after this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down command is issued while an Erase, Program or Read Operation is in process (when OIP equal 1) the command is ignored and will not have any effects on the current cycle.

Figure 12-4. Release Power-Down Sequence Diagram



Note：

(1) FFh/ABh can get off from the DPD. About tRES1, user can get feature to check OIP if it’s ready.

(2) 66h+99h will terminate the DPD. About tVSL the device will return to its default power-on state and lose all the current feature settings.

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13 POWER ON/OFF TIMING

Figure 13. Power on/off Timing Sequence

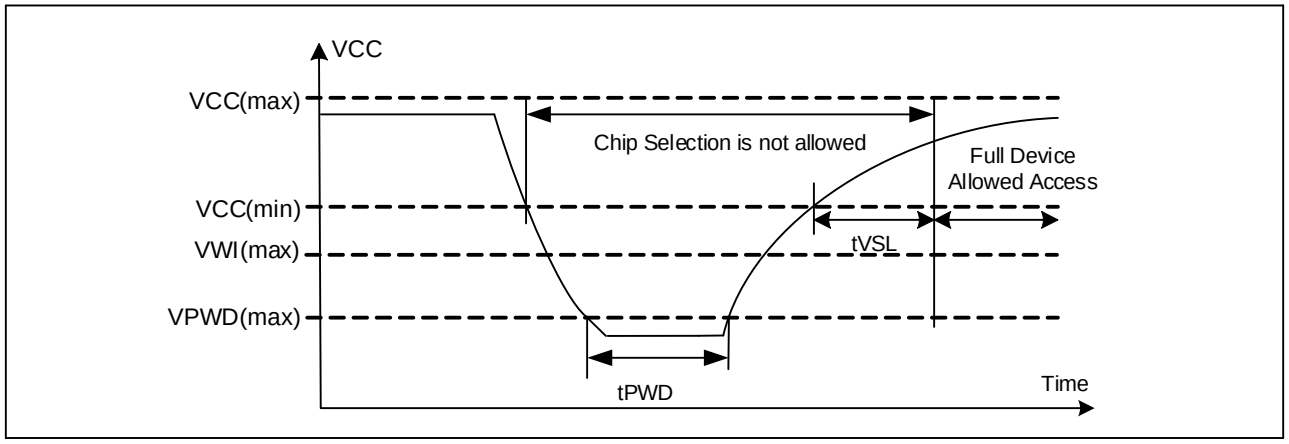


Table 13. Power-On/Off Timing and Write Inhibit Threshold for 1.8V/3.3V

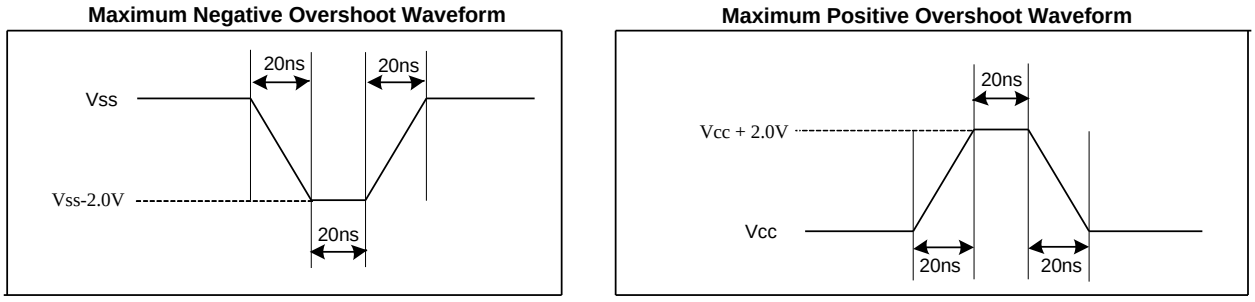
Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC (min.) to device operation	2		ms
VWI	Write Inhibit Voltage(1.8V)		1.5	V
VWI	Write Inhibit Voltage(3.3V)		2.5	V
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		0.7	V
tPWD	The minimum duration for ensuring initialization will occur	50		µs

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14 ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85 / -40 to 105	℃
Storage Temperature	-65 to 150	℃
Applied Input / Output Voltage	-0.6 to VCC+0.4	V
VCC(3.3V)	-0.6 to 4.0	V
VCC(1.8V)	-0.6 to 2.5	V

Figure 14. Overshoot Waveform

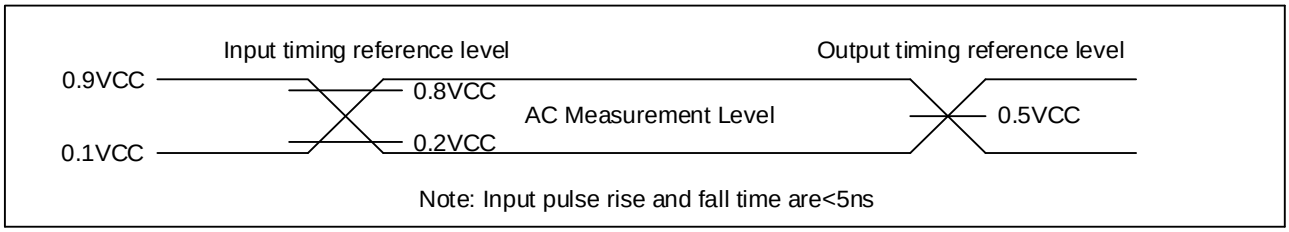


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15 CAPACITANCE MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.9VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.8VCC			V	
	Output Timing Reference Voltage	0.5VCC			V	

Figure 15. Input Test Waveform and Measurement Level



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16 DC CHARACTERISTIC

(T= -40℃~85℃/-40℃~105℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit.
I_{LI}	Input Leakage Current				±10	μA
I_{LO}	Output Leakage Current				±10	μA
I_{CC1}	Standby Current	CS#=VCC, V_{IN}=VCC or VSS		10	50	μA
I_{CC2}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 133MHz, Q=Open(*1,*2,*4 I/O)		15	30	mA
I_{CC3}	Operating Current (Program)			15	30	mA
I_{CC4}	Operating Current (Erase)			15	30	mA
I_{CC5}	Operating Current (Read)			15	30	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.8VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} =1.6mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} =-100μA	VCC-0.2			V

Note: Value guaranteed by design and/or characterization, not 100% tested in production

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(T= -40℃~85℃/-40℃~105℃, VCC=1.7~2.0V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit.
I_{LI}	Input Leakage Current				±10	μA
I_{LO}	Output Leakage Current				±10	μA
I_{CC1}	Standby Current	CS#=VCC, V_{IN}=VCC or VSS		10	50	μA
$I_{CC1-DPD}$	Standby Current Deep Power Down Mode(1.8V only)			1		uA
I_{CC2}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 104MHz, Q=Open(*1,*2,*4 I/O)		10	30	mA
I_{CC3}	Operating Current (Program)			10	30	mA
I_{CC4}	Operating Current (Erase)			10	30	mA
I_{CC5}	Operating Current (Read)			10	30	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.8VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} =1.6mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} =-100μA	VCC-0.2			V

Note: Value guaranteed by design and/or characterization, not 100% tested in production

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17 AC CHARACTERISTICS

(T= -40℃~85℃/-40℃~105℃, VCC=1.7~2.0V/2.7~3.6V, C_L=30pf)

Symbol	Parameter	1.8V		3.3V		Unit.
		Min.	Max.	Min.	Max.	
FC1	Serial Clock Frequency		104		133	MHz
FC_DTR	Serial Clock Frequency For: DTR		80		104	MHz
tCH	Serial Clock High Time	4		3.375		ns
tCL	Serial Clock Low Time	4		3.375		ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.2		0.2		V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.2		0.2		V/ns
tCHSH	CS# Active Hold Time	5		5		ns
tSHCH	CS# Not Active Setup Time	5		5		ns
tSLCH	CS# Active Setup Time	7		5		ns
tCHSL	CS# Not Active Hold Time	5		5		ns
tSHSL/tCS	CS# High Time	20		20		ns
tSHQZ	Output Disable Time		20		20	ns
tCLQX	Output Hold Time	2		2		ns
tCHQX	Output Hold Time (DTR Only)	2		2		ns
tDVCH	Data In Setup Time(STR&DTR)	2		2		ns
tCHDX	Data In Hold Time(STR&DTR)	2		2		ns
tDVCL	Data In Setup Time(DTR Only)	2		2		ns
tCLDX	Data In Hold Time(DTR Only)	2		2		ns
tHLCH	Hold# Low Setup Time (relative to Clock)	5		5		ns
tHHCH	Hold# High Setup Time (relative to Clock)	5		5		ns
tCHHL	Hold# High Hold Time (relative to Clock)	5		5		ns
tCHHH	Hold# Low Hold Time (relative to Clock)	5		5		ns
tHLQZ	Hold# Low To High-Z Output		15		15	ns
tHHQX	Hold# High To Low-Z Output		15		15	ns
tCLQV	Clock Low To Output Valid		9		7	ns
tCHQV	Clock High To Output Valid (DTR Only)		9		7	ns
tWHSL	WP# Setup Time Before CS# Low	20		20		ns
tSHWL	WP# Hold Time After CS# High	100		100		ns
tDP	CS# High To Deep Power-Down Mode		3		-	μs
tRES1	CS# High To Standby Mode		30		-	μs

Note:

Value guaranteed by design and/or characterization, not 100% tested in production

Please contact GigaDevice when there is a need to use the EEh command for DTR.

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18 PERFORMANCE AND TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit.
tRST	CS# High To Next Command After Reset(FFh)			500	us
tRD	Read From Array			25	us
tRD_ECC	Read From Array with ECC		50	120	us
tPROG	Page Programming Time		300	600	us
tPROG_ECC	Page Programming Time with ECC		320	600	us
tBERS	Block Erase Time		3	10	ms

Figure 18-1. Serial Input Timing

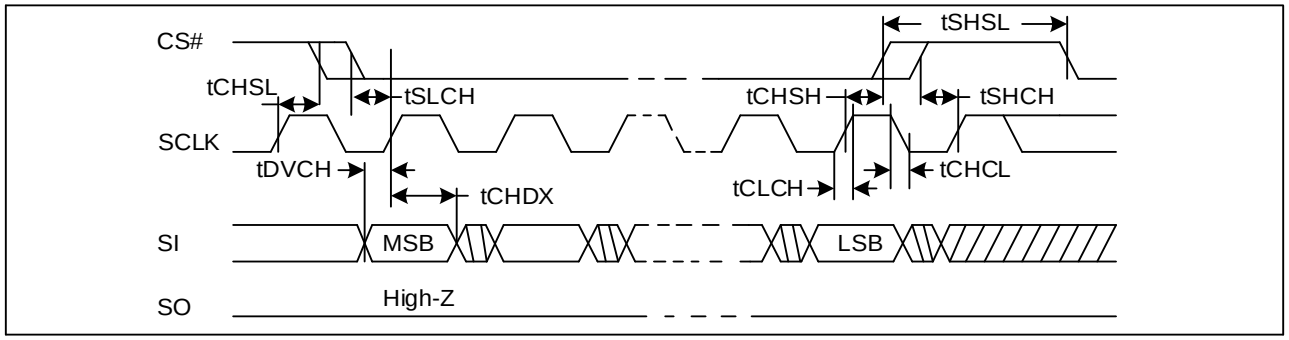
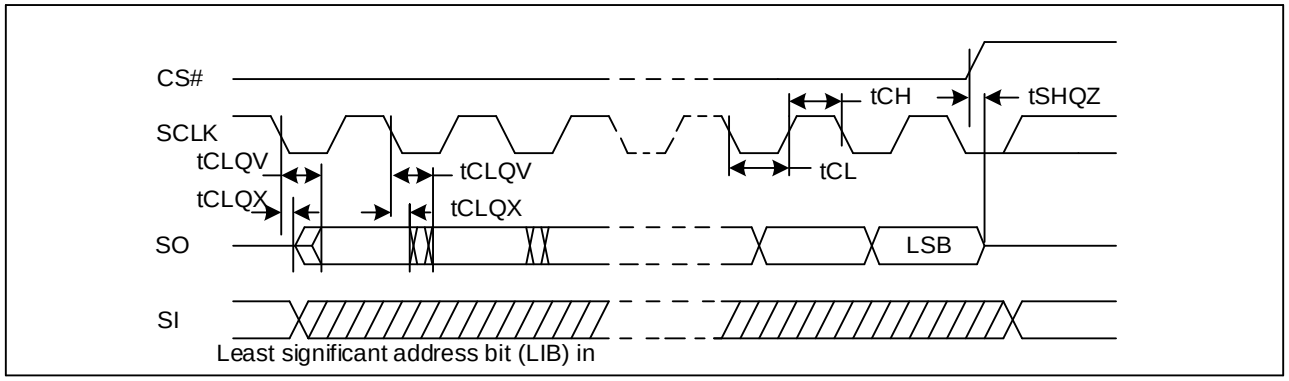


Figure 18-2. Serial Output Timing



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Figure 18-3. Hold Timing

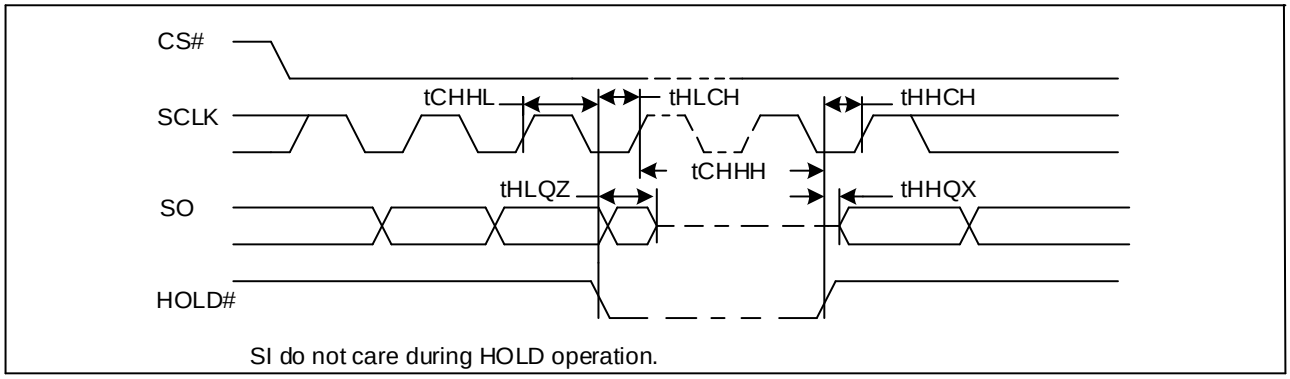


Figure 18-4. Serial Input Timing (DTR)

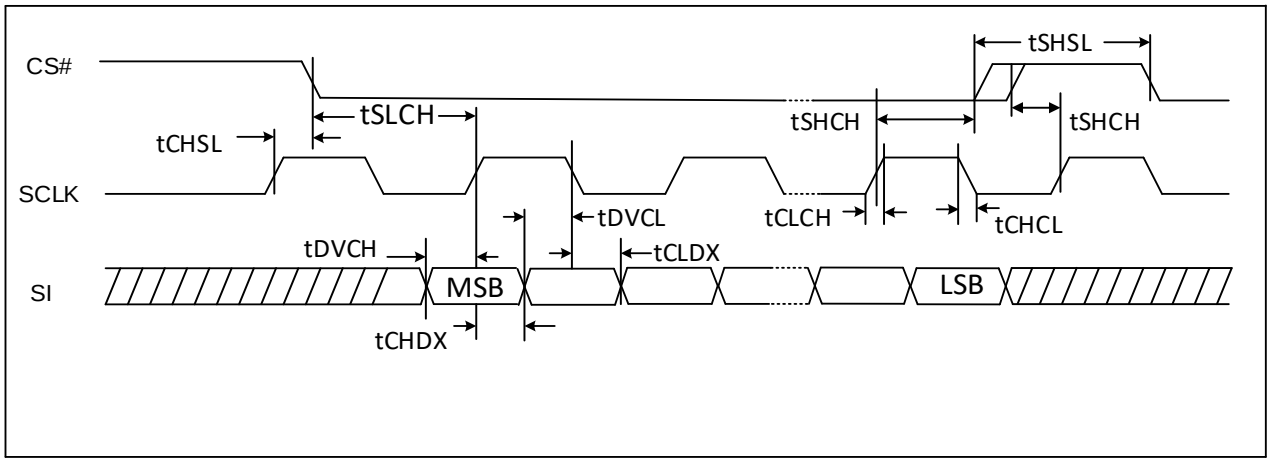
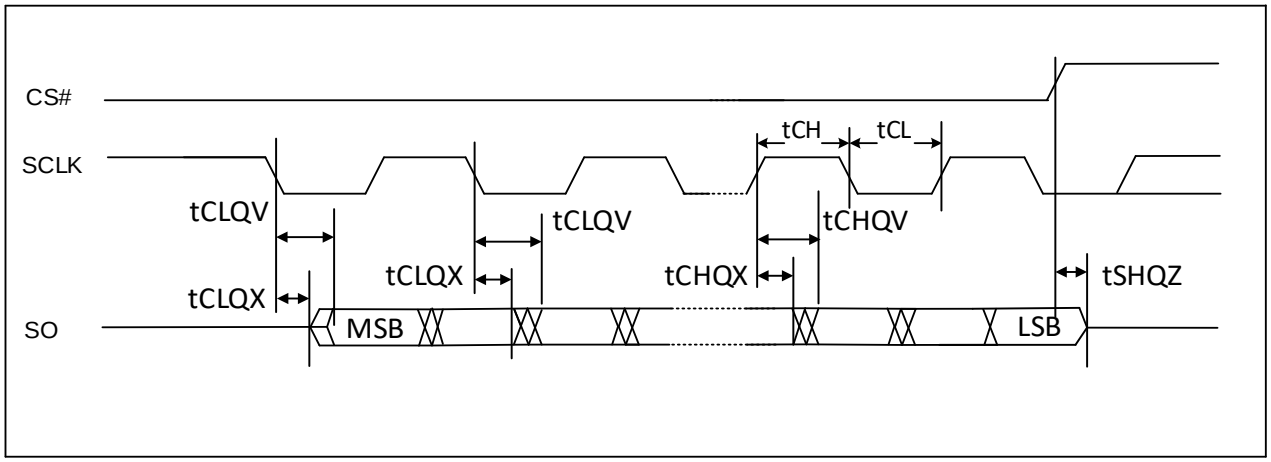
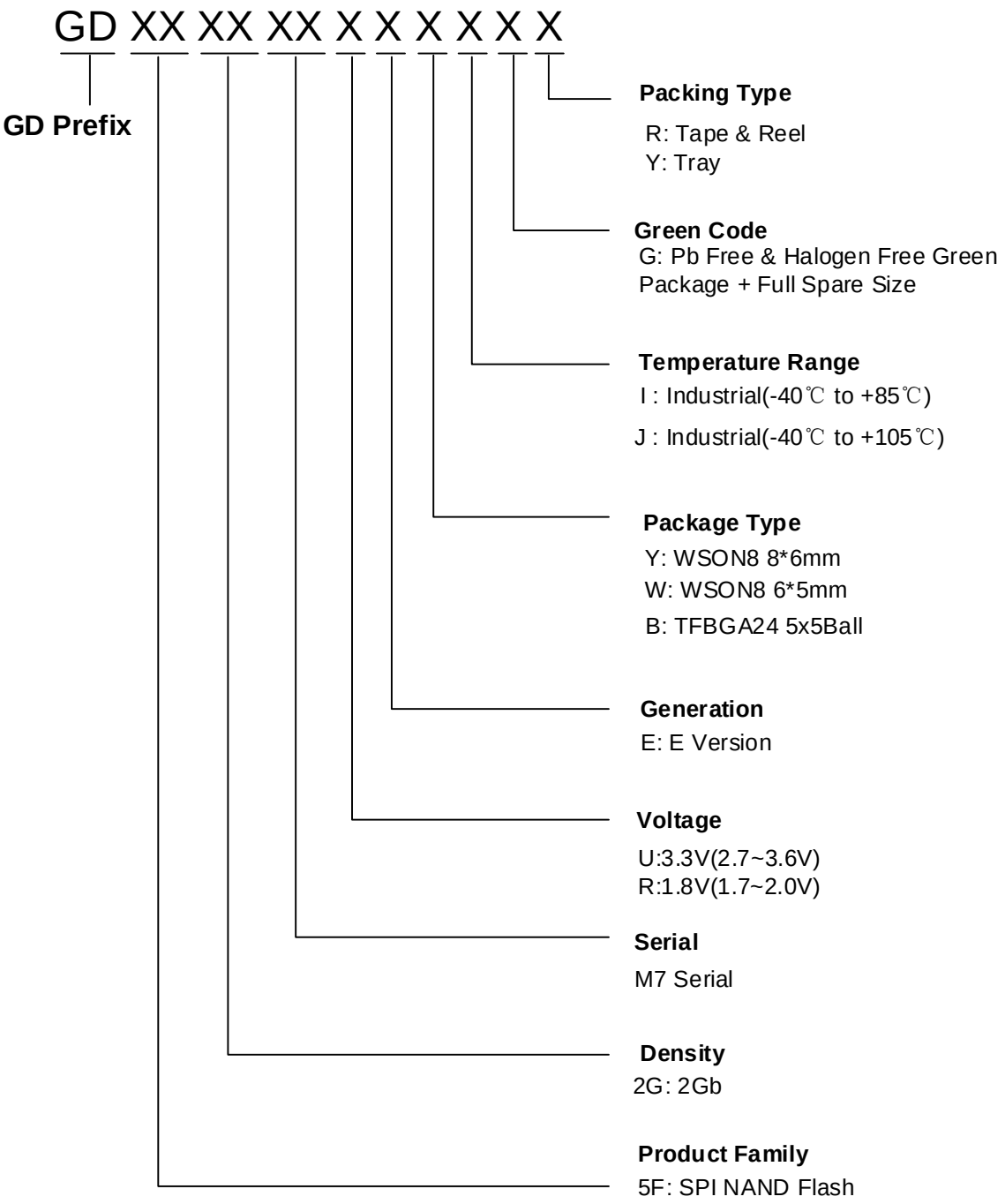


Figure 18-5. Serial Output Timing (DTR)



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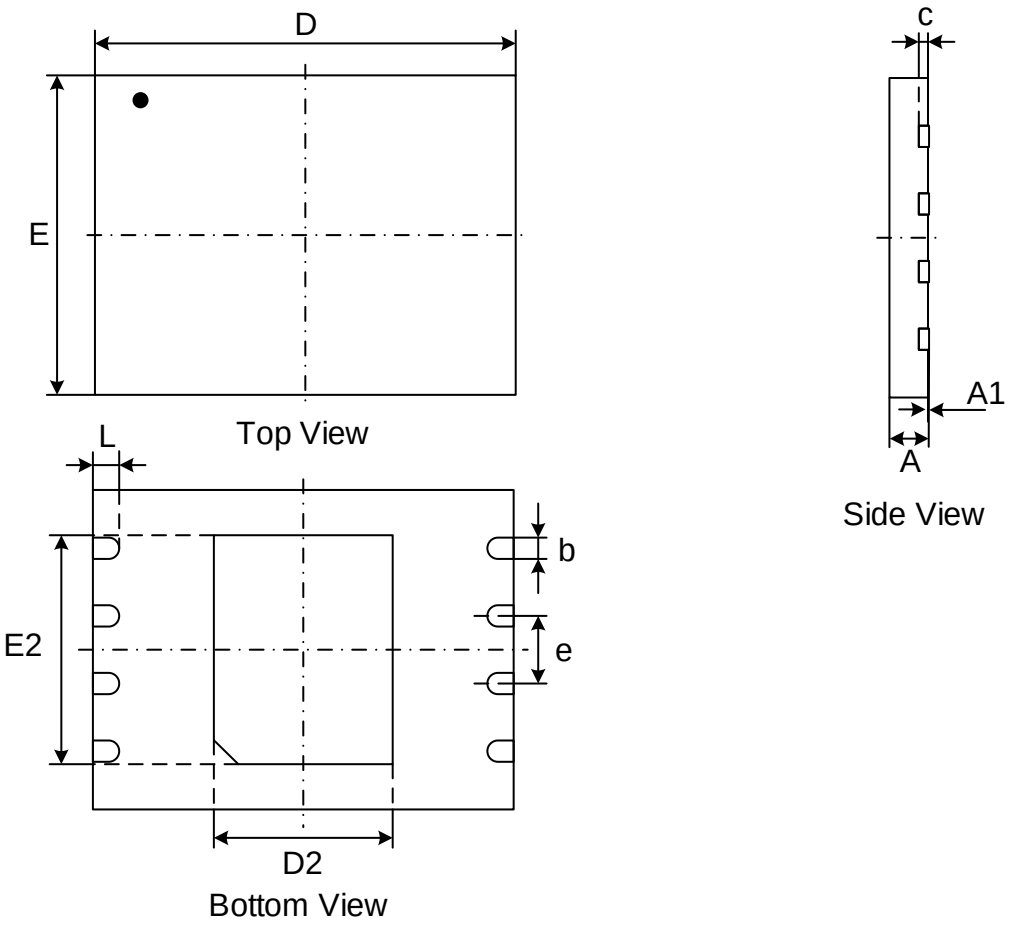
19 ORDERING INFORMATION



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20 PACKAGE INFORMATION

Figure 20-1. WSON8 (8*6mm)

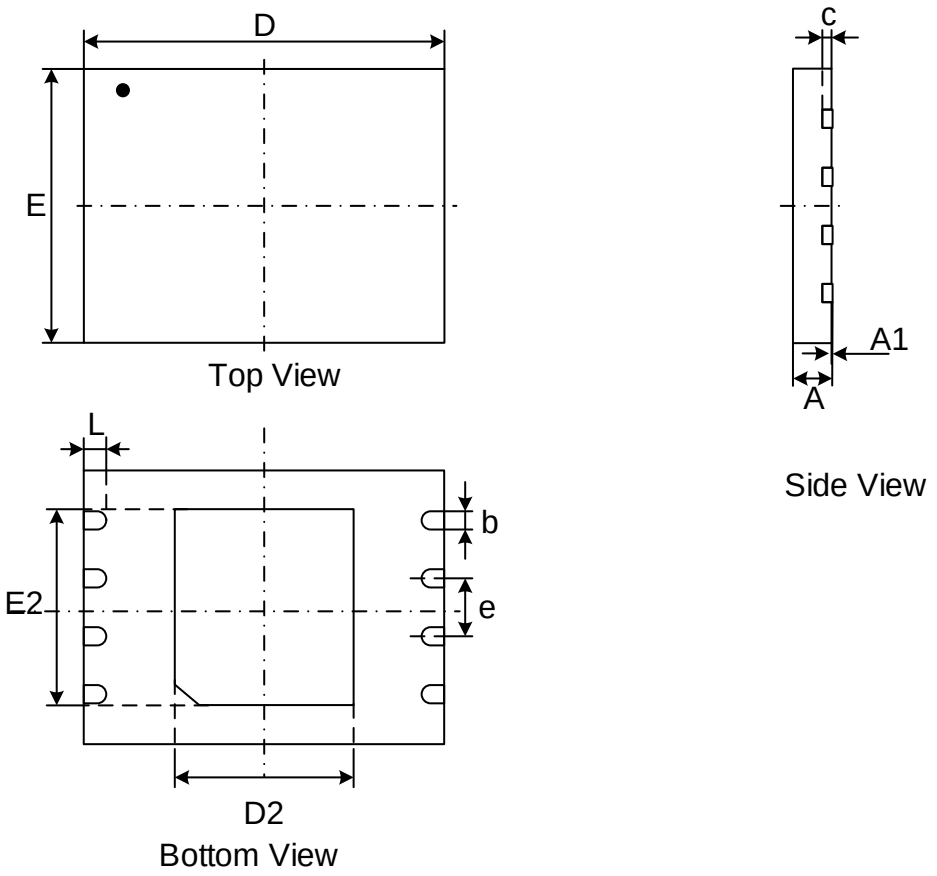


Dimensions

Symbol / Unit		A	A1	c	b	D	D2	E	E2	e	L
mm	Min	0.70	0.00	0.180	0.35	7.90	3.30	5.90	4.20	1.27	0.45
	Nom	0.75	0.02	0.203	0.40	8.00	3.40	6.00	4.30		0.50
	Max	0.80	0.05	0.250	0.45	8.10	3.50	6.10	4.40		0.55
Inch	Min	0.028	0	0.007	0.014	0.311	0.130	0.232	0.165	0.05	0.018
	Nom	0.030	0.001	0.008	0.016	0.315	0.134	0.236	0.169		0.020
	Max	0.032	0.002	0.010	0.018	0.319	0.138	0.240	0.173		0.022

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Figure 20-2. WSON8 (6*5mm)

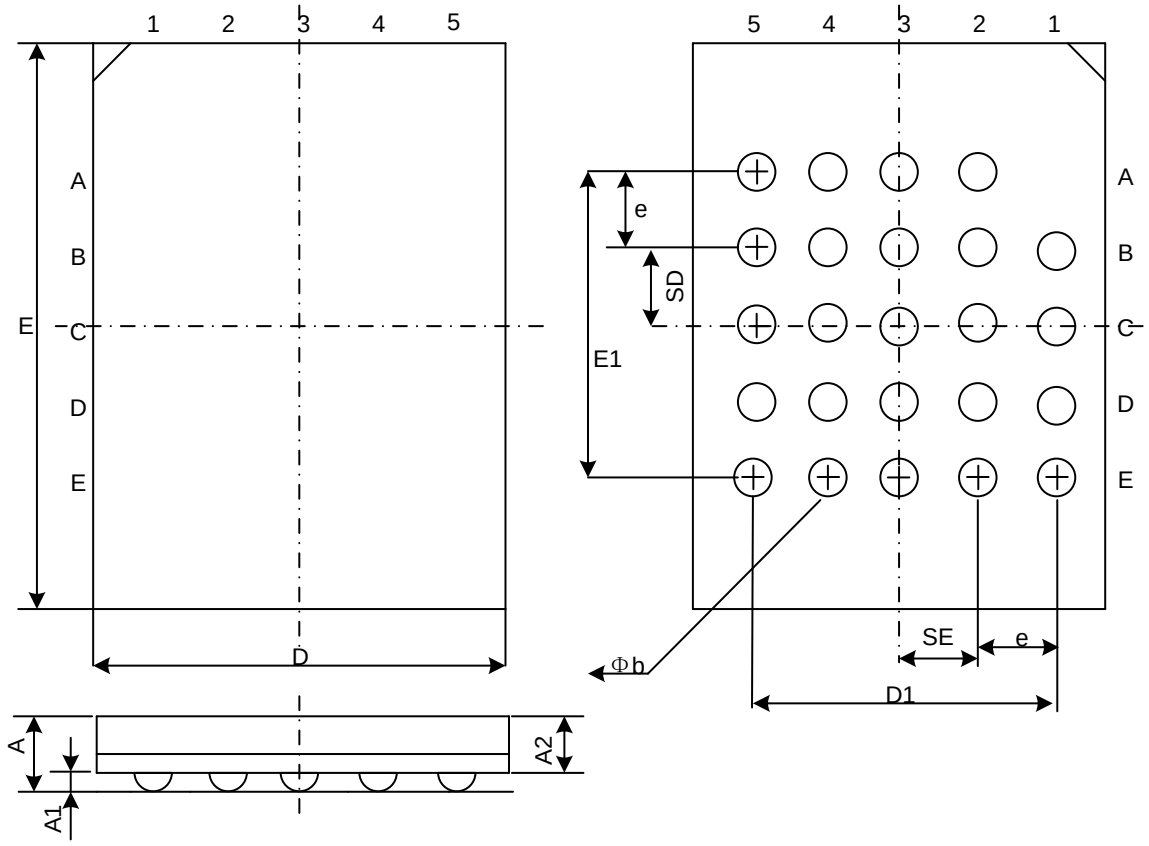


Dimensions

Symbol / Unit		A	A1	c	b	D	D2	E	E2	e	L
mm	Min	0.70	0.00	0.180	0.35	5.90	3.30	4.90	3.90	1.27	0.50
	Nom	0.75	0.02	0.203	0.40	6.00	3.40	5.00	4.00		0.60
	Max	0.80	0.05	0.250	0.45	6.10	3.50	5.10	4.10		0.75
Inch	Min	0.028	0	0.007	0.014	0.232	0.130	0.193	0.154	0.05	0.020
	Nom	0.030	0.001	0.008	0.016	0.236	0.134	0.197	0.157		0.024
	Max	0.032	0.002	0.010	0.018	0.240	0.138	0.201	0.161		0.030

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Figure 20-3. TFBGA-24 6x8 BALL (5*5-1 ball array)



Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	SE	SD
mm	Min		0.25	0.75	0.35	5.90	4.00 BSC	7.90	4.00 BSC	1.00 BSC	1.00 TYP	1.00 TYP
	Nom		0.30	0.80	0.40	6.00		8.00				
	Max	1.20	0.35	0.85	0.45	6.10		8.10				
Inch	Min		0.010	0.030	0.014	0.232	0.157 BSC	0.311	0.157 BSC	0.039 BSC	0.039 TYP	0.039 TYP
	Nom		0.012	0.031	0.016	0.236		0.315				
	Max	0.047	0.014	0.033	0.018	0.240		0.319				

Note：Both package length and width do not include mold flash.

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21 REVISION HISTORY

Version No	Description	Page	Date
1.0	Initial Release		2021-08-16
1.1	Add Note of WP# and HOLD# in 2.3 Pin Description	7	2022-3-24
1.2	Update 1.8V Deep Power Down current Update P/E cycles with ECC to 80K	57 4	2022-12-29
1.3	Add Industrial 105℃ WSON8 8x6 Product and update ordering information Update Industrial 105℃ AC/DC condition Add the note for the P/E cycles 60K at 105℃	6/61 56/57/58 4	2023-10-07
1.4	Add VPWD and tPWD Update Figure13. Power-On/Off Timing Sequence Diagram Modify 3V product tRES1 value	53 53 58	2024-4-29
1.5	Modify the test condition Input Pulse Voltage from ‘0.1VCC to 0.8VCC’ to ‘0.1V to 0.9VCC’ Modify the Input Timing Reference Voltage from ’0.2VCC to 0.7VCC’ to ‘0.2VCC to 0.8VCC’ Modify the tCH and tCL from 3.75ns to 3.375ns.	55 55 58	2024-7-11

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