GigaDevice Semiconductor Inc.

GD32F310xx
Arm® Cortex®-M4 32-bit MCU

Datasheet

Revision 2.0

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1 General description

The GD32F310xx device belongs to the value line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M4 RISC core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. The Cortex®-M4 core features implement a full set of DSP instructions to address digital signal control markets that demand an efficient, easy-to-use blend of control and signal processing capabilities. It also provides a powerful trace technology for enhanced application security and advanced debug support.

The GD32F310xx device incorporates the Arm® Cortex®-M4 32-bit processor core operating at 72 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 128 KB on-chip Flash memory and up to 16 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer one 12-bit ADC, up to five general 16-bit timers, a PWM advanced timer, as well as standard and advanced communication interfaces: up to two SPIs, two I2Cs, an I2S, two USARTs.

The device operates from a 2.6 to 3.6 V power supply and available in –40 to +85 °C temperature range for grade 6 devices, or –40 to +105 °C temperature range for grade 7 devices. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32F310xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike and so on.



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2 Device overview

2.1 Device information

Table 2-1. GD32F310xx devices features and peripheral list

Part Number		GD32F310xx						
		F4P6	F6P6	F8P6	G8U6	G8U7	K6T6	K8T6
Flash	Code area (KB)	16	32	64	64	64	32	64
	Data area (KB)	0	0	0	0	0	0	0
	Total (KB)	16	32	64	64	64	32	64
SRAM (KB)		4	6	8	8	8	6	8
Timers	General timer (16-bit)	4 (2,13,15,16)	4 (2,13,15,16)	4 (2,13,15,16)	5 (2,13-16)	5 (2,13-16)	4 (2,13,15,16)	5 (2,13-16)
	Advanced timer (16-bit)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)
	SysTick	1	1	1	1	1	1	1
	Watchdog	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1
Connectivity	USART	1 (0)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)
	I2C	1 (0)	1 (0)	2 (0-1)	2 (0-1)	2 (0-1)	1 (0)	2 (0-1)
	SPI	1 (0)	1 (0)	2 (0-1)	2 (0-1)	2 (0-1)	1 (0)	2 (0-1)
	I2S	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)
GPIO		15	15	15	23	23	25	25
EXTI		12	12	12	14	14	16	16
ADC	Units	1	1	1	1	1	1	1
	Channels (External)	9	9	9	10	10	10	10
	Channels (Internal)	3	3	3	3	3	3	3
Package		TSSOP20			QFN28		LQFP32	

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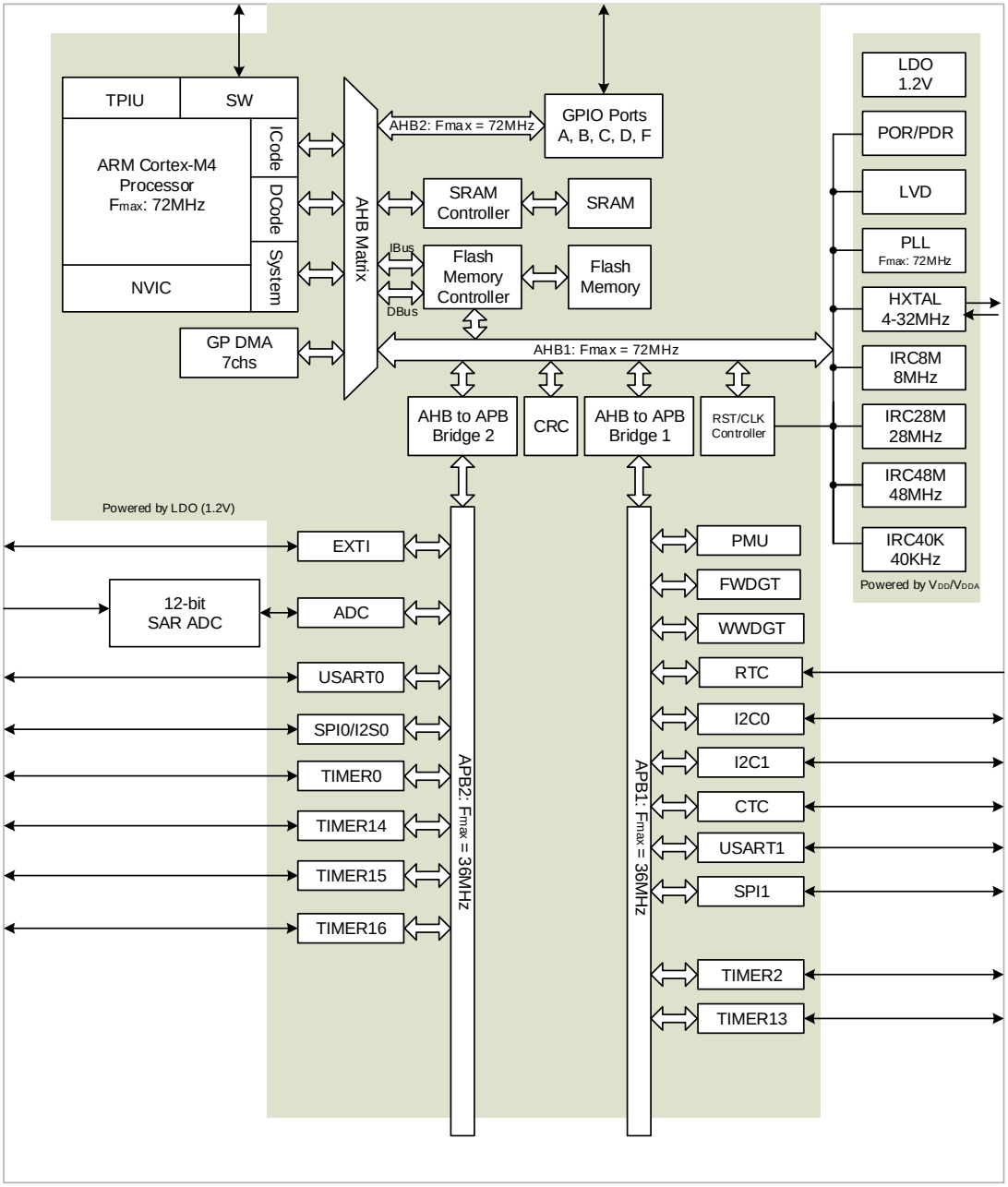
Table 2-2. GD32F310xx devices features and peripheral list (continued)

Part Number		GD32F310xx				
		K8T7	K8U6	C8T6	C8T7	CBT6
Flash	Code area (KB)	64	64	64	64	64
	Data area (KB)	0	0	0	0	64
	Total (KB)	64	64	64	64	128
SRAM (KB)		8	8	8	8	16
Timers	General timer (16-bit)	5 (2,13-16)	5 (2,13-16)	5 (2,13-16)	5 (2,13-16)	5 (2,13-16)
	Advanced timer (16-bit)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)
	SysTick	1	1	1	1	1
	Watchdog	2	2	2	2	2
	RTC	1	1	1	1	1
Connectivity	USART	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)
	I2C	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)
	SPI	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)
	I2S	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)
GPIO		25	27	39	39	39
EXTI		16	16	16	16	16
ADC	Units	1	1	1	1	1
	Channels (External)	10	10	10	10	10
	Channels (Internal)	3	3	3	3	3
Package		LQFP32	QFN32	LQFP48		

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2.2 Block diagram

Figure 2-1. GD32F310xx block diagram



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2.3 Pinouts and pin assignment

Figure 2-2. GD32F310Cx LQFP48 pinouts

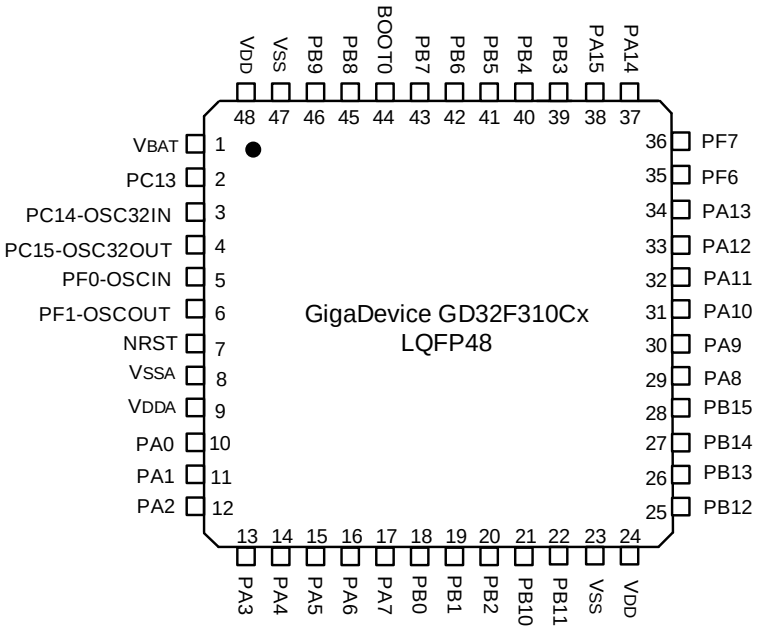
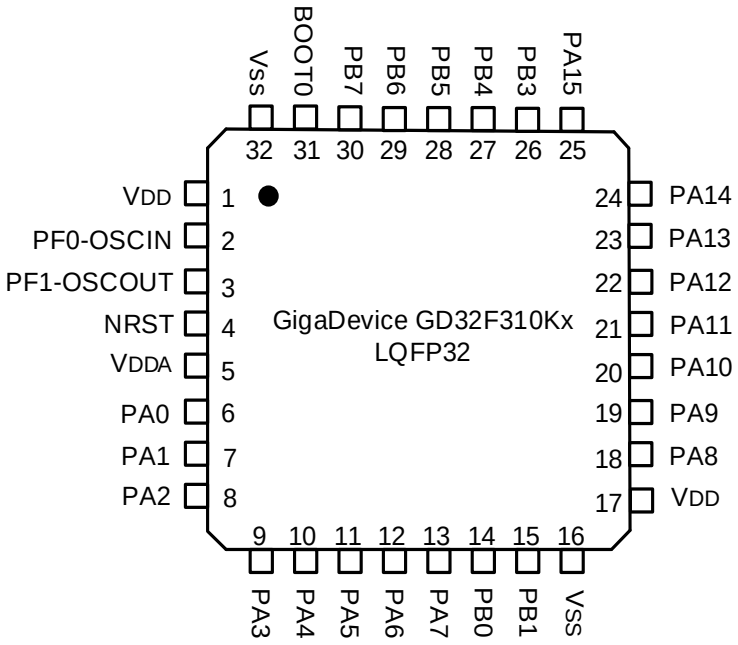


Figure 2-3. GD32F310Kx LQFP32 pinouts



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Figure 2-4. GD32F310KxU6 QFN32 pinouts

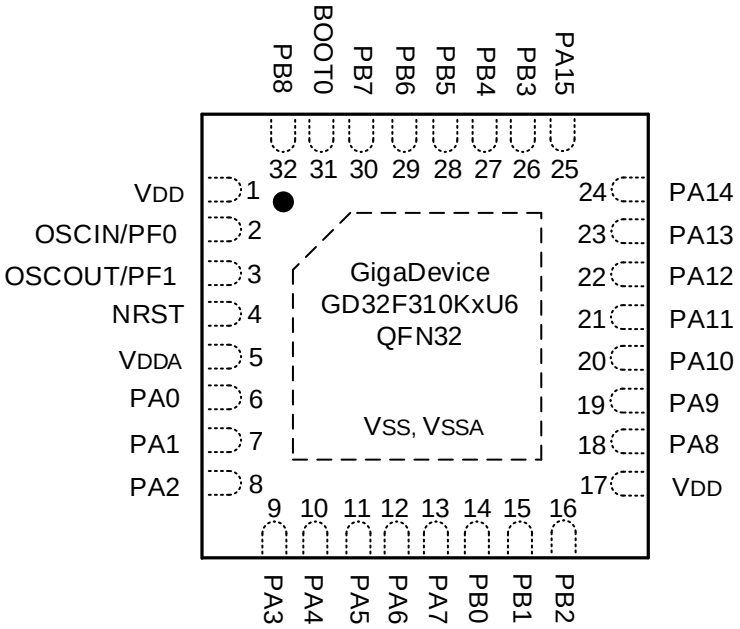
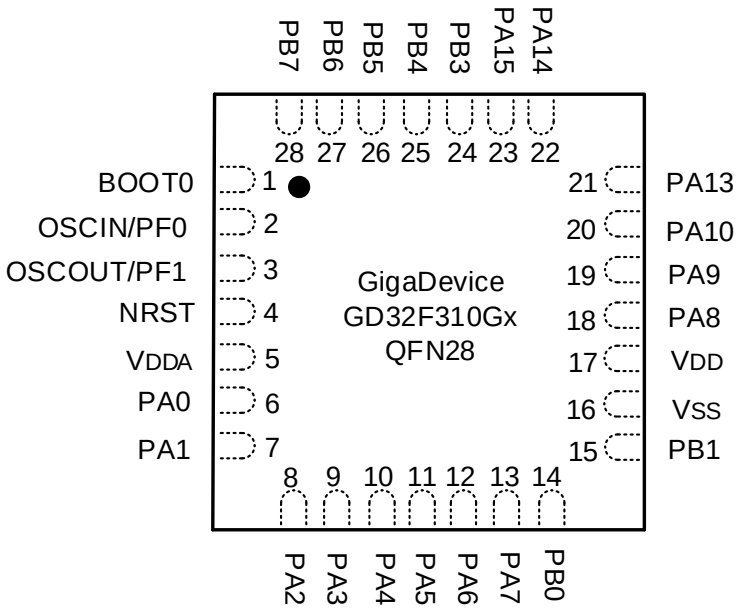
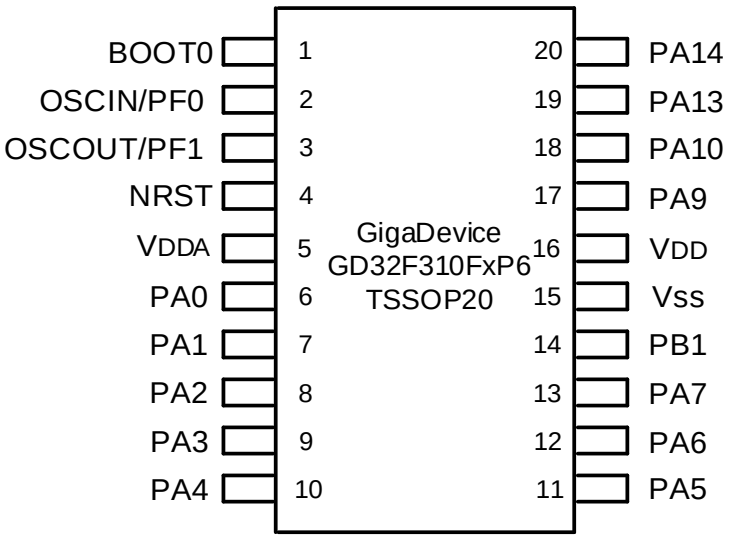


Figure 2-5. GD32F310Gx QFN28 pinouts



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Figure 2-6. GD32F310FxP6 TSSOP20 pinouts



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2.4 Memory map

Table 2-3. GD32F310xx memory map

Pre-defined Regions	Bus	Address	Peripherals
		0xE000 0000 - 0xE00F FFFF	Cortex®-M4 internal peripherals
External Device		0xA000 0000 - 0xDFFF FFFF	Reserved
External RAM		0x6000 0000 - 0x9FFF FFFF	Reserved
Peripherals	AHB1	0x5004 0000 - 0x5FFF FFFF	Reserved
		0x5000 0000 - 0x5003 FFFF	Reserved
	AHB2	0x4800 1800 - 0x4FFF FFFF	Reserved
		0x4800 1400 - 0x4800 17FF	GPIOF
		0x4800 1000 - 0x4800 13FF	Reserved
		0x4800 0C00 - 0x4800 0FFF	GPIOD
		0x4800 0800 - 0x4800 0BFF	GPIOC
		0x4800 0400 - 0x4800 07FF	GPIOB
		0x4800 0000 - 0x4800 03FF	GPIOA
	AHB1	0x4002 4400 - 0x47FF FFFF	Reserved
		0x4002 4000 - 0x4002 43FF	Reserved
		0x4002 3400 - 0x4002 3FFF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2400 - 0x4002 2FFF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1400 - 0x4002 1FFF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0400 - 0x4002 0FFF	Reserved
		0x4002 0000 - 0x4002 03FF	DMA
	APB2	0x4001 8000 - 0x4001 FFFF	Reserved
		0x4001 5C00 - 0x4001 7FFF	Reserved
		0x4001 4C00 - 0x4001 5BFF	Reserved
		0x4001 4800 - 0x4001 4BFF	TIMER16
		0x4001 4400 - 0x4001 47FF	TIMER15
		0x4001 4000 - 0x4001 43FF	TIMER14
		0x4001 3C00 - 0x4001 3FFF	Reserved
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	Reserved
		0x4001 3000 - 0x4001 33FF	SPI0/I2S0
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	Reserved
		0x4001 2400 - 0x4001 27FF	ADC
		0x4001 0800 - 0x4001 23FF	Reserved
		0x4001 0400 - 0x4001 07FF	EXTI

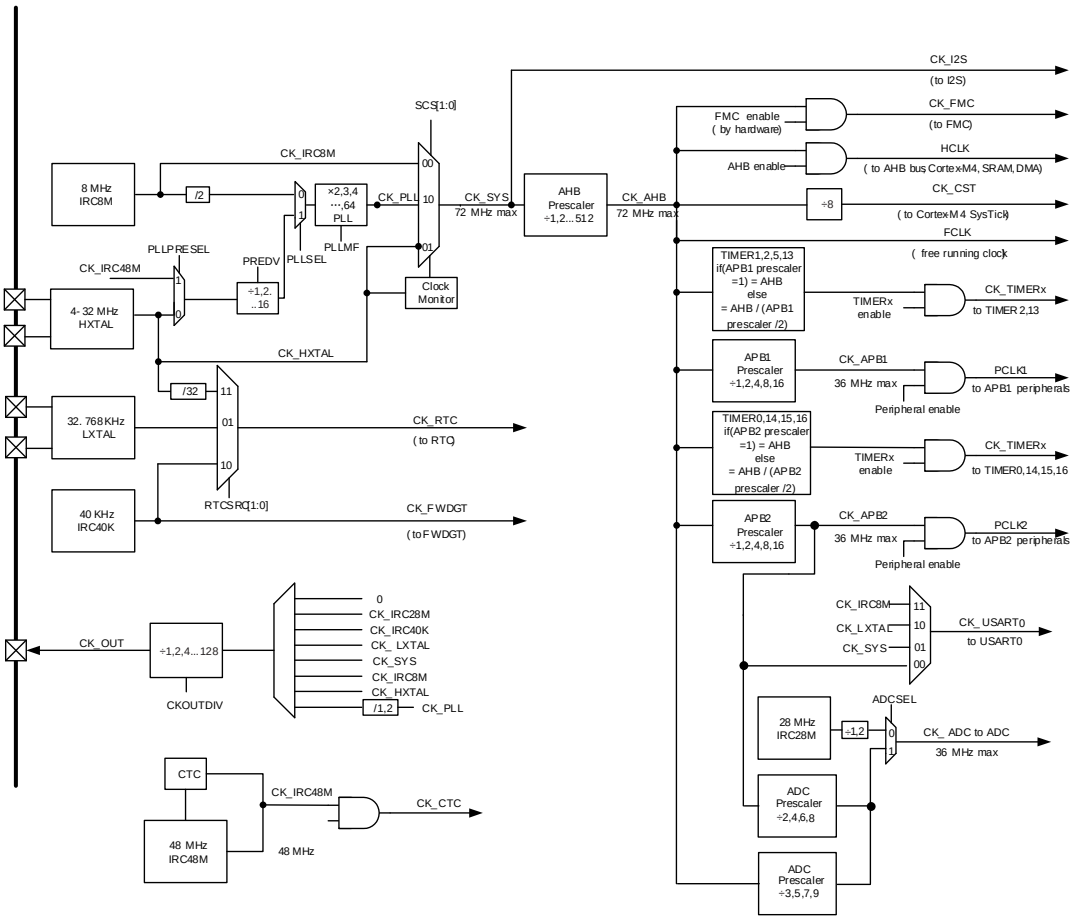
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Pre-defined Regions	Bus	Address	Peripherals
		0x4001 0000 - 0x4001 03FF	SYSCFG
	APB1	0x4000 CC00 - 0x4000 FFFF	Reserved
		0x4000 C800 - 0x4000 CBFF	CTC
		0x4000 C400 - 0x4000 C7FF	Reserved
		0x4000 C000 - 0x4000 C3FF	Reserved
		0x4000 8000 - 0x4000 BFFF	Reserved
		0x4000 7C00 - 0x4000 7FFF	Reserved
		0x4000 7800 - 0x4000 7BFF	Reserved
		0x4000 7400 - 0x4000 77FF	Reserved
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6400 - 0x4000 6FFF	Reserved
		0x4000 6000 - 0x4000 63FF	Reserved
		0x4000 5C00 - 0x4000 5FFF	Reserved
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 4800 - 0x4000 53FF	Reserved
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	Reserved
		0x4000 3C00 - 0x4000 3FFF	Reserved
		0x4000 3800 - 0x4000 3BFF	SPI1
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	TIMER13
		0x4000 1400 - 0x4000 1FFF	Reserved
		0x4000 1000 - 0x4000 13FF	Reserved
		0x4000 0800 - 0x4000 0FFF	Reserved
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	Reserved
SRAM		0x2000 4000 - 0x3FFF FFFF	Reserved
		0x2000 0000 - 0x2000 3FFF	SRAM
Code		0x1FFF FC00 - 0x1FFF FFFF	Reserved
		0x1FFF F800 - 0x1FFF FBFF	Option bytes
		0x1FFF EC00 - 0x1FFF F7FF	System memory
		0x0802 0000 - 0x1FFF EBFF	Reserved
		0x0800 0000 - 0x0801 FFFF	Main Flash memory
		0x0010 0000 - 0x07FF FFFF	Reserved
		0x0000 0000 - 0x000F FFFF	Aliased to Flash or system memory

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2.5 Clock tree

Figure 2-7. GD32F310xx clock tree



Note:

If the APB prescaler is 1, the timer clock frequencies are set to AHB frequency divide by 1. Otherwise, they are set to the AHB frequency divide by half of APB prescaler.

Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC8M: Internal 8M RC oscillators

IRC40K: Internal 40K RC oscillator

IRC48M: Internal 48M RC oscillator

IRC28M: Internal 28M RC oscillators

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2.6 Pin definitions

2.6.1 GD32F310Cx LQFP48 pin definitions

Table 2-4. GD32F310Cx LQFP48 pin definitions

GD32F310Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
V_{BAT}	1	P		Default: V_{BAT}
PC13-TAMPER-RTC	2	I/O		Default: PC13 Additional: RTC_TAMP0, RTC_TS, RTC_OUT, WKUP1
PC14-OSC32IN	3	I/O		Default: PC14 Additional: OSC32IN
PC15-OSC32OUT	4	I/O		Default: PC15 Additional: OSC32OUT
PF0-OSCIN	5	I/O	5VT	Default: PF0 Alternate: CTC_SYNC Additional: OSCIN
PF1-OSCOUT	6	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	7	I/O		Default: NRST
V_{SSA}	8	P		Default: V_{SSA}
V_{DDA}	9	P		Default: V_{DDA}
PA0-WKUP	10	I/O		Default: PA0 Alternate: USART1_CTS, I2C1_SCL Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	11	I/O		Default: PA1 Alternate: USART1_RTS, I2C1_SDA, EVENTOUT Additional: ADC_IN1
PA2	12	I/O		Default: PA2 Alternate: USART1_TX, TIMER14_CH0 Additional: ADC_IN2
PA3	13	I/O		Default: PA3 Alternate: USART1_RX, TIMER14_CH1 Additional: ADC_IN3
PA4	14	I/O		Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART1_CK, TIMER13_CH0, SPI1_NSS Additional: ADC_IN4
PA5	15	I/O		Default: PA5 Alternate: SPI0_SCK, I2S0_CK Additional: ADC_IN5
PA6	16	I/O		Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0,

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GD32F310Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	17	I/O		Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB0	18	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX, EVENTOUT Additional: ADC_IN8
PB1	19	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK Additional: ADC_IN9
PB2	20	I/O	5VT	Default: PB2
PB10	21	I/O	5VT	Default: PB10 Alternate: I2C1_SCL, SPI1_IO2
PB11	22	I/O	5VT	Default: PB11 Alternate: I2C1_SDA, EVENTOUT, SPI1_IO3
V_{SS}	23	P		Default: V_{SS}
V_{DD}	24	P		Default: V_{DD}
PB12	25	I/O	5VT	Default: PB12 Alternate: SPI1_NSS, TIMER0_BRKIN, I2C1_SMBA, EVENTOUT
PB13	26	I/O	5VT	Default: PB13 Alternate: SPI1_SCK, TIMER0_CH0_ON
PB14	27	I/O	5VT	Default: PB14 Alternate: SPI1_MISO, TIMER0_CH1_ON, TIMER14_CH0
PB15	28	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, TIMER0_CH2_ON, TIMER14_CH0_ON, TIMER14_CH1 Additional: RTC_REFIN, WKUP6
PA8	29	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX, EVENTOUT,CTC_SYNC
PA9	30	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN , I2C0_SCL
PA10	31	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA

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GD32F310Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PA11	32	I/O	5VT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT, SPI1_IO2
PA12	33	I/O	5VT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT, SPI1_IO3
PA13	34	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO
PF6	35	I/O	5VT	Default: PF6 Alternate: I2C1_SCL
PF7	36	I/O	5VT	Default: PF7 Alternate: I2C1_SDA
PA14	37	I/O	5VT	Default: PA14 Alternate: USART1_TX, SWCLK, SPI1_MOSI
PA15	38	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, I2S0_WS, USART1_RX, SPI1_NSS, EVENTOUT
PB3	39	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, I2S0_CK, EVENTOUT
PB4	40	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, EVENTOUT
PB5	41	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2S0_SD, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1 Additional:WKUP5
PB6	42	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	43	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON
BOOT0	44	I		Default: BOOT0
PB8	45	I/O	5VT	Default: PB8 Alternate: I2C0_SCL, TIMER15_CH0
PB9	46	I/O	5VT	Default: PB9 Alternate: I2C0_SDA, IFRP_OUT,TIMER16_CH0, EVENTOUT, I2S0_MCK
V_{SS}	47	P		Default: V_{SS}
V_{DD}	48	P		Default: V_{DD}

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

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2.6.2 GD32F310Kx LQFP32 pin definitions

Table 2-5. GD32F310Kx LQFP32 pin definitions

GD32F310Kx LQFP32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
V_{DD}	1	P		Default: V_{DD}
PF0-OSCIN	2	I/O	5VT	Default: PF0 Alternate: CTC_SYNC Additional: OSCIN
PF1-OSCOUT	3	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	4	I/O		Default: NRST
V_{DDA}	5	P		Default: V_{DDA}
PA0-WKUP	6	I/O		Default: PA0 Alternate: USART1_CTS(3), I2C1_SCL(4) Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	7	I/O		Default: PA1 Alternate: USART1_RTS(3), I2C1_SDA(4), EVENTOUT Additional: ADC_IN1
PA2	8	I/O		Default: PA2 Alternate: USART1_TX(3), TIMER14_CH0(4) Additional: ADC_IN2
PA3	9	I/O		Default: PA3 Alternate: USART1_RX(3), TIMER14_CH1(4) Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART1_CK(3), TIMER13_CH0, SPI1_NSS(4) Additional: ADC_IN4
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, I2S0_CK Additional: ADC_IN5
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	13	I/O		Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB0	14	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX(3), EVENTOUT Additional: ADC_IN8
PB1	15	I/O		Default: PB1

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GD32F310Kx LQFP32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(4) Additional: ADC_IN9
V_{SS}	16	P		Default: V_{SS}
V_{DD}	17	P		Default: V_{DD}
PA8	18	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX(3), EVENTOUT, CTC_SYNC
PA9	19	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN(4), I2C0_SCL
PA10	20	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA11	21	I/O	5VT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT, SPI1_IO2(4)
PA12	22	I/O	5VT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT, SPI1_IO3(4)
PA13	23	I/O	5VT	Default: PA13 Alternate: SWDIO, IFRP_OUT, SPI1_MISO(4)
PA14	24	I/O	5VT	Default: PA14 Alternate: USART1_TX(3), SWCLK, SPI1_MOSI(4)
PA15	25	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, I2S0_WS, USART1_RX(3), SPI1_NSS(4), EVENTOUT
PB3	26	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, I2S0_CK, EVENTOUT
PB4	27	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, EVENTOUT
PB5	28	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2S0_SD, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1 Additional: WKUP5
PB6	29	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	30	I/O	5VT	Default: PB7 Alternate:I2C0_SDA, USART0_RX,TIMER16_CH0_ON
BOOT0	31	I		Default: BOOT0
V_{SS}	32	P		Default: V_{SS}

Notes:

(1) Type: I = input, O = output, P = power.

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(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32F310K8/6 devices.

(4) Functions are available on GD32F310K8 devices only.

2.6.3 GD32F310KxU6 QFN32 pin definitions

Table 2-6. GD32F310KxU6 QFN32 pin definitions

GD32F310KxU6 QFN32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
V_{DD}	1	P		Default: V_{DD}
PF0-OSCIN	2	I/O	5VT	Default: PF0 Alternate: CTC_SYNC Additional: OSCIN
PF1-OSCOUT	3	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	4	I/O		Default: NRST
V_{DDA}	5	P		Default: V_{DDA}
PA0-WKUP	6	I/O		Default: PA0 Alternate: USART1_CTS(3), I2C1_SCL(4) Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	7	I/O		Default: PA1 Alternate: USART1_RTS(3), I2C1_SDA(4), EVENTOUT Additional: ADC_IN1
PA2	8	I/O		Default: PA2 Alternate: USART1_TX(3), TIMER14_CH0(4) Additional: ADC_IN2
PA3	9	I/O		Default: PA3 Alternate: USART1_RX(3), TIMER14_CH1(4) Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART1_CK(3), TIMER13_CH0, SPI1_NSS(4) Additional: ADC_IN4
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, I2S0_CK Additional: ADC_IN5
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	13	I/O		Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB0	14	I/O		Default: PB0

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GD32F310KxU6 QFN32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX(3), EVENTOUT Additional: ADC_IN8
PB1	15	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(4) Additional: ADC_IN9
PB2	16	I/O	5VT	Default: PB2
V_{DD}	17	P		Default: V_{DD}
PA8	18	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX(3), EVENTOUT, CTC_SYNC
PA9	19	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN(4), I2C0_SCL
PA10	20	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA11	21	I/O	5VT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, EVENTOUT, SPI1_IO2(4)
PA12	22	I/O	5VT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, EVENTOUT, SPI1_IO3(4)
PA13	23	I/O	5VT	Default: PA13 Alternate: SWDIO, IFRP_OUT, SPI1_MISO(4)
PA14	24	I/O	5VT	Default: PA14 Alternate: USART1_TX(3), SWCLK, SPI1_MOSI(4)
PA15	25	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, I2S0_WS, USART1_RX(3), SPI1_NSS(4), EVENTOUT
PB3	26	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, I2S0_CK, EVENTOUT
PB4	27	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, EVENTOUT
PB5	28	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2S0_SD, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1 Additional: WKUP5
PB6	29	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	30	I/O	5VT	Default: PB7 Alternate:I2C0_SDA, USART0_RX,TIMER16_CH0_ON

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GD32F310KxU6 QFN32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
BOOT0	31	I		Default: BOOT0
PB8	32	I/O	5VT	Default: PB8 Alternate: I2C0_SCL, TIMER15_CH0

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32F310K8/6 devices.

(4) Functions are available on GD32F310K8 devices only.

2.6.4 GD32F310Gx QFN28 pin definitions

Table 2-7. GD32F310Gx QFN28 pin definitions

GD32F310Gx QFN28				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
BOOT0	1	I		Default: BOOT0
PF0-OSCIN	2	I/O	5VT	Default: PF0 Alternate: CTC_SYNC Additional: OSCIN
PF1-OSCOUT	3	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	4	I/O		Default: NRST
V_{DDA}	5	P		Default: V_{DDA}
PA0-WKUP	6	I/O		Default: PA0 Alternate: USART1_CTS, I2C1_SCL Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	7	I/O		Default: PA1 Alternate: USART1_RTS, I2C1_SDA, EVENTOUT Additional: ADC_IN1
PA2	8	I/O		Default: PA2 Alternate: USART1_TX, TIMER14_CH0 Additional: ADC_IN2
PA3	9	I/O		Default: PA3 Alternate: USART1_RX, TIMER14_CH1 Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART1_CK, TIMER13_CH0, SPI1_NSS Additional: ADC_IN4
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, I2S0_CK Additional: ADC_IN5
PA6	12	I/O		Default: PA6

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GD32F310Gx QFN28				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	13	I/O		Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB0	14	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, USART1_RX, EVENTOUT Additional: ADC_IN8
PB1	15	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK Additional: ADC_IN9
V_{SS}	16	P		Default: V_{SS}
V_{DD}	17	P		Default: V_{DD}
PA8	18	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX, EVENTOUT,CTC_SYNC
PA9	19	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN , I2C0_SCL
PA10	20	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA13	21	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO
PA14	22	I/O	5VT	Default: PA14 Alternate: USART1_TX, SWCLK, SPI1_MOSI
PA15	23	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, I2S0_WS, USART1_RX, SPI1_NSS, EVENTOUT
PB3	24	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, I2S0_CK, EVENTOUT
PB4	25	I/O	5VT	Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, EVENTOUT
PB5	26	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2S0_SD, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1 Additional:WKUP5
PB6	27	I/O	5VT	Default: PB6

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GD32F310Gx QFN28				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON
PB7	28	I/O	5VT	Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.5 GD32F310FxP6 TSSOP20 pin definitions

Table 2-8. GD32F310FxP6 TSSOP20 pin definitions

GD32F310FxP6 TSSOP20				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
BOOT0	1	I		Default: BOOT0
PF0-OSCIN	2	I/O	5VT	Default: PF0 Alternate: CTC_SYNC Additional: OSCIN
PF1-OSCOUT	3	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	4	I/O		Default: NRST
V_{DDA}	5	P		Default: V_{DDA}
PA0-WKUP	6	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), I2C1_SCL(5) Additional: ADC_IN0, RTC_TAMP1, WKUP0
PA1	7	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), I2C1_SDA(5), EVENTOUT Additional: ADC_IN1
PA2	8	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4) Additional: ADC_IN2
PA3	9	I/O		Default: PA3 Alternate: USART0_RX(3), USART1_RX(4) Additional: ADC_IN3
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, SPI1_NSS(5) Additional: ADC_IN4
PA5	11	I/O		Default: PA5 Alternate: SPI0_SCK, I2S0_CK Additional: ADC_IN5

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GD32F310FxP6 TSSOP20				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, EVENTOUT Additional: ADC_IN6
PA7	13	I/O		Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, EVENTOUT Additional: ADC_IN7
PB1	14	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, SPI1_SCK(5) Additional: ADC_IN9
V_{SS}	15	P		Default: V_{SS}
V_{DD}	16	P		Default: V_{DD}
PA9	17	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, I2C0_SCL
PA10	18	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, I2C0_SDA
PA13	19	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO(5)
PA14	20	I/O	5VT	Default: PA14 Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI(5)

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available on GD32F310F4 devices only.

(4) Functions are available on GD32F310F8/6 devices.

(5) Functions are available on GD32F310F8 devices.

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2.6.6 GD32F310xx pin alternate functions

Table 2-9. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PA0		USART0_CTS(1) USART1_CTS(2)			I2C1_SCL(3)		
PA1	EVENTOUT	USART0_RTS(1) USART1_RTS(2)			I2C1_SDA(3)		
PA2	TIMER14_CH0	USART0_TX(1) USART1_TX(2)					
PA3	TIMER14_CH1	USART0_RX(1) USART1_RX(2)					
PA4	SPI0_NSS/ I2S0_WS	USART0_CK(1) USART1_CK(2)			TIMER13_CH0		SPI1_NSS(3)
PA5	SPI0_SCK/ I2S0_CK						
PA6	SPI0_MISO/I2S0_MCK	TIMER2_CH0	TIMER0_BRKIN			TIMER15_CH0	EVENTOUT
PA7	SPI0_MOSI/ I2S0_SD	TIMER2_CH1	TIMER0_CH0_ON		TIMER13_CH0	TIMER16_CH0	EVENTOUT
PA8	CK_OUT	USART0_CK	TIMER0_CH0	EVENTOUT	USART1_TX(2)		CTC_SYNC
PA9	TIMER14_BRKIN	USART0_TX	TIMER0_CH1		I2C0_SCL		
PA10	TIMER16_BRKIN	USART0_RX	TIMER0_CH2		I2C0_SDA		
PA11	EVENTOUT	USART0_CTS	TIMER0_CH3				SPI1_IO2(3)
PA12	EVENTOUT	USART0_RTS	TIMER0_ETI				SPI1_IO3(3)
PA13	SWDIO	IFRP_OUT					SPI1_MISO(3)
PA14	SWCLK	USART0_TX(1) USART1_TX(2)					SPI1_MOSI(3)
PA15	SPI0_NSS/ I2S0_WS	USART0_RX(1) USART1_RX(2)		EVENTOUT			SPI1_NSS(3)

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Table 2-10. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PB0	EVENTOUT	TIMER2_CH2	TIMER0_CH1_ON		USART1_RX(2)		
PB1	TIMER13_CH0	TIMER2_CH3	TIMER0_CH2_ON				SPI1_SCK(3)
PB2							
PB3	SPI0_SCK / I2S0_CK	EVENTOUT					
PB4	SPI0_MISO / I2S0_MCK	TIMER2_CH0	EVENTOUT				
PB5	SPI0_MOSI / I2S0_SD	TIMER2_CH1	TIMER15_BRKIN	I2C0_SMBA			
PB6	USART0_TX	I2C0_SCL	TIMER15_CH0_ON				
PB7	USART0_RX	I2C0_SDA	TIMER16_CH0_ON				
PB8		I2C0_SCL	TIMER15_CH0				
PB9	IFRP_OUT	I2C0_SDA	TIMER16_CH0	EVENTOUT		I2S0_MCK	
PB10		I2C0_SCL(1) I2C1_SCL(3)					SPI1_IO2(3)
PB11	EVENTOUT	I2C0_SDA(1), I2C1_SDA(3)					SPI1_IO3(3)
PB12	SPI0_NSS(1) SPI1_NSS(3)	EVENTOUT	TIMER0_BRKIN		I2C1_SMBA(3)		
PB13	SPI0_SCK(1) SPI1_SCK(3)		TIMER0_CH0_ON				
PB14	SPI0_MISO(1) SPI1_MISO(3)	TIMER14_CH0	TIMER0_CH1_ON				
PB15	SPI0_MOSI(1) SPI1_MOSI(3)	TIMER14_CH1	TIMER0_CH2_ON	TIMER14_CH0_ON			

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Table 2-11. Port C alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PC0	EVENTOUT						
PC1	EVENTOUT						
PC2	EVENTOUT						
PC3	EVENTOUT						
PC4	EVENTOUT						
PC5							
PC6	TIMER2_CH0		I2S0_MCK				
PC7	TIMER2_CH1						
PC8	TIMER2_CH2						
PC9	TIMER2_CH3						
PC10							
PC11							
PC12							
PC13							
PC14							
PC15							

Table 2-12. Port D alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PD0							
PD1							
PD2	TIMER2_ETI						
PD3							
PD4							
PD5							
PD6							
PD7							
PD8							
PD9							
PD10							
PD11							
PD12							
PD13							
PD14							
PD15							

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Table 2-13. Port F alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PF0	CTC_SYNC						
PF1							
PF2							
PF3							
PF4	EVENTOUT						
PF5	EVENTOUT						
PF6	I2C0_SCL(1) I2C1_SCL(3)						
PF7	I2C0_SDA(1) I2C1_SDA(3)						
PF8							
PF9							
PF10							
PF11							
PF12							
PF13							
PF14							
PF15							

Notes:

(1) Functions are available on GD32F310x4 devices only.

(2) Functions are available on GD32F310xB/8/6 devices.

(3) Functions are available on GD32F310xB/8 devices.

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3 Functional description

3.1 Arm® Cortex®-M4 core

The Arm® Cortex®-M4 processor is a high performance embedded processor with DSP instructions which allow efficient signal processing and complex algorithm execution. It brings an efficient, easy-to-use blend of control and signal processing capabilities to meet the digital signal control markets demand. The processor is highly configurable enabling a wide range of implementations from those requiring memory protection and powerful trace technology to cost sensitive devices requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

32-bit Arm® Cortex®-M4 processor core:

- Up to 72 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Floating Point Unit (FPU)
- Integrated DSP instructions
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M4 processor is based on the Armv7-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M4:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Serial Wire Debug Port (SW-DP)
- Trace Port Interface Unit (TPIU)

3.2 On-chip memory

- Up to 128 Kbytes of Flash memory
- The region of the MCU executing instructions without waiting time is up to 64K bytes (in case that Flash size equal to 16K, 32K or 64K, all memory is no waiting time). A long delay when CPU fetches the instructions out of the range.
- Up to 16 Kbytes of SRAM with hardware parity checking

The Arm® Cortex®-M4 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 128 Kbytes of inner Flash at most, which includes code Flash and data Flash is available for storing programs and data, and there is

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no waiting time within code Flash area when CPU executes instructions. ***Table 2-3. GD32F310xx memory map*** shows the memory map of the GD32F310xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3 Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 48 MHz RC oscillator
- Internal 28 MHz RC oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB, APB2 and APB1 domains is 72 MHz/36 MHz/36 MHz. See ***Figure 2-7. GD32F310xx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 2.6 V and down to 1.8V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL.
- V_{BAT} range: 1.8 to 3.6 V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

In default condition, boot from main Flash memory is selected. The boot loader is located in

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the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10) or USART1 (PA14 and PA15).

3.5 Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep mode**
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep mode**
  In deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC8M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, RTC tamper and timestamp, LVD output and USART wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.
- **Standby mode**
  In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. The contents of SRAM and registers (except backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, and the rising edge on WKUP pin.

3.6 Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 2.86 MSPS
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Input voltage range: V_{SSA} to V_{DDA} (2.6 to 3.6 V)
- Temperature sensor

One 12-bit 2.86 MSPS multi-channel ADCs are integrated in the device. It has a total of 19 multiplexed channels: 10 external channels, 1 channel for internal temperature sensor (V_{SENSE}), 1 channel for internal reference voltage (V_{REFINT}) and 1 channel for battery voltage (V_{BAT}). The input voltage range is between V_{SSA} and V_{DDA}. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

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The ADC can be triggered from the events generated by the general level 0 timers (TIMER2) and the advanced timer (TIMER0) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

3.7 DMA

- 7 channel DMA controller
- Peripherals supported: Timers, ADC, SPIs, I2Cs, USARTs and I2S

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.8 General-purpose inputs/outputs (GPIOs)

- Up to 39 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 39 general purpose I/O pins (GPIO) in GD32F310xx, named PA0 ~ PA15 and PB0 ~ PB15, PC13 ~ PC15, PF0, PF1, PF6, PF7 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull, open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.9 Timers and PWM generation

- One 16-bit advanced timer (TIMER0) and five 16-bit general timers (TIMER2, TIMER13 ~ TIMER16)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input

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- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge-aligned or center-aligned mode) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER2 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER13 ~ TIMER16 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The GD32F310xx have two watchdog peripherals, free watchdog and window watchdog. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler. It is clocked from an independent 40 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.10 Real time clock (RTC)

- Independent binary-coded decimal (BCD) format timer/counter with five 32-bit backup registers.

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- Calendar with subsecond, seconds, minutes, hours, week day, date, year and month automatically correction
- Alarm function with wake up from deep-sleep and standby mode capability
- On-the-fly correction for synchronization with master clock. Digital calibration with 0.954 ppm resolution for compensation of quartz crystal inaccuracy.

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. In the RTC unit, there are two prescalers used for implementing the calendar and other functions. One prescaler is a 7-bit asynchronous prescaler and the other is a 15-bit synchronous prescaler.

3.11 Inter-integrated circuit (I2C)

- Up to two I2C bus interfaces can support both master and slave mode with a frequency up to 1 MHz (Fast mode plus)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides different data transfer rates: up to 100 KHz in standard mode, up to 400 KHz in the fast mode and up to 1 MHz in the fast mode plus. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.12 Serial peripheral interface (SPI)

- Up to two SPI interfaces with a frequency of up to 18 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

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3.13 Universal synchronous asynchronous receiver transmitter (USART)

- Up to two USARTs with operating frequency up to 4.5 MB/s
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.14 Inter-IC sound (I2S)

- One I2S bus Interfaces with sampling frequency from 8 KHz to 192 KHz, multiplexed with SPI0
- Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 3-wire serial lines. GD32F310xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI0. The audio sampling frequency from 8 KHz to 192 KHz is supported with less than 0.5% accuracy error.

3.15 Debug mode

- Serial wire debug port (SW-DP)

Debug capabilities can be accessed by a debug tool via serial wire.

3.16 Package and operation temperature

- LQFP48 (GD32F310Cx), LQFP32 (GD32F310KxT6), QFN32 (GD32F310KxU6), QFN28 (GD32F310GxU6) and TSSOP20 (GD32F310FxP6)
- Operation temperature range: -40°C to +85°C for grade 6 devices (industrial level), or –40 to +105 °C for grade 7 devices (industrial level)

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4 Electrical characteristics

4.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly over the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings(1)(4)

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range(2)	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5V tolerant pin(3)	V_{SS} - 0.3	V_{DD} + 3.6	V
	Input voltage on other I/O	V_{SS} - 0.3	3.6	V
$\|\Delta V_{DDx}\|$	Variations between different VDD power pins	—	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between different ground pins	—	50	mV
I_{IO}	Maximum current for GPIO pin	—	±25	mA
T_A	Operating temperature range for grade 6 device	-40	+85	°C
	Operating temperature range for grade 7 device	-40	+105	
P_D	Power dissipation at T_A = 85°C of LQFP48(5)	—	621	mW
	Power dissipation at T_A = 85°C of LQFP32(5)	—	605	
	Power dissipation at T_A = 85°C of QFN32(5)	—	825	
	Power dissipation at T_A = 85°C of QFN28(5)	—	605	
	Power dissipation at T_A = 85°C of TSSOP20(5)	—	553	
	Power dissipation at T_A = 105°C of LQFP48(5)	—	311	
	Power dissipation at T_A = 105°C of LQFP32(5)	—	303	
	Power dissipation at T_A = 105°C of QFN28(5)	—	303	
T_{STG}	Storage temperature range	-65	+150	°C
T_J	Maximum junction temperature	—	125	°C

(1) Guaranteed by design, not tested in production.

(2) All main power and ground pins should be connected to an external power source within the allowable range.

(3) V_{IN} maximum value cannot exceed 5.5 V.

(4) It is recommended that VDD and VDDA are powered by the same source. The maximum difference between VDD and VDDA does not exceed 300 mV during power-up and operation.

(5) For grade 6 devices, the parameter of T_A=85°C, For grade 7 devices, the parameter of T_A=105°C.

4.2 Operating conditions characteristics

Table 4-2. DC operating conditions

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit

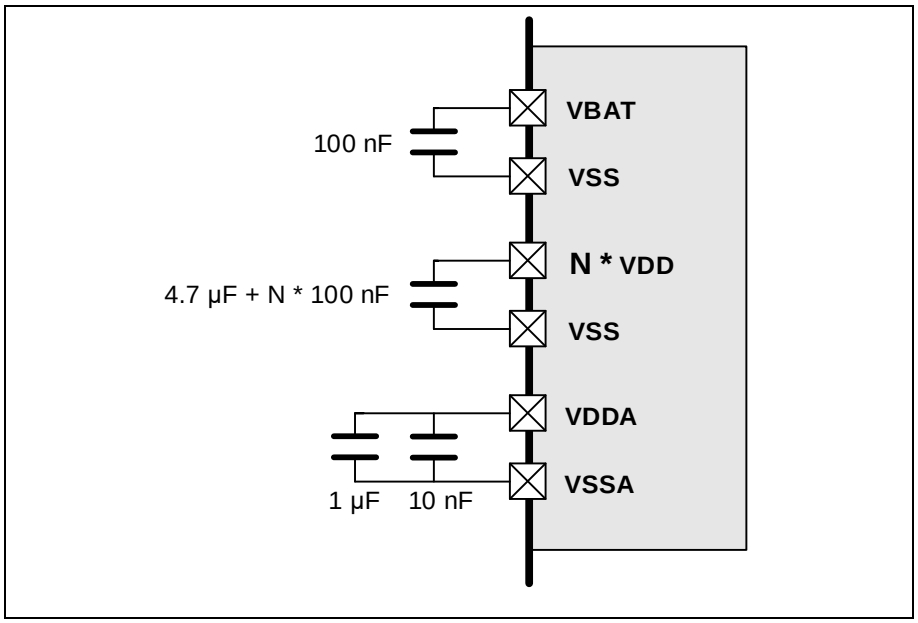
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V_{DD}	Supply voltage	—	2.6	3.3	3.6	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	2.6	3.3	3.6	V
V_{BAT}	Battery supply voltage	—	1.8(2)	—	3.6	V

(1) Based on characterization, not tested in production.

(2) In the application which V_{BAT} supply the backup domains, if the V_{BAT} voltage drops below the minimum value, when V_{DD} is powered on again, it is necessary to refresh the registers of backup domains and enable LXTAL again.

Figure 4-1. Recommended power supply decoupling capacitors(1)



(1) All decoupling capacitors need to be as close as possible to the pins on the PCB board. More details refer to ***AN057 GD32F3x0 Hardware Development Guide***.

Table 4-3. Clock frequency(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK1}	AHB1 clock frequency	—	0	72	MHz
f_{HCLK2}	AHB2 clock frequency	—	0	72	MHz
f_{APB1}	APB1 clock frequency	—	0	36	MHz
f_{APB2}	APB2 clock frequency	—	0	36	MHz

(1) Guaranteed by design, not tested in production.

Table 4-4. Operating conditions at Power up/ Power down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	—	0	∞	µs /V
	V_{DD} fall time rate		20	∞	

(1) Guaranteed by design, not tested in production.

Table 4-5. Start-up timings of Operating conditions(1)(2)(3)

Symbol	Parameter	Conditions	Typ	Unit
$t_{start-up}$	Start-up time	Clock source from HXTAL	33.2	ms
		Clock source from IRC8M	31.8	

(1) Based on characterization, not tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the main function.

(3) PLL is off.

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Table 4-6. Power saving mode wakeup timings characteristics(1)(2)

Symbol	Parameter	Typ	Unit
t_{Sleep}	Wakeup from Sleep mode	2.8	μs
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode（LDO On）	3.6	
	Wakeup from Deep-sleep mode（LDO in low power mode）	3.6	
$t_{Standby}$	Wakeup from Standby mode	31.6	ms

(1) Based on characterization, not tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 3.3 V, IRC8M = System clock = 8 MHz.

4.3 Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-7.Power consumption characteristics(2)(3)(3)(4)(5)(6)

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
I_{DD} + I_{DDA}	Supply current (Run mode)	V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 72 MHz, All peripherals enabled	—	14.64	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 72 MHz, All peripherals disabled	—	10.91	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 48 MHz, All peripherals enabled	—	10.29	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 48 MHz, All peripherals disabled	—	7.80	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 36 MHz, All peripherals enabled	—	8.10	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 36 MHz, All peripherals disabled	—	6.23	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 24 MHz, All peripherals enabled	—	5.91	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 24 MHz, All peripherals disabled	—	4.67	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 16 MHz, All peripherals enabled	—	4.45	—	mA

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Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 16 MHz, All peripherals disabled	—	3.62	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 8 MHz, All peripherals enabled	—	3.01	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 8 MHz, All peripherals disabled	—	2.51	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 4 MHz, System clock = 4 MHz, All peripherals enabled	—	1.11	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 4 MHz, System clock = 4 MHz, All peripherals disabled	—	0.86	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 2 MHz, System clock = 2 MHz, All peripherals enabled	—	0.7	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 2 MHz, System clock = 2 MHz, All peripherals disabled	—	0.58	—	mA
	Supply current (Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 72 MHz, All peripherals enabled	—	9.03	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 72 MHz, All peripherals disabled	—	4.77	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 48 MHz, All peripherals enabled	—	6.53	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 48 MHz, All peripherals disabled	—	3.69	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 36 MHz, All peripherals enabled	—	5.27	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 36 MHz, All peripherals disabled	—	3.14	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 24 MHz, All peripherals enabled	—	4.01	—	mA

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Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 24 MHz, All peripherals disabled	—	2.60	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 16 MHz, All peripherals enabled	—	3.18	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 16 MHz, All peripherals disabled	—	2.23	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 8 MHz, All peripherals enabled	—	2.38	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, CPU clock off, System clock = 8 MHz, All peripherals disabled	—	1.82	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 4 MHz, CPU clock off, System clock = 4 MHz, All peripherals enabled	—	0.77	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 4 MHz, CPU clock off, System clock = 4 MHz, All peripherals disabled	—	0.49	—	mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 2 MHz, CPU clock off, System clock = 2 MHz, All peripherals enabled	—	0.52	—	mA
		VDD = VDDA = 3.3 V, HXTAL = 2 MHz, CPU clock off, System clock =2 MHz, All peripherals disabled	—	0.38	—	mA
	Supply current (Deep-sleep mode)	V_{DD} = V_{DDA} = 3.3 V, LDO in normal power and normal driver mode, IRC40K off, RTC off	—	172.26	330.00	µA
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power and normal driver mode, IRC40K off, RTC off	—	120.37	278.11(1)	µA
		V_{DD} = V_{DDA} = 3.3 V, LDO in normal power and low driver mode, IRC40K off, RTC off	—	146.29	304.03(1)	µA
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power and low driver mode, IRC40K off, RTC off	—	94.66	252.40(1)	µA
	Supply current (Standby mode)	V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC on	—	6.96	13.16(1)	µA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC off	—	6.63	12.83(1)	µA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K off, RTC off, VDDA Monitor on	—	5.90	12.10	µA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K off, RTC off, V_{DDA} Monitor off	—	3.69	9.89(1)	µA

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Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
I_{BAT}	Battery supply current	V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL High driving	—	2.32	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL High driving	—	2.10	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.6 V, LXTAL on with external crystal, RTC on, LXTAL High driving	—	1.85	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving	—	1.90	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving	—	1.68	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving	—	1.44	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving	—	1.47	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving	—	1.24	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving	—	1.01	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL Low driving	—	1.32	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Low driving	—	1.12	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.6 V, LXTAL on with external crystal, RTC on, LXTAL Low driving	—	0.88	—	μA

(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all values given for T_A = 25 ℃ and test result is mean value.

(3) When System Clock is less than 4 MHz, an external source is used, and the HXTAL bypass function is needed, no PLL.

(4) When System Clock is greater than 8 MHz, a crystal 8 MHz is used, and the HXTAL bypass function is closed, using PLL.

(5) When analog peripheral blocks such as ADCs, HXTAL, LXTAL, IRC8M, or IRC40K are ON, an additional power consumption should be considered.

(6) All GPIOs are configured as analog mode except standby mode.

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Figure 4-2. Typical supply current consumption in Run mode

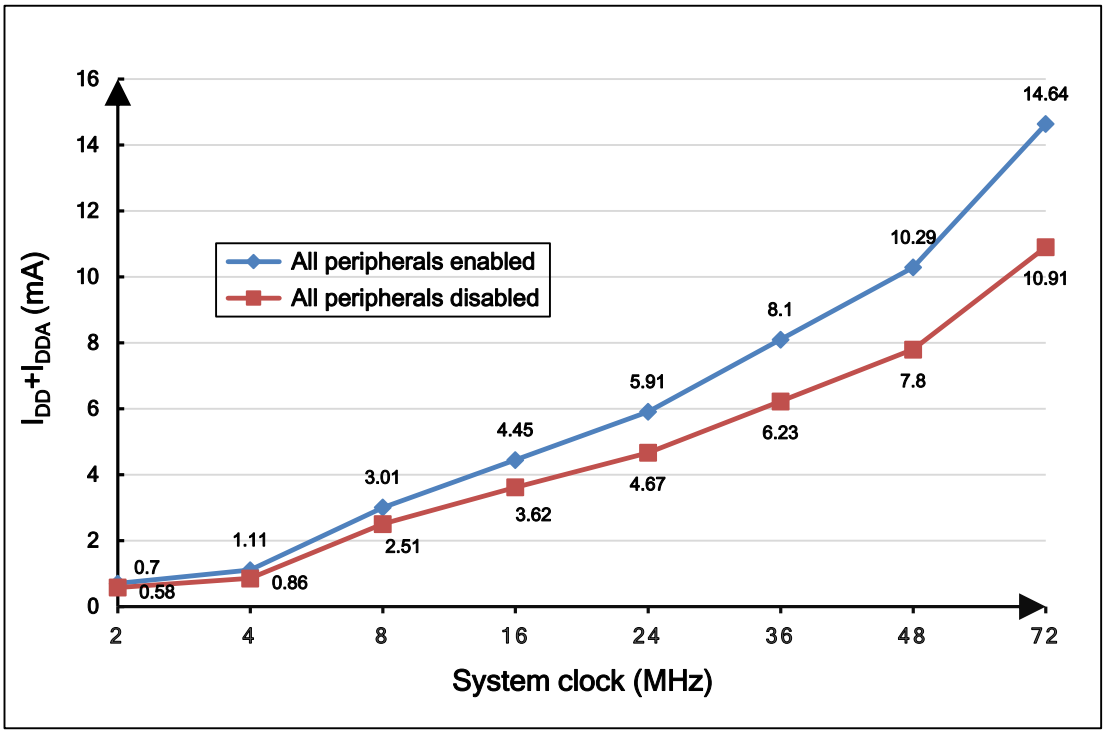


Figure 4-3. Typical supply current consumption in Sleep mode

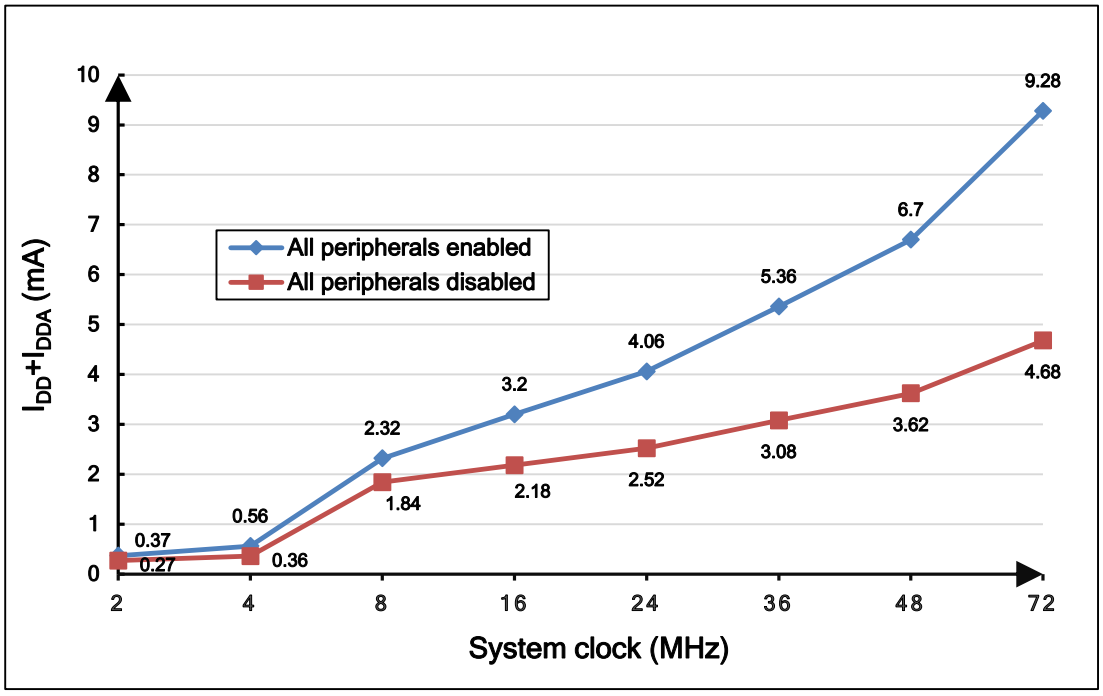


Table 4-8. Peripheral current consumption characteristics(1)

Peripherials(3)		Typical consumption(1)	Unit
AHB1	CRC	0.10	mA
	DMA	0.32	
AHB2	GPIOF	0.11	

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Peripherials(3)		Typical consumption(1)	Unit
	GPIOD	0.10	
	GPIOC	0.13	
	GPIOB	0.13	
	GPIOA	0.13	
APB2	TIMER16	0.24	
	TIMER15	0.24	
	TIMER14	0.31	
	USART0	0.41	
	TIMER0	0.50	
	SPI0	0.19	
	ADC(2)	0.91	
APB1	PMU	0.31	
	I2C1	0.17	
	I2C0	0.17	
	USART1	0.15	
	SPI1	0.12	
	WWDGT	0.11	
	TIMER13	0.15	
	TIMER2	0.29	
	I2S0	0.17	

(1) Based on characterization, not tested in production.

(2) System clock = f_{HCLK} = 72 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/2$, ADCON bit is set to 1.

(3) If there is no other description, then HXTAL = 8 MHz, System clock = f_{HCLK} = 72 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$.

4.4 EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in ***Table 4-9. EMS characteristics(1)***, based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 4-9. EMS characteristics(1)

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25 °C, LQFP48, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	3A
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on VDD and VSS pins	V_{DD} = 3.3 V, T_A = 25 °C, LQFP48, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	3A

(1) Based on characterization, not tested in production.

EMI (Electromagnetic Interference) emission test result is given in the ***Table 4-10. EMI***

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characteristics[1], The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

Table 4-10. EMI characteristics[1]

Symbol	Parameter	Conditions	Tested frequency band	Max vs. [f_{HXTAL}/f_{HCLK}]	Unit
				8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +25 °C, LQFP48, f_{HCLK} = 72 MHz, conforms to SAE J1752-3:2017	0.15 to 30 MHz	-1.19	dBµV
			30 to 130 MHz	3.08	
			130 MHz to 1GHz	8.82	

(1) Based on characterization, not tested in production.

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4.5 Power supply supervisor characteristics

Table 4-11. Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LVD}(1)	Low Voltage Detector Threshold	LVDT[2:0] = 000, rising edge	—	2.15	—	V
		LVDT[2:0] = 000, falling edge	—	2.04	—	V
		LVDT[2:0] = 001, rising edge	—	2.30	—	V
		LVDT[2:0] = 001, falling edge	—	2.20	—	V
		LVDT[2:0] = 010, rising edge	—	2.44	—	V
		LVDT[2:0] = 010, falling edge	—	2.34	—	V
		LVDT[2:0] = 011, rising edge	—	2.57	—	V
		LVDT[2:0] = 011, falling edge	—	2.46	—	V
		LVDT[2:0] = 100, rising edge	—	2.72	—	V
		LVDT[2:0] = 100, falling edge	—	2.61	—	V
		LVDT[2:0] = 101, rising edge	—	2.86	—	V
		LVDT[2:0] = 101, falling edge	—	2.74	—	V
		LVDT[2:0] = 110, rising edge	—	3.00	—	V
		LVDT[2:0] = 110, falling edge	—	2.88	—	V
		LVDT[2:0] = 111, rising edge	—	3.14	—	V
		LVDT[2:0] = 111, falling edge	—	3.03	—	V
$V_{LVDhyst}$(2)	LVD hysteresis	—	—	100	—	mV
V_{POR}(1)	Power on reset threshold	—	—	2.38	—	V
V_{PDR}(1)	Power down reset threshold		—	1.84	—	V
$V_{PDRhyst}$(2)	PDR hysteresis		—	600	—	mV
$t_{RSTTEMPO}$(2)	Reset temporization		—	2	—	ms

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.6 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up

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(LU) test is based on the two measurement methods.

Table 4-12. ESD characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C; JS-001-2017	—	—	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C; JS-002-2018	—	—	500	V

(1) Based on characterization, not tested in production.

Table 4-13. Static latch-up characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A = 25 °C; JESD78D	—	—	±200	mA
	V_{supply} over voltage		—	—	5.4	V

(1) Based on characterization, not tested in production.

4.7 External clock characteristics

Table 4-14. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}(1)	Crystal or ceramic frequency	2.6 V ≤ V_{DD} ≤ 3.6 V	4	8	32	MHz
R_F(2)	Feedback resistor	V_{DD} = 3.3 V	—	400	—	kΩ
C_{HXTAL}(2)(3)	Recommended matching capacitance on OSCIN and OSCOUT	—	—	20	30	pF
$Ducy_{(HXTAL)}$(2)	Crystal or ceramic duty cycle	—	30	50	70	%
g_m(2)	Oscillator transconductance	Startup	—	25	—	mA/V
$I_{DD(HXTAL)}$(1)	Crystal or ceramic operating current	V_{DD} = 3.3 V, f_{HCLK} = f_{IRC8M} = 8 MHz T_A = 25 °C	—	1.1	—	mA
$t_{SUHXTAL}$(1)	Crystal or ceramic startup time	V_{DD} = 3.3 V, f_{HCLK} = f_{IRC8M} = 8 MHz T_A = 25 °C	—	1.4	—	ms

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S), For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

Table 4-15. High speed external user clock characteristics (HXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}(1)	External clock source or oscillator frequency	V_{DD} = 3.3 V	1	8	50	MHz

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{HXTALH}(2)	OSCIN input pin high level voltage	V_{DD} = 3.3 V	0.7 V_{DD}	—	V_{DD}	V
V_{HXTALL}(2)	OSCIN input pin low level voltage		V_{SS}	—	0.3 V_{DD}	
$t_{H/L(HXTAL)}$(2)	OSCIN high or low time	—	5	—	—	ns
$t_{R/F(HXTAL)}$(2)	OSCIN rise or fall time	—	—	—	10	
C_{IN}(2)	OSCIN input capacitance	—	—	5	—	pF
$Ducy_{(HXTAL)}$ (2)	Duty cycle	—	30	50	70	%

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-16. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}(1)	Crystal or ceramic frequency	—	—	32.768	—	kHz
C_{LXTAL}(2)(3)	Recommended matching capacitance on OSC32IN and OSC32OUT	—	—	15	—	pF
$Ducy_{(LXTAL)}$(2)	Crystal or ceramic duty cycle	—	30	—	70	%
g_m(2)	Oscillator transconductance	Lower driving capability	—	4	—	μA/V
		Medium low driving capability	—	6	—	
		Medium high driving capability	—	12	—	
		Higher driving capability	—	18	—	
$I_{DDLXTAL}$ (1)	Crystal or ceramic operating current	Lower driving capability	—	0.8	—	μA
		Medium low driving capability	—	0.9	—	
		Medium high driving capability	—	1.3	—	
		Higher driving capability	—	1.8	—	
$t_{SULXTAL}$(1)(4)	Crystal or ceramic startup time	—	—	0.8	—	s

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For CS, it is PCB and MCU pin stray capacitance.

(4) $t_{SULXTAL}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

Table 4-17. Low speed external user clock characteristics (LXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL_ext}(1)	External clock source or oscillator	V_{DD} = 3.3 V	—	32.768	1000	kHz

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	frequency					
V_{LXTALH}(2)	OSC32IN input pin high level voltage	—	0.7 V_{DD}	—	V_{DD}	V
V_{LXTALL}(2)	OSC32IN input pin low level voltage	—	V_{SS}	—	0.3 V_{DD}	
$t_{H/L(LXTAL)}$ (2)	OSC32IN high or low time	—	450	—	—	ns
$t_{R/F(LXTAL)}$ (2)	OSC32IN rise or fall time	—	—	—	50	
C_{IN}(2)	OSC32IN input capacitance	—	—	5	—	pF
$Ducy_{(LXTAL)}$ (2)	Duty cycle	—	30	50	70	%

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

4.8 Internal clock characteristics

Table 4-18. High speed internal clock (IRC8M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC8M}	High Speed Internal Oscillator (IRC8M) frequency	V_{DD} = V_{DDA} = 3.3 V	—	8	—	MHz
ACC_{IRC8M}	IRC8M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +85 °C for grade 6 devices	—	-0.62 to 0.46(1)	—	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C for grade 7 devices	—	-0.7 to 0.46(1)	—	
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-1.0	—	+1.0	
	IRC8M oscillator Frequency accuracy, User trimming step(1)	—	—	0.5	—	%
$Ducy_{IRC8M}$(2)	IRC8M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDAIRC8M}$(1)	IRC8M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V	—	58	—	μA
$t_{SUIRC8M}$(1)	IRC8M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V	—	1.2	—	μs

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

Table 4-19. Low speed internal clock (IRC40K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC40K}(1)	Low Speed Internal oscillator (IRC40K) frequency	V_{DD} = V_{DDA} = 3.3 V	—	40	—	kHz

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DDAIRC40K}$(2)	IRC40K oscillator operating current	V_{DD} = V_{DDA} = 3.3 V	—	0.5	—	μA
$t_{SUIRC40K}$(2)	IRC40K oscillator startup time	V_{DD} = V_{DDA} = 3.3 V	—	75	—	μs

(1) Guaranteed by design, not tested in production.
(2) Based on characterization, not tested in production.

Table 4-20. High speed internal clock (IRC28M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC28M}	High Speed Internal Oscillator (IRC28M) frequency	V_{DD} = V_{DDA} = 3.3 V	—	28	—	MHz
ACC_{IRC28M}	IRC28M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +85 °C for grade 6 devices	—	-0.86 to 0.9(1)	—	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C for grade 7 devices	—	-1.02 to 0.9(1)	—	
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-1.0	—	+1.0	
	IRC28M oscillator Frequency accuracy, User trimming step(1)	—	—	0.5	—	%
D_{IRC28M}(2)	IRC28M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDAIRC28M}$(1)	IRC28M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V	—	114	—	μA
$t_{SUIRC28M}$(1)	IRC28M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V	—	1.6	—	μs

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

Table 4-21. High speed internal clock (IRC48M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	V_{DD} = V_{DDA} = 3.3 V	—	48	—	MHz
ACC_{IRC48M}	IRC48M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +85 °C for grade 6 devices	—	-0.81 to 0.35(1)	—	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C for grade 7 devices	—	-0.86 to 0.35(1)	—	
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-2.0	—	+2.0	
	IRC48M oscillator Frequency accuracy, User trimming step(1)	—	—	0.12	—	%

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
D_{IRC48M}(2)	IRC48M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDAIRC48M}$(1)	IRC48M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V	—	238	—	μA
$t_{SUIRC48M}$(1)	IRC48M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V	—	1.3	—	μs

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

4.9 PLL characteristics

Table 4-22. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	1	—	25	MHz
f_{PLLOUT}(2)	PLL output clock frequency	—	16	—	72	MHz
f_{VCO}(2)	PLL VCO output clock frequency	—	—	—	72	MHz
t_{LOCK}(2)	PLL lock time	—	—	—	300	μs
I_{DDA}(1) (3)	Current consumption on V_{DDA}	VCO freq = 72 MHz	—	210	—	μA
$Jitter_{PLL}$(4)	Cycle to cycle Jitter（rms）	System clock	—	32.1	—	ps
	Cycle to cycle Jitter（peak to peak）		—	255.6	—	

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) System clock = IRC8M = 8 MHz, f_{PLLOUT} = 72 MHz.
(4) Value given with main PLL running.

4.10 Memory characteristics

Table 4-23 Flash memory characteristics(1)

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(1)	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	—	100	—	—	kcycles
t_{READ}	Read time at code flash area	—	—	1	—	hclks
	Read time at data flash area		56	—	3536	
t_{RET}	Data retention time	—	—	20	—	years
t_{PROG}	Word programming time	T_A range(2)	—	37.5	86	μs
t_{ERASE}	Page erase time		—	45	300	ms
$t_{MERASE(64KB)}$	Mass erase time		—	0.5	1.6	s

(1) Guaranteed by design and/or characterization, not 100% tested in production.

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(2) For grade 6 devices, T_A range= -40°C ~ +85°C. For grade 7 devices, T_A range= -40°C ~ +105°C.

4.11 NRST pin characteristics

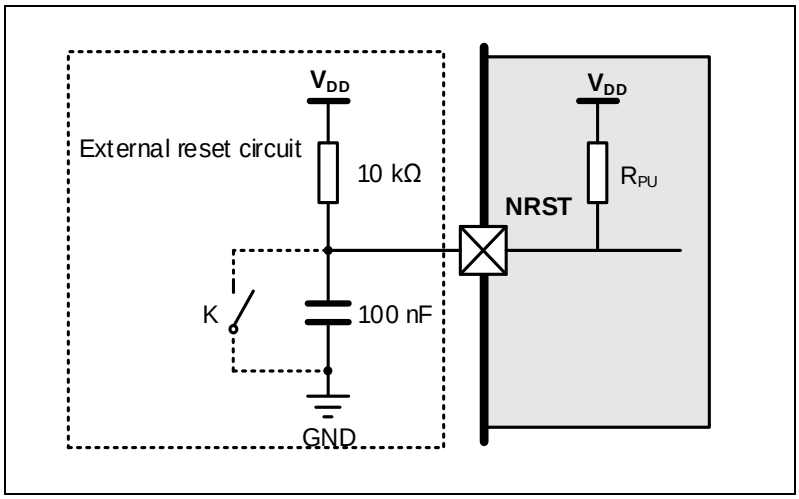
Table 4-24. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	2.6 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	-0.5	—	0.3 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.5	
V_{hyst}(2)	Schmidt trigger Voltage hysteresis		—	360	—	mV
R_{pu}(2)	Pull-up equivalent resistor	—	—	40	—	kΩ

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Figure 4-4. Recommended external NRST pin circuit(1)



(1) Unless the voltage on NRST pin go below $V_{IL(NRST)}$ level, the device would not generate a reliable reset.

4.12 GPIO characteristics

Table 4-25. I/O port DC characteristics(1)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage	2.6 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	—	—	0.3 V_{DD}	V
	5V-tolerant IO Low level input voltage	2.6 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	—	—	0.3 V_{DD}	V
V_{IH}	Standard IO High level input voltage	2.6 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	0.7 V_{DD}	—	—	V
	5V-tolerant IO High level input voltage	2.6 V ≤ V_{DD} = V_{DDA} ≤ 3.6 V	0.7 V_{DD}	—	—	V
V_{OL}	Low level output voltage for 8 IO Pins (each I_{IO} = +8 mA)	V_{DD} = 2.6 V	—	0.14	—	V
		V_{DD} = 3.3 V	—	0.13	—	
		V_{DD} = 3.6 V	—	0.12	—	

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Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{OL}	Low level output voltage for 8 IO Pins (each I_{IO} = +20 mA)		V_{DD} = 2.6 V	—	0.36	—	V
			V_{DD} = 3.3 V	—	0.32	—	
			V_{DD} = 3.6 V	—	0.31	—	
V_{OH}	High level output voltage for 8 IO Pins (each I_{IO} = +8 mA)		V_{DD} = 2.6 V	—	2.42	—	V
			V_{DD} = 3.3 V	—	3.16	—	
			V_{DD} = 3.6 V	—	3.47	—	
V_{OH}	High level output voltage for 8 IO Pins (each I_{IO} = +20 mA)		V_{DD} = 2.6 V	—	2.15	—	V
			V_{DD} = 3.3 V	—	2.92	—	
			V_{DD} = 3.6 V	—	3.24	—	
R_{PU}(2)	Internal pull-up resistor	All pins	V_{IN} = V_{SS}	30	40	50	kΩ
		PA10	—	7.5	10	13.5	kΩ
R_{PD}(2)	Internal pull-down resistor	All pins	V_{IN} = V_{DD}	30	40	50	kΩ
		PA10	—	7.5	10	13.5	kΩ

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current(typical source capability:3 mA shared between these IOs, but sink capability is same as other IO), the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode(maximum load: 30 pF).

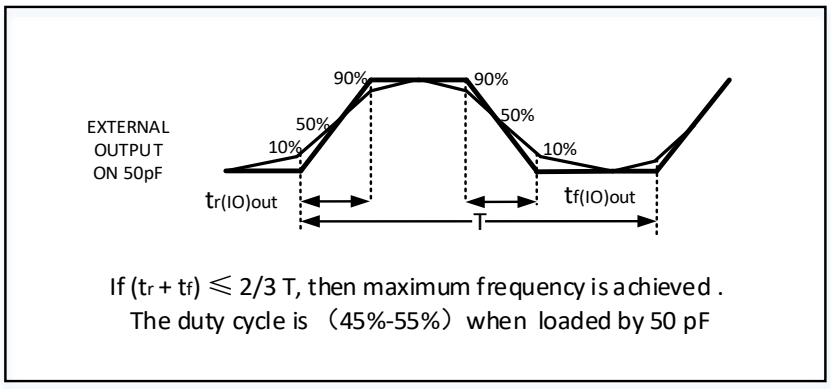
Table 4-26. I/O port AC characteristics(1)(2)

GPIOx_OSPD[1:0] bit value(3)	Parameter	Conditions	Typ	Unit
GPIOx_OSPD0->OSPDy[1:0] = X0 （IO_Speed = 2 MHz）	T_{Rise}/T_{Fall}	2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	36.82	ns
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	43.91	
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	49.92	
GPIOx_OSPD0->OSPDy[1:0] = 01 （IO_Speed = 10 MHz）	T_{Rise}/T_{Fall}	2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	9.27	ns
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF	10.46	
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	11.72	
GPIOx_OSPD0->OSPDy[1:0] = 11 （IO_Speed = 50 MHz）	T_{Rise}/T_{Fall}	2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	1.66	ns
		2.6 ≤ V_{DD} ≤ 3.6V, C_L = 30 pF	2.43	
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	3.2	
GPIOx_OSPD0->OSPDy[1:0] = 11 and GPIOx_OSPD1->SPDy = 1 （IO_Speed mode = MAX）	T_{Rise}/T_{Fall}	2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 10 pF	1.36	ns
		2.6 ≤ V_{DD} ≤ 3.6V, C_L = 30 pF	2.11	
		2.6 ≤ V_{DD} ≤ 3.6 V, C_L = 50 pF	2.8	

(1) Based on characterization, not tested in production.
(2) Unless otherwise specified, all test results given for T_A = 25 ℃.
(3) The I/O speed is configured using the GPIOx_OSPD0->OSPDy [1:0] bits. Refer to the GD32F3x0 user manual which is selected to set the GPIO port output speed.
(4) The maximum frequency is defined in ***Figure 4-5. I/O port AC characteristics definition***, and maximum frequency cannot exceed 72 MHz.

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Figure 4-5. I/O port AC characteristics definition



4.13 ADC characteristics

Table 4-27. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—	2.6	3.3	3.6	V
V_{IN}(1)	ADC input voltage range	—	0	—	V_{DDA}	V
f_{ADC}(1)	ADC clock	—	0.1	—	36	MHz
f_S(1)	Sampling rate	12-bit	0.007	—	2.57	MSPS
		10-bit	0.008	—	3.00	
		8-bit	0.01	—	3.60	
		6-bit	0.011	—	4.50	
V_{AIN}(1)	Analog input voltage	10 external; 3 internal	0	—	V_{DDA}	V
R_{AIN}(2)	External input impedance	See ***Equation 1***	—	—	171	kΩ
R_{ADC}(2)	Input sampling switch resistance	—	—	—	0.2	kΩ
C_{ADC}(2)	Input sampling capacitance	No pin/pad capacitance included	—	—	4	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 40 MHz	—	3.63	—	μs
t_s(2)	Sampling time	f_{ADC} = 40 MHz	0.04	—	6.65	μs
t_{CONV}(2)	Total conversion time(including sampling time)	12-bit	—	14	—	1/ f_{ADC}
		10-bit	—	12	—	
		8-bit	—	10	—	
		6-bit	—	8	—	
t_{SU}(2)	Startup time	—	—	—	1	μs

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Equation 1 ： R_{AIN} max formula $R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above (***Equation 1***) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

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Table 4-28. ADC R_{AIN} max for f_{ADC} = 36 MHz(1)

T_s(cycles)	t_s(μs)	R_{AINmax} (kΩ)
1.5	0.04	0.8
7.5	0.20	5.1
13.5	0.37	9.4
28.5	0.79	20.1
41.5	1.15	29.4
55.5	1.54	39.5
71.5	1.98	50.9
239.5	6.65	171

(1) Based on characterization, not tested in production.

Table 4-29. ADC dynamic accuracy at f_{ADC} = 14 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 14 MHz	—	10.9	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA} = V_{DD} = 3.3 V	—	67.3	—	dB
SNR	Signal-to-noise ratio	Input Frequency = 20 kHz	—	67.6	—	
THD	Total harmonic distortion	Temperature = 25℃	—	-79	—	

(1) Based on characterization, not tested in production.

Table 4-30. ADC dynamic accuracy at f_{ADC} = 28 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 28 MHz	—	10.8	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA} = V_{DD} = 3.3 V	—	66.7	—	dB
SNR	Signal-to-noise ratio	Input Frequency = 20 kHz	—	67.0	—	
THD	Total harmonic distortion	Temperature = 25 ℃	—	-78	—	

(1) Based on characterization, not tested in production.

Table 4-31.ADC dynamic accuracy at f_{ADC} = 36 MHz(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 36 MHz	—	10.8	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA} = V_{DD} = 3.3 V	—	66.7	—	dB
SNR	Signal-to-noise ratio	Input Frequency = 20 kHz	—	67.0	—	
THD	Total harmonic distortion	Temperature = 25℃	—	-78	—	

(1) Based on characterization, not tested in production.

Table 4-32. ADC static accuracy at f_{ADC} = 14 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max	Unit
Offset	Offset error	f_{ADC} = 14 MHz V_{DDA} = V_{DD} = 3.3 V	±1	—	LSB
DNL	Differential linearity error		±1	—	
INL	Integral linearity error		±1.5	—	

(1) Based on characterization, not tested in production.

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4.14 Temperature sensor characteristics

Table 4-33. Temperature sensor characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	—	±1.5	—	℃
Avg_Slope	Average slope	—	4.3	—	mV/℃
V_{25}	Voltage at 25 °C	—	1.45	—	V
t_{S_temp} (2)	ADC sampling time when reading the temperature	—	17.1	—	μs

(1) Based on characterization, not tested in production.

(2) Shortest sampling time can be determined in the application by multiple iterations.

4.15 I2C characteristics

Table 4-34. I2C characteristics(1)(2)(3)

Symbol	Parameter	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	μs
$t_{SU(SDA)}$	SDA setup time	—	250	—	100	—	50	—	ns
$t_{H(SDA)}$	SDA data hold time	—	0(3)	3450	0	900	0	450	ns
$t_{R(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	—	300	—	120	ns
$t_{F(SDA/SCL)}$	SDA and SCL fall time	—	—	300	—	300	—	120	ns
$t_{H(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	μs
$t_{SU(STA)}$	Repeated Start condition setup time	—	4.7	—	0.6	—	0.26	—	μs
$t_{SU(STO)}$	Stop condition setup time	—	4.0	—	0.6	—	0.26	—	μs
t_{BUFF}	Stop to Start condition time (bus free)	—	4.7	—	1.3	—	0.5	—	μs

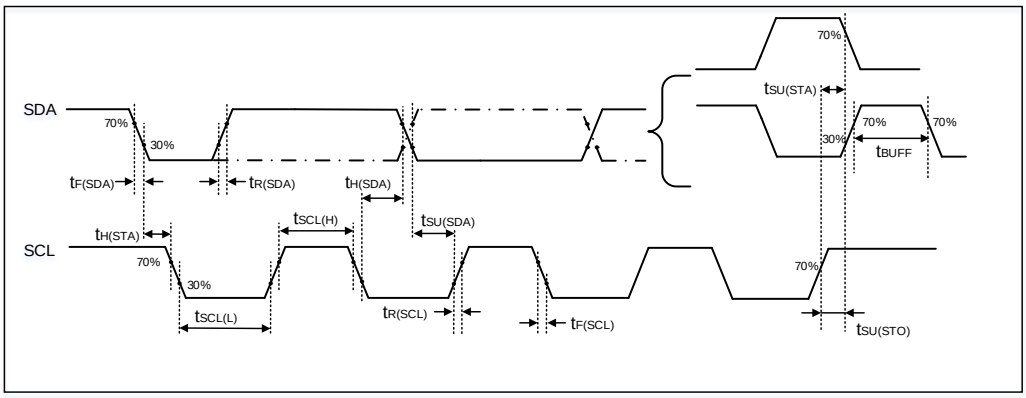
(1) Guaranteed by design, not tested in production.

(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

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(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

Figure 4-6. I2C bus timing diagram



4.16 SPI characteristics

Table 4-35. Standard SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}(1)	SCK clock frequency	—	—	—	18	MHz
$t_{SCK(H)}$ (1)	SCK clock high time	Master mode, f_{PCLKx} = 72 MHz	25.78	27.78	29.78	ns
$t_{SCK(L)}$ (1)	SCK clock low time	Master mode, f_{PCLKx} = 72 MHz	25.78	27.78	29.78	ns
SPI master mode						
$t_{V(MO)}$(2)	Data output valid time	—	—	6.67	—	ns
$t_{H(MO)}$(2)	Data output hold time	—	—	5.67	—	ns
$t_{SU(MI)}$(1)	Data input setup time	—	1	—	—	ns
$t_{H(MI)}$ (1)	Data input hold time	—	0	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$(1)	NSS enable setup time	—	0	—	—	ns
$t_{H(NSS)}$(1)	NSS enable hold time	—	1	—	—	ns
$t_{A(SO)}$(2)	Data output access time	—	—	10.8	—	ns
$t_{DIS(SO)}$(2)	Data output disable time	—	—	15.5	—	ns
$t_{V(SO)}$(2)	Data output valid time	—	—	13.5	—	ns
$t_{H(SO)}$(2)	Data output hold time	—	—	11.1	—	ns
$t_{SU(SI)}$ (1)	Data input setup time	—	0	—	—	ns
$t_{H(SI)}$ (1)	Data input hold time	—	3	—	—	ns

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production.

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Figure 4-7. SPI timing diagram - master mode

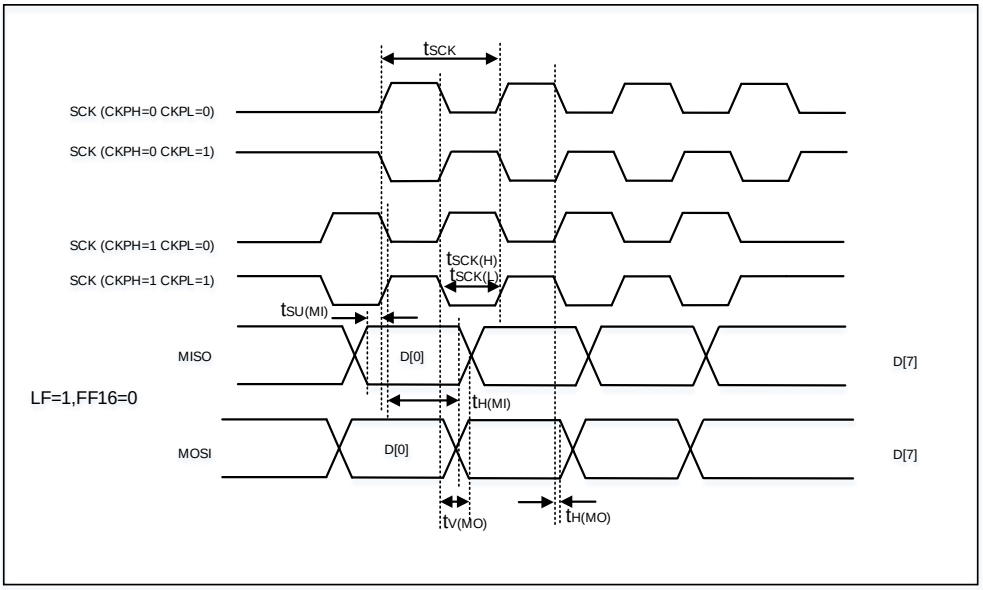
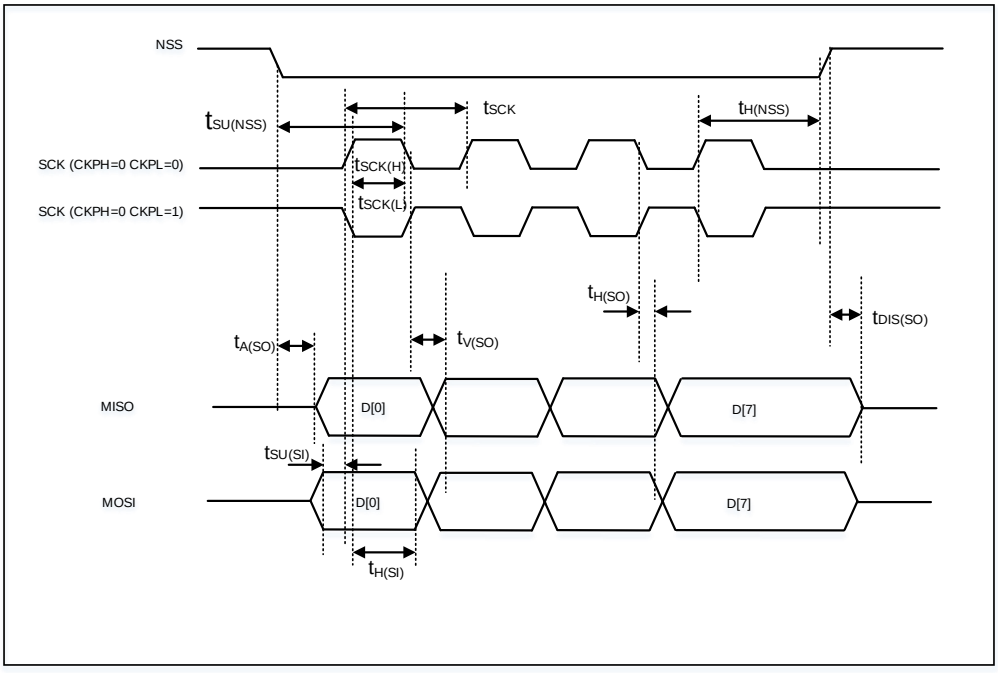


Figure 4-8. SPI timing diagram - slave mode



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4.17 I2S characteristics

Table 4-36. I2S characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}(1)	Clock frequency	Master mode (data: 16 bits, Audio frequency = 96 kHz)	3.084	3.086	3.088	MHz
		Slave mode	0	—	10	
t_H(1)	Clock high time	—	162	—	—	ns
t_L(1)	Clock low time		162	—	—	ns
$t_{V(WS)}$(2)	WS valid time	Master mode	—	1.88	—	ns
$t_{H(WS)}$(2)	WS hold time	Master mode	—	2.5	—	ns
$t_{SU(WS)}$(1)	WS setup time	Slave mode	0	—	—	ns
$t_{H(WS)}$(1)	WS hold time	Slave mode	2	—	—	ns
$Ducy_{(sck)}$(1)	I2S slave input clock duty cycle	Slave mode	—	50	—	%
$t_{SU(SD_MR)}$(1)	Data input setup time	Master mode	2	—	—	ns
$t_{SU(SD_SR)}$(1)	Data input setup time	Slave mode	0	—	—	ns
$t_{H(SD_MR)}$(1)	Data input hold time	Master receiver	0	—	—	ns
$t_{H(SD_SR)}$(1)		Slave receiver	1	—	—	ns
$t_{V\ (SD_ST)}$(2)	Data output valid time	Slave transmitter (after enable edge)	—	13.5	—	ns
$t_{H\ (SD_ST)}$(2)	Data output hold time	Slave transmitter (after enable edge)	—	13.8	—	ns
$T_{V(SD_MT)}$(2)	Data output valid time	Master transmitter (after enable edge)	—	7.55	—	ns
$t_{H(SD_MT)}$(2)	Data output hold time	Master transmitter (after enable edge)	—	8.33	—	ns

(1) Guaranteed by design, not tested in production

(2) Based on characterization, not tested in production.

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Figure 4-9. I2S timing diagram - master mode

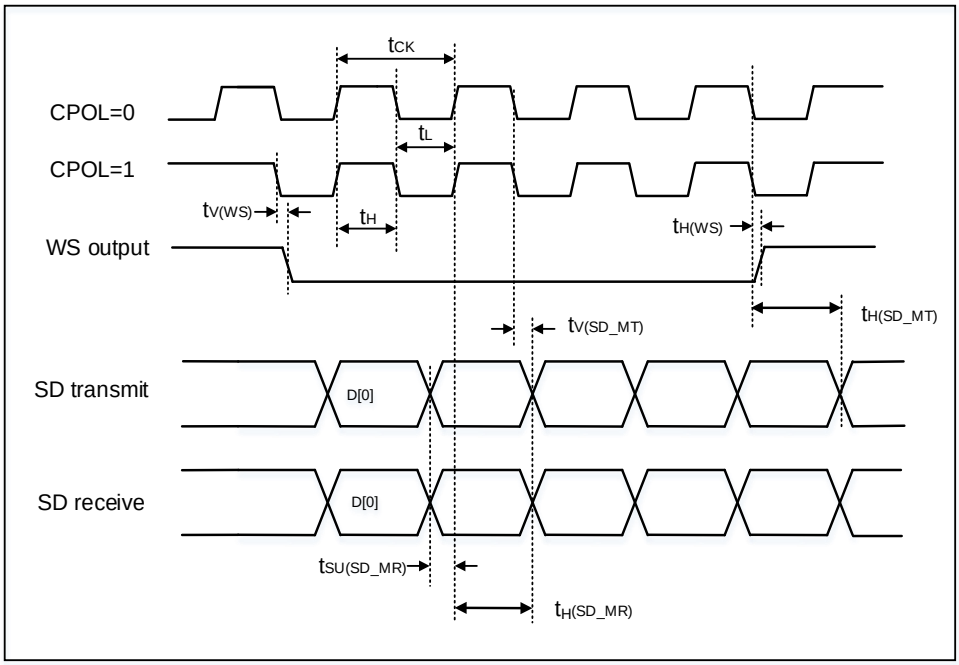
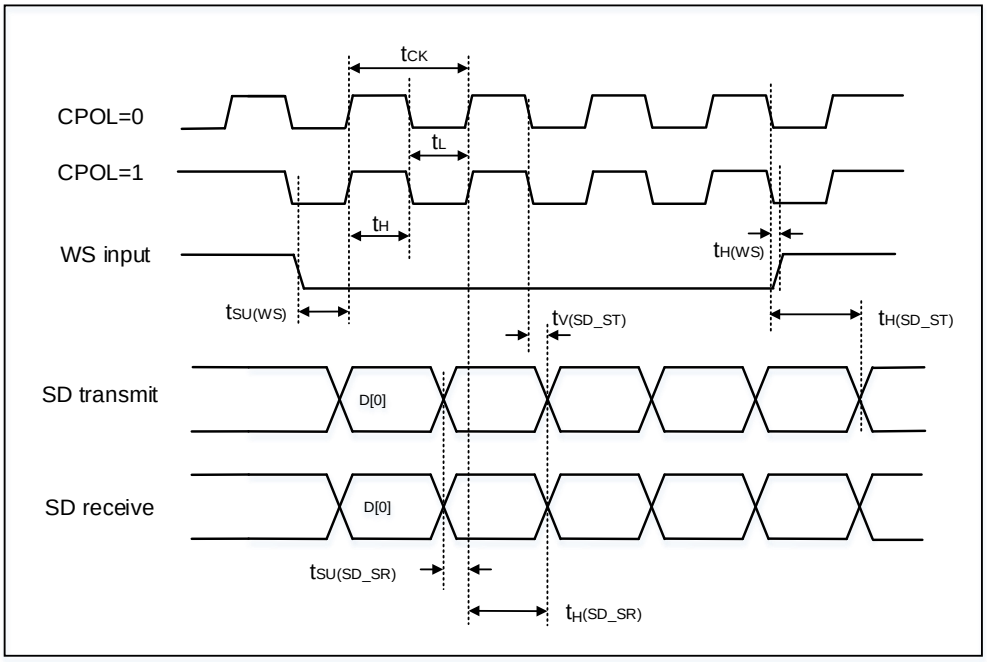


Figure 4-10. I2S timing diagram - slave mode



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4.18 USART characteristics

Table 4-37. USART characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLKx} = 72 MHz	—	—	36	MHz
$t_{SCK(H)}$	SCK clock high time	f_{PCLKx} = 72 MHz	13.8	—	—	ns
$t_{SCK(L)}$	SCK clock low time	f_{PCLKx} = 72 MHz	13.8	—	—	ns

(1) Guaranteed by design, not tested in production.

4.19 TIMER characteristics

Table 4-38. TIMER characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 72 MHz	13.9	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}$/2	MHz
		$f_{TIMERxCLK}$ = 72 MHz	0	36	MHz
RES	Timer resolution	—	—	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 72 MHz	0.0139	910	μs
t_{MAX_COUNT}	Maximum possible count	—	—	65536 × 65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 72 MHz	—	59.6	s

(1) Guaranteed by design, not tested in production.

4.20 WDGT characteristics

Table 4-39. FWDGT min/max timeout period at 40 kHz (IRC40K)(1)

Prescaler divider	PSC[2:0] bits	Min timeout RLD[11:0] = 0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/4	000	0.025	409.525	ms
1/8	001	0.025	819.025	
1/16	010	0.025	1638.025	
1/32	011	0.025	3276.025	
1/64	100	0.025	6552.025	
1/128	101	0.025	13104.025	
1/256	110 or 111	0.025	26208.025	

(1) Guaranteed by design, not tested in production.

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Table 4-40. WWDGT min-max timeout value at 36 MHz (f_{PCLK1})(1)

Prescaler divider	PSC[1:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00	113.78	μs	7.28	ms
1/2	01	227.56		14.56	
1/4	10	455.11		29.13	
1/8	11	910.22		58.25	

(1) Guaranteed by design, not tested in production.

4.21 Parameter conditions

Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_A = 25 ℃.

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5 Package information

5.1 LQFP48 package outline dimensions

Figure 5-1. LQFP48 package outline

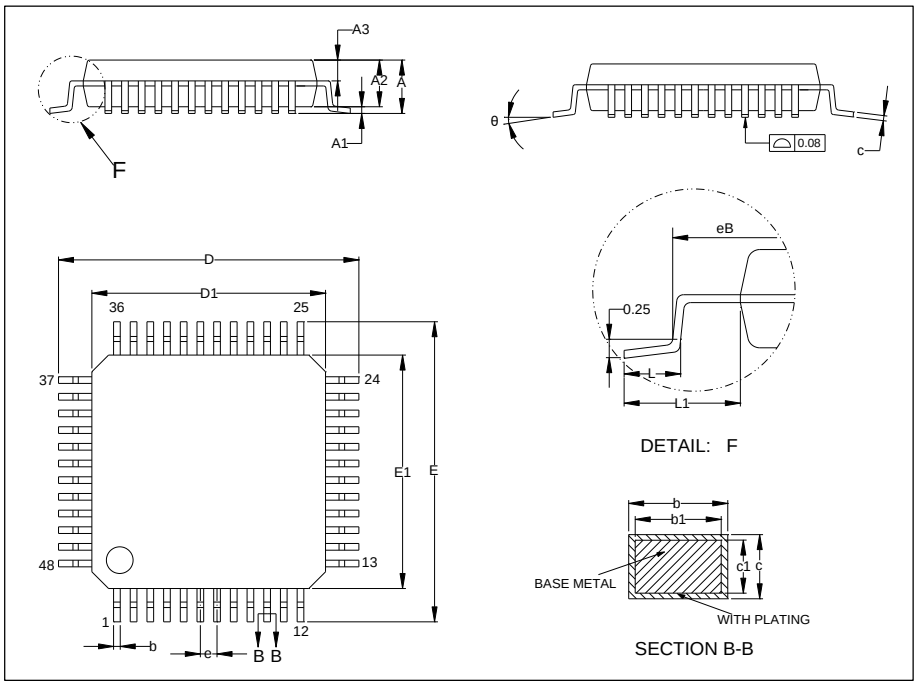


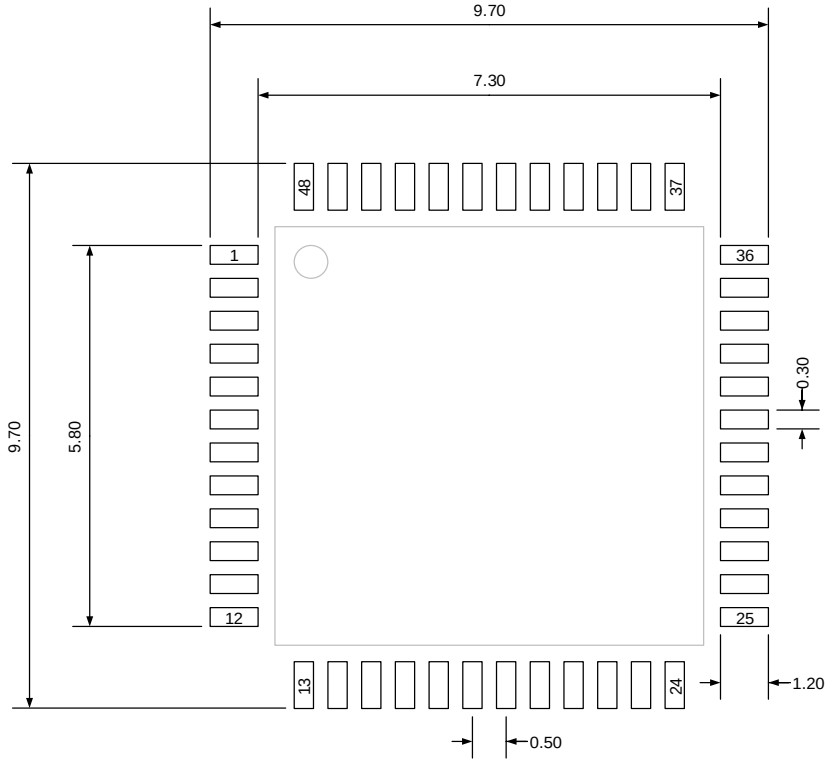
Table 5-1. LQFP48 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	—	0.50	—
eB	8.10	—	8.25
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

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(Original dimensions are in millimeters)

Figure 5-2. LQFP48 recommended footprint



(Original dimensions are in millimeters)

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5.2 LQFP32 package outline dimensions

Figure 5-3. LQFP32 package outline

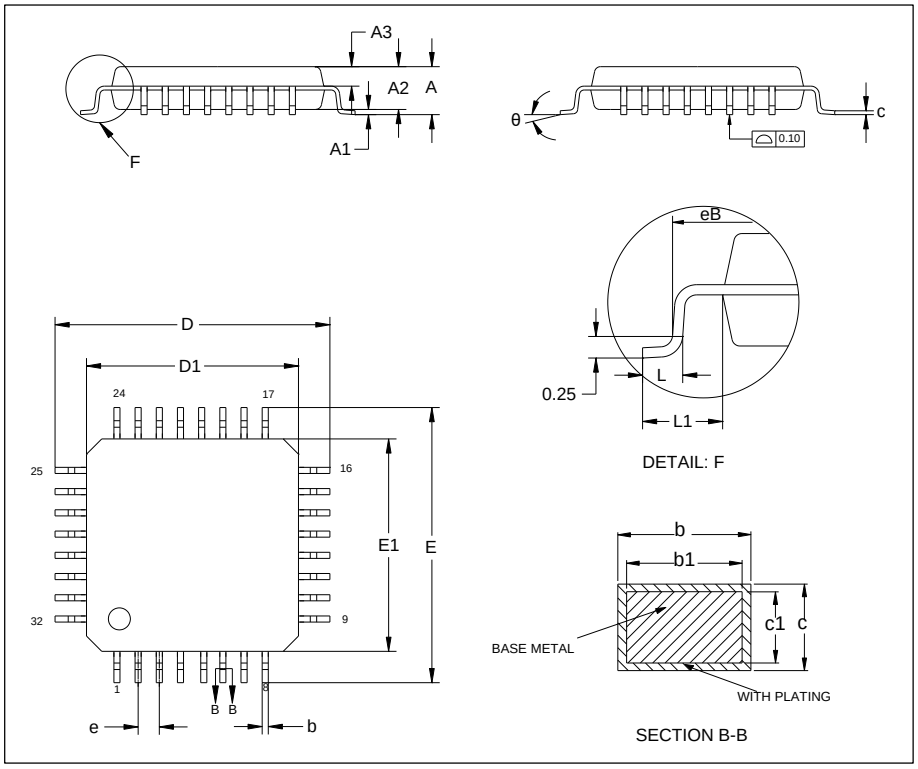


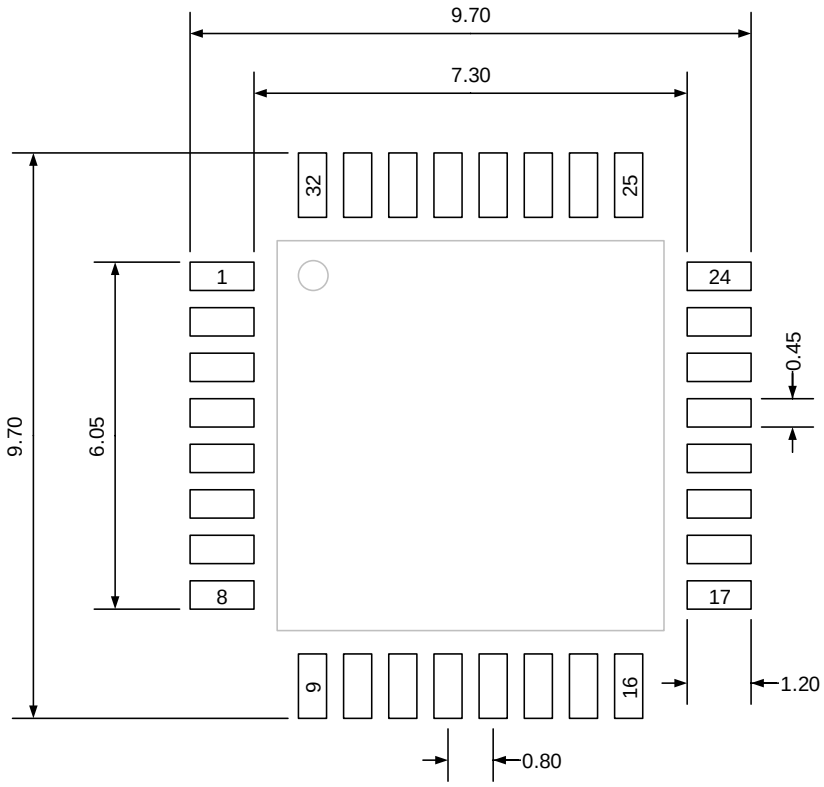
Table 5-2. LQFP32 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	—	0.41
b1	0.32	0.35	0.38
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	—	0.80	—
eB	8.10	—	8.25
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

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(Original dimensions are in millimeters)

Figure 5-4. LQFP32 recommended footprint



(Original dimensions are in millimeters)

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5.3 QFN32 package outline dimensions

Figure 5-5. QFN32 package outline

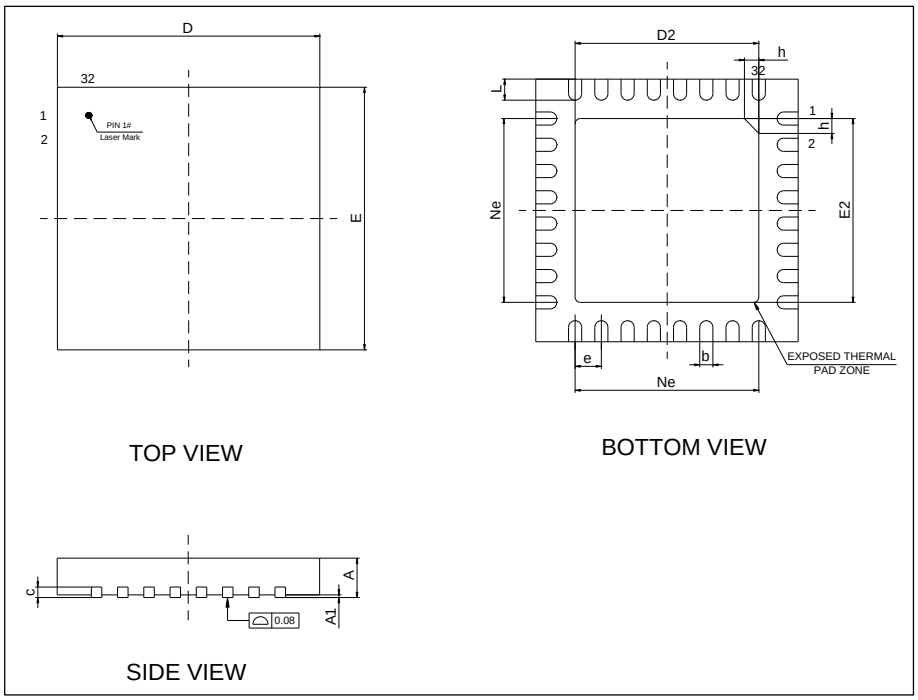


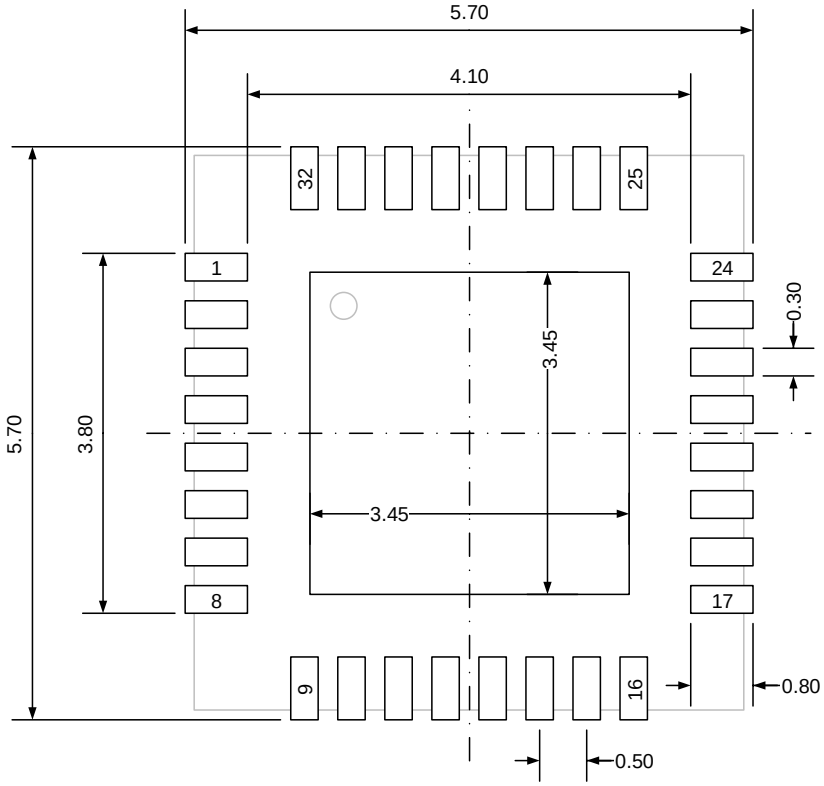
Table 5-3. QFN32 package dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
e	—	0.50	—
h	0.30	0.35	0.40
L	0.35	0.40	0.45
Ne	—	3.50	—

(Original dimensions are in millimeters)

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Figure 5-6. QFN32 recommended footprint



(Original dimensions are in millimeters)

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5.4 QFN28 package outline dimensions

Figure 5-7. QFN28 package outline

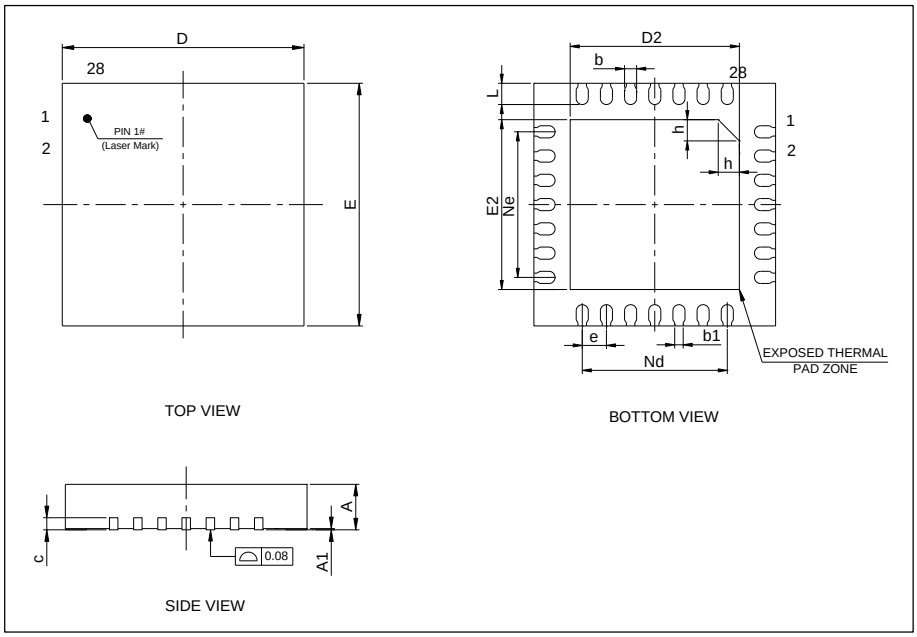


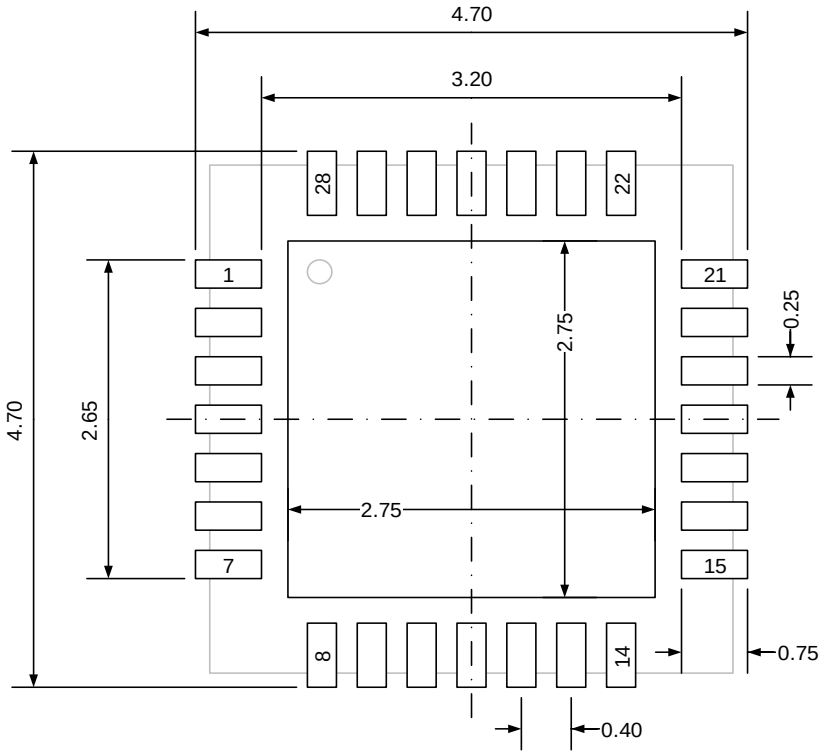
Table 5-4. QFN28 package dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	—	0.14	—
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
e	—	0.40	—
h	0.30	0.35	0.40
L	0.30	0.35	0.40
Nd	—	2.40	—
Ne	—	2.40	—

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Figure 5-8. QFN28 recommended footprint



(Original dimensions are in millimeters)

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5.5 TSSOP20 package outline dimensions

Figure 5-9. TSSOP20 package outline

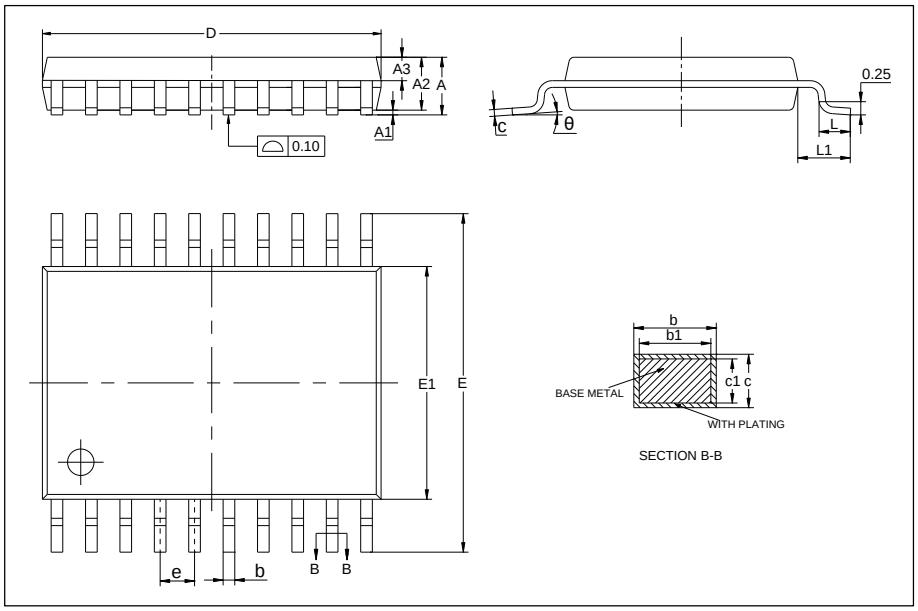


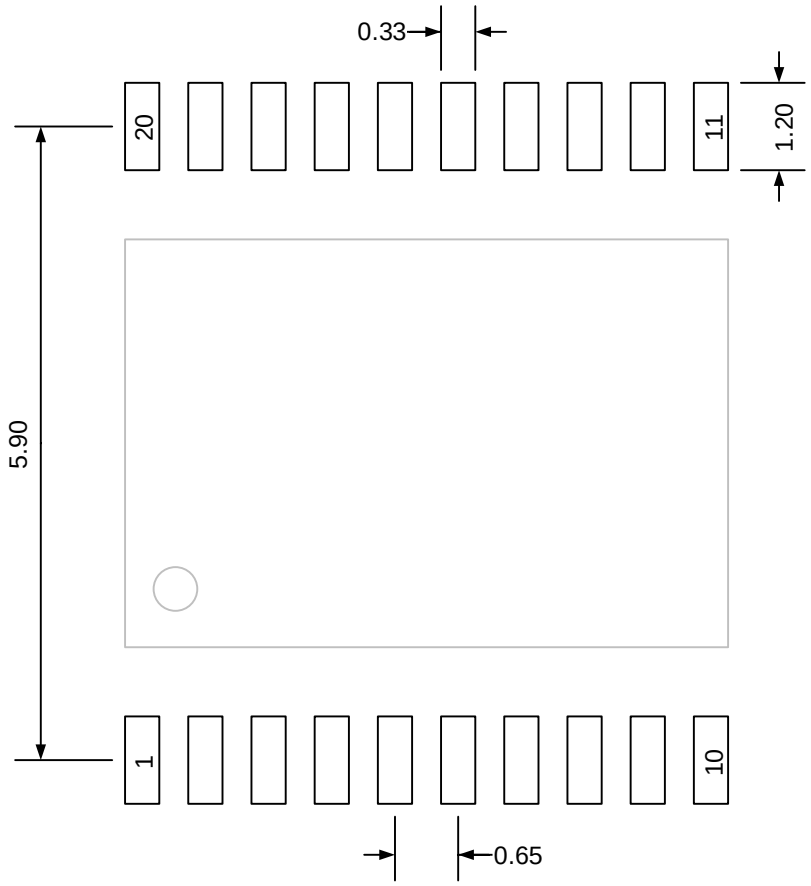
Table 5-5. TSSOP20 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	—	0.65	—
L	0.45	0.60	0.75
L1	—	1.00	—
θ	0°	—	8°

(Original dimensions are in millimeters)

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Figure 5-10. TSSOP20 recommended footprint



(Original dimensions are in millimeters)

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5.6 Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA}: Thermal resistance, junction-to-ambient.

θ_{JB}: Thermal resistance, junction-to-board.

θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. θ_{JA} is generally used to estimate junction temperature.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-6. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	LQFP48	64.40	°C/W
		LQFP32	66.11	
		QFN32	48.50	
		QFN28	66.07	
		TSSOP20	72.35	
θ_{JB}	Cold plate, 2S2P PCB	LQFP48	42.32	°C/W
		LQFP32	42.66	

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Symbol	Condition	Package	Value	Unit
		QFN32	28.32	
		QFN28	32.52	
		TSSOP20	53.01	
θ_{JC}	Cold plate, 2S2P PCB	LQFP48	22.47	°C/W
		LQFP32	30.06	
		QFN32	24.07	
		QFN28	30.58	
		TSSOP20	25.05	
Ψ_{JB}	Natural convection, 2S2P PCB	LQFP48	42.42	°C/W
		LQFP32	43.18	
		QFN32	28.93	
		QFN28	32.55	
		TSSOP20	53.15	
Ψ_{JT}	Natural convection, 2S2P PCB	LQFP48	1.74	°C/W
		LQFP32	4.56	
		QFN32	3.33	
		QFN28	3.27	
		TSSOP20	1.93	

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

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6 Ordering information

Table 6-1. Part ordering code for GD32F310xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32F310CBT6	128	LQFP48	Green	Industrial -40 °C to +85 °C
GD32F310C8T6	64	LQFP48	Green	Industrial -40 °C to +85 °C
GD32F310C8T7	64	LQFP48	Green	Industrial -40 °C to +105 °C
GD32F310K8T6	64	LQFP32	Green	Industrial -40 °C to +85 °C
GD32F310K8T7	64	LQFP32	Green	Industrial -40 °C to +105 °C
GD32F310K6T6	32	LQFP32	Green	Industrial -40 °C to +85 °C
GD32F310K8U6	64	QFN32	Green	Industrial -40 °C to +85 °C
GD32F310G8U6TR	64	QFN28	Green	Industrial -40 °C to +85 °C
GD32F310G8U7TR	64	QFN28	Green	Industrial -40 °C to +105 °C
GD32F310F8P6TR	64	TSSOP20	Green	Industrial -40 °C to +85 °C
GD32F310F6P6TR	32	TSSOP20	Green	Industrial -40 °C to +85 °C
GD32F310F4P6TR	16	TSSOP20	Green	Industrial -40 °C to +85 °C

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7 Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Dec.4, 2021
1.1	Update ***Arm® Cortex®-M4 core***. Update ***Debug mode***. Update ***Table 4-24. I/O port DC characteristics(1)(3)*** . Update ***Table 4-25. I/O port AC characteristics(1)(2)*** . Update ***Table 4-26. ADC characteristics*** . Update ***Table 4-27. ADC RAIN max for fADC = 36 MHz(1)*** . Update ***Table 4-28. ADC dynamic accuracy at fADC = 14 MHz(1)*** . Update ***Table 4-29. ADC dynamic accuracy at fADC = 28 MHz(1)*** . Update ***Table 4-30.ADC dynamic accuracy at fADC = 36 MHz(1)*** .	Apr.7, 2022
1.2	Update ***I2C characteristics***. Update ***Absolute maximum ratings***. Update ***Thermal characteristics***. Update ***NRST pin characteristics***. Update ***External clock characteristics***. Update ***Internal clock characteristics***. Update ***PLL characteristics***. Update ***GPIO characteristics***. Update ***Table 2-1. GD32F310xx devices features and peripheral list***. Update ***On-chip memory***.	Jul. 29, 2022
1.3	Update ***General description***. Add ***Table 2-2. GD32F310xx devices features and peripheral list (continued)***. Update ***Pinouts and pin assignment***. Update ***Pin definitions***. Update ***Package and operation temperature***. Update ***Absolute maximum ratings***. Update ***Operating conditions characteristics***. Update ***Internal clock characteristics***. Update ***Memory characteristics***. Update ***Ordering information***.	Aug. 22, 2022
1.4	Update ***Table 2-6. GD32F310KxU6 QFN32 pin definitions***. Update ***Table 2-7. GD32F310Gx QFN28 pin definitions.***	Sep. 14, 2022

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Revision No.	Description	Date
1.5	Update ***Power consumption***. Update ***I2C characteristics***.	Dec. 21, 2022
1.6	Update ***Table 4-1. Absolute maximum ratings(1)(4)*** . Update ***Package information***. Update ***Ordering information***.	Mar. 7, 2023
1.7	Update ***Table 2-4 GD32F310Cx LQFP48 pin definitions***. Update ***Table 2-5 GD32F310Kx LQFP32 pin definitions***. Update ***Table 2-6 GD32F310KxU6 QFN32 pin definitions***. Update ***Table 2-7 GD32F310Gx QFN28 pin definitions***. Update ***Table 2-8 GD32F310FxP6 TSSOP20 pin definitions***. Add note in chapter ***Operating conditions characteristics***.	Jun. 15, 2023
1.8	Version split. Update ***GPIO characteristics***.	Dec. 4, 2023
1.9	Update ***Pin definitions***. Change abbreviations BKIN->BRKIN. Update ***Absolute maximum ratings.*** Update ***Package information***. Add information to all PODs. Update ***Figure 2-7. GD32F310xx clock tree***. CK_ADC max is 36MHz.	Jun. 7, 2024
2.0	Add GD32F310CBT6. Update ***General description***. Update ***Device information*** . Update ***On-chip memory*** . Update ***Ordering information*** .	Sep. 19, 2024

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