GigaDevice Semiconductor Inc.

GD32F305xx
ARM® Cortex®-M4 32-bit MCU

Datasheet

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1 General description

The GD32F305xx device belongs to the mainstream line of GD32 MCU Family. It is a new 32-bit general-purpose microcontroller based on the ARM® Cortex®-M4 RISC core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. The Cortex®-M4 core features implements a full set of DSP instructions to address digital signal control markets that demand an efficient, easy-to-use blend of control and signal processing capabilities. It also provides a Memory Protection Unit (MPU) and powerful trace technology for enhanced application security and advanced debug support.

The GD32F305xx device incorporates the ARM® Cortex®-M4 32-bit processor core operating at 120 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 1024 KB on-chip Flash memory and 96 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to two 12-bit 2.6M SPS ADCs, two 12-bit DACs, up to ten general-purpose 16-bit timers, two 16-bit PWM advanced-control timers, and two 16-bit basic timers, as well as standard and advanced communication interfaces: up to three SPIs, two I2Cs, three USARTs and two UARTs, two I2Ss, two CANs, a USB device/host/OTG FS and an Ethernet MAC.

The device operates from a 2.6 to 3.6 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make GD32F305xx devices suitable for a wide range of interconnection and advanced applications, especially in areas such as industrial control, consumer and handheld equipment, communication networks, embedded modules, human machine interface, security and alarm systems, graphic display, automotive navigation, IoT and so on.



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2 Device overview

2.1 Device information

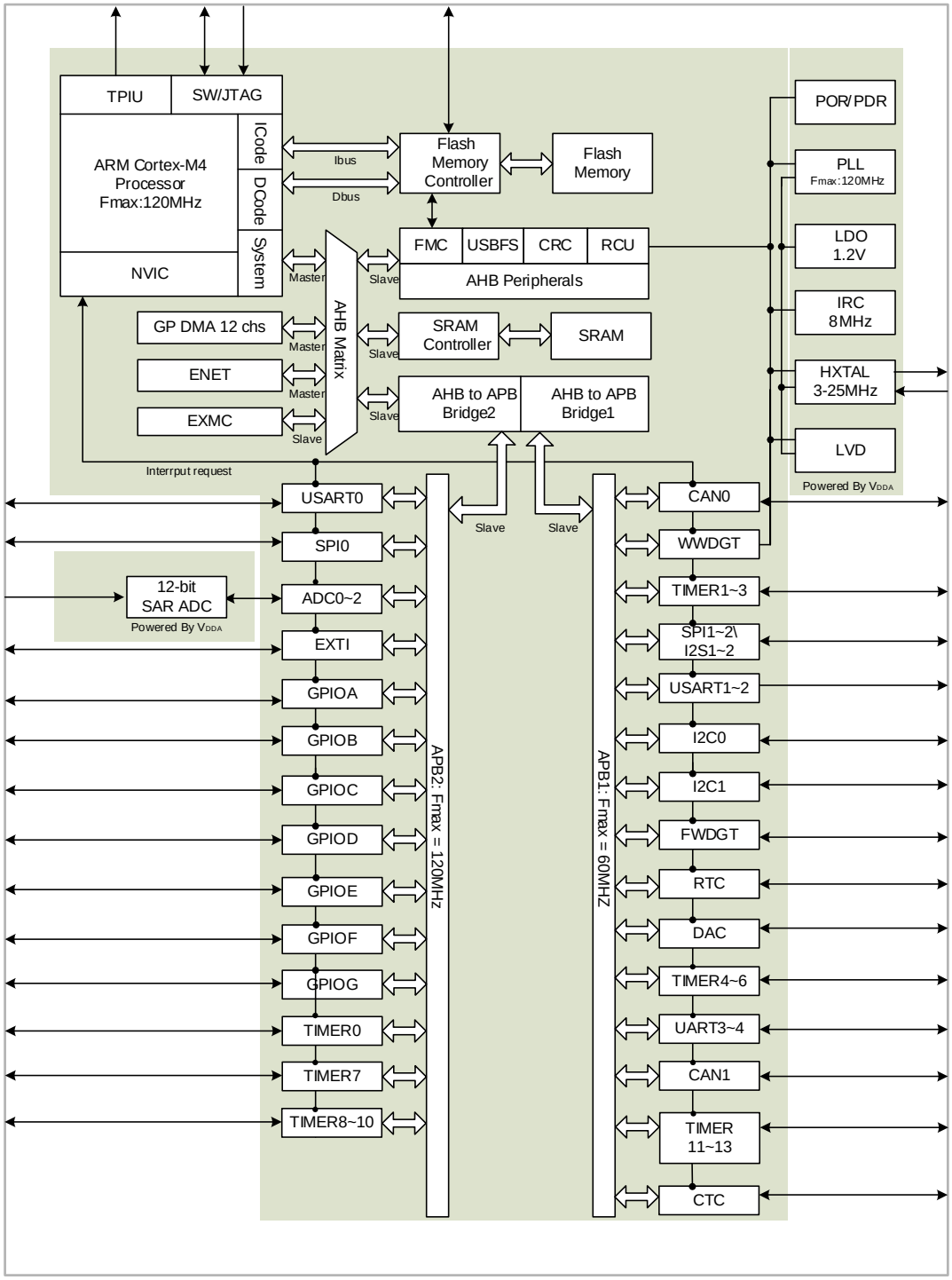
Table 1. GD32F305xx devices features and peripheral list

Part Number		GD32F305xx									
		RB	RC	RE	RG	VC	VE	VG	ZC	ZE	ZG
Flash	Code Area (KB)	128	256	256	256	256	256	256	256	256	256
	Data Area (KB)	0	0	256	768	0	256	768	0	256	768
	Total (KB)	128	256	512	1024	256	512	1024	256	512	1024
SRAM (KB)		64	96	96	96	96	96	96	96	96	96
Timers	16-bit GPTM	4	4	4	10	4	4	10	4	4	10
	Adv. 16-bit TM	1	1	2	2	1	2	2	2	2	2
	Basic 16-bit TM	2	2	2	2	2	2	2	2	2	2
	SysTick	1	1	1	1	1	1	1	1	1	1
	Watchdog	2	2	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1	1	1
Connectivity	USART+UART	3+2	3+2	3+2	3+2	3+2	3+2	3+2	3+2	3+2	3+2
	I2C	2	2	2	2	2	2	2	2	2	2
	SPI/I2S	3/2	3/2	3/2	3/2	3/2	3/2	3/2	3/2	3/2	3/2
	CAN 2.0B	2	2	2	2	2	2	2	2	2	2
	USB OTG FS	1	1	1	1	1	1	1	1	1	1
GPIO		51	51	51	51	80	80	80	112	112	112
EXMC		0	0	0	0	1	1	1	1	1	1
EXTI		16	16	16	16	16	16	16	16	16	16
ADC Unit (CHs)		2(16)	2(16)	2(16)	2(16)	2(16)	2(16)	2(16)	2(21)	2(21)	2(21)
DAC		2	2	2	2	2	2	2	2	2	2
Package		LQFP64				LQFP100			LQFP144		

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2.2 Block diagram

Figure 1. GD32F305xx block diagram



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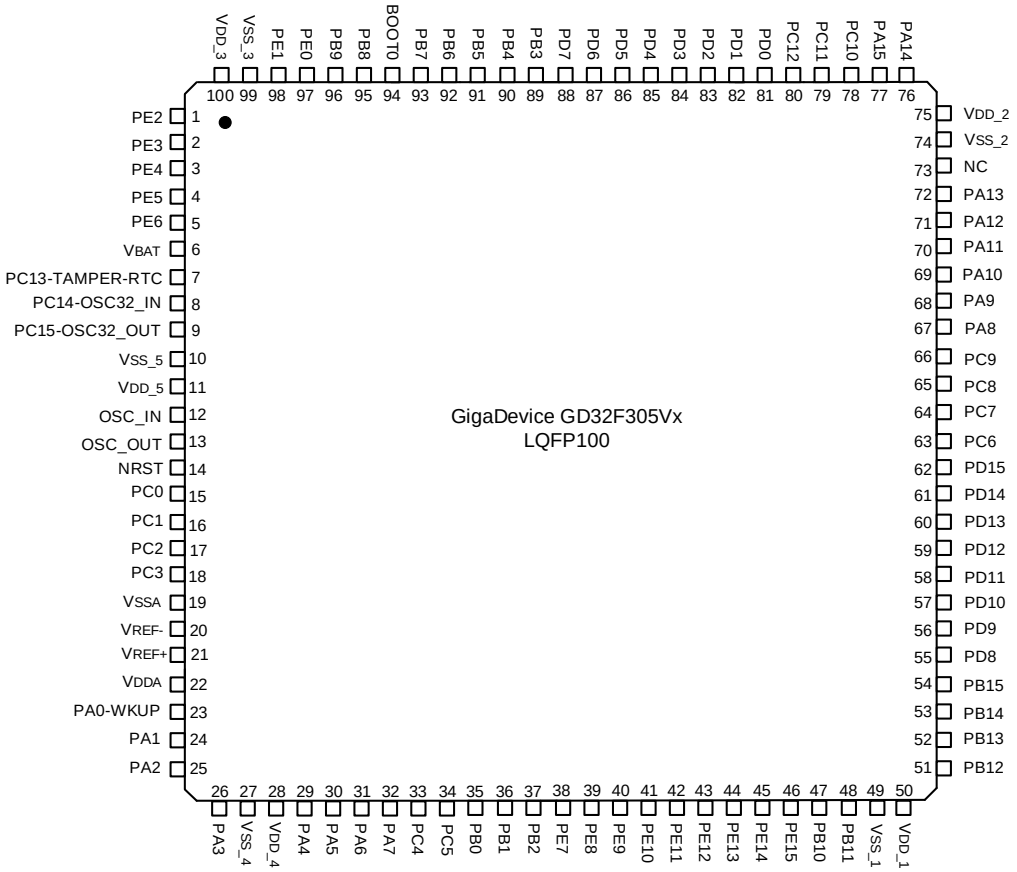
2.3 Pinouts and pin assignment

Figure 2. GD32F305Zx LQFP144 pinouts



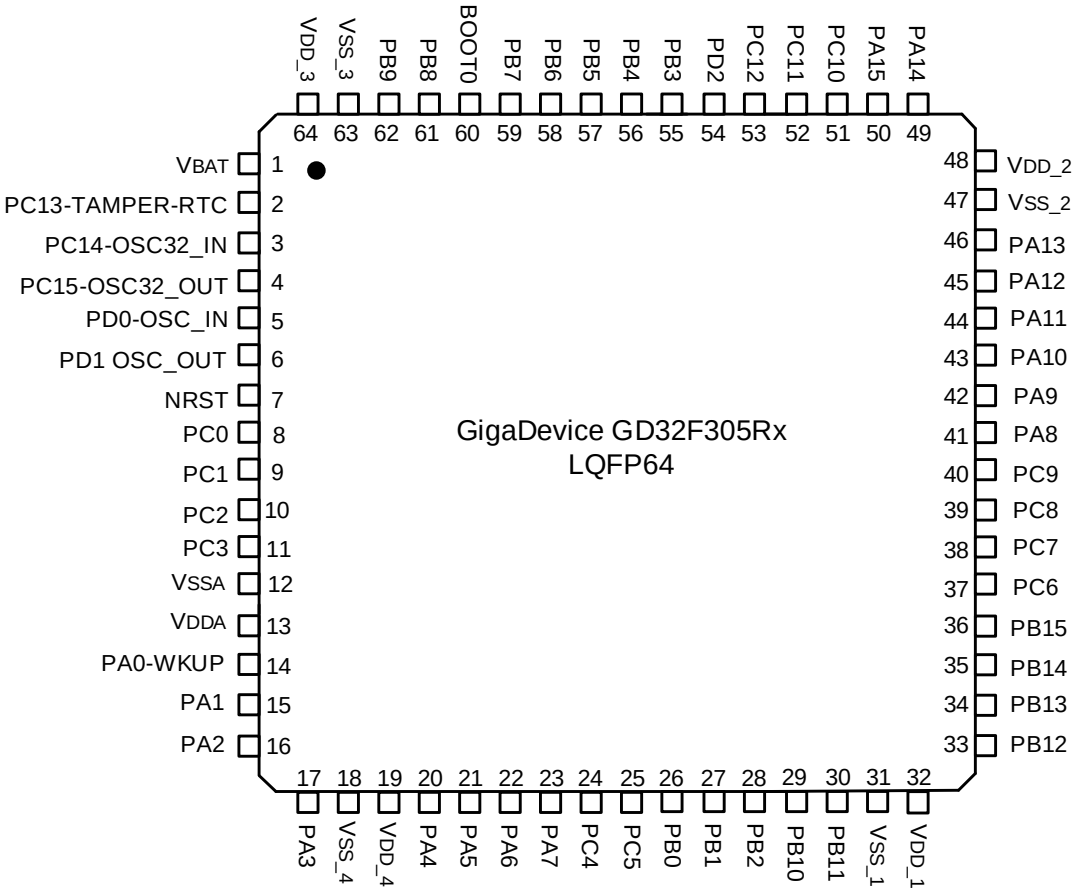
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Figure 3. GD32F305Vx LQFP100 pinouts



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Figure 4. GD32F305Rx LQFP64 pinouts



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2.4 Memory map

Figure 5. GD32F305xx memory map

Pre-defined Regions	Bus	Address	Peripherals
External device	AHB3	0xA000 0000 - 0xA000 0FFF	EXMC - SWREG
External RAM		0x9000 0000 - 0x9FFF FFFF	EXMC - PC CARD
		0x7000 0000 - 0x8FFF FFFF	EXMC - NAND
		0x6000 0000 - 0x6FFF FFFF	EXMC - NOR/PSRAM/SRAM
Peripheral	AHB1	0x5000 0000 - 0x5003 FFFF	USBFS
		0x4008 0000 - 0x4FFF FFFF	Reserved
		0x4004 0000 - 0x4007 FFFF	Reserved
		0x4002 BC00 - 0x4003 FFFF	Reserved
		0x4002 B000 - 0x4002 BBFF	Reserved
		0x4002 A000 - 0x4002 AFFF	Reserved
		0x4002 8000 - 0x4002 9FFF	Reserved
		0x4002 6800 - 0x4002 7FFF	Reserved
		0x4002 6400 - 0x4002 67FF	Reserved
		0x4002 6000 - 0x4002 63FF	Reserved
		0x4002 5000 - 0x4002 5FFF	Reserved
		0x4002 4000 - 0x4002 4FFF	Reserved
		0x4002 3C00 - 0x4002 3FFF	Reserved
		0x4002 3800 - 0x4002 3BFF	Reserved
		0x4002 3400 - 0x4002 37FF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2C00 - 0x4002 2FFF	Reserved
		0x4002 2800 - 0x4002 2BFF	Reserved
		0x4002 2400 - 0x4002 27FF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1C00 - 0x4002 1FFF	Reserved
		0x4002 1800 - 0x4002 1BFF	Reserved
		0x4002 1400 - 0x4002 17FF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0C00 - 0x4002 0FFF	Reserved
		0x4002 0800 - 0x4002 0BFF	Reserved
		0x4002 0400 - 0x4002 07FF	DMA1
		0x4002 0000 - 0x4002 03FF	DMA0
		0x4001 8400 - 0x4001 FFFF	Reserved
		0x4001 8000 - 0x4001 83FF	SDIO
	APB2	0x4001 7C00 - 0x4001 7FFF	Reserved
		0x4001 7800 - 0x4001 7BFF	Reserved

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Pre-defined Regions	Bus	Address	Peripherals
		0x4001 7400 - 0x4001 77FF	Reserved
		0x4001 7000 - 0x4001 73FF	Reserved
		0x4001 6C00 - 0x4001 6FFF	Reserved
		0x4001 6800 - 0x4001 6BFF	Reserved
		0x4001 5C00 - 0x4001 67FF	Reserved
		0x4001 5800 - 0x4001 5BFF	Reserved
		0x4001 5400 - 0x4001 57FF	TIMER10
		0x4001 5000 - 0x4001 53FF	TIMER9
		0x4001 4C00 - 0x4001 4FFF	TIMER8
		0x4001 4800 - 0x4001 4BFF	Reserved
		0x4001 4400 - 0x4001 47FF	Reserved
		0x4001 4000 - 0x4001 43FF	Reserved
		0x4001 3C00 - 0x4001 3FFF	ADC2
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	TIMER7
		0x4001 3000 - 0x4001 33FF	SPI0
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	ADC1
		0x4001 2400 - 0x4001 27FF	ADC0
		0x4001 2000 - 0x4001 23FF	GPIOG
		0x4001 1C00 - 0x4001 1FFF	GPIOF
		0x4001 1800 - 0x4001 1BFF	GPIOE
		0x4001 1400 - 0x4001 17FF	GPIOD
		0x4001 1000 - 0x4001 13FF	GPIOC
		0x4001 0C00 - 0x4001 0FFF	GPIOB
		0x4001 0800 - 0x4001 0BFF	GPIOA
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	AFIO
	APB1	0x4000 CC00 - 0x4000 FFFF	Reserved
		0x4000 C800 - 0x4000 CBFF	CTC
		0x4000 C400 - 0x4000 C7FF	Reserved
		0x4000 C000 - 0x4000 C3FF	Reserved
		0x4000 8000 - 0x4000 BFFF	Reserved
		0x4000 7C00 - 0x4000 7FFF	Reserved
		0x4000 7800 - 0x4000 7BFF	Reserved
		0x4000 7400 - 0x4000 77FF	DAC
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6C00 - 0x4000 6FFF	BKP
		0x4000 6800 - 0x4000 6BFF	CAN1
		0x4000 6400 - 0x4000 67FF	CAN0

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Pre-defined Regions	Bus	Address	Peripherals
		0x4000 6000 - 0x4000 63FF	Shared USBD/CAN SRAM 512 bytes
		0x4000 5C00 - 0x4000 5FFF	USBD
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 5000 - 0x4000 53FF	UART4
		0x4000 4C00 - 0x4000 4FFF	UART3
		0x4000 4800 - 0x4000 4BFF	USART2
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	Reserved
		0x4000 3C00 - 0x4000 3FFF	SPI2/I2S2
		0x4000 3800 - 0x4000 3BFF	SPI1/I2S1
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	TIMER13
		0x4000 1C00 - 0x4000 1FFF	TIMER12
		0x4000 1800 - 0x4000 1BFF	TIMER11
		0x4000 1400 - 0x4000 17FF	TIMER6
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0C00 - 0x4000 0FFF	TIMER4
		0x4000 0800 - 0x4000 0BFF	TIMER3
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM	AHB	0x2007 0000 - 0x3FFF FFFF	Reserved
		0x2006 0000 - 0x2006 FFFF	Reserved
		0x2003 0000 - 0x2005 FFFF	Reserved
		0x2002 0000 - 0x2002 FFFF	Reserved
		0x2001 C000 - 0x2001 FFFF	Reserved
		0x2001 8000 - 0x2001 BFFF	SRAM
		0x2000 5000 - 0x2001 7FFF	
		0x2000 0000 - 0x2000 4FFF	
Code	AHB	0x1FFF F810 - 0x1FFF FFFF	Reserved
		0x1FFF F800 - 0x1FFF F80F	Option Bytes
		0x1FFF F000 - 0x1FFF F7FF	Boot loader
		0x1FFF C010 - 0x1FFF EFFF	
		0x1FFF C000 - 0x1FFF C00F	
		0x1FFF B000 - 0x1FFF BFFF	

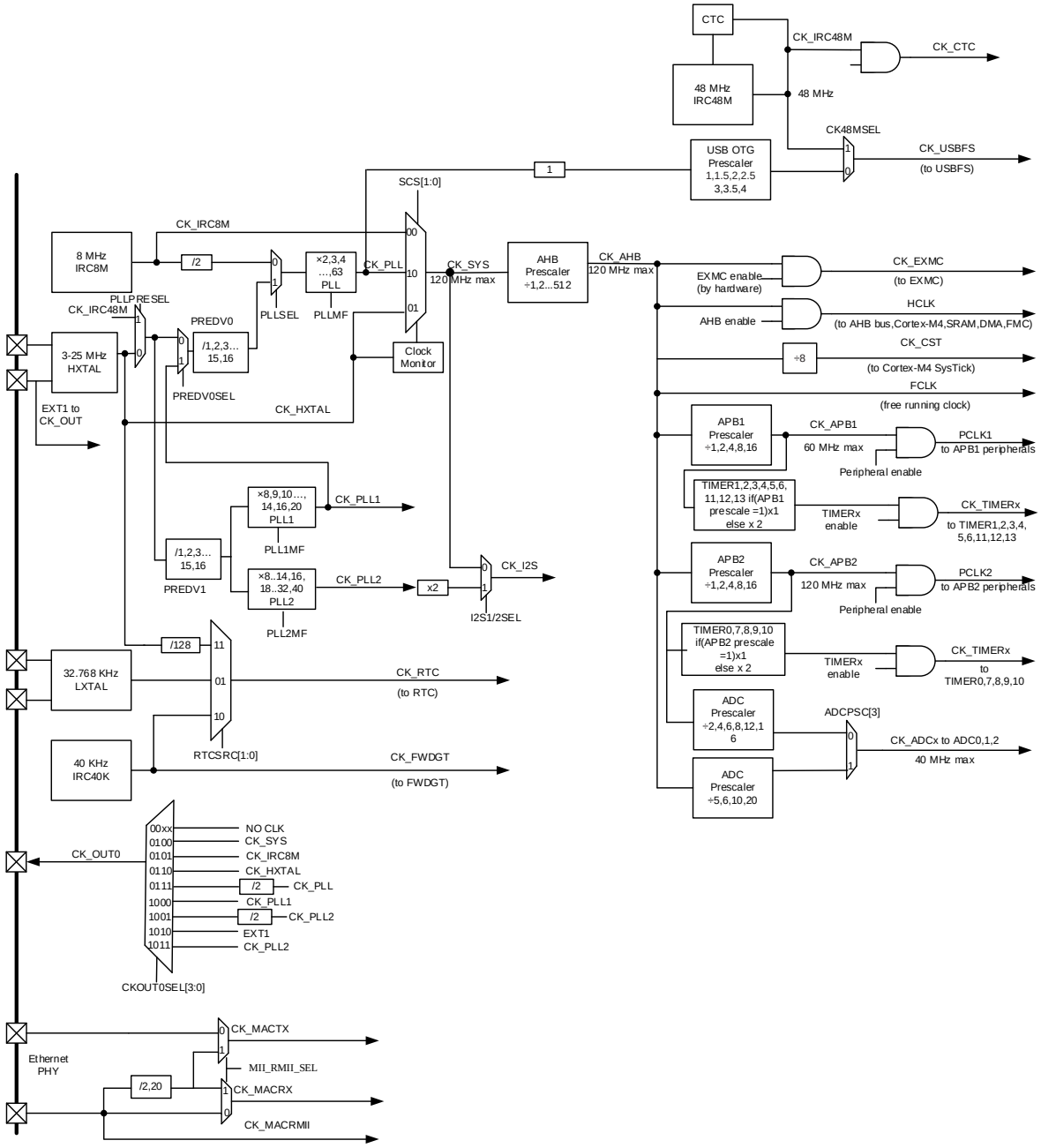
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Pre-defined Regions	Bus	Address	Peripherals
		0x1FFF 7A10 - 0x1FFF AFFF	Reserved
		0x1FFF 7800 - 0x1FFF 7A0F	Reserved
		0x1FFF 0000 - 0x1FFF 77FF	Reserved
		0x1FFE C010 - 0x1FFE FFFF	Reserved
		0x1FFE C000 - 0x1FFE C00F	Reserved
		0x1001 0000 - 0x1FFE BFFF	Reserved
		0x1000 0000 - 0x1000 FFFF	Reserved
		0x083C 0000 - 0x0FFF FFFF	Reserved
		0x0830 0000 - 0x083B FFFF	Reserved
		0x0810 0000 - 0x082F FFFF	Main Flash
		0x0802 0000 - 0x080F FFFF	
		0x0800 0000 - 0x0801 FFFF	
		0x0030 0000 - 0x07FF FFFF	Reserved
		0x0010 0000 - 0x002F FFFF	Aliased to Main Flash or Boot loader
		0x0002 0000 - 0x000F FFFF	
		0x0000 0000 - 0x0001 FFFF	

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2.5 Clock tree

Figure 6. GD32F305xx clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC8M: Internal 8M RC oscillators

IRC48M: Internal 48M RC oscillators

IRC32K: Internal 32K RC oscillator

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2.6 Pin definitions

Table 2. GD32F305xx pin definitions

Pin Name	Pins			Pin Type(1)	I/O(2) Level	Functions description
	LQFP144	LQFP100	LQFP64			
PE2	1	1	-	I/O	5VT	Default: PE2 Alternate: TRACECK, EXMC_A23
PE3	2	2	-	I/O	5VT	Default: PE3 Alternate: TRACED0, EXMC_A19
PE4	3	3	-	I/O	5VT	Default: PE4 Alternate:TRACED1, EXMC_A20
PE5	4	4	-	I/O	5VT	Default: PE5 Alternate:TRACED2, EXMC_A21 Remap: TIMER8_CH0
PE6	5	5	-	I/O	5VT	Default: PE6 Alternate:TRACED3, EXMC_A22 Remap: TIMER8_CH1
V_{BAT}	6	6	1	P		Default: V_{BAT}
PC13-TAMPER-RTC	7	7	2	I/O		Default: PC13 Alternate: TAMPER, RTC
PC14-OSC32_IN	8	8	3	I/O		Default: PC14 Alternate: OSC32_IN
PC15-OSC32_OUT	9	9	4	I/O		Default: PC15 Alternate: OSC32_OUT
PF0	10	-	-	I/O	5VT	Default: PF0 Alternate: EXMC_A0 Remap: CTC_SYNC
PF1	11	-	-	I/O	5VT	Default: PF1 Alternate: EXMC_A1
PF2	12	-	-	I/O	5VT	Default: PF2 Alternate: EXMC_A2
PF3	13	-	-	I/O	5VT	Default: PF3 Alternate: EXMC_A3
PF4	14	-	-	I/O	5VT	Default: PF4 Alternate: EXMC_A4
PF5	15	-	-	I/O	5VT	Default: PF5 Alternate: EXMC_A5
V_{SS_5}	16	10	-	P		Default: V_{SS_5}
V_{DD_5}	17	11	-	P		Default: V_{DD_5}
PF6	18	-	-	I/O		Default: PF6 Alternate: EXMC_NIORD Remap: TIMER9_CH0

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Pin Name	Pins			Pin Type(1)	I/O(2) Level	Functions description
	LQFP144	LQFP100	LQFP64			
PF7	19	-	-	I/O		Default: PF7 Alternate: EXMC_NREG Remap: TIMER10_CH0
PF8	20	-	-	I/O		Default: PF8 Alternate: EXMC_NIOWR Remap: TIMER12_CH0
PF9	21	-	-	I/O		Default: PF9 Alternate: EXMC_CD Remap: TIMER13_CH0
PF10	22	-	-	I/O		Default: PF10 Alternate: EXMC_INTR
OSC_IN	23	12	5	I		Default: OSC_IN Remap: PD0
OSC_OUT	24	13	6	O		Default: OSC_OUT Remap: PD1
NRST	25	14	7	I/O		Default: NRST
PC0	26	15	8	I/O		Default: PC0 Alternate: ADC01_IN10
PC1	27	16	9	I/O		Default: PC1 Alternate: ADC01_IN11
PC2	28	17	10	I/O		Default: PC2 Alternate: ADC01_IN12
PC3	29	18	11	I/O		Default: PC3 Alternate: ADC01_IN13
V_{SSA}	30	19	12	P		Default: V_{SSA}
V_{REF-}	31	20	-	P		Default: V_{REF-}
V_{REF+}	32	21	-	P		Default: V_{REF+}
V_{DDA}	33	22	13	P		Default: V_{DDA}
PA0-WKUP	34	23	14	I/O		Default: PA0 Alternate: WKUP, USART1_CTS, ADC01_IN0, TIMER1_CH0_ETI, TIMER4_CH0, TIMER7_ETI
PA1	35	24	15	I/O		Default: PA1 Alternate: USART1_RTS, ADC01_IN1, TIMER1_CH1, TIMER4_CH1
PA2	36	25	16	I/O		Default: PA2 Alternate: USART1_TX, ADC01_IN2, TIMER1_CH2, TIMER4_CH2, TIMER8_CH0, SPI0_IO2
PA3	37	26	17	I/O		Default: PA3 Alternate: USART1_RX, ADC01_IN3, TIMER1_CH3, TIMER4_CH3, TIMER8_CH1, SPI0_IO3
V_{SS_4}	38	27	18	P		Default: V_{SS_4}
V_{DD_4}	39	28	19	P		Default: V_{DD_4}
PA4	40	29	20	I/O		Default: PA4

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Pin Name	Pins			Pin Type(1)	I/O(2) Level	Functions description
	LQFP144	LQFP100	LQFP64			
						Alternate: SPI0_NSS, USART1_CK, ADC01_IN4, DAC_OUT0 Remap:SPI2_NSS, I2S2_WS
PA5	41	30	21	I/O		Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1
PA6	42	31	22	I/O		Default: PA6 Alternate: SPI0_MISO, ADC01_IN6, TIMER2_CH0, TIMER7_BKIN, TIMER12_CH0 Remap: TIMER0_BKIN
PA7	43	32	23	I/O		Default: PA7 Alternate: SPI0_MOSI, ADC01_IN7, TIMER2_CH1, TIMER7_CH0_ON, TIMER13_CH0 Remap: TIMER0_CH0_ON
PC4	44	33	24	I/O		Default: PC4 Alternate: ADC01_IN14
PC5	45	34	25	I/O		Default: PC5 Alternate: ADC01_IN15
PB0	46	35	26	I/O		Default: PB0 Alternate: ADC01_IN8, TIMER2_CH2, TIMER7_CH1_ON Remap: TIMER0_CH1_ON
PB1	47	36	27	I/O		Default: PB1 Alternate: ADC01_IN9, TIMER2_CH3, TIMER7_CH2_ON Remap: TIMER0_CH2_ON
PB2	48	37	28	I/O	5VT	Default: PB2, BOOT1
PF11	49	-	-	I/O	5VT	Default: PF11 Alternate: EXMC_NIOS16
PF12	50	-	-	I/O	5VT	Default: PF12 Alternate: EXMC_A6
V_{SS_6}	51	-	-	P		Default: V_{SS_6}
V_{DD_6}	52	-	-	P		Default: V_{DD_6}
PF13	53	-	-	I/O	5VT	Default: PF13 Alternate: EXMC_A7
PF14	54	-	-	I/O	5VT	Default: PF14 Alternate: EXMC_A8
PF15	55	-	-	I/O	5VT	Default: PF15 Alternate: EXMC_A9
PG0	56	-	-	I/O	5VT	Default: PG0 Alternate: EXMC_A10
PG1	57	-	-	I/O	5VT	Default: PG1 Alternate: EXMC_A11
PE7	58	38	-	I/O	5VT	Default: PE7 Alternate: EXMC_D4 Remap: TIMER0_ETI

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Pin Name	Pins			Pin Type(1)	I/O(2) Level	Functions description
	LQFP144	LQFP100	LQFP64			
PE8	59	39	-	I/O	5VT	Default: PE8 Alternate: EXMC_D5 Remap: TIMER0_CH0_ON
PE9	60	40	-	I/O	5VT	Default: PE9 Alternate: EXMC_D6 Remap: TIMER0_CH0
V_{SS_7}	61	-	-	P		Default: V_{SS_7}
V_{DD_7}	62	-	-	P		Default: V_{DD_7}
PE10	63	41	-	I/O	5VT	Default: PE10 Alternate: EXMC_D7 Remap: TIMER0_CH1_ON
PE11	64	42	-	I/O	5VT	Default: PE11 Alternate: EXMC_D8 Remap: TIMER0_CH1
PE12	65	43	-	I/O	5VT	Default: PE12 Alternate: EXMC_D9 Remap: TIMER0_CH2_ON
PE13	66	44	-	I/O	5VT	Default: PE13 Alternate: EXMC_D10 Remap: TIMER0_CH2
PE14	67	45	-	I/O	5VT	Default: PE14 Alternate: EXMC_D11 Remap: TIMER0_CH3
PE15	68	46	-	I/O	5VT	Default: PE15 Alternate: EXMC_D12 Remap: TIMER0_BKIN
PB10	69	47	29	I/O	5VT	Default: PB10 Alternate: I2C1_SCL, USART2_TX Remap: TIMER1_CH2
PB11	70	48	30	I/O	5VT	Default: PB11 Alternate: I2C1_SDA, USART2_RX Remap: TIMER1_CH3
V_{SS_1}	71	49	31	P		Default: V_{SS_1}
V_{DD_1}	72	50	32	P		Default: V_{DD_1}
PB12	73	51	33	I/O	5VT	Default: PB12 Alternate: SPI1_NSS, I2C1_SMBA, USART2_CK, TIMER0_BKIN, I2S1_WS, CAN1_RX
PB13	74	52	34	I/O	5VT	Default: PB13 Alternate: SPI1_SCK, USART2_CTS, TIMER0_CH0_ON, I2S1_CK, CAN1_TX
PB14	75	53	35	I/O	5VT	Default: PB14 Alternate: SPI1_MISO, USART2_RTS, TIMER0_CH1_ON, TIMER11_CH0

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	LQFP144	LQFP100	LQFP64			
PB15	76	54	36	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, TIMER0_CH2_ON, I2S1_SD, TIMER11_CH1
PD8	77	55	-	I/O	5VT	Default: PD8 Alternate: EXMC_D13 Remap: USART2_TX
PD9	78	56	-	I/O	5VT	Default: PD9 Alternate: EXMC_D14 Remap: USART2_RX
PD10	79	57	-	I/O	5VT	Default: PD10 Alternate: EXMC_D15 Remap: USART2_CK
PD11	80	58	-	I/O	5VT	Default: PD11 Alternate: EXMC_A16 Remap: USART2_CTS
PD12	81	59	-	I/O	5VT	Default: PD12 Alternate: EXMC_A17 Remap: TIMER3_CH0, USART2_RTS
PD13	82	60	-	I/O	5VT	Default: PD13 Alternate: EXMC_A18 Remap: TIMER3_CH1
V_{SS_8}	83	-	-	P		Default: V_{SS_8}
V_{DD_8}	84	-	-	P		Default: V_{DD_8}
PD14	85	61	-	I/O	5VT	Default: PD14 Alternate: EXMC_D0 Remap: TIMER3_CH2
PD15	86	62	-	I/O	5VT	Default: PD15 Alternate: EXMC_D1 Remap: TIMER3_CH3, CTC_SYNC
PG2	87	-	-	I/O	5VT	Default: PG2 Alternate: EXMC_A12
PG3	88	-	-	I/O	5VT	Default: PG3 Alternate: EXMC_A13
PG4	89	-	-	I/O	5VT	Default: PG4 Alternate: EXMC_A14
PG5	90	-	-	I/O	5VT	Default: PG5 Alternate: EXMC_A15
PG6	91	-	-	I/O	5VT	Default: PG6 Alternate: EXMC_INT1
PG7	92	-	-	I/O	5VT	Default: PG7 Alternate: EXMC_INT2
PG8	93	-	-	I/O	5VT	Default: PG8
V_{SS_9}	94	-	-	P		Default: V_{SS_9}

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Pin Name	Pins			Pin Type(1)	I/O(2) Level	Functions description
	LQFP144	LQFP100	LQFP64			
V_{DD_9}	95	-	-	P		Default: V_{DD_9}
PC6	96	63	37	I/O	5VT	Default: PC6 Alternate: I2S1_MCK, TIMER7_CH0 Remap: TIMER2_CH0
PC7	97	64	38	I/O	5VT	Default: PC7 Alternate: I2S2_MCK, TIMER7_CH1 Remap: TIMER2_CH1
PC8	98	65	39	I/O	5VT	Default: PC8 Alternate: TIMER7_CH2 Remap: TIMER2_CH2
PC9	99	66	40	I/O	5VT	Default: PC9 Alternate: TIMER7_CH3 Remap: TIMER2_CH3
PA8	100	67	41	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, VCORE, USBFS_SOF, CTC_SYNC
PA9	101	68	42	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS
PA10	102	69	43	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, USBFS_ID
PA11	103	70	44	I/O	5VT	Default: PA11 Alternate: USART0_CTS, CAN0_RX, USBFS_DM, TIMER0_CH3
PA12	104	71	45	I/O	5VT	Default: PA12 Alternate: USART0_RTS, USBFS_DP, CAN0_TX, TIMER0_ETI
PA13	105	72	46	I/O	5VT	Default: JTMS, SWDIO Remap: PA13
NC	106	73	-			-
V_{SS_2}	107	74	47	P		Default: V_{SS_2}
V_{DD_2}	108	75	48	P		Default: V_{DD_2}
PA14	109	76	49	I/O	5VT	Default: JTCK, SWCLK Remap: PA14
PA15	110	77	50	I/O	5VT	Default: JTDI Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0_ETI, PA15, SPI0_NSS
PC10	111	78	51	I/O	5VT	Default: PC10 Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK
PC11	112	79	52	I/O	5VT	Default: PC11 Alternate: UART3_RX Remap: USART2_RX, SPI2_MISO
PC12	113	80	53	I/O	5VT	Default: PC12 Alternate: UART4_TX

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Pin Name	Pins			Pin Type(1)	I/O(2) Level	Functions description
	LQFP144	LQFP100	LQFP64			
						Remap: USART2_CK, SPI2_MOSI, I2S2_SD
PD0	114	81	-	I/O	5VT	Default: PD0 Alternate: EXMC_D2 Remap: CAN0_RX, OSC_IN
PD1	115	82	-	I/O	5VT	Default: PD1 Alternate: EXMC_D3 Remap: CAN0_TX, OSC_OUT
PD2	116	83	54	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, UART4_RX
PD3	117	84	-	I/O	5VT	Default: PD3 Alternate: EXMC_CLK Remap: USART1_CTS
PD4	118	85	-	I/O	5VT	Default: PD4 Alternate: EXMC_NOE Remap: USART1_RTS
PD5	119	86	-	I/O	5VT	Default: PD5 Alternate: EXMC_NWE Remap: USART1_TX
V_{SS_10}	120	-	-			Default: V_{SS_10}
V_{DD_10}	121	-	-			Default: V_{DD_10}
PD6	122	87	-	I/O	5VT	Default: PD6 Alternate: EXMC_NWAIT Remap: USART1_RX
PD7	123	88	-	I/O	5VT	Default: PD7 Alternate: EXMC_NE0, EXMC_NCE1 Remap: USART1_CK
PG9	124	-	-	I/O	5VT	Default: PG9 Alternate: EXMC_NE1, EXMC_NCE2
PG10	125	-	-	I/O	5VT	Default: PG10 Alternate: EXMC_NCE3_0, EXMC_NE2
PG11	126	-	-	I/O	5VT	Default: PG11 Alternate: EXMC_NCE3_1
PG12	127	-	-	I/O	5VT	Default: PG12 Alternate: EXMC_NE3
PG13	128	-	-	I/O	5VT	Default: PG13 Alternate: EXMC_A24
PG14	129	-	-	I/O	5VT	Default: PG14 Alternate: EXMC_A25
V_{SS_11}	130	-	-	P		Default: V_{SS_11}
V_{DD_11}	131	-	-	P		Default: V_{DD_11}
PG15	132	-	-	I/O	5VT	Default: PG15
PB3	133	89	55	I/O	5VT	Default: JTDO

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Pin Name	Pins			Pin Type(1)	I/O(2) Level	Functions description
	LQFP144	LQFP100	LQFP64			
						Alternate:SPI2_SCK, I2S2_CK Remap: PB3, TRACESWO, TIMER1_CH1, SPI0_SCK
PB4	134	90	56	I/O	5VT	Default: NJTRST Alternate: SPI2_MISO Remap: TIMER2_CH0, PB4, SPI0_MISO
PB5	135	91	57	I/O		Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD Remap: TIMER2_CH1, SPI0_MOSI, CAN1_RX
PB6	136	92	58	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, TIMER3_CH0 Remap: USART0_TX, CAN1_TX, SPI0_IO2
PB7	137	93	59	I/O	5VT	Default: PB7 Alternate: I2C0_SDA , TIMER3_CH1, EXMC_NADV Remap: USART0_RX, SPI0_IO3
BOOT0	138	94	60	I		Default: BOOT0
PB8	139	95	61	I/O	5VT	Default: PB8 Alternate: TIMER3_CH2, TIMER9_CH0 Remap: I2C0_SCL, CAN0_RX
PB9	140	96	62	I/O	5VT	Default: PB9 Alternate: TIMER3_CH3, TIMER10_CH0 Remap: I2C0_SDA, CAN0_TX
PE0	141	97	-	I/O	5VT	Default: PE0 Alternate: TIMER3_ETI, EXMC_NBL0
PE1	142	98	-	I/O	5VT	Default: PE1 Alternate: EXMC_NBL1
V_{SS_3}	143	99	63	P		Default: V_{SS_3}
V_{DD_3}	144	100	64	P		Default: V_{DD_3}

Notes:

1. Type: I = input, O = output, P = power.
2. I/O Level: 5VT = 5 V tolerant.

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3 Functional description

3.1 ARM® Cortex®-M4 core

The ARM® Cortex®-M4 processor is a high performance embedded processor with DSP instructions which allow efficient signal processing and complex algorithm execution. It brings an efficient, easy-to-use blend of control and signal processing capabilities to meet the digital signal control markets demand. The processor is highly configurable enabling a wide range of implementations from those requiring floating point operations, memory protection and powerful trace technology to cost sensitive devices requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

32-bit ARM® Cortex®-M4 processor core

- Up to 120 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Floating Point Unit (FPU)
- Integrated DSP instructions
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M4 processor is based on the ARMv7-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M4:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Memory Protection Unit (MPU)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

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3.2 On-chip memory

- Up to 1024 Kbytes of Flash memory, including code Flash and data Flash
- Up to 96 KB of SRAM

The ARM® Cortex®-M4 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 1024 Kbytes of inner Flash at most, which includes code Flash that available for storing programs and data, and accessed (R/W) at CPU clock speed with zero wait states. An extra data Flash is also included for storing data mainly. The Figure of GD32F305xx memory map shows the memory of the GD32F305xx series of devices, including Flash, SRAM, peripheral, and other pre-defined regions.

3.3 Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 48 MHz RC oscillator
- Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the two AHB domains are 120 MHz. The maximum frequency of the two APB domains including APB1 is 60 MHz and APB2 is 120 MHz. See Figure 6 for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from/down to 2.6 V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: 1.8 to 3.6 V, power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

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3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0, USART1, CAN1, USB OTG FS in device mode. It also can be used to transfer and update the Flash memory code, the data and the vector table sections. In default condition, boot from bank 1 of Flash memory is selected. It also supports to boot from bank 2 of Flash memory by setting a bit in option bytes.

3.5 Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are Sleep mode, Deep-sleep mode, and Standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In Deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC8M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the Deep-sleep mode including the 23 external lines, the RTC alarm, the LVD output, and USB wakeup. When exiting the Deep-sleep mode, the IRC8M is selected as the system clock.
- **Standby** mode
  In Standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. The contents of SRAM and registers (except Backup Registers) are lost. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC, the FWDG reset, and the rising edge on WKUP pin.

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3.6 Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 2.6MSPS
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Input voltage range: V_{SSA} to V_{DDA} (2.6 to 3.6 V)
- Temperature sensor

Up to three 12-bit 2.6MSPS multi-channel ADCs are integrated in the device. It has a total of 18 multiplexed channels: 16 external channels, 1 channel for internal temperature sensor (V_{SENSE}), 1 channel for internal reference voltage (V_{REFINT}). The input voltage range is between 2.6 V and 3.6 V. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general-purpose level 0 timers (TMx) and the advanced-control timers (TM0 and TM7) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

3.7 Digital to analog converter (DAC)

- Two 12-bit DACs with independent output channels
- 8-bit or 12-bit mode in conjunction with the DMA controller

The two 12-bit buffered DACs are used to generate variable analog outputs. The DAC channels can be triggered by the timer or EXTI with DMA support. In dual DAC channel operation, conversions could be done independently or simultaneously. The maximum output value of the DAC is V_{REF+}.

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3.8 DMA

- 7 channel DMA 1 controller and 5 channel DMA 2 controller
- Peripherals supported: Timers, ADC, SPIs, I²Cs, USARTs, DAC, I²S

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Four types of access method are supported: peripheral to peripheral, peripheral to memory, memory to peripheral, memory to memory

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.9 General-purpose inputs/outputs (GPIOs)

- Up to 112 fast GPIOs, all mappable on 16 external interrupt vectors (EXTI)
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 112 general purpose I/O pins (GPIO) in GD32F305xx, named PA0 ~ PA15 and PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0-PF15, PG0-PG15 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

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3.10 Timers and PWM generation

- Two 16-bit advanced-control timer (TM0 & TM7), ten 16-bit general-purpose timers (TM1 ~ TM4, TM8 ~ TM13), and two 16-bit basic timer (TM5 & TM6)
- Up to 4 independent channels of PWM, output compare or input capture for each general-purpose timer (GPTM) and external trigger input
- 16-bit, motor control PWM advanced-control timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (Free watchdog and window watchdog)

The advanced-control timer (TM0 & TM7) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general-purpose timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge- or center-aligned counting modes) and single pulse mode output. If configured as a general-purpose 16-bit timer, it has the same functions as the TMx timer. It can be synchronized with external signals or to interconnect with other GPTMs together which have the same architecture and features.

The general-purpose timer (GPTM), can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TM1 ~ TM4 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TM8 ~ TM13 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The GPTM also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TM5 & TM6, are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32F305xx have two watchdog peripherals, Independent watchdog and window watchdog. They offer a combination of high safety level, flexibility of use and timing accuracy.

The independent watchdog timer includes a 12-bit down-counting counter and a 8-bit prescaler, It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in stop and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

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The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.11 Real time clock (RTC)

- 32-bit up-counter with a programmable 20-bit prescaler
- Alarm function
- Interrupt and wake-up event

The real time clock is an independent timer which provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and an expected interrupt. The RTC features a 32-bit programmable counter for long-term measurement using the compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz from external crystal oscillator.

3.12 Inter-integrated circuit (I2C)

- Up to two I2C bus interfaces can support both master and slave mode with a frequency up to 1 MHz (Fast mode plus)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides several data transfer rates: 100 KHz of standard mode, 400 KHz of the fast mode and 1 MHz of the fast mode plus . The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

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3.13 Serial peripheral interface (SPI)

- Up to three SPI interfaces with a frequency of up to 30 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

3.14 Universal synchronous asynchronous receiver transmitter (USART)

- Up to three USARTs and two UARTs with operating frequency up to 10.5 MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- USARTs support ISO 7816-3 compliant smart card interface

The USART (USART0, USART1 and USART2) and UART (UART3 & UART4) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART/UART also supports DMA function for high speed data communication except UART4.

3.15 Inter-IC sound (I2S)

- Two I2S bus Interfaces with sampling frequency from 8 kHz to 192 kHz
- Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 3-wire serial lines. GD32F305xx contain two I2S-bus interfaces that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1 and SPI2. The audio sampling frequency from 8 kHz to 192 kHz is supported.

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3.16 Universal serial bus on-the-go full-speed (USB OTG FS)

- One USB device/host/OTG full-speed Interface with frequency up to 12 Mbit/s
- Internal 48 MHz oscillator (IRC48M) support crystal-less operation
- Internal main PLL for USB CLK compliantly
- Internal USB OTG FS PHY support

The Universal Serial Bus (USB) is a 4-wire bus with 4 bidirectional endpoints. The device controller enables 12 Mbit/s data exchange with integrated transceivers. Transaction formatting is performed by the hardware, including CRC generation and checking. It supports both host and device modes, as well as OTG mode with Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The controller contains a full-speed USB PHY internal. For full-speed or low-speed operation, no more external PHY chip is needed. It supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. The required precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HXTAL crystal oscillator) or by the internal 48 MHz oscillator (IRC48M) in automatic trimming mode that allows crystal-less operation.

3.17 Controller area network (CAN)

- Two CAN2.0B interface with communication frequency up to 1 Mbit/s
- Internal main PLL for CAN CLK compliantly

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three mailboxes for transmission and two FIFOs of three message deep for reception. It also provides 28 scalable/configurable identifier filter banks for selecting the incoming messages needed and discarding the others.

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3.18 External memory controller (EXMC)

- Supported external memory: SRAM, PSRAM, ROM and NOR-Flash, NAND Flash and CF card
- Provide ECC calculating hardware module for NAND Flash memory block
- Up to 16-bit data bus
- Support to interface with Motorola 6800 and Intel 8080 type LCD directly

External memory controller (EXMC) is an abbreviation of external memory controller. It is divided in to several sub-banks for external device support, each sub-bank has its own chip selection signal but at one time, only one bank can be accessed. The EXMC support code execution from external memory except NAND Flash and CF card. The EXMC also can be configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

3.19 Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.20 Package and operation temperature

- LQFP144 (GD32F305Zx), LQFP100 (GD32F305Vx) and LQFP64 (GD32F305Rx)
- Operation temperature range: -40°C to +85°C (industrial level)

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4 Electrical characteristics

4.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5V tolerant pin	V_{SS} - 0.3	V_{DD} + 4.0	V
	Input voltage on other I/O	V_{SS} - 0.3	4.0	V
$\|\Delta V_{DDx}\|$	Variations between different VDD power pins	—	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between different ground pins	—	50	mV
I_{IO}	Maximum current for GPIO pins	—	25	mA
T_A	Operating temperature range	-40	+85	°C
T_{STG}	Storage temperature range	-55	+150	°C
T_J	Maximum junction temperature	—	125	°C

4.2 Recommended DC characteristics

Table 4. DC operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	—	2.6	3.3	3.6	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	2.6	3.3	3.6	V
V_{BAT}	Battery supply voltage	—	1.8	—	3.6	V

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4.3 Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 5. Power consumption characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current (Run mode)	V_{DD}=V_{DDA}=3.3V, HXTAL=25MHz, System clock=120MHz, All peripherals enabled	—	45.6	—	mA
		V_{DD}=V_{DDA}=3.3V, HXTAL =25MHz, System clock =120MHz, All peripherals disabled	—	25.0	—	mA
		V_{DD}=V_{DDA}=3.3V, HXTAL =25MHz, System clock =108MHz, All peripherals enabled	-—	42.5	—	mA
		V_{DD}=V_{DDA}=3.3V, HXTAL =25MHz, System Clock =108MHz, All peripherals disabled	—	22.5	—	mA
	Supply current (Sleep mode)	V_{DD}=V_{DDA}=3.3V, HXTAL =25MHz, CPU clock off, System clock=120MHz, All peripherals enabled	—	44.9	—	mA
		V_{DD}=V_{DDA}=3.3V, HXTAL =25MHz, CPU clock off, System clock=120MHz, All peripherals disabled	—	13.86	—	mA
	Supply current (Deep-Sleep mode)	V_{DD}=V_{DDA}=3.3V, Regulator in run mode, IRC32K on, RTC on, All GPIOs analog mode	—	208	—	µA
		V_{DD}=V_{DDA}=3.3V, Regulator in low power mode, IRC32K on, RTC on, All GPIOs analog mode	—	180	—	µA
	Supply current (Standby mode)	V_{DD}=V_{DDA}=3.3V, LXTAL off, IRC32K on, RTC on	—	5.10	—	µA
		V_{DD}=V_{DDA}=3.3V, LXTAL off, IRC32K on, RTC off	—	4.90	—	µA
		V_{DD}=V_{DDA}=3.3V, LXTAL off, IRC32K off, RTC off	—	4.30	—	µA
I_{BAT}	Battery supply current	V_{DD} not available, V_{BAT}=3.6 V, LXTAL on with external crystal, RTC on, Higher driving	—	1.78	—	µA
		V_{DD} not available, V_{BAT}=3.3 V, LXTAL on with external crystal, RTC on, Higher driving	—	1.48	—	µA
		V_{DD} not available, V_{BAT}=2.6 V, LXTAL on with external crystal, RTC on, Higher driving	—	1.16	—	µA
		V_{DD} not available, V_{BAT}=3.6 V, LXTAL on with external crystal, RTC on, Lower driving	—	1.11	—	µA

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		V_{DD} not available, V_{BAT}=3.3 V, LXTAL on with external crystal, RTC on, Lower driving	—	0.83	—	µA
		V_{DD} not available, V_{BAT}=2.6 V, LXTAL on with external crystal, RTC on, Lower driving	—	0.51	—	µA

4.4 EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in the following table, based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 6. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	VDD = 3.3 V, TA = +25 °C conforms to IEC 61000-4-2	3B
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V_{DD} and V_{SS} pins	VDD = 3.3 V, TA = +25 °C conforms to IEC 61000-4-4	4A

EMI (Electromagnetic Interference) emission testing result is given in the following table, compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 7. EMI characteristics

Symbol	Parameter	Conditions	Tested frequency band	Conditions		Unit
				24M	48M	
S_{EMI}	Peak level	VDD = 5.0 V, TA = +25 °C, compliant with IEC 61967-2	0.1 to 2 MHz	<0	<0	dBµV
			2 to 30 MHz	-3.9	-2.8	
			30 to 130 MHz	-7.2	-8	
			130 MHz to 1GHz	-7	-7	

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4.5 Power supply supervisor characteristics

Table 8. Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{POR}	Power on reset threshold	—	2.30	2.40	2.48	V
V_{PDR}	Power down reset threshold		1.72	1.80	1.88	V
V_{HYST}	PDR hysteresis		—	0.6	—	V
$T_{RSTTEMP}$	Reset temporization		—	2	—	ms

4.6 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 9. ESD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=25 °C; JESD22-A114	—	—	6000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A=25 °C; JESD22-C101	—	—	1000	V

Table 10. Static latch-up characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A=25 °C; JESD78	—	—	±200	mA
	V_{supply} over voltage		—	—	5.4	V

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4.7 External clock characteristics

Table 11. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}	High Speed External oscillator (HXTAL) frequency	V_{DD}=5.0V	4	8	32	MHz
C_{HXTAL}	Recommended load capacitance on OSC_IN and OSC_OUT	—	—	20	30	pF
R_{FHXTAL}	Recommended external feedback resistor between OSC_IN and OSC_OUT	—	—	400	—	KΩ
D_{HXTAL}	HXTAL oscillator duty cycle	—	30	50	70	%
$I_{DDHXTAL}$	HXTAL oscillator operating current	V_{DD}=3.3V, T_A=25°C	—	1	—	mA
$t_{SUHXTAL}$	HXTAL oscillator startup time	V_{DD}=3.3V, T_A=25°C	—	2	—	ms

Table 12. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}	Low Speed External oscillator (LXTAL) frequency	V_{DD}=V_{BAT}=3.3V	—	32.768	—	KHz
C_{LXTAL}	Recommended load capacitance on OSC32_IN and OSC32_OUT	—	—	—	15	pF
D_{LXTAL}	LXTAL oscillator duty cycle	—	30	50	70	%
$I_{DDLXTAL}$	LXTAL oscillator operating current	Low Drive	—	0.7	—	µA
		High Drive	—	1.3	—	
$t_{SULXTAL}$	LXTAL oscillator startup time	V_{DD}=V_{BAT}=3.3V	—	2	—	s

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4.8 Internal clock characteristics

Table 13. High speed internal clock (IRC8M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC8M}	High Speed Internal Oscillator (IRC8M) frequency	V_{DD}=3.3V	—	8	—	MHz
ACC_{IRC8M}	IRC8M oscillator Frequency accuracy, Factory-trimmed	V_{DD}=3.3V, T_A=-40°C ~+105°C	-4.0	—	+5.0	%
		V_{DD}=3.3V, T_A=0°C ~ +85°C	-2.0	—	+2.0	%
		V_{DD}=3.3V, T_A=25°C	-1.0	—	+1.0	%
	IRC8M oscillator Frequency accuracy, User trimming step	—	—	0.5	—	%
D_{IRC8M}	IRC8M oscillator duty cycle	V_{DD}=3.3V, f_{IRC8M}=8MHz	45	50	55	%
$I_{DDIRC8M}$	IRC8M oscillator operating current	V_{DD}=3.3V, f_{IRC8M}=8MHz	—	66	80	μA
$t_{SUIRC8M}$	IRC8M oscillator startup time	V_{DD}=3.3V, f_{IRC8M}=8MHz	—	2.5	4	us

Table 14. High speed internal clock (IRC48M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	V_{DD}=3.3V	—	48	—	MHz
ACC_{IRC48M}	IRC48M oscillator Frequency accuracy, Factory-trimmed	V_{DD}=3.3V, T_A=-40°C ~+105°C	-4.0	—	+5.0	%
		V_{DD}=3.3V, T_A=0°C ~ +85°C	-3.0	—	+3.0	%
		V_{DD}=3.3V, T_A=25°C	-2.0	—	+2.0	%
	IRC48M oscillator Frequency accuracy, User trimming step	—	—	0.12	—	%
D_{IRC48M}	IRC48M oscillator duty cycle	V_{DD}=3.3V, f_{IRC48M}=16MHz	45	50	55	%
$I_{DDIRC48M}$	IRC48M oscillator operating current	V_{DD}=3.3V, f_{IRC48M}=16MHz	—	240	300	μA
$t_{SUIRC48M}$	IRC48M oscillator startup time	V_{DD}=3.3V, f_{IRC48M}=16MHz	—	2.5	4	us

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Table 15. Low speed internal clock (IRC32K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC32K}	Low Speed Internal oscillator (IRC32K) frequency	V_{DD}=V_{BAT}=3.3V, T_A=-40°C ~ +85°C	20	40	45	KHz
$I_{DDIRC32K}$	IRC32K oscillator operating current	V_{DD}=V_{BAT}=3.3V, T_A=25°C	—	0.4	0.6	µA
$t_{SUIRC32K}$	IRC32K oscillator startup time	V_{DD}=V_{BAT}=3.3V, T_A=25°C	—	110	130	µs

4.9 PLL characteristics

Table 16. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock frequency	—	1	—	25	MHz
f_{PLLOUT}	PLL output clock frequency	—	16	—	120	MHz
f_{VCOOUT}	PLL VCO output clock frequency	—	32	—	240	MHz
t_{LOCK}	PLL lock time	—	—	—	300	µs
I_{DD}	Current consumption on VDD	VCO freq=240MHz	—	450	—	µA
I_{DDA}	Current consumption on VDDA	VCO freq=240MHz	—	680	—	µA
$Jitter_{PLL}$	Cycle to cycle Jitter	System clock	—	300	—	ps

Table 17. PLL2/3 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock frequency	—	1	—	25	MHz
f_{PLLOUT}	PLL output clock frequency	—	16	—	100	MHz
f_{VCOOUT}	PLL VCO output clock frequency	—	32	—	200	MHz
t_{LOCK}	PLL lock time	—	—	—	300	µs
I_{DD}	Current consumption on VDD	VCO freq=200MHz	—	290	—	µA
I_{DDA}	Current consumption on VDDA	VCO freq=200MHz	—	440	—	µA
$Jitter_{PLL}$	Cycle to cycle Jitter	System clock	—	300	—	ps

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4.10 Memory characteristics

Table 18. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	T_A=-40°C ~ +85°C	100	—	—	kcycles
t_{RET}	Data retention time	T_A=125°C	20	—	—	years
t_{PROG}	Word programming time	T_A=-40°C ~ +85°C	200	—	400	us
t_{ERASE}	Page erase time	T_A=-40°C ~ +85°C	60	100	450	ms
t_{MERASE}	Mass erase time	T_A=-40°C ~ +85°C	3.2	—	9.6	s

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4.11 GPIO characteristics

Table 19. I/O port characteristics

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage		V_{DD}=2.6V	—	—	0.97	V
			V_{DD}=3.3V	—	—	1.29	
			V_{DD}=3.6V	—	—	1.42	
	High Voltage tolerant IO Low level input voltage		V_{DD}=2.6V	—	—	0.98	V
			V_{DD}=3.3V	—	—	1.29	
			V_{DD}=3.6V	—	—	1.41	
V_{IH}	Standard IO High level input voltage		V_{DD}=2.6V	1.67	—	—	V
			V_{DD}=3.3V	1.97	—	—	
			V_{DD}=3.6V	2.09	—	—	
	High Voltage tolerant IO High level input voltage		V_{DD}=2.6V	1.64	—	—	V
			V_{DD}=3.3V	1.97	—	—	
			V_{DD}=3.6V	2.07	—	—	
V_{OL}	Low level output voltage		V_{DD}=2.6V, I_{IO}=8mA	—	—	0.17	V
			V_{DD}=3.3V, I_{IO}=8mA	—	—	0.15	
			V_{DD}=3.6V, I_{IO}=8mA	—	—	0.15	
			V_{DD}=2.6V, I_{IO}=20mA	—	—	0.49	
			V_{DD}=3.3V, I_{IO}=20mA	—	—	0.40	
			V_{DD}=3.6V, I_{IO}=20mA	—	—	0.40	
V_{OH}	High level output voltage		V_{DD}=2.6V, I_{IO}=8mA	2.40	—	—	V
			V_{DD}=3.3V, I_{IO}=8mA	3.11	—	—	
			V_{DD}=3.6V, I_{IO}=8mA	3.44	—	—	
			V_{DD}=2.6V, I_{IO}=20mA	2.02	—	—	
			V_{DD}=3.3V, I_{IO}=20mA	2.81	—	—	
			V_{DD}=3.6V, I_{IO}=20mA	3.15	—	—	
R_{PU}	Internal pull-up resistor	All pins	V_{IN}=V_{SS}	30	40	50	kΩ
		PA10	—	7.5	10	13.5	
R_{PD}	Internal pull-down resistor	All pins	V_{IN}=V_{DD}	30	40	50	kΩ
		PA10	—	7.5	10	13.5	

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4.12 ADC characteristics

Table 20. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	2.6	3.3	3.6	V
V_{ADCIN}	ADC input voltage range	—	0	—	V_{REF+}	V
f_{ADC}	ADC clock	—	0.1	—	40	MHz
f_S	Sampling rate	12-bit	0.007	—	2.86	MSPS
		10-bit	0.008	—	3.33	
		8-bit	0.01	—	4.00	
		6-bit	0.012	—	5.00	
V_{IN}	Analog input voltage	16 external;2 internal	0	—	V_{DDA}	V
V_{REF+}	Positive Reference Voltage	—	—	V_{DDA}	—	V
V_{REF-}	Negative Reference Voltage	—	—	0	—	V
R_{AIN}	External input impedance	See ***Equation 2***	—	—	32.9	kΩ
R_{ADC}	Input sampling switch resistance	—	—	—	0.55	kΩ
C_{ADC}	Input sampling capacitance	No pin/pad capacitance included	—	—	5.5	pF
t_{CAL}	Calibration time	f_{ADC}=40MHz	—	3.275	—	μs
t_s	Sampling time	f_{ADC}=40MHz	0.0375	—	5.99	μs
t_{CONV}	Total conversion time (including sampling time)	12-bit	—	14	—	1/ f_{ADC}
		10-bit	—	12	—	
		8-bit	—	10	—	
		6-bit	—	8	—	
t_{SU}	Startup time	—	—	—	1	μs

Equation 2: R_{AIN} max formula $R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above (Equation 2) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N=12 (from 12-bit resolution).

Table 21. ADC $R_{AIN\ max}$ for f_{ADC}=40MHz

T_s (cycles)	t_s (us)	$R_{AIN\ max}$ (KΩ)
1.5	0.0375	0.15
7.5	0.1875	2.96
13.5	0.3375	5.77
28.5	0.7125	12.8
41.5	1.0375	18.9
55.5	1.3875	25.4
71.5	1.7875	32.9
239.5	5.9875	N/A

Note: Guaranteed by design, not tested in production.

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Table 22. ADC dynamic accuracy at f_{ADC} = 30 MHz

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC}=30MHz	10.5	10.6	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA}=V_{REFP}=2.6V	65	65.6	—	dB
SNR	Signal-to-noise ratio	Input Frequency=110KHz	65.5	66	—	
THD	Total harmonic distortion	Temperature=25℃	-74	-76	—	

Table 23. ADC dynamic accuracy at f_{ADC} = 30 MHz

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC}=30MHz	10.7	10.8	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA}=V_{REFP}=3.3V	66.2	65.8	—	dB
SNR	Signal-to-noise ratio	Input Frequency=110KHz	66.8	67.4	—	
THD	Total harmonic distortion	Temperature=25℃	-71	-75	—	

Table 24. ADC dynamic accuracy at f_{ADC} = 36 MHz

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC}=36MHz	10.3	10.4	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA}=V_{REFP}=3.3V	63.8	64.4	—	dB
SNR	Signal-to-noise ratio	Input Frequency=110KHz	64.2	65	—	
THD	Total harmonic distortion	Temperature=25℃	-70	-72	—	

Table 25. ADC dynamic accuracy at f_{ADC} = 40 MHz

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC}=40MHz	9.9	10.0	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA}=V_{REFP}=3.3V	61.4	62	—	dB
SNR	Signal-to-noise ratio	Input Frequency=110KHz	62	62.4	—	
THD	Total harmonic distortion	Temperature=25℃	-68	-70	—	

Table 26. ADC static accuracy at f_{ADC} = 15 MHz

Symbol	Parameter	Test conditions	Typ	Max	Unit
Offset	Offset error	f_{ADC}=15MHz V_{DDA}=V_{REFP}=3.3V	±2	±3	LSB
DNL	Differential linearity error		±0.9	±1.2	
INL	Integral linearity error		±1.1	±1.5	

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4.13 DAC characteristics

Table 27. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	2.6	3.3	3.6	V
R_{LOAD}	Resistive load	Resistive load with buffer ON	5	—	—	kΩ
R_O	Impedance output	Impedance output with buffer OFF	—	—	15	kΩ
C_{LOAD}	Capacitive load	Capacitive load with buffer ON	—	—	50	pF
DAC_OUT_{min}	Lower DAC_OUT voltage	Lower DAC_OUT voltage with buffer ON	0.2	—	—	V
		Lower DAC_OUT voltage with buffer OFF	0.5	—	—	mV
DAC_OUT_{max}	Higher DAC_OUT voltage	Higher DAC_OUT voltage with buffer ON	—	—	V_{DDA}-0.2	V
		Higher DAC_OUT voltage with buffer OFF	—	—	V_{DDA}-1LSB	V
I_{DDA}	DC current consumption in quiescent mode with no load	Middle code on the input	—	—	500	μA
		Worst code on the input	—	—	560	
DNL	Differential non linearity	10-bit configuration	—	—	±0.5	LSB
		12-bit configuration	—	—	±2	
INL	Integral non linearity	10-bit configuration	—	—	±1	LSB
		12-bit configuration	—	—	±4	
Gain error	Gain error	—	—	±0.5	—	%
$T_{SETTLING}$	Settling time	C_{LOAD}≤50pF, R_{LOAD}≥5kΩ	—	0.5	1	μs
Update rate	Max frequency for a correct DAC_OUT change from code i to i±1LSB	C_{LOAD}≤50pF, R_{LOAD}≥5kΩ	—	—	4	MS/s
T_{WAKEUP}	Wakeup time from off state	C_{LOAD}≤50pF, R_{LOAD}≥5kΩ	—	1	2	μs
PSRR	Power supply rejection ratio	No R_{Load}, C_{LOAD}=50pF	—	-90	-75	dB

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4.14 SPI characteristics

Table 28. SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	30	MHz
$TSI_{K(H)}$	SCK clock high time	—	16	—	—	ns
$TSI_{K(L)}$	SCK clock low time	—	16	—	—	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	—	25	ns
$t_{H(MO)}$	Data output hold time	—	2	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	5	—	—	ns
$t_{H(MI)}$	Data input hold time	—	5	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	f_{PCLK}=54MHz	74	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	f_{PCLK}=54MHz	37	—	—	ns
$t_{A(SO)}$	Data output access time	f_{PCLK}=54MHz	0	—	55	ns
$t_{DIS(SO)}$	Data output disable time	—	3	—	10	ns
$t_{V(SO)}$	Data output valid time	—	—	—	25	ns
$t_{H(SO)}$	Data output hold time	—	15	—	—	ns
$t_{SU(SI)}$	Data input setup time	—	5	—	—	ns
$t_{H(SI)}$	Data input hold time	—	4	—	—	ns

4.15 I2C characteristics

Table 29. I2C characteristics

Symbol	Parameter	Conditions	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	—	0	100	0	1000	KHz
$TSI_{L(H)}$	SCL clock high time	—	4.0	—	0.6	—	ns
$TSI_{L(L)}$	SCL clock low time	—	4.7	—	1.3	—	ns

4.16 USART characteristics

Table 30. USART characteristics

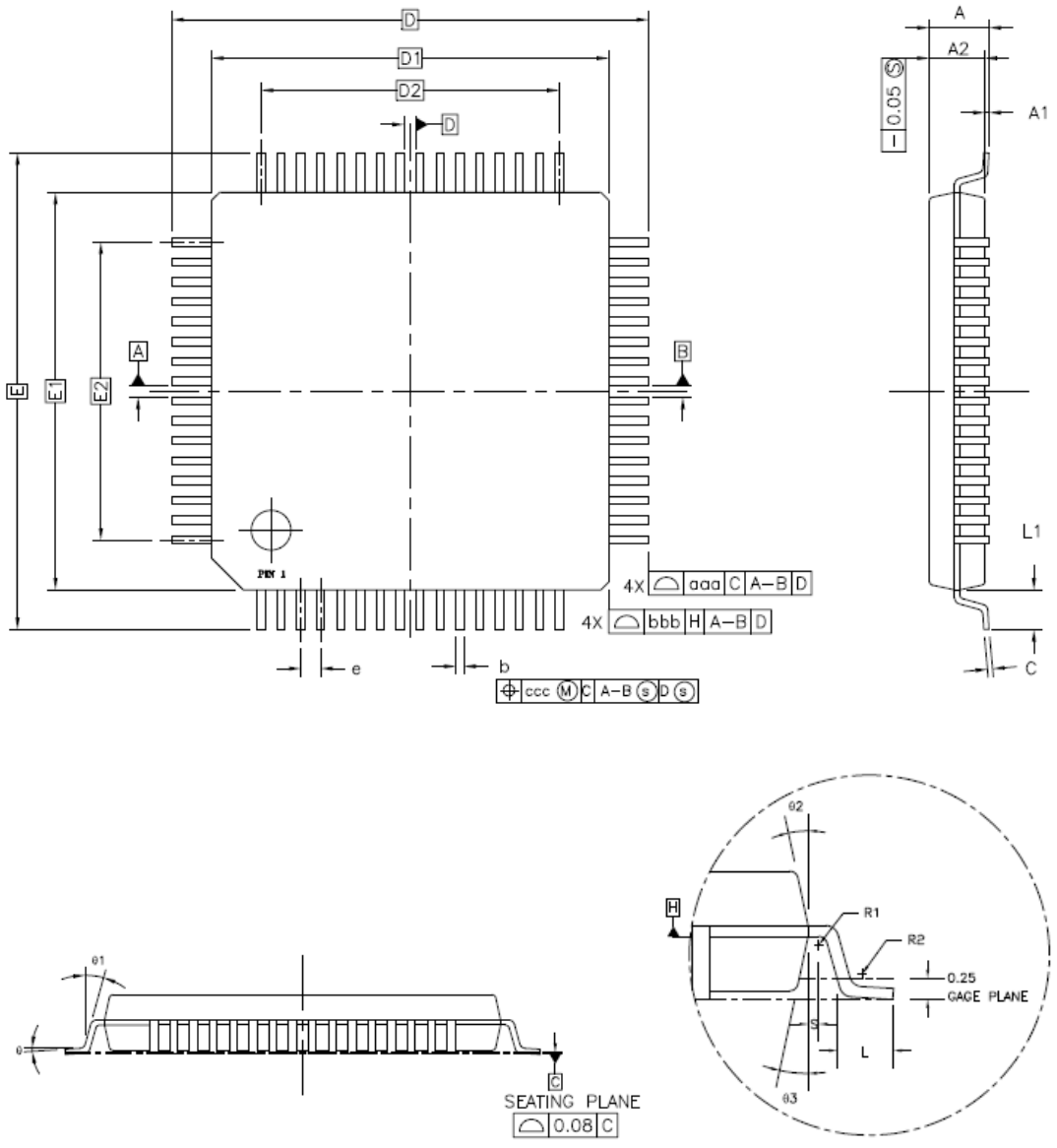
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	84	MHz
$TSI_{K(H)}$	SCK clock high time	—	5.5	—	—	ns
$TSI_{K(L)}$	SCK clock low time	—	5.5	—	—	ns

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5 Package information

5.1 LQFP package outline dimensions

Figure 7. LQFP package outline



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Table 31. LQFP package dimensions

Symbol	LQFP64			LQFP100			LQFP144		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	1.60	-	-	1.60
A1	0.05	-	0.15	0.05	-	0.15	0.05	-	0.15
A2	1.35	1.40	1.45	1.35	1.40	1.45	1.35	1.40	1.45
D	-	12.00	-	-	16.00	-	-	22.00	-
D1	-	10.00	-	-	14.00	-	-	20.00	-
E	-	12.00	-	-	16.00	-	-	22.00	-
E1	-	10.00	-	-	14.00	-	-	20.00	-
R1	0.08	-	-	0.08	-	-	0.08	-	-
R2	0.08	-	0.20	0.08	-	0.20	0.08	-	0.20
θ	0°	3.5°	7°	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-	0°	-	-
θ2	11°	12°	13°	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°	11°	12°	13°
c	0.09	-	0.20	0.09	-	0.20	0.09	-	0.20
L	0.45	0.60	0.75	0.45	0.60	0.75	0.45	0.60	0.75
L1	-	1.00	-	-	1.00	-	-	1.00	-
S	0.20	-	-	0.20	-	-	0.20	-	-
b	0.17	0.20	0.27	0.17	0.20	0.27	0.17	0.20	0.27
e	-	0.50	-	-	0.50	-	-	0.50	-
D2	-	7.50	-	-	12.00	-	-	17.50	-
E2	-	7.50	-	-	12.00	-	-	17.50	-
aaa	0.20			0.20			0.20		
bbb	0.20			0.20			0.20		
ccc	0.08			0.08			0.08		

(Original dimensions are in millimeters)

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6 Ordering Information

Table 32. Part ordering code for GD32F305xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32F305RBT6	128	LQFP64	Green	Industrial -40°C to +85°C
GD32F305RCT6	256	LQFP64	Green	Industrial -40°C to +85°C
GD32F305RET6	512	LQFP64	Green	Industrial -40°C to +85°C
GD32F305RGT6	1024	LQFP64	Green	Industrial -40°C to +85°C
GD32F305VCT6	256	LQFP100	Green	Industrial -40°C to +85°C
GD32F305VET6	512	LQFP100	Green	Industrial -40°C to +85°C
GD32F305VGT6	1024	LQFP100	Green	Industrial -40°C to +85°C
GD32F305ZCT6	256	LQFP144	Green	Industrial -40°C to +85°C
GD32F305ZET6	512	LQFP144	Green	Industrial -40°C to +85°C
GD32F305ZGT6	1024	LQFP144	Green	Industrial -40°C to +85°C

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7 Revision History

Table 33. Revision history

Revision No.	Description	Date
1.0	Initial Release	Mar.20, 2017

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