GigaDevice Semiconductor Inc.

GD32F205xx
ARM® Cortex®-M3 32-bit MCU

Datasheet

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1 Introduction

The GD32F205xx device belongs to the performance line of GD32 MCU Family. It is a new 32-bit general-purpose microcontroller based on the ARM® Cortex®-M3 RISC core with best cost-performance ratio in terms of processing capacity, reduced power consumption and peripheral set. The Cortex®-M3 is a next generation processor core which is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), SysTick timer and advanced debug support.

The GD32F205xx device incorporates the ARM® Cortex®-M3 32-bit processor core operating at 120 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 3072 KB on-chip Flash memory and 256 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to three 12-bit 2M SPS ADCs, two 12-bit DACs, up to ten general-purpose 16-bit timers, two 16-bit basic timers plus two 16-bit PWM advanced-control timers, as well as standard and advanced communication interfaces: up to three SPIs, three I2Cs, four USARTs and four UARTs, two I2Ss, two CANs, a SDIO, an USB device/host/OTG FS. Additional peripherals as TFT-LCD Interface (TLDI) and EXMC interface with SDRAM extension support are included.

The device operates from a 2.6 to 3.6V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization of power consumption, an especially important consideration in low power applications.

The above features make GD32F205xx devices suitable for a wide range of interconnection and advanced applications, especially in areas such as industrial control, consumer and handheld equipment, embedded modules, human machine interface, security and alarm systems, automotive navigation and so on.

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2 Device overview

2.1 Device information

Table 1. GD32F205xx devices features and peripheral list

Part Number		GD32F205xx							
		RC	RE	RG	RK	VC	VE	VG	VK
Flash	Code Area (KB)	256	512	384	384	256	512	384	384
	Data Area (KB)	0	0	640	2688	0	0	640	2688
	Total (KB)	256	512	1024	3072	256	512	1024	3072
SRAM (KB)		128	128	256	256	128	128	256	256
Timers	GPTM	10	10	10	10	10	10	10	10
	Advanced TM	2	2	2	2	2	2	2	2
	SysTick	1	1	1	1	1	1	1	1
	Basic TM	2	2	2	2	2	2	2	2
	Watchdog	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1
Connectivity	USART+UART	4+2	4+2	4+2	4+2	4+4	4+4	4+4	4+4
	I2C	3	3	3	3	3	3	3	3
	SPI/I2S	3/2	3/2	3/2	3/2	3/2	3/2	3/2	3/2
	SDIO	1	1	1	1	1	1	1	1
	CAN 2.0B	2	2	2	2	2	2	2	2
	USB OTG FS	1	1	1	1	1	1	1	1
	TFT-LCD	0	0	0	0	1	1	1	1
GPIO		51	51	51	51	82	82	82	82
EXMC/SDRAM		0/0	0/0	0/0	0/0	1/0	1/0	1/0	1/0
ADC Unit (CHs)		3(16)	3(16)	3(16)	3(16)	3(16)	3(16)	3(16)	3(16)
DAC		2	2	2	2	2	2	2	2
Package		LQFP64				LQFP100			

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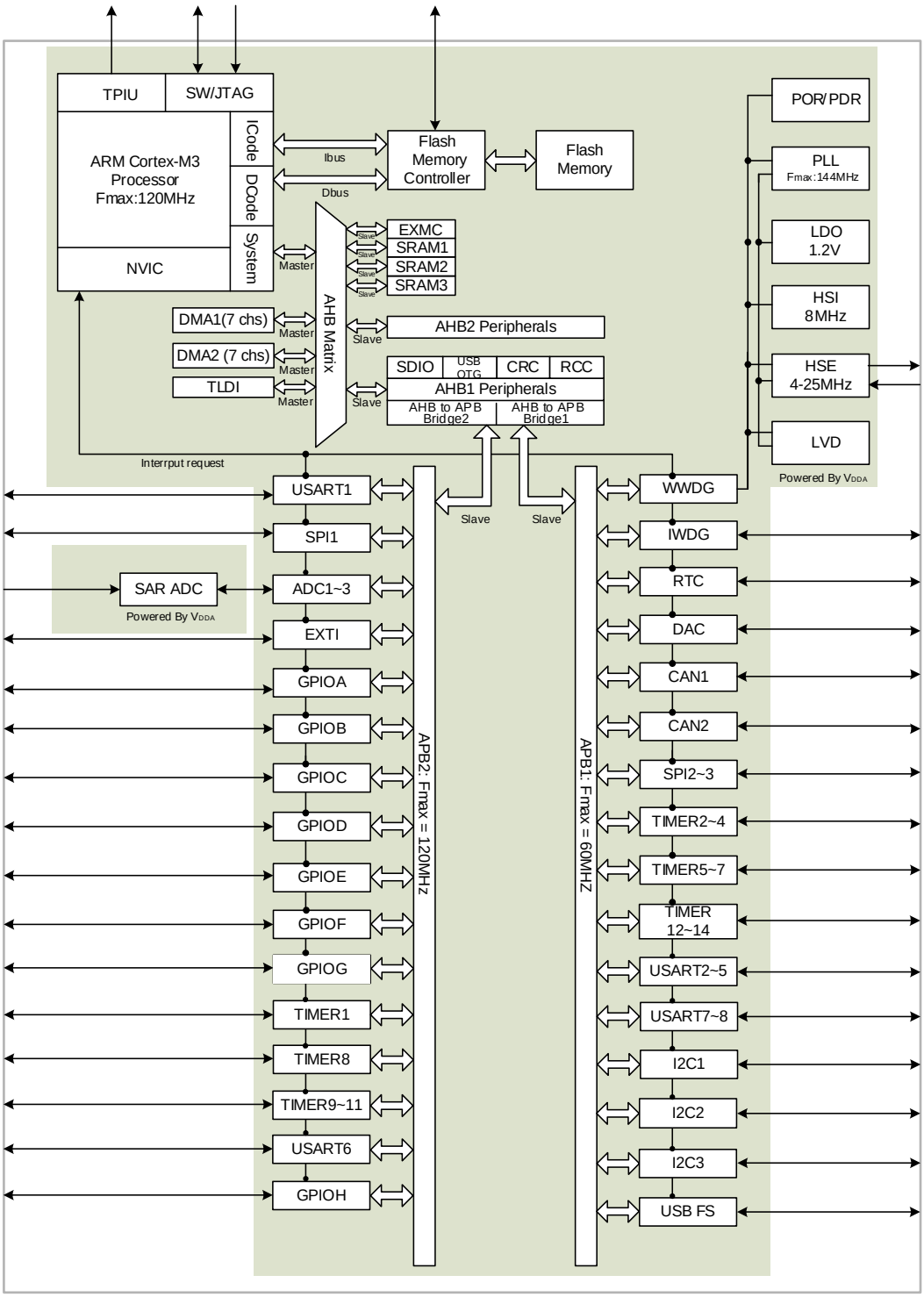
Table 1. GD32F205xx devices features and peripheral list (continued)

Part Number		GD32F205xx			
		ZC	ZE	ZG	ZK
Flash	Code Area (KB)	256	512	384	384
	Data Area (KB)	0	0	640	2688
	Total (KB)	256	512	1024	3072
SRAM (KB)		128	128	256	256
Timers	GPTM	10	10	10	10
	Advanced TM	2	2	2	2
	SysTick	1	1	1	1
	Basic TM	2	2	2	2
	Watchdog	2	2	2	2
	RTC	1	1	1	1
Connectivity	USART+UART	4+4	4+4	4+4	4+4
	I2C	3	3	3	3
	SPI/I2S	3/2	3/2	3/2	3/2
	SDIO	1	1	1	1
	CAN 2.0B	2	2	2	2
	USB OTG FS	1	1	1	1
	TFT-LCD	1	1	1	1
GPIO		114	114	114	114
EXMC/SDRAM		1/1	1/1	1/1	1/1
ADC Unit (CHs)		3(24)	3(24)	3(24)	3(24)
DAC		2	2	2	2
Package		LQFP144			

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2.2 Block diagram

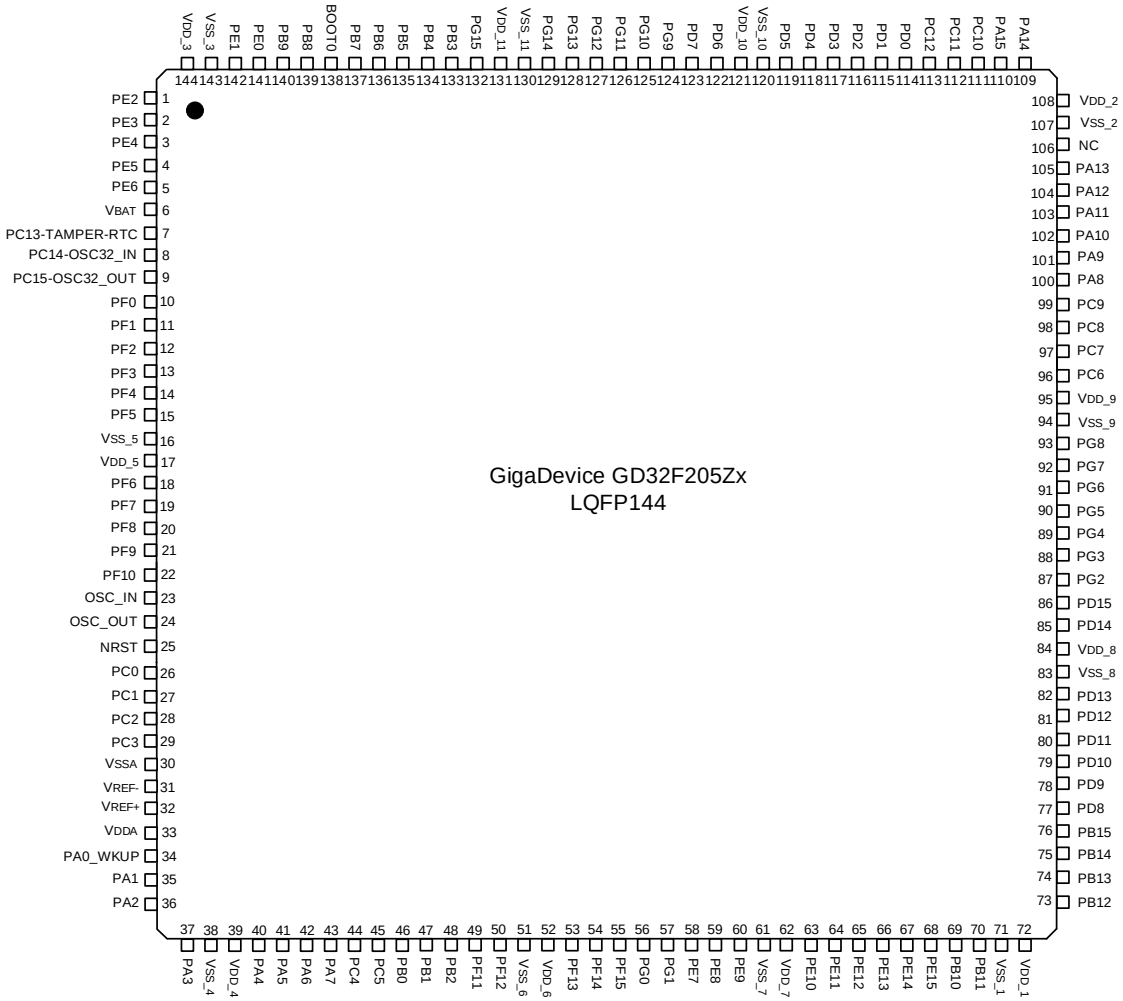
Figure 1. GD32F205xx block diagram



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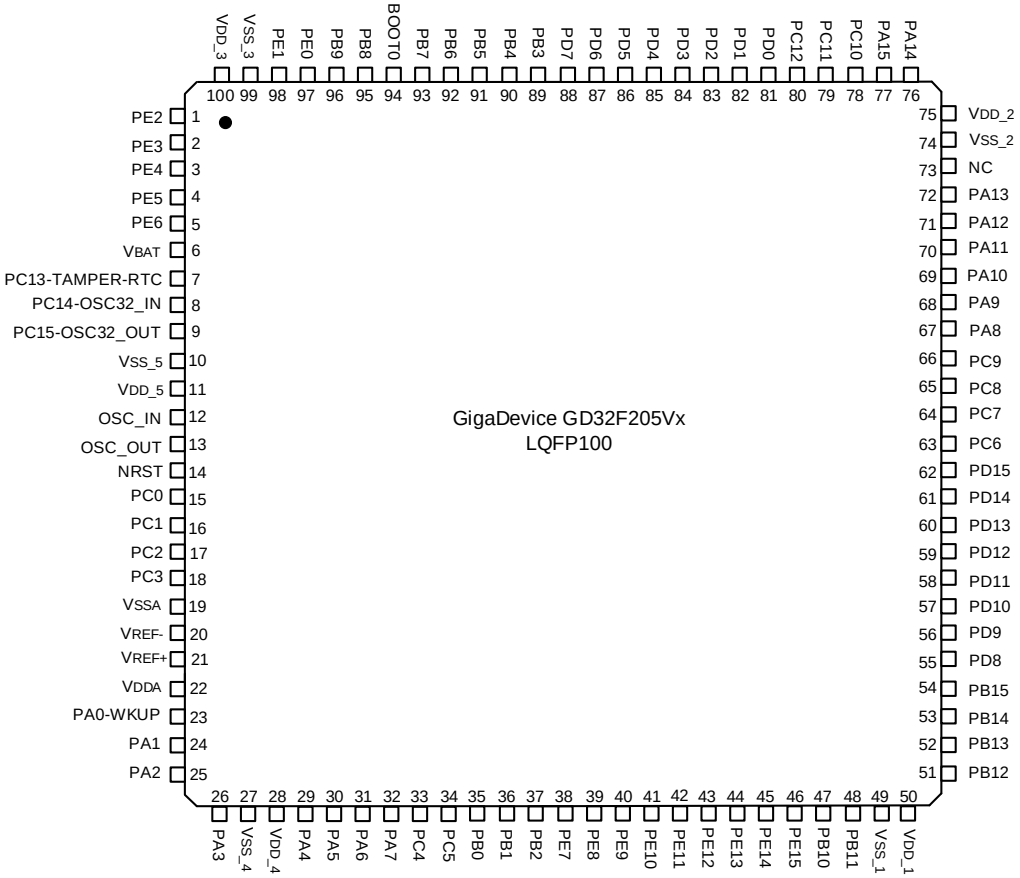
2.3 Pinouts and pin assignment

Figure 2. GD32F205Zx LQFP144 pinouts



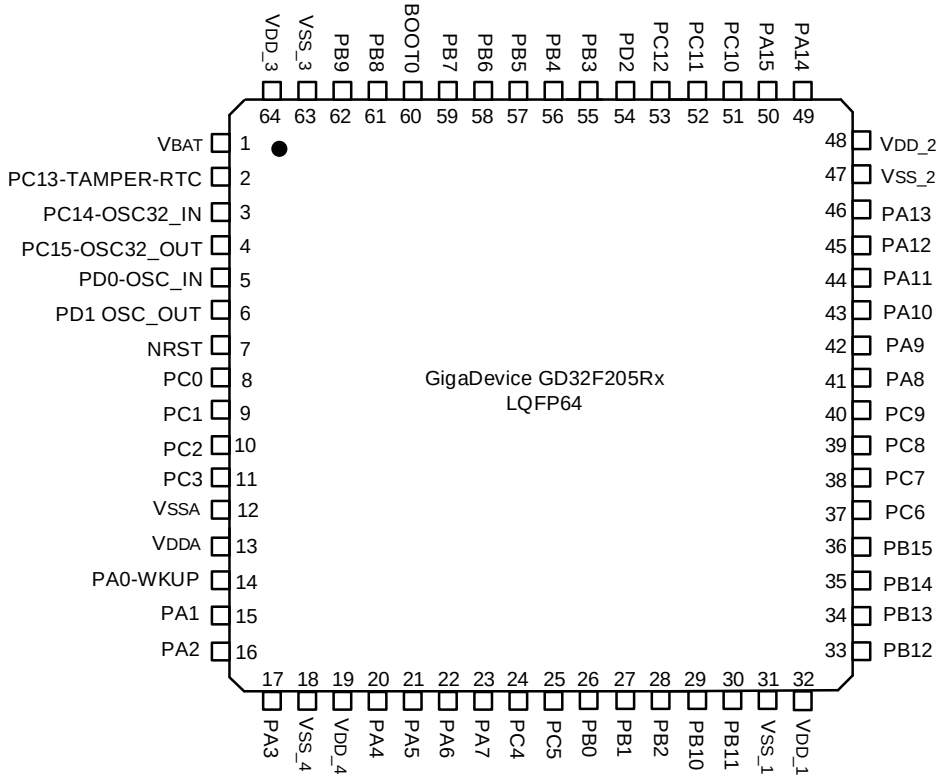
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Figure 3. GD32F205Vx LQFP100 pinouts



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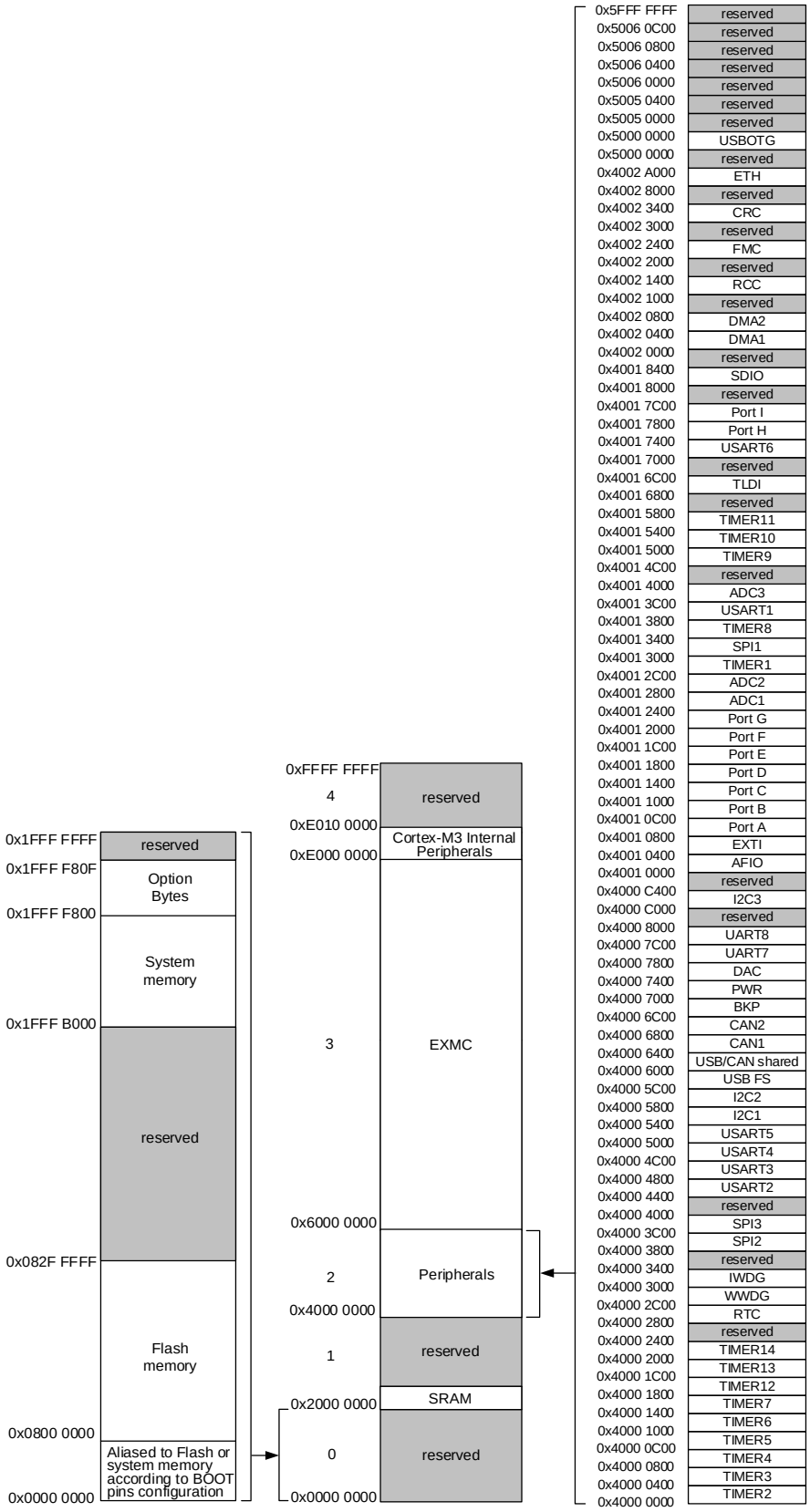
Figure 4. GD32F205Rx LQFP64 pinouts



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2.4 Memory map

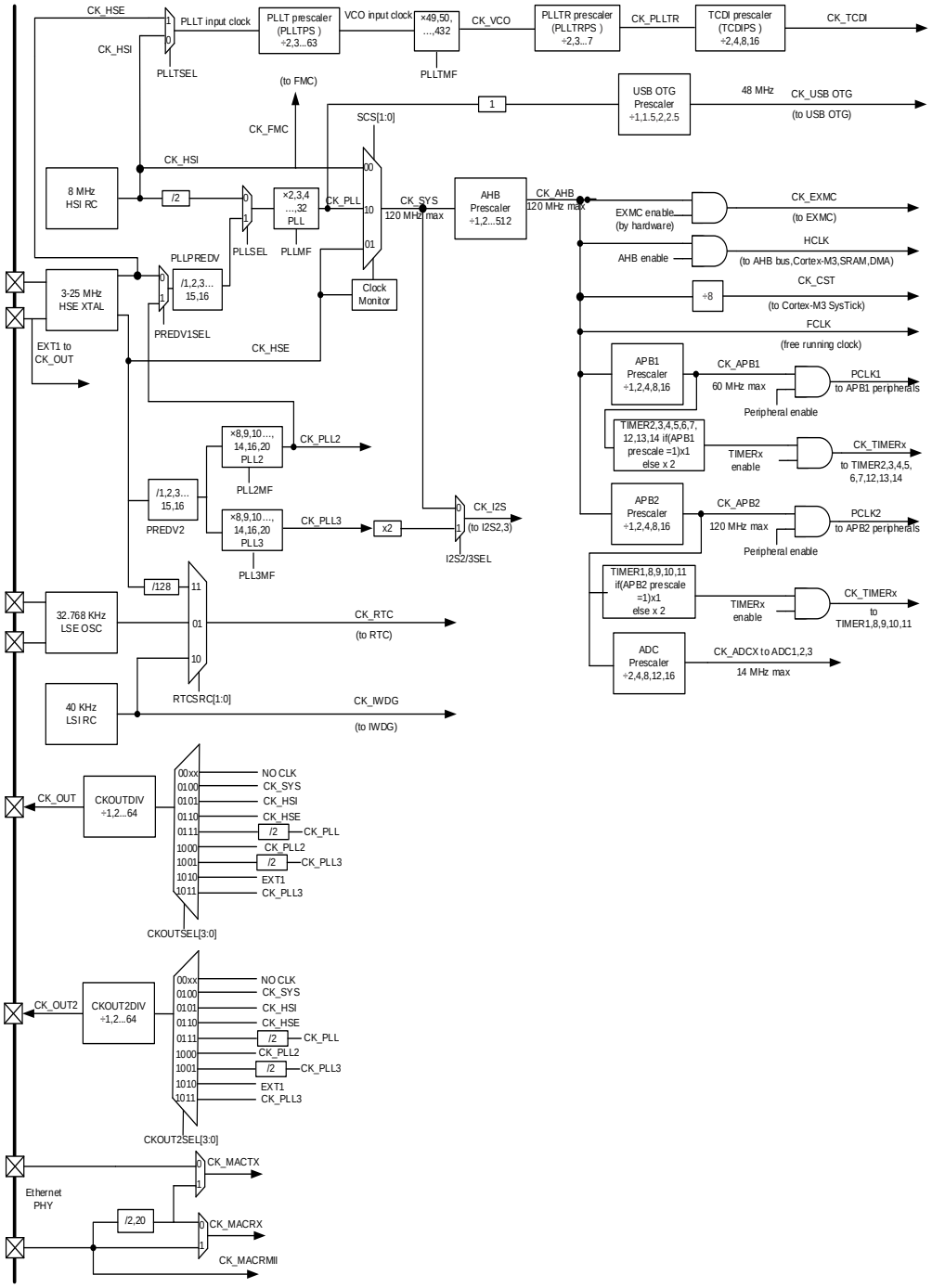
Figure 5. GD32F205xx memory map



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2.5 Clock tree

Figure 6. GD32F205xx clock tree



Legend:

HSE = High speed external clock

HSI = High speed internal clock

LSE = Low speed external clock

LSI = Low speed internal clock

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2.6 Pin definitions

Table 2. GD32F205xx pin definitions

Pin Name	Pins			Pin Type(1)	I/O(2) Level	Functions description
	LQFP144	LQFP100	LQFP64			
PE2	1	1	-	I/O	5VT	Default: PE2 Alternate: TRACECK, EXMC_A23
PE3	2	2	-	I/O	5VT	Default: PE3 Alternate: TRACED0, EXMC_A19
PE4	3	3	-	I/O	5VT	Default: PE4 Alternate:TRACED1, EXMC_A20 Remap: LCD_B0
PE5	4	4	-	I/O	5VT	Default: PE5 Alternate:TRACED2, EXMC_A21 Remap: TM9_CH1, LCD_G0
PE6	5	5	-	I/O	5VT	Default: PE6 Alternate:TRACED3, EXMC_A22 Remap: TM9_CH2, LCD_G1
V_{BAT}	6	6	1	P		Default: V_{BAT}
PC13-TAMPER-RTC	7	7	2	I/O		Default: PC13 Alternate: TAMPER, RTC
PC14-OSC32_IN	8	8	3	I/O		Default: PC14 Alternate: OSC32_IN
PC15-OSC32_OUT	9	9	4	I/O		Default: PC15 Alternate: OSC32_OUT
PF0	10	-	-	I/O	5VT	Default: PF0 Alternate: EXMC_A0 Remap: I2C2_SDA
PF1	11	-	-	I/O	5VT	Default: PF1 Alternate: EXMC_A1 Remap: I2C2_SCL
PF2	12	-	-	I/O	5VT	Default: PF2 Alternate: EXMC_A2 Remap: I2C2_SMBA
PF3	13	-	-	I/O	5VT	Default: PF3 Alternate: EXMC_A3 Remap: ADC3_IN9
PF4	14	-	-	I/O	5VT	Default: PF4 Alternate: EXMC_A4 Remap: ADC3_IN14
PF5	15	-	-	I/O	5VT	Default: PF5 Alternate: EXMC_A5

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Pin Name	Pins			Pin Type(1)	I/O(2) Level	Functions description
	LQFP144	LQFP100	LQFP64			
						Remap: ADC3_IN15
V_{SS_5}	16	10	-	P		Default: V_{SS_5}
V_{DD_5}	17	11	-	P		Default: V_{DD_5}
PF6	18	-	-	I/O		Default: PF6 Alternate: ADC3_IN4, EXMC_NIORD Remap: TM10_CH1, UART7_RX
PF7	19	-	-	I/O		Default: PF7 Alternate: ADC3_IN5, EXMC_NREG Remap: TM11_CH1, UART7_TX
PF8	20	-	-	I/O		Default: PF8 Alternate: ADC3_IN6, EXMC_NIOWR Remap: TM13_CH1
PF9	21	-	-	I/O		Default: PF9 Alternate: ADC3_IN7, EXMC_CD Remap: TM14_CH1
PF10	22	-	-	I/O		Default: PF10 Alternate: ADC3_IN8, EXMC_INTR Remap: LCD_DE
PH0-OSC_IN	23	12	5	I		Default: OSC_IN Remap: PD0, PH0
PH1-OSC_OUT	24	13	6	O		Default: OSC_OUT Remap: PD1, PH1
NRST	25	14	7	I/O		Default: NRST
PC0	26	15	8	I/O		Default: PC0 Alternate: ADC_IN10 Remap: EXMC_SDNWE
PC1	27	16	9	I/O		Default: PC1 Alternate: ADC_IN11
PC2	28	17	10	I/O		Default: PC2 Alternate: ADC_IN12 Remap: EXMC_SDNE0, SPI2_MISO
PC3	29	18	11	I/O		Default: PC3 Alternate: ADC_IN13 Remap: EXMC_SDCKE0, SPI2_MOSI, I2S2_SD
V_{SSA}	30	19	12	P		Default: V_{SSA}
V_{REF-}	31	20	-	P		Default: V_{REF-}
V_{REF+}	32	21	-	P		Default: V_{REF+}
V_{DDA}	33	22	13	P		Default: V_{DDA}
PA0-WKUP	34	23	14	I/O		Default: PA0 Alternate: WKUP, USART2_CTS, ADC_IN0, TM2_CH1_ETR, TM5_CH1, TM8_ETR Remap: UART4_TX

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Pin Name	Pins			Pin Type(1)	I/O(2) Level	Functions description
	LQFP144	LQFP100	LQFP64			
PA1	35	24	15	I/O		Default: PA1 Alternate: USART2_RTS, ADC_IN1, TM2_CH2, TM5_CH2 Remap: UART4_RX
PA2	36	25	16	I/O		Default: PA2 Alternate: USART2_TX, ADC_IN2, TM2_CH3, TM5_CH3, TM9_CH1, SPI1_IO3
PA3	37	26	17	I/O		Default: PA3 Alternate: USART2_RX, ADC_IN3, TM2_CH4, TM5_CH4, TM9_CH2, SPI1_IO4 Remap: LCD_B5
V_{SS_4}	38	27	18	P		Default: V_{SS_4}
V_{DD_4}	39	28	19	P		Default: V_{DD_4}
PA4	40	29	20	I/O		Default: PA4 Alternate: SPI1_NSS, USART2_CK, DAC_OUT1, ADC12_IN4 Remap: SPI3_NSS, I2S3_WS, LCD_VSYNC
PA5	41	30	21	I/O		Default: PA5 Alternate: SPI1_SCK, ADC12_IN5, DAC_OUT2 Remap: TM2_CH1_ETR, TM8_CH1N
PA6	42	31	22	I/O		Default: PA6 Alternate: SPI1_MISO, ADC12_IN6, TM3_CH1, TM8_BKIN, TM13_CH1 Remap: TM1_BKIN, LCD_G2
PA7	43	32	23	I/O		Default: PA7 Alternate: SPI1_MOSI, ADC12_IN7, TM3_CH2, TM8_CH1N, TM14_CH1 Remap: TM1_CH1N
PC4	44	33	24	I/O		Default: PC4 Alternate: ADC12_IN14
PC5	45	34	25	I/O		Default: PC5 Alternate: ADC12_IN15
PB0	46	35	26	I/O		Default: PB0 Alternate: ADC12_IN8, TM3_CH3, TM8_CH2N Remap: TM1_CH2N, LCD_R3
PB1	47	36	27	I/O		Default: PB1 Alternate: ADC12_IN9, TM3_CH4, TM8_CH3N Remap: TM1_CH3N, LCD_R6
PB2	48	37	28	I/O	5VT	Default: PB2, BOOT1
PF11	49	-	-	I/O	5VT	Default: PF11 Alternate: EXMC_NIOS16, EXMC_SDNRAS
PF12	50	-	-	I/O	5VT	Default: PF12 Alternate: EXMC_A6
V_{SS_6}	51	-	-	P		Default: V_{SS_6}
V_{DD_6}	52	-	-	P		Default: V_{DD_6}
PF13	53	-	-	I/O	5VT	Default: PF13 Alternate: EXMC_A7

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Pin Name	Pins			Pin Type(1)	I/O(2) Level	Functions description
	LQFP144	LQFP100	LQFP64			
PF14	54	-	-	I/O	5VT	Default: PF14 Alternate: EXMC_A8
PF15	55	-	-	I/O	5VT	Default: PF15 Alternate: EXMC_A9
PG0	56	-	-	I/O	5VT	Default: PG0 Alternate: EXMC_A10
PG1	57	-	-	I/O	5VT	Default: PG1 Alternate: EXMC_A11
PE7	58	38	-	I/O	5VT	Default: PE7 Alternate: EXMC_D4, UART7_RX Remap: TM1_ETR
PE8	59	39	-	I/O	5VT	Default: PE8 Alternate: EXMC_D5, UART7_TX Remap: TM1_CH1N
PE9	60	40	-	I/O	5VT	Default: PE9 Alternate: EXMC_D6 Remap: TM1_CH1
V_{SS_7}	61	-	-	P		Default: V_{SS_7}
V_{DD_7}	62	-	-	P		Default: V_{DD_7}
PE10	63	41	-	I/O	5VT	Default: PE10 Alternate: EXMC_D7 Remap: TM1_CH2N
PE11	64	42	-	I/O	5VT	Default: PE11 Alternate: EXMC_D8 Remap: TM1_CH2, LCD_G3
PE12	65	43	-	I/O	5VT	Default: PE12 Alternate: EXMC_D9 Remap: TM1_CH3N, LCD_B4
PE13	66	44	-	I/O	5VT	Default: PE13 Alternate: EXMC_D10 Remap: TM1_CH3, LCD_DE
PE14	67	45	-	I/O	5VT	Default: PE14 Alternate: EXMC_D11 Remap: TM1_CH4, LCD_CLK
PE15	68	46	-	I/O	5VT	Default: PE15 Alternate: EXMC_D12 Remap: TM1_BKIN, LCD_R7
PB10	69	47	29	I/O	5VT	Default: PB10 Alternate: I2C2_SCL, USART3_TX Remap: TM2_CH3, LCD_G4, SPI2_SCK, I2S2_CK
PB11	70	48	30	I/O	5VT	Default: PB11 Alternate: I2C2_SDA, USART3_RX Remap: TM2_CH4, LCD_G5

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Pin Name	Pins			Pin Type(1)	I/O(2) Level	Functions description
	LQFP144	LQFP100	LQFP64			
V_{SS_1}	71	49	31	P		Default: V_{SS_1}
V_{DD_1}	72	50	32	P		Default: V_{DD_1}
PB12	73	51	33	I/O	5VT	Default: PB12 Alternate: SPI2_NSS, I2C2_SMBA, USART3_CK, TM1_BKIN, I2S2_WS, CAN2_RX
PB13	74	52	34	I/O	5VT	Default: PB13 Alternate: SPI2_SCK, USART3_CTS, TM1_CH1N, I2S2_CK, CAN2_TX
PB14	75	53	35	I/O	5VT	Default: PB14 Alternate: SPI2_MISO, USART3_RTS, TM1_CH2N, TM12_CH1
PB15	76	54	36	I/O	5VT	Default: PB15 Alternate: SPI2_MOSI, TM1_CH3N, I2S2_SD, TM12_CH2
PD8	77	55	-	I/O	5VT	Default: PD8 Alternate: EXMC_D13 Remap: USART3_TX
PD9	78	56	-	I/O	5VT	Default: PD9 Alternate: EXMC_D14 Remap: USART3_RX
PD10	79	57	-	I/O	5VT	Default: PD10 Alternate: EXMC_D15 Remap: USART3_CK, LCD_B3
PD11	80	58	-	I/O	5VT	Default: PD11 Alternate: EXMC_A16 Remap: USART3_CTS
PD12	81	59	-	I/O	5VT	Default: PD12 Alternate: EXMC_A17 Remap: TM4_CH1, USART3_RTS
PD13	82	60	-	I/O	5VT	Default: PD13 Alternate: EXMC_A18 Remap: TM4_CH2
V_{SS_8}	83	-	-	P		Default: V_{SS_8}
V_{DD_8}	84	-	-	P		Default: V_{DD_8}
PD14	85	61	-	I/O	5VT	Default: PD14 Alternate: EXMC_D0 Remap: TM4_CH3
PD15	86	62	-	I/O	5VT	Default: PD15 Alternate: EXMC_D1 Remap: TM4_CH4
PG2	87	-	-	I/O	5VT	Default: PG2 Alternate: EXMC_A12
PG3	88	-	-	I/O	5VT	Default: PG3 Alternate: EXMC_A13
PG4	89	-	-	I/O	5VT	Default: PG4 Alternate: EXMC_A14, EXMC_BA0

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Pin Name	Pins			Pin Type(1)	I/O(2) Level	Functions description
	LQFP144	LQFP100	LQFP64			
PG5	90	-	-	I/O	5VT	Default: PG5 Alternate: EXMC_A15, EXMC_BA1
PG6	91	-	-	I/O	5VT	Default: PG6 Alternate: EXMC_INT2 Remap:LCD_R7
PG7	92	-	-	I/O	5VT	Default: PG7 Alternate: EXMC_INT3 Remap: USART6_CK, LCD_CLK
PG8	93	-	-	I/O	5VT	Default: PG8 Alternate: EXMC_SDCLK, USART6_RTS
V_{SS_9}	94	-	-	P		Default: V_{SS_9}
V_{DD_9}	95	-	-	P		Default: V_{DD_9}
PC6	96	63	37	I/O	5VT	Default: PC6 Alternate: I2S2_MCK; TM8_CH1, SDIO_D6, USART6_TX Remap: TM3_CH1, LCD_HSYNC
PC7	97	64	38	I/O	5VT	Default: PC7 Alternate: I2S3_MCK; TM8_CH2, SDIO_D7, USART6_RX Remap: TM3_CH2, LCD_G6
PC8	98	65	39	I/O	5VT	Default: PC8 Alternate: TM8_CH3, SDIO_D0, USART6_CK Remap: TM3_CH3
PC9	99	66	40	I/O	5VT	Default: PC9 Alternate: TM8_CH4, SDIO_D, MCO2 Remap: TM3_CH4, I2C3_SDA
PA8	100	67	41	I/O	5VT	Default: PA8 Alternate: USART1_CK, TM1_CH1, MCO, VCORE, OTG_FS_SOF Remap: LCD_R6, I2C3_SCL
PA9	101	68	42	I/O	5VT	Default: PA9 Alternate: USART1_TX, TM1_CH2, OTG_FS_VBUS Remap: I2C3_SMBAI
PA10	102	69	43	I/O	5VT	Default: PA10 Alternate: USART1_RX, TM1_CH3, OTG_FS_ID
PA11	103	70	44	I/O	5VT	Default: PA11 Alternate: USART1_CTS, CANRX, OTG_FS_DM, USBDM, TM1_CH4 Remap: LCD_R4
PA12	104	71	45	I/O	5VT	Default: PA12 Alternate: USART1_RTS, OTG_FS_DP, CAN1_TX, TM1_ETR,USBDP Remap: LCD_R5
PA13	105	72	46	I/O	5VT	Default: JTMS, SWDIO Remap: PA13
NC	106	73	-			-
V_{SS_2}	107	74	47	P		Default: V_{SS_2}
V_{DD_2}	108	75	48	P		Default: V_{DD_2}

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Pin Name	Pins			Pin Type(1)	I/O(2) Level	Functions description
	LQFP144	LQFP100	LQFP64			
PA14	109	76	49	I/O	5VT	Default: JTCK, SWCLK Remap: PA14
PA15	110	77	50	I/O	5VT	Default: JTDI Alternate: SPI3_NSS, I2S3_WS Remap: TM2_CH1_ETR, PA15, SPI1_NSS
PC10	111	78	51	I/O	5VT	Default: PC10 Alternate: UART4_TX, SDIO_D2 Remap: USART3_TX, SPI3_SCK, I2S3_CK, LCD_R2
PC11	112	79	52	I/O	5VT	Default: PC11 Alternate: UART4_RX, SDIO_D3 Remap: USART3_RX, SPI3_MISO
PC12	113	80	53	I/O	5VT	Default: PC12 Alternate: UART5_TX, SDIO_CK Remap: USART3_CK, SPI3_MOSI, I2S3_SD
PD0	114	81	5	I/O	5VT	Default: PD0 Alternate: EXMC_D2 Remap: CAN1_RX, OSC_IN
PD1	115	82	6	I/O	5VT	Default: PD1 Alternate: EXMC_D3 Remap: CAN1_TX, OSC_OUT
PD2	116	83	54	I/O	5VT	Default: PD2 Alternate: TM3_ETR, UART5_RX, SDIO_CMD
PD3	117	84	-	I/O	5VT	Default: PD3 Alternate: EXMC_CLK Remap: USART2_CTS, LCD_G7, SPI2_SCK, I2S2_CK
PD4	118	85	-	I/O	5VT	Default: PD4 Alternate: EXMC_NOE Remap: USART2_RTS
PD5	119	86	-	I/O	5VT	Default: PD5 Alternate: EXMC_NWE Remap: USART2_TX
V_{SS_10}	120	-	-			Default: V_{SS_10}
V_{DD_10}	121	-	-			Default: V_{DD_10}
PD6	122	87	-	I/O	5VT	Default: PD6 Alternate: EXMC_NWAIT Remap: USART2_RX, LCD_B2, SPI3_MOSI, I2S3_SD
PD7	123	88	-	I/O	5VT	Default: PD7 Alternate: EXMC_NE1, EXMC_NCE2 Remap: USART2_CK
PG9	124	-	-	I/O	5VT	Default: PG9 Alternate: EXMC_NE2, EXMC_NCE3 Remap: USART6_RX
PG10	125	-	-	I/O	5VT	Default: PG10

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Pin Name	Pins			Pin Type(1)	I/O(2) Level	Functions description
	LQFP144	LQFP100	LQFP64			
						Alternate: EXMC_NCE4_1, EXMC_NE3 Remap: LCD_G3, LCD_B2
PG11	126	-	-	I/O	5VT	Default: PG11 Alternate: EXMC_NCE4_2 Remap: LCD_B3
PG12	127	-	-	I/O	5VT	Default: PG12 Alternate: EXMC_NE4 Remap: USART6_RTS, LCD_B4, LCD_B1
PG13	128	-	-	I/O	5VT	Default: PG13 Alternate: EXMC_A24 Remap: USART6_CTS
PG14	129	-	-	I/O	5VT	Default: PG14 Alternate: EXMC_A25 Remap: USART6_TX
V_{SS_11}	130	-	-	P		Default: V_{SS_10}
V_{DD_11}	131	-	-	P		Default: V_{DD_10}
PG15	132	-	-	I/O	5VT	Default: PG15 Alternate: EXMC_SDNCAS, USART6_CTS
PB3	133	89	55	I/O	5VT	Default: JTDO Alternate:SPI3_SCK, I2S3_CK Remap: PB3, TRACESWO, TM2_CH2, SPI1_SCK
PB4	134	90	56	I/O	5VT	Default: NJTRST Alternate: SPI3_MISO Remap: TM3_CH1, PB4, SPI1_MISO
PB5	135	91	57	I/O		Default: PB5 Alternate: I2C1_SMBA, SPI3_MOSI, I2S3_SD Remap: TM3_CH2, SPI1_MOSI, CAN2_RX, EXMC_SDCKE1
PB6	136	92	58	I/O	5VT	Default: PB6 Alternate: I2C1_SCL, TM4_CH1 Remap: USART1_TX, CAN2_TX, EXMC_SDNE1, SPI1_IO3
PB7	137	93	59	I/O	5VT	Default: PB7 Alternate: I2C1_SDA , TM4_CH2, EXMC_NADV Remap: USART1_RX, SPI1_IO4
BOOT0	138	94	60	I		Default: BOOT0
PB8	139	95	61	I/O	5VT	Default: PB8 Alternate: TM4_CH3, TM10_CH1, SDIO_D4 Remap: I2C1_SCL, CAN1_RX, LCD_B6
PB9	140	96	62	I/O	5VT	Default: PB9 Alternate: TM4_CH4, TM11_CH1, SDIO_D5 Remap: I2C1_SDA, CAN1_TX, LCD_B7, SPI2_NSS, I2S2_WS
PE0	141	97	-	I/O	5VT	Default: PE0 Alternate: TM4_ETR, EXMC_NBL0, UART8_RX
PE1	142	98	-	I/O	5VT	Default: PE1

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Pin Name	Pins			Pin Type(1)	I/O(2) Level	Functions description
	LQFP144	LQFP100	LQFP64			
						Alternate: EXMC_NBL1, UART8_TX
V_{SS_3}	143	99	63	P		Default: V_{SS_3}
V_{DD_3}	144	100	64	P		Default: V_{DD_3}

Notes:

1. Type: I = input, O = output, P = power.
2. I/O Level: 5VT = 5 V tolerant.

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3 Functional description

3.1 ARM® Cortex®-M3 core

The Cortex®-M3 processor is the latest generation of ARM® processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

- 32-bit ARM® Cortex®-M3 processor core
- Up to 120 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M3:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Memory Protection Unit (MPU)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

3.2 On-chip memory

- Up to 3072 Kbytes of Flash memory, including code Flash and data Flash
- Up to 256 Kbytes of SRAM

The ARM® Cortex®-M3 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 3072 Kbytes of inner Flash at most, which includes code Flash and data Flash is available for storing programs and data, and accessed (R/W) at CPU clock speed with zero wait states. Up to 256 Kbytes of inner SRAM is composed of SRAM1, SRAM2, and SRAM3 that can be accessed at same time. The Figure of GD32F205xx memory map shows the memory map of the GD32F205xx series of devices, including Flash, SRAM, peripheral, and other pre-defined regions.

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3.3 Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB and two APB domains is 72 MHz. See Figure 9 for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 2.6 V and down to 1.8V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: 1.8 to 3.6 V, power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART1, USART2, CAN2, USB OTG FS in device mode. It also can be used to transfer and update the Flash memory code, the data and the vector table sections. In default condition, boot from bank 1 of Flash memory is selected. It also supports to boot from bank 2 of Flash memory by setting a bit in option bytes.

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3.5 Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are Sleep mode, Deep-sleep mode, and Standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In Deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (HSI, HSE) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the Deep-sleep mode including the 16 external lines, the RTC alarm, the LVD output, and USB wakeup. When exiting the Deep-sleep mode, the HSI is selected as the system clock.
- **Standby** mode
  In Standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of HSI, HSE and PLL are disabled. The contents of SRAM and registers (except Backup Registers) are lost. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC alarm, the IWDG reset, and the rising edge on WKUP pin.

3.6 Analog to digital converter (ADC)

- 12-bit SAR ADC engine with up to 2M SPS conversion rate
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Conversion range: V_{SSA} to V_{DDA} (2.6 to 3.6 V)
- Temperature sensor

Up to three 12-bit 2M SPS multi-channel ADC are integrated in the device. It is a total of up to 16 multiplexed external channels with 2 internal channels for temperature sensor and voltage reference measurement. The conversion range is between 2.6 V < V_{DDA} < 3.6 V. An on-chip 16-bit hardware oversample scheme improves performances while off-loading the related computational burden from the MCU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block of analog inputs also can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced usages.

The ADC can be triggered from the events generated by the general-purpose timers (TMx) and the advanced-control timers (TM1 and TM8) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally

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connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

3.7 Digital to analog converter (DAC)

- 12-bit DAC converter of independent output channel
- 8-bit or 12-bit mode in conjunction with the DMA controller

The 12-bit buffered DAC channel is used to generate variable analog outputs. The DAC is designed with integrated resistor strings structure. The DAC channels can be triggered by the timer update outputs or EXTI with DMA support. The maximum output value of the DAC is V_{REF+}.

3.8 DMA

- 14 channels DMA controller and each channel are configurable (7 for DMA1 and 7 for DMA2)
- Peripherals supported: Timers, ADC, SPIs, I^2Cs, USARTs, DAC, I^2S and SDIO

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.9 General-purpose inputs/outputs (GPIOs)

- Up to 144 fast GPIOs, all mappable on 16 external interrupt vectors (EXTI)
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 140 general purpose I/O pins (GPIO) in GD32F205xx, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0 ~ PF15, PG0 ~ PG15, PH0 ~ PH1 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are

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shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.10 Timers and PWM generation

- Two 16-bit advanced-control timer (TM1 & TM8), ten 16-bit general-purpose timers (TM2 ~ TM5, TM9 ~ TM14), and two 16-bit basic timer (TM6 & TM7)
- Up to 4 independent channels of PWM, output compare or input capture for each general-purpose timer (GPTM) and external trigger input
- 16-bit, motor control PWM advanced-control timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (Independent watchdog and window watchdog)

The advanced-control timer (TM1 & TM8) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general-purpose timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge- or center-aligned counting modes) and single pulse mode output. If configured as a general-purpose 16-bit timer, it has the same functions as the TMx timer. It can be synchronized with external signals or to interconnect with other GPTMs together which have the same architecture and features.

The general-purpose timer (GPTM), known TM2 ~ TM5, TM9 ~ TM14 as can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. The GPTM is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TM2 ~ TM5 and TM9/TM12 also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TM6 & TM7, are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32F205xx have two watchdog peripherals, Independent watchdog and window watchdog. They offer a combination of high safety level, flexibility of use and timing accuracy.

The independent watchdog timer includes a 12-bit down-counting counter and a 8-bit prescaler, It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in stop and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

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The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.11 Real time clock (RTC) and backup registers

- 32-bit up-counter with a programmable 20-bit prescaler
- Alarm function
- Interrupt and wake-up event
- 84 bytes backup registers for data protection

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz from external crystal oscillator.

The Backup registers are located in the Backup domain that remains powered-on by V_{BAT} even if V_{DD} power is shut down, they are forty two 16-bit (84 bytes) registers for data protection of user application data, and the wake-up action from standby mode or system reset are not affect these registers.

In addition, the backup registers can be used to implement the tamper detection, RTC calibration function and waveform detection.

3.12 Inter-integrated circuit (I2C)

- Up to three I2C bus interfaces can support both master and slave mode with a frequency up to 400 kHz
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides two data transfer rates: 100 KHz of standard mode or 400 KHz of the fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

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3.13 Serial peripheral interface (SPI)

- Up to three SPI interfaces with a frequency of up to 30 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking
- Quad wire configuration available in master mode

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

3.14 Universal synchronous/asynchronous receiver transmitter (USART/UART)

- Up to four USARTs and four UARTs with operating frequency up to 7.5 MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART1, USART2, USART3, USART6) and UART (UART4, UART5, UART7, UART8) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART/UART transmitter and receiver. The USART/UART also supports DMA function for high speed data communication.

3.15 Inter-IC sound (I2S)

- Two I2S bus Interfaces with sampling frequency from 8 kHz to 192 kHz, multiplexed with SPI2 and SPI3
- Support either master or slave mode Audio
- Sampling frequencies from 8 kHz up to 192 kHz are supported.

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 3-wire serial lines. GD32F205xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI2 and SPI3. The audio sampling frequencies from 8 kHz to 192 kHz is supported with less than 0.5% accuracy error.

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3.16 Universal serial bus on-the-go full-speed (USB OTG FS)

- One USB device/host/OTG full-speed Interface with frequency up to 12 Mbit/s
- Internal main PLL for USB CLK compliantly

The Universal Serial Bus (USB) is a 4-wire bus with 4 bidirectional endpoints. The device controller enables 12 Mbit/s data exchange with integrated transceivers in device/host/OTG mode. Full-speed peripheral is compliant with the USB 2.0 specification. Transaction formatting is performed by the hardware, including CRC generation and checking. The status of a completed USB transfer or error condition is indicated by status registers. An interrupt is also generated if enabled. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator) and the operating frequency divided from APB1 should be 12 MHz above.

3.17 Controller area network (CAN)

- Two CAN2.0B interface with communication frequency up to 1 Mbit/s
- Internal main PLL for USB CLK compliantly

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three mailboxes for transmission and two FIFOs of three message deep for reception. It also provides 14 scalable/configurable identifier filter banks for selecting the incoming messages needed and discarding the others.

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3.18 External memory controller (EXMC)

- Supported external memory: SRAM, PSRAM, ROM and NOR-Flash, NAND Flash and CF card, SDRAM with up to 32-bit data bus
- Provide ECC calculating hardware module for NAND Flash memory block
- Two SDRAM banks with independent configuration, up to 13-bits Row Address, 11-bits Column Address, 2-bits internal banks address
- SDRAM Memory size: 4x16Mx32bit(256 MB), 4x16Mx16bit (128 MB), 4x16Mx8bit (64 MB)

External memory controller (EXMC) is an abbreviation of external memory controller. It is divided in to several sub-banks for external device support, each sub-bank has its own chip selection signal but at one time, only one bank can be accessed. The EXMC support code execution from external memory except NAND Flash and CF card. The EXMC also can be configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

The EXMC of GD32F205xx in LQFP144 package also supports synchronous dynamic random access memory (SDRAM). It translates AHB transactions into the appropriate SDRAM protocol, and meanwhile, makes sure the access time requirements of the external SDRAM devices are satisfied.

3.19 Secure digital input and output card interface (SDIO)

- Support SD2.0/SDIO2.0/MMC4.2 host interface

The Secure Digital Input and Output Card Interface (SDIO) provides access to external SD memory cards specifications version 2.0, SDIO card specification version 2.0 and multi-media card system specification version 4.2 with DMA supported. In addition, this interface is also compliant with CE-ATA digital protocol rev1.1.

3.20 TFT LCD display interface (TLDI)

- 24-bit RGB Parallel Pixel Output; 8 bits-per-pixel (RGB888)
- Supports up to SVGA (800x600) resolution

The TFT LCD display interface provides a parallel digital RGB (Red, Green, Blue) and signals for horizontal, vertical synchronization, Pixel Clock and Data Enable as output to interface directly to a variety of LCD (Liquid Crystal Display) and TFT (Thin Film Transistor) panels.

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3.26 Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.27 Package and operation temperature

- LQFP144 (GD32F205Zx), LQFP100 (GD32F205Vx), LQFP64 (GD32F205Rx)
- Operation temperature range: -40°C to +85°C (industrial level)

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4 Electrical characteristics

4.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5V tolerant pin	V_{SS} - 0.3	V_{DD} + 4.0	V
	Input voltage on other I/O	V_{SS} - 0.3	4.0	V
I_{IO}	Maximum current for GPIO pins	—	25	mA
I_{INJ}	Injected current on 5V tolerant pin	—	±5	mA
	Injected current on other I/O	—	±5	mA
ΣI_{INJ}	Injected current on all I/O	—	±25	mA
T_A	Operating temperature range	-40	+85	°C
T_{STG}	Storage temperature range	-55	+150	°C
T_J	Maximum junction temperature	—	125	°C

4.2 Recommended DC characteristics

Table 4. DC operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	—	2.6	3.3	3.6	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	2.6	3.3	3.6	V
V_{BAT}	Battery supply voltage	—	1.8	—	3.6	V

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4.3 Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 5. Power consumption characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current (Run mode)	V_{DD}=V_{DDA}=3.3V, HSE=25MHz, System clock=120 MHz, All peripherals enabled	—	95.52	—	mA
		V_{DD}=V_{DDA}=3.3V, HSE=25MHz, System clock =120 MHz, All peripherals disabled	—	55.23	—	mA
		V_{DD}=V_{DDA}=3.3V, HSE=25MHz, System clock=108 MHz, All peripherals enabled	—	86.22	—	mA
		V_{DD}=V_{DDA}=3.3V, HSE=25MHz, System clock =108 MHz, All peripherals disabled	—	50.05	—	mA
		V_{DD}=V_{DDA}=3.3V, HSE=25MHz, System clock =72MHz, All peripherals enabled	-—	58.42	—	mA
		V_{DD}=V_{DDA}=3.3V, HSE=25MHz, System Clock =72 MHz, All peripherals disabled	—	34.32	—	mA
	Supply current (Sleep mode)	V_{DD}=V_{DDA}=3.3V, HSE=8MHz, CPU clock off, System clock=120 MHz, All peripherals enabled	—	59.46	—	mA
		V_{DD}=V_{DDA}=3.3V, HSE=8MHz, CPU clock off, System clock=120 MHz, All peripherals disabled	—	12.22	—	mA
	Supply current (Deep-Sleep mode)	V_{DD}=V_{DDA}=3.3V, Regulator in Run mode, LSI on, RTC on, All GPIOs analog mode	—	1.23	—	mA
		V_{DD}=V_{DDA}=3.3V, Regulator in Low Power mode, LSI on, RTC on, All GPIOs analog mode	—	1.18	—	mA
	Supply current (Standby mode)	V_{DD}=V_{DDA}=3.3V, LSE off, LSI on, RTC on	—	7.47	—	µA
		V_{DD}=V_{DDA}=3.3V, LSE off, LSI on, RTC off	—	7.35	—	µA
		V_{DD}=V_{DDA}=3.3V, LSE off, LSI off, RTC off	—	6.13	—	µA
I_{BAT}	Battery supply current	V_{BAT}=3.6V, LSE on, RTC on, LSE High driving	—	2.69	—	µA
		V_{BAT}=3.3V, LSE on, RTC on, LSE High driving	—	2.41	—	µA
		V_{BAT}=2.6V, LSE on, RTC on, LSE High driving	—	1.81	—	µA
		V_{BAT}=3.6V, LSE on, RTC on,LSE Mid High driving	—	1.10	—	µA
		V_{BAT}=3.3V, LSE on, RTC on,LSE Mid High driving	—	1.04	—	µA
		V_{BAT}=2.6V, LSE on, RTC on,LSE Mid High driving	—	0.92	—	µA
		V_{BAT}=3.6V, LSE on, RTC on, LSE Mid Low driving	—	0.83	—	µA
		V_{BAT}=3.3V, LSE on, RTC on, LSE Mid Low driving	—	0.76	—	µA
		V_{BAT}=2.6V, LSE on, RTC on, LSE Mid Low driving	—	0.63	—	µA

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4.4 EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in the following table, based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 6. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	VDD = 3.3 V, TA = +25 °C conforms to IEC 61000-4-2	3B
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V_{DD} and V_{SS} pins	VDD = 3.3 V, TA = +25 °C conforms to IEC 61000-4-4	4A

EMI (Electromagnetic Interference) emission testing result is given in the following table, compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 7. EMI characteristics

Symbol	Parameter	Conditions	Tested frequency band	Conditions			Unit
				56M	72M	120M	
S_{EMI}	Peak level	VDD = 3.3 V, TA = +25 °C, compliant with IEC 61967-2	0.1 to 2 MHz	<0	<0	<0	dBµV
			2 to 30 MHz	-3.7	-2.8	-1.8	
			30 to 130 MHz	-6.5	-8	-5.3	
			130 MHz to 1GHz	-7	-7	-5	

4.5 Power supply supervisor characteristics

Table 8. Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{POR}	Power on reset threshold		2.32	2.40	2.48	V
V_{PDR}	power down reset threshold		2.27	2.35	2.43	V
V_{HYST}	PDR hysteresis		—	0.05	—	V
$T_{RSTTEMP}$	Reset temporization		—	2	—	s

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4.6 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 9. ESD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=25 °C; JESD22-A114	—	—	5000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A=25 °C; JESD22-C101	—	—	500	V

Table 10. Static latch-up characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A=25 °C; JESD78	—	—	±100	mA
	V_{supply} over voltage		—	—	5.4	V

4.7 External clock characteristics

Table 11. High speed external clock (HSE) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	High Speed External oscillator (HSE) frequency	V_{DD}=3.3V	3	8	32	MHz
C_{HSE}	Recommended load capacitance on OSC_IN and OSC_OUT	—	—	20	30	pF
R_{FHSE}	Recommended external feedback resistor between XTALIN and XTALOUT	—	—	1	—	MΩ
D_{HSE}	HSE oscillator duty cycle	—	48	50	52	%
I_{DDHSE}	HSE oscillator operating current	V_{DD}=3.3V, T_A=25°C	—	—	1.2	μA
t_{SUHSE}	HSE oscillator startup time	V_{DD}=3.3V, T_A=25°C	—	2	—	ms

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Table 12. Low speed external clock (LSE) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low Speed External oscillator (LSE) frequency	V_{DD}=V_{BAT}=3.3V	—	32.768	1000	KHz
C_{LSE}	Recommended load capacitance on OSC32_IN and OSC32_OUT	—	8	10	15	pF
R_{FLSE}	Recommended external feedback resistor between XTAL32IN and XTAL32OUT	—	—	5	—	MΩ
D_{LSE}	LSE oscillator duty cycle	—	48	50	52	%
I_{DDLSE}	LSE oscillator operating current	V_{DD}=V_{BAT}=3.3V	—	10	—	μA
t_{SULSE}	LSE oscillator startup time	V_{DD}=V_{BAT}=3.3V	—	3	—	s

4.8 Internal clock characteristics

Table 13. High speed internal clock (HSI) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	High Speed Internal Oscillator (HSI) frequency	V_{DD}=3.3V	—	8	—	MHz
ACC_{HSI}	HSI oscillator Frequency accuracy, Factory-trimmed	V_{DD}=3.3V, T_A=-40°C ~+105°C	-2.5	—	+1.5	%
		V_{DD}=3.3V, T_A=0°C ~ +85°C	-1.2	—	+1.2	%
		V_{DD}=3.3V, T_A=25°C	-1	—	+1	%
D_{HSI}	HSI oscillator duty cycle	V_{DD}=3.3V, f_{HSI}=8MHz	48	50	52	%
I_{DDHSI}	HSI oscillator operating current	V_{DD}=3.3V, f_{HSI}=8MHz	—	80	100	μA
t_{SUHSI}	HSI oscillator startup time	V_{DD}=3.3V, f_{HSI}=8MHz	1	—	2	us

Table 14. Low speed internal clock (LSI) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Low Speed Internal oscillator (LSI) frequency	V_{DD}=V_{BAT}=3.3V, T_A=-40°C ~ +85°C	30	40	60	KHz
I_{DDLSI}	LSI oscillator operating current	V_{DD}=V_{BAT}=3.3V, T_A=25°C	—	1	2	μA
t_{SULSI}	LSI oscillator startup time	V_{DD}=V_{BAT}=3.3V, T_A=25°C	—	—	80	μs

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4.9 PLL characteristics

Table 15. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock frequency		1	8	25	MHz
f_{PLL}	PLL output clock frequency		16	—	120	MHz
t_{LOCK}	PLL lock time		—		100	μs

4.10 Memory characteristics

Table 16. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	T_A=-40°C ~ +85°C	100	—	—	kcycles
t_{RET}	Data retention time	T_A=125°C	20	—	—	years
t_{PROG}	Word programming time	T_A=-40°C ~ +85°C	200	—	400	us
t_{ERASE}	Page erase time	T_A=-40°C ~ +85°C	60	100	450	ms
t_{MERASE}	Mass erase time	T_A=-40°C ~ +85°C	3.2	—	9.6	s

4.11 GPIO characteristics

Table 17. I/O port characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage	V_{DD}=2.6V	-0.3	—	0.95	V
	5V-tolerant IO Low level input voltage	V_{DD}=2.6V	-0.3	—	0.9	V
V_{IH}	Standard IO High level input voltage	V_{DD}=2.6V	1.2	—	4.0	V
	5V-tolerant IO High level input voltage	V_{DD}=2.6V	1.5	—	5.5	V
V_{OL}	Low level output voltage	V_{DD}=2.6V	—	—	0.2	V
V_{OH}	High level output voltage	V_{DD}=2.6V	2.3	—	—	V
R_{PU}	Internal pull-up resistor	V_{IN}=V_{SS}	30	40	50	kΩ
R_{PD}	Internal pull-down resistor	V_{IN}=V_{DD}	30	40	50	kΩ

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4.12 ADC characteristics

Table 18. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage		2.6	3.3	3.6	V
V_{ADCIN}	ADC input voltage range		0	—	V_{REF+}	V
f_{ADC}	ADC clock		0.6	—	28	MHz
f_S	Sampling rate	12-bit	—	—	2	MHz
R_{ADC}	Input sampling switch resistance		—	—	0.45	kΩ
C_{ADC}	Input sampling capacitance	No pin/pad capacitance included	—	6.4	—	pF
t_{SU}	Startup time		—	—	1	µs

4.13 DAC characteristics

Table 19. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage		2.6	3.3	3.6	V
V_{DACIN}	DAC input voltage range		0	—	V_{REF+}	V
R_{LOAD}	Load resistance	Resistive load vs. V_{SSA} with buffer ON	5	—	—	kΩ
C_{LOAD}	Load capacitance	No pin/pad capacitance included	—	—	50	pF
DNE	Differential non-linearity error	DAC in 12-bit	—	—	±3	LSB
INL	Integral non-linearity	DAC in 12-bit	—	—	±4	LSB
Offset	Offset error	DAC in 12-bit, V_{REF+} = 3.6 V	—	—	±12	LSB
GE	Gain error	DAC in 12-bit	—	—	±0.5	%

4.14 I2C characteristics

Table 20. I2C characteristics

Symbol	Parameter	Conditions	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	KHz
$t_{SCL(H)}$	SCL clock high time		4.0	—	0.6	—	ns
$t_{SCL(L)}$	SCL clock low time		4.7	—	1.3	—	ns

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4.15 SPI characteristics

Table 21. SPI characteristics

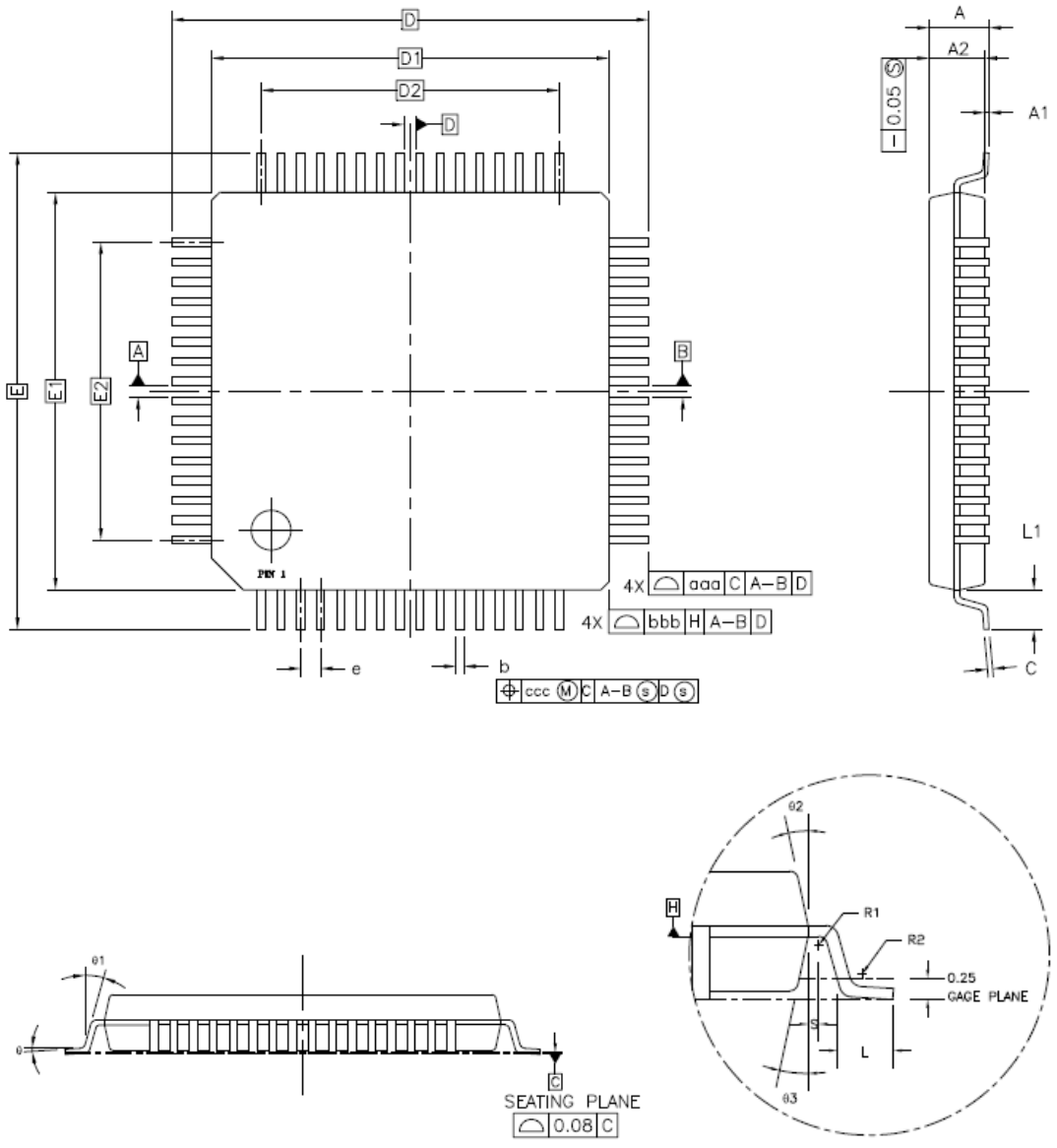
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency		—	—	30	MHz
$t_{SCK(H)}$	SCK clock high time		19	—	—	ns
$t_{SCK(L)}$	SCK clock low time		19	—	—	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time		—	—	25	ns
$t_{H(MO)}$	Data output hold time		2	—	—	ns
$t_{SU(MI)}$	Data input setup time		5	—	—	ns
$t_{H(MI)}$	Data input hold time		5	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	f_{PCLK}=54MHz	74	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	f_{PCLK}=54MHz	37	—	—	ns
$t_{A(SO)}$	Data output access time	f_{PCLK}=54MHz	0	—	55	ns
$t_{DIS(SO)}$	Data output disable time		3	—	10	ns
$t_{V(SO)}$	Data output valid time		—	—	25	ns
$t_{H(SO)}$	Data output hold time		15	—	—	ns
$t_{SU(SI)}$	Data input setup time		5	—	—	ns
$t_{H(SI)}$	Data input hold time		4	—	—	ns

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5 Package information

5.1 LQFP package outline dimensions

Figure 7. LQFP package outline



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Table 22. LQFP package dimensions

Symbol	LQFP64			LQFP100			LQFP144		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	1.60	-	-	1.60
A1	0.05	-	0.15	0.05	-	0.15	0.05	-	0.15
A2	1.35	1.40	1.45	1.35	1.40	1.45	1.35	1.40	1.45
D	-	12.00	-	-	16.00	-	-	22.00	-
D1	-	10.00	-	-	14.00	-	-	20.00	-
E	-	12.00	-	-	16.00	-	-	22.00	-
E1	-	10.00	-	-	14.00	-	-	20.00	-
R1	0.08	-	-	0.08	-	-	0.08	-	-
R2	0.08	-	0.20	0.08	-	0.20	0.08	-	0.20
θ	0°	3.5°	7°	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-	0°	-	-
θ2	11°	12°	13°	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°	11°	12°	13°
c	0.09	-	0.20	0.09	-	0.20	0.09	-	0.20
L	0.45	0.60	0.75	0.45	0.60	0.75	0.45	0.60	0.75
L1	-	1.00	-	-	1.00	-	-	1.00	-
S	0.20	-	-	0.20	-	-	0.20	-	-
b	0.17	0.20	0.27	0.17	0.20	0.27	0.17	0.20	0.27
e	-	0.50	-	-	0.50	-	-	0.50	-
D2	-	7.50	-	-	12.00	-	-	17.50	-
E2	-	7.50	-	-	12.00	-	-	17.50	-
aaa	0.20			0.20			0.20		
bbb	0.20			0.20			0.20		
ccc	0.08			0.08			0.08		

(Original dimensions are in millmeters)

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6 Ordering information

Table 23. Part ordering code for GD32F205xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32F205RCT6	256	LQFP64	Green	Industrial -40°C to +85°C
GD32F205RET6	512	LQFP64	Green	Industrial -40°C to +85°C
GD32F205RGT6	1024	LQFP64	Green	Industrial -40°C to +85°C
GD32F205RKT6	3072	LQFP64	Green	Industrial -40°C to +85°C
GD32F205VCT6	256	LQFP100	Green	Industrial -40°C to +85°C
GD32F205VET6	512	LQFP100	Green	Industrial -40°C to +85°C
GD32F205VGT6	1024	LQFP100	Green	Industrial -40°C to +85°C
GD32F205VKT6	3072	LQFP100	Green	Industrial -40°C to +85°C
GD32F205ZCT6	256	LQFP144	Green	Industrial -40°C to +85°C
GD32F205ZET6	512	LQFP144	Green	Industrial -40°C to +85°C
GD32F205ZGT6	1024	LQFP144	Green	Industrial -40°C to +85°C
GD32F205ZKT6	3072	LQFP144	Green	Industrial -40°C to +85°C

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7 Revision history

Table 24. Revision history

Revision No.	Description	Date
1.0	Initial Release	Jul. 10, 2015

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