# GigaDevice Semiconductor Inc.

# GD32F205xx
# ARM® Cortex®-M3 32-bit MCU

Datasheet

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# 1. General description

The GD32F205xx device belongs to the performance line of GD32 MCU Family. It is a new 32-bit general-purpose microcontroller based on the ARM® Cortex®-M3 RISC core with best cost-performance ratio in terms of processing capacity, reduced power consumption and peripheral set. The Cortex®-M3 is a next generation processor core which is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), SysTick timer and advanced debug support.

The GD32F205xx device incorporates the ARM® Cortex®-M3 32-bit processor core operating at 120 MHz frequency with flash accesses zero wait states to obtain maximum efficiency. It provides up to 3072 KB on-chip flash memory and 256 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to three 12-bit 2 MSPS ADCs, two 12-bit DACs, up to ten 16-bit general timers, two 16-bit basic timers plus two 16-bit PWM advanced timers, as well as standard and advanced communication interfaces: up to three SPIs, three I2Cs, four USARTs and four UARTs, two I2Ss, two CANs, a SDIO, a USBFS. Additional peripherals as TFT-LCD Interface (TLI) and EXMC interface with SDRAM extension support are included.

The device operates from a 2.6 to 3.6V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization of power consumption, an especially important consideration in low power applications.

The above features make GD32F205xx devices suitable for a wide range of interconnection and advanced applications, especially in areas such as industrial control, consumer and handheld equipment, embedded modules, human machine interface, security and alarm systems, automotive navigation and so on.






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# 2. Device overview

## 2.1. Device information

**Table 2-1. GD32F205xx devices features and peripheral list**

| Part Number | | GD32F205xx | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | RC | RE | RG | RK | VC | VE | VG | VK |
| Flash | Fast area (KB) | 256 | 512 | 384 | 384 | 256 | 512 | 384 | 384 |
| | Normal area (KB) | 0 | 0 | 640 | 2688 | 0 | 0 | 640 | 2688 |
| | Total (KB) | 256 | 512 | 1024 | 3072 | 256 | 512 | 1024 | 3072 |
| SRAM (KB) | | 128 | 128 | 256 | 256 | 128 | 128 | 256 | 256 |
| Timers | General timer (16-bit) | 10 (1-4,8-13) | 10 (1-4,8-13) | 10 (1-4,8-13) | 10 (1-4,8-13) | 10 (1-4,8-13) | 10 (1-4,8-13) | 10 (1-4,8-13) | 10 (1-4,8-13) |
| | Advanced timer (16-bit) | 2 (0,7) | 2 (0,7) | 2 (0,7) | 2 (0,7) | 2 (0,7) | 2 (0,7) | 2 (0,7) | 2 (0,7) |
| | SysTick | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Basic timer (16-bit) | 2 (5,6) | 2 (5,6) | 2 (5,6) | 2 (5,6) | 2 (5,6) | 2 (5,6) | 2 (5,6) | 2 (5,6) |
| | Watchdog | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | RTC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Connectivity | USART | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| | UART | 2 (3-4) | 2 (3-4) | 2 (3-4) | 2 (3-4) | 4 (3-4,6-7) | 4 (3-4,6-7) | 4 (3-4,6-7) | 4 (3-4,6-7) |
| | I2C | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| | SPI/I2S | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) |
| | SDIO | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | CAN | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | USBFS | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | TLI | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| GPIO | | 51 | 51 | 51 | 51 | 82 | 82 | 82 | 82 |
| EXMC/SDRAM | | 0/0 | 0/0 | 0/0 | 0/0 | 1/0 | 1/0 | 1/0 | 1/0 |
| ADC (CHs) | | 3(16) | 3(16) | 3(16) | 3(16) | 3(16) | 3(16) | 3(16) | 3(16) |
| DAC | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |



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| Part Number | GD32F205xx | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | RC | RE | RG | RK | VC | VE | VG | VK |
| Package | LQFP64 | | | | LQFP100 | | | |

**Table 2-1. GD32F205xx devices features and peripheral list (continued)**

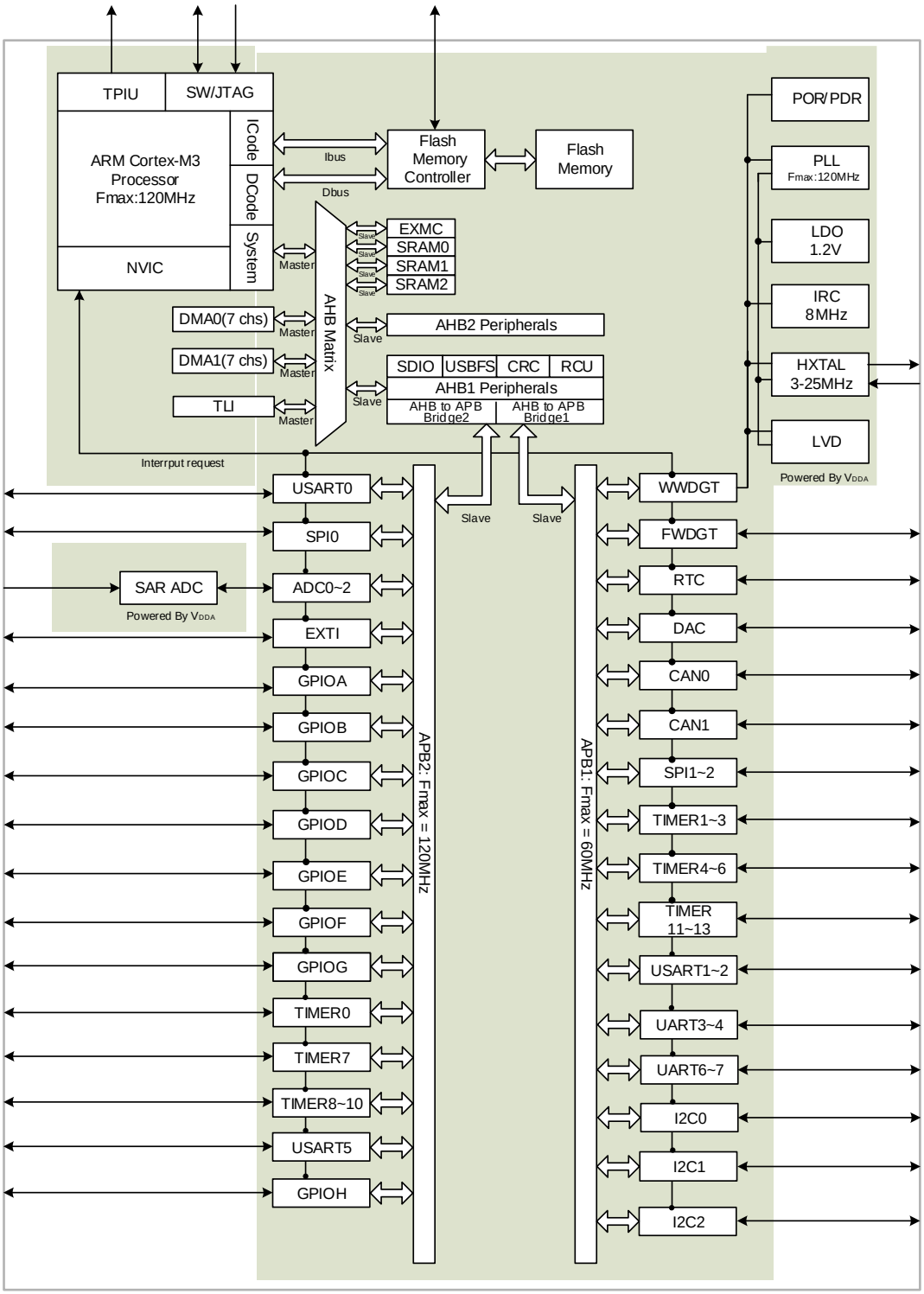
| Part Number | | GD32F205xx | | | |
|---|---|---|---|---|---|
| | | ZC | ZE | ZG | ZK |
| Flash | Code area (KB) | 256 | 512 | 384 | 384 |
| | Data area (KB) | 0 | 0 | 640 | 2688 |
| | Total (KB) | 256 | 512 | 1024 | 3072 |
| SRAM (KB) | | 128 | 128 | 256 | 256 |
| Timers | General timer (16-bit) | 10 (1-4,8-13) | 10 (1-4,8-13) | 10 (1-4,8-13) | 10 (1-4,8-13) |
| | Advanced timer (16-bit) | 2 (0,7) | 2 (0,7) | 2 (0,7) | 2 (0,7) |
| | SysTick | 1 | 1 | 1 | 1 |
| | Basic timer (16-bit) | 2 (5,6) | 2 (5,6) | 2 (5,6) | 2 (5,6) |
| | Watchdog(16-bit) | 2 | 2 | 2 | 2 |
| | RTC | 1 | 1 | 1 | 1 |
| Connectivity | USART | 4 | 4 | 4 | 4 |
| | UART | 4 | 4 | 4 | 4 |
| | I2C | 3 | 3 | 3 | 3 |
| | SPI/I2S | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) | 3/2 (0-2)/(1-2) |
| | SDIO | 1 | 1 | 1 | 1 |
| | CAN | 2 | 2 | 2 | 2 |
| | USBFS | 1 | 1 | 1 | 1 |
| | TLI | 1 | 1 | 1 | 1 |
| GPIO | | 114 | 114 | 114 | 114 |
| EXMC/SDRAM | | 1/1 | 1/1 | 1/1 | 1/1 |
| ADC (CHs) | | 3(24) | 3(24) | 3(24) | 3(24) |
| DAC | | 2 | 2 | 2 | 2 |
| Package | | LQFP144 | | | |



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## 2.2. Block diagram

**Figure 2-1. GD32F205xx block diagram**

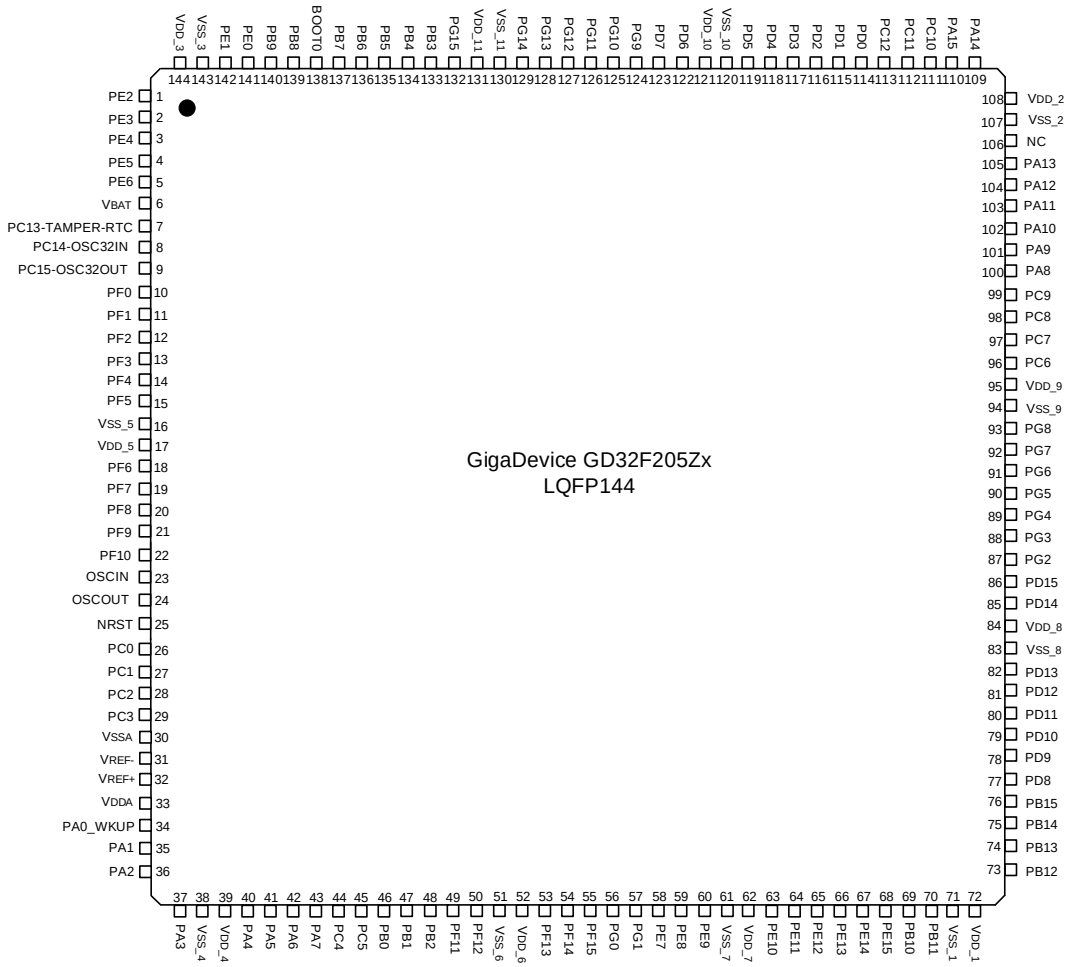





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## 2.3. Pinouts and pin assignment

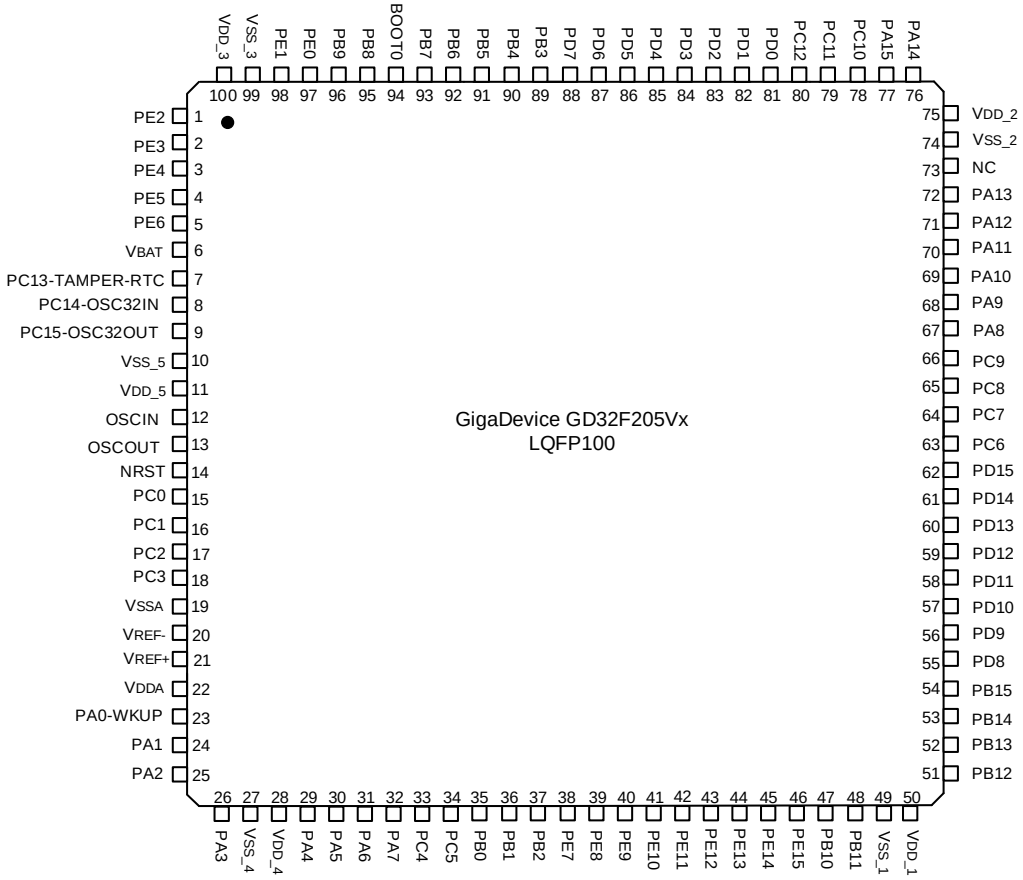
**Figure 2-2. GD32F205Zx LQFP144 pinouts**






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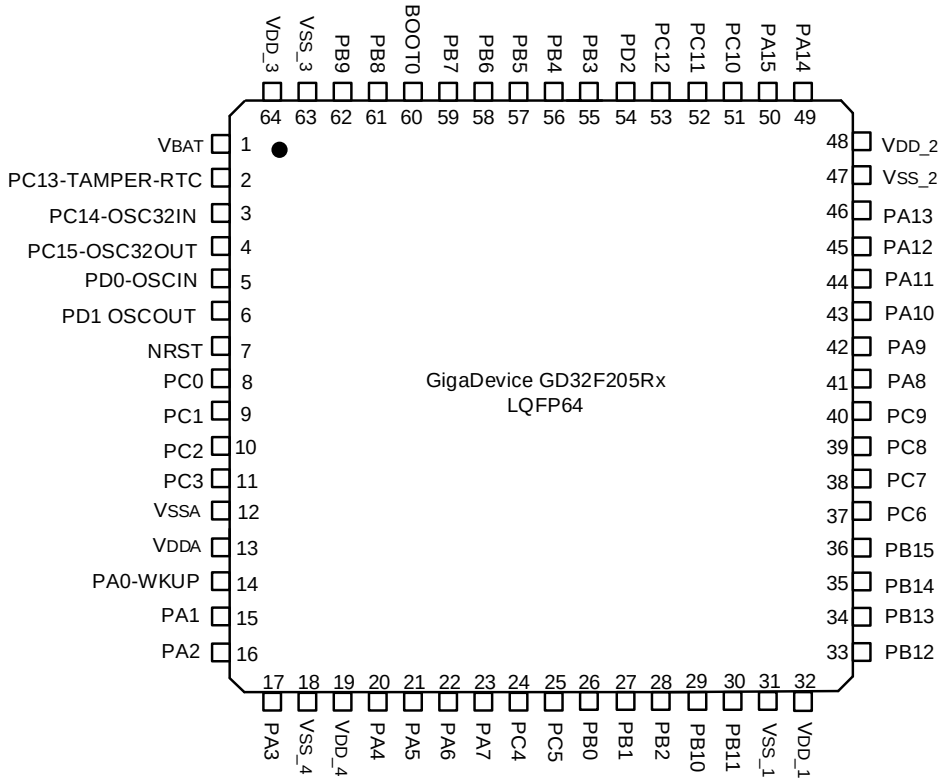
**Figure 2-3. GD32F205Vx LQFP100 pinouts**






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**Figure 2-4. GD32F205Rx LQFP64 pinouts**






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## 2.4. Memory map

**Table 2-2 GD32F205xx memory map**

| Pre-defined Regions | Bus | Address | Peripherals |
|---|---|---|---|
| External Device | AHB | 0xC000 0000 - 0xDFFF FFFF | EXMC - SDRAM |
| | | 0xA000 1000 - 0xBFFF FFFF | Reserved |
| | | 0xA000 0000 - 0xA000 0FFF | EXMC - SWREG |
| External RAM | | 0x9000 0000 - 0x9FFF FFFF | EXMC - PC CARD |
| | | 0x7000 0000 - 0x8FFF FFFF | EXMC - NAND |
| | | 0x6000 0000 - 0x6FFF FFFF | EXMC - NOR/PSRAM/SRAM |
| Peripheral | AHB2 | 0x5004 0000 - 0x5FFF FFFF | Reserved |
| | AHB1 | 0x5000 0000 - 0x5003 FFFF | USBFS |
| | | 0x4002 3400 - 0x4FFF FFFF | Reserved |
| | | 0x4002 3000 - 0x4002 33FF | CRC |
| | | 0x4002 2400 - 0x4002 2FFF | Reserved |
| | | 0x4002 2000 - 0x4002 23FF | FMC |
| | | 0x4002 1400 - 0x4002 1FFF | Reserved |
| | | 0x4002 1000 - 0x4002 13FF | RCU |
| | | 0x4002 0800 - 0x4002 0FFF | Reserved |
| | | 0x4002 0400 - 0x4002 07FF | DMA0 |
| | | 0x4002 0000 - 0x4002 03FF | DMA1 |
| | APB2 | 0x4001 8400 - 0x4001 FFFF | Reserved |
| | | 0x4001 8000 - 0x4001 83FF | SDIO |
| | | 0x4001 7800 - 0x4001 7FFF | Reserved |
| | | 0x4001 7400 - 0x4001 77FF | GPIOH |
| | | 0x4001 7000 - 0x4001 73FF | USART5 |
| | | 0x4001 6C00 - 0x4001 6FFF | Reserved |
| | | 0x4001 6800 - 0x4001 6BFF | TLI |
| | | 0x4001 5800 - 0x4001 67FF | Reserved |
| | | 0x4001 5400 - 0x4001 57FF | TIMER10 |
| | | 0x4001 5000 - 0x4001 53FF | TIMER9 |
| | | 0x4001 4C00 - 0x4001 4FFF | TIMER8 |
| | | 0x4001 4000 - 0x4001 4BFF | Reserved |
| | | 0x4001 3C00 - 0x4001 3FFF | ADC2 |
| | | 0x4001 3800 - 0x4001 3BFF | USART0 |
| | | 0x4001 3400 - 0x4001 37FF | TIMER7 |
| | | 0x4001 3000 - 0x4001 33FF | SPI0 |
| | | 0x4001 2C00 - 0x4001 2FFF | TIMER0 |
| | | 0x4001 2800 - 0x4001 2BFF | ADC1 |
| | | 0x4001 2400 - 0x4001 27FF | ADC0 |
| | | 0x4001 2000 - 0x4001 23FF | GPIOG |



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| Pre-defined Regions | Bus | Address | Peripherals |
|---|---|---|---|
| | | 0x4001 1C00 - 0x4001 1FFF | GPIOF |
| | | 0x4001 1800 - 0x4001 1BFF | GPIOE |
| | | 0x4001 1400 - 0x4001 17FF | GPIOD |
| | | 0x4001 1000 - 0x4001 13FF | GPIOC |
| | | 0x4001 0C00 - 0x4001 0FFF | GPIOB |
| | | 0x4001 0800 - 0x4001 0BFF | GPIOA |
| | | 0x4001 0400 - 0x4001 07FF | EXTI |
| | | 0x4001 0000 - 0x4001 03FF | AFIO |
| | APB1 | 0x4000 C400 - 0x4000 FFFF | Reserved |
| | | 0x4000 C000 - 0x4000 C3FF | I2C2 |
| | | 0x4000 8000 - 0x4000 BFFF | Reserved |
| | | 0x4000 7C00 - 0x4000 7FFF | UART7 |
| | | 0x4000 7800 - 0x4000 7BFF | UART6 |
| | | 0x4000 7400 - 0x4000 77FF | DAC |
| | | 0x4000 7000 - 0x4000 73FF | PMU |
| | | 0x4000 6C00 - 0x4000 6FFF | BKP |
| | | 0x4000 6800 - 0x4000 6BFF | CAN1 |
| | | 0x4000 6400 - 0x4000 67FF | CAN0 |
| | | 0x4000 5C00 - 0x4000 63FF | USBFS/CAN shared |
| | | 0x4000 5800 - 0x4000 5BFF | I2C1 |
| | | 0x4000 5400 - 0x4000 57FF | I2C0 |
| | | 0x4000 5000 - 0x4000 53FF | UART4 |
| | | 0x4000 4C00 - 0x4000 4FFF | UART3 |
| | | 0x4000 4800 - 0x4000 4BFF | USART2 |
| | | 0x4000 4400 - 0x4000 47FF | USART1 |
| | | 0x4000 4000 - 0x4000 43FF | Reserved |
| | | 0x4000 3C00 - 0x4000 3FFF | SPI2/I2S2 |
| | | 0x4000 3800 - 0x4000 3BFF | SPI1/I2S1 |
| | | 0x4000 3400 - 0x4000 37FF | Reserved |
| | | 0x4000 3000 - 0x4000 33FF | FWDGT |
| | | 0x4000 2C00 - 0x4000 2FFF | WWDGT |
| | | 0x4000 2800 - 0x4000 2BFF | RTC |
| | | 0x4000 2400 - 0x4000 27FF | Reserved |
| | | 0x4000 2000 - 0x4000 23FF | TIMER13 |
| | | 0x4000 1C00 - 0x4000 1FFF | TIMER12 |
| | | 0x4000 1800 - 0x4000 1BFF | TIMER11 |
| | | 0x4000 1400 - 0x4000 17FF | TIMER6 |
| | | 0x4000 1000 - 0x4000 13FF | TIMER5 |
| | | 0x4000 0C00 - 0x4000 0FFF | TIMER4 |
| | | 0x4000 0800 - 0x4000 0BFF | TIMER3 |



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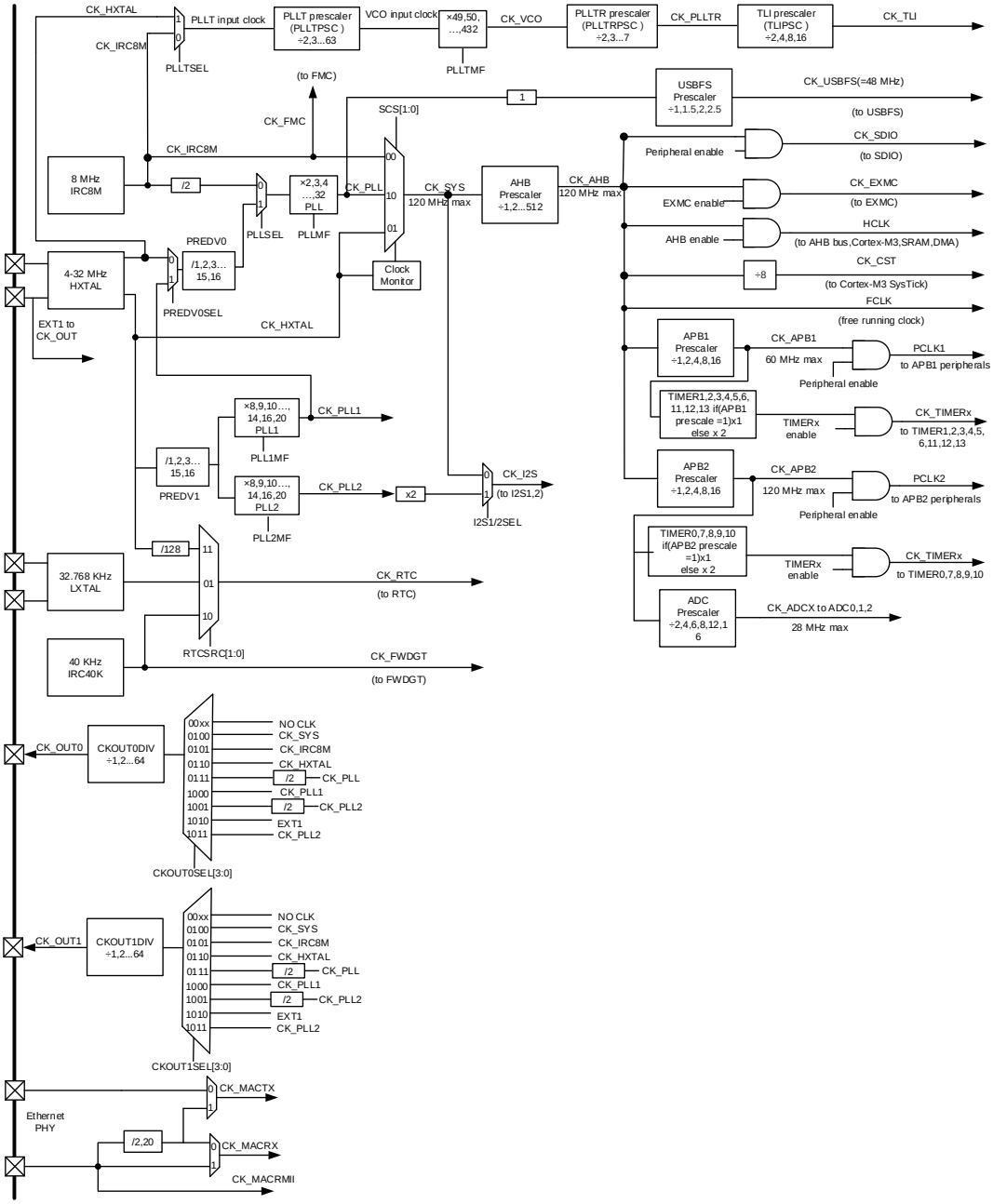
| Pre-defined Regions | Bus | Address | Peripherals |
|---|---|---|---|
| | | 0x4000 0400 - 0x4000 07FF | TIMER2 |
| | | 0x4000 0000 - 0x4000 03FF | TIMER1 |
| SRAM | AHB | 0x2004 0000 - 0x3FFF FFFF | Reserved |
| | | 0x2002 0000 - 0x2003 FFFF | SRAM2(128KB) |
| | | 0x2001 C000 - 0x2001 FFFF | SRAM1(16KB) |
| | | 0x2000 0000 - 0x2001 BFFF | SRAM0(112KB) |
| Code | AHB | 0x1FFF F810 - 0x1FFF FFFF | Reserved |
| | | 0x1FFF F800 - 0x1FFF F80F | Option Bytes |
| | | 0x1FFF B000 - 0x1FFF F7FF | System memory |
| | | 0x0830 0000 - 0x1FFF AFFF | Reserved |
| | | 0x0800 0000 - 0x082F FFFF | Main flash(3072KB) |
| | | 0x0000 0000 - 0x07FF FFFF | Aliased to flash or system memory according to BOOT pins configuration |



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## 2.5. Clock tree

**Figure 2-5. GD32F205xx clock tree**




**Legend:**

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC8M: Internal 8M RC oscillators

IRC40K: Internal 40K RC oscillator



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## 2.6. Pin definitions

### 2.6.1. GD32F205Zx LQFP144 pin definitions

**Table 2-3. GD32F205Zx LQFP144 pin definitions**

| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| PE2 | 1 | I/O | 5VT | Default: PE2<br>Alternate: TRACECK, EXMC_A23 |
| PE3 | 2 | I/O | 5VT | Default: PE3<br>Alternate: TRACED0, EXMC_A19 |
| PE4 | 3 | I/O | 5VT | Default: PE4<br>Alternate:TRACED1, EXMC_A20<br>Remap: TLI_B0 |
| PE5 | 4 | I/O | 5VT | Default: PE5<br>Alternate:TRACED2, EXMC_A21<br>Remap: TIMER8_CH0, TLI_G0 |
| PE6 | 5 | I/O | 5VT | Default: PE6<br>Alternate:TRACED3, EXMC_A22<br>Remap: TIMER8_CH1, TLI_G1 |
| $V_{BAT}$ | 6 | P | | Default: $V_{BAT}$ |
| PC13-TAMPER-RTC | 7 | I/O | | Default: PC13<br>Alternate: TAMPER-RTC |
| PC14-OSC32IN | 8 | I/O | | Default: PC14<br>Alternate: OSC32IN |
| PC15-OSC32OUT | 9 | I/O | | Default: PC15<br>Alternate: OSC32OUT |
| PF0 | 10 | I/O | 5VT | Default: PF0<br>Alternate: EXMC_A0<br>Remap: I2C1_SDA |
| PF1 | 11 | I/O | 5VT | Default: PF1<br>Alternate: EXMC_A1<br>Remap: I2C1_SCL |
| PF2 | 12 | I/O | 5VT | Default: PF2<br>Alternate: EXMC_A2<br>Remap: I2C1_SMBA |
| PF3 | 13 | I/O | 5VT | Default: PF3<br>Alternate: EXMC_A3, ADC2_IN9 |
| PF4 | 14 | I/O | 5VT | Default: PF4<br>Alternate: EXMC_A4, ADC2_IN14 |
| PF5 | 15 | I/O | 5VT | Default: PF5<br>Alternate: EXMC_A5, ADC2_IN15 |
| $V_{SS_5}$ | 16 | P | | Default: $V_{SS_5}$ |
| $V_{DD_5}$ | 17 | P | | Default: $V_{DD_5}$ |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| PF6 | 18 | I/O | | Default: PF6<br>Alternate: ADC2_IN4, EXMC_NIORD<br>Remap: TIMER9_CH0, UART6_RX |
| PF7 | 19 | I/O | | Default: PF7<br>Alternate: ADC2_IN5, EXMC_NREG<br>Remap: TIMER10_CH0, UART6_TX |
| PF8 | 20 | I/O | | Default: PF8<br>Alternate: ADC2_IN6, EXMC_NIOWR<br>Remap: TIMER12_CH0 |
| PF9 | 21 | I/O | | Default: PF9<br>Alternate: ADC2_IN7, EXMC_CD<br>Remap: TIMER13_CH0 |
| PF10 | 22 | I/O | | Default: PF10<br>Alternate: ADC2_IN8, EXMC_INTR<br>Remap: TLI_DE |
| OSCIN | 23 | I | | Default: OSCIN<br>Remap: PH0 |
| OSCOUT | 24 | O | | Default: OSCOUT<br>Remap: PH1 |
| NRST | 25 | I/O | | Default: NRST |
| PC0 | 26 | I/O | | Default: PC0<br>Alternate: ADC012_IN10<br>Remap: EXMC_SDNWE |
| PC1 | 27 | I/O | | Default: PC1<br>Alternate: ADC012_IN11 |
| PC2 | 28 | I/O | | Default: PC2<br>Alternate: ADC012_IN12<br>Remap: EXMC_SDNE0, SPI1_MISO |
| PC3 | 29 | I/O | | Default: PC3<br>Alternate: ADC012_IN13<br>Remap: EXMC_SDCKE0, SPI1_MOSI, I2S1_SD |
| $V_{SSA}$ | 30 | P | | Default: $V_{SSA}$ |
| $V_{REF-}$ | 31 | P | | Default: $V_{REF-}$ |
| $V_{REF+}$ | 32 | P | | Default: $V_{REF+}$ |
| $V_{DDA}$ | 33 | P | | Default: $V_{DDA}$ |
| PA0-WKUP | 34 | I/O | | Default: PA0<br>Alternate: WKUP, USART1_CTS, ADC012_IN0, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI<br>Remap: UART3_TX |
| PA1 | 35 | I/O | | Default: PA1<br>Alternate: USART1_RTS, ADC012_IN1, TIMER1_CH1, TIMER4_CH1<br>Remap: UART3_RX |
| PA2 | 36 | I/O | | Default: PA2<br>Alternate: USART1_TX, ADC012_IN2, TIMER1_CH2, |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | TIMER4_CH2, TIMER8_CH0, SPI0_IO3 |
| PA3 | 37 | I/O | | Default: PA3<br>Alternate: USART1_RX, ADC012_IN3, TIMER1_CH3, TIMER4_CH3, TIMER8_CH1, SPI0_IO4<br>Remap: TLI_B5 |
| $V_{SS_4}$ | 38 | P | | Default: $V_{SS_4}$ |
| $V_{DD_4}$ | 39 | P | | Default: $V_{DD_4}$ |
| PA4 | 40 | I/O | | Default: PA4<br>Alternate: SPI0_NSS, USART1_CK, DAC_OUT0, ADC01_IN4<br>Remap: SPI2_NSS, I2S2_WS, TLI_VSYNC |
| PA5 | 41 | I/O | | Default: PA5<br>Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1<br>Remap: TIMER1_CH0, TIMER1_ETI, TIMER7_CH0_ON |
| PA6 | 42 | I/O | | Default: PA6<br>Alternate: SPI0_MISO, ADC01_IN6, TIMER2_CH0, TIMER7_BRKIN, TIMER12_CH0<br>Remap: TIMER0_BRKIN, TLI_G2 |
| PA7 | 43 | I/O | | Default: PA7<br>Alternate: SPI0_MOSI, ADC01_IN7, TIMER2_CH1, TIMER7_CH0_ON, TIMER13_CH0<br>Remap: TIMER0_CH0_ON |
| PC4 | 44 | I/O | | Default: PC4<br>Alternate: ADC01_IN14 |
| PC5 | 45 | I/O | | Default: PC5<br>Alternate: ADC01_IN15 |
| PB0 | 46 | I/O | | Default: PB0<br>Alternate: ADC01_IN8, TIMER2_CH2, TIMER7_CH1_ON<br>Remap: TIMER0_CH1_ON, TLI_R3 |
| PB1 | 47 | I/O | | Default: PB1<br>Alternate: ADC01_IN9, TIMER2_CH3, TIMER7_CH2_ON<br>Remap: TIMER0_CH2_ON, TLI_R6 |
| PB2 | 48 | I/O | 5VT | Default: PB2, BOOT1 |
| PF11 | 49 | I/O | 5VT | Default: PF11<br>Alternate: EXMC_NIOS16, EXMC_SDNRAS |
| PF12 | 50 | I/O | 5VT | Default: PF12<br>Alternate: EXMC_A6 |
| $V_{SS_6}$ | 51 | P | | Default: $V_{SS_6}$ |
| $V_{DD_6}$ | 52 | P | | Default: $V_{DD_6}$ |
| PF13 | 53 | I/O | 5VT | Default: PF13<br>Alternate: EXMC_A7 |
| PF14 | 54 | I/O | 5VT | Default: PF14<br>Alternate: EXMC_A8 |
| PF15 | 55 | I/O | 5VT | Default: PF15<br>Alternate: EXMC_A9 |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| PG0 | 56 | I/O | 5VT | Default: PG0<br>Alternate: EXMC_A10 |
| PG1 | 57 | I/O | 5VT | Default: PG1<br>Alternate: EXMC_A11 |
| PE7 | 58 | I/O | 5VT | Default: PE7<br>Alternate: EXMC_D4, UART6_RX<br>Remap: TIMER0_ETI |
| PE8 | 59 | I/O | 5VT | Default: PE8<br>Alternate: EXMC_D5, UART6_TX<br>Remap: TIMER0_CH0_ON |
| PE9 | 60 | I/O | 5VT | Default: PE9<br>Alternate: EXMC_D6<br>Remap: TIMER0_CH0 |
| $V_{SS_7}$ | 61 | P | | Default: $V_{SS_7}$ |
| $V_{DD_7}$ | 62 | P | | Default: $V_{DD_7}$ |
| PE10 | 63 | I/O | 5VT | Default: PE10<br>Alternate: EXMC_D7<br>Remap: TIMER0_CH1_ON |
| PE11 | 64 | I/O | 5VT | Default: PE11<br>Alternate: EXMC_D8<br>Remap: TIMER0_CH1, TLI_G3 |
| PE12 | 65 | I/O | 5VT | Default: PE12<br>Alternate: EXMC_D9<br>Remap: TIMER0_CH2_ON, TLI_B4 |
| PE13 | 66 | I/O | 5VT | Default: PE13<br>Alternate: EXMC_D10<br>Remap: TIMER0_CH2, TLI_DE |
| PE14 | 67 | I/O | 5VT | Default: PE14<br>Alternate: EXMC_D11<br>Remap: TIMER0_CH3, TLI_PIXCLK |
| PE15 | 68 | I/O | 5VT | Default: PE15<br>Alternate: EXMC_D12<br>Remap: TIMER0_BRKIN, TLI_R7 |
| PB10 | 69 | I/O | 5VT | Default: PB10<br>Alternate: I2C1_SCL, USART2_TX<br>Remap: TIMER1_CH2, TLI_G4, SPI1_SCK, I2S1_CK |
| PB11 | 70 | I/O | 5VT | Default: PB11<br>Alternate: I2C1_SDA, USART2_RX<br>Remap: TIMER1_CH3, TLI_G5 |
| $V_{SS_1}$ | 71 | P | | Default: $V_{SS_1}$ |
| $V_{DD_1}$ | 72 | P | | Default: $V_{DD_1}$ |
| PB12 | 73 | I/O | 5VT | Default: PB12<br>Alternate: SPI1_NSS, I2C1_SMBA, USART2_CK, TIMER0_BRKIN, I2S1_WS, CAN1_RX |
| PB13 | 74 | I/O | 5VT | Default: PB13 |



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|---|---|---|---|---|
| | | | | Alternate: SPI1_SCK, USART2_CTS, TIMER0_CH0_ON, I2S1_CK, CAN1_TX |
| PB14 | 75 | I/O | 5VT | Default: PB14<br>Alternate: SPI1_MISO, USART2_RTS, TIMER0_CH1_ON, TIMER11_CH0 |
| PB15 | 76 | I/O | 5VT | Default: PB15<br>Alternate: SPI1_MOSI, TIMER0_CH2_ON, I2S1_SD, TIMER11_CH1 |
| PD8 | 77 | I/O | 5VT | Default: PD8<br>Alternate: EXMC_D13<br>Remap: USART2_TX |
| PD9 | 78 | I/O | 5VT | Default: PD9<br>Alternate: EXMC_D14<br>Remap: USART2_RX |
| PD10 | 79 | I/O | 5VT | Default: PD10<br>Alternate: EXMC_D15<br>Remap: USART2_CK, TLI_B3 |
| PD11 | 80 | I/O | 5VT | Default: PD11<br>Alternate: EXMC_A16<br>Remap: USART2_CTS |
| PD12 | 81 | I/O | 5VT | Default: PD12<br>Alternate: EXMC_A17<br>Remap: TIMER3_CH0, USART2_RTS |
| PD13 | 82 | I/O | 5VT | Default: PD13<br>Alternate: EXMC_A18<br>Remap: TIMER3_CH1 |
| $V_{SS_8}$ | 83 | P | | Default: $V_{SS_8}$ |
| $V_{DD_8}$ | 84 | P | | Default: $V_{DD_8}$ |
| PD14 | 85 | I/O | 5VT | Default: PD14<br>Alternate: EXMC_D0<br>Remap: TIMER3_CH2 |
| PD15 | 86 | I/O | 5VT | Default: PD15<br>Alternate: EXMC_D1<br>Remap: TIMER3_CH3 |
| PG2 | 87 | I/O | 5VT | Default: PG2<br>Alternate: EXMC_A12 |
| PG3 | 88 | I/O | 5VT | Default: PG3<br>Alternate: EXMC_A13 |
| PG4 | 89 | I/O | 5VT | Default: PG4<br>Alternate: EXMC_A14, EXMC_BA0 |
| PG5 | 90 | I/O | 5VT | Default: PG5<br>Alternate: EXMC_A15, EXMC_BA1 |
| PG6 | 91 | I/O | 5VT | Default: PG6<br>Alternate: EXMC_INT1<br>Remap:TLI_R7 |
| PG7 | 92 | I/O | 5VT | Default: PG7 |



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|---|---|---|---|---|
| | | | | Alternate: EXMC_INT2<br>Remap: USART5_CK, TLI_PIXCLK |
| PG8 | 93 | I/O | 5VT | Default: PG8<br>Alternate: EXMC_SDCLK, USART5_RTS |
| $V_{SS_9}$ | 94 | P | | Default: $V_{SS_9}$ |
| $V_{DD_9}$ | 95 | P | | Default: $V_{DD_9}$ |
| PC6 | 96 | I/O | 5VT | Default: PC6<br>Alternate: I2S1_MCK, TIMER7_CH0, SDIO_D6, USART5_TX<br>Remap: TIMER2_CH0, TLI_HSYNC |
| PC7 | 97 | I/O | 5VT | Default: PC7<br>Alternate: I2S2_MCK, TIMER7_CH1, SDIO_D7, USART5_RX<br>Remap: TIMER2_CH1, TLI_G6 |
| PC8 | 98 | I/O | 5VT | Default: PC8<br>Alternate: TIMER7_CH2, SDIO_D0, USART5_CK<br>Remap: TIMER2_CH2 |
| PC9 | 99 | I/O | 5VT | Default: PC9<br>Alternate: TIMER7_CH3, SDIO_D, CK_OUT1<br>Remap: TIMER2_CH3, I2C2_SDA |
| PA8 | 100 | I/O | 5VT | Default: PA8<br>Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, VCORE, USBFS_SOF<br>Remap: TLI_R6, I2C2_SCL |
| PA9 | 101 | I/O | 5VT | Default: PA9<br>Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS<br>Remap: I2C2_SMBAI |
| PA10 | 102 | I/O | 5VT | Default: PA10<br>Alternate: USART0_RX, TIMER0_CH2, USBFS_ID |
| PA11 | 103 | I/O | 5VT | Default: PA11<br>Alternate: USART0_CTS, CAN0_RX, USBFS_DM, TIMER0_CH3<br>Remap: TLI_R4 |
| PA12 | 104 | I/O | 5VT | Default: PA12<br>Alternate: USART0_RTS, USBFS_DP, CAN0_TX, TIMER0_ETI<br>Remap: TLI_R5 |
| PA13 | 105 | I/O | 5VT | Default: JTMS, SWDIO<br>Remap: PA13 |
| NC | 106 | | | - |
| $V_{SS_2}$ | 107 | P | | Default: $V_{SS_2}$ |
| $V_{DD_2}$ | 108 | P | | Default: $V_{DD_2}$ |
| PA14 | 109 | I/O | 5VT | Default: JTCK, SWCLK<br>Remap: PA14 |
| PA15 | 110 | I/O | 5VT | Default: JTDI |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | Alternate: SPI2_NSS, I2S2_WS<br>Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS |
| PC10 | 111 | I/O | 5VT | Default: PC10<br>Alternate: UART3_TX, SDIO_D2<br>Remap: USART2_TX, SPI2_SCK, I2S2_CK, TLI_R2 |
| PC11 | 112 | I/O | 5VT | Default: PC11<br>Alternate: UART3_RX, SDIO_D3<br>Remap: USART2_RX, SPI2_MISO |
| PC12 | 113 | I/O | 5VT | Default: PC12<br>Alternate: UART4_TX, SDIO_CK<br>Remap: USART2_CK, SPI2_MOSI, I2S2_SD |
| PD0 | 114 | I/O | 5VT | Default: PD0<br>Alternate: EXMC_D2<br>Remap: CAN0_RX, OSCIN |
| PD1 | 115 | I/O | 5VT | Default: PD1<br>Alternate: EXMC_D3<br>Remap: CAN0_TX, OSCOUT |
| PD2 | 116 | I/O | 5VT | Default: PD2<br>Alternate: TIMER2_ETI, UART4_RX, SDIO_CMD |
| PD3 | 117 | I/O | 5VT | Default: PD3<br>Alternate: EXMC_CLK<br>Remap: USART1_CTS, TLI_G7, SPI1_SCK, I2S1_CK |
| PD4 | 118 | I/O | 5VT | Default: PD4<br>Alternate: EXMC_NOE<br>Remap: USART1_RTS |
| PD5 | 119 | I/O | 5VT | Default: PD5<br>Alternate: EXMC_NWE<br>Remap: USART1_TX |
| $V_{SS_10}$ | 120 | | | Default: $V_{SS_10}$ |
| $V_{DD_10}$ | 121 | | | Default: $V_{DD_10}$ |
| PD6 | 122 | I/O | 5VT | Default: PD6<br>Alternate: EXMC_NWAIT<br>Remap: USART1_RX, TLI_B2, SPI2_MOSI, I2S2_SD |
| PD7 | 123 | I/O | 5VT | Default: PD7<br>Alternate: EXMC_NE0, EXMC_NCE1<br>Remap: USART1_CK |
| PG9 | 124 | I/O | 5VT | Default: PG9<br>Alternate: EXMC_NE1, EXMC_NCE2<br>Remap: USART5_RX |
| PG10 | 125 | I/O | 5VT | Default: PG10<br>Alternate: EXMC_NCE3_0, EXMC_NE2<br>Remap: TLI_G3, TLI_B2 |
| PG11 | 126 | I/O | 5VT | Default: PG11<br>Alternate: EXMC_NCE3_1<br>Remap: TLI_B3 |
| PG12 | 127 | I/O | 5VT | Default: PG12 |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | Alternate: EXMC_NE3<br>Remap: USART5_RTS, TLI_B4, TLI_B1 |
| PG13 | 128 | I/O | 5VT | Default: PG13<br>Alternate: EXMC_A24<br>Remap: USART5_CTS |
| PG14 | 129 | I/O | 5VT | Default: PG14<br>Alternate: EXMC_A25<br>Remap: USART5_TX |
| $V_{SS_11}$ | 130 | P | | Default: $V_{SS_10}$ |
| $V_{DD_11}$ | 131 | P | | Default: $V_{DD_10}$ |
| PG15 | 132 | I/O | 5VT | Default: PG15<br>Alternate: EXMC_SDNCAS, USART5_CTS |
| PB3 | 133 | I/O | 5VT | Default: JTDO<br>Alternate:SPI2_SCK, I2S2_CK<br>Remap: PB3, TRACESWO, TIMER1_CH1, SPI0_SCK |
| PB4 | 134 | I/O | 5VT | Default: JNTRST<br>Alternate: SPI2_MISO<br>Remap: TIMER2_CH0, PB4, SPI0_MISO |
| PB5 | 135 | I/O | | Default: PB5<br>Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD<br>Remap: TIMER2_CH1, SPI0_MOSI, CAN1_RX, EXMC_SDCKE1 |
| PB6 | 136 | I/O | 5VT | Default: PB6<br>Alternate: I2C0_SCL, TIMER3_CH0<br>Remap: USART0_TX, CAN1_TX, EXMC_SDNE1, SPI0_IO3 |
| PB7 | 137 | I/O | 5VT | Default: PB7<br>Alternate: I2C0_SDA , TIMER3_CH1, EXMC_NL<br>Remap: USART0_RX, SPI0_IO4 |
| BOOT0 | 138 | I | | Default: BOOT0 |
| PB8 | 139 | I/O | 5VT | Default: PB8<br>Alternate: TIMER3_CH2, TIMER9_CH0, SDIO_D4<br>Remap: I2C0_SCL, CAN0_RX, TLI_B6 |
| PB9 | 140 | I/O | 5VT | Default: PB9<br>Alternate: TIMER3_CH3, TIMER10_CH0, SDIO_D5<br>Remap: I2C0_SDA, CAN0_TX, TLI_B7, SPI1_NSS, I2S1_WS |
| PE0 | 141 | I/O | 5VT | Default: PE0<br>Alternate: TIMER3_ETI, EXMC_NBL0, UART7_RX |
| PE1 | 142 | I/O | 5VT | Default: PE1<br>Alternate: EXMC_NBL1, UART7_TX |
| $V_{SS_3}$ | 143 | P | | Default: $V_{SS_3}$ |
| $V_{DD_3}$ | 144 | P | | Default: $V_{DD_3}$ |

**Notes:**

(1) Type: I = input, O = output, P = power.



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(2) I/O Level: 5VT = 5 V tolerant.



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### 2.6.2. GD32F205Vx LQFP100 pin definitions

**Table 2-4. GD32F205Vx LQFP100 pin definitions**

| Pin Name | Pins | Pin Type(1) | I/O(2) Level | Functions description |
|---|---|---|---|---|
| PE2 | 1 | I/O | 5VT | Default: PE2<br>Alternate: TRACECK, EXMC_A23 |
| PE3 | 2 | I/O | 5VT | Default: PE3<br>Alternate: TRACED0, EXMC_A19 |
| PE4 | 3 | I/O | 5VT | Default: PE4<br>Alternate:TRACED1, EXMC_A20<br>Remap: TLI_B0 |
| PE5 | 4 | I/O | 5VT | Default: PE5<br>Alternate:TRACED2, EXMC_A21<br>Remap: TIMER8_CH0, TLI_G0 |
| PE6 | 5 | I/O | 5VT | Default: PE6<br>Alternate:TRACED3, EXMC_A22<br>Remap: TIMER8_CH1, TLI_G1 |
| $V_{BAT}$ | 6 | P | | Default: $V_{BAT}$ |
| PC13-TAMPER-RTC | 7 | I/O | | Default: PC13<br>Alternate: TAMPER-RTC |
| PC14-OSC32IN | 8 | I/O | | Default: PC14<br>Alternate: OSC32IN |
| PC15-OSC32OUT | 9 | I/O | | Default: PC15<br>Alternate: OSC32OUT |
| $V_{SS_5}$ | 10 | P | | Default: $V_{SS_5}$ |
| $V_{DD_5}$ | 11 | P | | Default: $V_{DD_5}$ |
| OSCIN | 12 | I | | Default: OSCIN<br>Remap: PH0 |
| OSCOUT | 13 | O | | Default: OSCOUT<br>Remap: PH1 |
| NRST | 14 | I/O | | Default: NRST |
| PC0 | 15 | I/O | | Default: PC0<br>Alternate: ADC012_IN10<br>Remap: EXMC_SDNWE |
| PC1 | 16 | I/O | | Default: PC1<br>Alternate: ADC012_IN11 |
| PC2 | 17 | I/O | | Default: PC2<br>Alternate: ADC012_IN12<br>Remap: EXMC_SDNE0, SPI1_MISO |
| PC3 | 18 | I/O | | Default: PC3<br>Alternate: ADC012_IN13<br>Remap: EXMC_SDCKE0, SPI1_MOSI, I2S1_SD |
| $V_{SSA}$ | 19 | P | | Default: $V_{SSA}$ |
| $V_{REF-}$ | 20 | P | | Default: $V_{REF-}$ |



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| Pin Name | Pins | Pin Type(1) | I/O(2) Level | Functions description |
|---|---|---|---|---|
| $V_{REF+}$ | 21 | P | | Default: $V_{REF+}$ |
| $V_{DDA}$ | 22 | P | | Default: $V_{DDA}$ |
| PA0-WKUP | 23 | I/O | | Default: PA0<br>Alternate: WKUP, USART1_CTS, ADC012_IN0, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI<br>Remap: UART3_TX |
| PA1 | 24 | I/O | | Default: PA1<br>Alternate: USART1_RTS, ADC012_IN1, TIMER1_CH1, TIMER4_CH1<br>Remap: UART3_RX |
| PA2 | 25 | I/O | | Default: PA2<br>Alternate: USART1_TX, ADC012_IN2, TIMER1_CH2, TIMER4_CH2, TIMER8_CH0, SPI0_IO3 |
| PA3 | 26 | I/O | | Default: PA3<br>Alternate: USART1_RX, ADC012_IN3, TIMER1_CH3, TIMER4_CH3, TIMER8_CH1, SPI0_IO4<br>Remap: TLI_B5 |
| $V_{SS_4}$ | 27 | P | | Default: $V_{SS_4}$ |
| $V_{DD_4}$ | 28 | P | | Default: $V_{DD_4}$ |
| PA4 | 29 | I/O | | Default: PA4<br>Alternate: SPI0_NSS, USART1_CK, DAC_OUT0, ADC01_IN4<br>Remap: SPI2_NSS, I2S2_WS, TLI_VSYNC |
| PA5 | 30 | I/O | | Default: PA5<br>Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1<br>Remap: TIMER1_CH0, TIMER1_ETI, TIMER7_CH0_ON |
| PA6 | 31 | I/O | | Default: PA6<br>Alternate: SPI0_MISO, ADC01_IN6, TIMER2_CH0, TIMER7_BRKIN, TIMER12_CH0<br>Remap: TIMER0_BRKIN, TLI_G2 |
| PA7 | 32 | I/O | | Default: PA7<br>Alternate: SPI0_MOSI, ADC01_IN7, TIMER2_CH1, TIMER7_CH0_ON, TIMER13_CH0<br>Remap: TIMER0_CH0_ON |
| PC4 | 33 | I/O | | Default: PC4<br>Alternate: ADC01_IN14 |
| PC5 | 34 | I/O | | Default: PC5<br>Alternate: ADC01_IN15 |
| PB0 | 35 | I/O | | Default: PB0<br>Alternate: ADC01_IN8, TIMER2_CH2, TIMER7_CH1_ON<br>Remap: TIMER0_CH1_ON, TLI_R3 |
| PB1 | 36 | I/O | | Default: PB1<br>Alternate: ADC01_IN9, TIMER2_CH3, TIMER7_CH2_ON<br>Remap: TIMER0_CH2_ON, TLI_R6 |
| PB2 | 37 | I/O | 5VT | Default: PB2, BOOT1 |
| PE7 | 38 | I/O | 5VT | Default: PE7 |



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| Pin Name | Pins | Pin Type(1) | I/O(2) Level | Functions description |
|---|---|---|---|---|
| | | | | Alternate: EXMC_D4, UART6_RX<br>Remap: TIMER0_ETI |
| PE8 | 39 | I/O | 5VT | Default: PE8<br>Alternate: EXMC_D5, UART6_TX<br>Remap: TIMER0_CH0_ON |
| PE9 | 40 | I/O | 5VT | Default: PE9<br>Alternate: EXMC_D6<br>Remap: TIMER0_CH0 |
| PE10 | 41 | I/O | 5VT | Default: PE10<br>Alternate: EXMC_D7<br>Remap: TIMER0_CH1_ON |
| PE11 | 42 | I/O | 5VT | Default: PE11<br>Alternate: EXMC_D8<br>Remap: TIMER0_CH1, TLI_G3 |
| PE12 | 43 | I/O | 5VT | Default: PE12<br>Alternate: EXMC_D9<br>Remap: TIMER0_CH2_ON, TLI_B4 |
| PE13 | 44 | I/O | 5VT | Default: PE13<br>Alternate: EXMC_D10<br>Remap: TIMER0_CH2, TLI_DE |
| PE14 | 45 | I/O | 5VT | Default: PE14<br>Alternate: EXMC_D11<br>Remap: TIMER0_CH3, TLI_PIXCLK |
| PE15 | 46 | I/O | 5VT | Default: PE15<br>Alternate: EXMC_D12<br>Remap: TIMER0_BRKIN, TLI_R7 |
| PB10 | 47 | I/O | 5VT | Default: PB10<br>Alternate: I2C1_SCL, USART2_TX<br>Remap: TIMER1_CH2, TLI_G4, SPI1_SCK, I2S1_CK |
| PB11 | 48 | I/O | 5VT | Default: PB11<br>Alternate: I2C1_SDA, USART2_RX<br>Remap: TIMER1_CH3, TLI_G5 |
| $V_{SS_1}$ | 49 | P | | Default: $V_{SS_1}$ |
| $V_{DD_1}$ | 50 | P | | Default: $V_{DD_1}$ |
| PB12 | 51 | I/O | 5VT | Default: PB12<br>Alternate: SPI1_NSS, I2C1_SMBA, USART2_CK, TIMER0_BRKIN, I2S1_WS, CAN1_RX |
| PB13 | 52 | I/O | 5VT | Default: PB13<br>Alternate: SPI1_SCK, USART2_CTS, TIMER0_CH0_ON, I2S1_CK, CAN1_TX |
| PB14 | 53 | I/O | 5VT | Default: PB14<br>Alternate: SPI1_MISO, USART2_RTS, TIMER0_CH1_ON, TIMER11_CH0 |
| PB15 | 54 | I/O | 5VT | Default: PB15<br>Alternate: SPI1_MOSI, TIMER0_CH2_ON, I2S1_SD, TIMER11_CH1 |



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| Pin Name | Pins | Pin Type(1) | I/O(2) Level | Functions description |
|---|---|---|---|---|
| PD8 | 55 | I/O | 5VT | Default: PD8<br>Alternate: EXMC_D13<br>Remap: USART2_TX |
| PD9 | 56 | I/O | 5VT | Default: PD9<br>Alternate: EXMC_D14<br>Remap: USART2_RX |
| PD10 | 57 | I/O | 5VT | Default: PD10<br>Alternate: EXMC_D15<br>Remap: USART2_CK, TLI_B3 |
| PD11 | 58 | I/O | 5VT | Default: PD11<br>Alternate: EXMC_A16<br>Remap: USART2_CTS |
| PD12 | 59 | I/O | 5VT | Default: PD12<br>Alternate: EXMC_A17<br>Remap: TIMER3_CH0, USART2_RTS |
| PD13 | 60 | I/O | 5VT | Default: PD13<br>Alternate: EXMC_A18<br>Remap: TIMER3_CH1 |
| PD14 | 61 | I/O | 5VT | Default: PD14<br>Alternate: EXMC_D0<br>Remap: TIMER3_CH2 |
| PD15 | 62 | I/O | 5VT | Default: PD15<br>Alternate: EXMC_D1<br>Remap: TIMER3_CH3 |
| PC6 | 63 | I/O | 5VT | Default: PC6<br>Alternate: I2S1_MCK, TIMER7_CH0, SDIO_D6, USART5_TX<br>Remap: TIMER2_CH0, TLI_HSYNC |
| PC7 | 64 | I/O | 5VT | Default: PC7<br>Alternate: I2S2_MCK, TIMER7_CH1, SDIO_D7, USART5_RX<br>Remap: TIMER2_CH1, TLI_G6 |
| PC8 | 65 | I/O | 5VT | Default: PC8<br>Alternate: TIMER7_CH2, SDIO_D0, USART5_CK<br>Remap: TIMER2_CH2 |
| PC9 | 66 | I/O | 5VT | Default: PC9<br>Alternate: TIMER7_CH3, SDIO_D, CK_OUT1<br>Remap: TIMER2_CH3, I2C2_SDA |
| PA8 | 67 | I/O | 5VT | Default: PA8<br>Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, VCORE, USBFS_SOF<br>Remap: TLI_R6, I2C2_SCL |
| PA9 | 68 | I/O | 5VT | Default: PA9<br>Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS<br>Remap: I2C2_SMBAI |
| PA10 | 69 | I/O | 5VT | Default: PA10<br>Alternate: USART0_RX, TIMER0_CH2, USBFS_ID |
| PA11 | 70 | I/O | 5VT | Default: PA11 |



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| Pin Name | Pins | Pin Type(1) | I/O(2) Level | Functions description |
|---|---|---|---|---|
| | | | | Alternate: USART0_CTS, CAN0_RX, USBFS_DM, TIMER0_CH3<br>Remap: TLI_R4 |
| PA12 | 71 | I/O | 5VT | Default: PA12<br>Alternate: USART0_RTS, USBFS_DP, CAN0_TX, TIMER0_ETI<br>Remap: TLI_R5 |
| PA13 | 72 | I/O | 5VT | Default: JTMS, SWDIO<br>Remap: PA13 |
| NC | 73 | | | - |
| $V_{SS_2}$ | 74 | P | | Default: $V_{SS_2}$ |
| $V_{DD_2}$ | 75 | P | | Default: $V_{DD_2}$ |
| PA14 | 76 | I/O | 5VT | Default: JTCK, SWCLK<br>Remap: PA14 |
| PA15 | 77 | I/O | 5VT | Default: JTDI<br>Alternate: SPI2_NSS, I2S2_WS<br>Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS |
| PC10 | 78 | I/O | 5VT | Default: PC10<br>Alternate: UART3_TX, SDIO_D2<br>Remap: USART2_TX, SPI2_SCK, I2S2_CK, TLI_R2 |
| PC11 | 79 | I/O | 5VT | Default: PC11<br>Alternate: UART3_RX, SDIO_D3<br>Remap: USART2_RX, SPI2_MISO |
| PC12 | 80 | I/O | 5VT | Default: PC12<br>Alternate: UART4_TX, SDIO_CK<br>Remap: USART2_CK, SPI2_MOSI, I2S2_SD |
| PD0 | 81 | I/O | 5VT | Default: PD0<br>Alternate: EXMC_D2<br>Remap: CAN0_RX, OSCIN |
| PD1 | 82 | I/O | 5VT | Default: PD1<br>Alternate: EXMC_D3<br>Remap: CAN0_TX, OSCOUT |
| PD2 | 83 | I/O | 5VT | Default: PD2<br>Alternate: TIMER2_ETI, UART4_RX, SDIO_CMD |
| PD3 | 84 | I/O | 5VT | Default: PD3<br>Alternate: EXMC_CLK<br>Remap: USART1_CTS, TLI_G7, SPI1_SCK, I2S1_CK |
| PD4 | 85 | I/O | 5VT | Default: PD4<br>Alternate: EXMC_NOE<br>Remap: USART1_RTS |
| PD5 | 86 | I/O | 5VT | Default: PD5<br>Alternate: EXMC_NWE<br>Remap: USART1_TX |
| PD6 | 87 | I/O | 5VT | Default: PD6<br>Alternate: EXMC_NWAIT<br>Remap: USART1_RX, TLI_B2, SPI2_MOSI, I2S2_SD |



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| Pin Name | Pins | Pin Type(1) | I/O(2) Level | Functions description |
|---|---|---|---|---|
| PD7 | 88 | I/O | 5VT | Default: PD7<br>Alternate: EXMC_NE0, EXMC_NCE1<br>Remap: USART1_CK |
| PB3 | 89 | I/O | 5VT | Default: JTDO<br>Alternate:SPI2_SCK, I2S2_CK<br>Remap: PB3, TRACESWO, TIMER1_CH1, SPI0_SCK |
| PB4 | 90 | I/O | 5VT | Default: JNTRST<br>Alternate: SPI2_MISO<br>Remap: TIMER2_CH0, PB4, SPI0_MISO |
| PB5 | 91 | I/O | | Default: PB5<br>Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD<br>Remap: TIMER2_CH1, SPI0_MOSI, CAN1_RX,<br>EXMC_SDCKE1 |
| PB6 | 92 | I/O | 5VT | Default: PB6<br>Alternate: I2C0_SCL, TIMER3_CH0<br>Remap: USART0_TX, CAN1_TX, EXMC_SDNE1, SPI0_IO3 |
| PB7 | 93 | I/O | 5VT | Default: PB7<br>Alternate: I2C0_SDA , TIMER3_CH1, EXMC_NL<br>Remap: USART0_RX, SPI0_IO4 |
| BOOT0 | 94 | I | | Default: BOOT0 |
| PB8 | 95 | I/O | 5VT | Default: PB8<br>Alternate: TIMER3_CH2, TIMER9_CH0, SDIO_D4<br>Remap: I2C0_SCL, CAN0_RX, TLI_B6 |
| PB9 | 96 | I/O | 5VT | Default: PB9<br>Alternate: TIMER3_CH3, TIMER10_CH0, SDIO_D5<br>Remap: I2C0_SDA, CAN0_TX, TLI_B7, SPI1_NSS, I2S1_WS |
| PE0 | 97 | I/O | 5VT | Default: PE0<br>Alternate: TIMER3_ETI, EXMC_NBL0, UART7_RX |
| PE1 | 98 | I/O | 5VT | Default: PE1<br>Alternate: EXMC_NBL1, UART7_TX |
| $V_{SS_3}$ | 99 | P | | Default: $V_{SS_3}$ |
| $V_{DD_3}$ | 100 | P | | Default: $V_{DD_3}$ |

**Notes:**

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.



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### 2.6.3. GD32F205Rx LQFP64 pin definitions

**Table 2-5. GD32F205Rx LQFP64 pin definitions**

| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| $V_{BAT}$ | 1 | P | | Default: $V_{BAT}$ |
| PC13-TAMPER-RTC | 2 | I/O | | Default: PC13<br>Alternate: TAMPER-RTC |
| PC14-OSC32IN | 3 | I/O | | Default: PC14<br>Alternate: OSC32IN |
| PC15-OSC32OUT | 4 | I/O | | Default: PC15<br>Alternate: OSC32OUT |
| OSCIN | 5 | I | | Default: OSCIN<br>Remap: PD0 |
| OSCOUT | 6 | O | | Default: OSCOUT<br>Remap: PD1 |
| NRST | 7 | I/O | | Default: NRST |
| PC0 | 8 | I/O | | Default: PC0<br>Alternate: ADC012_IN10<br>Remap: EXMC_SDNWE |
| PC1 | 9 | I/O | | Default: PC1<br>Alternate: ADC012_IN11 |
| PC2 | 10 | I/O | | Default: PC2<br>Alternate: ADC012_IN12<br>Remap: EXMC_SDNE0, SPI1_MISO |
| PC3 | 11 | I/O | | Default: PC3<br>Alternate: ADC012_IN13<br>Remap: EXMC_SDCKE0, SPI1_MOSI, I2S1_SD |
| $V_{SSA}$ | 12 | P | | Default: $V_{SSA}$ |
| $V_{DDA}$ | 13 | P | | Default: $V_{DDA}$ |
| PA0-WKUP | 14 | I/O | | Default: PA0<br>Alternate: WKUP, USART1_CTS, ADC012_IN0, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI<br>Remap: UART3_TX |
| PA1 | 15 | I/O | | Default: PA1<br>Alternate: USART1_RTS, ADC012_IN1, TIMER1_CH1, TIMER4_CH1<br>Remap: UART3_RX |
| PA2 | 16 | I/O | | Default: PA2<br>Alternate: USART1_TX, ADC012_IN2, TIMER1_CH2, TIMER4_CH2, TIMER8_CH0, SPI0_IO3 |
| PA3 | 17 | I/O | | Default: PA3<br>Alternate: USART1_RX, ADC012_IN3, TIMER1_CH3, TIMER4_CH3, TIMER8_CH1, SPI0_IO4<br>Remap: TLI_B5 |
| $V_{SS_4}$ | 18 | P | | Default: $V_{SS_4}$ |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| $V_{DD_4}$ | 19 | P | | Default: $V_{DD_4}$ |
| PA4 | 20 | I/O | | Default: PA4<br>Alternate: SPI0_NSS, USART1_CK, DAC_OUT0, ADC01_IN4<br>Remap: SPI2_NSS, I2S2_WS, TLI_VSYNC |
| PA5 | 21 | I/O | | Default: PA5<br>Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1<br>Remap: TIMER1_CH0, TIMER1_ETI, TIMER7_CH0_ON |
| PA6 | 22 | I/O | | Default: PA6<br>Alternate: SPI0_MISO, ADC01_IN6, TIMER2_CH0, TIMER7_BRKIN, TIMER12_CH0<br>Remap: TIMER0_BRKIN, TLI_G2 |
| PA7 | 23 | I/O | | Default: PA7<br>Alternate: SPI0_MOSI, ADC01_IN7, TIMER2_CH1, TIMER7_CH0_ON, TIMER13_CH0<br>Remap: TIMER0_CH0_ON |
| PC4 | 24 | I/O | | Default: PC4<br>Alternate: ADC01_IN14 |
| PC5 | 25 | I/O | | Default: PC5<br>Alternate: ADC01_IN15 |
| PB0 | 26 | I/O | | Default: PB0<br>Alternate: ADC01_IN8, TIMER2_CH2, TIMER7_CH1_ON<br>Remap: TIMER0_CH1_ON, TLI_R3 |
| PB1 | 27 | I/O | | Default: PB1<br>Alternate: ADC01_IN9, TIMER2_CH3, TIMER7_CH2_ON<br>Remap: TIMER0_CH2_ON, TLI_R6 |
| PB2 | 28 | I/O | 5VT | Default: PB2, BOOT1 |
| PB10 | 29 | I/O | 5VT | Default: PB10<br>Alternate: I2C1_SCL, USART2_TX<br>Remap: TIMER1_CH2, TLI_G4, SPI1_SCK, I2S1_CK |
| PB11 | 30 | I/O | 5VT | Default: PB11<br>Alternate: I2C1_SDA, USART2_RX<br>Remap: TIMER1_CH3, TLI_G5 |
| $V_{SS_1}$ | 31 | P | | Default: $V_{SS_1}$ |
| $V_{DD_1}$ | 32 | P | | Default: $V_{DD_1}$ |
| PB12 | 33 | I/O | 5VT | Default: PB12<br>Alternate: SPI1_NSS, I2C1_SMBA, USART2_CK, TIMER0_BRKIN, I2S1_WS, CAN1_RX |
| PB13 | 34 | I/O | 5VT | Default: PB13<br>Alternate: SPI1_SCK, USART2_CTS, TIMER0_CH0_ON, I2S1_CK, CAN1_TX |
| PB14 | 35 | I/O | 5VT | Default: PB14<br>Alternate: SPI1_MISO, USART2_RTS, TIMER0_CH1_ON, TIMER11_CH0 |
| PB15 | 36 | I/O | 5VT | Default: PB15 |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | Alternate: SPI1_MOSI, TIMER0_CH2_ON, I2S1_SD, TIMER11_CH1 |
| PC6 | 37 | I/O | 5VT | Default: PC6<br>Alternate: I2S1_MCK, TIMER7_CH0, SDIO_D6, USART5_TX<br>Remap: TIMER2_CH0, TLI_HSYNC |
| PC7 | 38 | I/O | 5VT | Default: PC7<br>Alternate: I2S2_MCK, TIMER7_CH1, SDIO_D7, USART5_RX<br>Remap: TIMER2_CH1, TLI_G6 |
| PC8 | 39 | I/O | 5VT | Default: PC8<br>Alternate: TIMER7_CH2, SDIO_D0, USART5_CK<br>Remap: TIMER2_CH2 |
| PC9 | 40 | I/O | 5VT | Default: PC9<br>Alternate: TIMER7_CH3, SDIO_D, CK_OUT1<br>Remap: TIMER2_CH3, I2C2_SDA |
| PA8 | 41 | I/O | 5VT | Default: PA8<br>Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, VCORE, USBFS_SOF<br>Remap: TLI_R6, I2C2_SCL |
| PA9 | 42 | I/O | 5VT | Default: PA9<br>Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS<br>Remap: I2C2_SMBAI |
| PA10 | 43 | I/O | 5VT | Default: PA10<br>Alternate: USART0_RX, TIMER0_CH2, USBFS_ID |
| PA11 | 44 | I/O | 5VT | Default: PA11<br>Alternate: USART0_CTS, CAN0_RX, USBFS_DM, TIMER0_CH3<br>Remap: TLI_R4 |
| PA12 | 45 | I/O | 5VT | Default: PA12<br>Alternate: USART0_RTS, USBFS_DP, CAN0_TX, TIMER0_ETI<br>Remap: TLI_R5 |
| PA13 | 46 | I/O | 5VT | Default: JTMS, SWDIO<br>Remap: PA13 |
| $V_{SS_2}$ | 47 | P | | Default: $V_{SS_2}$ |
| $V_{DD_2}$ | 48 | P | | Default: $V_{DD_2}$ |
| PA14 | 49 | I/O | 5VT | Default: JTCK, SWCLK<br>Remap: PA14 |
| PA15 | 50 | I/O | 5VT | Default: JTDI<br>Alternate: SPI2_NSS, I2S2_WS<br>Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS |
| PC10 | 51 | I/O | 5VT | Default: PC10<br>Alternate: UART3_TX, SDIO_D2<br>Remap: USART2_TX, SPI2_SCK, I2S2_CK, TLI_R2 |
| PC11 | 52 | I/O | 5VT | Default: PC11<br>Alternate: UART3_RX, SDIO_D3 |



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| Pin Name | Pins | Pin Type(1) | I/O Level(2) | Functions description |
|---|---|---|---|---|
| | | | | Remap: USART2_RX, SPI2_MISO |
| PC12 | 53 | I/O | 5VT | Default: PC12<br>Alternate: UART4_TX, SDIO_CK<br>Remap: USART2_CK, SPI2_MOSI, I2S2_SD |
| PD2 | 54 | I/O | 5VT | Default: PD2<br>Alternate: TIMER2_ETI, UART4_RX, SDIO_CMD |
| PB3 | 55 | I/O | 5VT | Default: JTDO<br>Alternate:SPI2_SCK, I2S2_CK<br>Remap: PB3, TRACESWO, TIMER1_CH1, SPI0_SCK |
| PB4 | 56 | I/O | 5VT | Default: JNTRST<br>Alternate: SPI2_MISO<br>Remap: TIMER2_CH0, PB4, SPI0_MISO |
| PB5 | 57 | I/O | | Default: PB5<br>Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD<br>Remap: TIMER2_CH1, SPI0_MOSI, CAN1_RX, EXMC_SDCKE1 |
| PB6 | 58 | I/O | 5VT | Default: PB6<br>Alternate: I2C0_SCL, TIMER3_CH0<br>Remap: USART0_TX, CAN1_TX, EXMC_SDNE1, SPI0_IO3 |
| PB7 | 59 | I/O | 5VT | Default: PB7<br>Alternate: I2C0_SDA , TIMER3_CH1, EXMC_NL<br>Remap: USART0_RX, SPI0_IO4 |
| BOOT0 | 60 | I | | Default: BOOT0 |
| PB8 | 61 | I/O | 5VT | Default: PB8<br>Alternate: TIMER3_CH2, TIMER9_CH0, SDIO_D4<br>Remap: I2C0_SCL, CAN0_RX, TLI_B6 |
| PB9 | 62 | I/O | 5VT | Default: PB9<br>Alternate: TIMER3_CH3, TIMER10_CH0, SDIO_D5<br>Remap: I2C0_SDA, CAN0_TX, TLI_B7, SPI1_NSS, I2S1_WS |
| $V_{SS_3}$ | 63 | P | | Default: $V_{SS_3}$ |
| $V_{DD_3}$ | 64 | P | | Default: $V_{DD_3}$ |

**Notes:**

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.



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# 3. Functional description

## 3.1. ARM® Cortex®-M3 core

The Cortex®-M3 processor is the latest generation of ARM® processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

- 32-bit ARM® Cortex®-M3 processor core
- Up to 120 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M3:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Memory Protection Unit (MPU)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

## 3.2. On-chip memory

- Up to 3072 Kbytes of flash memory, including code flash and data flash
- Up to 256 Kbytes of SRAM

The ARM® Cortex®-M3 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 3072 Kbytes of inner flash at most, which includes code flash and data flash is available for storing programs and data, and accessed (R/W) at CPU clock speed with zero wait states. Up to 256 Kbytes of inner SRAM is composed of SRAM0, SRAM1, and SRAM2 that can be accessed at same time. ***Table 2-2 GD32F205xx memory map*** shows the memory map of the GD32F205xx series of devices, including flash, SRAM, peripheral, and other pre-defined regions.



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## 3.3. Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 3 to 25 MHz crystal oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB/APB2/APB1 domains is 120/120/60 MHz. See ***Figure 2-5. GD32F205xx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 2.6 V and down to 1.8V. The device remains in reset mode when $V_{DD}$ is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- $V_{DD}$ range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through $V_{DD}$ pins.
- $V_{SSA}$, $V_{DDA}$ range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.
- $V_{BAT}$ range: 1.8 to 3.6 V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.

## 3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the flash memory by using USART0 (PA9 and PA10), USART1 (PD5 and PD6) and USB (PA9, PA10, PA11 and PA12). It also can be used to transfer and update the flash memory code, the data and the vector table sections. In default condition, boot from bank 0 of flash memory is selected. It also supports to boot from bank 1 of flash memory by setting a bit in option bytes.



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## 3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC8M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, the LVD output, and USB wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.
- **Standby** mode
  In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. The contents of SRAM and registers (except backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, and the rising edge on WKUP pin.

## 3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC engine with up to 2 MSPS conversion rate
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Conversion range: $V_{SSA}$ to $V_{DDA}$ (2.6 to 3.6 V)
- Temperature sensor

Up to three 12-bit 2 MSPS multi-channel ADC are integrated in the device. It is a total of up to 16 multiplexed external channels with 2 internal channels for temperature sensor and voltage reference measurement. The conversion range is between 2.6 V < $V_{DDA}$ < 3.6 V. An on-chip 16-bit hardware oversample scheme improves performances while off-loading the related computational burden from the MCU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block of analog inputs also can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced usages.

The ADC can be triggered from the events generated by the general level 0 timers (TIMERx) and the advanced timers (TIMER0 and TIMER7) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally



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connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

## 3.7. Digital to analog converter (DAC)

- 12-bit DAC converter of independent output channel
- 8-bit or 12-bit mode in conjunction with the DMA controller

The 12-bit buffered DAC channel is used to generate variable analog outputs. The DAC is designed with integrated resistor strings structure. The DAC channels can be triggered by the timer update outputs or EXTI with DMA support. The maximum output value of the DAC is $V_{REF+}$.

## 3.8. DMA

- 14 channels DMA controller and each channel are configurable (7 for DMA0 and 7 for DMA1)
- Peripherals supported: Timers, ADC, SPIs, I2Cs, USARTs, DAC, I2S and SDIO

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

## 3.9. General-purpose inputs/outputs (GPIOs)

- Up to 114 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 114 general purpose I/O pins (GPIO) in GD32F205xx, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0 ~ PF15, PG0 ~ PG15, PH0 ~ PH1 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with



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digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

## 3.10. Timers and PWM generation

- Two 16-bit advanced timer (TIMER0 & TIMER7), ten 16-bit general timers (TIMER1 ~ TIMER4, TIMER8 ~ TIMER13), and two 16-bit basic timer (TIMER5 & TIMER6)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0 & TIMER7) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge- or center-aligned counting modes) and single pulse mode output. If configured as a 16-bit general timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer, known as TIMER1 ~ TIMER4, TIMER8 ~ TIMER13 can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. The general timer is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. TIMER1 ~ TIMER4 and TIMER8/TIMER11 also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5 & TIMER6, are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32F205xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler, it is clocked from an independent 40 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.



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The SysTick timer is dedicated for OS, but could also be used as a standard down counter.

The features are shown below:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

## 3.11. Real time clock (RTC) and backup registers

- 32-bit up-counter with a programmable 20-bit prescaler
- Alarm function
- Interrupt and wake-up event
- 84 bytes backup registers for data protection

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 KHz from external crystal oscillator.

The backup registers are located in the backup domain that remains powered-on by $V_{BAT}$ even if $V_{DD}$ power is shut down, they are forty two 16-bit (84 bytes) registers for data protection of user application data, and the wake-up action from standby mode or system reset do not affect these registers.

In addition, the backup registers can be used to implement the tamper detection, RTC calibration function and waveform detection.

## 3.12. Inter-integrated circuit (I2C)

- Up to three I2C bus interfaces can support both master and slave mode with a frequency up to 400 KHz
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides transfer rate of up to 100 KHz in standard mode and up to 400 KHz in fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking



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for I2C data.

## 3.13. Serial peripheral interface (SPI)

- Up to three SPI interfaces with a frequency of up to 30 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking
- Quad wire configuration available in master mode (only in SPI0)

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is also supported in SPI0.

## 3.14. Universal synchronous/asynchronous receiver transmitter (USART/UART)

- Up to four USARTs and four UARTs with operating frequency up to 7.5 MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1, USART2, USART5) and UART (UART3, UART4, UART6, UART7) are used to transmit data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART/UART transmitter and receiver. The USART/UART also supports DMA function for high speed data communication.

## 3.15. Inter-IC sound (I2S)

- Two I2S bus Interfaces with sampling frequency from 8 KHz to 192 KHz, multiplexed with SPI1 and SPI2
- Support either master or slave mode audio
- Sampling frequencies from 8 KHz up to 192 KHz are supported.

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 3-wire serial lines. GD32F205xx contain an I2S-bus interface that can be operated with 16/32-bit resolution in master or slave mode, pin multiplexed with SPI1 and



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SPI2. The audio sampling frequencies from 8 KHz to 192 KHz is supported with less than 0.5% accuracy error.

## 3.16. Universal serial bus full-speed interface (USBFS)

- One USB device/host full-speed Interface with frequency up to 12 Mbit/s
- Internal main PLL for USB CLK compliantly

The Universal Serial Bus (USB) is a 4-wire bus with 4 bidirectional endpoints. The device controller enables 12 Mbit/s data exchange with integrated transceivers in device/host mode. Full-speed peripheral is compliant with the USB 2.0 specification. Transaction formatting is performed by the hardware, including CRC generation and checking. The status of a completed USB transfer or error condition is indicated by status registers. An interrupt is also generated if enabled. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HXTAL crystal oscillator) and the operating frequency divided from APB1 should be 12 MHz above.

## 3.17. Controller area network (CAN)

- Two CAN2.0B interface with communication frequency up to 1 Mbit/s
- Internal main PLL for CAN CLK compliantly

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three mailboxes for transmission and two FIFOs of three message deep for reception. It also provides 28 scalable/configurable identifier filter banks for selecting the incoming messages needed and discarding the others.

## 3.18. External memory controller (EXMC)

- Supported external memory: SRAM, PSRAM, ROM and NOR-Flash, NAND Flash and PC card, SDRAM with up to 32-bit data bus
- Provide ECC calculating hardware module for NAND Flash memory block
- Two SDRAM banks with independent configuration, up to 13-bits Row Address, 11-bits Column Address, 2-bits internal banks address
- SDRAM Memory size: 4x16Mx32bit(256 MB), 4x16Mx16bit (128 MB), 4x16Mx8bit (64 MB)

External memory controller (EXMC) is an abbreviation of external memory controller. It is divided into several sub-banks for external device support, each sub-bank has its own chip selection signal but at one time, only one bank can be accessed. The EXMC support code execution from external memory except NAND Flash and PC card. The EXMC also can be



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configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

The EXMC of GD32F205xx in LQFP144 package also supports synchronous dynamic random access memory (SDRAM). It translates AHB transactions into the appropriate SDRAM protocol, and meanwhile, makes sure the access time requirements of the external SDRAM devices are satisfied.

## 3.19. Secure digital input and output card interface (SDIO)

- Support SD2.0/SDIO2.0/MMC4.2 host interface

The Secure Digital Input and Output Card Interface (SDIO) provides access to external SD memory cards specifications version 2.0, SDIO card specification version 2.0 and multi-media card system specification version 4.2 with DMA supported. In addition, this interface is also compliant with CE-ATA digital protocol rev1.1.

## 3.20. TFT LCD interface (TLI)

- 24-bit RGB Parallel Pixel Output; 8 bits-per-pixel (RGB888)
- Supports up to SVGA (800x600) resolution

The TFT LCD interface provides a parallel digital RGB (Red, Green, Blue) and signals for horizontal, vertical synchronization, pixel clock and data enable as output to interface directly to a variety of LCD (Liquid Crystal Display) and TFT (Thin Film Transistor) panels. A built-in DMA engine continuously move data from system memory to TLI and then, output to an external LCD display. Two separate layers are supported in TLI, as well as layer window and blending function.

## 3.21. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

## 3.22. Package and operation temperature

- LQFP144 (GD32F205Zx), LQFP100 (GD32F205Vx), LQFP64 (GD32F205Rx)
- Operation temperature range: -40°C to +85°C (industrial level)



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# 4. Electrical characteristics

## 4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4-1. Absolute maximum ratings**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ | External voltage range | $V_{SS}$ - 0.3 | $V_{SS}$ + 3.6 | V |
| $V_{DDA}$ | External analog supply voltage | $V_{SSA}$ - 0.3 | $V_{SSA}$ + 3.6 | V |
| $V_{BAT}$ | External battery supply voltage | $V_{SS}$ - 0.3 | $V_{SS}$ + 3.6 | V |
| $V_{IN}$ | Input voltage on 5V tolerant pin | $V_{SS}$ - 0.3 | $V_{DD}$ + 4.0 | V |
| | Input voltage on other I/O | $V_{SS}$ - 0.3 | 4.0 | V |
| $I_{IO}$ | Maximum current for GPIO pins | — | 25 | mA |
| $I_{INJ}$ | Injected current on 5V tolerant pin | — | ±5 | mA |
| | Injected current on other I/O | — | ±5 | mA |
| $\sum I_{INJ}$ | Injected current on all I/O | — | ±25 | mA |
| $T_A$ | Operating temperature range | -40 | +85 | °C |
| $T_{STG}$ | Storage temperature range | -55 | +150 | °C |
| $T_J$ | Maximum junction temperature | — | 125 | °C |

## 4.2. Recommended DC characteristics

**Table 4-2. DC operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | — | 2.6 | 3.3 | 3.6 | V |
| $V_{DDA}$ | Analog supply voltage | Same as $V_{DD}$ | 2.6 | 3.3 | 3.6 | V |
| $V_{BAT}$ | Battery supply voltage | — | 1.8 | — | 3.6 | V |

## 4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

**Table 4-3. Power consumption characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current | $V_{DD}$=$V_{DDA}$=3.3V, HXTAL=25MHz, System clock=120 MHz, All peripherals enabled | — | 95.52 | — | mA |



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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | (Run mode) | $V_{DD}$=$V_{DDA}$=3.3V, HXTAL=25MHz, System clock =120 MHz, All peripherals disabled | — | 55.23 | — | mA |
| | | $V_{DD}$=$V_{DDA}$=3.3V, HXTAL=25MHz, System clock=108 MHz, All peripherals enabled | — | 86.22 | — | mA |
| | | $V_{DD}$=$V_{DDA}$=3.3V, HXTAL=25MHz, System clock =108 MHz, All peripherals disabled | — | 50.05 | — | mA |
| | | $V_{DD}$=$V_{DDA}$=3.3V, HXTAL=25MHz, System clock =72MHz, All peripherals enabled | -— | 58.42 | — | mA |
| | | $V_{DD}$=$V_{DDA}$=3.3V, HXTAL=25MHz, System Clock =72 MHz, All peripherals disabled | — | 34.32 | — | mA |
| | Supply current (Sleep mode) | $V_{DD}$=$V_{DDA}$=3.3V, HXTAL=8MHz, CPU clock off, System clock=120 MHz, All peripherals enabled | — | 59.46 | — | mA |
| | | $V_{DD}$=$V_{DDA}$=3.3V, HXTAL=8MHz, CPU clock off, System clock=120 MHz, All peripherals disabled | — | 12.22 | — | mA |
| | Supply current (Deep-Sleep mode) | $V_{DD}$=$V_{DDA}$=3.3V, Regulator in Run mode, IRC40K on, RTC on, All GPIOs analog mode | — | 1.23 | — | mA |
| | | $V_{DD}$=$V_{DDA}$=3.3V, Regulator in Low Power mode, IRC40K on, RTC on, All GPIOs analog mode | — | 1.18 | — | mA |
| | Supply current (Standby mode) | $V_{DD}$=$V_{DDA}$=3.3V, LXTAL off, IRC40K on, RTC on | — | 7.47 | — | μA |
| | | $V_{DD}$=$V_{DDA}$=3.3V, LXTAL off, IRC40K on, RTC off | — | 7.35 | — | μA |
| | | $V_{DD}$=$V_{DDA}$=3.3V, LXTAL off, IRC40K off, RTC off | — | 6.13 | — | μA |
| $I_{BAT}$ | Battery supply current | $V_{BAT}$=3.6V, LXTAL on, RTC on, LXTAL High driving | — | 2.69 | — | μA |
| | | $V_{BAT}$=3.3V, LXTAL on, RTC on, LXTAL High driving | — | 2.41 | — | μA |
| | | $V_{BAT}$=2.6V, LXTAL on, RTC on, LXTAL High driving | — | 1.81 | — | μA |
| | | $V_{BAT}$=3.6V, LXTAL on, RTC on, LXTAL Mid High driving | — | 1.10 | — | μA |
| | | $V_{BAT}$=3.3V, LXTAL on, RTC on, LXTAL Mid High driving | — | 1.04 | — | μA |
| | | $V_{BAT}$=2.6V, LXTAL on, RTC on, LXTAL Mid High driving | — | 0.92 | — | μA |
| | | $V_{BAT}$=3.6V, LXTAL on, RTC on, LXTAL Mid Low driving | — | 0.83 | — | μA |
| | | $V_{BAT}$=3.3V, LXTAL on, RTC on, LXTAL Mid Low driving | — | 0.76 | — | μA |
| | | $V_{BAT}$=2.6V, LXTAL on, RTC on, LXTAL Mid Low driving | — | 0.63 | — | μA |

## 4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in the ***Table 4-4. EMS characteristics***, based on the EMS levels and classes compliant with IEC 61000 series standard.

**Table 4-4. EMS characteristics**

| Symbol | Parameter | Conditions | Level/Class |
|---|---|---|---|
| $V_{ESD}$ | Voltage applied to all device pins to | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C | 3B |



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| Symbol | Parameter | Conditions | Level/Class |
|---|---|---|---|
| | induce a functional disturbance | conforms to IEC 61000-4-2 | |
| $V_{FTB}$ | Fast transient voltage burst applied to induce a functional disturbance through 100 pF on $V_{DD}$ and $V_{SS}$ pins | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C conforms to IEC 61000-4-4 | 4A |

EMI (Electromagnetic Interference) emission testing result is given in the ***Table 4-5. EMI characteristics***, compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 4-5. EMI characteristics**

| Symbol | Parameter | Conditions | Tested frequency band | Conditions | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | 56M | 72M | 120M | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, compliant with IEC 61967-2 | 0.1 to 2 MHz | <0 | <0 | <0 | dBμV |
| | | | 2 to 30 MHz | -3.7 | -2.8 | -1.8 | |
| | | | 30 to 130 MHz | -6.5 | -8 | -5.3 | |
| | | | 130 MHz to 1GHz | -7 | -7 | -5 | |

## 4.5. Power supply supervisor characteristics

**Table 4-6. Power supply supervisor characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{POR}$ | Power on reset threshold | | 2.32 | 2.40 | 2.48 | V |
| $V_{PDR}$ | power down reset threshold | | 1.72 | 1.80 | 1.88 | V |
| $V_{HYST}$ | PDR hysteresis | | — | 0.6 | — | V |
| $T_{RSTTEMP}$ | Reset temporization | | — | 2 | — | ms |



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## 4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

**Table 4-7. ESD characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$=25 °C; JESD22-A114 | — | — | 5000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$=25 °C; JESD22-C101 | — | — | 500 | V |

**Table 4-8. Static latch-up characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| LU | I-test | $T_A$=25 °C; JESD78 | — | — | ±100 | mA |
| | $V_{supply}$ over voltage | | — | — | 5.4 | V |



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## 4.7. External clock characteristics

**Table 4-9. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HXTAL}$ | High Speed External oscillator (HXTAL) frequency | $V_{DD}$=3.3V | 3 | 8 | 32 | MHz |
| $C_{HXTAL}$ | Recommended load capacitance on OSCIN and OSCOUT | — | — | 20 | 30 | pF |
| $R_{FHXTAL}$ | Recommended external feedback resistor between XTALIN and XTALOUT | — | — | 1 | — | MΩ |
| $D_{HXTAL}$ | HXTAL oscillator duty cycle | — | 48 | 50 | 52 | % |
| $I_{DDHXTAL}$ | HXTAL oscillator operating current | $V_{DD}$=3.3V, $T_A$=25°C | — | — | 1.2 | μA |
| $t_{SUHXTAL}$ | HXTAL oscillator startup time | $V_{DD}$=3.3V, $T_A$=25°C | — | 2 | — | ms |

**Table 4-10. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LXTAL}$ | Low Speed External oscillator (LXTAL) frequency | $V_{DD}$=$V_{BAT}$=3.3V | — | 32.768 | 1000 | KHz |
| $C_{LXTAL}$ | Recommended load capacitance on OSC32IN and OSC32OUT | — | 8 | 10 | 15 | pF |
| $R_{FLXTAL}$ | Recommended external feedback resistor between XTAL32IN and XTAL32OUT | — | — | 5 | — | MΩ |
| $D_{LXTAL}$ | LXTAL oscillator duty cycle | — | 48 | 50 | 52 | % |
| $I_{DDLXTAL}$ | LXTAL oscillator operating current | $V_{DD}$=$V_{BAT}$=3.3V | — | 10 | — | μA |
| $t_{SULXTAL}$ | LXTAL oscillator startup time | $V_{DD}$=$V_{BAT}$=3.3V | — | 3 | — | s |



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## 4.8. Internal clock characteristics

**Table 4-11. High speed internal clock (IRC8M) characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IRC8M}$ | High Speed Internal Oscillator (IRC8M) frequency | $V_{DD}$=3.3V | — | 8 | — | MHz |
| $ACC_{IRC8M}$ | IRC8M oscillator Frequency accuracy, Factory-trimmed | $V_{DD}$=3.3V, $T_A$=-40°C ~+105°C | -2.5 | — | +1.5 | % |
| | | $V_{DD}$=3.3V, $T_A$=0°C ~ +85°C | -1.2 | — | +1.2 | % |
| | | $V_{DD}$=3.3V, $T_A$=25°C | -1 | — | +1 | % |
| $D_{IRC8M}$ | IRC8M oscillator duty cycle | $V_{DD}$=3.3V, $f_{IRC8M}$=8MHz | 48 | 50 | 52 | % |
| $I_{DDIRC8M}$ | IRC8M oscillator operating current | $V_{DD}$=3.3V, $f_{IRC8M}$=8MHz | — | 80 | 100 | μA |
| $t_{SUIRC8M}$ | IRC8M oscillator startup time | $V_{DD}$=3.3V, $f_{IRC8M}$=8MHz | 1 | — | 2 | us |

**Table 4-12. Low speed internal clock (IRC40K) characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IRC40K}$ | Low Speed Internal oscillator (IRC40K) frequency | $V_{DD}$=$V_{BAT}$=3.3V, $T_A$=-40°C ~ +85°C | 30 | 40 | 60 | KHz |
| $I_{DDIRC40K}$ | IRC40K oscillator operating current | $V_{DD}$=$V_{BAT}$=3.3V, $T_A$=25°C | — | 1 | 2 | μA |
| $t_{SUIRC40K}$ | IRC40K oscillator startup time | $V_{DD}$=$V_{BAT}$=3.3V, $T_A$=25°C | — | — | 80 | μs |

## 4.9. PLL characteristics

**Table 4-13. PLL characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLLIN}$ | PLL input clock frequency | | 1 | 8 | 25 | MHz |
| $f_{PLL}$ | PLL output clock frequency | | 16 | — | 120 | MHz |
| $t_{LOCK}$ | PLL lock time | | — | | 100 | μs |



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## 4.10. Memory characteristics

**Table 4-14. Flash memory characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $PE_{CYC}$ | Number of guaranteed program /erase cycles before failure (Endurance) | $T_A$=-40°C ~ +85°C | 100 | — | — | kcycles |
| $t_{RET}$ | Data retention time | $T_A$=125°C | 20 | — | — | years |
| $t_{PROG}$ | Word programming time | $T_A$=-40°C ~ +85°C | 200 | — | 400 | us |
| $t_{ERASE}$ | Page erase time | $T_A$=-40°C ~ +85°C | 60 | 100 | 450 | ms |
| $t_{MERASE}$ | Mass erase time | $T_A$=-40°C ~ +85°C | 3.2 | — | 9.6 | s |

## 4.11. GPIO characteristics

**Table 4-15. I/O port characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Standard IO Low level input voltage | $V_{DD}$=2.6V | -0.3 | — | 0.95 | V |
| | 5V-tolerant IO Low level input voltage | $V_{DD}$=2.6V | -0.3 | — | 0.9 | V |
| $V_{IH}$ | Standard IO High level input voltage | $V_{DD}$=2.6V | 1.2 | — | 4.0 | V |
| | 5V-tolerant IO High level input voltage | $V_{DD}$=2.6V | 1.5 | — | 5.5 | V |
| $V_{OL}$ | Low level output voltage | $V_{DD}$=2.6V | — | — | 0.2 | V |
| $V_{OH}$ | High level output voltage | $V_{DD}$=2.6V | 2.3 | — | — | V |
| $R_{PU}$ | Internal pull-up resistor | $V_{IN}$=$V_{SS}$ | 30 | 40 | 50 | kΩ |
| $R_{PD}$ | Internal pull-down resistor | $V_{IN}$=$V_{DD}$ | 30 | 40 | 50 | kΩ |



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## 4.12. ADC characteristics

**Table 4-16. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Operating voltage | | 2.6 | 3.3 | 3.6 | V |
| $V_{IN}$ | ADC input voltage range | | 0 | — | $V_{REF+}$ | V |
| $f_{ADC}$ | ADC clock | | 0.6 | — | 28 | MHz |
| $f_S$ | Sampling rate | 12-bit | — | — | 2 | MHz |
| $R_{ADC}$ | Input sampling switch resistance | | — | — | 0.45 | kΩ |
| $C_{ADC}$ | Input sampling capacitance | No pin/pad capacitance included | — | 6.4 | — | pF |
| $t_{SU}$ | Startup time | | — | — | 1 | μs |

## 4.13. DAC characteristics

**Table 4-17. DAC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Operating voltage | | 2.6 | 3.3 | 3.6 | V |
| $V_{DACIN}$ | DAC input voltage range | | 0 | — | $V_{REF+}$ | V |
| $R_{LOAD}$ | Load resistance | Resistive load vs. $V_{SSA}$ with buffer ON | 5 | — | — | kΩ |
| $C_{LOAD}$ | Load capacitance | No pin/pad capacitance included | — | — | 50 | pF |
| DNE | Differential non-linearity error | DAC in 12-bit | — | — | ±3 | LSB |
| INL | Integral non-linearity | DAC in 12-bit | — | — | ±4 | LSB |
| Offset | Offset error | DAC in 12-bit, $V_{REF+}$ = 3.6 V | — | — | ±12 | LSB |
| GE | Gain error | DAC in 12-bit | — | — | ±0.5 | % |

## 4.14. I2C characteristics

**Table 4-18. I2C characteristics**

| Symbol | Parameter | Conditions | Standard mode | | Fast mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $f_{SCL}$ | SCL clock frequency | | 0 | 100 | 0 | 400 | KHz |
| $t_{SCL(H)}$ | SCL clock high time | | 4.0 | — | 0.6 | — | ns |
| $t_{SCL(L)}$ | SCL clock low time | | 4.7 | — | 1.3 | — | ns |



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## 4.15. SPI characteristics

**Table 4-19. Standard SPI characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$ | SCK clock frequency | | — | — | 30 | MHz |
| $t_{SCK(H)}$ | SCK clock high time | | 19 | — | — | ns |
| $t_{SCK(L)}$ | SCK clock low time | | 19 | — | — | ns |
| **SPI master mode** | | | | | | |
| $t_{V(MO)}$ | Data output valid time | | — | — | 25 | ns |
| $t_{H(MO)}$ | Data output hold time | | 2 | — | — | ns |
| $t_{SU(MI)}$ | Data input setup time | | 5 | — | — | ns |
| $t_{H(MI)}$ | Data input hold time | | 5 | — | — | ns |
| **SPI slave mode** | | | | | | |
| $t_{SU(NSS)}$ | NSS enable setup time | $f_{PCLK}$=54MHz | 74 | — | — | ns |
| $t_{H(NSS)}$ | NSS enable hold time | $f_{PCLK}$=54MHz | 37 | — | — | ns |
| $t_{A(SO)}$ | Data output access time | $f_{PCLK}$=54MHz | 0 | — | 55 | ns |
| $t_{DIS(SO)}$ | Data output disable time | | 3 | — | 10 | ns |
| $t_{V(SO)}$ | Data output valid time | | — | — | 25 | ns |
| $t_{H(SO)}$ | Data output hold time | | 15 | — | — | ns |
| $t_{SU(SI)}$ | Data input setup time | | 5 | — | — | ns |
| $t_{H(SI)}$ | Data input hold time | | 4 | — | — | ns |

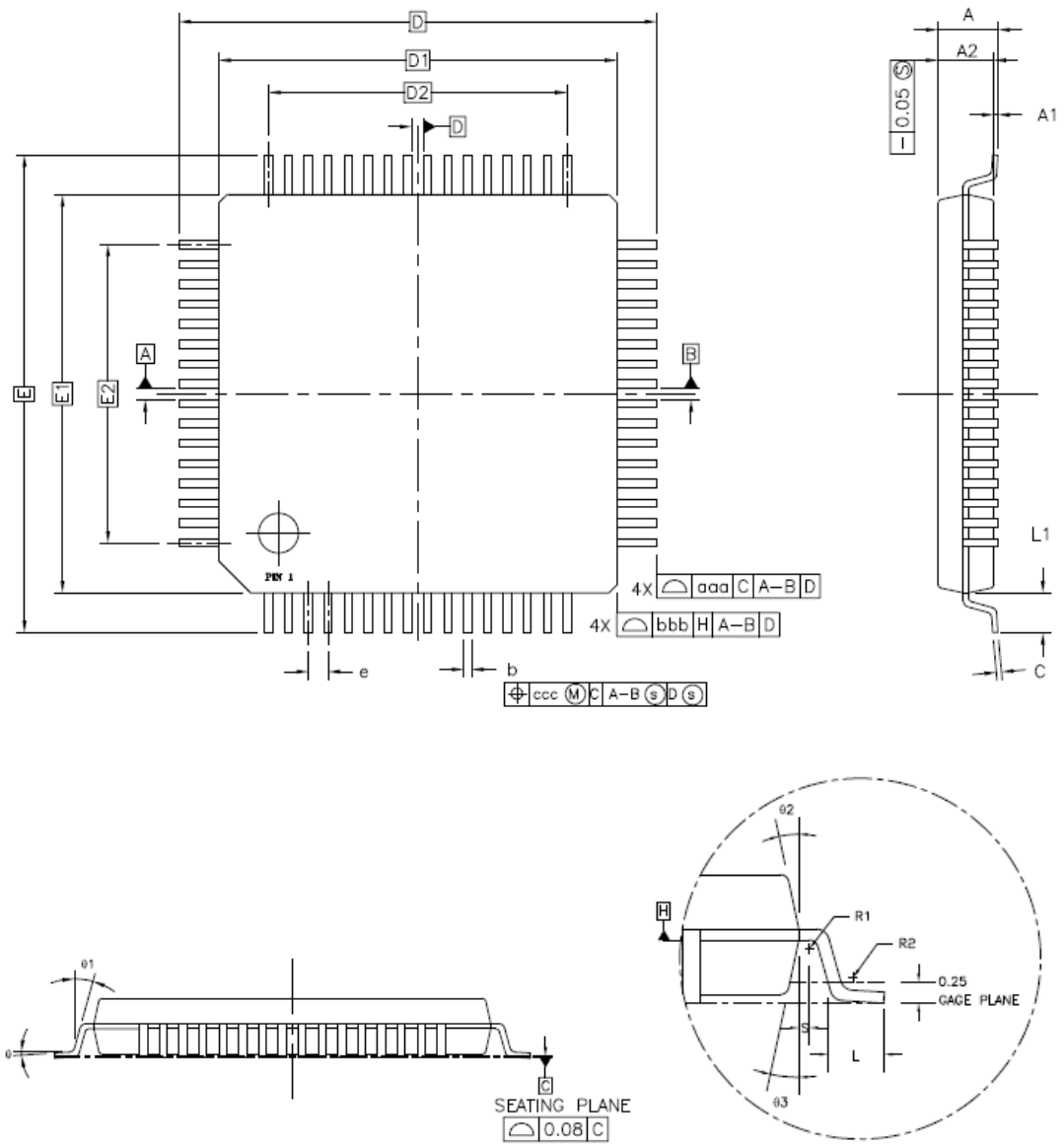


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# 5. Package information

## 5.1. LQFP package outline dimensions

**Figure 5-1. LQFP package outline**






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**Table 5-1. LQFP package dimensions**

| Symbol | LQFP64 | | | LQFP100 | | | LQFP144 | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.60 | - | - | 1.60 | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 | 0.05 | - | 0.15 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 | 1.35 | 1.40 | 1.45 | 1.35 | 1.40 | 1.45 |
| D | - | 12.00 | - | - | 16.00 | - | - | 22.00 | - |
| D1 | - | 10.00 | - | - | 14.00 | - | - | 20.00 | - |
| E | - | 12.00 | - | - | 16.00 | - | - | 22.00 | - |
| E1 | - | 10.00 | - | - | 14.00 | - | - | 20.00 | - |
| R1 | 0.08 | - | - | 0.08 | - | - | 0.08 | - | - |
| R2 | 0.08 | - | 0.20 | 0.08 | - | 0.20 | 0.08 | - | 0.20 |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | - | - | 0° | - | - | 0° | - | - |
| θ2 | 11° | 12° | 13° | 11° | 12° | 13° | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | - | 0.20 | 0.09 | - | 0.20 | 0.09 | - | 0.20 |
| L | 0.45 | 0.60 | 0.75 | 0.45 | 0.60 | 0.75 | 0.45 | 0.60 | 0.75 |
| L1 | - | 1.00 | - | - | 1.00 | - | - | 1.00 | - |
| S | 0.20 | - | - | 0.20 | - | - | 0.20 | - | - |
| b | 0.17 | 0.20 | 0.27 | 0.17 | 0.20 | 0.27 | 0.17 | 0.20 | 0.27 |
| e | - | 0.50 | - | - | 0.50 | - | - | 0.50 | - |
| D2 | - | 7.50 | - | - | 12.00 | - | - | 17.50 | - |
| E2 | - | 7.50 | - | - | 12.00 | - | - | 17.50 | - |
| aaa | 0.20 | | | 0.20 | | | 0.20 | | |
| bbb | 0.20 | | | 0.20 | | | 0.20 | | |
| ccc | 0.08 | | | 0.08 | | | 0.08 | | |

(Original dimensions are in millmeters)



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# 6. Ordering information

**Table 6-1. Part ordering code for GD32F205xx devices**

| Ordering code | Flash (KB) | Package | Package type | Temperature operating range |
|---|---|---|---|---|
| GD32F205RCT6 | 256 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F205RET6 | 512 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F205RGT6 | 1024 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F205RKT6 | 3072 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F205VCT6 | 256 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F205VET6 | 512 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F205VGT6 | 1024 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F205VKT6 | 3072 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F205ZCT6 | 256 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F205ZET6 | 512 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F205ZGT6 | 1024 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F205ZKT6 | 3072 | LQFP144 | Green | Industrial -40°C to +85°C |



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# 7. Revision history

**Table 7-1. Revision history**

| Revision No. | Description | Date |
|---|---|---|
| 1.0 | Initial Release | Jul. 10, 2015 |
| 2.0 | Adapt To New Name Convention | Jan. 24, 2018 |
| 2.1 | Change pin definitions | Dec. 7, 2018 |
| 2.2 | Modify the clock tree | Nov. 30, 2019 |
| 2.3 | 1.Modify the HXTAL frequency range of the clock tree to 4-32MHz。<br>2. The ADC2 mapping function corresponding to PF3, PF4 and PF5 pins is modified to multiplexing function. | Mar.13, 2020 |



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