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FM33256B

256-Kbit (32 K × 8) Integrated Processor Companion with F-RAM

Features

- 256-Kbit ferroelectric random access memory (F-RAM)
  - Logically organized as 32 K × 8
  - High-endurance 100 trillion (10^{14}) read/writes
  - 151-year data retention (See the Data Retention and Endurance table)
  - NoDelay™ writes
  - Advanced high-reliability ferroelectric process
- High Integration Device Replaces Multiple Parts
  - Serial nonvolatile memory
  - Real time clock (RTC) with alarm
  - Low V_{DD} detection drives reset
  - Watchdog window timer
  - Early power-fail warning / NMI
  - 16-bit nonvolatile event counter
  - Serial number with write-lock for security
- Real-time Clock/Calendar
  - Backup current at 2 V: 1.15 µA at +25 °C
  - Seconds through centuries in BCD format
  - Tracks leap years through 2099
  - Uses standard 32.768 kHz crystal (6 pF/12.5 pF)
  - Software calibration
  - Supports battery or capacitor backup
- Processor Companion
  - Active-low reset output for V_{DD} and watchdog
  - Programmable low-V_{DD} reset thresholds
  - Manual reset filtered and debounced
  - Programmable watchdog window timer
  - Nonvolatile event counter tracks system intrusions or other events
  - Comparator for power-fail interrupt or other use
  - 64-bit programmable serial number with lock
- Fast serial peripheral interface (SPI)
  - Up to 16-MHz frequency
  - RTC, Supervisor controlled via SPI interface
  - Supports SPI mode 0 (0, 0) and mode 3 (1, 1)
- Low power consumption
  - 1.1 mA active current at 1 MHz
  - 150 µA standby current
- Operating voltage: V_{DD} = 2.7 V to 3.6 V
- Industrial temperature: –40 °C to +85 °C
- 14-pin small outline integrated circuit (SOIC) package
- Restriction of hazardous substances (RoHS) compliant
- Underwriters laboratory (UL) recognized

Functional Overview

The FM33256B device integrates F-RAM memory with the most commonly needed functions for processor-based systems. Major features include nonvolatile memory, real time clock, low-V_{DD} reset, watchdog timer, nonvolatile event counter, lockable 64-bit serial number area, and general purpose comparator that can be used for a power-fail (NMI) interrupt or any other purpose.

The FM33256B is a 256-Kbit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or F-RAM is nonvolatile and performs reads and writes similar to a RAM. It provides reliable data retention for 151 years while eliminating the complexities, overhead, and system-level reliability problems caused by other nonvolatile memories. The FM33256B is capable of supporting 10^{14} read/write cycles, or 100 million times more write cycles than EEPROM.

The real time clock (RTC) provides time and date information in BCD format. It can be permanently powered from an external backup voltage source, either a battery or a capacitor. The timekeeper uses a common external 32.768 kHz crystal and provides a calibration mode that allows software adjustment of timekeeping accuracy.

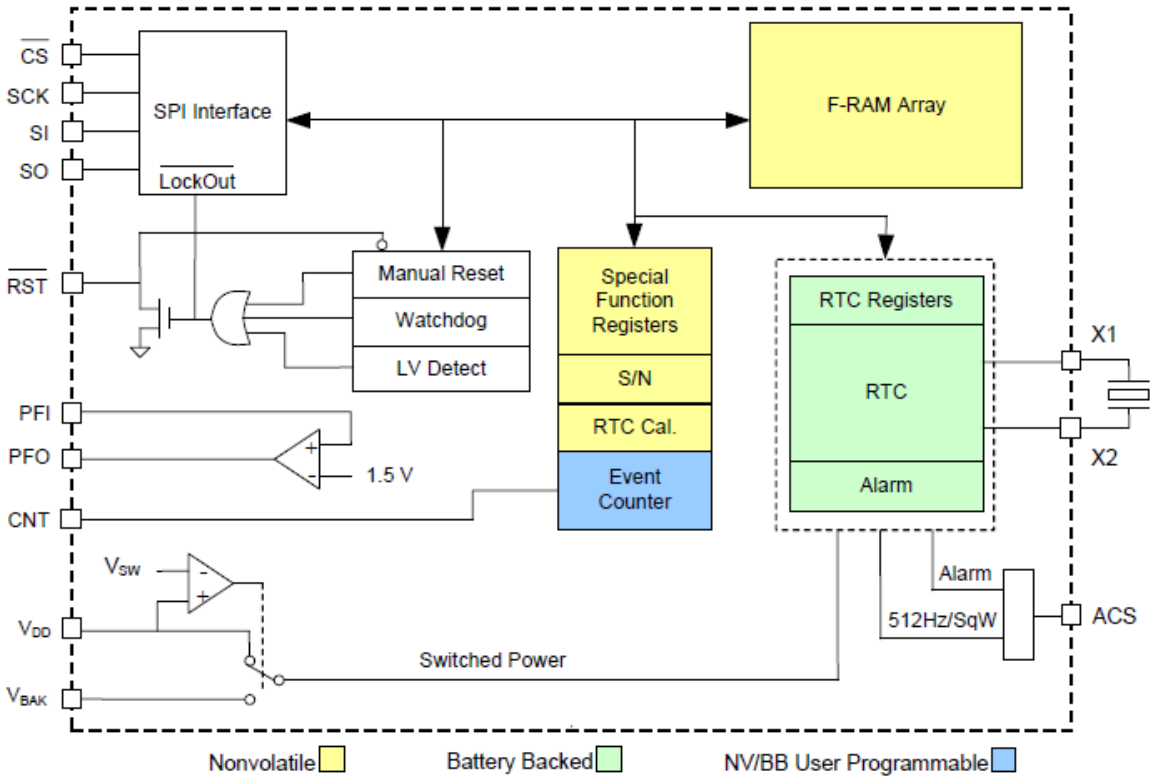
The processor companion includes commonly needed CPU support functions. Supervisory functions include a reset output signal controlled by either a low V_{DD} condition or a watchdog timeout. $\overline{RST}$ goes active when V_{DD} drops below a programmable threshold and remains active for 100 ms (max.) after V_{DD} rises above the trip point. A programmable watchdog timer runs from 60 ms to 1.8 seconds. The timer may also be programmed for a delayed start, which functions as a window timer. The watchdog timer is optional, but if enabled it will assert the reset signal for 100 ms if not restarted by the host within the time window. A flag-bit indicates the source of the reset.

A comparator on PFI compares an external input pin to the onboard 1.5 V reference. This is useful for generating a power-fail interrupt (NMI) but can be used for any purpose. The family also includes a programmable 64-bit serial number that can be locked making it unalterable. Additionally it offers an event counter that tracks the number of rising or falling edges detected on a dedicated input pin. The counter can be programmed to be nonvolatile under V_{DD} power or battery-backed using only V_{BAK}. If V_{BAK} is connected to a battery or capacitor, then events will be counted even in the absence of V_{DD}.

For a complete list of related documentation, click here.

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Web:www.manduic.com Email:sales@manduic.com

Logic Block Diagram



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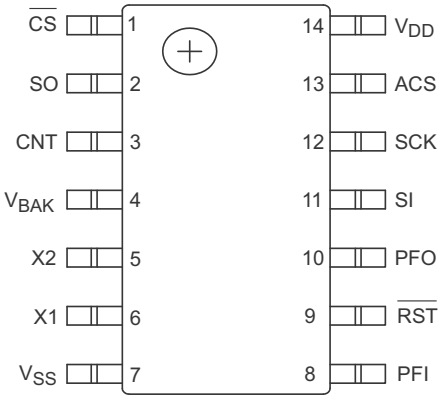
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Pinout

Figure 1. 14-pin SOIC pinout



Pin Definitions

Pin Name	I/O Type	Description
$\overline{CS}$	Input	**Chip Select**. This active LOW input activates the device. When HIGH, the device enters low-power standby mode, ignores SCK and SI inputs, and the SO output is tristated. When LOW, the device internally activates the SCK signal. A falling edge on $\overline{CS}$ must occur before every opcode.
SCK	Input	**Serial Clock**. SI and SO activity is synchronized to the serial clock. Inputs are latched on the rising edge and outputs occur on the falling edge. Because the device is synchronous, the clock frequency may be any value between 0 and 16 MHz and may be interrupted at any time.
SI [1]	Input	**Serial Input**. Data is input to the device on this pin. The pin is sampled on the rising edge of SCK and is ignored at other times. It should always be driven to a valid logic level to meet I_{DD} specifications.
SO [1]	Output	**Serial Output**. This is the data output pin. It is driven during a read and remains tristated at all other times. Data transitions are driven on the falling edge of the serial clock.
CNT	Input	**Event Counter Input**. This input increments the counter when an edge is detected on this pin. The polarity is programmable and the counter value is nonvolatile or battery-backed, depending on the mode. This pin should be tied to ground if unused.
ACS	Output	**Alarm/Calibration/SquareWave**. This is an open-drain output that requires an external pull-up resistor. In normal operation, this pin acts as the active-low alarm output. In Calibration mode, a 512 Hz square-wave is driven out. In SquareWave mode, the user may select a frequency of 1, 512, 4096, or 32768 Hz to be used as a continuous output. The SquareWave mode is entered by clearing the AL/SW and CAL bits in the register 18h.
X1, X2	Input/Output	32.768 kHz crystal connection. These pins should be left unconnected if RTC is not used.
$\overline{RST}$	Input/Output	**Reset**. This active-low output is open drain with weak pull-up. It is also an input when used as a manual reset. This pin should be left floating if unused.
PFI	Input	**Early Power-fail Input**. Typically connected to an unregulated power supply to detect an early power failure. This pin must be tied to ground if unused.
PFO	Output	**Early Power-fail Output**. This pin is the early power-fail output and is typically used to drive a micro-controller NMI pin. PFO drives LOW when the PFI voltage is < 1.5 V.
V_{BAK}	Power supply	**Backup supply voltage**. Connected to a 3 V battery or a large value capacitor. If no backup supply is used, this pin should be tied to V_{SS} and the VBC bit should be cleared in the RTC register 18h. The trickle charger is UL recognized and ensures no excessive current when using a lithium battery.
V_{SS}	Power supply	Ground for the device. Must be connected to the ground of the system.
V_{DD}	Power supply	Power supply input to the device.

Note
1. SI may be connected to SO for a single pin data interface.

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Tel:150-1290-5940
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Overview

The FM33256B device combines a serial nonvolatile RAM with a real time clock (RTC) and a processor companion. The companion is a highly integrated peripheral including a processor supervisor, analog comparator, a nonvolatile counter, and a serial number. The FM33256B integrates these complementary but distinct functions under a common interface in a single package. The product is organized as two logical devices. The first is a memory and the second is the companion which includes all the remaining functions. From the system perspective they appear to be two separate devices with unique opcodes on the serial bus.

The memory is organized as a standalone nonvolatile SPI memory using standard opcodes. The real time clock and supervisor functions are accessed under their own opcodes. The clock and supervisor functions are controlled by 30 special function registers. The RTC alarm and some control registers are maintained by the power source on the V_{BAK} pin, allowing them to operate from battery or backup capacitor power when V_{DD} drops below a set threshold. Each functional block is described below.

Memory Architecture

The FM33256B is available with 256-Kbit of memory. The device uses two-byte addressing for the memory portion of the chip. This makes the device software compatible with its standalone memory counterparts, such as the FM25W256.

The memory array is logically organized as 32,768 × 8 bits and is accessed using an industry-standard serial peripheral interface (SPI) bus. The memory is based on F-RAM technology. Therefore it can be treated as RAM and is read or written at the speed of the SPI bus with no delays for write operations. It also offers effectively unlimited write endurance unlike other nonvolatile memory technologies. The SPI protocol is described on page 23.

The memory array can be write-protected by software. Two bits (BP1, BP0) in the Status Register control the protection setting. Based on the setting, the protected addresses cannot be written. The Status Register & Write Protection is described in more detail on page 26.

Processor Companion

In addition to nonvolatile RAM, the FM33256B incorporates a real time clock with alarm and highly integrated processor companion. The companion includes a low-V_{DD} reset, a programmable watchdog timer, a 16-bit nonvolatile event counter, a comparator for early power-fail detection or other purposes, and a 64-bit serial number.

Processor Supervisor

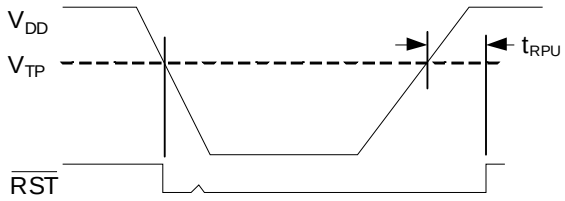
Supervisors provide a host processor two basic functions: Detection of power supply fault conditions and a watchdog timer to escape a software lockup condition. The FM33256B has a reset pin ($\overline{RST}$) to drive a processor reset input during power faults, power-up, and software lockups. It is an open drain output with a weak internal pull-up to V_{DD}. This allows other reset sources to be wire-OR'd to the $\overline{RST}$ pin. When V_{DD} is above the programmed trip point, $\overline{RST}$ output is pulled weakly to V_{DD}. If V_{DD} drops below the reset trip point voltage level (V_{TP}), the $\overline{RST}$ pin will be driven LOW. It will remain LOW until V_{DD} falls too low for circuit operation which is the V_{RST} level. When V_{DD} rises again above V_{TP}, $\overline{RST}$ continues to drive LOW for at least 30 ms (t_{RPU}) to ensure a robust system reset at a reliable V_{DD} level. After t_{RPU} has been met, the $\overline{RST}$ pin will return to the weak HIGH state. While $\overline{RST}$ is asserted, serial bus activity is locked out even if a transaction occurred as V_{DD} dropped below V_{TP}. A memory operation started while V_{DD} is above V_{TP} will be completed internally.

Table 1 below shows how bits VTP(1:0) control the trip point of the low-V_{DD} reset. They are located in register 18h, bits 1 and 0. The reset pin will drive LOW when V_{DD} is below the selected V_{TP} voltage, and the SPI interface and F-RAM array will be locked out. Figure 2 illustrates the reset operation in response to a low V_{DD}.

Table 1. VTP setting

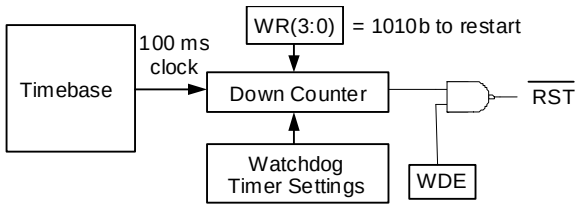
VTP Setting	VTP1	VTP0
2.6 V	0	0
2.75 V	0	1
2.9 V	1	0
3.0 V	1	1

Figure 2. Low V_{DD} Reset



A watchdog timer can also be used to drive an active reset signal. The watchdog is a free-running programmable timer. The timeout period can be software programmed from 60 ms to 1.8 seconds in 60 ms increments via a 5-bit nonvolatile setting (register 0Ch).

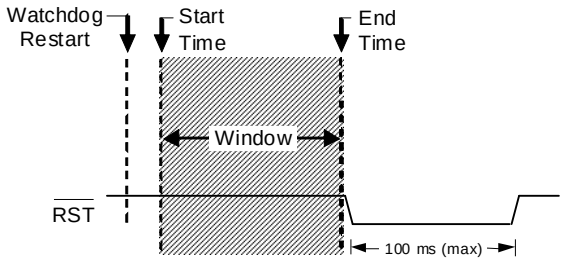
Figure 3. Watchdog Timer



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The watchdog also incorporates a window timer feature that allows a delayed start. The starting time and ending time defines the window and each may be set independently. The starting time has 25 ms resolution and 0 ms to 775 ms range.

Figure 4. Window Timer



The watchdog EndTime value is located in register 0Ch, bits 4:0, the watchdog enable is bit 7. The watchdog is restarted by writing the pattern 1010b to the lower nibble of register 0Ah. Writing the correct pattern will also cause the timer to load new timeout values. Writing other patterns to this address will not affect its operation. Note the watchdog timer is free-running. Prior to enabling it, users should restart the timer as described above. This assures that the full timeout is provided immediately after enabling. The watchdog is disabled when V_{DD} drops below V_{TP}. **Note** setting the EndTime timeout setting to all zeroes (00000b) disables the timer to save power. The listing below summarizes the watchdog bits.

Watchdog Start Time	WDST(4:0)	0Bh, bits 4:0
Watchdog EndTime	WDET(4:0)	0Ch, bits 4:0
Watchdog Enable	WDE	0Ch, bit 7
Watchdog Restart	WR(3:0)	0Ah, bits 3:0
Watchdog Flags	EWDF	09h, bit 7
	LWDF	09h, bit 6

The programmed StartTime value is a guaranteed maximum time while the EndTime value is a guaranteed minimum time, and both vary with temperature and V_{DD} voltage. The watchdog has two additional controls associated with its operation. The nonvolatile enable bit WDE allows the $\overline{RST}$ to go active if the watchdog reaches the timeout without being restarted. If a reset occurs, the timer will restart on the rising edge of the reset pulse. If WDE is not enabled, the watchdog timer still runs but has no effect on $\overline{RST}$. The second control is a nibble that restarts the timer, thus preventing a reset. The timer should be restarted after changing the timeout value.

This procedure must be followed to properly load the watchdog registers:

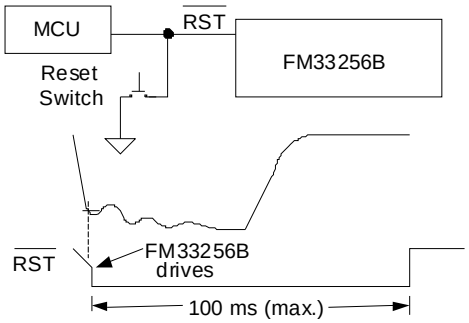
	Address
1. Write the StartTime value	0Bh
2. Write the EndTime value and WDE = '1'	0Ch
3. Issue a Restart command	0Ah

The restart command in step 3 must be issued before t_{DOG2}, which was programmed in step 2. The window timer starts counting when the restart command is issued.

Manual Reset

The $\overline{RST}$ is a bi-directional signal allowing the FM33256B to filter and de-bounce a manual reset switch. The $\overline{RST}$ input detects an external low condition and responds by driving the $\overline{RST}$ signal LOW for 100 ms (max). This effectively filters and de-bounces a reset switch. After this timeout (t_{RPU}), the user may continue pulling down on the $\overline{RST}$ pin, but SPI commands will not be locked out.

Figure 5. Manual Reset



Note The internal weak pull-up eliminates the need for additional external components.

Reset Flags

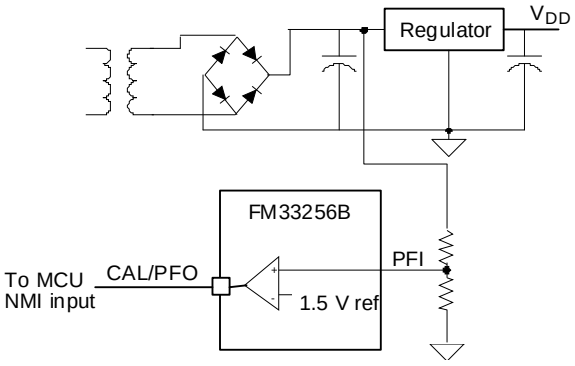
In case of a reset condition, a flag bit will be set to indicate the source of the reset. A low-V_{DD} reset is indicated by the POR flag, register 09h bit 5. There are two watchdog reset flags - one for an early fault (EWDF) and the other for a late fault (LWDF), located in register 09h bits 7 and 6. A manual reset will result in no flag being set, so the absence of a flag is a manual reset. Note that the bits are set in response to reset sources but they must be cleared by the user. It is possible to read the register and have both sources indicated if both have occurred since the user cleared them.

Power Fail Comparator

An analog comparator compares the PFI input pin to an onboard 1.5 V reference. When the PFI input voltage drops below this threshold, the comparator will drive the PFO pin to a LOW state. The comparator has 100 mV of hysteresis (rising voltage only) to reduce noise sensitivity. The most common application of this comparator is to create an early warning power fail interrupt (NMI). This can be accomplished by connecting the PFI pin to an upstream power supply via a resistor divider. An application circuit is shown below. The comparator is a general purpose device and its application is not limited to the NMI function.

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Figure 6. Comparator as a Power-Fail Warning



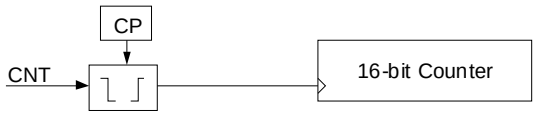
If the power-fail comparator is not used, the PFI pin should be tied to either V_{DD} or V_{SS}. Note that the PFO output will drive to V_{DD} or V_{SS} as well.

Event Counter

The FM33256B offers the user a nonvolatile 16-bit event counter. The input pin CNT has a programmable edge detector. The CNT pin clocks the counter. The counter is located in registers 0E-0Fh. When the programmed edge polarity occurs, the counter will increment its count value. The register value is read by setting the RC bit (register 0Dh, bit 3) to '1'. This takes a snapshot of the counter byte allowing a stable value even if a count occurs during the read. The register value can be written by first setting the WC bit (register 0Dh, bit 2) to '1'. The user then may clear or preset the counter by writing to registers 0E-0Fh. Counts are blocked when the WC bit is set, so the user must clear the bit to allow counts.

The counter polarity control bit is CP (register 0Dh, bit 0). When CP is '0', the counter increments on a falling edge of CNT, and when CP is set to '1', the counter increments on a rising edge of CNT. The polarity bit CP is nonvolatile.

Figure 7. Event Counter

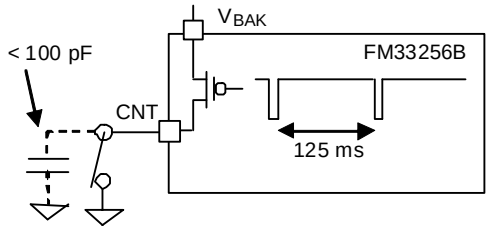


The counter does not wrap back to zero when it reaches the limit of 65,535 (FFFFh). Care must be taken prior to the rollover, and a subsequent counter reset operation must occur to continue counting.

There is also a control bit that allows the user to define the counter as nonvolatile or battery-backed. The counter is nonvolatile when the NVC bit (register 0Dh, bit 7) is logic 1 and battery-backed when the NVC bit is logic 0. Setting the counter mode to battery-backed allows counter operation under V_{BAK} (as well as V_{DD}) power. The lowest operating voltage for battery-backed mode is 2.0 V. When set to "nonvolatile" mode, the counter operates only when V_{DD} is applied and is above the V_{TP} voltage.

The event counter may be programmed to detect a tamper event, such as the system's case or access door being opened. A normally closed switch is tied to the CNT pin and the other contact to the case chassis, usually ground. The typical solution uses a pull-up resistor on the CNT pin and will continuously draw battery current. The FM33256B chip allows the user to invoke a polled mode, which occasionally samples the pin in order to minimize battery drain. It internally tries to pull the CNT pin up and if open circuit will be pulled up to a V_{IH} level, which will trip the edge detector and increment the event counter value. Setting the POLL bit (register 0Dh, bit 1) places the CNT pin into this mode. This mode allows the event counter to detect a rising edge tamper event but the user is restricted to operating in battery-backed mode (NVC = '0') and using rising edge detection (CP = '1'). The CNT pin is polled once every 125 ms. The additional average I_{BAK} current is less than 20 nA. The polling timer circuit operates from the RTC, so the oscillator must be enabled for this to function properly.

Figure 8. Polled Mode on CNT pin Detects Tamper



In the polled mode, the internal pull-up circuit can source a limited amount of current. The maximum capacitance (switch open circuit) allowed on the CNT pin is 100 pF.

Serial Number

A memory location to write a 64-bit serial number is provided. It is a writeable nonvolatile memory block that can be locked by the user once the serial number is set. The 8 bytes of data and the lock bit are all accessed via unique opcodes for the RTC and Processor Companion registers. Therefore the serial number area is separate and distinct from the memory array. The serial number registers can be written an unlimited number of times, so these locations are general purpose memory. However once the lock bit is set, the values cannot be altered and the lock cannot be removed. Once locked the serial number registers can still be read by the system.

The serial number is located in registers 10h to 17h. The lock bit is SNL (register 18h, bit 7). Setting the SNL bit to a '1' disables writes to the serial number registers, and the SNL bit cannot be cleared.

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Alarm

The alarm function compares user-programmed values to the corresponding time/date values and operates under V_{DD} or V_{BAK} power. When a match occurs, an alarm event occurs. The alarm drives an internal flag AF (register 00h, bit 6) and may drive the ACS pin, if desired, by setting the AL/SW bit (register 18h, bit 6) in the Companion Control register. The alarm condition is cleared by writing a '0' to the AF bit.

There are five alarm match fields. They are Month, Date, Hours, Minutes, and Seconds. Each of these fields also has a Match bit that is used to determine if the field is used in the alarm match logic. Setting the Match bit to '0' indicates that the corresponding field will be used in the match process.

Depending on the Match bits, the alarm can occur as specifically as one particular second on one day of the month, or as frequently as once per second continuously. The MSB of each Alarm register is a Match bit. Examples of the Match bit settings are shown in Table 3. Selecting none of the match bits (all '1's) indicates that no match is required. The alarm occurs every second. Setting the match select bit for seconds to '0' causes the logic to match the seconds alarm value to the current time of day. Since a match will occur for only one value per minute, the alarm occurs once per minute. Likewise setting the seconds and minutes match select bits causes an exact match of these values. Thus, an alarm will occur once per hour. Setting seconds, minutes, and hours causes a match once per day. Lastly, selecting all match-values causes an exact time and date match. Selecting other bit combinations will not produce meaningful results, however the alarm circuit will follow the functions described.

There are two ways a user can detect an alarm event, by reading the AF flag or monitoring the ACS pin. The interrupt pin on the host processor may be used to detect an alarm event. The AF flag in register 00h (bit 6) will indicate that a time/date match has occurred. The AF flag will be set to '1' when a match occurs. The AEN bit must be set to enable the AF flag on alarm matches. The flag and ACS pin will remain in this state until the AF bit is cleared by writing it to a '0'. Clearing the AEN bit will prevent further matches from setting AF but will not automatically clear the AF flag.

The RTC alarm is integrated into the special function registers and shares its output pin with the 512 Hz calibration and square wave outputs. When the RTC calibration mode is invoked by setting the CAL bit (register 00h, bit 2), the ACS output pin will be driven with a 512 Hz square wave and the alarm will continue to operate. Since most users only invoke the calibration mode during production this should have no impact on the otherwise normal operation of the alarm.

The ACS output may also be used to drive the system with a frequency other than 512 Hz. The AL/SW bit (register 18h, bit 6) must be '0'. A user-selectable frequency is provided by F0 and F1 (register 18h, bits 4 and 5). The other frequencies are 1, 4096, and 32768 Hz. If a continuous frequency output is enabled with CAL mode, the alarm function will not be available.

Following is a summary table that shows the relationship between register control settings and the state of the ACS pin.

Table 2. State of Register Bit

State of Register Bit			Function of ACS pin
CAL	AEN	AL/SW	
0	1	1	Alarm
0	X	0	Square Wave out
1	X	X	512 Hz out
0	0	1	HI-Z

Table 3. Alarm Match Bit Examples

Seconds	Minutes	Hours	Date	Months	Alarm condition
1	1	1	1	1	No match required = alarm 1/second
0	1	1	1	1	Alarm when seconds match = alarm 1/minute
0	0	1	1	1	Alarm when seconds, minutes match = alarm 1/hour
0	0	0	1	1	Alarm when seconds, minutes, hours match = alarm 1/date
0	0	0	0	1	Alarm when seconds, minutes, hours, date match = alarm 1/month

Real-time Clock Operation

The real-time clock (RTC) is a timekeeping device that can be capacitor- or battery-backed for permanently-powered operation. It offers a software calibration feature that allows high accuracy.

The RTC consists of an oscillator, clock divider, and a register system for user access. It divides down the 32.768 kHz time-base and provides a minimum resolution of seconds (1 Hz).

Static registers provide the user with read/write access to the time values. It includes registers for seconds, minutes, hours, day-of-the-week, date, months, and years. A block diagram shown in Figure 9 illustrates the RTC function.

The user registers are synchronized with the timekeeper core using R and W bits in register 00h. The R bit is used to read the time. Changing the R bit from ‘0’ to ‘1’ transfers timekeeping information from the core into the user registers 02-08h that can be read by the user. If a timekeeper update is pending when R

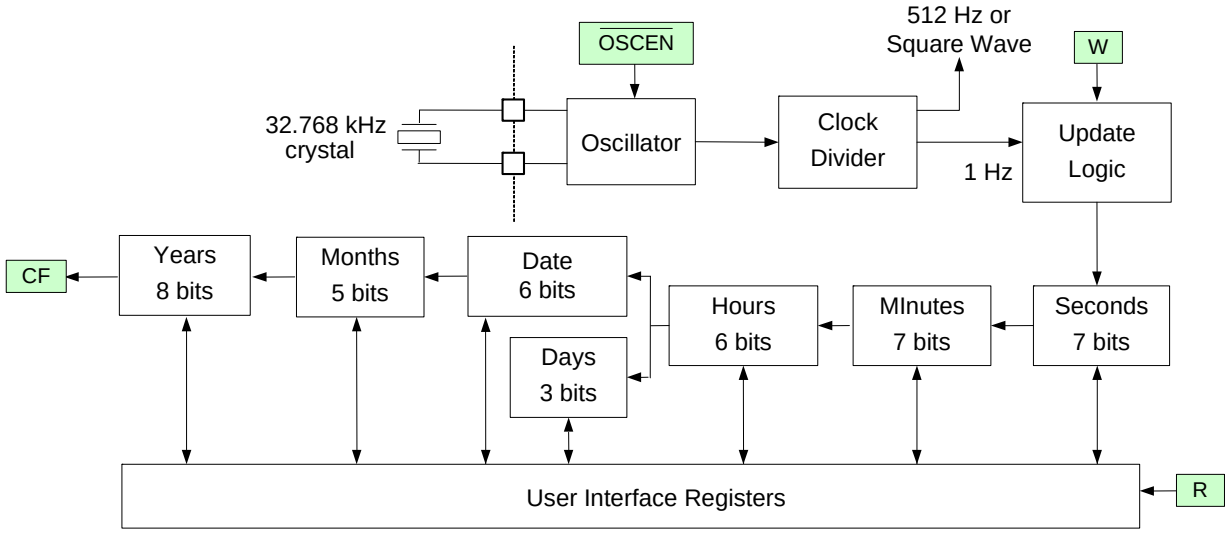
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is set, then the core will be updated prior to loading the user registers. The user registers are frozen and will not be updated again until the R bit is cleared to a '0'.

The W bit is used to write new time/date values. Setting the W bit to a '1' stops the RTC and allows the timekeeping core to be written with new data. Clearing it to '0' causes the RTC to start running based on the new values loaded in the timekeeper core. The RTC may be synchronized to another clock source. On the 8th clock of the write to register 00h (W = '0'), the RTC starts counting with a timebase that has been reset to zero milliseconds.

Note: Users should be certain not to load invalid values, such as FFh, to the timekeeping registers. Updates to the timekeeping core occur continuously except when locked.

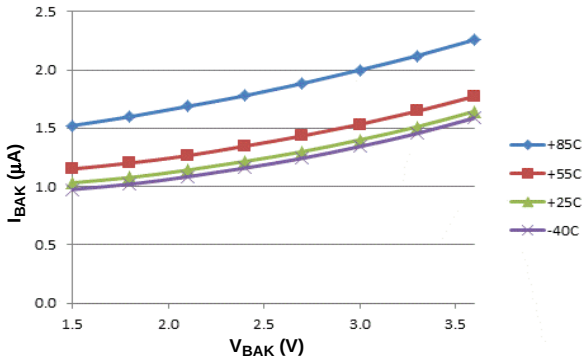
Figure 9. Real-time Clock Core Block Diagram



Backup Power

The real-time clock/calendar is intended to be permanently powered. When the primary system power fails, the voltage on the V_{DD} pin will drop. When V_{DD} is less than 2.5 V, the RTC (and event counters) will switch to the backup power supply on V_{BAK}. The clock operates at extremely low current in order to maximize battery or capacitor life. However, an advantage of combining a clock function with FRAM memory is that data is not lost regardless of the backup power source.

Figure 10. I_{BAK} vs. V_{BAK} Voltage

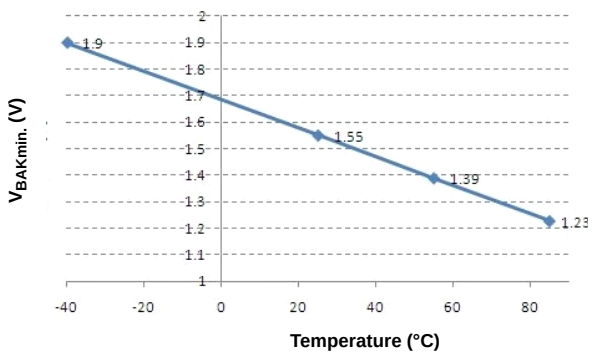


The I_{BAK} current varies with temperature and voltage (see DC Electrical Characteristics table). Figure 10 shows I_{BAK} as a function of V_{BAK}. These curves are useful for calculating backup time when a capacitor is used as the V_{BAK} source.

The minimum V_{BAK} voltage varies linearly with temperature. The user can expect the minimum V_{BAK} voltage to be 1.23 V at +85 °C and 1.90 V at -40 °C. The tested limit is 1.55 V at +25 °C.

Note The minimum V_{BAK} voltage has been characterized at -40 °C and +85 °C but is not 100% tested.

Figure 11. V_{BAK} (min.) vs Temperature



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Trickle Charger

To facilitate capacitor backup, the V_{BAK} pin can optionally provide a trickle charge current. When the VBC bit (register 18h, bit 3) is set to a '1', the V_{BAK} pin will source approximately 80 µA until V_{BAK} reaches V_{DD}. This charges the capacitor to V_{DD} without an external diode and resistor charger. There is also a Fast Charge mode which is enabled by the FC bit (register 18h, bit 2). In this mode the trickle charger current is set to approximately 1 mA, allowing a large backup capacitor to charge more quickly.

In the case where no backup supply is used, the V_{BAK} pin should be tied to V_{SS} and VBC bit cleared.

Note Systems using lithium batteries should clear the VBC bit to '0' to prevent battery charging. The V_{BAK} circuitry includes an internal 1 KΩ series resistor as a safety element. The trickle charger is UL Recognized.

Calibration

When the CAL bit in register 00h is set to a '1', the clock enters calibration mode. The FM33256B employs a digital method for calibrating the crystal oscillator frequency. The digital calibration scheme applies a digital correction to the RTC counters based on the calibration settings, CALS and CAL(4:0). In calibration mode (CAL = '1'), the ACS pin is driven with a 512 Hz (nominal) square wave and the alarm is temporarily unavailable. Any measured deviation from 512 Hz translates into a timekeeping error. The user measures the frequency and writes the appropriate correction value to the calibration register. The correction codes are listed in the table below. For convenience, the table also shows the frequency error in ppm. Positive ppm errors require a negative adjustment that removes pulses. Negative ppm errors require a positive correction that adds pulses. Positive ppm adjustments have the CALS (sign) bit set to '1', whereas negative ppm adjustments have CALS = '0'. After calibration, the clock will have a maximum error of ±2.17 ppm or ±0.09 minutes per month at the calibrated temperature.

The user will not be able to see the effect of the calibration setting on the 512 Hz output. The addition or subtraction of digital pulses occurs after the 512 Hz output.

The calibration setting is stored in F-RAM so it is not lost should the backup source fail. It is accessed with bits CAL(4:0) in register 01h. These bits can be written when the CAL bit is set to a '1'. To exit the calibration mode, the user must clear the CAL bit to a logic '0'. When the CAL bit is '0', the ACS pin will revert to the function according to Table 2.

Crystal Type

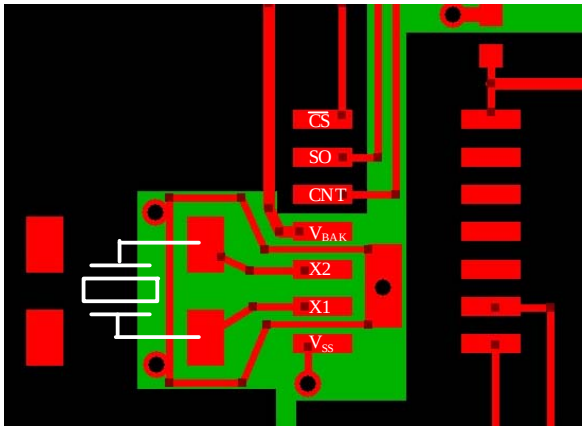
The crystal oscillator is designed to use a 6 pF/12.5 pF crystal without the need for external components, such as loading capacitors. The FM33256B device has built-in loading capacitors that are optimized for use with 6 pF crystals, but which work well with 12.5 pF crystals. For either crystal, no additional external loading capacitors are required nor suggested.

If a 32.768 kHz crystal is not used, an external oscillator may be connected to the FM33256B.

Layout Recommendations

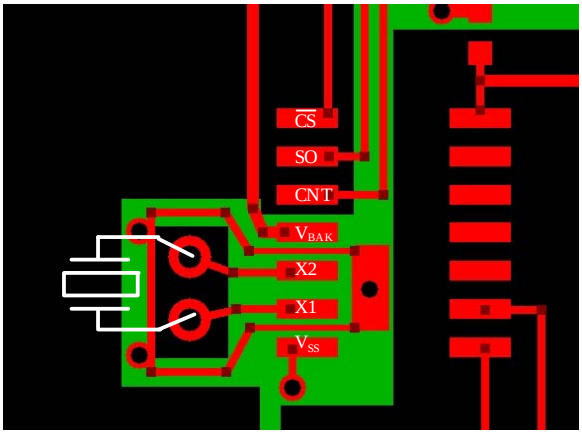
The X1 and X2 crystal pins employ very high impedance circuits and the oscillator connected to these pins can be upset by noise or extra loading. To reduce RTC clock errors from signal switching noise, a guard ring should be placed around these pads and the guard ring grounded. High speed SPI traces should be routed away from the X1/X2 pads. The X1 and X2 trace lengths should be less than 5 mm. The use of a ground plane on the backside or inner board layer is preferred. See layout example. Red is the top layer, green is the bottom layer.

Figure 12. Layout Recommendations



Layout for Surface Mount Crystal

(red = top layer, green = bottom layer)



Layout for Through Hole Crystal

(red = top layer, green = bottom layer)

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Table 4. Digital Calibration Adjustments

Positive Calibration for slow clocks: Calibration will achieve ± 2.17 PPM after calibration					
	Measured Frequency Range		Error Range (PPM)		
	Min	Max	Min	Max	Program Calibration Register to:
0	512.0000	511.9989	0	2.17	000000
1	511.9989	511.9967	2.18	6.51	100001
2	511.9967	511.9944	6.52	10.85	100010
3	511.9944	511.9922	10.86	15.19	100011
4	511.9922	511.9900	15.20	19.53	100100
5	511.9900	511.9878	19.54	23.87	100101
6	511.9878	511.9856	23.88	28.21	100110
7	511.9856	511.9833	28.22	32.55	100111
8	511.9833	511.9811	32.56	36.89	101000
9	511.9811	511.9789	36.90	41.23	101001
10	511.9789	511.9767	41.24	45.57	101010
11	511.9767	511.9744	45.58	49.91	101011
12	511.9744	511.9722	49.92	54.25	101100
13	511.9722	511.9700	54.26	58.59	101101
14	511.9700	511.9678	58.60	62.93	101110
15	511.9678	511.9656	62.94	67.27	101111
16	511.9656	511.9633	67.28	71.61	110000
17	511.9633	511.9611	71.62	75.95	110001
18	511.9611	511.9589	75.96	80.29	110010
19	511.9589	511.9567	80.30	84.63	110011
20	511.9567	511.9544	84.64	88.97	110100
21	511.9544	511.9522	88.98	93.31	110101
22	511.9522	511.9500	93.32	97.65	110110
23	511.9500	511.9478	97.66	101.99	110111
24	511.9478	511.9456	102.00	106.33	111000
25	511.9456	511.9433	106.34	110.67	111001
26	511.9433	511.9411	110.68	115.01	111010
27	511.9411	511.9389	115.02	119.35	111011
28	511.9389	511.9367	119.36	123.69	111100
29	511.9367	511.9344	123.70	128.03	111101
30	511.9344	511.9322	128.04	132.37	111110
31	511.9322	511.9300	132.38	136.71	111111

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Table 4. Digital Calibration Adjustments (continued)

Negative Calibration for fast clocks: Calibration will achieve ± 2.17 PPM after calibration					
	Measured Frequency Range		Error Range (PPM)		
	Min	Max	Min	Max	Program Calibration Register to:
0	512.0000	512.0011	0	2.17	000000
1	512.0011	512.0033	2.18	6.51	000001
2	512.0033	512.0056	6.52	10.85	000010
3	512.0056	512.0078	10.86	15.19	000011
4	512.0078	512.0100	15.20	19.53	000100
5	512.0100	512.0122	19.54	23.87	000101
6	512.0122	512.0144	23.88	28.21	000110
7	512.0144	512.0167	28.22	32.55	000111
8	512.0167	512.0189	32.56	36.89	001000
9	512.0189	512.0211	36.90	41.23	001001
10	512.0211	512.0233	41.24	45.57	001010
11	512.0233	512.0256	45.58	49.91	001011
12	512.0256	512.0278	49.92	54.25	001100
13	512.0278	512.0300	54.26	58.59	001101
14	512.0300	512.0322	58.60	62.93	001110
15	512.0322	512.0344	62.94	67.27	001111
16	512.0344	512.0367	67.28	71.61	010000
17	512.0367	512.0389	71.62	75.95	010001
18	512.0389	512.0411	75.96	80.29	010010
19	512.0411	512.0433	80.30	84.63	010011
20	512.0433	512.0456	84.64	88.97	010100
21	512.0456	512.0478	88.98	93.31	010101
22	512.0478	512.0500	93.32	97.65	010110
23	512.0500	512.0522	97.66	101.99	010111
24	512.0522	512.0544	102.00	106.33	011000
25	512.0544	512.0567	106.34	110.67	011001
26	512.0567	512.0589	110.68	115.01	011010
27	512.0589	512.0611	115.02	119.35	011011
28	512.0611	512.0633	119.36	123.69	011100
29	512.0633	512.0656	123.70	128.03	011101
30	512.0656	512.0678	128.04	132.37	011110
31	512.0678	512.0700	132.38	136.71	011111

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Register Map

The RTC and processor companion functions are accessed via 30 special function registers, which are mapped to unique opcodes. The interface protocol is described on page 23. The registers contain timekeeping data, alarm settings, control bits, and information flags. A description of each register follows the summary table.

Table 5. Register Map Summary Table

Battery-backed = ☐ Nonvolatile = ☐ BB/NV User Programmable = ☐

Address	Data								Function	Range
	D7	D6	D5	D4	D3	D2	D1	D0		
1Dh	$\overline{M}$	0	0	Alarm 10 months	Alarm months				Alarm Month	01-12
1Ch	$\overline{M}$	0	Alarm 10 date		Alarm date				Alarm Date	01-31
1Bh	$\overline{M}$	0	Alarm 10 hours		Alarm hours				Alarm Hours	00-23
1Ah	$\overline{M}$	Alarm 10 minutes			Alarm minutes				Alarm Minutes	00-59
19h	$\overline{M}$	Alarm 10 seconds			Alarm seconds				Alarm Seconds	00-59
18h	SNL	AL/SW	F1	F0	VBC	FC	VTP1	VTP0	Companion Control	
17h	Serial Number Byte 7								Serial Number 7	FFh
16h	Serial Number Byte 6								Serial Number 6	FFh
15h	Serial Number Byte 5								Serial Number 5	FFh
14h	Serial Number Byte 4								Serial Number 4	FFh
13h	Serial Number Byte 3								Serial Number 3	FFh
12h	Serial Number Byte 2								Serial Number 2	FFh
11h	Serial Number Byte 1								Serial Number 1	FFh
10h	Serial Number Byte 0								Serial Number 0	FFh
0Fh	Event Counter Byte 1								Event Counter 1	FFh
0Eh	Event Counter Byte 0								Event Counter 0	FFh
0Dh	NVC	-	-	-	RC	WC	POLL	CP	Event Counter Control	
0Ch	WDE	-	-	WDET4	WDET3	WDET2	WDET1	WDET0	Watchdog Control	
0Bh	-	-	-	WDST4	WDST3	WDST2	WDST1	WDST0	Watchdog Control	
0Ah	-	-	-	-	WR3	WR2	WR1	WR0	Watchdog Restart	
09h	EWDF	LWDF	POR	LB	-	-	-	-	Watchdog Flags	
08h	10 years				years				Years	00-99
07h	0	0	0	10 months	months				Month	01-12
06h	0	0	10 date		date				Date	01-31
05h	0	0	0	0	0	day			Day	01-07
04h	0	0	10 hours		hours				Hours	00-23
03h	0	10 minutes			minutes				Minutes	00-59
02h	0	10 seconds			seconds				Seconds	00-59
01h	-	-	CALS	CAL4	CAL3	CAL2	CAL1	CAL0	CAL/Control	
00h	$\overline{OSCEN}$	AF	CF	AEN	reserved	CAL	W	R	RTC/Alarm Control	

Note When the device is first powered up and programmed, all timekeeping registers must be written because the battery-backed register values cannot be guaranteed. The table below shows the default values of the non-volatile registers and some of the battery-backed bits. All other register values should be treated as unknown.

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Table 6. Default Register Values

Address	Hex Value
1Dh	0x81
1Ch	0x81
1Bh	0x80
1Ah	0x80
19h	0x80
18h	0x40
17h	0x00
16h	0x00
15h	0x00
14h	0x00
13h	0x00

Address	Hex Value
12h	0x00
11h	0x00
10h	0x00
0Fh	0x00
0Eh	0x00
0Dh	0x01
0Ch	0x00
0Bh	0x00
08h	0x00
07h	0x00
06h	0x00

Address	Hex Value
05h	0x00
04h	0x00
03h	0x00
02h	0x00
01h	0x00
00h	0x80

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Table 7. Register Description

Address	Description							
1Dh	**Alarm – Month**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{M}$	0	0	10 Month	Month.3	Month.2	Month.1	Month.0
	Contains the alarm value for the month and the mask bit to select or deselect the Month value.							
$\overline{M}$	Match. Setting this bit to '0' causes the Month value to be used in the alarm match logic. Setting this bit to '1' causes the match circuit to ignore the Month value. Battery-backed, read/write.							
1Ch	**Alarm – Date**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{M}$	0	10 date.1	10 date.0	Date.3	Date.2	Date.1	Date.0
	Contains the alarm value for the date and the mask bit to select or deselect the Date value.							
$\overline{M}$	Match: Setting this bit to '0' causes the Date value to be used in the alarm match logic. Setting this bit to '1' causes the match circuit to ignore the Date value. Battery-backed, read/write.							
1Bh	**Alarm – Hours**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{M}$	0	10 hours.1	10 hours.0	Hours.3	Hours.2	Hours.1	Hours.0
	Contains the alarm value for the hours and the mask bit to select or deselect the Hours value.							
$\overline{M}$	Match: Setting this bit to '0' causes the Hours value to be used in the alarm match logic. Setting this bit to '1' causes the match circuit to ignore the Hours value. Battery-backed, read/write.							
1Ah	**Alarm – Minutes**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{M}$	10 min.2	10 min.1	10 min.0	Min.3	Min.2	Min.1	Min.0
	Contains the alarm value for the minutes and the mask bit to select or deselect the Minutes value							
$\overline{M}$	Match: Setting this bit to '0' causes the Minutes value to be used in the alarm match logic. Setting this bit to '1' causes the match circuit to ignore the Minutes value. Battery-backed, read/write.							
19h	**Alarm – Seconds**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{M}$	10 sec.2	10 sec.1	10 sec.0	Seconds.3	Seconds.2	Seconds.1	Seconds.0
	Contains the alarm value for the seconds and the mask bit to select or deselect the Seconds value.							
$\overline{M}$	Match: Setting this bit to '0' causes the Seconds value to be used in the alarm match logic. Setting this bit to '1' causes the match circuit to ignore the Seconds value. Battery-backed, read/write.							
18h	**Companion Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SNL	AL/SW	F1	F0	VBC	FC	VTP1	VTP0
SNL	Serial Number Lock: Setting to a '1' makes registers 10h to 17h and SNL read-only. SNL cannot be cleared once set to '1'. Nonvolatile, read/write.							
AL/SW	Alarm/Square Wave Select: When set to '1', the alarm match drives the ACS pin as well as the AF flag. When set to '0', the selected Square Wave Freq will be driven on the ACS pin, and an alarm match only sets the AF flag. Nonvolatile, read/write.							

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Table 7. Register Description (continued)

Address	Description
F(1:0)	Square Wave Frequency Select: These bits select the frequency on the ACS pin when the CAL and AL/SW bits are both '0'. Nonvolatile. Setting — F(1:0) 1 Hz — 00 (default) 512 Hz — 01 4096 Hz — 10 32768 Hz — 11
VBC	VBAK Charger Control: Setting VBC to '1' (and FC = '0') causes a 80 µA (1 mA if FC = '1') trickle charge current to be supplied on V_{BAK}. Clearing VBC to '0' disables the charge current. Battery-backed, read/write. VBC — FC — Trickle charge current 0 — X — Disabled 1 — 0 — 80 µA 1 — 1 — 1 mA
FC	Fast Charge: Setting FC to '1' (and VBC = '1') causes a ~1 mA trickle charge current to be supplied on V_{BAK}. Clearing VBC to '0' disables the charge current. Battery-backed, read/write.
VTP(1:0)	VTP Select. These bits control the reset trip point for the low V_{DD} reset function. Nonvolatile, read/write. VTP — VTP1 — VTP0 2.60 V — 0 — 0 (factory default) 2.75 V — 0 — 1 2.90 V — 1 — 0 3.00 V — 1 — 1

17h	**Serial Number Byte 7**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.63	SN.62	SN.61	SN.60	SN.59	SN.58	SN.57	SN.56
16h	**Serial Number Byte 6**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.55	SN.54	SN.53	SN.52	SN.51	SN.50	SN.49	SN.48
15h	**Serial Number Byte 5**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.47	SN.46	SN.45	SN.44	SN.43	SN.42	SN.41	SN.40
14h	**Serial Number Byte 4**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.39	SN.38	SN.37	SN.36	SN.35	SN.34	SN.33	SN.32
13h	**Serial Number Byte 3**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.31	SN.30	SN.29	SN.28	SN.27	SN.26	SN.25	SN.24

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Table 7. Register Description (continued)

Address	Description							
12h	**Serial Number Byte 2**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.23	SN.22	SN.21	SN.20	SN.19	SN.18	SN.17	SN.16
11h	**Serial Number Byte 1**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.15	SN.14	SN.13	SN.12	SN.11	SN.10	SN.9	SN.8
10h	**Serial Number Byte 0**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.7	SN.6	SN.5	SN.4	SN.3	SN.2	SN.1	SN.0
	All serial number bytes are read/write when SNL = ‘0’, read-only when SNL = ‘1’. Nonvolatile.							
0Fh	**Event Counter Byte 1**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	EC.15	EC.14	EC.13	EC.12	EC.11	EC.10	EC.9	EC.8
	Event Counter Byte 1. Increments on programmed edge event on CNT input. Nonvolatile when NVC = ‘1’, Battery-backed when NVC = ‘0’, read/write.							
0Eh	**Event Counter Byte 0**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	EC.7	EC.6	EC.5	EC.4	EC.3	EC.2	EC.1	EC.0
	Event Counter Byte 0. Increments on programmed edge event on CNT input. Nonvolatile when NVC = ‘1’, Battery-backed when NVC = ‘0’, read/write.							
0Dh	**Event Counter Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	NVC	-	-	-	RC	WC	POLL	CP
NVC	Nonvolatile/Volatile Counter: Setting this bit to ‘1’ makes the counter nonvolatile and counter operates only when V_{DD} is greater than V_{TP}. Setting this bit to ‘0’ makes the counter volatile, which allows counter operation under V_{BAK} or V_{DD} power. If the NVC bit is changed, the counter value is not valid. Nonvolatile, read/write.							
RC	Read Counter. Setting this bit to ‘1’ takes a snapshot of the two counter bytes allowing the system to read the values without missing count events. The RC bit will be automatically cleared.							
WC	Write Counter. Setting this bit to a ‘1’ allows the user to write the counter bytes. While WC = ‘1’, the counter is blocked from count events on the CNT pin. The WC bit must be cleared by the user to activate the counter.							
POLL	Polled Mode: When POLL = ‘1’, the CNT pin is sampled for 30 µs every 125 ms. If POLL is set, the NVC bit is internally cleared and the CP bit is set to detect a rising edge. The RTC oscillator must be enabled ($\overline{OSCEN}$ = ‘0’) to operate in polled mode. When POLL = ‘0’, CNT pin is continuously active. Nonvolatile, read/write.							
CP	The CNT pin detects falling edges when CP = ‘0’, rising edges when CP = ‘1’. Nonvolatile, read/write.							

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Table 7. Register Description (continued)

Address	Description							
0Ch	**Watchdog Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	WDE	-	-	WDET4	WDET3	WDET2	WDET1	WDET0
WDE	Watchdog Enable: When WDE = '1', a watchdog timer fault will cause the $\overline{RST}$ signal to go active. When WDE = '0' the timer runs but has no effect on the $\overline{RST}$ pin. Nonvolatile, read/write.							
WDET(4:0)	Watchdog EndTime: Sets the ending time for the watchdog window timer with 60 ms (min.) resolution. The window timer allows independent leading and trailing edges (start and end of window) to be set. New watchdog timeouts are loaded when the timer is restarted by writing the 1010b pattern to WR(3:0). To save power (disable timer circuit), the EndTime may be set to all zeroes. Nonvolatile, read/write.							

Watchdog EndTime		WDET4	WDET3	WDET2	WDET1	WDET0
Disables Timer		0	0	0	0	0
(min.)	(max.)					
60 ms	200 ms	0	0	0	0	1
120 ms	400 ms	0	0	0	1	0
180 ms	600 ms	0	0	0	1	1
.	.					
.	.					
1200 ms	4000 ms	1	0	1	0	0
1260 ms	4200 ms	1	0	1	0	1
1320 ms	4400 ms	1	0	1	1	0
.	.					
.	.					
1740 ms	5800 ms	1	1	1	0	1
1800 ms	6000 ms	1	1	1	1	0
1860 ms	6200 ms	1	1	1	1	1

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Table 7. Register Description (continued)

Address	Description							
0Bh	**Watchdog Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	-	-	-	WDST4	WDST3	WDST2	WDST1	WDST0
WDST(4:0)	Watchdog StartTime. Sets the starting time for the watchdog window timer with 25 ms (max.) resolution. The window timer allow independent leading and trailing edges (start and end of window) to be set. New watchdog timer settings are loaded when the timer is restarted by writing the 1010b pattern to WR(3:0). Nonvolatile, read/write.							
	Watchdog StartTime		WDST4	WDST3	WDST2	WDST1	WDST0	
	0 ms (default)		0	0	0	0	0	
	(min.)	(max.)						
	7.5 ms	25 ms	0	0	0	0	1	
	15 ms	50 ms	0	0	0	1	0	
	22.5 ms	75 ms	0	0	0	1	1	
	.	.						
	.	.						
	150 ms	500 ms	1	0	1	0	0	
	157.5 ms	525 ms	1	0	1	0	1	
	165 ms	550 ms	1	0	1	1	0	
	.	.						
	.	.						
	217.5 ms	725 ms	1	1	1	0	1	
	225 ms	750 ms	1	1	1	1	0	
	232.5 ms	775 ms	1	1	1	1	1	
0Ah	**Watchdog Restart**							
	D7		**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	-		-	-	WR3	WR2	WR1	WR0
WR(3:0)	Watchdog Restart. Writing a pattern 1010b to WR(3:0) restarts the watchdog timer. The upper nibble contents do not affect this operation. Writing any pattern other than 1010b to WR(3:0) has no effect on the watchdog. Write-only.							
09h	**Watchdog Flags**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	EWDF	-	POR	LB	-	-	-	-
EWDF	Early Watchdog Timer Fault Flag: When a watchdog restart occurs too early (before the programmed watchdog StartTime), the $\overline{RST}$ pin is driven LOW and this flag is set. It must be cleared by the user. Note that both EWDF and POR could be set if both reset sources have occurred since the flags were cleared by the user. Battery-backed, read/write.							
LWDF	Late Watchdog Timer Fault Flag: When either a watchdog restart occurs too late (after the programmed watchdog EndTime) or no restart occurs, the $\overline{RST}$ pin is driven LOW and this flag is set. It must be cleared by the user. Note that both LWDF and POR could be set if both reset sources have occurred since the flags were cleared by the user. Battery-backed, read/write.							

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Table 7. Register Description (continued)

Address	Description							
POR	Power-On Reset: When the $\overline{RST}$ signal is activated by $V_{DD} < V_{TP}$, the POR bit will be set to '1'. A manual reset will not set this flag. Note that one or both of the watchdog flags and the POR flag could be set if both reset sources have occurred since the flags were cleared by the user. Battery-backed, read/write. (internally set, user must clear bit).							
LB	Low Backup: If the V_{BAK} source drops to a voltage level insufficient to operate the RTC/alarm when $V_{DD} < V_{BAK}$, this bit will be set to '1'. All registers need to be re-initialized since the battery-backed register values should be treated as unknown. The user should clear it to '0' when initializing the system. Battery-backed. Read/Write (internally set, user must clear bit).							
08h	**Timekeeping – Years**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	10 year.3	10 year.2	10 year.1	10 year.0	Year.3	Year.2	Year.1	Year.0
	Contains the lower two BCD digits of the year. Lower nibble contains the value for years; upper nibble contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is 0-99. Battery-backed, read/write.							
07h	**Timekeeping – Months**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	10 Month	Month.3	Month.2	Month.1	Month.0
	Contains the BCD digits for the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is 1-12. Battery-backed, read/write.							
06h	**Timekeeping – Date of the month**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10 date.1	10 date.0	Date.3	Date.2	Date.1	Date.0
	Contains the BCD digits for the date of the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 3. The range for the register is 1-31. Battery-backed, read/write.							
05h	**Timekeeping – Day of the week**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	0	0	Day.2	Day.1	Day.0
	Lower nibble contains a value that correlates to day of the week. Day of the week is a ring counter that counts from 1 to 7 then returns to 1. The user must assign meaning to the day value, as the day is not integrated with the date. Battery-backed, read/write.							
04h	**Timekeeping – Hours**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10 hours.1	10 hours.0	Hours.3	Hours.2	Hours.1	Hours.0
	Contains the BCD value of hours in 24-hour format. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0-23. Battery-backed, read/write.							

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Table 7. Register Description (continued)

Address	Description							
03h	**Timekeeping – Minutes**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10 min.2	10 min.1	10 min.0	Min.3	Min.2	Min.1	Min.0
	Contains the BCD value of minutes. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper minutes digit and operates from 0 to 5. The range for the register is 0-59. Battery-backed, read/write.							
02h	**Timekeeping - Seconds**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10 sec.2	10 sec.1	10 sec.0	Seconds.3	Seconds.2	Seconds.1	Seconds.0
	Contains the BCD value of seconds. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 5. The range for the register is 0-59. Battery-backed, read/write.							
01h	**CAL/Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	-	-	CALS	CAL.4	CAL.3	CAL.2	CAL.1	CAL.0
CALS	Calibration Sign: Determines if the calibration adjustment is applied as an addition to or as a subtraction from the time-base. This bit can be written only when CAL = ‘1’. Nonvolatile, read/write.							
CAL(4:0)	Calibration Code: These five bits control the calibration of the clock. These bits can be written only when CAL = ‘1’. Nonvolatile, read/write.							
00h	**RTC/Alarm Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{\text{OSCEN}}$	AF	CF	AEN	Reserved	CAL	W	R
$\overline{\text{OSCEN}}$	Oscillator Enable. When set to '1', the oscillator is halted. When set to '0', the oscillator runs. Disabling the oscillator can save battery power during storage. On a power-up without a V_{BAK} source or on a power-up after a V_{BAK} source has been applied, this bit is internally set to '1', which turns off the oscillator. Battery-backed, read/write.							
AF	Alarm Flag: This bit is set to ‘1’ when the time and date match the values stored in the alarm registers with the Match bit(s) = ‘0’. The user must clear it to '0'. Battery-backed. (internally set, user must clear bit)							
CF	Century Overflow Flag: This bit is set to a ‘1’ when the values in the years register overflows from 99 to 00. This indicates a new century, such as going from 1999 to 2000 or 2099 to 2100. The user should record the new century information as needed. The user must clear the CF bit to '0'. Battery-backed. (internally set, user must clear bit)							
AEN	Alarm Enable: This bit enables the alarm function. When AEN is set (and CAL cleared), the ACS pin operates as an active-low alarm. The state of the ACS pin is detailed in Table 2. When AEN is cleared, no new alarm events that set the AF bit will be generated. Clearing the AEN bit does not automatically clear AF. Battery-backed.							
CAL	Calibration Setting: When CAL is set to ‘1’, the clock enters calibration mode. When CAL is set to ‘0’, the clock operates normally, and the ACS pin is controlled by the RTC alarm. Battery-backed, read/write.							
W	Write Time. Setting the W bit to ‘1’ freezes updates of the user timekeeping registers. The user can then write them with updated values. Setting the W bit to ‘0’ causes the contents of the time registers to be transferred to the timekeeping counters. Battery-backed, read/write.							

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Table 7. Register Description (continued)

Address	Description
R	Read Time. Setting the R bit to '1' copies a static image of the timekeeping core and places it into the user registers. The user can then read them without concerns over changing values causing system errors. The R bit going from ‘0’ to ‘1’ causes the timekeeping capture, so the bit must be returned to ‘0’ prior to reading again. Battery-backed, read/write.
Reserved	Reserved bits. Do not use. Should remain set to ‘0’.

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Serial Peripheral Interface – SPI Bus

The FM33256B employs a serial peripheral interface (SPI) bus. It is specified to operate at speeds up to 16 MHz. This high-speed serial bus provides high-performance serial communication to an SPI master. Many common microcontrollers have hardware SPI ports allowing a direct interface. It is quite simple to emulate the port using ordinary port pins for microcontrollers that do not. The FM33256B operates in SPI Mode 0 and 3.

SPI Overview

The SPI is a four-pin interface with Chip Select ($\overline{CS}$), Serial Input (SI), Serial Output (SO), and Serial Clock (SCK) pins.

The SPI is a synchronous serial interface, which uses clock and data pins for memory access and supports multiple devices on the data bus. A device on the SPI bus is activated using the $\overline{CS}$ pin.

The relationship between chip select, clock, and data is dictated by the SPI mode. This device supports SPI modes 0 and 3. In both of these modes, data is clocked into the F-RAM on the rising edge of SCK starting from the first rising edge after $\overline{CS}$ goes active.

The SPI protocol is controlled by opcodes. These opcodes specify the commands from the bus master to the slave device. After $\overline{CS}$ is activated, the first byte transferred from the bus master is the opcode. Following the opcode, any addresses and data are then transferred. The $\overline{CS}$ must go inactive after an operation is complete and before a new opcode can be issued. The commonly used terms in the SPI protocol are as follows:

SPI Master

The SPI master device controls the operations on an SPI bus. An SPI bus may have only one master with one or more slave devices. All the slaves share the same SPI bus lines and the master may select any of the slave devices using the $\overline{CS}$ pin. All of the operations must be initiated by the master activating a slave device by pulling the $\overline{CS}$ pin of the slave LOW. The master also generates the SCK and all the data transmission on SI and SO lines are synchronized with this clock.

SPI Slave

The SPI slave device is activated by the master through the Chip Select line. A slave device gets the SCK as an input from the SPI master and all the communication is synchronized with this clock. An SPI slave never initiates a communication on the SPI bus and acts only on the instruction from the master.

The FM33256B operates as an SPI slave and may share the SPI bus with other SPI slave devices.

Chip Select ($\overline{CS}$)

To select any slave device, the master needs to pull down the corresponding $\overline{CS}$ pin. Any instruction can be issued to a slave device only while the $\overline{CS}$ pin is LOW. When the device is not selected, data through the SI pin is ignored and the serial output pin (SO) remains in a high-impedance state.

Note A new instruction must begin with the falling edge of $\overline{CS}$. Therefore, only one opcode can be issued for each active Chip Select cycle.

Serial Clock (SCK)

The Serial Clock is generated by the SPI master and the communication is synchronized with this clock after $\overline{CS}$ goes LOW.

The FM33256B enables SPI modes 0 and 3 for data communication. In both of these modes, the inputs are latched by the slave device on the rising edge of SCK and outputs are issued on the falling edge. Therefore, the first rising edge of SCK signifies the arrival of the first bit (MSB) of an SPI instruction on the SI pin. Further, all data inputs and outputs are synchronized with SCK.

Data Transmission (SI/SO)

The SPI data bus consists of two lines, SI and SO, for serial data communication. SI is also referred to as Master Out Slave In (MOSI) and SO is referred to as Master In Slave Out (MISO). The master issues instructions to the slave through the SI pin, while the slave responds through the SO pin. Multiple slave devices may share the SI and SO lines as described earlier.

The FM33256B has two separate pins for SI and SO, which can be connected with the master as shown in Figure 13.

For a microcontroller that has no dedicated SPI bus, a general-purpose port may be used. To reduce hardware resources on the controller, it is possible to connect the two data pins (SI, SO) together. Figure 14 shows such a configuration, which uses only three pins.

Most Significant Bit (MSB)

The SPI protocol requires that the first bit to be transmitted is the Most Significant Bit (MSB). This is valid for both address and data transmission.

The 256-Kbit serial F-RAM requires a 2-byte address for any read or write operation. Because the address is only 15 bits, the upper bit which is fed in is ignored by the device. Although this bit is ‘don’t care’, Cypress recommends that this bit be set to ‘0’ to enable seamless transition to higher memory densities.

Serial Opcode

After the slave device is selected with $\overline{CS}$ going LOW, the first byte received is treated as the opcode for the intended operation. FM33256B uses the standard opcodes for memory accesses.

Invalid Opcode

If an invalid opcode is received, the opcode is ignored and the device ignores any additional serial data on the SI pin until the next falling edge of $\overline{CS}$, and the SO pin remains tristated.

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Tel:150-1290-5940
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Status Register

The FM33256B has an 8-bit Status Register. The bits in the Status Register are used to configure the device. These bits are described in Table 10 on page 26.

Figure 13. System Configuration with SPI Port

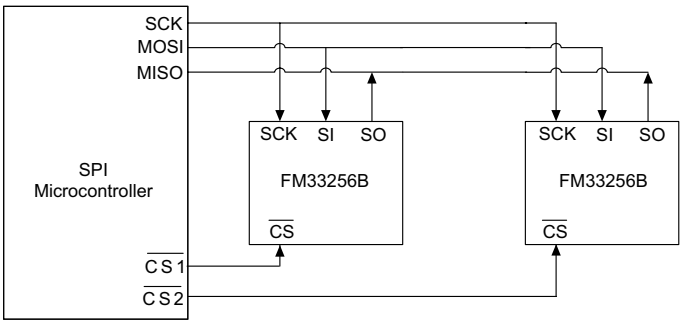
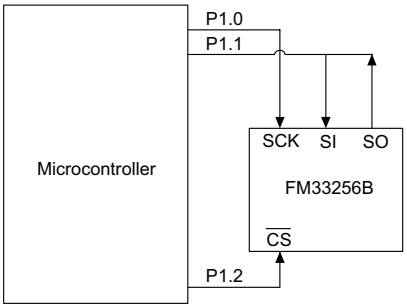


Figure 14. System Configuration without SPI Port



SPI Modes

The FM33256B may be driven by a microcontroller with its SPI peripheral running in either of the following two modes:

- SPI Mode 0 (CPOL = 0, CPHA = 0)
- SPI Mode 3 (CPOL = 1, CPHA = 1)

For both these modes, the input data is latched in on the rising edge of SCK starting from the first rising edge after $\overline{CS}$ goes active. If the clock starts from a HIGH state (in mode 3), the first rising edge after the clock toggles is considered. The output data is available on the falling edge of SCK.

The two SPI modes are shown in Figure 15 on page 24 and Figure 16 on page 24. The status of the clock when the bus master is not transferring data is:

- SCK remains at 0 for Mode 0
- SCK remains at 1 for Mode 3

The device detects the SPI mode from the status of the SCK pin when the device is selected by bringing the $\overline{CS}$ pin LOW. If the SCK pin is LOW when the device is selected, SPI Mode 0 is assumed and if the SCK pin is HIGH, it works in SPI Mode 3.

Figure 15. SPI Mode 0

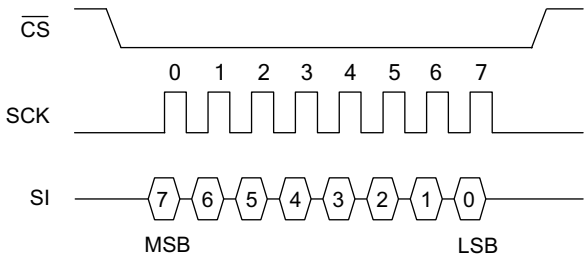
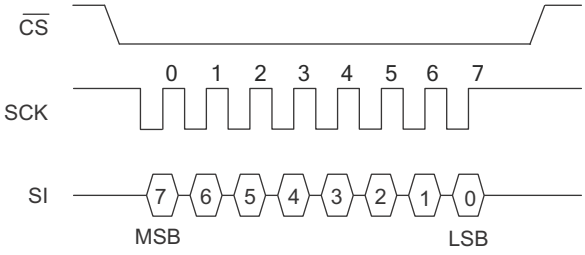


Figure 16. SPI Mode 3



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Power Up to First Access

The FM33256B is not accessible for a t_{PU} time after power-up. Users must comply with the timing parameter, t_{PU}, which is the minimum time from V_{DD} (min) to the first $\overline{CS}$ LOW.

Command Structure

There are eight commands, called opcodes, that can be issued by the bus master to the FM33256B. They are listed in Table 1. These opcodes control the functions performed by the memory and processor companion.

Table 8. Opcode Commands

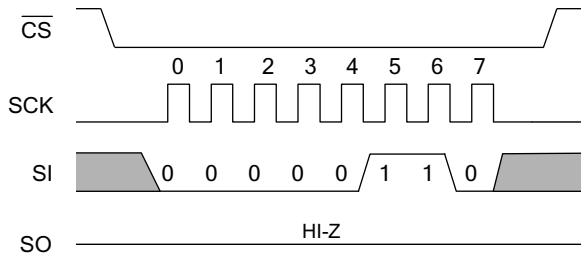
Name	Description	Opcode
WREN	Set write enable latch	0000 0110b
WRDI	Reset write enable latch	0000 0100b
RDSR	Read Status Register	0000 0101b
WRSR	Write Status Register	0000 0001b
READ	Read memory data	0000 0011b
WRITE	Write memory data	0000 0010b
RDPC	Read Processor Companion	0001 0011b
WRPC	Write Processor Companion	0001 0010b

WREN - Set Write Enable Latch

The FM33256B will power up with writes disabled. The WREN command must be issued before any write operation. Sending the WREN opcode allows the user to issue subsequent opcodes for write operations. These include writing the Status Register (WRSR) and writing the memory (WRITE).

Sending the WREN opcode causes the internal Write Enable Latch to be set. A flag bit in the Status Register, called WEL, indicates the state of the latch. WEL = '1' indicates that writes are permitted. Attempting to write the WEL bit in the Status Register has no effect on the state of this bit – only the WREN opcode can set this bit. The WEL bit will be automatically cleared on the rising edge of $\overline{CS}$ following a WRDI, a WRSR, a WRPC or a WRITE operation. This prevents further writes to the Status Register or the F-RAM array without another WREN command. Figure 17 illustrates the WREN command bus configuration.

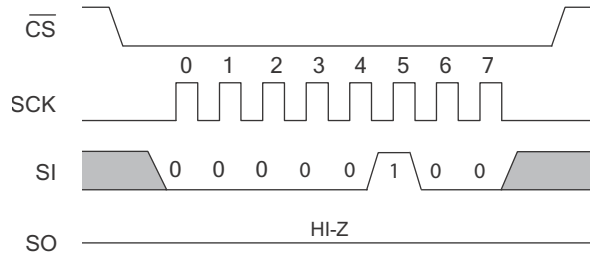
Figure 17. WREN Bus Configuration



WRDI - Reset Write Enable Latch

The WRDI command disables all write activity by clearing the Write Enable Latch. The user can verify that writes are disabled by reading the WEL bit in the Status Register and verifying that WEL is equal to '0'. Figure 18 illustrates the WRDI command bus configuration.

Figure 18. WRDI Bus Configuration



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Status Register and Write Protection

The write protection features of the FM33256B are multi-tiered and are enabled through the status register. The Status Register is organized as follows. (The default value shipped from the factory for bits 0-4, bit 6 is ‘0’ and bit 5 is ‘1’ in the Status Register).

Table 9. Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X (0)	X (1)	X (0)	X (0)	BP1 (0)	BP0 (0)	WEL (0)	X (0)

Table 10. Status Register Bit Definition

Bit	Definition	Description
Bit 0	Don’t care	This bit is non-writable and always returns ‘0’ upon read.
Bit 1 (WEL)	Write Enable	WEL indicates if the device is write enabled. This bit defaults to ‘0’ (disabled) on power-up. WEL = '1' --> Write enabled WEL = '0' --> Write disabled
Bit 2 (BP0)	Block Protect bit ‘0’	Used for block protection. For details, see Table 11 on page 26.
Bit 3 (BP1)	Block Protect bit ‘1’	Used for block protection. For details, see Table 11 on page 26.
Bit 4-5	Don’t care	These bits are non-writable and always return ‘0’ upon read.
Bit 6	Don’t care	This bit is non-writable and always returns ‘1’ upon read.
Bit 7	Don’t care	This bit is non-writable and always returns ‘0’ upon read.

Bit 0, bits 4-5 bit, bit 7 are fixed at ‘0’ and bit 6 is fixed at ‘1’; none of these bits can be modified. Note that bit 0 (“Ready or Write in progress” bit in serial flash and EEPROM) is unnecessary, as the F-RAM writes in real-time and is never busy, so it reads out as a ‘0’. BP1 and BP0 control the software write-protection features and are nonvolatile bits. The WEL flag indicates the state of the Write Enable Latch. Attempting to directly write the WEL bit in the Status Register has no effect on its state. This bit is internally set and cleared via the WREN and WRDI commands, respectively.

BP1 and BP0 are memory block write protection bits. They specify portions of memory that are write-protected as shown in Table 4.

Table 11. Block Memory Write Protection

BP1	BP0	Protected Address Range
0	0	None
0	1	6000h to 7FFFh (upper 1/4)
1	0	4000h to 7FFFh (upper 1/2)
1	1	0000h to 7FFFh (all)

The BP1 and BP0 bits and the Write Enable Latch are the only mechanisms that protect the memory from writes. The remaining write protection features protect inadvertent changes to the block protect bits.

RDSR - Read Status Register

The RDSR command allows the bus master to verify the contents of the Status Register. Reading the status register provides information about the current state of the write-protection features. Following the RDSR opcode, the FM33256B will return one byte with the contents of the Status Register.

WRSR - Write Status Register

The WRSR command allows the SPI bus master to write into the Status Register and change the write protect configuration by setting the BP0 and BP1 bits as required. Before sending the WRSR command, the user must send a WREN command to enable writes. Executing a WRSR command is a write operation and therefore, clears the Write Enable Latch.

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Figure 19. RDSR Bus Configuration

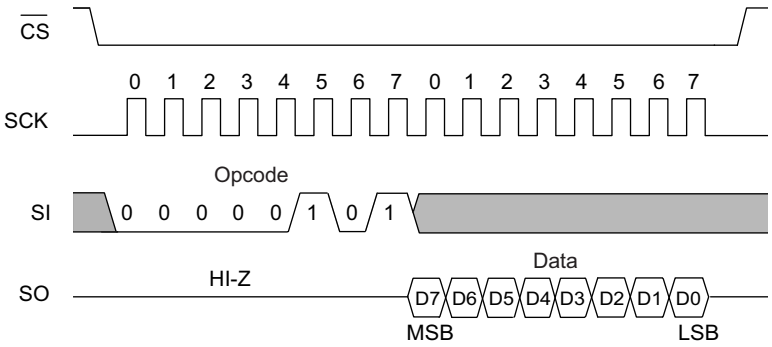
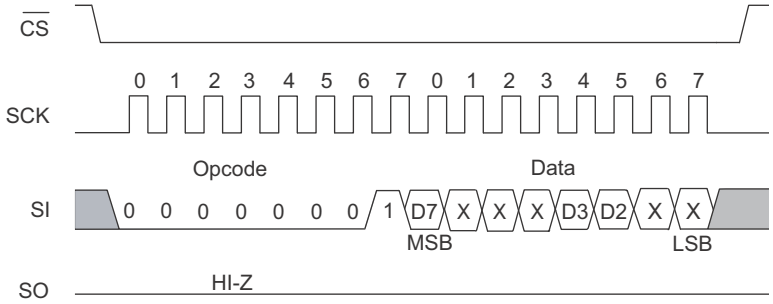


Figure 20. WRSR Bus Configuration (WREN not shown)



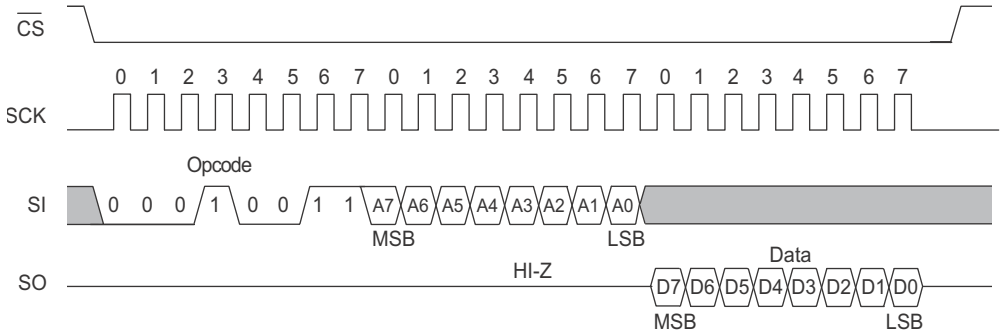
RDPC - Read Processor Companion

The RDPC command allows the bus master to verify the contents of the Processor Companion registers. Following the RDPC opcode, a single-byte register address is sent. The FM33256B will then return one or more bytes with the contents of the companion registers. When reading multiple data bytes, the internal register address will wrap around to 00h after 1Dh is reached.

WRPC - Write Processor Companion

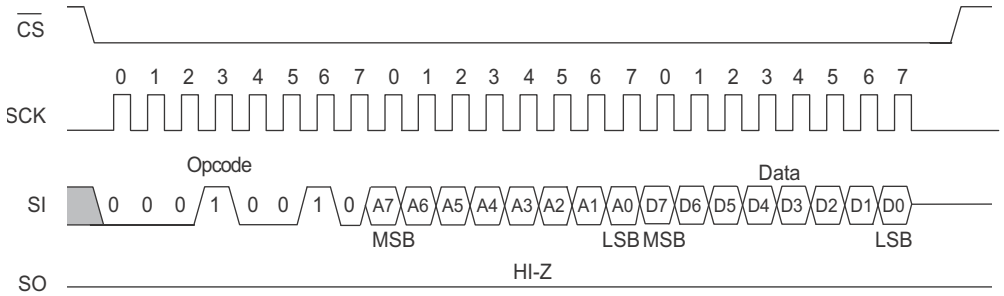
The WRPC command is used to set companion control settings. A WREN command is required prior to sending the WRPC command. Following the WRPC opcode, a single-byte register address is sent. The controller then drives one or more bytes to program the companion registers. When writing multiple data bytes, the internal register address will wrap around to 00h after 1Dh is reached. The rising edge of $\overline{CS}$ terminates a WRPC operation. See Figure 22.

Figure 21. Processor Companion Read



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Figure 22. Processor Companion Write (WREN not shown)



Memory Operation

The SPI interface, which is capable of a high clock frequency, highlights the fast write capability of the F-RAM technology. Unlike serial flash and EEPROMs, the FM33256B can perform sequential writes at bus speed. No page register is needed and any number of sequential writes may be performed.

Write Operation

All writes to the memory begin with a WREN opcode with $\overline{CS}$ being asserted and deasserted. The next opcode is WRITE. The WRITE opcode is followed by a two-byte address containing the 15-bit address (A14-A0) of the first data byte to be written into the memory. The upper bit of the two-byte address is ignored. Subsequent bytes are data bytes, which are written sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks and keeps $\overline{CS}$ LOW. If the last address of 7FFFh is reached, the counter will roll over to 0000h. Data is written MSB first. The rising edge of $\overline{CS}$ terminates a write operation. A write operation is shown in Figure 23.

Note When a burst write reaches a protected block address, the automatic address increment stops and all the subsequent data bytes received for write will be ignored by the device.

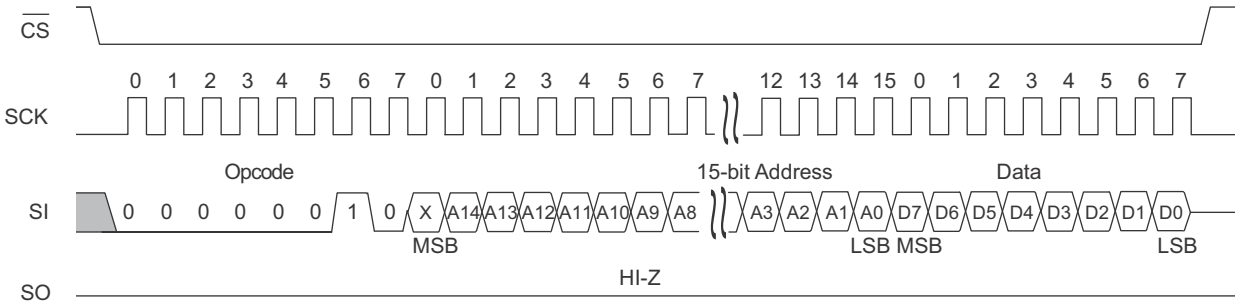
EEPROMs use page buffers to increase their write throughput. This compensates for the technology's inherently slow write operations. F-RAM memories do not have page buffers because each byte is written to the F-RAM array immediately after it is clocked in (after the eighth clock). This allows any number of bytes to be written without page buffer delays.

Note If the power is lost in the middle of the write operation, only the last completed byte will be written.

Read Operation

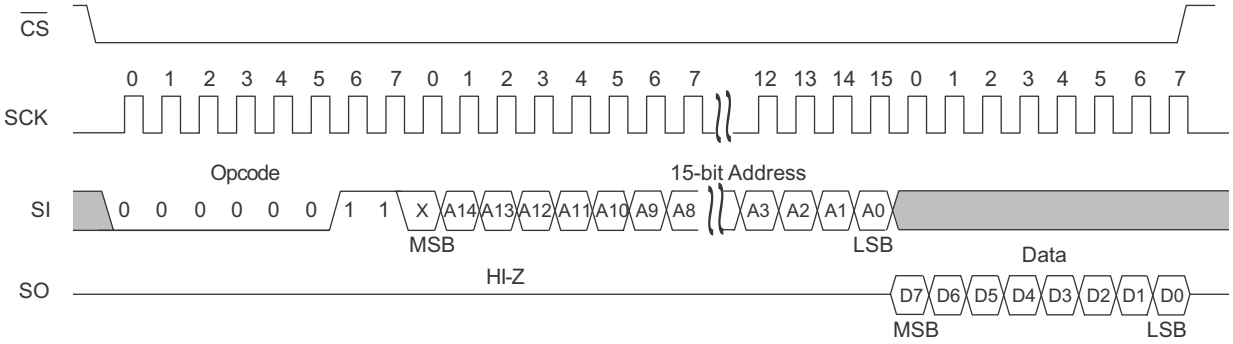
After the falling edge of $\overline{CS}$, the bus master can issue a READ opcode. Following the READ command is a two-byte address containing the 15-bit address (A14-A0) of the first byte of the read operation. The upper bit of the address is ignored. After the opcode and address are issued, the device drives out the read data on the next eight clocks. The SI input is ignored during read data bytes. Subsequent bytes are data bytes, which are read out sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks and $\overline{CS}$ is LOW. If the last address of 7FFFh is reached, the counter will roll over to 0000h. Data is read MSB first. The rising edge of $\overline{CS}$ terminates a read operation and tristates the SO pin. A read operation is shown in Figure 24.

Figure 23. Memory Write (WREN not shown) Operation



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Figure 24. Memory Read Operation



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Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –55 °C to +125 °C

Maximum accumulated storage time
At 125 °C ambient temperature ..... 1000 h
At 85 °C ambient temperature ..... 10 Years

Ambient temperature
with power applied ..... –55 °C to +125 °C

Supply voltage on V_{DD} relative to V_{SS} .....–1.0 V to +5.0 V

Input voltage ..... –1.0 V to +5.0 V and $V_{IN} < V_{DD} + 1.0$ V

Backup supply voltage.....–1.0 V to +4.5 V

DC voltage applied to outputs
in High-Z state .....–0.5 V to V_{DD} + 0.5 V

Transient voltage (< 20 ns) on
any pin to ground potential .....–2.0 V to V_{DD} + 2.0 V

Package power dissipation
capability (T_A = 25 °C) ..... 1.0 W

Surface mount lead soldering
temperature (3 seconds) ..... +260 °C

DC output current
(1 output at a time, 1s duration) ..... 15 mA

Electrostatic Discharge Voltage
Human Body Model (JEDEC Std JESD22-A114-E) ..... 4.5 kV

Charged Device Model (JEDEC Std JESD22-C101-C) ..... 1.25 kV

Machine Model (JEDEC Std JESD22-A115-A) 200

Latch-up current .....> ±100 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}
Industrial	–40 °C to +85 °C	2.7 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [2]	Max	Unit
V_{DD}[3]	Power supply			2.7	–	3.6	V
I_{DD}	V_{DD} supply current (VBC = '0')	SCK toggling between V_{DD} – 0.3 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.3 V. SO = Open	f_{SCK} = 1 MHz	–	–	1.1	mA
			f_{SCK} = 16 MHz	–	–	16.0	mA
I_{SB}	V_{DD} standby current Trickle Charger Off (VBC = '0')	$\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.		–	–	150	µA
V_{BAK}[4]	RTC backup voltage		T_A = +25 °C to +85 °C	1.55	–	3.75	V
			T_A = –40 °C to +25 °C	1.90	–	3.75	V
I_{BAK}	RTC backup current	$V_{DD} < V_{SW}$, oscillator running, CNT at V_{BAK}.	T_A = +25 °C, V_{BAK} = 3.0 V	–	–	1.4	µA
			T_A = +85 °C, V_{BAK} = 3.0 V	–	–	2.0	µA
			T_A = +25 °C, V_{BAK} = 2.0 V	–	–	1.15	µA
			T_A = +85 °C, V_{BAK} = 2.0 V	–	–	1.65	µA
I_{BAKTC}[5]	Trickle Charge Current with V_{BAK} = 0 V		Fast Charge Off (FC = '0')	50	–	200	µA
			Fast Charge On (FC = '1')	200	–	2500	µA

Notes
2. Typical values are at 25 °C, $V_{DD} = V_{DD}$(typ). Not 100% tested.
3. Full complete operation. Supervisory circuits, RTC, etc operate to lower voltages as specified.
4. The V_{BAK} trickle charger automatically regulates the maximum voltage on this pin for capacitor backup applications.
5. V_{BAK} will source current when trickle charge is enabled (VBC bit = '1'), $V_{DD} > V_{BAK}$, and $V_{BAK} < V_{BAK}$(max).

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DC Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [2]	Max	Unit
I_{QTC}[6]	V_{DD} Quiescent Current (VBC = '1')			–	–	70	µA
I_{QWD}[7]	V_{DD} Quiescent Current (WDE = '1')			–	–	30	µA
V_{TP0}	V_{DD} Trip Point Voltage, VTP(1:0) = 00b	$\overline{RST}$ is asserted active when $V_{DD} < V_{TP}$.		2.53	2.6	2.72	V
V_{TP1}	V_{DD} Trip Point Voltage, VTP(1:0) = 01b	$\overline{RST}$ is asserted active when $V_{DD} < V_{TP}$.		2.68	2.75	2.87	V
V_{TP2}	V_{DD} Trip Point Voltage, VTP(1:0) = 10b	$\overline{RST}$ is asserted active when $V_{DD} < V_{TP}$.		2.78	2.9	2.99	V
V_{TP3}	V_{DD} Trip Point Voltage, VTP(1:0) = 11b	$\overline{RST}$ is asserted active when $V_{DD} < V_{TP}$.		2.91	3.0	3.15	V
V_{RST}[8]	V_{DD} for valid $\overline{RST}$	I_{OL} = 80 µA at V_{OL}	$V_{BAK} > V_{BAK}$ min	0	–	–	V
			$V_{BAK} < V_{BAK}$ min	1.6	–	–	V
V_{SW}	Battery Switchover voltage	$\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.		2.0	–	2.7	V
I_{LI}	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$. Does not apply to PFI, $\overline{RST}$, X1, or X2		–	–	±1	µA
I_{LO}	Output leakage current	$V_{SS} \le V_{OUT} \le V_{DD}$. Does not apply to $\overline{RST}$, X1, or X2		–	–	±1	µA
V_{IL}[9]	Input LOW voltage		All inputs except as listed below	– 0.3	–	0.3 × V_{DD}	V
			CNT battery-backed ($V_{DD} < V_{SW}$)	– 0.3	–	0.5	V
			CNT ($V_{DD} > V_{SW}$)	– 0.3	–	0.8	V
V_{IH}	Input HIGH voltage		All inputs except as listed below	0.7 × V_{DD}	–	V_{DD} + 0.3	V
			CNT battery-backed ($V_{DD} < V_{SW}$)	V_{BAK} – 0.5	–	V_{BAK} + 0.3	V
			CNT ($V_{DD} > V_{SW}$)	0.7 × V_{DD}	–	V_{DD} + 0.3	V
			PFI	–	–	V_{DD} + 0.3	V

Notes
6. This is the V_{DD} supply current contributed by enabling the trickle charger circuit, and does not account for I_{BAKTC}.
7. This is the V_{DD} supply current contributed by enabling the watchdog circuit, WDE = '1' and WDET set to a non-zero value.
8. The minimum V_{DD} to guarantee the level of $\overline{RST}$ remains a valid V_{OL} level.
9. Includes $\overline{RST}$ input detection of external reset condition to trigger driving of $\overline{RST}$ signal by FM33256B.

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DC Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions	Min	Typ [2]	Max	Unit
V_{OH}	Output HIGH voltage (SO, PFO)	I_{OH} = –2 mA	V_{DD} – 0.8	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 3 mA	–	–	0.4	V
R_{RST}	Pull-up resistance for $\overline{RST}$ inactive		50	–	400	kΩ
V_{PFI}	Power Fail Input Reference Voltage		1.475	1.50	1.525	V
V_{HYS}	Power Fail Input (PFI) Hysteresis (Rising)		–	–	100	mV

Data Retention and Endurance

Parameter	Description	Test condition	Min	Max	Unit
T_{DR}	Data retention	T_A = 85 °C	10	–	Years
		T_A = 75 °C	38	–	
		T_A = 65 °C	151	–	
NV_C	Endurance	Over operating temperature	10^{14}	–	Cycles

Capacitance

Parameter [10]	Description	Test Conditions	Typ	Max	Unit
C_{IO}	Input/Output pin capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = V_{DD}(typ)	–	8	pF
C_{XTL}	X1, X2 Crystal pin Capacitance		12	–	pF
C_{CNT}[11]	Max. Allowable Capacitance on CNT (polled mode)		–	100	pF

Thermal Resistance

Parameter	Description	Test Conditions	14-pin SOIC	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	81	°C/W
Θ_{JC}	Thermal resistance (junction to case)		31	°C/W

AC Test Conditions

Input pulse levels .....10% and 90% of V_{DD}
Input rise and fall times .....5 ns
Input and output timing reference levels .....0.5 × V_{DD}
Output load capacitance ..... 30 pF

Notes
10. This parameter is characterized and not 100% tested.
11. The crystal attached to the X1/X2 pins must be rated as 6 pF/12.5 pF.

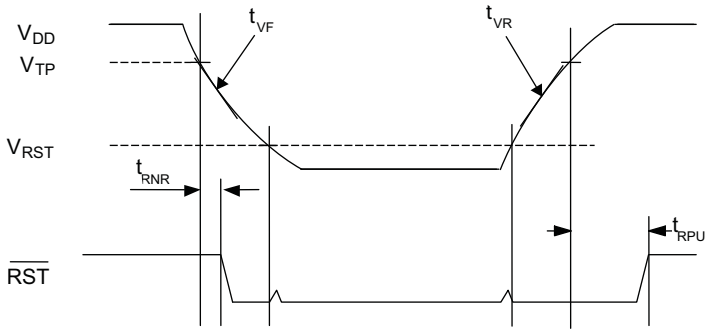
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Supervisor Timing

Over the Operating Range

Parameter	Description	Min	Max	Units
t_{RPU}[12]	$\overline{RST}$ active (LOW) after $V_{DD} > V_{TP}$	30	100	ms
t_{RNR}[13]	$\overline{RST}$ response time to $V_{DD} < V_{TP}$ (noise filter)	7	25	µs
t_{VR}[13, 14]	V_{DD} power-up ramp rate	50	100,000	µs/V
t_{VF}[13, 14]	V_{DD} power-down ramp rate	100	-	µs/V
t_{WDST}[15]	Watchdog StartTime	0.3 × t_{DOG1}	t_{DOG1}	ms
t_{WDET}[15]	Watchdog EndTime	t_{DOG2}	3.3 × t_{DOG2}	ms
f_{CNT}	Frequency of event counter	0	1	kHz

Figure 25. $\overline{RST}$ Timing



Notes

12. The $\overline{RST}$ pin will drive LOW for this length of time after the internal reset circuit is activated due to a watchdog, low voltage, or manual reset event.
13. This parameter is characterized and not 100% tested.
14. Slope measured at any point on V_{DD} waveform.
15. t_{DOG1} is the programmed StartTime and t_{DOG2} is the programmed EndTime in registers 0Bh and 0Ch, $V_{DD} > V_{TP}$, and t_{RPU} satisfied. The StartTime has a resolution of 25 ms. The EndTime has a resolution of 60 ms.

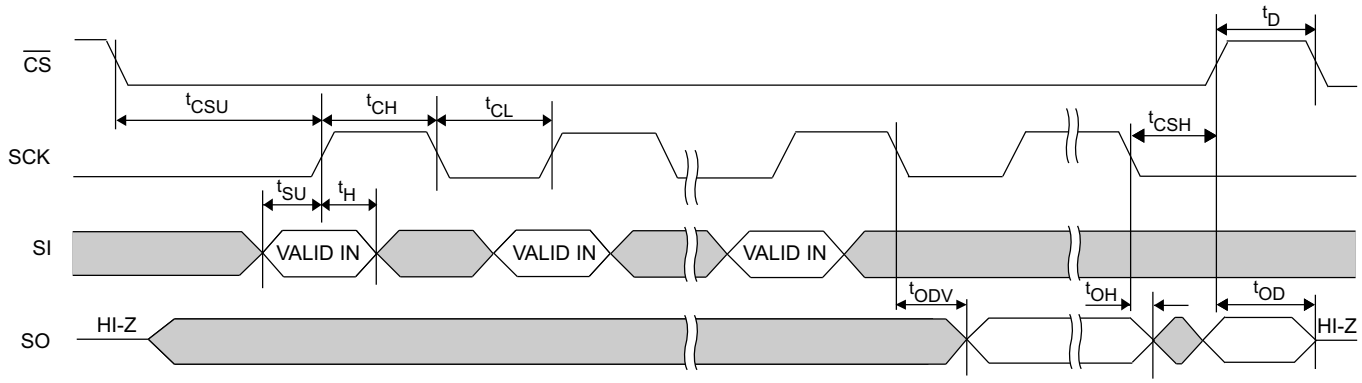
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AC Switching Characteristics

Over the Operating Range

Parameters [16]		Description	Min	Max	Unit
Cypress Parameter	Alt. Parameter				
f_{SCK}	–	SCK clock frequency	0	16	MHz
t_{CH}	–	Clock HIGH time	28	–	ns
t_{CL}	–	Clock LOW time	28	–	ns
t_{CSU}	t_{CSS}	Chip select setup	10	–	ns
t_{CSH}	t_{CSH}	Chip select hold	10	–	ns
t_{OD} [17, 18]	t_{HZCS}	Output disable time	–	20	ns
t_{ODV}	t_{CO}	Output data valid time	–	24	ns
t_{OH}	–	Output hold time	0	–	ns
t_D	–	Deselect time	90	–	ns
t_R [19]	–	Data in rise time	–	50	ns
t_F [19]	–	Data in fall time	–	50	ns
t_{SU}	t_{SD}	Data setup time	6	–	ns
t_H	t_{HD}	Data hold time	6	–	ns

Figure 26. Synchronous Data Timing (Mode 0)



Notes

16. Test conditions assume a signal transition time of 5 ns or less, timing reference levels of 0.5 × V_{DD}, input pulse levels of 10% to 90% of V_{DD}, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance shown in AC Test Conditions on page 32.
17. t_{OD} is specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state
18. This parameter is characterized and not 100% tested.
19. Rise and fall times measured between 10% and 90% of waveform.

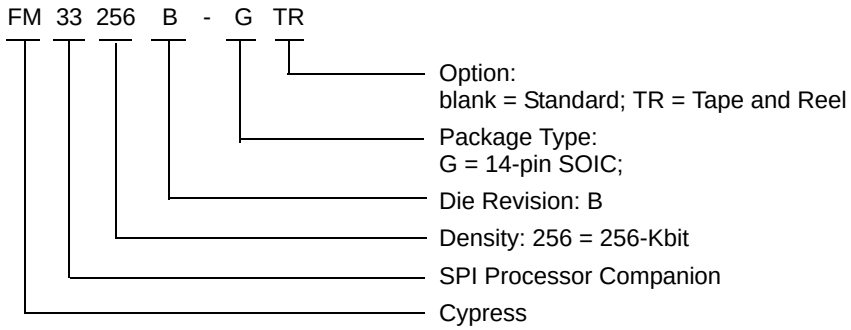
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Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
FM33256B-G	51-85067	14-pin SOIC	Industrial
FM33256B-GTR	51-85067	14-pin SOIC	

All these parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

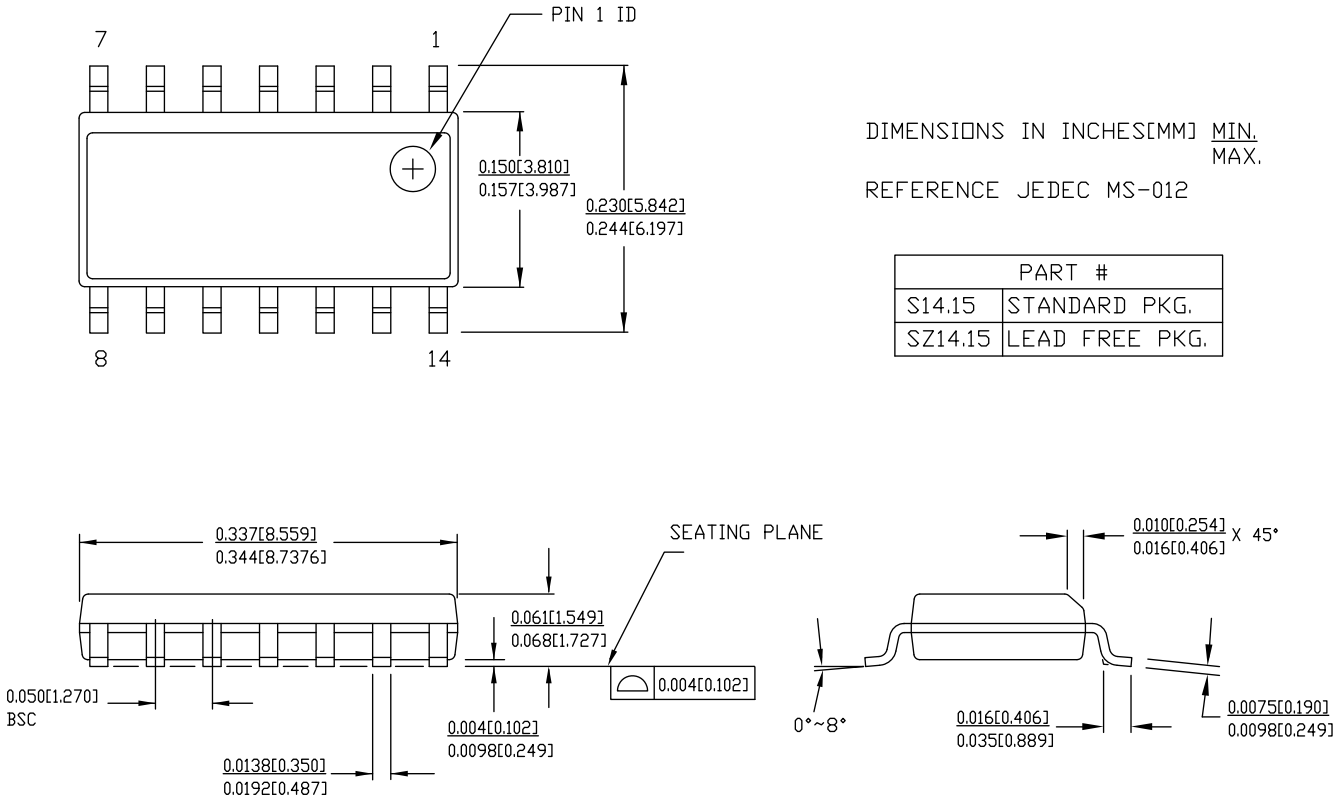
Ordering Code Definitions



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Package Diagram

Figure 27. 14-pin SOIC (150 Mils) Package Outline, 51-85067



51-85067 *E

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Acronyms

Acronym	Description
CPHA	Clock Phase
CPOL	Clock Polarity
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIA	Electronic Industries Alliance
F-RAM	Ferroelectric Random Access Memory
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
JESD	JEDEC Standards
LSB	Least Significant Bit
MSB	Most Significant Bit
NMI	Non Maskable interrupt
RoHS	Restriction of Hazardous Substances
SPI	Serial Peripheral Interface
SOIC	Small Outline Integrated Circuit

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
kΩ	kiloohm
Mbit	megabit
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

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Document History Page

Document Title: FM33256B, 256-Kbit (32 K × 8) Integrated Processor Companion with F-RAM Document Number: 001-86213				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3912947	GVCH	02/25/2013	New spec
*A	4333078	GVCH	05/05/2014	Converted to Cypress standard format Crystal Type: Added use of 6 pF crystal Updated Maximum Ratings table - Removed Moisture Sensitivity Level (MSL) - Added junction temperature and latch up current Updated Data Retention and Endurance table Changed C_{XTL} parameter typ value from 25 pF to 12 pF. Added Thermal Resistance table Removed Package Marking Scheme (top mark) Removed Ramtron revision history
*B	4563141	GVCH	11/06/2014	Added related documentation hyperlink in page 1.
*C	4872944	ZSK / PSR	08/05/2015	Updated Maximum Ratings: Removed “Maximum junction temperature”. Added “Maximum accumulated storage time”. Added “Ambient temperature with power applied”. Updated Package Diagram: spec 51-85067 – Changed revision from *D to *E. Updated to new template.

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