FM24V02A

256-Kbit (32K × 8) Serial (I^2C) F-RAM

Features

- 256-Kbit ferroelectric random access memory (F-RAM) logically organized as 32K × 8
  - High-endurance 100 trillion (10^{14}) read/writes
  - 151-year data retention (See the Data Retention and Endurance table)
  - NoDelay™ writes
  - Advanced high-reliability ferroelectric process
- Fast two-wire serial interface (I^2C)
  - Up to 3.4-MHz frequency[1]
  - Direct hardware replacement for serial EEPROM
  - Supports legacy timings for 100 kHz and 400 kHz
- Device ID
  - Manufacturer ID and Product ID
- Low power consumption
  - 175-µA active current at 100 kHz
  - 150-µA standby current
  - 8-µA sleep mode current
- Low-voltage operation: V_{DD} = 2.0 V to 3.6 V
- Industrial temperature: –40 °C to +85 °C
- 8-pin small outline integrated circuit (SOIC) package
- Restriction of hazardous substances (RoHS) compliant

Functional Description

The FM24V02A is a 256-Kbit nonvolatile memory employing an advanced ferroelectric process. An F-RAM is nonvolatile and performs reads and writes similar to a RAM. It provides reliable data retention for 151 years while eliminating the complexities, overhead, and system-level reliability problems caused by EEPROM and other nonvolatile memories.

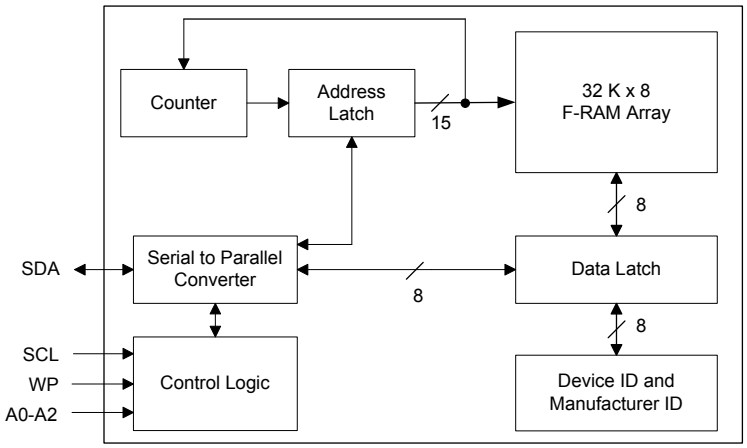
Unlike EEPROM, the FM24V02A performs write operations at bus speed. No write delays are incurred. Data is written to the memory array immediately after each byte is successfully transferred to the device. The next bus cycle can commence without the need for data polling. In addition, the product offers substantial write endurance compared with other nonvolatile memories. F-RAM also exhibits much lower power during writes than EEPROM because write operations do not require an internally elevated power supply voltage for write circuits. The FM24V02A is capable of supporting 10^{14} read/write cycles, or 100 million times more write cycles than EEPROM.

These capabilities make the FM24V02A ideal for nonvolatile memory applications, requiring frequent or rapid writes. Examples range from data logging, where the number of write cycles may be critical, to demanding industrial controls where the long write time of EEPROM can cause data loss. The combination of features allows more frequent data writing with less overhead for the system.

The FM24V02A provides substantial benefits to users of serial EEPROM as a hardware drop-in replacement. The device incorporates a read-only Device ID that allows the host to determine the manufacturer, product density, and product revision. The device specifications are guaranteed over an industrial temperature range of –40 °C to +85 °C.

For a complete list of related resources, click here.

Logic Block Diagram



Note

1. The FM24V02A does not meet the NXP I^2C specification in the Fast-mode Plus (Fm+, 1 MHz) for I_{OL} and in the High Speed Mode (Hs-mode, 3.4 MHz) for V_{hys}. Refer to the DC Electrical Characteristics table for more details.

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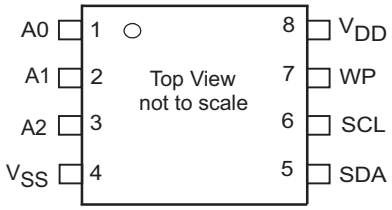
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Pinout

Figure 1. 8-pin SOIC Pinout



Pin Definitions

Pin Name	I/O Type	Description
A0-A2	Input	**Device Select Address 0-2**. These pins are used to select one of up to eight devices of the same type on the same two-wire bus. To select the device, the address value on the three pins must match the corresponding bits contained in the slave address. The address pins are pulled down internally.
SDA	Input/Output	**Serial Data Address**. This is a bidirectional pin for the two-wire interface. It is open-drain and is intended to be wire-AND'd with other devices on the two-wire bus. The input buffer incorporates a Schmitt trigger for noise immunity and the output driver includes slope control for falling edges. An external pull-up resistor is required.
SCL	Input	**Serial Clock**. The serial clock pin for the two-wire interface. Data is clocked out of the part on the falling edge, and into the device on the rising edge. The SCL input also incorporates a Schmitt trigger input for noise immunity.
WP	Input	**Write Protect**. When tied to V_{DD}, addresses in the entire memory map will be write-protected. When WP is connected to ground, all addresses are write enabled. This pin is pulled down internally.
V_{SS}	Power supply	Ground for the device. Must be connected to the ground of the system.
V_{DD}	Power supply	Power supply input to the device.

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Functional Overview

The FM24V02A is a serial F-RAM memory. The memory array is logically organized as 32,768 × 8 bits and is accessed using a two-wire (I^2C) interface. The functional operation of the F-RAM is similar to serial EEPROM. The major difference between the FM24V02A and a serial EEPROM with the same pinout is the F-RAM's superior write performance, high endurance, and low power consumption.

Memory Architecture

When accessing the FM24V02A, the user addresses 32K locations of eight data bits each. These eight data bits are shifted in or out serially. The addresses are accessed using the two-wire protocol, which includes a slave address (to distinguish other non-memory devices) and a two-byte address. The upper MSB bit of the address range is 'don't care' value. The complete address of 15 bits specifies each byte address uniquely.

The access time for the memory operation is essentially zero, beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the two-wire bus. Unlike a serial EEPROM, it is not necessary to poll the device for a ready condition because writes occur at bus speed. By the time a new bus transaction can be shifted into the device, a write operation is complete. This is explained in more detail in Memory Operation on page 7.

Two-wire Interface

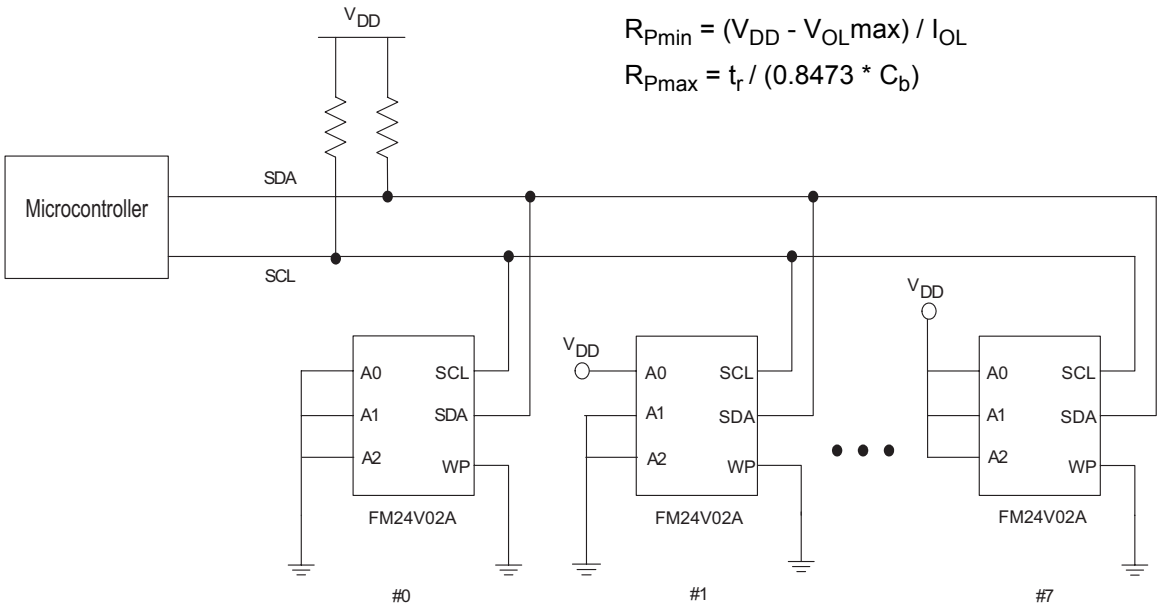
The FM24V02A employs a bidirectional two-wire bus protocol using few pins or board space. Figure 2 illustrates a typical system configuration using the FM24V02A in a microcontroller-based system. The two-wire bus is familiar to many users but is described in this section.

By convention, any device that is sending data to the bus is the transmitter while the target device for this data is the receiver. The device that is controlling the bus is the master. The master is responsible for generating the clock signal for all operations. Any device on the bus that is being controlled is a slave. The FM24V02A is always a slave device.

The bus protocol is controlled by transition states in the SDA and SCL signals. There are four conditions including START, STOP, data bit, or acknowledge. Figure 3 and Figure 4 on page 5 illustrate the signal conditions that specify the four states. Detailed timing diagrams are shown in the electrical specifications section.

The FM24V02A does not meet the NXP I^2C specification in the Fast-mode Plus (Fm+, 1 MHz) for I_{OL} and in the High Speed Mode (Hs-mode, 3.4 MHz) for V_{hys}. Refer to the DC Electrical Characteristics table for more details.

Figure 2. System Configuration Using Serial (I^2C) F-RAM



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STOP Condition (P)

A STOP condition is indicated when the bus master drives SDA from LOW to HIGH while the SCL signal is HIGH. All operations using the FM24V02A should end with a STOP condition. If an operation is in progress when a STOP is asserted, the operation will be aborted. The master must have control of SDA (not a memory read) in order to assert a STOP condition.

START Condition (S)

A START condition is indicated when the bus master drives SDA from HIGH to LOW while the SCL signal is HIGH. All commands should be preceded by a START condition. An operation in progress can be aborted by asserting a START condition at any time. Aborting an operation using the START condition will ready the FM24V02A for a new operation.

If during operation the power supply drops below the specified V_{DD} minimum, the system should issue a START condition prior to performing another operation.

Figure 3. START and STOP Conditions

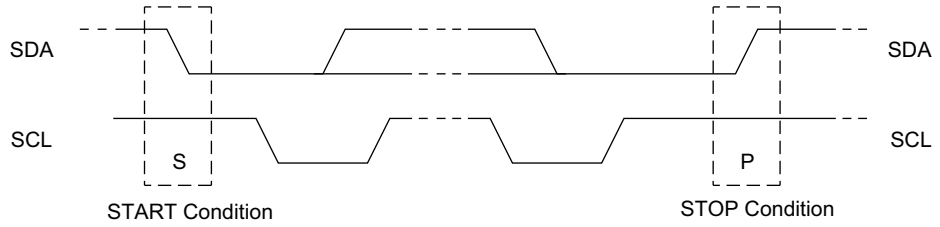
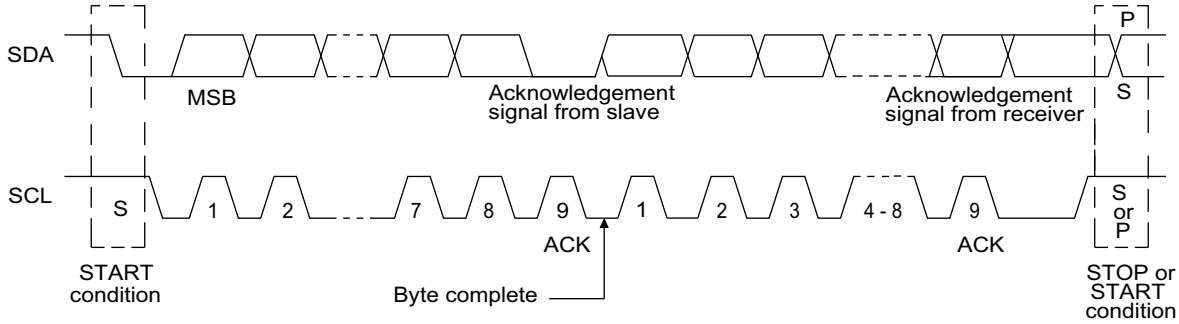


Figure 4. Data Transfer on the I²C Bus



Data/Address Transfer

All data transfers (including addresses) take place while the SCL signal is HIGH. Except under the three conditions described above, the SDA signal should not change while SCL is HIGH.

Acknowledge / No-Acknowledge

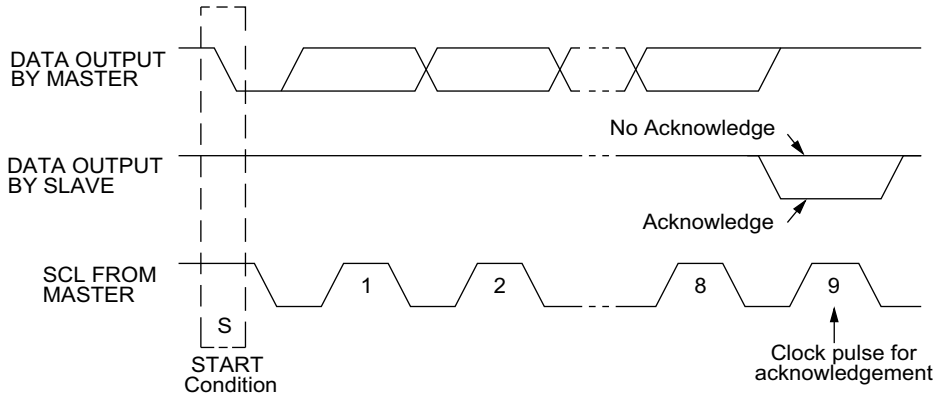
The acknowledge takes place after the 8th data bit has been transferred in any transaction. During this state the transmitter should release the SDA bus to allow the receiver to drive it. The receiver drives the SDA signal LOW to acknowledge receipt of the byte. If the receiver does not drive SDA LOW, the condition is a no-acknowledge and the operation is aborted.

The receiver will fail to acknowledge for two distinct reasons, the first being that a byte transfer fails. In this case, the no-acknowledge ceases the current operation so that the part can be addressed again. This allows the last byte to be recovered in the event of a communication error.

The second and most common reason is that the receiver does not acknowledge to deliberately end an operation. For example, during a read operation, the FM24V02A will continue to place data on the bus as long as the receiver sends acknowledges (and clocks). When a read operation is complete and no more data is needed, the receiver must not acknowledge the last byte. If the receiver acknowledges the last byte, this causes the FM24V02A to attempt to drive the bus on the next clock while the master is sending a new command such as STOP.

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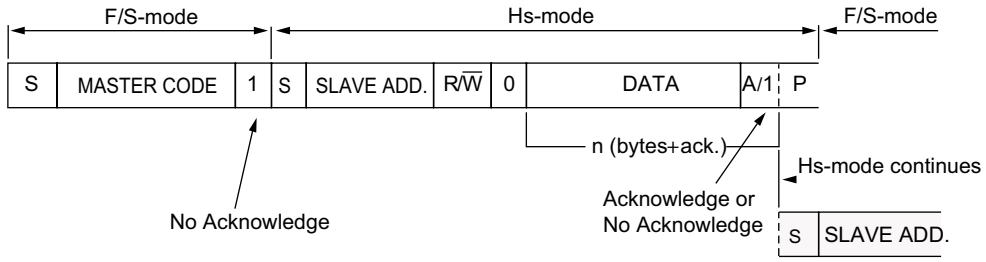
Figure 5. Acknowledge on the I²C Bus



High Speed Mode (Hs-mode)

The FM24V02A supports a 3.4-MHz high-speed mode. A master code (00001XXXb) must be issued to place the device into the high-speed mode. Communication between master and slave will then be enabled for speeds up to 3.4-MHz. A STOP condition will exit Hs-mode. Single- and multiple-byte reads and writes are supported.

Figure 6. Data Transfer Format in Hs-mode

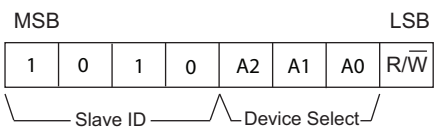


Slave Device Address

The first byte that the FM24V02A expects after a START condition is the slave address. As shown in Figure 7, the slave address contains the device type or slave ID, the device select address bits, and a bit that specifies if the transaction is a read or a write.

Bits 7-4 are the device type (slave ID) and should be set to 1010b for the FM24V02A. These bits allow other function types to reside on the two-wire bus within an identical address range. Bits 3-1 are the device select address bits. They must match the corresponding value on the external address pins to select the device. Up to eight FM24V02A devices can reside on the same two-wire bus by assigning a different address to each. Bit 0 is the read/write bit (R/$\overline{W}$). R/$\overline{W}$ = '1' indicates a read operation and R/$\overline{W}$ = '0' indicates a write operation.

Figure 7. Memory Slave Device Address



Addressing Overview

After the FM24V02A (as receiver) acknowledges the slave address, the master can place the memory address on the bus for a write operation. The address requires two bytes. The complete 15-bit address is latched internally. Each access causes the latched address value to be incremented automatically. The current address is the value that is held in the latch; either a newly written value or the address following the last access. The current address will be held for as long as power remains or until a new value is written. Reads always use the current address. A random read address can be loaded by beginning a write operation as explained below.

After transmission of each data byte, just prior to the acknowledge, the FM24V02A increments the internal address latch. This allows the next sequential byte to be accessed with no additional addressing. After the last address (7FFFh) is reached, the address latch will roll over to 0000h. There is no limit to the number of bytes that can be accessed with a single read or write operation.

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Data Transfer

After the address bytes have been transmitted, data transfer between the bus master and the FM24V02A can begin. For a read operation the FM24V02A will place 8 data bits on the bus then wait for an acknowledge from the master. If the acknowledge occurs, the FM24V02A will transfer the next sequential byte. If the acknowledge is not sent, the FM24V02A will end the read operation. For a write operation, the FM24V02A will accept 8 data bits from the master then sends an acknowledge. All data transfer occurs MSB (most significant bit) first.

Memory Operation

The FM24V02A is designed to operate in a manner very similar to other two-wire interface memory products. The major differences result from the higher performance write capability of F-RAM technology. These improvements result in some differences between the FM24V02A and a similar configuration EEPROM during writes. The complete operation for both writes and reads is explained below.

Write Operation

All writes begin with a slave address, then a memory address. The bus master indicates a write operation by setting the LSB of the slave address (R/$\overline{W}$ bit) to a '0'. After addressing, the bus master sends each byte of data to the memory and the memory generates an acknowledge condition. Any number of sequential bytes may be written. If the end of the address range is reached internally, the address counter will wrap from 7FFFh to 0000h.

Unlike other nonvolatile memory technologies, there is no effective write delay with F-RAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory cycle occurs in less time than a single bus clock. Therefore, any operation including read or write can occur immediately following a write. Acknowledge polling, a technique used with EEPROMs to determine if a write is complete is unnecessary and will always return a ready condition.

Internally, an actual memory write occurs after the 8th data bit is transferred. It will be complete before the acknowledge is sent. Therefore, if the user desires to abort a write without altering the memory contents, this should be done using START or STOP condition prior to the 8th data bit. The FM24V02A uses no page buffering.

The memory array can be write-protected using the WP pin. Setting the WP pin to a HIGH condition (V_{DD}) will write-protect all addresses. The FM24V02A will not acknowledge data bytes that are written to protected addresses. In addition, the address counter will not increment if writes are attempted to these addresses. Setting WP to a LOW state (V_{SS}) will disable the write protect. WP is pulled down internally.

Figure 8 and Figure 9 illustrate a single-byte and multiple-byte write cycles in Fast-mode Plus (Fm+). Figure 10 illustrates a single-byte write cycles in Hs mode.

Figure 8. Single-Byte Write

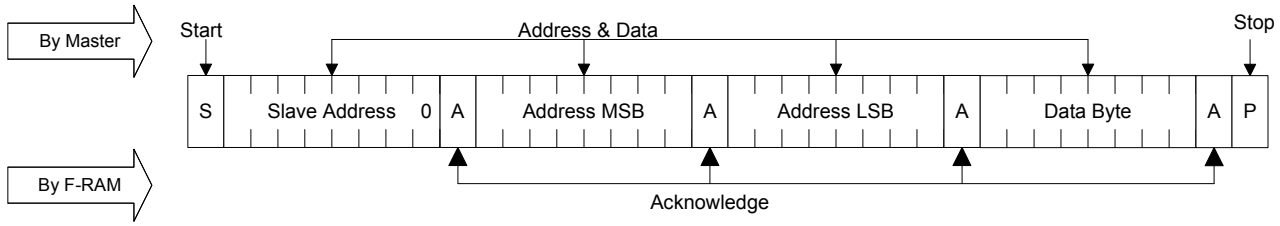
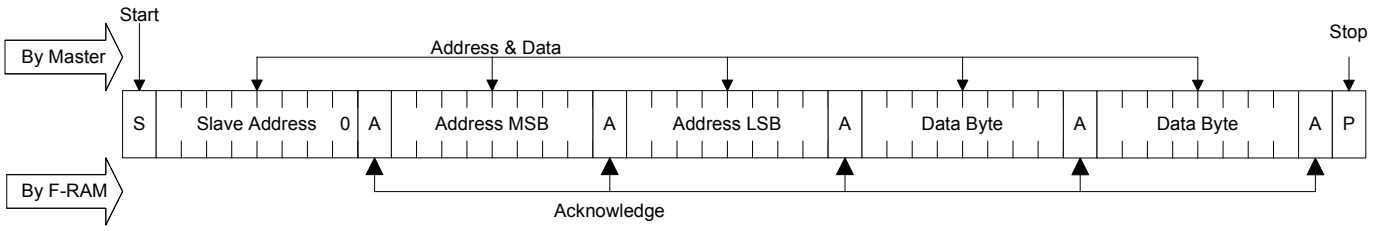
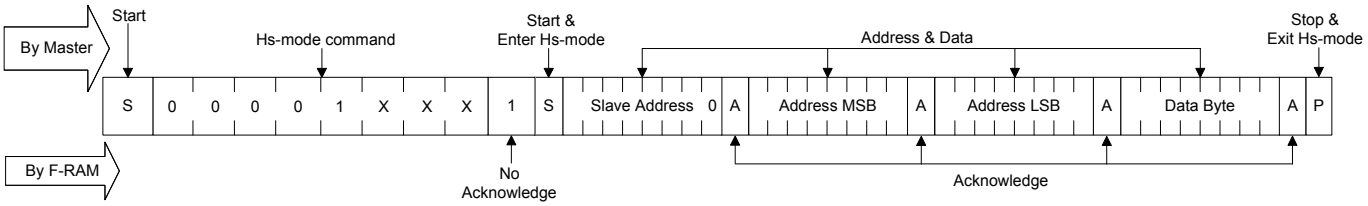


Figure 9. Multi-Byte Write



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Figure 10. Hs-Mode Byte Write



Read Operation

There are two basic types of read operations. They are current address read and selective address read. In a current address read, the FM24V02A uses the internal address latch to supply the address. In a selective read, the user performs a procedure to set the address to a specific value.

Current Address & Sequential Read

As mentioned above the FM24V02A uses an internal latch to supply the address for a read operation. A current address read uses the existing value in the address latch as a starting place for the read operation. The system reads from the address immediately following that of the last operation.

To perform a current address read, the bus master supplies a slave address with the LSB set to a '1'. This indicates that a read operation is requested. After receiving the complete slave address, the FM24V02A will begin shifting out data from the current address on the next clock. The current address is the value held in the internal address latch.

Beginning with the current address, the bus master can read any number of bytes. Thus, a sequential read is simply a current address read with multiple byte transfers. After each byte the internal address counter will be incremented.

Note Each time the bus master acknowledges a byte, this indicates that the FM24V02A should read out the next sequential byte.

There are four ways to properly terminate a read operation. Failing to properly terminate the read will most likely create a bus contention as the FM24V02A attempts to read out additional data onto the bus. The four valid methods are:

1. The bus master issues a no-acknowledge in the 9th clock cycle and a STOP in the 10th clock cycle. This is illustrated in the diagrams below. This is preferred.
2. The bus master issues a no-acknowledge in the 9th clock cycle and a START in the 10th.
3. The bus master issues a STOP in the 9th clock cycle.
4. The bus master issues a START in the 9th clock cycle.

If the internal address reaches 7FFFh, it will wrap around to 0000h on the next read cycle. Figure 11 and Figure 12 show the proper operation for current address reads.

Figure 11. Current Address Read

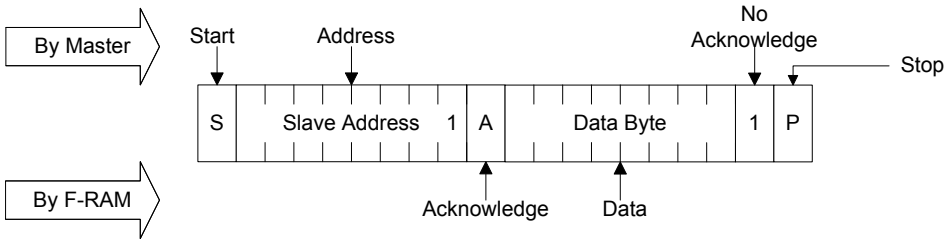
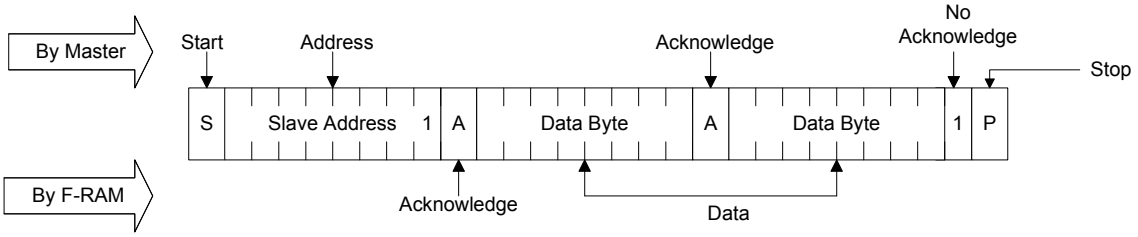
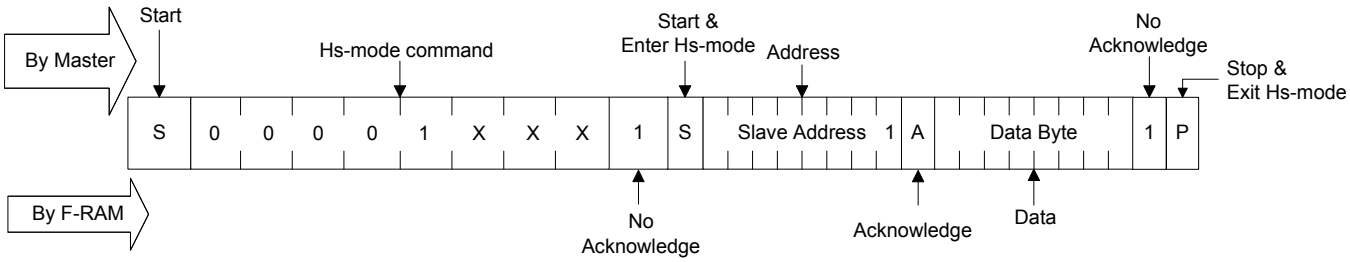


Figure 12. Sequential Read



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Figure 13. Hs-Mode Current Address Read



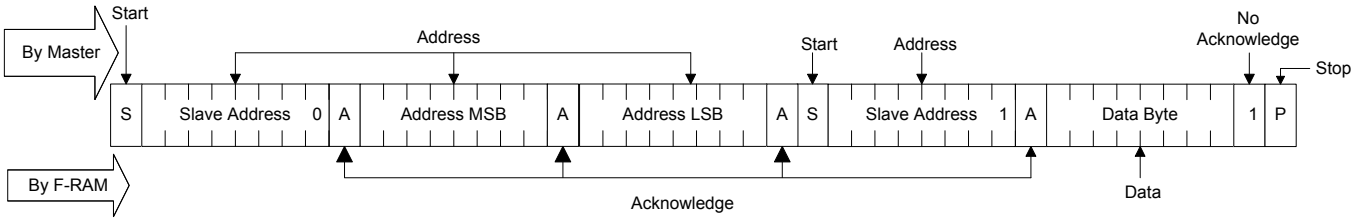
Selective (Random) Read

There is a simple technique that allows a user to select a random address location as the starting point for a read operation. This involves using the first three bytes of a write operation to set the internal address followed by subsequent read operations.

To perform a selective read, the bus master sends out the slave address with the LSB (R/W) set to 0.

This specifies a write operation. According to the write protocol, the bus master then sends the address bytes that are loaded into the internal address latch. After the FM24V02A acknowledges the address, the bus master issues a START condition. This simultaneously aborts the write operation and allows the read command to be issued with the slave address LSB set to a '1'. The operation is now a current address read.

Figure 14. Selective (Random) Read



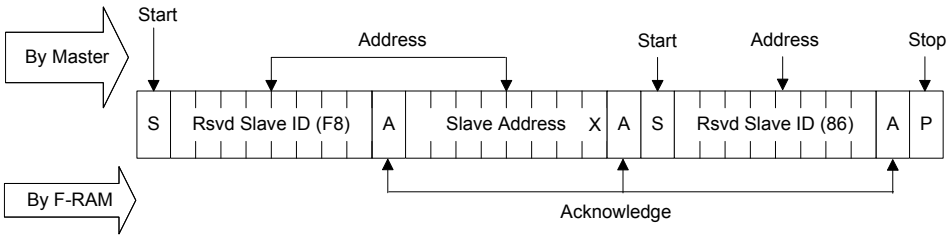
Sleep Mode

A low power mode called Sleep Mode is implemented on the FM24V02A device. The device will enter this low power state when the Sleep command 86h is clocked-in. Sleep Mode entry can be entered as follows:

1. The master sends a START command.
2. The master sends Reserved Slave ID 0xF8.
3. The FM24V02A sends an ACK.
4. The master sends the I^2C-bus slave address of the slave device it needs to identify. The last bit is a 'Don't care' value (R/W bit). Only one device must acknowledge this byte (the one that has the I^2C-bus slave address).
5. The FM24V02A sends an ACK.
6. The master sends a Re-START command.
7. The master sends Reserved Slave ID 0x86.
8. The FM24V02A sends an ACK.
9. The master sends STOP to ensure the device enters sleep mode.

Once in sleep mode, the device draws I_{ZZ} current, but the device continues to monitor the I^2C pins. Once the master sends a Slave Address that the FM24V02A identifies, it will "wakeup" and be ready for normal operation within t_{REC} (400-µs max.). As an alternative method of determining when the device is ready, the master can send read or write commands and look for an ACK. While the device is waking up, it will NACK the master until it is ready.

Figure 15. Sleep Mode Entry



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Device ID

The FM24V02A device incorporates a means of identifying the device by providing three bytes of data, which are manufacturer, product ID, and die revision. The Device ID is read-only. It can be accessed as follows:

1. The master sends a START command.
2. The master sends Reserved Slave ID 0xF8.
3. The FM24V02A sends an ACK.
4. The master sends the I^2C-bus slave address of the slave device it needs to identify. The last bit is a 'Don't care' value (R/W bit). Only one device must acknowledge this byte (the one that has the I^2C-bus slave address).
5. The FM24V02A sends an ACK.
6. The master sends a Re-START command.
7. The master sends Reserved Slave ID 0xF9.
8. The FM24V02A sends an ACK.
9. The Device ID Read can be done, starting with the 12 manufacturer bits, followed by the 9 part identification bits, and then the 3 die revision bits.
10. The master ends the Device ID read sequence by NACKing the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.

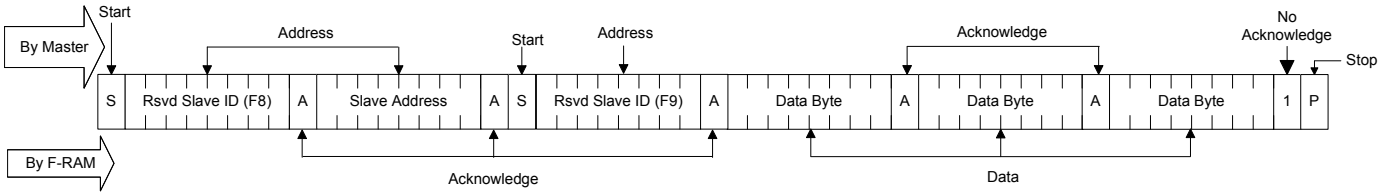
Note The reading of the Device ID can be stopped anytime by sending a NACK command.

Table 1. Device ID

Device ID (3 bytes)	Device ID Description			
	23–12 (12 bits)	11–8 (4 bits)	7–3 (5 bits)	2–0 (3 bits)
	Manufacturer ID	Product ID		
		Density	Variation	Die Rev
004201h	000000000100	0010	00000	001

Note Product ID bits 0 and 4 are reserved.

Figure 16. Read Device ID



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Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –55 °C to +125 °C

Maximum accumulated storage time
At 125 °C ambient temperature ..... 1000 h
At 85 °C ambient temperature ..... 10 Years

Ambient temperature
with power applied ..... –55 °C to +125 °C

Supply voltage on V_{DD} relative to V_{SS} .....–1.0 V to +4.5 V

Input voltage* ..... –1.0 V to + 4.5 V and $V_{IN} < V_{DD} + 1.0$ V

DC voltage applied to outputs
in HI-Z state ..... –0.5 V to V_{DD} + 0.5 V

Transient voltage (< 20 ns) on
any pin to ground potential ..... –2.0 V to V_{DD} + 2.0 V

Package power dissipation
capability (T_A = 25 °C) ..... 1.0 W

Surface mount lead soldering
temperature (3 seconds) ..... +260 °C

Electrostatic discharge voltage
Human Body Model (JEDEC Std JESD22-A114-B) ..... 2 kV

Charged Device Model (JEDEC Std JESD22-C101-A) ..... 500 V

Latch-up current ..... > 140 mA

* Exception: The "$V_{IN} < V_{DD} + 1.0$ V" restriction does not apply to the SCL and SDA inputs.

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}
Industrial	–40 °C to +85 °C	2.0 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [2]	Max	Unit
V_{DD}	Power supply			2.0	3.3	3.6	V
I_{DD}	Average V_{DD} current	SCL toggling between V_{DD} – 0.2 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.2 V.	f_{SCL} = 100 kHz	–	–	175	µA
			f_{SCL} = 1 MHz	–	–	400	µA
			f_{SCL} = 3.4 MHz	–	–	1000	µA
I_{SB}	V_{DD} standby current	SCL = SDA = V_{DD}. All other inputs V_{SS} or V_{DD}. Stop command issued.		–	90	150	µA
I_{ZZ}	Sleep mode current	SCL = SDA = V_{DD}. All other inputs V_{SS} or V_{DD}. Stop command issued.		–	5	8	µA
I_{LI}	Input leakage current (Except WP and A2-A0)	$V_{SS} \le V_{IN} \le V_{DD}$		–1	–	+1	µA
	Input leakage current (for WP and A2-A0)			–1	–	+100	µA
I_{LO}	Output leakage current	$V_{SS} \le V_{OUT} \le V_{DD}$		–1	–	+1	µA
V_{IH}	Input HIGH voltage (SDL, SDA)			0.7 × V_{DD}	–	V_{DD}(max)+ 0.3	V
	Input HIGH voltage (WP, A2-A0)			0.7 × V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage			– 0.3	–	0.3 × V_{DD}	V
V_{OL}[3]	Output LOW voltage	I_{OL} = 3 mA		–	–	0.4	V
		I_{OL} = 6 mA		–	–	0.6	V
R_{in}[4]	Input resistance (WP, A2-A0)	For $V_{IN} = V_{IL(Max)}$		50	–	–	kΩ
		For $V_{IN} = V_{IH(Min)}$		1	–	–	MΩ
V_{hys}[5]	Hysteresis of Schmitt Trigger inputs		f_{SCL} = 100 kHz, 400 kHz, 1 MHz	0.05 × V_{DD}	–	–	V
			f_{SCL} = 3.4 MHz	0.06 × V_{DD}	–	–	V

Notes
2. Typical values are at 25 °C, $V_{DD} = V_{DD}$(typ). Not 100% tested.
3. The FM24V02A does not meet the NXP I²C specification in the Fast-mode Plus (Fm+, 1 MHz) for I_{OL} of 20 mA at a V_{OL} of 0.4 V.
4. The input pull-down circuit is strong (50 kΩ) when the input voltage is below V_{IL} and weak (1 MΩ) when the input voltage is above V_{IH}.
5. The FM24V02A does not meet the NXP I²C specification in the High Speed Mode (Hs-mode, 3.4 MHz) for V_{hys} of 0.1 × V_{DD}.

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Data Retention and Endurance

Parameter	Description	Test condition	Min	Max	Unit
T_{DR}	Data retention	T_A = 85 °C	10	–	Years
		T_A = 75 °C	38	–	
		T_A = 65 °C	151	–	
NV_C	Endurance	Over operating temperature	10^{14}	–	Cycles

Capacitance

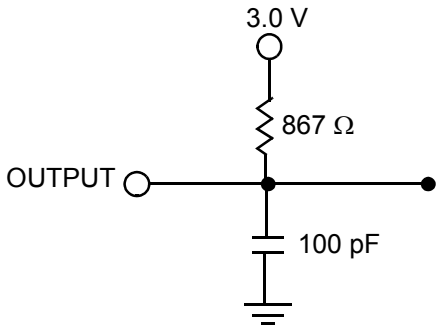
Parameter [6]	Description	Test Conditions	Max	Unit
C_{IO}	Input/Output pin capacitance (SDA)	T_A = 25 °C, f = 1 MHz, V_{DD} = V_{DD}(typ)	8	pF
C_I	Input pin capacitance		6	pF

Thermal Resistance

Parameter [6]	Description	Test Conditions	8-pin SOIC	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	146	°C/W
Θ_{JC}	Thermal resistance (junction to case)		48	°C/W

AC Test Loads and Waveforms

Figure 17. AC Test Loads and Waveforms



AC Test Conditions

Input pulse levels .....10% and 90% of V_{DD}
Input rise and fall times .....10 ns
Input and output timing reference levels .....0.5 × V_{DD}
Output load capacitance ..... 100 pF

Note
6. These parameters are guaranteed by design and are not tested.

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AC Switching Characteristics

Over the Operating Range

Parameter[7]	Alt. Parameter	Description	Fast-Mode Plus (Fm+) [9]		Hs-Mode[9]		Unit
			Min	Max	Min	Max	
f_{SCL}[8]		SCL clock frequency	–	1.0	–	3.4	MHz
$t_{SU;\ STA}$		Start condition setup for repeated Start	260	–	160	–	ns
$t_{HD;STA}$		Start condition hold time	260	–	160	–	ns
t_{LOW}		Clock LOW period	500	–	160	–	ns
t_{HIGH}		Clock HIGH period	260	–	60	–	ns
$t_{SU;DAT}$	$t_{SU;DATA}$	Data in setup	50	–	10	–	ns
$t_{HD;DAT}$	$t_{HD;DATA}$	Data in hold	0	–	0	70	ns
t_{DH}		Data output hold (from SCL at V_{IL})	0	–	0	–	ns
t_R[10]	t_r	Input rise time	–	120	10	80	ns
t_F[10]	t_f	Input fall time	20 * (V_{DD} / 5.5 V)	120	10	80	ns
$t_{SU;STO}$		STOP condition setup	260	–	160	–	ns
t_{AA}	$t_{VD;DATA}$	SCL LOW to SDA Data Out Valid	–	450	–	130	ns
$t_{VD;ACK}$		ACK output valid time	–	450	–	130	ns
t_{OF}[10]		Output fall time from V_{IH} min to V_{IL} max	20 * (V_{DD} / 5.5 V)	120	–	80	ns
t_{BUF}		Bus free before new transmission	500	–	300	–	ns
t_{SP}		Noise suppression time constant on SCL, SDA	0	50	–	5	ns

Figure 18. Read Bus Timing Diagram

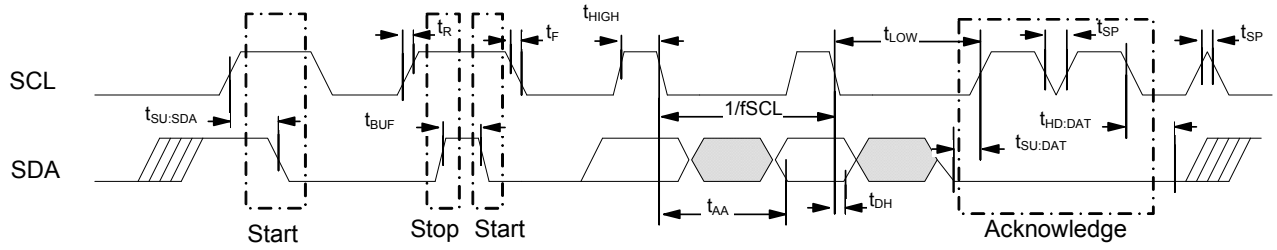
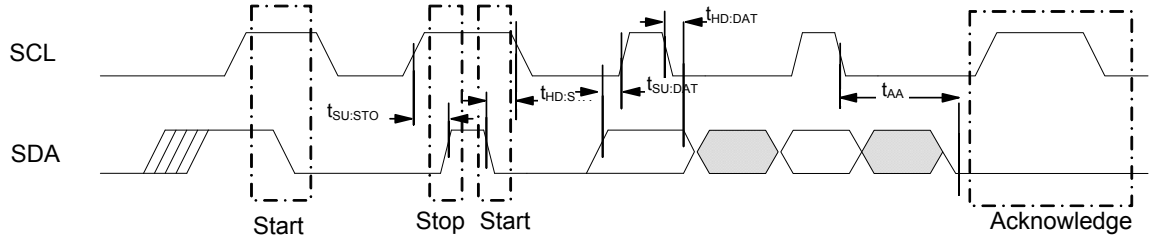


Figure 19. Write Bus Timing Diagram



Notes

7. Test conditions assume signal transition time of 10 ns or less, timing reference levels of V_{DD}/2, input pulse levels of 0 to V_{DD}(typ), and output loading of the specified I_{OL} and 100 pF load capacitance shown in Figure 17.
8. The speed-related specifications are guaranteed characteristic points along a continuous curve of operation from DC to f_{SCL}(max).
9. Bus Load (Cb) considerations; Cb < 550 pF for I^2C clock frequency (SCL) 1 MHz; Cb < 100 pF for SCL at 3.4 MHz.
10. These parameters are guaranteed by design and are not tested.

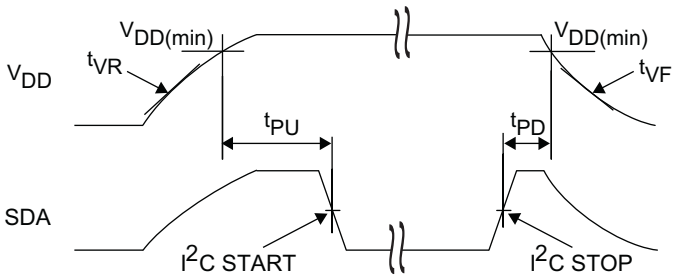
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Power Cycle Timing

Over the Operating Range

Parameter	Description	Min	Max	Unit
t_{PU}	Power-up V_{DD}(min) to first access (START condition)	250	–	µs
t_{PD}	Last access (STOP condition) to power-down (V_{DD}(min))	0	–	µs
t_{VR} [11, 12]	V_{DD} power-up ramp rate	50	–	µs/V
t_{VF} [11, 12]	V_{DD} power-down ramp rate	100	–	µs/V
t_{REC}	Recovery time from sleep mode	–	400	µs

Figure 20. Power Cycle Timing



Notes
11. Slope measured at any point on the V_{DD} waveform.
12. These parameters are guaranteed by design and are not tested.

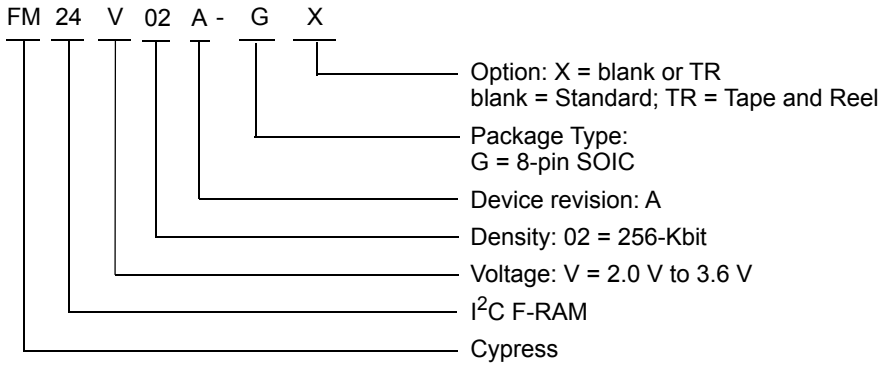
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Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
FM24V02A-G	51-85066	8-pin SOIC	Industrial
FM24V02A-GTR	51-85066	8-pin SOIC	

All these parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

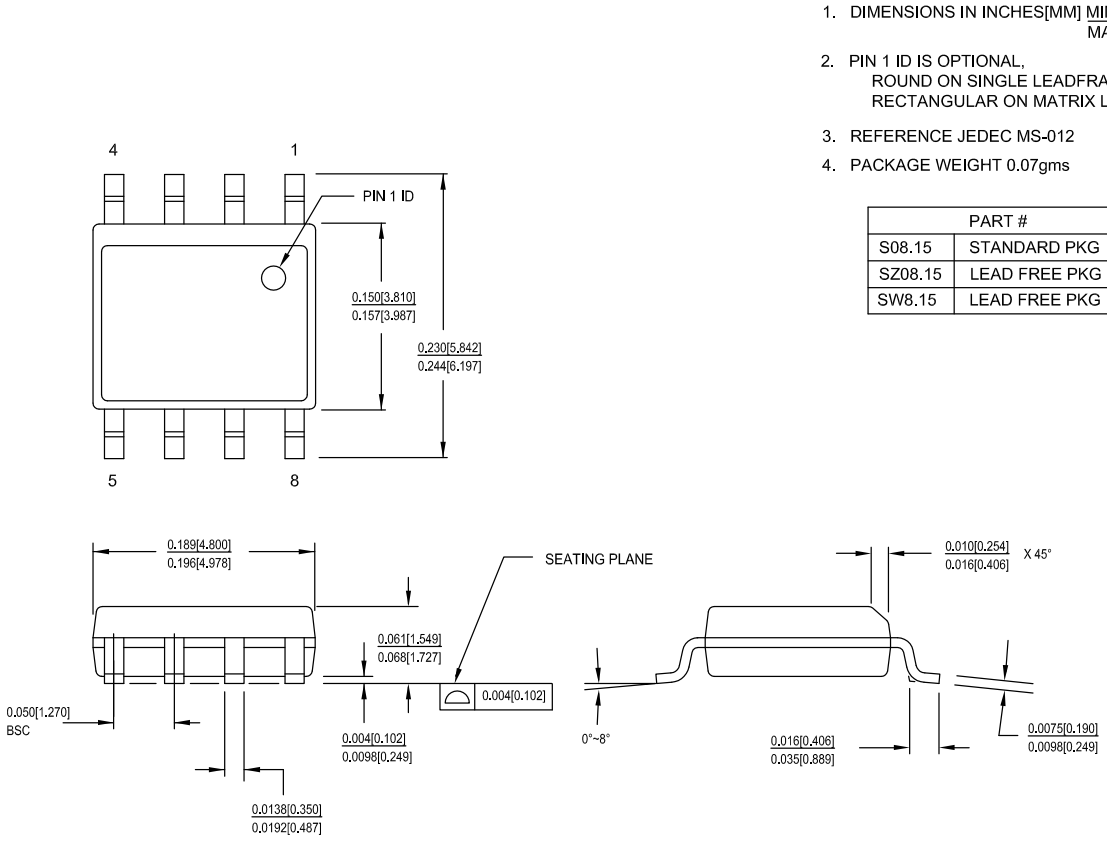
Ordering Code Definitions



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Package Diagram

Figure 21. 8-pin SOIC (150 Mils) Package Outline, 51-85066



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Acronyms

Acronym	Description
ACK	Acknowledge
CMOS	Complementary Metal Oxide Semiconductor
EIA	Electronic Industries Alliance
I^2C	Inter-Integrated Circuit
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
LSB	Least Significant Bit
MSB	Most Significant Bit
NACK	No Acknowledge
RoHS	Restriction of Hazardous Substances
R/$\overline{W}$	Read/Write
SCL	Serial Clock Line
SDA	Serial Data Access
SOIC	Small Outline Integrated Circuit
WP	Write Protect

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
Kb	1024 bit
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
µA	microampere
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

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Document History Page

Document Title: FM24V02A, 256-Kbit (32K × 8) Serial (I^2C) F-RAM Document Number: 001-90839				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4266205	GVCH	01/29/2014	New data sheet.
*A	4390913	GVCH	06/20/2014	Changed status from Advance to Preliminary. Maximum Ratings: Electrostatic Discharge Voltage Removed machine model. DC Electrical Characteristics: Added I_{SB} and I_{ZZ} typical value. Changed V_{IH} value from V_{DD}+ 0.5 V to V_{DD}(max) + 0.3 V for SDA, SCL and V_{DD}(max) + 0.3 V for WP, A2-A0. Removed V_{OL2} parameter spec and renamed V_{OL1} as V_{OL} parameter spec. Added V_{OL} = 0.6 V at 6 mA. Changed V_{IL} min value from – 0.5 V to – 0.3 V. Added V_{hys} parameter spec. Updated Capacitance. AC Switching Characteristics: Added t_{OF}, t_{BUF}, t_{AA}, $t_{VD;ACK}$ value for 3.4 MHz. Removed footnote 7.
*B	4512788	GVCH	09/24/2014	Added footnote 3 for the difference in I_{OL} with respect to I^2C specification.
*C	4571858	GVCH	11/18/2014	Changed V_{hys} spec value from 0.1 × V_{DD} to 0.05 × V_{DD} for 3.4 MHz frequency. Added footnote 5 for the difference in V_{hys} with respect to I^2C specification.
*D	4596783	GVCH	12/17/2014	Added footnote 1 for the difference in I_{OL} and V_{hys} with respect to NXP I^2C specification. Two-wire Interface: Added description for the difference in I_{OL} and V_{hys} with respect to NXP I^2C specification. Changed V_{hys} spec value from 0.05 × V_{DD} to 0.06 × V_{DD} for 3.4 MHz frequency Updated footnote 3. Updated footnote 5 for the difference in V_{hys} with respect to NXP I^2C specification. Updated to new template.
*E	4651363	ZSK	02/10/2015	Changed status from Preliminary to Final. Updated Functional Description: Added “For a complete list of related resources, click here.” at the end. Updated Package Diagram: spec 51-85066 – Changed revision from *F to *G.
*F	4874478	ZSK / PSR	08/06/2015	Updated Maximum Ratings: Removed “Maximum junction temperature”. Added “Maximum accumulated storage time”. Added “Ambient temperature with power applied”.
*G	5085665	GVCH	01/14/2016	Updated Ordering Information: Updated part numbers. Updated Package Diagram: spec 51-85066 – Changed revision from *G to *H.
*H	5452467	ZSK	09/28/2016	Updated Power Cycle Timing: Changed minimum value of t_{PU} parameter from 1 ms to 250 µs. Updated to new template.
*I	5734131	AESATMP7	05/11/2017	Updated Cypress Logo and Copyright.

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