# FORESEE®

# Industrial eMMC Datasheet

A-00140

FEMDRM0xxG-A3A55

Version 1.0

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# 1 INTRODUCTION

FORESEE eMMC is an embedded storage solution designed in the BGA package. The FORESEE eMMC consists of NAND flash and eMMC controller. The controller could manage the interface protocols, wear-leveling, bad block management and ECC.
FORESEE eMMC has high performance at a competitive cost, high quality and low power consumption, and eMMC is compatible with JEDEC standard eMMC 5.1 specifications.

# 2 PRODUCT LIST

**Table 1. Product List**

| Capacity | Part Number | NAND Flash Type | User Density | Package Size(mm) | Package Type |
|---|---|---|---|---|---|
| 32GB | FEMDRM032G-A3A55 | 256Gb x1 | 28.8GB | 11.5×13.0×1.0 | 153 FBGA |
| 64GB | FEMDRM064G-A3A55 | 256Gb x2 | 57.6GB | 11.5×13.0×1.0 | 153 FBGA |

# 3 KEY FEATURES

- **eMMC5.1 specification compatibility**
  - Backward compatible to eMMC4.41/4.5/5.0

- **Bus mode**
  - Data bus width: 1 bit (default), 4 bits, 8 bits
  - Data transfer rate: up to 400MB/s (HS400)
  - MMC I/F Clock frequency: 0~200MHz

- **Operating voltage range**
  - $V_{CC}$(NAND): 2.7 ~ 3.6V
  - $V_{CCQ}$(Controller): 1.7 ~ 1.95V / 2.7 ~ 3.6V

- **Temperature**
  - Operation: -25℃ ~ +85℃
  - Storage without operation: -40℃ ~ +85℃

- **Sudden-Power-Loss safeguard**
- **Hardware ECC engine**
- **Unique firmware backup mechanism**
- **Global-wear-leveling**
- **Supported features.**
  - HS400, HS200
  - Partitioning, RPMB
  - Boot feature, boot partition
  - HW Reset/SW Reset
  - Discard, Trim, Erase, Sanitize
  - Background operations, HPI
  - Enhanced reliable write
  - S.M.A.R.T. Health Report
  - FFU
  - Sleep / awake

- **Others**
  - Compliance with the RoHS Directive



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# 4 PACKAGE CONFIGURATIONS

## 4.1 Ball Pin Configuration

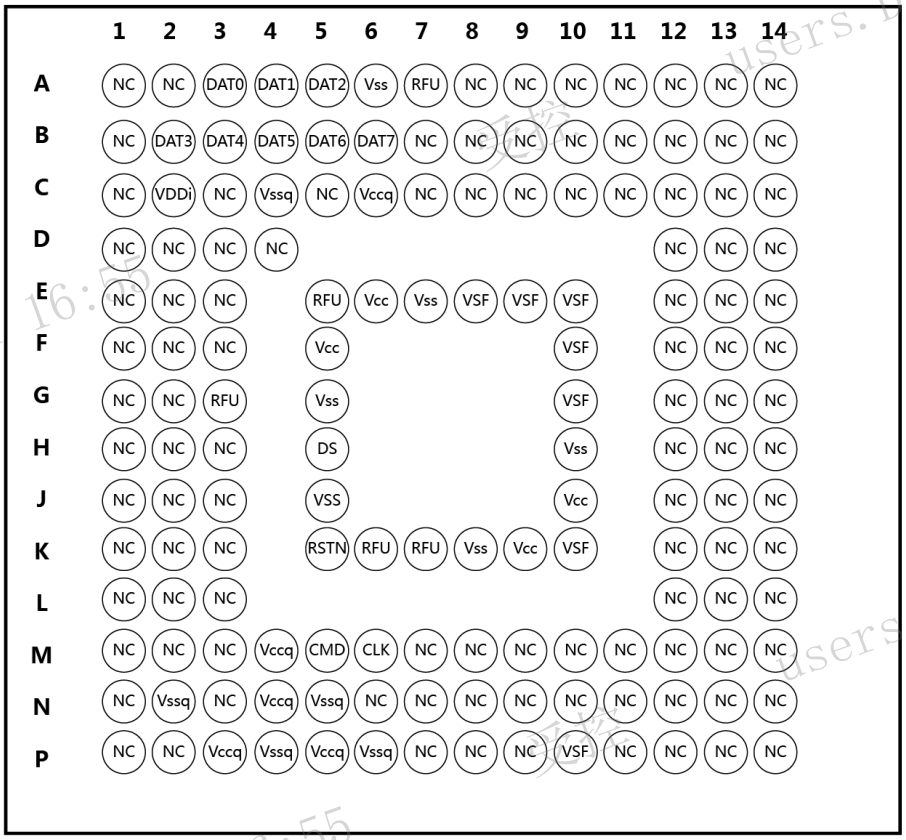



**Figure 1. Ball Array (Top View through package)**

**Table 2. Ball Array Description**

| Pin No. | Pin Name | Description |
|---|---|---|
| A3 | DAT0 | These are bidirectional data signal. The DAT signals operate in push-pull mode. Only the device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the eMMC host controller. The eMMC device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode the device disconnects the internal pull-ups of lines DAT1–DAT7 |
| A4 | DAT1 | |
| A5 | DAT2 | |
| B2 | DAT3 | |
| B3 | DAT4 | |
| B4 | DAT5 | |
| B5 | DAT6 | |
| B6 | DAT7 | |
| K5 | RSTN | Hardware Reset Input |



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| Pin No. | Pin Name | Description |
|---|---|---|
| C6 | VCCQ | VCCQ is the power supply line for host interface, have two power mode: High power mode:2.7V~3.6V; Lower power mode:1.7V~1.95V. |
| M4 | VCCQ | |
| N4 | VCCQ | |
| P3 | VCCQ | |
| P5 | VCCQ | |
| E6 | VCC | VCC is the power supply line for internal flash memory, its power voltage range is:2.7V~3.6V. |
| F5 | VCC | |
| J10 | VCC | |
| K9 | VCC | |
| C2 | VDDi | VDDi is internal power node, not the power supply. Connect 1uF capacitor VDDi to ground. |
| M5 | CMD | This signal is a bidirectional command channel used for device initialization and command transfer. Commands are sent from the host to the device, and responses are sent from the device to the host. The CMD Signal has 2 operation modes: open drain for initialization, and push-pull for command transfer. |
| H5 | DS | Data Strobe signal. Newly assigned pin for HS400 mode. Data Strobe is generated from e·MMC to host. In HS400 mode, read data and CRC response are synchronized with Data Strobe. |
| M6 | CLK | Each cycle of this signal directs a one-bit transfer on the command and either a one-bit (1x) or a two-bits transfer (2x) on all the data lines. |
| J5 | VSS | Ground connections |
| A6 | VSS | |
| C4 | VSS | |
| E7 | VSS | |
| G5 | VSS | |
| H10 | VSS | |
| K8 | VSS | |
| N2 | VSS | |
| N5 | VSS | |
| P4 | VSS | |
| P6 | VSS | |

**Note:**

NC: No Connect, shall be connected to ground or left floating.

RFU: Reserved for Future Use, must be left floating for future use.

VSF: Vendor Specific Function, must be left floating.



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## 4.2 Package Dimension

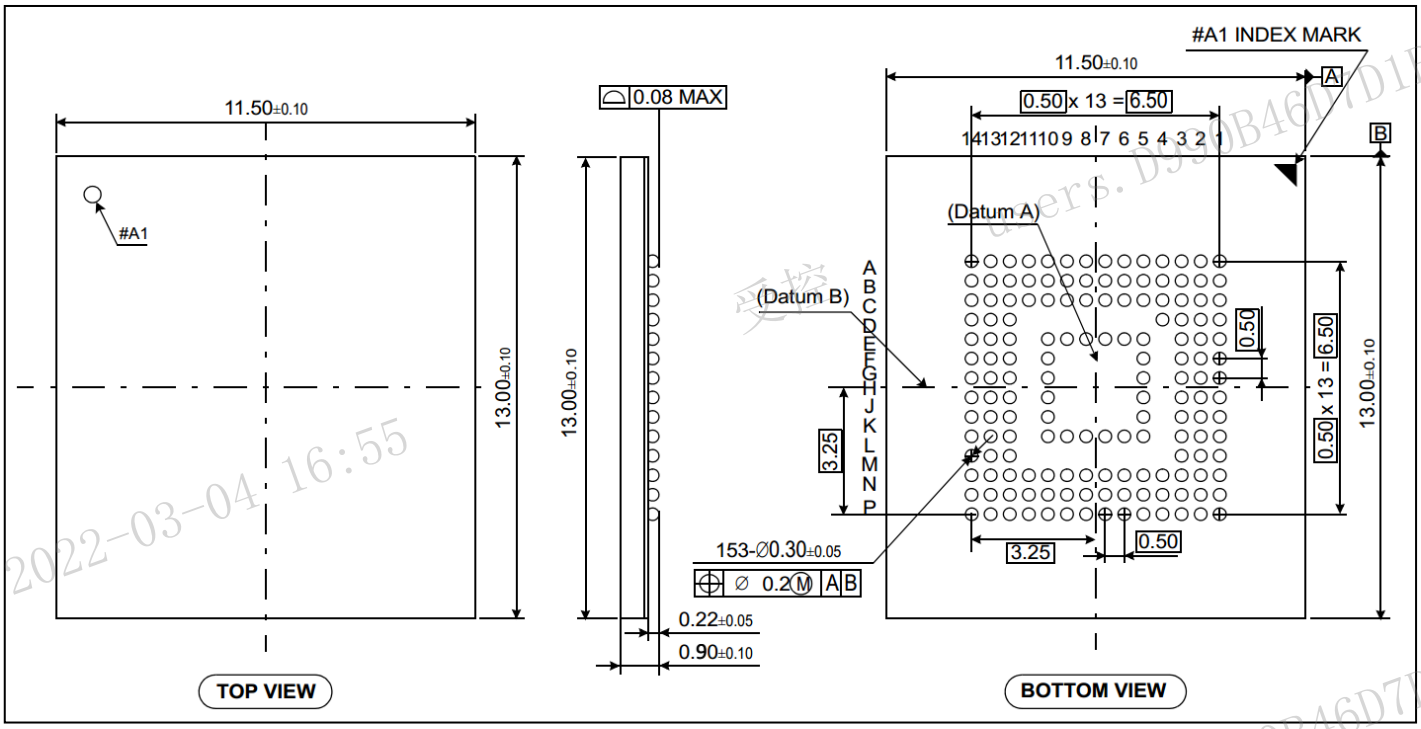



**Figure 2. 11.5mm x 13.0mm x 1.0mm Package Dimension**

# 5 PRODUCT SPECIFICATIONS

## 5.1 Write/Read Performance

**Table 3. Write/Read Performance**

| Part Number | Write | Read |
|---|---|---|
| FEMDRM032G-A3A55 | Up to 150 MB/s | Up to300 MB/s |
| FEMDRM064G-A3A55 | Up to 200 MB/s | Up to300 MB/s |

Note:

Test Condition: Bus width x8, 200MHz DDR, 512KB data transfer, w/o file system overhead, measured on internal board.

Test tool: uBOOT (Without O/S)

Chunk size: 1MB

Test area: 100MB/ Full-range of LBA.



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## 5.2 Power Consumption

### 5.2.1 Active Power Consumption During Operation

**Table 4. Active Power Consumption During Operation**

| Part Number | $I_{CC}$ | $I_{CCQ}$ |
|---|---|---|
| FEMDRM032G-A3A55 | 100mA | 150mA |
| FEMDRM064G-A3A55 | 120mA | 150mA |

Note:

Power Measurement conditions: Bus configuration =x8 @200MHz DDR, 23℃.

VCC = 3.3V & VCCQ = 1.8V.

The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

### 5.2.2 Low power mode (stand-by)

**Table 5. Low power mode (stand-by)**

| Part Number | $I_{CC}$ | $I_{CCQ}$ |
|---|---|---|
| FEMDRM032G-A3A55 | 100uA | 150uA |
| FEMDRM064G-A3A55 | 120uA | 150uA |

Note:

Power Measurement conditions: Bus configuration =x8 @200MHz DDR, 23℃.

Standby: NAND Flash VCC & Controller VCCQ power supply is switched on.

The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

### 5.2.3 Low power mode (sleep)

**Table 6. Low power mode (sleep)**

| Part Number | $I_{CC}$ | $I_{CCQ}$ |
|---|---|---|
| FEMDRM032G-A3A55 | 0 | 150uA |
| FEMDRM064G-A3A55 | 0 | 170uA |

Note:

Power Measurement conditions: Bus configuration =x8 @200MHz DDR, 23℃.

Sleep: NAND Flash VCC power supply is switched off (Controller VCCQ on)

The measurement for max RMS current is the average RMS current consumption over a period of 100ms.



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# 6 Technical Notes

## 6.1 Functional Description

FORESEE eMMC with powerful L2P (Logical to Physical) NAND Flash management algorithm provides unique functions:

- **Host independence from details of operating NAND flash**
  The eMMC Controller already includes Flash management technologies such as data storage and retrieval, defect handling and diagnostics, and power management. Host can be free from considering about NAND Flash data operating.

- **Internal ECC to correct defect in NAND flash**
  The hardware error correction code (ECC) function, which can prevent data corruption data corruption is included in the eMMC controller.

- **Sudden-Power-Loss Safeguard**
  To prevent from data loss, a mechanism named Sudden-Power-Loss Safeguard is added in the eMMC. In the case of sudden power-failure, the eMMC would work properly after power cycling.

- **Global-wear-leveling**
  To achieve the best stability and device endurance, this eMMC equips the Global Wear Leveling algorithm. It ensures that not only normal area, but also the frequently accessed area, such as FAT, would be programmed and erased evenly.

- **IDA (Initial Data Acceleration)**
  The eMMC prevents the pre-burned data from data-loss with IDA, in case of our customer had pre-burned data to eMMC, before the eMMC being SMT.

- **Cache**
  The eMMC enhanced the data written performance with Cache, with which our customer would get more endurance and reliability.

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## 6.2 Interface timing mode

FORESEE eMMC support supports high speed DDR interface timing mode up to 400MB/s at 200MHz with 1.8V I/O supply.

**Table 7. Device Type Value (EXT_CSD register : DEVICE_TYPE [196])**

| Bit | Device Type | Supportability |
|---|---|---|
| 7 | HS400 Dual Data Rate eMMC at 200 MHz – 1.2 V I/O | Not support |
| 6 | HS400 Dual Data Rate eMMC at 200 MHz – 1.8 V I/O | Support |
| 5 | HS200 Single Data Rate eMMC at 200 MHz - 1.2 V I/O | Not support |
| 4 | HS200 Single Data Rate eMMC at 200 MHz - 1.8 V I/O | Support |
| 3 | High-Speed Dual Data Rate eMMC at 52 MHz - 1.2 V I/O | Not support |
| 2 | High-Speed Dual Data Rate eMMC at 52 MHz - 1.8 V or 3.3 V I/O | Support |
| 1 | High-Speed eMMC at 52 MHz - at rated device voltage(s) | Support |
| 0 | High-Speed eMMC at 26 MHz - at rated device voltage(s) | Support |

## 6.3 System Architecture

The eMMC can be operated in 1-bit, 4-bit, or 8-bit mode. NAND flash memory is managed by a controller inside, which manages ECC, wear leveling and bad block management. The eMMC provides easy integration with the host process that all flash management hassles are invisible to the host.

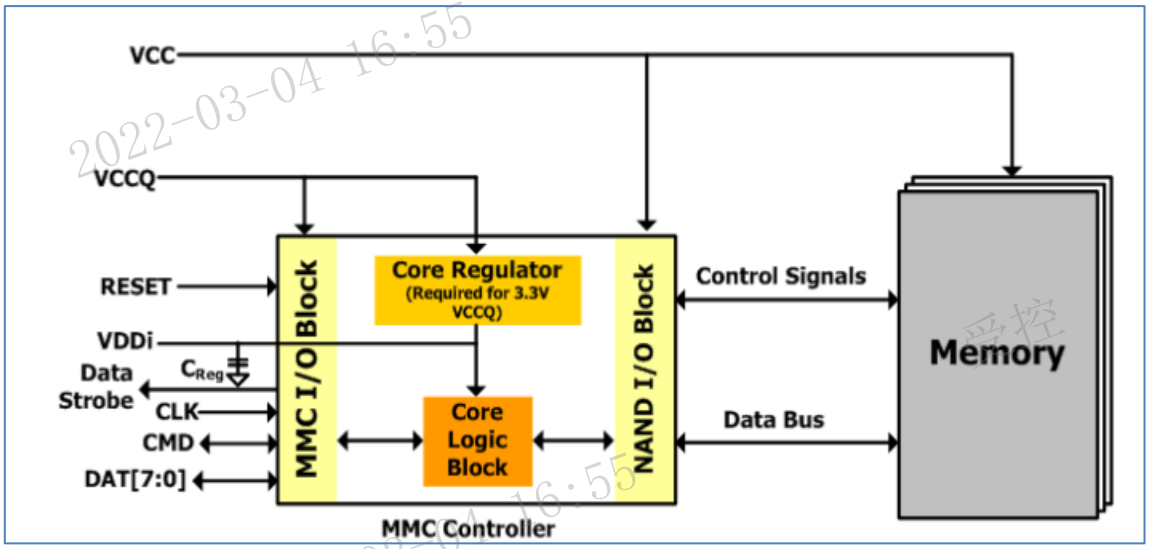



**Figure 3. eMMC System Architecture**



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## 6.4 Partition Management

The embedded device offers also the possibility of configuring by the host additional split local memory partitions with independent addressable space starting from logical address 0x00000000 for different usage models. Default size of each Boot Area Partition is 4096 KB and can be changed by Vendor Command as multiple of 128KB. Boot area partition size is calculated as (128KB * BOOT_SIZE_MULTI) The size of Boot Area Partition 1 and 2 cannot be set independently and is set as same value Boot area partition which is enhanced partition. Therefore, memory block area scan is classified as follows:

- **Factory configuration supplies boot partitions.**
- **The RPMB partition is 4MB.**
- **The host is free to configure one segment in the User Data Area to be implemented as enhanced storage media, and to specify its starting location and size in terms of Write Protect Groups. The attributes of this Enhanced User Data Area can be programmed only once during the device life-cycle (one-time programmable).**
- **Up to four General Purpose Area Partitions can be configured to store user data or sensitive data, or for other host usage models. The size of these partitions is a multiple of the write protect group. Size and attributes can be programmed once in device life-cycle (one-time programmable). Each of the General-Purpose Area Partitions can be implemented with enhanced technological features.**

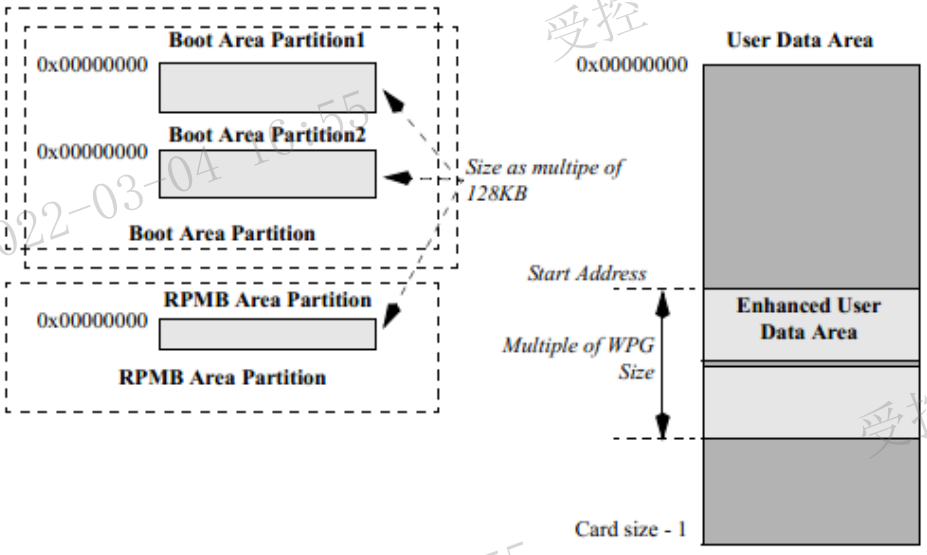



**Figure 4. Partitions and user data area configuration**



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In boot operation mode, the master can read boot data from the slave (device) by keeping CMD line low or sending CMD0 with argument + 0xFFFFFFFA, before issuing CMD1. The data can be read from either boot area or user area depending on register setting.

**Table 8. Boot ack, boot data and initialization Time**

| Timing Factor | Value |
|---|---|
| Boot ACK Time | < 50 ms |
| Boot Data Time | < 1 s |
| Initialization Time | < 1 s |

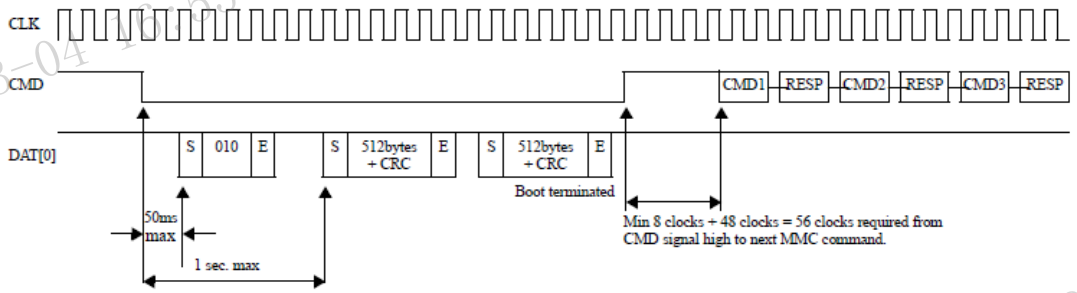



**Figure 5. State diagram (boot mode)**

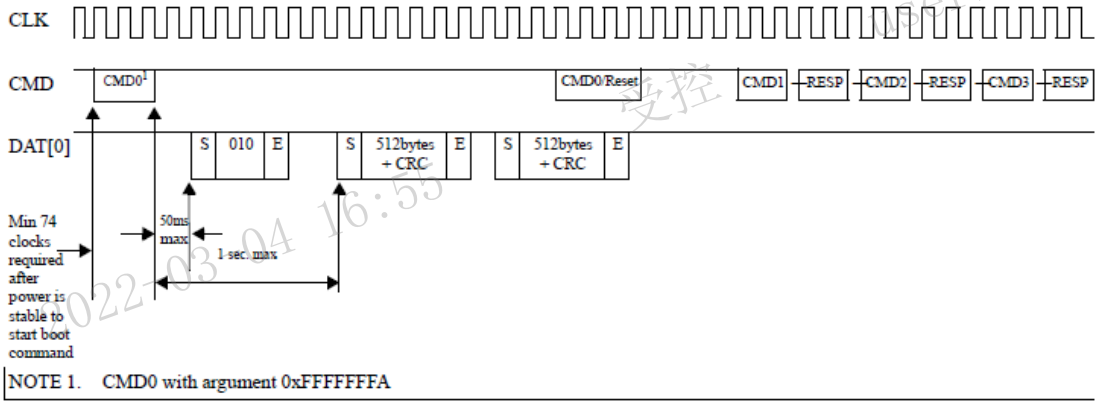



**Figure 6. State diagram (alternative boot mode)**



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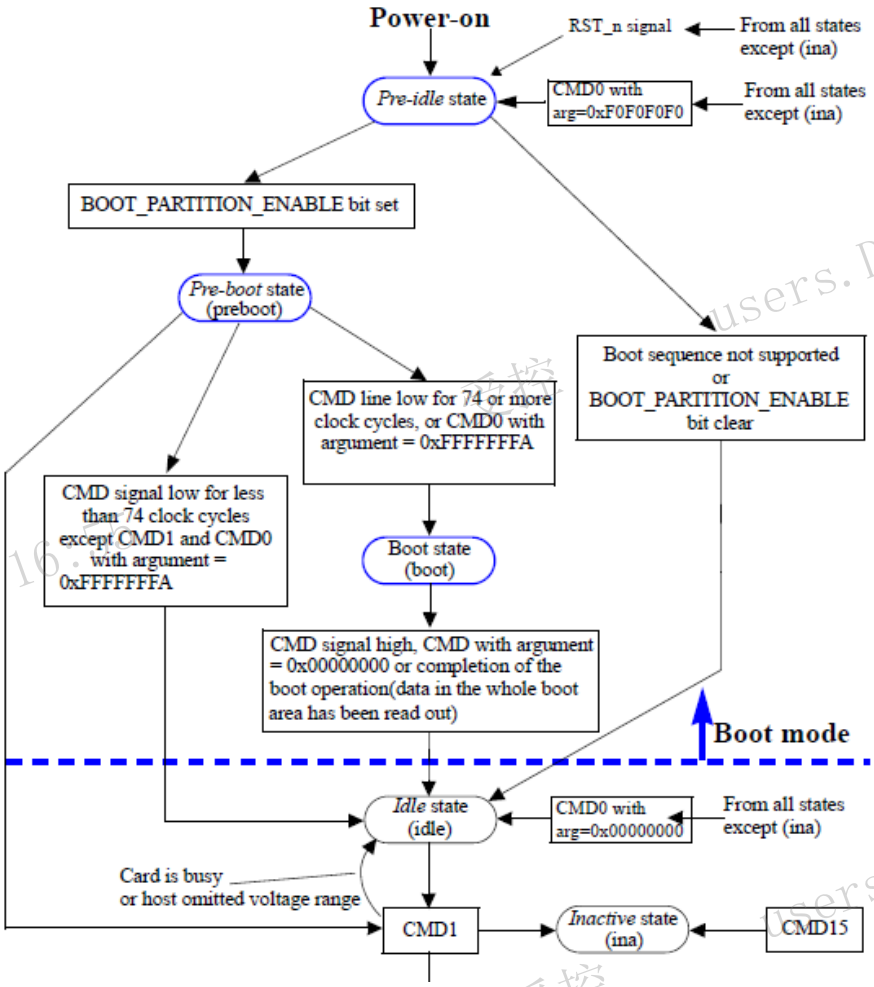



**Figure 7. State diagram (boot mode) ***

## 6.5 Automatic Sleep Mode

If host does not issue any command during certain duration **(1s)**, after previously issued command is completed, the device enters “Power Saving mode” to reduce power consumption. At this time, commands arriving at the device while it is in power saving mode will be serviced in normal fashion. The below table explains the condition to enter and exit Auto Power Saving Mode



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## 6.6 Sleep (CMD5)

A card may be switched between a Sleep state and a Standby state by SLEEP/AWAKE (CMD5). In the Sleep state the power consumption of the memory device is minimized. In this state the memory device reacts only to the commands RESET (CMD0 with argument of either 0x00000000 or 0xF0F0F0F0 or H/W reset) and SLEEP/AWAKE (CMD5). All the other commands are ignored by the memory device. The timeout for state transitions between Standby state and Sleep state is defined in the EXT_CSD register S_A_timeout. The maximum current consumptions during the Sleep state are defined in the EXT_CSD registers S_A_VCC and S_A_VCCQ. Sleep command: The bit 15 as set to 1 in SLEEP/ AWAKE (CMD5) argument. A wake command: The bit 15 as set to 0 in SLEEP/AWAKE (CMD5) argument.

## 6.7 H/W Reset operation

Device will detect the rising edge of RST_n signal to trigger internal reset sequence

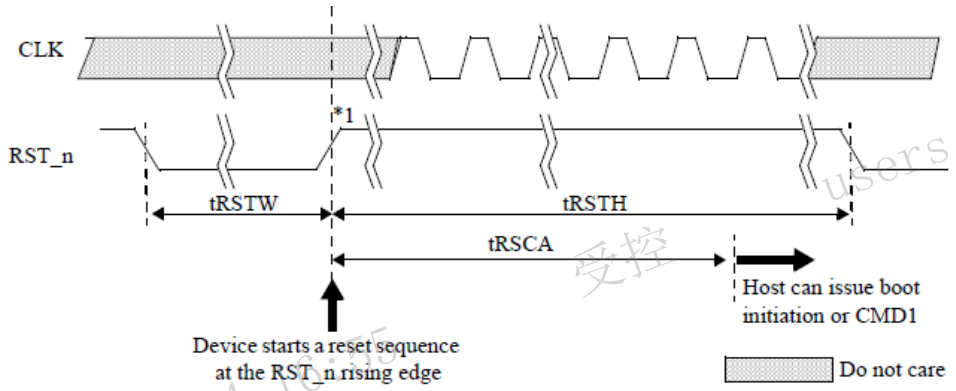



**Figure 8. H/W reset waveform**

## 6.8 Initial Data Acceleration(IDA)

In the case of pre-burn before SMT, it is recommended to limit the size of data pre-burned to the eMMC, please contact your agency for more information.

- **The amount of data pre-burned (data written before SMT) is limited, it should be managed properly.**
- **Maximum size for the data-written to IDA:**

**Table 9. IDA Maximum Size**

| Part Number | Size limited for Pre-burned Data |
|---|---|
| FEMDRM032G-A3A55 | 9.5GB |
| FEMDRM064G-A3A55 | 18.5GB |



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## 6.9 High-speed mode selection

After the host verifies that the card complies with version 4.0, or higher, of this standard, it has to enable the high-speed mode timing in the card, before changing the clock frequency to a frequency higher than 20MHz. For the host to change to a higher clock frequency, it has to enable the high-speed interface timing. The host uses the SWITCH command to write 0x01 to the HS_TIMING byte, in the Modes segment of the EXT_CSD register.

## 6.10 Bus width selection

After the host has verified the functional pins on the bus it should change the bus width configuration accordingly, using the SWITCH command. The bus width configuration is changed by writing to the BUS_WIDTH byte in the Modes Segment of the EXT_CSD register (using the SWITCH command to do so). After power-on, or software reset, the contents of the BUS_WIDTH byte is 0x00.

## 6.11 Partition Configuration

**Table 10. Partition Configuration**

| Model | Area/Partition | Size (GB) | Size (MB) | Size (Sector) | Size (Byte) | Size (Hex, Byte) |
|---|---|---|---|---|---|---|
| FEMDRM032G-A3A55 | User | 28.8GB | 29600 | 60620800 | 31037849600 | 73A000000 |
| | Boot Partition 1 | - | 4 | 8192 | 4194304 | 400000 |
| | Boot Partition 2 | - | 4 | 8192 | 4194304 | 400000 |
| | RPMB | - | 4 | 8192 | 4194304 | 400000 |
| FEMDRM064G-A3A55 | User | 57.6GB | 59000 | 120832000 | 61865984000 | E67800000 |
| | Boot Partition 1 | - | 4 | 8192 | 4194304 | 400000 |
| | Boot Partition 2 | - | 4 | 8192 | 4194304 | 400000 |
| | RPMB | - | 4 | 8192 | 4194304 | 400000 |



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## 6.12 Reference Schematics

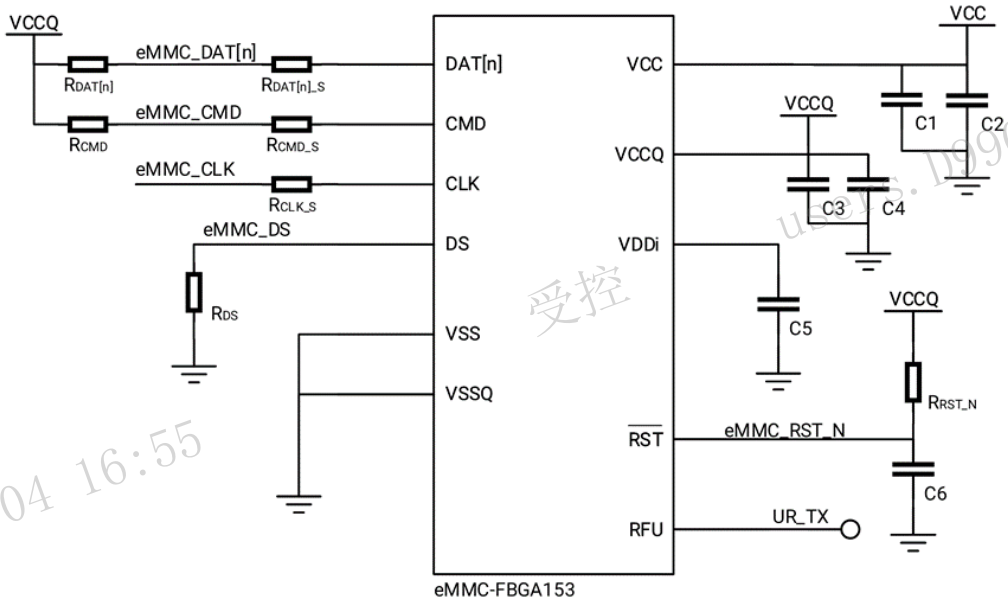



**Figure 9. eMMC Reference Schematics**

**Table 11. Reference component parameter**

| Parameter | Symbol | Min | Typical | Max | Remark |
|---|---|---|---|---|---|
| Power of VCC | VCC | 2.7V | 3.3V | 3.6V | Should be separated from VCCQ |
| Power of VCCQ (High Perf.) | VCCQ | 1.7V | 1.8V | 1.95V | HS200/HS400 |
| Power of VCCQ (Low Perf.) | VCCQ | 2.7V | 3.3V | 3.6V | 52MHz CLK SDR/DDR |
| DAT[n] Pull-Up Resistance | $R_{DAT[n]}$ | 10kΩ | -- | 100kΩ | DAT[n], n=0~7 |
| CMD Pull-Up Resistance | $R_{CMD}$ | 4.7kΩ | -- | 100kΩ | |
| DS Pull-Down Resistance | $R_{DS}$ | 10kΩ | -- | 100kΩ | HS200/HS400 |
| RST_N Pull-Up Resistance | $R_{RST_N}$ | -- | NC | -- | Reserving for EVT |
| DAT[n] Serial Resistance | $R_{DAT[n]_S}$ | -- | 0Ω | 33Ω | Reserving for EVT |
| CMD Serial Resistance | $R_{CMD_S}$ | -- | 0Ω | 33Ω | Reserving for EVT |
| CLK Serial Resistance | $R_{CLK_S}$ | -- | 0Ω | 33Ω | Reserving for EVT |
| Power Coupling Capacitor 1 | C1, C3 | 2.2μF | -- | 4.7μF | 6.3V, X5R or higher classification |
| Power Coupling Capacitor 2 | C2, C4 | -- | 0.1μF | -- | 6.3V, X5R or higher classification |
| VDDi Coupling Capacitor | C5 | 0.1μF | 1μF | -- | 6.3V, X5R or higher classification |
| RST_N Coupling Capacitor | C6 | -- | NC | -- | 6.3V, X5R or higher classification |

Design note:

1. Coupling capacitor should be connected with VCC/VCCQ and VSS as closely as possible.
3. The VCC and VCCQ power should be separated.
4. LONGSYS recommends lay the VSS between the CLK and the Data lines.
5. For more details, please contact your technical support.



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# 7 REGISTER VALUE

## 7.1 CID register

The Card Identification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase (protocol). Every individual flash or I/O card shall have a unique identification number. Every type of ROM card (defined by content) shall have a unique identification number. The structure of the CID register is defined in the following sections.

**Table 12. CID register**

| Name | | Field | Width | CID-slice | CID Value | Remark |
|---|---|---|---|---|---|---|
| Manufacturer ID | | MID | 8 | [127:120] | D6h | |
| Reserved | | - | 6 | [119:114] | -- | |
| Card/BGA | | CBX | 2 | [113:112] | 01h | BGA |
| OEM/Application ID | | OID | 8 | [111:104] | 03h | |
| Product name | FEMDRM032G-A3A55 | PNM | 48 | [103:56] | 0x413341353542 | A3A55B |
| | FEMDRM064G-A3A55 | | | | 0x413341353543 | A3A55C |
| Product revision | | PRV | 8 | [55:48] | -- | |
| Product serial number | | PSN | 32 | [47:16] | -- | Not Fixed |
| Manufacturing date | | MDT | 8 | [15:8] | -- | Not Fixed |
| CRC7 checksum | | CRC | 7 | [7:1] | -- | Not Fixed |
| Not used, always '1' | | - | 1 | [0:0] | -- | |



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## 7.2 CSD register

The Card-Specific Data (CSD) register provides information on how to access the card contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the CSD Registry entries coded as follows:

**Table 13. CSD Register**

| Name | Field | Width | Cell Type | CSD-slice |
|---|---|---|---|---|
| CSD structure | CSD_STRUCTURE | 2 | R | [127:126] |
| System specification version | SPEC_VERS | 4 | R | [125:122] |
| Reserved | - | 2 | R | [121:120] |
| Data read access-time 1 | TAAC | 8 | R | [119:112] |
| Data read access-time 2 in CLK cycles (NSAC*100) | NSAC | 8 | R | [111:104] |
| Max. bus clock frequency | TRAN_SPEED | 8 | R | [103:96] |
| Card command classes | CCC | 12 | R | [95:84] |
| Max. read data block length | READ_BL_LEN | 4 | R | [83:80] |
| Partial blocks for read allowed | READ_BL_PARTIAL | 1 | R | [79:79] |
| Write block misalignment | WRITE_BLK_MISALIGN | 1 | R | [78:78] |
| Read block misalignment | READ_BLK_MISALIGN | 1 | R | [77:77] |
| DSR implemented | DSR_IMP | 1 | R | [76:76] |
| Reserved | - | 2 | R | [75:74] |
| Device size | C_SIZE | 12 | R | [73:62] |
| Max. read current @$V_{DD}$ min | VDD_R_CURR_MIN | 3 | R | [61:59] |
| Max. read current @$V_{DD}$ max | VDD_R_CURR_MAX | 3 | R | [58:56] |
| Max. write current @$V_{DD}$ min | VDD_W_CURR_MIN | 3 | R | [55:53] |
| Max. write current @$V_{DD}$ max | VDD_W_CURR_MAX | 3 | R | [52:50] |
| Device size multiplier | C_SIZE_MULT | 3 | R | [49:47] |
| Erase group size | ERASE_GRP_SIZE | 5 | R | [46:42] |
| Erase group size multiplier | ERASE_GRP_MULT | 5 | R | [41:37] |



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| Name | Field | Width | Cell Type | CSD-slice |
|---|---|---|---|---|
| Write protect group size | WP_GRP_SIZE | 5 | R | [36:32] |
| Write protect group enable | WP_GRP_MULT | 1 | R | [31:31] |
| Manufacturer default ECC | DEFAULT_ECC | 2 | R | [30:29] |
| Write speed factor | R2W_FACTOR | 3 | R | [28:26] |
| Max. write data block length | WRITE_BL_LEN | 4 | R | [25:22] |
| Partial blocks for write allowed | WRITE_BL_PARTIAL | 1 | R | [21:21] |
| Reserved | - | 4 | R | [20:17] |
| Content protection application | CONTENT_PROT_APP | 1 | R | [16:16] |
| File format group | FILE_FORMAT_GRP | 1 | R/W | [15:15] |
| Copy flag (OTP) | COPY | 1 | R/W | [14:14] |
| Permanent write protection | PERM_WRITE_PROTECT | 1 | R/W | [13:13] |
| Temporary write protection | TMP_WRITE_PROTECT | 1 | R/W/E | [12:12] |
| File format | FILE_FORMAT | 2 | R/W | [11:10] |
| ECC code | ECC | 2 | R/W/E | [9:8] |
| CRC | CRC | 7 | R/W/E | [7:1] |
| Not used, always '1' | - | 1 | - | [0:0] |

2022-03-04 16:55
受控
users.D990B46D7D1B4EAC



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## 7.3 Extended CSD register

The Extended CSD register defines the card properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the card capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the card is working in. These modes can be changed by the host by means of the SWITCH command.

**Table 14. Extended CSD Register**

| Name | Field | Size | Type | Slice[bytes] | Value |
|---|---|---|---|---|---|
| Reserved* | | 6 | - | [511:506] | - |
| Extended security error | EXT_SECURITU_ERR | 1 | R | [505] | 0 |
| Supported Command Sets | S_CMD_SET | 1 | R | [504] | 1h |
| HPI Features | HPI_FEATURES | 1 | R | [503] | 1h |
| Background operations support[1] | BKOPS_SUPPORT | 1 | R | [502] | 1h |
| Max packed read command | MAX_PACKED_READS | 1 | R | [501] | 3Fh |
| Max packed write command | MAX_PACKED_WRITES | 1 | R | [500] | 3Fh |
| Data Tag Support | DATA_TAD_SUPPORT | 1 | R | [499] | 1h |
| Tag Unit Size | TAG_UNIT_SIZE | 1 | R | [498] | 3h |
| Tag Resource Size | TAG_RES_SIZE | 1 | R | [497] | 0h |
| Context management capabilities | CONTEXT_CAPABITILITIES | 1 | R | [496] | 5h |
| Large Unit size[2] | LARGE_UNIT_SIZE_M1 | 1 | R | [495] | 7h |
| Extended partitions attribute support | EXT_SUPPORT | 1 | R | [494] | 3h |
| Supported modes | SUPPORTED_MODES | 1 | R | [493] | 3h |
| FFU features | FFU_FEATURES | 1 | R | [492] | 0h |
| Operation codes timeout | OPERATION_CODE_TIMEOUT | 1 | R | [491] | 0h |
| FFU Argument | FFU_ARG | 4 | R | [490:487] | 0h |
| Barrier support | BARRIER_SUPPORT | 1 | R | [486] | 0h |
| Reserved* | | 177 | - | [485:309] | - |

1 BKOPS supported.
2 Large Unit size 8MB.



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| Name | Field | Size | Type | Slice[bytes] | Value |
|---|---|---|---|---|---|
| CMDQ support | CMDQ_SUPPORT | 1 | W/R | [308] | 1h |
| CMDQ depth | CMDQ_DEPTH | 1 | W/R | [307] | 1Fh |
| Reserved* | | 1 | - | [306] | - |
| Number of received sectors | NUMBER_OF_RECEIVED_SECTORS | 4 | R | [305:302] | 0h |
| Vendor proprietary health report | VENDOR_PROPRIETARY_HEALTH_REPORT | 1 | R | [301:270] | 0h |
| Device life time estimation type B | DEVICE_LIFE_TIME_EST_TYP_B | 1 | R | [269] | 0h |
| Device life time estimation type A | DEVICE_LIFE_TIME_EST_TYP_A | 1 | R | [268] | - |
| Pre EOL information | PRE_EOL_INFO | 1 | R | [267] | 1h |
| Optimal read size | OPTIMAL_READ_SIZE | 1 | R | [266] | 0h |
| Optimal write size | OPTIMAL_WRITE _SIZE | 1 | R | [265] | 20h |
| Optimal trim unit size | OPTIMAL_TRIM_UNIT_SIZE | 1 | R | [264] | 1h |
| Device version | DEVICE_VERSION | 2 | R | [263:262] | 0h |
| Firmware version[3] | FIRMWARE_VERSION | 8 | R | [261:254] | - |
| Power class for200MHz，DDR at VCC=3.6V | PWR_CL_DDR_200_360 | 1 | R | [253] | 0h |
| Cache size | CACHE_SIZE | 4 | R | [252:249] | 10000h |
| Generic CMD6 timeout[4] | GENERIC_CMD6_TIME | 1 | R | [248] | Ah |
| Power-off notification(long) timeout[5] | POWER_OFF_LONG_TIME | 1 | R | [247] | 3Ch |
| Background operations status[6] | BKOPS_STATUS | 1 | R | [246] | 0h |
| Number of correctly programmed sectors | CORRECTLY_PRG_SECTORS_NUM | 4 | R | [245:242] | - |
| First Initialization time after partitioning[7] | INI_TIMEOUT_AP | 1 | R | [241] | 1Eh |
| Cache Flushing Policy | CACHE_FLUSH_POLICY | 1 | R | [240] | 0h |
| Power class for 52Mhz, DDR at 3.6V[8] | PWR_CL_DDR_52_360 | 1 | R | [239] | 0h |

3 FW Patch Ver.
4 Generic CMD6 timeout 100ms.
5 Power off notification(long) timeout 600ms.
6 No operations required.
7 Initial time out 3s.
8 RMS 100 mA, peak 200 mA.



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| Name | Field | Size | Type | Slice[bytes] | Value |
|---|---|---|---|---|---|
| Power class for 52Mhz, DDR at 1.95V[9] | PWR_CL_DDR_52_195 | 1 | R | [238] | 0h |
| Power class for 200Mhz at VCCQ=1.95V，VCC=3.6V | PWR_CL_200_195 | 1 | R | [237] | 0h |
| Power class for 200Mhz at VCCQ=1.3V，VCC=3.6V | PWR_CL_200_360 | 1 | R | [236] | 0h |
| Minimum write performance for 8bit at 52MHz in DDR mode[10] | MIN_PERF_DDR_W_8_52 | 1 | R | [235] | 0h |
| Minimum read performance for 8bit at 52MHz in DDR mode[11] | MIN_PERF_DDR_R_8_52 | 1 | R | [234] | 0h |
| Reserved* | | 1 | - | [233] | - |
| TRIM Multiplier[12] | TRIM_MULT | 1 | R | [232] | 5h |
| Secure feature support[13] | SEC_FEATURE_SUPPORT | 1 | R | [231] | 55h |
| Secure Erase Multiplier[14] | SEC_ERASE_MULT | 1 | R | [230] | 1Bh |
| Secure TRIM Multiplier[15] | SEC_TRIM_MULT | 1 | R | [229] | 11h |
| Boot Information[16] | BOOT_INFO | 1 | R | [228] | 7h |
| Reserved* | | 1 | - | [227] | - |
| Boot partition size[17] | BOOT_SIZE_MULTI | 1 | R | [226] | 20h |
| Access size[18] | ACC_SIZE | 1 | R | [225] | 6h |
| High-capacity Erase unit size[19] | HC_ERASE_GROUP_SIZE | 1 | R | [224] | 1h |
| High-capacity Erase time out[20] | ERASE_TIMEOU_MULT | 1 | R | [223] | 5h |
| Reliable write sector count[21] | REL_WR_SEC_C | 1 | R | [222] | 1h |

9 RMS 65 mA, peak 130 mA.
10 For cards not reaching the 4.8MB/s value. Only support SDR.
11 For cards not reaching the 4.8MB/s value.
12 Trim time out 1.5s.
13 a) Support the secure and insecure trim operations.
b) Support the automatic secure purge operation on retired defective portions of the array.
c) Secure purge operations are supported.
d) Support the sanitize operation.
14 secure erase time out 40.5s.
15 secure trim time out 25.5s.
16 a) Support high speed timing boot.
b) Support dual data rate during boot.
c) Support alternative boot method.
17 Boot partition 4096KB.
18 Super page 16KB.
19 High-capacity erase group size 512KB.
20 High-capacity erase time out 1.5s.
21 1 sector.



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| Name | Field | Size | Type | Slice[bytes] | Value |
|---|---|---|---|---|---|
| High-capacity write protect group size[22] | HC_WP_GRP_SIZE | 1 | R | [221] | 8h |
| Sleep current (VCC)[23] | S_C_VCC | 1 | R | [220] | 7h |
| Sleep current [VCCQ][24] | S_C_VCCQ | 1 | R | [219] | 7h |
| Production state awareness timeout[25] | PRODUCTION_STATE_AWARENESS_TIMEOUT | 1 | R | [218] | 0h |
| Sleep/Awake time out[26] | S_A_TIMEOUT | 1 | R | [217] | 16h |
| Sleep Notification Time out[27] | SLEEP_NOTIFICATION_TIME | 1 | R | [216] | 10h |
| Sector count[28] | SEC_COUNT | 4 | R | [215:212] | depend on density |
| Secure Write Protection Mode | SECURE_WP_INFO | 1 | | [211] | 1h |
| Minimum Write Performance for 8bit @52MHz | MIN_PERF_W_8_52 | 1 | R | [210] | 0h |
| Minimum Read Performance for 8bit @52MHz | MIN_PERF_R_8_52 | 1 | R | [209] | 0h |
| Minimum Write Performance for 4bit @52MHz or 8bit @26MHz | MIN_PERF_W_8_26_4_52 | 1 | R | [208] | 0h |
| Minimum Read Performance for 4bit @52MHz or 8bit @26MHz | MIN_PERF_R_8_26_4_52 | 1 | R | [207] | 0h |
| Minimum Write Performance for 4bit @26MHz | MIN_PERF_W_4_26 | 1 | R | [206] | 0h |
| Minimum Read Performance for 4bit @26MHz | MIN_PERF_R_4_26 | 1 | R | [205] | 0h |
| Reserved* | | 1 | - | [204] | - |
| Power Class for 26MHz @3.6V[29] | PWR_CL_26_360 | 1 | R | [203] | 0h |
| Power Class for 52MHz @3.6V[30] | PWR_CL_52_360 | 1 | R | [202] | 0h |

22 High-capacity wp group size 4096KB.
23 RMS 128μA.
24 RMS 128μA.
25 Not defined.
26 Sleep/Awake timeout 419.43ms.
27 Sleep Notification Time out 655.36ms.
28 Depend on density.
29 RMS 100 mA, peak 200 mA.
30 RMS 100 mA, peak 200 mA.



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| Name | Field | Size | Type | Slice[bytes] | Value |
|---|---|---|---|---|---|
| Power Class for 26MHz @1.95V[31] | PWR_CL_26_195 | 1 | R | [201] | 0h |
| Power Class for 52MHz @1.95V[32] | PWR_CL_52_195 | 1 | R | [200] | 0h |
| Partition switching timing[33] | PARTITION_SWITCH_TIME | 1 | R | [199] | Ah |
| Out-of-interrupt busy timing[34] | OUT_OF_INTERRUPT_TIME | 1 | R | [198] | 5h |
| I/O Driver Strength | DRIVER_STRENGTH | 1 | R | [197] | 1Fh |
| Card Type[35] | CARD_TYPE | 1 | R | [196] | 57h |
| | Reserved* | 1 | - | [195] | - |
| CSD Structure Version[36] | CSD_STRUCTURE | 1 | R | [194] | 2h |
| | Reserved* | 1 | - | [193] | - |
| Extended CSD Revision[37] | EXT_CSD_REV | 1 | R | [192] | 8h |
| Command Set | CMD_SET | 1 | R/W/E_P | [191] | 0h |
| | Reserved* | 1 | - | [190] | - |
| Command set revision | CMD_SET_REV | 1 | R | [189] | 0h |
| | Reserved* | 1 | - | [188] | - |
| Power class | POWER_CLASS | 1 | R/W/E_P | [187] | Bh |
| | Reserved* | 1 | - | [186] | - |
| High Speed Interface Timing | HS_TIMING | 1 | R/W/E_P | [185] | 3h |
| Strobe Support | STROBE_SUPPORT | 1 | R | [184] | 1h |
| Bus Width Mode | BUS_WIDTH | 1 | W/E_P | [183] | 6h |
| | Reserved* | 1 | - | [182] | - |
| Erased memory range | ERASE_MEM_CONT | 1 | R | [181] | 0h |
| | Reserved* | 1 | - | [180] | - |
| Partition Configuration | PARTITION_CONFIG | 1 | R/W/E, R/W/E_P | [179] | 0h |

31 RMS 65 mA, peak 130 mA.
32 RMS 65 mA, peak 130 mA.
33 Partition switch time out 100ms.
34 HPI time out 50ms.
35 HS400 DDR eMMC@200Mhz-1.8V I/O.
36 CSD version No. 1.2.
37 Revision 1.8 (for MMC v5.1).



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| Name | Field | Size | Type | Slice[bytes] | Value |
|---|---|---|---|---|---|
| Boot config protection | BOOT_CONFIG_PROT | 1 | R/W, R/W/C_P | [178] | 0h |
| Boot bus width1 | BOOT_BUS_WIDTH | 1 | R/W/E | [177] | 0h |
| Reserved* | | 1 | - | [176] | - |
| High-density erase group definition | ERASE_GROUP_DEF | 1 | R/W/E_P | [175] | 0h |
| Boot write protection status registers | BOOT_WP_STATUS | 1 | R | [174] | 0h |
| Boot area write protect register | BOOT_WP | 1 | R/W, R/W/C_P | [173] | 0h |
| Reserved* | | 1 | - | [172] | - |
| User area write protect register | USER_WP | 1 | R/W, R/W/C_P, R/W/E_P | [171] | 0h |
| Reserved* | | 1 | - | [170] | - |
| FW Configuration | FW_CONFIG | 1 | R/W | [169] | 0h |
| RPMB Size[38] | RPMB_SIZE_MULT | 1 | R | [168] | 20h |
| Write reliability setting register | WR_REL_SET | 1 | R/W | [167] | 1Fh |
| Write reliability parameter register[39] | WR_REL_PARAM | 1 | R | [166] | 15h |
| Start Sanitize operation | SANITIZE_START | 1 | W/E_P | [165] | 0h |
| Manually start background operations | BKOPS_START | 1 | W/E_P | [164] | 0h |
| Enable background operations handshake | BKOPS_EN | 1 | R/W | [163] | 0h |
| H/W reset function | RST_n_FUNCTION | 1 | R/W | [162] | 0h |
| HPI management | HPI_MGMT | 1 | R/W/E_P | [161] | 0h |
| Partitioning support[40] | PARTITIONING_SUPPORT | 1 | R | [160] | 7h |
| Max Enhanced Area Size | MAX_ENH_SIZE_MULT | 3 | R | [159:157] | - |
| Partitions attribute | PARTITIONS_ATTRIBUTE | 1 | R/W | [156] | 0h |
| Partitions setting | PARTITIONS_SETTING_COMPLETED | 1 | R/W | [155] | 0h |

38 RPMB size is 4MB.
39 Support the enhanced definition of reliable write.
40 a) Enhanced technological features in partitions and user data area.
b) Device supports partitioning features
c) Device can have extended partition attribute.



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| Name | Field | Size | Type | Slice[bytes] | Value |
|---|---|---|---|---|---|
| General Purpose Partition Size | GP_SIZE_MULT | 12 | R/W | [154:143] | 0h |
| Enhanced User Data Area Size | ENH_SIZE_MULT | 3 | R/W | [142:140] | 0h |
| Enhanced User Data Start Address | ENH_START_ADDR | 4 | R/W | [139:136] | 0h |
| Reserved* | | 1 | - | [135] | - |
| Secure Bad Block Management Mode | SEC_BAD_BLK_MGMNT | 1 | R/W | [134] | 0h |
| Production state awareness | PRODUCTION_STATE_AWARENESS | 1 | R/W/E | [133] | 0h |
| Package Case Temperature is controlled | TCASE_SUPPORT | 1 | W/E_P | [132] | 0h |
| Periodic Wake-up | PERIODIC_WAKEUP | 1 | R/W/E | [131] | 0h |
| Program CID/CSD in DDR mode support | PROGRAM_CID_CSD_DDR_SUPPORT | 1 | R | [130] | 1h |
| Reserved* | | 2 | - | [129:128] | - |
| Vendor specific field | VENDOR_SPECIFIC_FIELD | 64 | <vendor specific> | [127:64] | 0h |
| Native sector size | NATIVE_SECTOR_SIZE | 1 | R | [63] | 0h |
| Sector size emulation | USE_NATIVE_SECTOR | 1 | R/W | [62] | 0h |
| Sector size | DATA_SECTOR_SIZE | 1 | R | [61] | 0h |
| 1st initialization after disabling sector size emulation | INI_TIMEOUT_EMU | 1 | R | [60] | 0h |
| Class 6 commands control | CLASS_6_CTRL | 1 | R/W/E_P | [59] | 0h |
| Number of addressed groups to be Released | DYNCAP_NEEDED | 1 | R | [58] | 0h |
| Exception events control | EXCEPTION_EVENTS_CTRL | 2 | R/W/E_P | [57:56] | 0h |
| Exception events status | EXCEPTION_EVENTS_STATUS | 2 | R | [55:54] | 0h |
| Extended Partitions Attribute | EXT_PARTITIONS_ATTRIBUTE | 2 | R/W | [53:52] | 0h |
| Context configuration | CONTEXT_CONF | 15 | R/W/E_P | [51:37] | 0h |
| Packed command status | PACKED_COMMAND_STATUS | 1 | R | [36] | 0h |
| Packed command failure index | PACKED_FAILURE_INDEX | 1 | R | [35] | 0h |
| Power Off Notification | POWER_OFF_NOTIFICATION | 1 | R/W/E_P | [34] | 0h |
| Control to turn the Cache ON/OFF | ON/OFF CACHE_CTRL | 1 | R/W/E_P | [33] | 0h |



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| Name | Field | Size | Type | Slice[bytes] | Value |
|---|---|---|---|---|---|
| Flushing of the cache | FLUSH_CACHE | 1 | W/E_P | [32] | 0h |
| Control to turn the Barrier ON/OFF | ON/OFF BARRIER_CTRL | 1 | R/W | [31] | 0h |
| Mode config | MODE_CONFIG | 1 | R/W/E_P | [30] | 0h |
| Mode operation codes | MODE_OPERATION_CODES | 1 | W/E_P | [29] | 0h |
| Reserved* | | 2 | - | [28:27] | - |
| FFU status | FFU_STATUS | 1 | R | [26] | 0h |
| Pre loading data size | PRE_LOADING_DATA_SIZE | 4 | R/W/E_P | [25:22] | 0h |
| Max pre loading data size | MAX_PRE_LOADING_DATA_SIZE | 4 | R | [21:18] | - |
| Product state awareness enablement | PRODUCT_STATE_AWARENESS_ENABLEMENT | 1 | R/W/E, R | [17] | 0h |
| Secure Removal Type | SECURE_REMOVAL_TYPE | 1 | R/W, R | [16] | 9h |
| Command Queue Mode Enable | CMDQ_MODE_EN | 1 | R/W/E_P | [15] | 0h |
| Reserved* | | 15 | - | [14:0] | - |

Note:

1 Type:

R: Read only

W: One time programmable and NOT readable.

R/W: One time programmable and readable.

R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.

R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.

R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.

2 Reserved*: Reserved bits should be read as 0.



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## 7.4 OCR Register

The 32-bit operation conditions register stores the VCCQ voltage profile of the eMMC. In addition, this register includes a status information bit. This status bit is set if the eMMC power up procedure has been finished. The OCR register shall be implemented by eMMC.

**Table 15. OCR register**

| OCR bit | VCCQ voltage window | eMMC |
|---|---|---|
| [6:0] | Reserved | 000 0000b |
| [7] | 1.7–1.95 | 1b |
| [14:8] | 2.0–2.6 | 000 0000b |
| [23:15] | 2.7–3.6 | 1 1111 1111b |
| [28:24] | Reserved | 000 0000b |
| [30:29] | Access Mode | 00b (byte mode)/10b (sector mode) |
| [31] | power up status bit (busy)* | |

Note:

This bit is set to LOW if the eMMC has not finished the power up routine. The supported voltage range is coded as shown in table.



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## 7.5 Field firmware update(FFU)

To download a new firmware, the controller requires instruction sequence following JEDEC standard. Longsys eMMC only supports Manual mode (MODE_OPERATION_CODES is not supported). For more details, refer to the App note.

### 7.5.1 Longsys eMMC (FEMDRM0xxG-A3A55) Field F/W update flow - CMD sequence

**Table 16. FFU Command Sequence**

| Operation | CMD | Remark |
|---|---|---|
| Set block length 512B | CMD16, arg: 0x00000200 | |
| Enter FFU mode | CMD6, arg: 0x031E0100 | |
| Send FW to device (Download) | CMD25, arg: 0x00000000 | Sending CMD25 is followed by sending FW data, the whole data should be sent by one CMD25 |
| CMD12: Stop | CMD12, arg: 0x00000000 | |
| CMD6: Exit FFU mode | CMD6, arg: 0x031E0000 | |
| HW Reset/Power cycle | | CMD0 Reset is not support |
| Re-Init to trans state | CMD0, CMD1 ... | |
| Check if FFU is succeeded | CMD8, arg: 0x00000000 | Check EXT_CSD [26]: FFU_SUCCESS<br>If FFU_SUCCESS is 0, FFU is succeeded, otherwise FFU is failed.<br>Do not verify data with CMD17/CMD18 while FFU mode. |

### 7.5.2 SUPPORTED_MODE [493] (Read Only)

BIT [0]: '0' FFU is not supported by the device.
'1' FFU is supported by the device.
BIT [1]: '0' Vendor specific mode (VSM) is not supported by the device.
'1' Vendor specific mode is supported by the device.

**Table 17. FFU Supported Mode Register**

| Bit | Field | Supportability |
|---|---|---|
| BIT [7:2] | Reserved | - |
| BIT [1] | VSM | Not support |
| BIT [0] | FFU | Support |



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### 7.5.3 FFU_FEATURE [492] (Read Only)

BIT [0]: '0' Device does not support MODE_OPERATION_CODES field (Manual mode).
'1' Device supports MODE_OPERATION_CODES field (Auto mode).

**Table 18. FFU Feature Register**

| Bit | Field | Supportability |
|---|---|---|
| BIT [7:1] | Reserved | - |
| BIT [0] | SUPPORTED_MODE_OPERATION_CODES | Not support |

### 7.5.4 FFU_ARG [490-487] (Read Only)

Using this field, the device reports to the host which value the host should set as an argument for read and write commands in FFU mode.

### 7.5.5 FW_CONFIG[169] (R/W)

BIT [0]: '0' FW updates enabled.
'1' FW update disabled permanently

**Table 19. FFU FW Config Register**

| Bit | Field | Supportability |
|---|---|---|
| BIT [7:1] | Reserved | - |
| BIT [0] | Update disable | FW updates enabled (0x0) |

### 7.5.6 FFU_STATUS [26] (R/W/E_P)

Using this field, the device reports to the host the state of FFU process

**Table 20. FFU Status Register**

| Value | Description |
|---|---|
| 0x13 ~ 0xFF | Reserved |
| 0x12 | Error in downloading Firmware |
| 0x11 | Firmware install error |
| 0x10 | General error |
| 0x01 ~ 0x0F | Reserved |
| 0x00 | Success |



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### 7.5.7 OPERATION_CODES_TIMEOUT[491](Read Only)

Maximum timeout for the SWITCH command when setting a value to the MODE_OPERATION_CODES field. The register is set to '0', because the controller doesn't support MODE_OPERATION_CODES.

**Table 21. FFU Operation Codes Timeout Register**

| Value | Description | Timeout value |
|---|---|---|
| 0x01 ~ 0x17 | MODE_OPERATION_CODES_TIMEOUT = 100us x 2OPERATION_CODES_TIMEOUT | (Not defined) |
| 0x18 ~ 0xFF | Reserved | - |

### 7.5.8 MODE_OPERATION_CODES[29] (W/E_P)

The host sets the operation to be performed at the selected mode, in case MODE_CONFIGS is set to FFU_MODE, MODE_OPERATION_CODES could have the following values:

**Table 22. FFU Mode Operation Codes Register**

| Value | Description |
|---|---|
| 0x01 | FFU_INSTALL |
| 0x02 | FFU_ABORT |
| 0x00, others | Reserved |

## 7.6 S.M.A.R.T. Health Report

S.M.A.R.T. is a monitoring system that detects and reports on various indicators of eMMC reliability (Including original bad blocks, increased bad blocks, power-up number, power-loss counts and etc.), with the intent of enabling the anticipation of hardware failures. We may be able to use recorded S.M.A.R.T. data to discover where the faults lie, ensure how to solve the problems and prevent them from recurring in future eMMC designs (For details, please refer to app note).

(End of Document)



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