EN25QH16B (2A)
16 Megabit Serial Flash Memory with 4Kbyte Uniform Sector

FEATURES

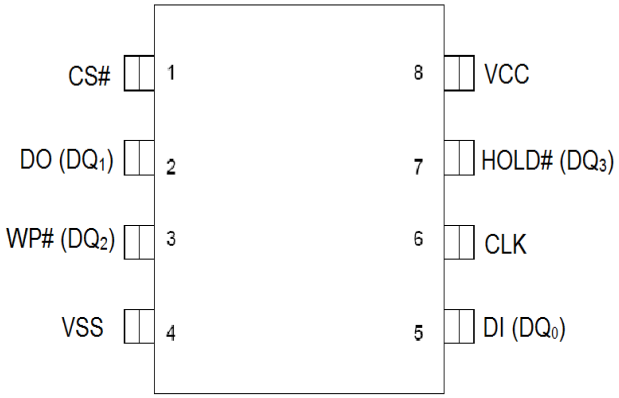
- Single power supply operation
  - Full voltage range: 2.3-3.6 volt
- Serial Interface Architecture
  - SPI Compatible: Mode 0 and Mode 3
- 16 M-bit Serial Flash
  - 16 M-bit/2,048 K-byte/8,192 pages
  - 256 bytes per programmable page
- Standard, Dual or Quad SPI
  - Standard SPI: CLK, CS#, DI, DO, WP#, HOLD#
  - Dual SPI: CLK, CS#, DQ_0, DQ_1, WP#, HOLD#
  - Quad SPI: CLK, CS#, DQ_0, DQ_1, DQ_2, DQ_3
- High performance
  - 2.3-2.7V
    - 86 MHz clock rate for Single/Dual/Quad I/O Fast Read
  - 2.7-3.6V
    - 104 MHz clock rate for Single/Dual/Quad I/O Fast Read
  - 3.0-3.6V
    - 133 MHz clock for Quad I/O Fast Read
- Low power consumption
  - 5 mA typical active current
  - 1 μA typical power down current
- Uniform Sector Architecture
  - 512 sectors of 4-Kbyte
  - 64 blocks of 32-Kbyte
  - 32 blocks of 64-Kbyte
  - Any sector or block can be erased individually
- Software and Hardware Write Protection
  - Write Protect all or portion of memory via software
  - Enable/Disable protection with WP# pin
- High performance program/erase speed
  - Page program time: 0.6 ms typical
  - Sector erase time: 50 ms typical
  - 32KB Block erase time 120 ms typical
  - 64KB Block erase time 150 ms typical
  - Chip erase time: 6 seconds typical
- 3 sets of OTP lockable 512 byte security sectors
- Support Serial Flash Discoverable Parameters (SFDP) signature
- Burst read with wrap(8/16/32/64 byte)
- Read Unique ID Number
- Minimum 100K endurance cycle
- Data retention time 20 years
- Package Options
  - 8-pin SOP 150 mil body width
  - 8-pin SOP 200 mil
  - 8-pin VSOP 150 mil
  - 8-pin PDIP
  - 8-contact VDFN / WSON (6x5 mm)
  - 8-contact USON (2x3x0.45 mm)
  - 8-contact USON (4x3x0.55 mm)
  - All Pb-free packages are compliant RoHS, Halogen-Free and REACH.
- Industrial temperature Range
- Volatile Status Register Bits

GENERAL DESCRIPTION

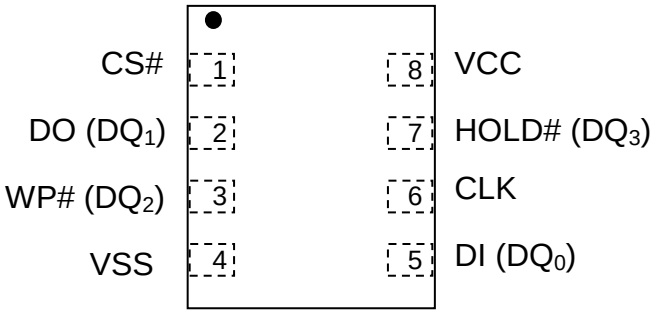
The device is a 16 Megabit (2,048 K-byte) Serial Flash memory, with enhanced write protection mechanisms. The device supports the standard Serial Peripheral Interface (SPI), and a high performance Dual/Quad output as well as Dual/Quad I/O using SPI pins: Serial Clock, Chip Select, Serial DQ_0 (DI), DQ_1 (DO), DQ_2 (WP#) and DQ_3 (HOLD#). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual Output and 416MHz (104MHz x 4) for Quad Output when using the Dual/Quad I/O Fast Read instructions. The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.

The device is designed to allow either single Sector/Block at a time or full chip erase operation. The device can be configured to protect part of the memory as the software protected mode. The device can sustain a minimum of 100K program/erase cycles on each sector or block.

CONNECTION DIAGRAMS (TOP VIEW)



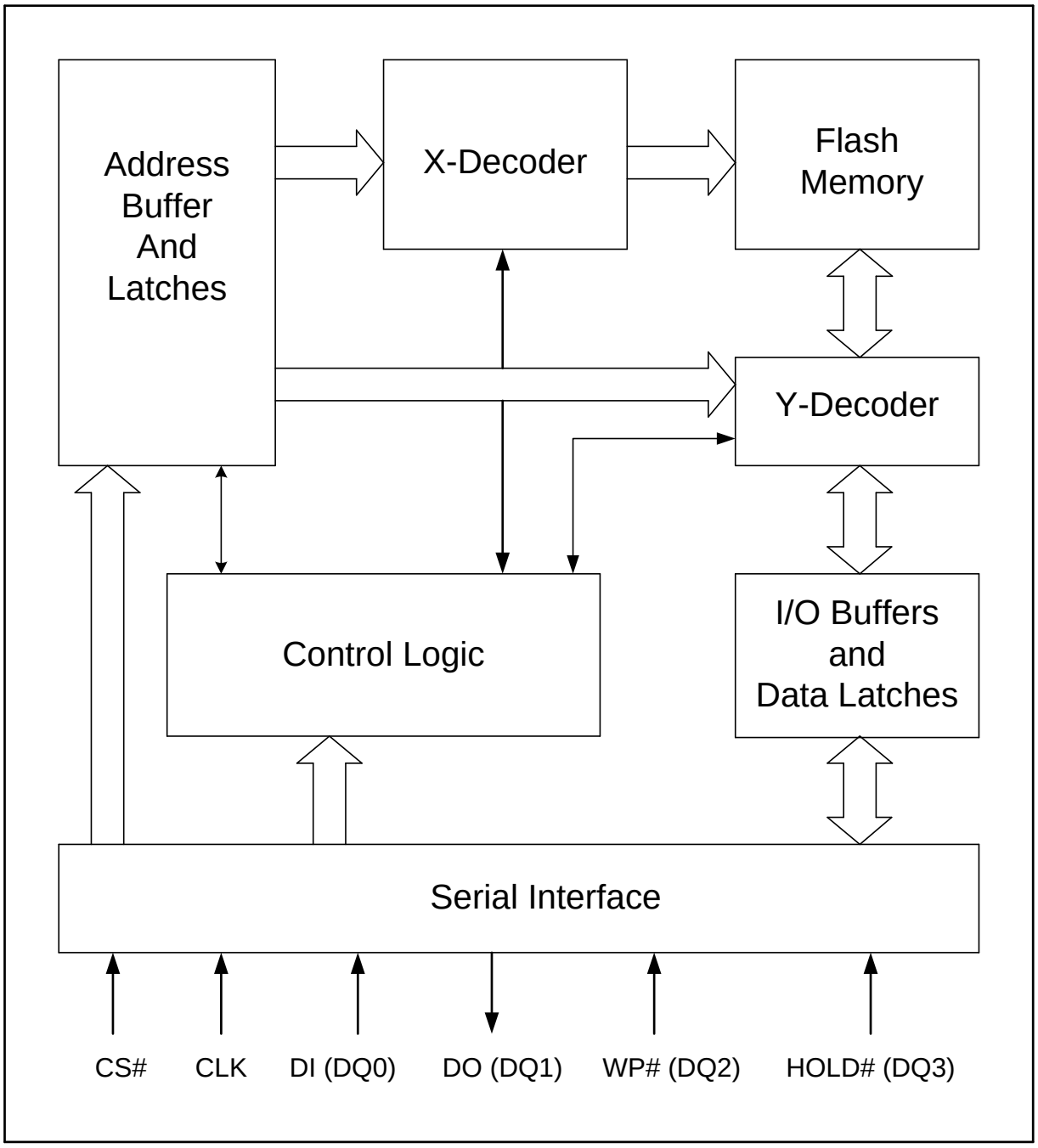
8 - LEAD SOP / PDIP



8 – LEAD USON / VDFN / WSON

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BLOCK DIAGRAM



Note:
1. DQ_0 and DQ_1 are used for Dual and Quad instructions.
2. DQ_0 ~ DQ_3 are used for Quad instructions.

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Pin Names

Symbol	Pin Name
CLK	Serial Clock Input
DI (DQ_0)	Serial Data Input (Data Input Output 0) *1
DO (DQ_1)	Serial Data Output (Data Input Output 1) *1
CS#	Chip Select
WP# (DQ_2)	Write Protect (Data Input Output 2) *2
HOLD# (DQ_3)	HOLD# pin (Data Input Output 3) *2
Vcc	Supply Voltage (2.3-3.6V)
Vss	Ground

Note:
1. DQ_0 and DQ_1 are used for Dual and Quad instructions.
2. DQ_2 ~ DQ_3 are used for Quad instructions.

SIGNAL DESCRIPTION

Serial Data Input, Output and IOs (DI, DO and DQ_0, DQ_1, DQ_2, DQ_3)

The device support standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge CLK.

Dual and Quad SPI instruction use the bidirectional IO pins to serially write instruction, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Mode")

Chip Select (CS#)

The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high the device is deselected and the Serial Data Output (DO, or DQ_0, DQ_1, DQ_2 and DQ_3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When CS# is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

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Hold (HOLD#)

The HOLD# pin allows the device to be paused while it is actively selected. When HOLD# is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). The hold function can be useful when multiple devices are sharing the same SPI signals. The HOLD# function is only available for standard SPI and Dual SPI operation, when during Quad SPI, this pin is the Serial Data IO (DQ_3) for Quad I/O operation.

Write Protect (WP#)

The Write Protect (WP#) pin enables the lock-down function of the Status Register Protect (SRP) bits in the Status Register. When WP# is driven low, the execution of the Write Status Register (WRSR) instruction is determined by the value of the SRP bit (see Conditions to Execute Write-Status- Register (WRSR) Instruction table). When WP# is high, the lock-down function of the SRP bit is disabled.

Conditions to Execute Write-Status- Register (WRSR) Instruction

WP#	SRP	Execute WRSR Instruction
L	1	Not Allowed
L	0	Allowed
H	X	Allowed

Uniform Block Sector Architecture

64K Block	32K Block	Sector	Address range	
31	63	511	01FF000h	01FFFFFh
	⋮	⋮	⋮	⋮
	62	496	01F0000h	01F0FFFh
30	61	495	01EF000h	01EFFFFh
	⋮	⋮	⋮	⋮
	60	480	01E0000h	01E0FFFh
29	59	479	01DF000h	01DFFFFh
	⋮	⋮	⋮	⋮
	58	464	01D0000h	01D0FFFh
⋮	⋮	⋮	⋮	⋮
18	37	303	012F000h	012FFFFh
	⋮	⋮	⋮	⋮
	36	288	0120000h	0120FFFh
17	35	287	011F000h	011FFFFh
	⋮	⋮	⋮	⋮
	34	272	0110000h	0110FFFh
16	33	271	010F000h	010FFFFh
	⋮	⋮	⋮	⋮
	32	256	0100000h	0100FFFh

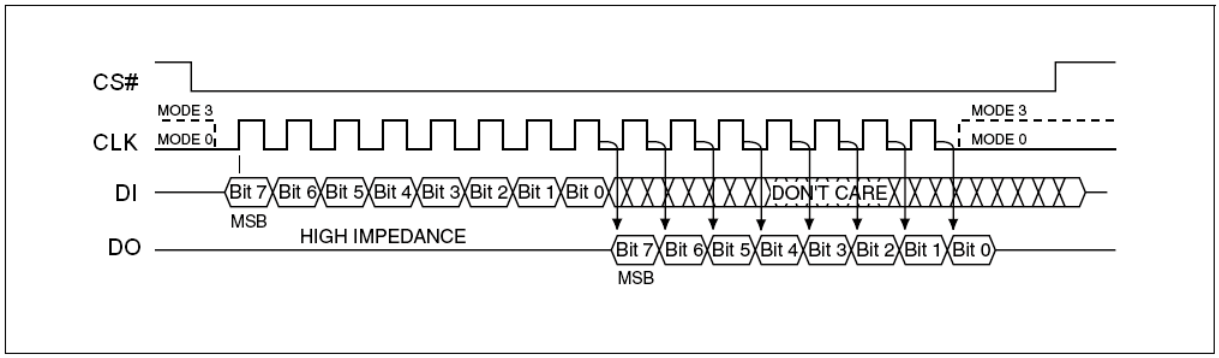
64K Block	32K Block	Sector	Address range	
15	31	255	00FF000h	00FFFFFh
	⋮	⋮	⋮	⋮
	30	240	00F0000h	00F0FFFh
14	29	239	00EF000h	00EFFFFh
	⋮	⋮	⋮	⋮
	28	224	00E0000h	00E0FFFh
13	27	223	00DF000h	00DFFFFh
	⋮	⋮	⋮	⋮
	26	208	00D0000h	00D0FFFh
⋮	⋮	⋮	⋮	⋮
2	5	47	002F000h	002FFFFh
	⋮	⋮	⋮	⋮
	4	32	0020000h	0020FFFh
1	3	31	001F000h	001FFFFh
	⋮	⋮	⋮	⋮
	2	16	0010000h	0010FFFh
0	1	15	000F000h	000FFFFh
	⋮	⋮	⋮	⋮
	0	0	0000000h	0000FFFh

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OPERATING FEATURES

Standard SPI Modes

The device is accessed through a SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Both SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3, as shown in SPI Modes figure, concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low. For Mode 3 the CLK signal is normally high. In either case data input on the DI pin is sampled on the rising edge of the CLK. Data output on the DO pin is clocked out on the falling edge of CLK.



SPI Modes

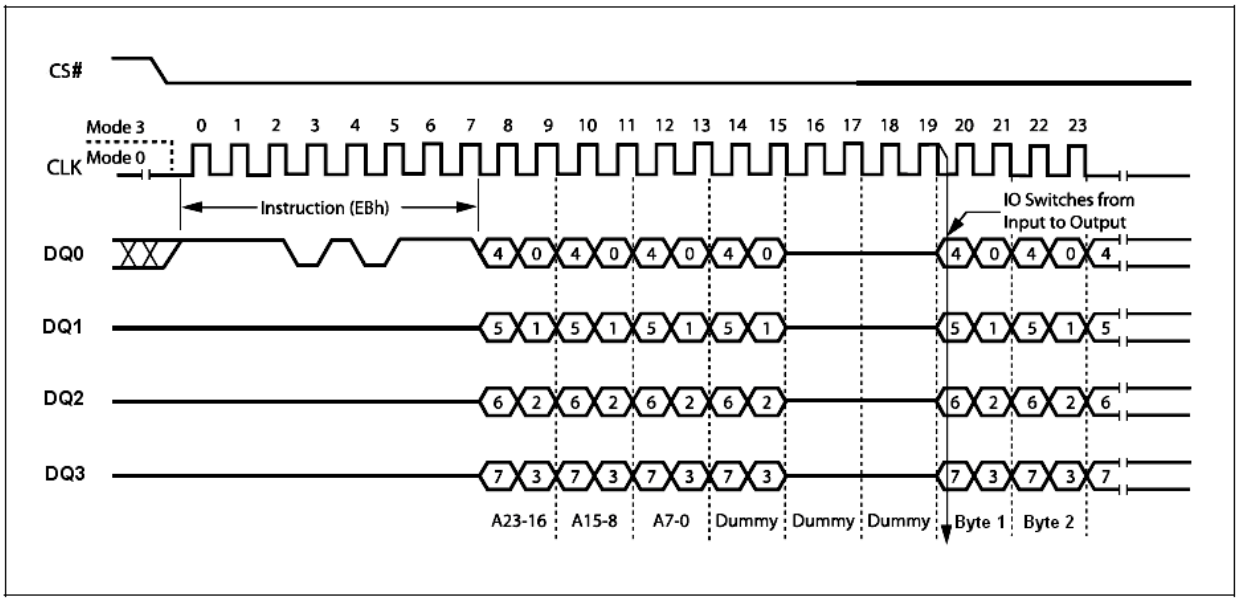
Dual SPI Instruction

The device supports Dual SPI operation when using the “Dual Output Fast Read and Dual I/O Fast Read “(3Bh and BBh) instructions. These instructions allow data to be transferred to or from the Serial Flash memory at two to three times the rate possible with the standard SPI. The Dual Read instructions are ideal for quickly downloading code from Flash to RAM upon power-up (code-shadowing) or for application that cache code-segments to RAM for execution. The Dual output feature simply allows the SPI input pin to also serve as an output during this instruction. When using Dual SPI instructions the DI and DO pins become bidirectional I/O pins; DQ_0 and DQ_1. All other operations use the standard SPI interface with single output signal.

Quad I/O SPI Modes

The device supports Quad input / output operation when using the Quad I/O Fast Read (EBh).This instruction allows data to be transferred to or from the Serial Flash memory at four to six times the rate possible with the standard SPI. The Quad Read instruction offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or for application that cache code-segments to RAM for execution. When using Quad SPI instruction the DI and DO pins become bidirectional I/O pins; DQ_0 and DQ_1, and the WP# and HOLD# pins become DQ_2 and DQ_3 respectively.

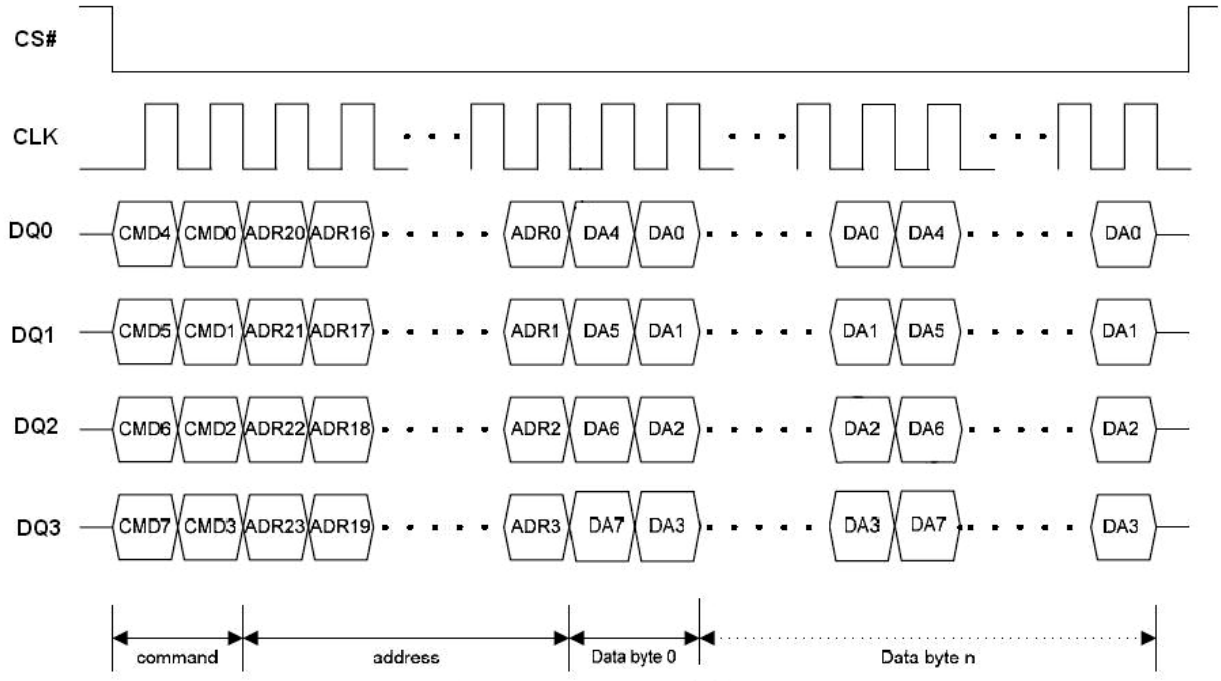
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Quad I/O SPI Modes

Full Quad SPI Modes (QPI)

The device also supports Full Quad SPI Mode (QPI) function while using the Enable Quad Peripheral Interface mode (EQPI) (38h). When using Quad SPI instruction the DI and DO pins become bidirectional I/O pins; DQ_0 and DQ_1, and the WP# and HOLD# pins become DQ_2 and DQ_3 respectively.



Full Quad SPI Modes

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Page Programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) or Quad Input Page Program (QPP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration t_{PP}).
To spread this overhead, the Page Program (PP) or Quad Input Page Program (QPP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0) provided that they lie in consecutive addresses on the same page of memory.

Sector Erase, Half Block Erase, Block Erase and Chip Erase

The Page Program (PP) or Quad Input Page Program (QPP) instruction allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved a sector at a time, using the Sector Erase (SE) instruction, half a block at a time using the Half Block Erase (HBE) instruction, a block at a time using the Block Erase (BE) instruction or throughout the entire memory, using the Chip Erase (CE) instruction. This starts an internal Erase cycle (of duration t_{SE}, t_{HBE}, t_{BE} or t_{CE}). The Erase instruction must be preceded by a Write Enable (WREN) instruction.

Polling During a Write, Program or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program (PP, QPP) or Erase (SE, HBE, BE or CE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{SE}, t_{HBE}, t_{BE} or t_{CE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

Active Power, Stand-by Power and Deep Power-Down Modes

When Chip Select (CS#) is Low, the device is enabled, and in the Active Power mode. When Chip Select (CS#) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, and Write Status Register). The device then goes into the Stand-by Power mode. The device consumption drops to I_{CC1}.

The Deep Power-down mode is entered when the specific instruction (the Enter Deep Power-down Mode (DP) instruction) is executed. The device consumption drops further to I_{CC2}. The device remains in this mode until another specific instruction (the Release from Deep Power-down Mode and Read Device ID (RDI) instruction) is executed.

All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program or Erase instructions.

Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern the device provides the following data protection mechanisms:

- Power-On Reset and an internal timer (t_{PUW}) can provide protection against inadvertent changes while the power supply is outside the operating specification.
- Program, Erase and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion or Write Status Register (WRSR) instruction completion or Page Program (PP), Quad Input Page Program (QPP) instruction completion or Sector Erase (SE) instruction completion or Half Block Erase (HBE) / Block Erase (BE) instruction completion or Chip Erase (CE) instruction completion
- The Block Protect (CMP, 4KBL, TB, BP2, BP1, BP0) bits allow part of the memory to be configured as read-only. This is the Software Protected Mode (SPM).
- The Write Protect (WP#) signal allows the Block Protect (4KBL, TB, BP2, BP1, BP0) bits and Status Register Protect (SRP) bit to be protected. This is the Hardware Protected Mode (HPM).
- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection from inadvertent Write, Program and Erase instructions, as all instructions are ignored except one particular instruction (the Release from Deep Power-down instruction).

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Protected Area Sizes Sector Organization

Status Register Content						Memory Content			
CMP	4KBL	TB	BP2	BP1	BP0	Protect area	Address	Density(KB)	portion
0	X	X	0	0	0	None	None	None	None
0	0	0	0	0	1	31	1F0000h-1FFFFFh	64KB	Upper 1/32
0	0	0	0	1	0	30 and 31	1E0000h-1FFFFFh	128KB	Upper 1/16
0	0	0	0	1	1	28 thru 31	1C0000h--1FFFFFh	256KB	Upper 1/8
0	0	0	1	0	0	24 thru 31	180000h--1FFFFFh	512KB	Upper 1/4
0	0	0	1	0	1	16 thru 31	100000h--1FFFFFh	1MB	Upper 1/2
0	0	1	0	0	1	0	000000h-00FFFFh	64KB	Lower 1/32
0	0	1	0	1	0	0 and 1	000000h-01FFFFh	128KB	Lower 1/16
0	0	1	0	1	1	0 thru 3	000000h-03FFFFh	256KB	Lower 1/8
0	0	1	1	0	0	0 thru 7	000000h-07FFFFh	512KB	Lower 1/4
0	0	1	1	0	1	0 thru 15	000000h-0FFFFFh	1MB	Lower 1/2
0	X	X	1	1	X	0 thru 31	000000h-1FFFFFh	2MB	All
0	1	0	0	0	1	31	1FF000h-1FFFFFh	4KB	Upper 1/512
0	1	0	0	1	0	31	1FE000h-1FFFFFh	8KB	Upper 1/256
0	1	0	0	1	1	31	1FC000h-1FFFFFh	16KB	Upper 1/128
0	1	0	1	0	X	31	1F8000h-1FFFFFh	32KB	Upper 1/64
0	1	1	0	0	1	0	000000h-000FFFh	4KB	Lower 1/512
0	1	1	0	1	0	0	000000h-001FFFh	8KB	Lower 1/256
0	1	1	0	1	1	0	000000h-003FFFh	16KB	Lower 1/128
0	1	1	1	0	X	0	000000h-007FFFh	32KB	Lower 1/64
1	X	X	0	0	0	0 thru 31	000000h-1FFFFFh	All	All
1	0	0	0	0	1	0 thru 30	000000h-1EFFFFh	1,948KB	Lower 31/32
1	0	0	0	1	0	0 thru 29	000000h-1DFFFFh	1,920KB	Lower 15/16
1	0	0	0	1	1	0 thru 27	000000h-1BFFFFh	1,792KB	Lower 7/8
1	0	0	1	0	0	0 thru 23	000000h-17FFFFh	1,536KB	Lower 3/4
1	0	0	1	0	1	0 thru 15	000000h-0FFFFFh	1MB	Lower 1/2
1	0	1	0	0	1	1 thru 31	010000h-1FFFFFh	1,984KB	Upper 31/32
1	0	1	0	1	0	2 and31	020000h-1FFFFFh	1,920KB	Upper 15/16
1	0	1	0	1	1	4 thru 31	040000h-1FFFFFh	1,792KB	Upper 7/8
1	0	1	1	0	0	8 thru 31	080000h-1FFFFFh	1,536KB	Upper 3/4
1	0	1	1	0	1	16 thru 31	100000h-1FFFFFh	1MB	Upper 1/2
1	X	X	1	1	X	None	None	None	None
1	1	0	0	0	1	0 thru 31	000000h-1FEFFFh	2,044KB	Lower 511/512
1	1	0	0	1	0	0 thru 31	000000h-1FDFFFh	2,040KB	Lower255/256
1	1	0	0	1	1	0 thru 31	000000h-1FBFFFh	2,032KB	Lower 127/128
1	1	0	1	0	X	0 thru 31	000000h-1F7FFFh	2,016KB	Lower 63/64

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1	1	1	0	0	1	0 thru 31	001000h-1FFFFFh	2,044KB	Upper 511/512
1	1	1	0	1	0	0 thru 31	002000h-1FFFFFh	2,040KB	U255/256
1	1	1	0	1	1	0 thru 31	004000h-1FFFFFh	2,032KB	U127/128
1	1	1	1	0	X	0 thru 31	00800h-1FFFFFh	2,016KB	U63/64

Enable Boot Lock

The Enable Boot Lock feature enables user to lock the 64KB block/sector on the top/bottom of the device for protection.

The bits' definitions are described in the following table.

The Enable Boot Lock feature

Normal mode

Register	Type	Description	Function
SR5	non-volatile / volatile	TB	0 : Top (default) 1 : Bottom
SR6	non-volatile / volatile	4KB BL bit	0 : 64KB-Block (default) 1 : Sector

OTP mode

Register	Type	Description	Function
SR3	OTP / volatile	EBL(Enable Boot Lock) bit	0 (default) 1 : 64KB-block/Sector lock selected

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INSTRUCTIONS

All instructions, addresses and data are shifted in and out of the device, most significant bit first. Serial Data Input (DI) is sampled on the first rising edge of Serial Clock (CLK) after Chip Select (CS#) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (DI), each bit being latched on the rising edges of Serial Clock (CLK).

The instruction set is listed in Instruction Set table. Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. Chip Select (CS#) must be driven High after the last bit of the instruction sequence has been shifted in. In the case of a Read Data Bytes (READ), Read Data Bytes at Higher Speed (Fast_Read), Dual Output Fast Read (3Bh), Dual I/O Fast Read (BBh), Quad Input/Output FAST_READ (EBh), Qual Output Fast Read (6Bh), Read Status Register (RDSR), Read Status Register 3 (RDSR3) or Release from Deep Power-down, and Read Device ID (RDI) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select (CS#) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a Page Program (PP), Quad Input Page Program (QPP), Sector Erase (SE), Half Block Erase (HBE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), Volatile Status Register Write Enable, Write Enable (WREN), Write Disable (WRDI) or Deep Power-down (DP) instruction, Chip Select (CS#) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select (CS#) must driven High when the number of clock pulses after Chip Select (CS#) being driven Low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

In the case of multi-byte commands of Page Program (PP), Quad Input Page Program (QPP) and Release from Deep Power Down (RES) minimum number of bytes specified has to be given, without which, the command will be ignored.

In the case of Page Program, if the number of byte after the command is less than 4 (at least 1 data byte), it will be ignored too. In the case of SE, HBE and BE, exact 24-bit address is a must, any less or more will cause the command to be ignored.

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected.

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Instruction Set

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
EQPI	38h						
RSTQIO(1) Release Quad I/O or Fast Read Enhanced Mode	FFh						
RSTEN	66h						
RST(2)	99h						
Write Enable	06h						
Volatile Status Register Write Enable (3)	50h						
Write Disable / Exit OTP mode	04h						
Read Status Register (RDSR)	05h	(SR7-SR0) (4)					continuous(5)
Read Status Register 3 (RDSR3)	95h	(SR7-SR0)(4)					
Write Status Register (WRSR)	01h	SR7-SR0					
Write Status Register 3 (WRSR3)	C0h	SR7-SR0					
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	Next byte	continuous
Quad Input Page Program	32h	A23-A16	A15-A8	A7-A0	(D7-D0, …) (6)		(one byte per 2 clocks, continuous)
Sector Erase	20h	A23-A16	A15-A8	A7-A0			
32KB Half Block Erase (HBE)	52h	A23-A16	A15-A8	A7-A0			
64KB Block Erase	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/ 60h						
Deep Power-down	B9h						
Release from Deep Power-down, and read Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)		(7)
Release from Deep Power-down							
Manufacturer/ Device ID	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	(8)
				01h	(ID7-ID0)	(M7-M0)	
Read Identification	9Fh	(M7-M0)	(ID15-ID8)	(ID7-ID0)	(9)		
Enter OTP mode	3Ah						
Read SFDP mode and Unique ID Number	5Ah	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(Next Byte) continuous

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Note:

1. Device accepts eight-clocks command in Standard SPI mode, or two-clocks command in Quad SPI mode.
2. RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.
3. Volatile Status Register Write Enable command must precede WRSR command without any intervening commands to write data to Volatile Status Register.
4. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data being read from the device on the DO pin.
5. The Status Register contents will repeat continuously until CS# terminate the instruction.
6. Quad Data
   DQ_0 = (D4, D0, ……)
   DQ_1 = (D5, D1, ……)
   DQ_2 = (D6, D2, …...)
   DQ_3 = (D7, D3, …...)
7. The Device ID will repeat continuously until CS# terminates the instruction.
8. The Manufacturer ID and Device ID bytes will repeat continuously until CS# terminates the instruction. 00h on Byte 4. starts with MID and alternate with DID, 01h on Byte 4 starts with DID and alternate with MID.
9. (M7-M0) : Manufacturer, (ID15-ID8) : Memory Type, (ID7-ID0) : Memory Capacity.

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Instruction Set (Read Instruction)

Instruction Name	OP Code	Address bits	Dummy bits / Clocks (Default)	Data Out	Remark
Read Data	03h	24 bits	0	(D7-D0, …)	(Next Byte) continuous
Fast Read	0Bh	24 bits	8 bits / 8 clocks	(D7-D0, …)	(Next Byte) continuous
Dual Output Fast Read	3Bh	24 bits	8 bits / 8 clocks	(D7-D0, …)	(one byte Per 4 clocks, continuous)
Dual I/O Fast Read	BBh	24 bits	8 bits / 4 clocks	(D7-D0, …)	(one byte Per 4 clocks, continuous)
Quad I/O Fast Read	EBh	24 bits	24 bits / 6 clocks	(D7-D0, …)	(one byte per 2 clocks, continuous)
Quad Output Fast Read	6Bh	24 bits	8 bits/ 8 clocks	(D7-D0, …)	(one byte per 2 clocks, continuous)
Burst Read with Wrap	0Ch	24 bits	8 bits / 8 clocks	(D7-D0, …)	(Next Byte) continuous

Instruction Set (Read Instruction support mode and apply dummy cycle setting)

Instruction Name	OP Code	Start From SPI/QPI (1)		Dummy Byte (2)	
		SPI	QPI	Start From SPI	Start From QPI
Read Data	03h	Yes	No	N/A	N/A
Fast Read	0Bh	Yes	Yes	8 clocks	By SR3.4~5
Dual Output Fast Read	3Bh	Yes	No	8 clocks	N/A
Dual I/O Fast Read	BBh	Yes	No	4 clocks	N/A
Quad Output Fast Read	6Bh	Yes	No	8 clocks	N/A
Quad I/O Fast Read	EBh	Yes	Yes	By SR3.4~5	By SR3.4~5
Read Burst with wrap	0Ch	Yes	Yes	8 clocks	By SR3.4~5

Note:
1. 'Start From SPI/QPI' means if this command is initiated from SPI or QPI mode.
2. The dummy byte settings please refer to Status Register 3 Bit Locations table.

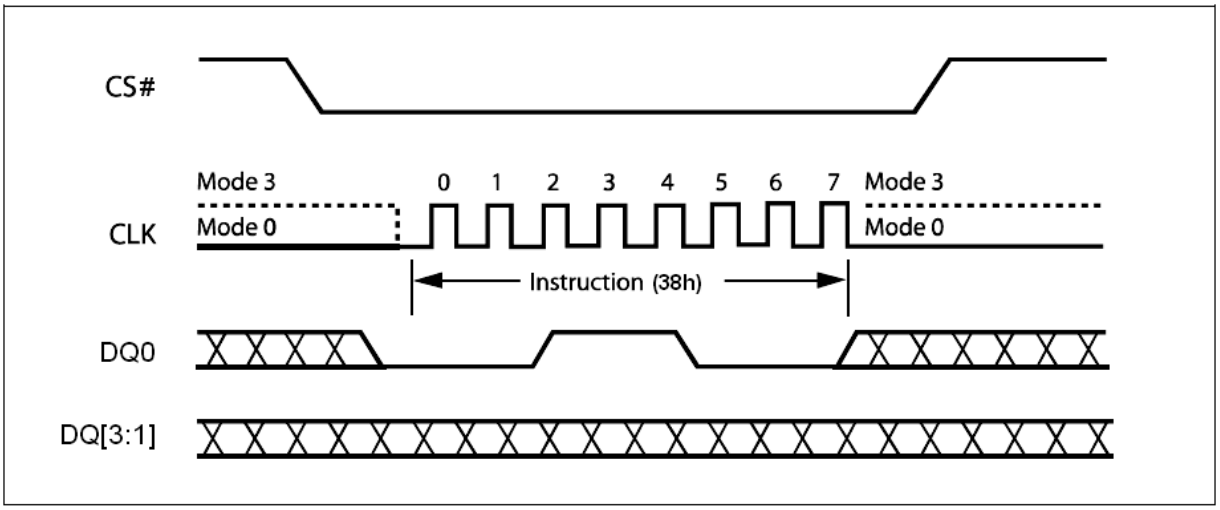
Manufacturer and Device Identification

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			14h
90h	1Ch		14h
9Fh	1Ch	7015h	

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Enable Quad Peripheral Interface mode (EQPI) (38h)

The Enable Quad Peripheral Interface mode (EQPI) instruction will enable the flash device for Quad SPI bus operation. Upon completion of the instruction, all instructions thereafter will be 4-bit multiplexed input/output until a power cycle or " Reset Quad I/O instruction " instruction, as shown in Enable Quad Peripheral Interface mode Sequence Diagram figure. The device did not support the Read Data Bytes (READ) (03h)**,** Dual Output Fast Read (3Bh) and Dual Input/Output FAST_READ (BBh), Quad Input Page Program (32h) and Qual output fast read (6Bh) modes while the Enable Quad Peripheral Interface mode (EQPI) (38h) turns on.



Enable Quad Peripheral Interface mode Sequence Diagram

Reset Quad I/O (RSTQIO) or Release Quad I/O Fast Read Enhancement Mode (FFh)

The Reset Quad I/O instruction resets the device to 1-bit Standard SPI operation. To execute a Reset Quad I/O operation, the host drives CS# low, sends the Reset Quad I/O command cycle (FFh) then, drives CS# high. This command can't be used in Standard SPI mode.

User also can use the 0xFFh command to release the Quad I/O Fast Read Enhancement Mode. The detail description, please see the Quad I/O Fast Read Enhancement Mode section.

Note:
If the system is in the Quad I/O Fast Read Enhance Mode in QPI Mode, it is necessary to execute 0xFFh command by two times. The first 0xFFh command is to release Quad I/O Fast Read Enhance Mode, and the second 0xFFh command is to release QPI Mode.

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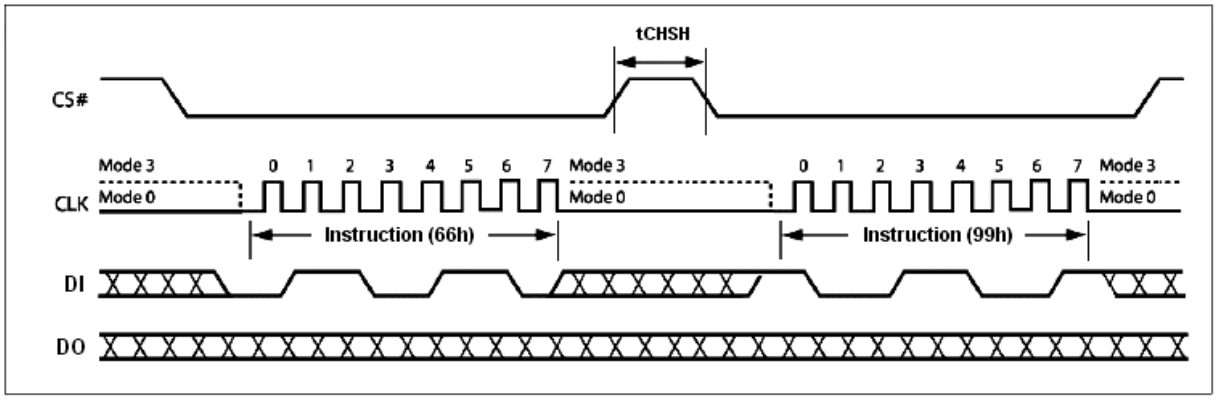
Reset-Enable (RSTEN) (66h) and Reset (RST) (99h)

The Reset operation is used as a system (software) reset that puts the device in normal operating Ready mode. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST).

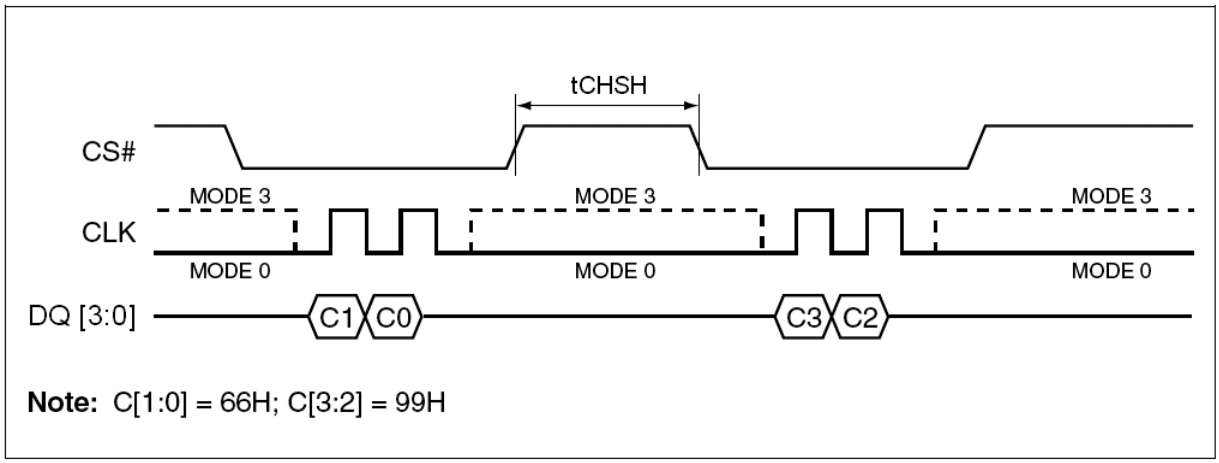
To reset the device the host drives CS# low, sends the Reset-Enable command (66h), and drives CS# high. Next, the host drives CS# low again, sends the Reset command (99h), and drives CS# high.

The Reset operation requires the Reset-Enable command followed by the Reset command. Any command other than the Reset command after the Reset-Enable command will disable the Reset-Enable.

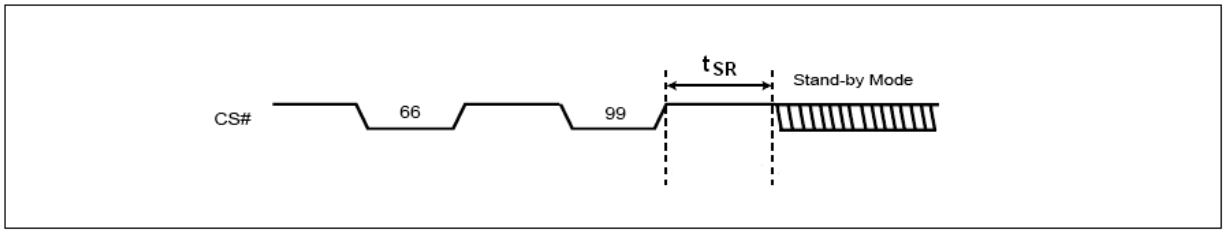
A successful command execution will reset the Status register to data = 00h, see Reset-Enable and Reset Sequence Diagram figure for SPI Mode and Reset-Enable and Reset Sequence Diagram in QPI Mode figure for QPI Mode. A device reset during an active Program or Erase operation aborts the operation, which can cause the data of the targeted address range to be corrupted or lost. Depending on the prior operation, the reset timing may vary. Recovery from a Write operation requires more software latency time (t_{SR}) than recovery from other operations. Please Software Reset Recovery figure.



Reset-Enable and Reset Sequence Diagram



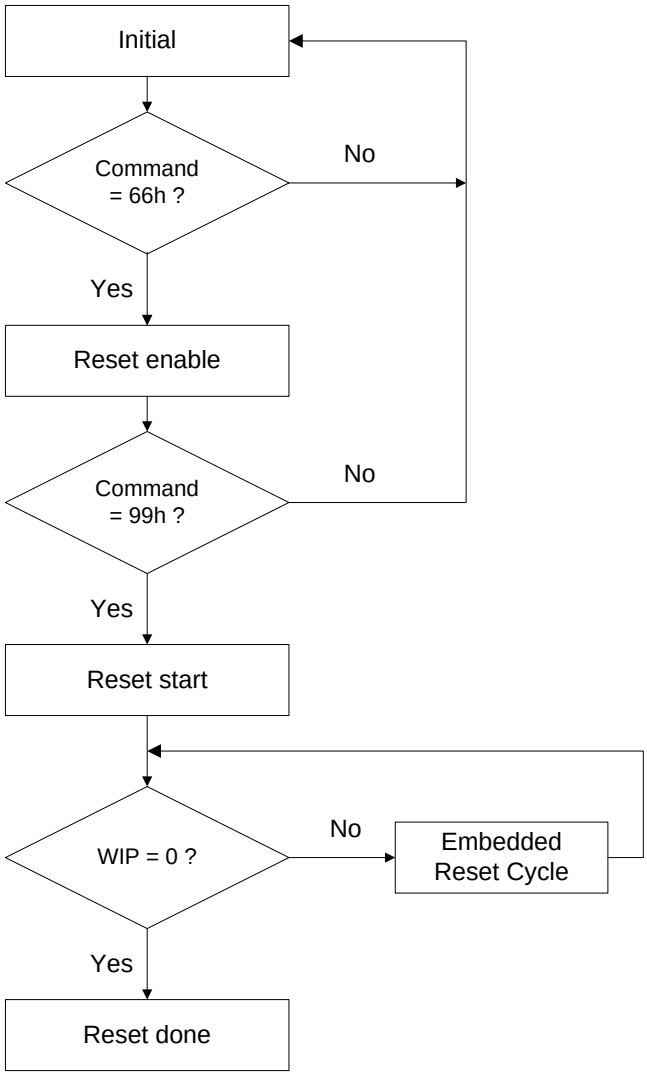
Reset-Enable and Reset Sequence Diagram in QPI Mode



Software Reset Recovery

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Software Reset Flow



Note:

1. Reset-Enable (RSTEN) (66h) and Reset (RST) (99h) commands need to match standard SPI or QPI (Full Quad) mode.
2. Continue (Enhance) EB mode need to use quad Reset-Enable (RSTEN) (66h) and quad Reset (RST) (99h) commands.
3. If user is not sure it is in SPI or Quad mode, we suggest to execute sequence as follows:
   Quad Reset-Enable (RSTEN) (66h) -> Quad Reset (RST) (99h) -> SPI Reset-Enable (RSTEN) (66h)
   -> SPI Reset (RST) (99h) to reset.
4. The reset command could be executed during embedded program and erase process, QPI mode and Continue EB mode to back to SPI mode.
5. This flow cannot release the device from Deep power down mode.
6. If user reset device during erase, the embedded reset cycle software reset latency will take about 28us in worst case.
7. User can't do software reset command while doing 4K/32K erase operation.

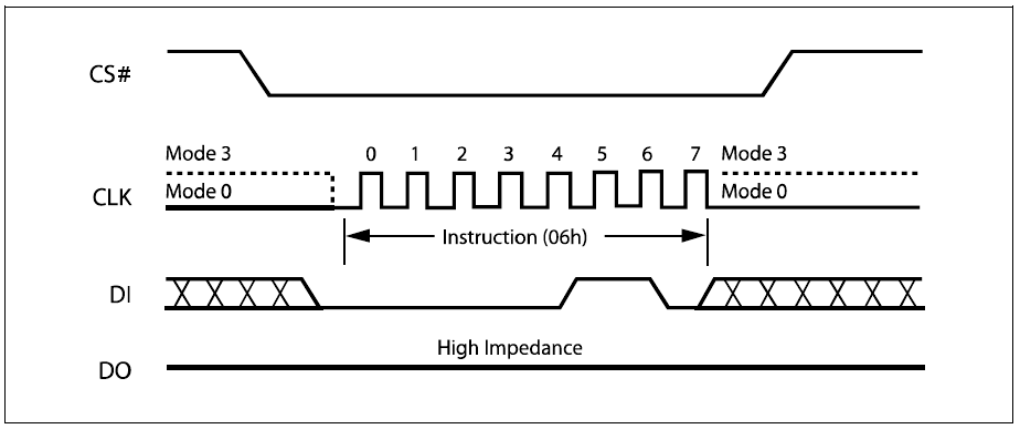
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Write Enable (WREN) (06h)

The Write Enable (WREN) instruction (Write Enable Instruction Sequence Diagram figure) sets the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Half Block Erase (HBE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR/WRSR3) instruction.

The Write Enable (WREN) instruction is entered by driving Chip Select (CS#) Low, sending the instruction code, and then driving Chip Select (CS#) High.

The instruction sequence is shown in Write Enable/Disable Instruction Sequence in QPI Mode figure while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.



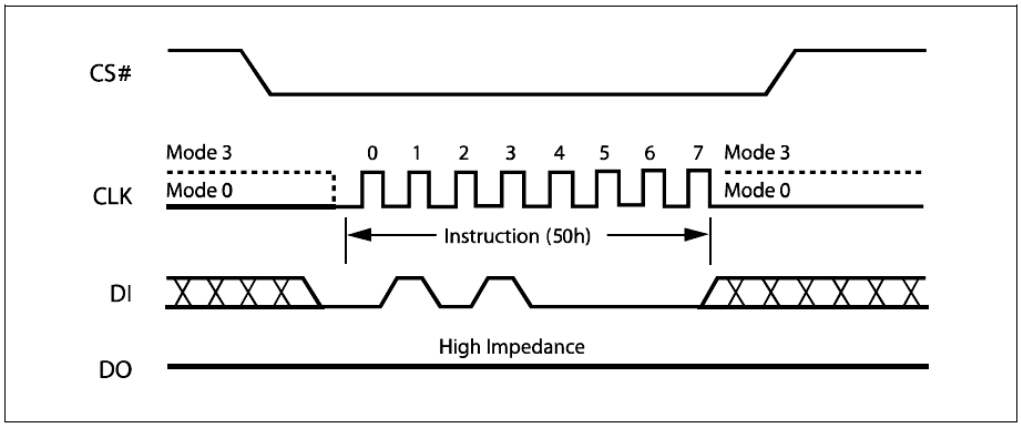
Write Enable Instruction Sequence Diagram

Volatile Status Register Write Enable (50h)

This feature enable user to change memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Volatile Status Register Write Enable (50h) command won't set the Write Enable Latch (WEL) bit, it is only valid for 'Write Status Register' command to change the Volatile Status Register bit values.

To write to Volatile Status Register, issue the Volatile Status Register Write Enable (50h) command prior issuing WRSR. The Status Register bits will be refresh to Volatile Status Register (SR[7:2]) within tSHSL2 (50ns). Upon power off or the execution of a Software/Hardware Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored. The instruction sequence is shown in Volatile Status Register Write Enable Instruction Sequence Diagram figure.

The instruction sequence is shown in Write Enable/Disable Instruction Sequence in QPI Mode figure while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.



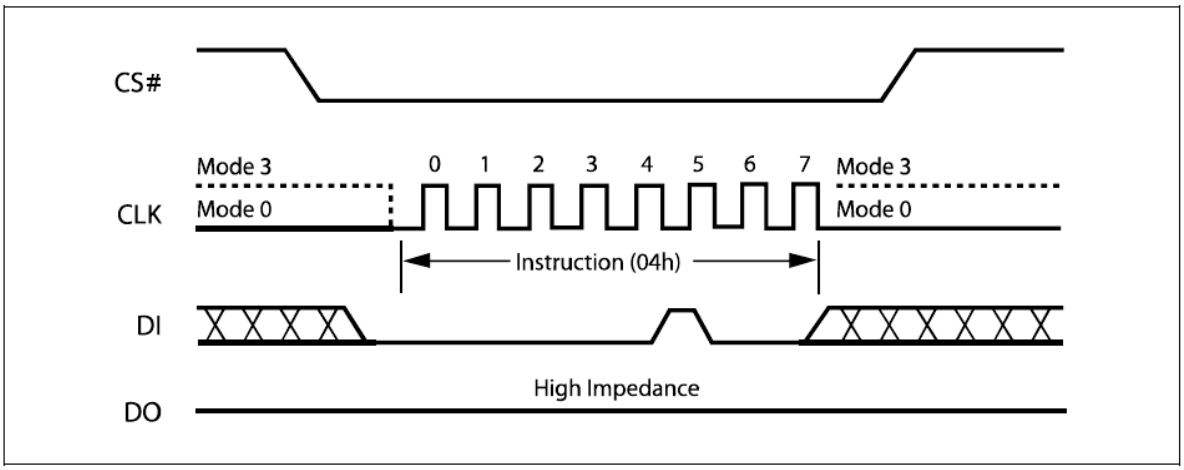
Volatile Status Register Write Enable Instruction Sequence Diagram

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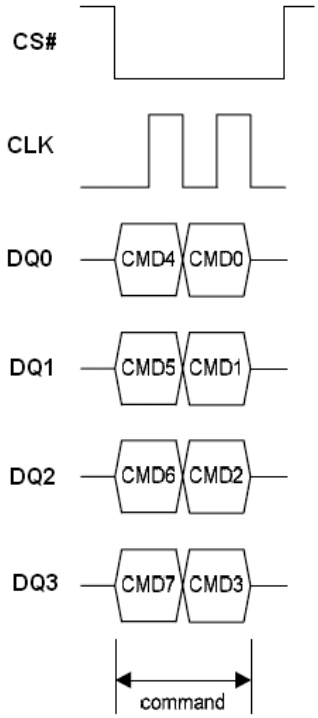
Write Disable (WRDI) (04h)

The Write Disable instruction (Write Disable Instruction Sequence Diagram figure) resets the Write Enable Latch (WEL) bit in the Status Register to a 0 or exit from OTP mode to normal mode. The Write Disable instruction is entered by driving Chip Select (CS#) low, shifting the instruction code “04h” into the DI pin and then driving Chip Select (CS#) high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Half Block Erase (HBE), Block Erase (BE) and Chip Erase instructions.

The instruction sequence is shown in Write Enable/Disable Instruction Sequence in QPI Mode figure while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.



Write Disable Instruction Sequence Diagram



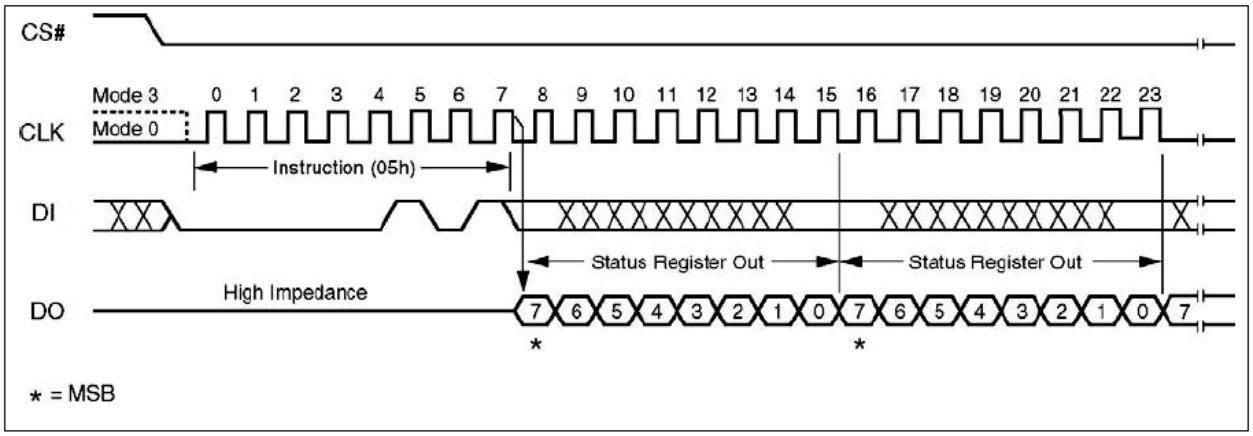
Write Enable/Disable Instruction Sequence in QPI Mode

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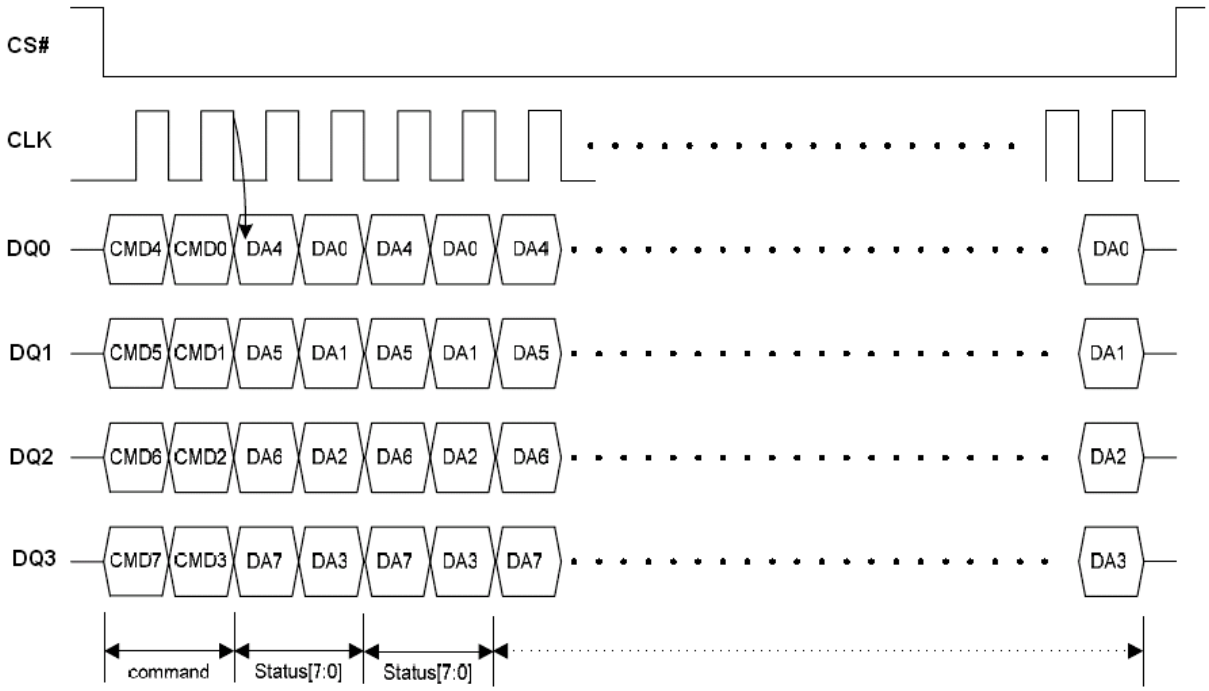
Read Status Register (RDSR) (05h)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in Read Status Register Instruction Sequence Diagram figure.

The instruction sequence is shown in Read Status Register Instruction Sequence in QPI Mode figure while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.



Read Status Register Instruction Sequence Diagram



Read Status Register Instruction Sequence in QPI Mode

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Status Register Bit Locations

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
SRP bit	4KBL	TB	BP2 bit	BP1 bit	BP0 bit	WEL bit	WIP bit
SPL0 bit	WHDIS bit	reversed	CMP	EBL	SPL1 bit	SPL2 bit	WIP bit

Status Register Bit Locations (In Normal mode)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
SRP Status Register Protect	4KB BL bit (4KB boot lock)	TB bit (Top / Bottom Protect)	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL bit (Write Enable Latch)	WIP bit (Write In Progress bit)
1 = status register write disable	1 = Sector 0 = 64KB Block (default 0)	1 = Bottom 0 = Top (default 0)	(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Volatile bit / Non-volatile bit	Non-volatile bit / Volatile bit	Non-volatile bit / Volatile bit	Volatile bit / Non-volatile bit	Volatile bit / Non-volatile bit	Volatile bit / Non-volatile bit	Read only bit	Read only bit

Status Register Bit Locations (In OTP mode)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
SPL0 bit	WHDIS bit (WP# and HOLD# disabled)	none	CMP	EBL bit (Enable Boot Lock)	SPL1 bit	SPL2 bit	WIP bit (Write In Progress bit)
1 = security page 0 is protected	1 = WP# and HOLD# disable 0 = WP# and HOLD# enable (default 0)		(note 2)	1 = Lock selected 64KB-Block-Sector	1 = security page 1 is protected	1 = security page 2 is protected	1 = write operation 0 = not in write operation
OTP bit / Volatile bit	OTP bit / Volatile bit		OTP bit / volatile bit	OTP bit / volatile bit	OTP bit / Volatile bit	OTP bit / Volatile bit	Read only bit

Note

1. In OTP mode, SR7 bit is served as SPL0 bit; SR6 bit is served as WHDIS bit; SR4, CMP, SR3, EBL, SR2 bit is served as SPL1 bit ; SR1 bit is served as SPL2 bit and SR0 bit is served as WIP bit.
2. See the “Protected Area Sizes Sector Organization” table.

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The status and control bits of the Status Register are as follows:

WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

BP2, BP1, BP0 bits. The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP2, BP1, BP0) bits is set to 1, the relevant memory area (as defined in Protected Area Sizes Sector Organization table.) becomes protected against Page Program (PP) Sector Erase (SE) and , Block Erase (BE), instructions. The Block Protect (BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) instruction is executed if, and only if, all Block Protect (BP2, BP1, BP0) bits are 0. (Note: If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.)

SRP bit. The Status Register Protect (SRP) bit is operated in conjunction with the Write Protect (WP#) signal. The Status Register Write Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected mode (when the Status Register Protect (SRP) bit is set to 1, and Write Protect (WP#) is driven Low). In this mode, the non-volatile bits of the Status Register (SRP, BP3, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Top/Bottom switch bit. (SR3)
This bit is set by WRSR command in normal mode and also it work for block Protect area by BP table. It is used to set the protected 64KB-Block/Sector location to the top/bottom in the device.

4KB BL bit. (SR4)
This bit is set by WRSR command in normal mode and also it work for block Protect area by BP table.. It is used to set the protection area size as block (64KB) or sector (4KB).

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In OTP mode, SR7, SR6, SR4, SR3, SR2, SR1 and SR0 are served as SPL0 Bit, WHDIS bit, CMP bit, EBL bit, SPL1 bit, SPL2 bit and WIP bit.

SPL2 bit. (SR1)

The SPL2 bit is non-volatile One Time Program (OTP) bit in status register that provide the write protect control and status to the security page 2. User can read/program/erase security page 2 as normal page while SPL2 value is equal 0, after SPL2 is programmed with 1 by WRSR command, the security page 2 is protected from program and erase operation. The SPL2 bit can only be programmed once.

SPL1 bit. (SR2)

The SPL1 bit is non-volatile One Time Program (OTP) bit in status register that provide the write protect control and status to the security page 1. User can read/program/erase security page 1 as normal page while SPL1 value is equal 0, after SPL1 is programmed with 1 by WRSR command, the security page 1 is protected from program and erase operation. The SPL1 bit can only be programmed once.

Enable Boot Lock bit

When this bit is programmed to '1' by WRSR command, the Top/Bottom switch bit and 4KB BL bit and the selected sector/block will be locked. It is OTP bit.

WHDIS bit. (SR6). The WP# and Hold# Disable bit (WHDIS bit), OTP bit, it indicates the WP# and HOLD# are enabled or not. When it is "0" (factory default), the WP# and HOLD# are enabled. On the other hand, while WHDIS bit is "1", the WP# and HOLD# are disabled. No matter WHDIS is "0" or "1", the system can executes Quad Input/Output FAST_READ (EBh) or EQPI (38h) command directly. User can use Flash Programmer to set WHDIS bit as "1" and then the host system can let WP# and HOLD# keep floating in SPI mode.

SPL0 bit. (SR7)

The SPL0 bit is non-volatile One Time Program (OTP) bit in status register that provide the write protect control and status to the security page 0. User can read/program/erase security page 0 as normal page while SPL0 value is equal 0, after SPL0 is programmed with 1 by WRSR command, the security page 0 is protected from program and erase operation. The SPL0 bit can only be programmed once.

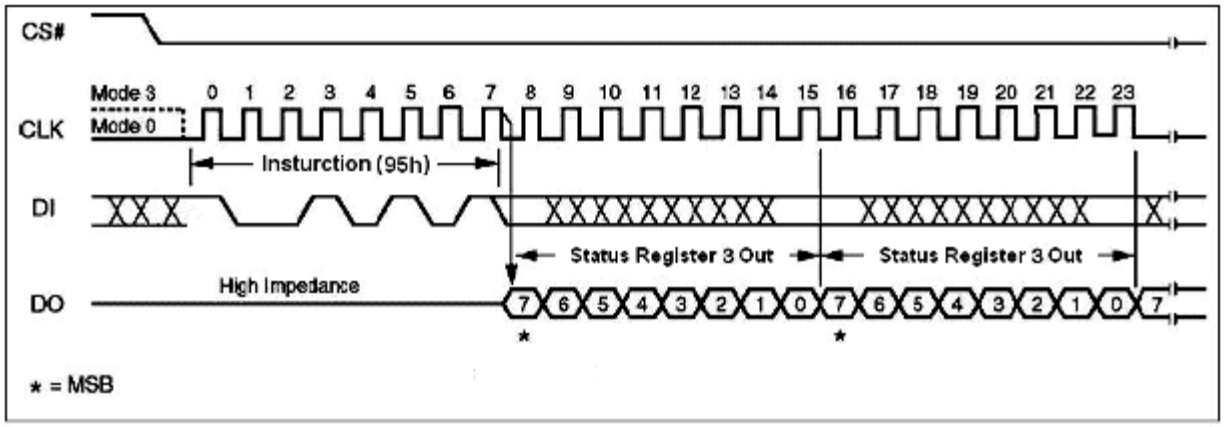
CMP bit. The Complement Protect bit (CMP) is a non-volatile bit in the Status Register 4. It is used in conjunction with 4KBL, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. The default setting is CMP=0.

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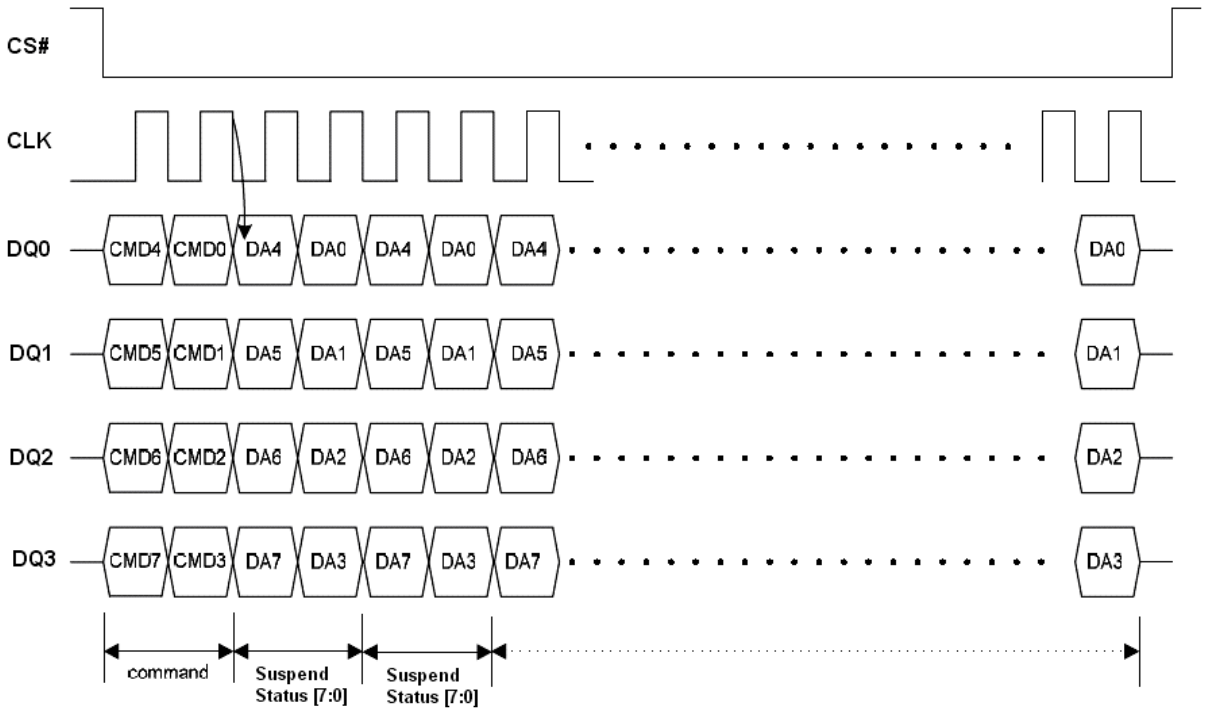
Read Status Register 3 (RDSR 3) (95h)

The Read Status Register 3 (RDSR3) instruction allows the Status Register 3 to be read. The Status Register 3 may be read at any time. When one of these bytes is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Read Status Register 3 continuously, as shown in Read Status Register 3 Instruction Sequence Diagram figure.

The instruction sequence is shown in Read Status Register 3 Instruction Sequence in QPI Mode figure while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.



Read Status Register 3 Instruction Sequence Diagram



Read Status Register 3 Instruction Sequence in QPI Mode

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The status and control bits of the Status Register 3 are as follows:

Burst Length. The Burst Length (SR3.1 and SR3.0) bits indicate the status of wrap burst read length.

Output Drive Strength. The Output Drive Strength (SR3.3 and SR3.2) bits indicate the status of output Drive Strength in I/O pins.

Dummy Byte. The Dummy Byte (SR3.5 and SR3.4) bits indicate the status of the number of dummy byte in high performance read.

Reserved bit. SR3.7 and SR3.6 are reserved for future use.

Status Register 3 Bit Locations

SR3.7	SR3.6	SR3.5	SR3.4	SR3.3	SR3.2	SR3.1	SR3.0
Reserved	Reserved	Dummy Byte (1) Default = 00		Output Drive Strength		Burst Length	
		For without Wrap command: 00 = 3 Bytes 01 = 2 Bytes 10 = 4 Bytes 11 = 5 Bytes	For with Wrap command: 00 = 2 Bytes 01 = 3 Bytes 10 = 4 Bytes 11 = 5 Bytes	00 = 67% (2/3) Drive (default) 01 = 100% (Full) Drive 10 = 50% (1/2) Drive 11 = 33% (1/3) Drive		00 = 8 Bytes(default) 01 = 16 Bytes 10 = 32 Bytes 11 = 64 Bytes	
volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	volatile bit

Note:

1. 2 Bytes (4 clocks in Quad mode), 3 Bytes (6 clocks in Quad mode), 4 Bytes (8 clocks in Quad mode), 5 Bytes (10 clocks in Quad mode)

SR3.4 and SR3.5 Status (for Dummy Bytes)

Instruction Name	Op Code	Start Address (1)	Dummy Byte settings
			<=104MHz
Fast Read	**0Bh**	Byte	3
		Word	2
		Dword	2
Quad IO Fast Read	**EBh**	Byte	3
		Word	2
		Dword	2
Read Burst with wrap	**0Ch**	Byte	3
		Word	2
		Dword	2

Note:

1. “Dword” means the start address is 4-byte aligned (i.e. Start Address is 0, 4, 8...), “Word” means the start address is 2-byte aligned (i.e. Start Address is 0, 2, 4, 8...) and “Byte” means the start address can be anywhere without 2-byte or 4-byte aligned.

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Write Status Register (WRSR) (01h)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

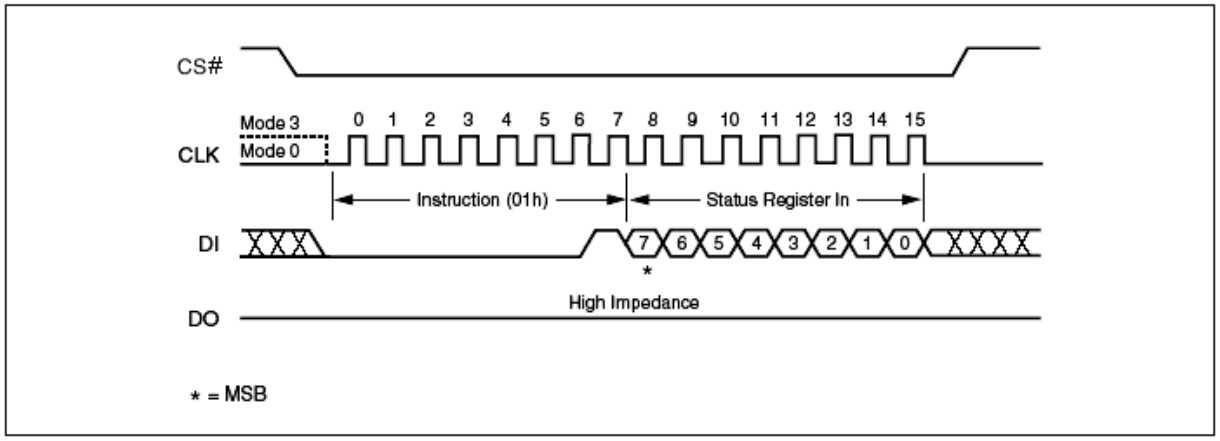
The Write Status Register (WRSR) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code and the data byte on Serial Data Input (DI).

The instruction sequence is shown in Write Status Register Instruction Sequence Diagram figure. The Write Status Register (WRSR) instruction has no effect on SR1 and SR0 of the Status Register. Chip Select (CS#) must be driven High after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (4KBL, TB, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Protected Area Sizes Sector Organization table. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction is not executed once the Hardware Protected Mode (HPM) is entered.

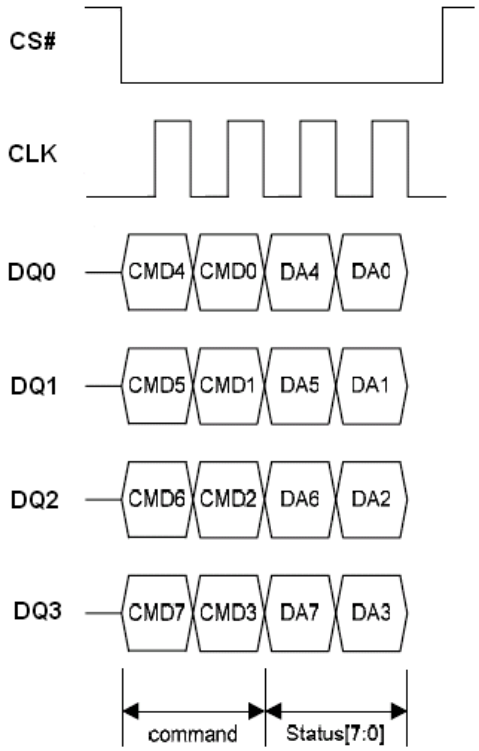
The instruction sequence is shown in Write Status Register Instruction Sequence in QPI Mode figure while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

Note :
In the OTP mode without enabling Volatile Status Register function (50h), WRSR command is used to program SPL0 bit, WHDIS bit, CMP bit, EBL bit, SPL1 bit and SPL2 bit to '1', but these bits can only be programmed once



Write Status Register Instruction Sequence Diagram

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Write Status Register Instruction Sequence in QPI Mode

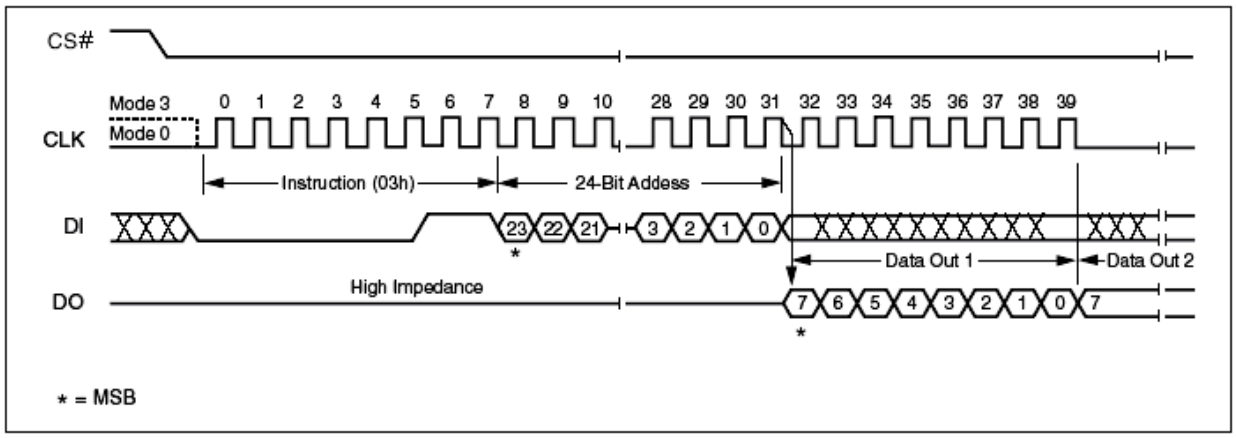
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Read Data Bytes (READ) (03h)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (CLK).

The instruction sequence is shown in Read Data Instruction Sequence Diagram figure. The first byte addresses can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.



Read Data Instruction Sequence Diagram

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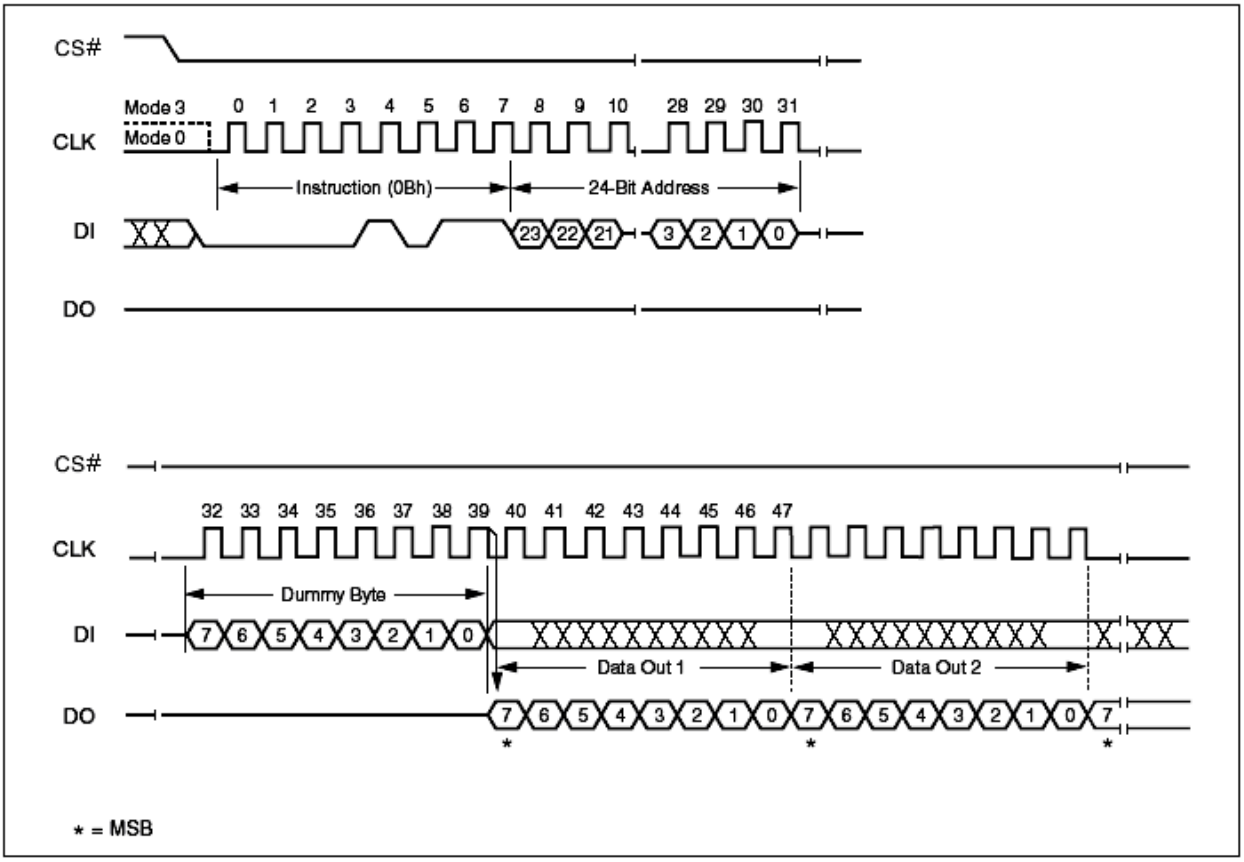
Read Data Bytes at Higher Speed (FAST_READ) (0Bh)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes at Higher Speed (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency F_R, during the falling edge of Serial Clock (CLK).

The instruction sequence is shown in Fast Read Instruction Sequence Diagram figure. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

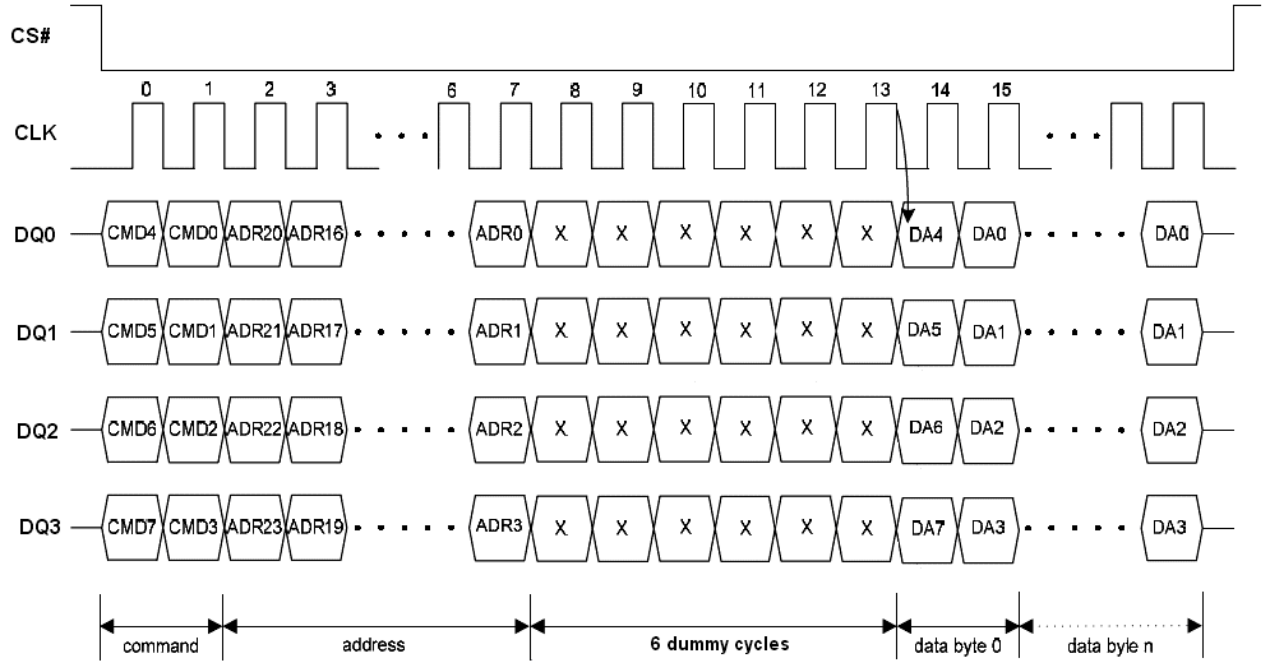
The Read Data Bytes at Higher Speed (FAST_READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed (FAST_READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

The instruction sequence is shown in Fast Read Instruction Sequence in QPI Mode figure while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.



Fast Read Instruction Sequence Diagram

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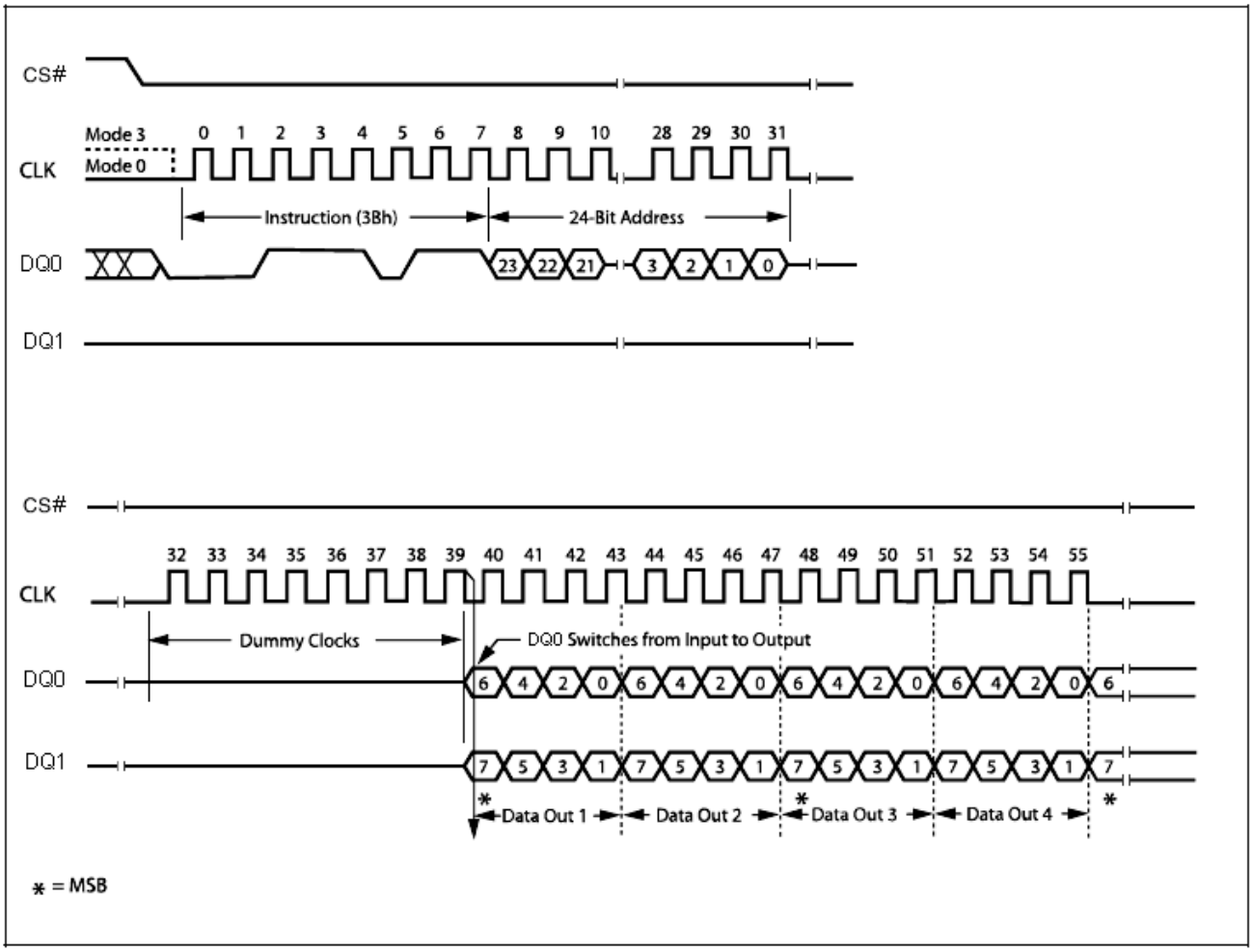
Fast Read Instruction Sequence in QPI Mode

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Dual Output Fast Read (3Bh)

The Dual Output Fast Read (3Bh) is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins, DQ_0 and DQ_1, instead of just DQ_0. This allows data to be transferred from the device at twice the rate of standard SPI devices. The Dual Output Fast Read instruction is ideal for quickly downloading code from to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Dual Output Fast Read instruction can operation at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding eight “dummy clocks after the 24-bit address as shown in Dual Output Fast Read Instruction Sequence Diagram figure. The dummy clocks allow the device’s internal circuits additional time for setting up the initial address. The input data during the dummy clock is “don’t care”. However, the DI pin should be high-impedance prior to the falling edge of the first data out clock.



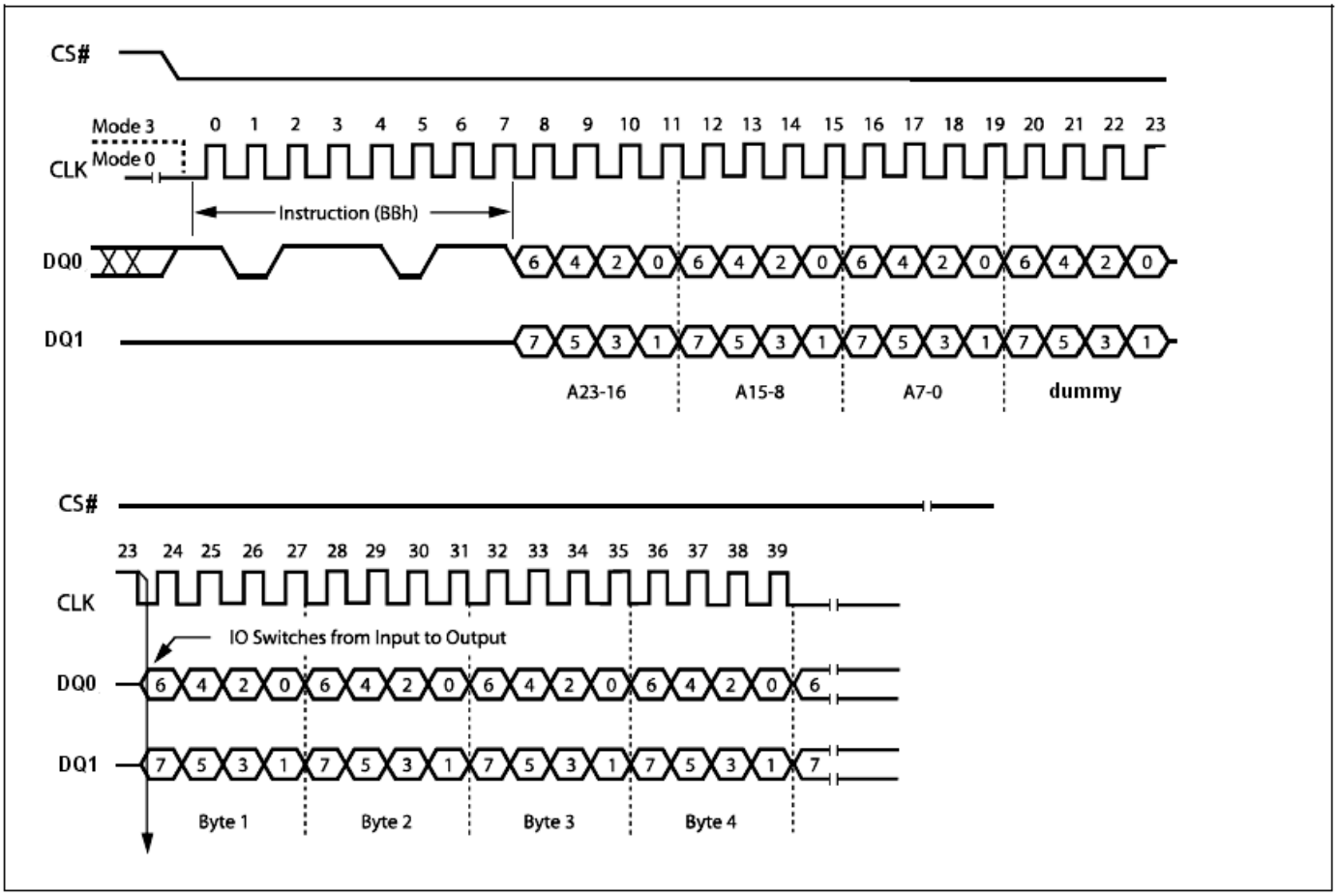
Dual Output Fast Read Instruction Sequence Diagram

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Dual Input / Output FAST_READ (BBh)

The Dual I/O Fast Read (BBh) instruction allows for improved random access while maintaining two IO pins, DQ_0 and DQ_1. It is similar to the Dual Output Fast Read (3Bh) instruction but with the capability to input the Address bits (A23-A0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

The Dual I/O Fast Read instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of CLK, and data of every two bits (interleave 2 I/O pins) shift out on the falling edge of CLK at a maximum frequency. The first address can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Dual I/O Fast Read instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing Dual I/O Fast Read instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit, as shown in Dual Input / Output Fast Read Instruction Sequence Diagram figure.



Dual Input / Output Fast Read Instruction Sequence Diagram

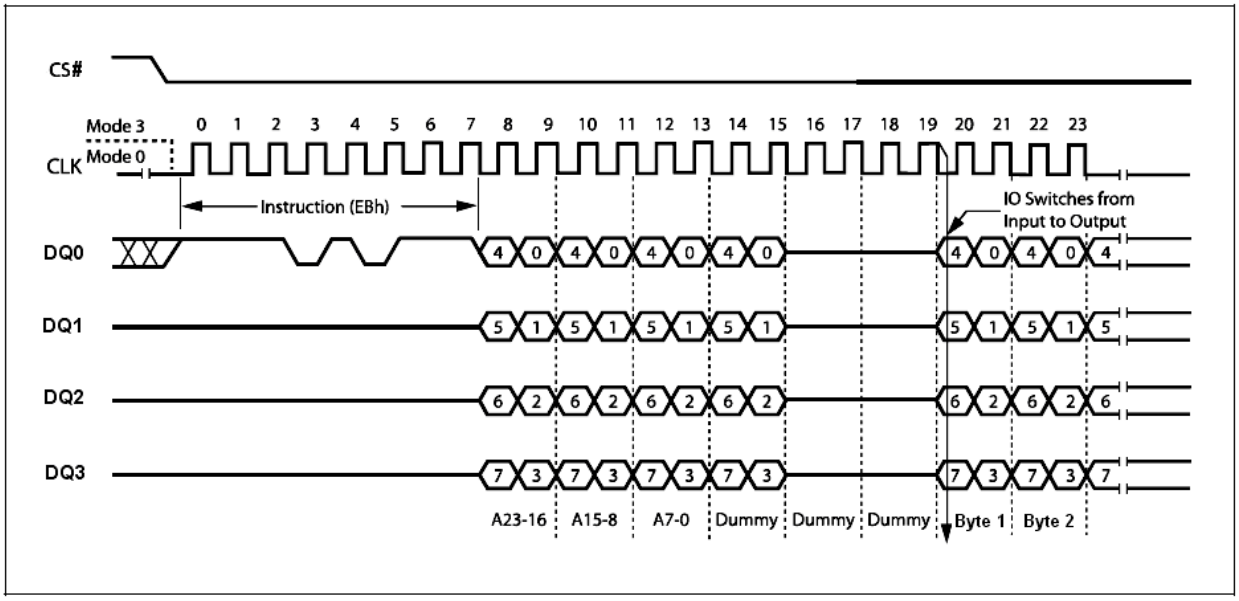
Quad Input / Output FAST_READ (EBh)

The Quad Input/Output FAST_READ (EBh) instruction is similar to the Dual I/O Fast Read (BBh) instruction except that address and data bits are input and output through four pins, DQ_0, DQ_1, DQ_2 and DQ_3 and six dummy clocks are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

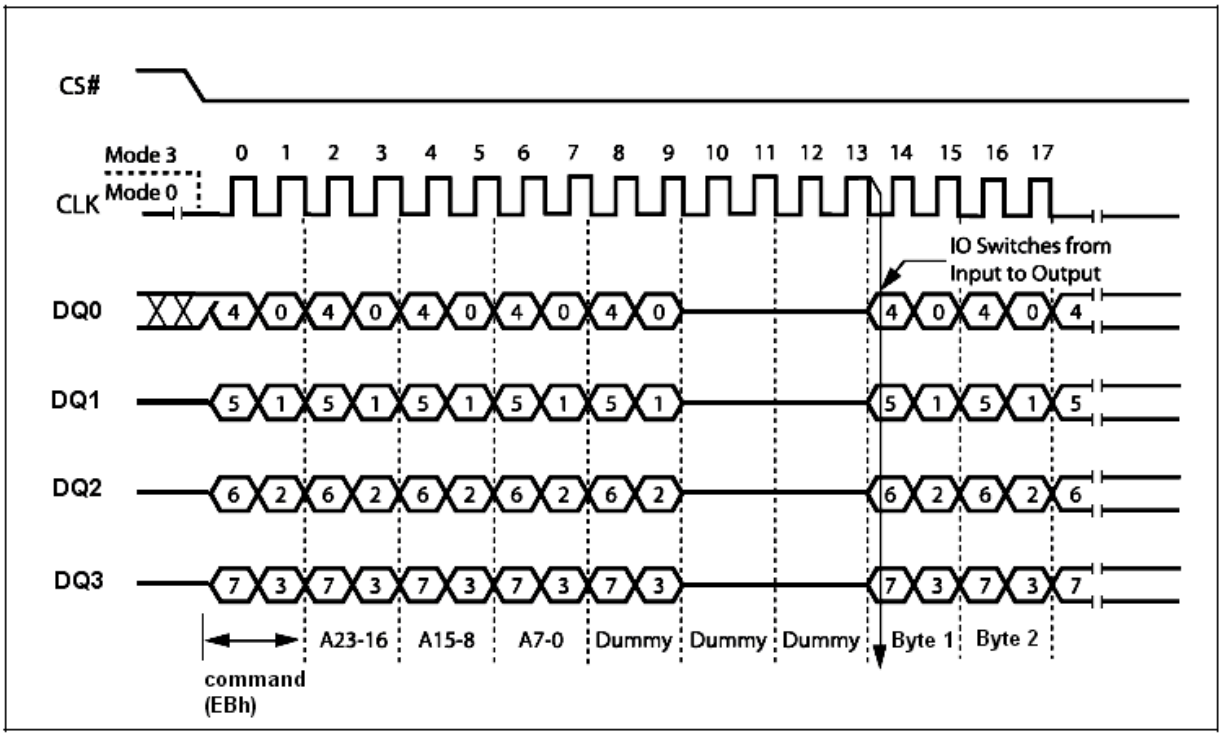
The Quad Input/Output FAST_READ (EBh) instruction enable quad throughput of Serial Flash in read mode. The address is latching on rising edge of CLK, and data of every four bits (interleave on 4 I/O pins) shift our on the falling edge of CLK at a maximum frequency F_R. The first address can be any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Quad Input/Output FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing Quad Input/Output FAST_READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing Quad Input/Output FAST_READ (EBh) instruction is: CS# goes low -> sending Quad Input/Output FAST_READ (EBh) instruction -> 24-bit address interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> 6 dummy cycles -> data out interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> to end Quad Input/Output FAST_READ (EBh) operation can use CS# to high at any time during data out, as shown in Quad Input / Output Fast Read Instruction Sequence Diagram figure.

The instruction sequence is shown in Quad Input / Output Fast Read Instruction Sequence in QPI Mode figure while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.



Quad Input / Output Fast Read Instruction Sequence Diagram



Quad Input / Output Fast Read Instruction Sequence in QPI Mode

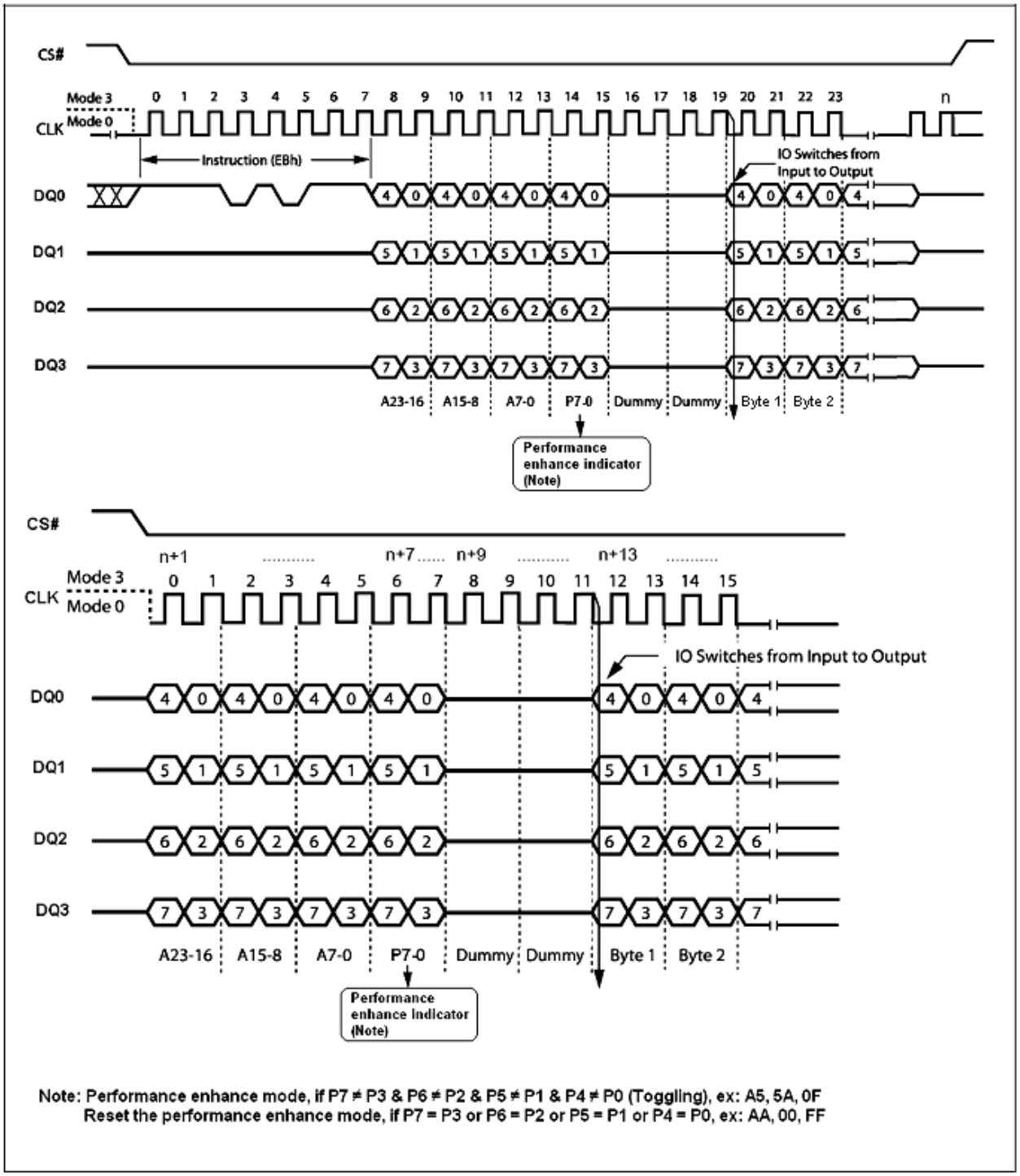
Another sequence of issuing Quad Input/Output FAST_READ (EBh) instruction especially useful in random access is : CS# goes low -> sending Quad Input/Output FAST_READ (EBh) instruction -> 24-bit address interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> performance enhance toggling bit P[7:0] -> 4 dummy cycles -> data out interleave on DQ_3, DQ_2, DQ_1 and DQ_0 till CS# goes high -> CS# goes low (reduce Quad Input/Output FAST_READ (EBh) instruction) -> 24-bit access address, as shown in Quad Input/Output Fast Read Enhance Performance Mode Sequence Diagram figure.

In the performance – enhancing mode, P[7:4] must be toggling with P[3:0] ; likewise P[7:0] = A5h, 5Ah, F0h or 0Fh can make this mode continue and reduce the next Quad Input/Output FAST_READ (EBh) instruction. Once P[7:4] is no longer toggling with P[3:0] ; likewise P[7:0] = FFh, 00h, AAh or 55h. And afterwards CS# is raised, the system then will escape from performance enhance mode and return to normal operation.

While Program/ Erase/ Write Status Register is in progress, Quad Input/Output FAST_READ (EBh) instruction is rejected without impact on the Program/ Erase/ Write Status Register current cycle.

The instruction sequence is shown in Quad Input/Output Fast Read Enhance Performance Mode Sequence in QPI Mode figure while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

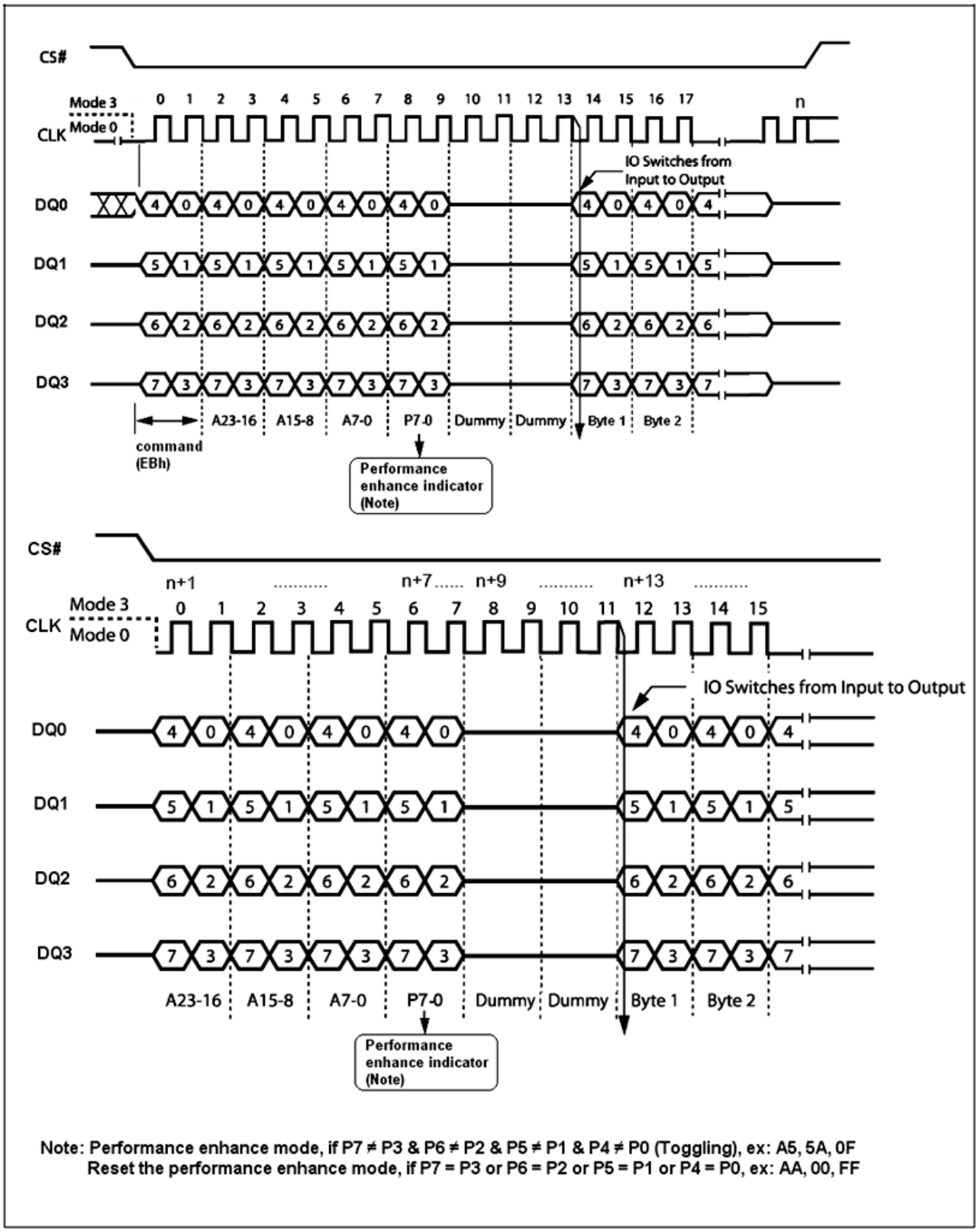
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Note: Performance enhance mode, if P7 ≠ P3 & P6 ≠ P2 & P5 ≠ P1 & P4 ≠ P0 (Toggling), ex: A5, 5A, 0F
Reset the performance enhance mode, if P7 = P3 or P6 = P2 or P5 = P1 or P4 = P0, ex: AA, 00, FF

Quad Input/Output Fast Read Enhance Performance Mode Sequence Diagram

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Note: Performance enhance mode, if P7 ≠ P3 & P6 ≠ P2 & P5 ≠ P1 & P4 ≠ P0 (Toggling), ex: A5, 5A, 0F
Reset the performance enhance mode, if P7 = P3 or P6 = P2 or P5 = P1 or P4 = P0, ex: AA, 00, FF

Quad Input/Output Fast Read Enhance Performance Mode Sequence in QPI Mode

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Read Burst (0Ch)

This device supports Read Burst with wrap in both SPI and QPI mode. To execute a Read Burst with wrap operation the host drivers CS# low, and sends the Read Burst with wrap (0Ch) command cycle, followed by three address bytes and one dummy byte (8 clocks) in SPI mode (Read Burst Instruction Sequence Diagram figure) or default two dummy bytes (4 clocks) in QPI mode (Read Burst Instruction Sequence Diagram in QPI mode figure).

After the dummy byte, the device outputs data on the falling edge of the CLK signal starting from the specific address location. The data output stream is continuous through all addresses until terminated by a low-to high transition of CS# signal.

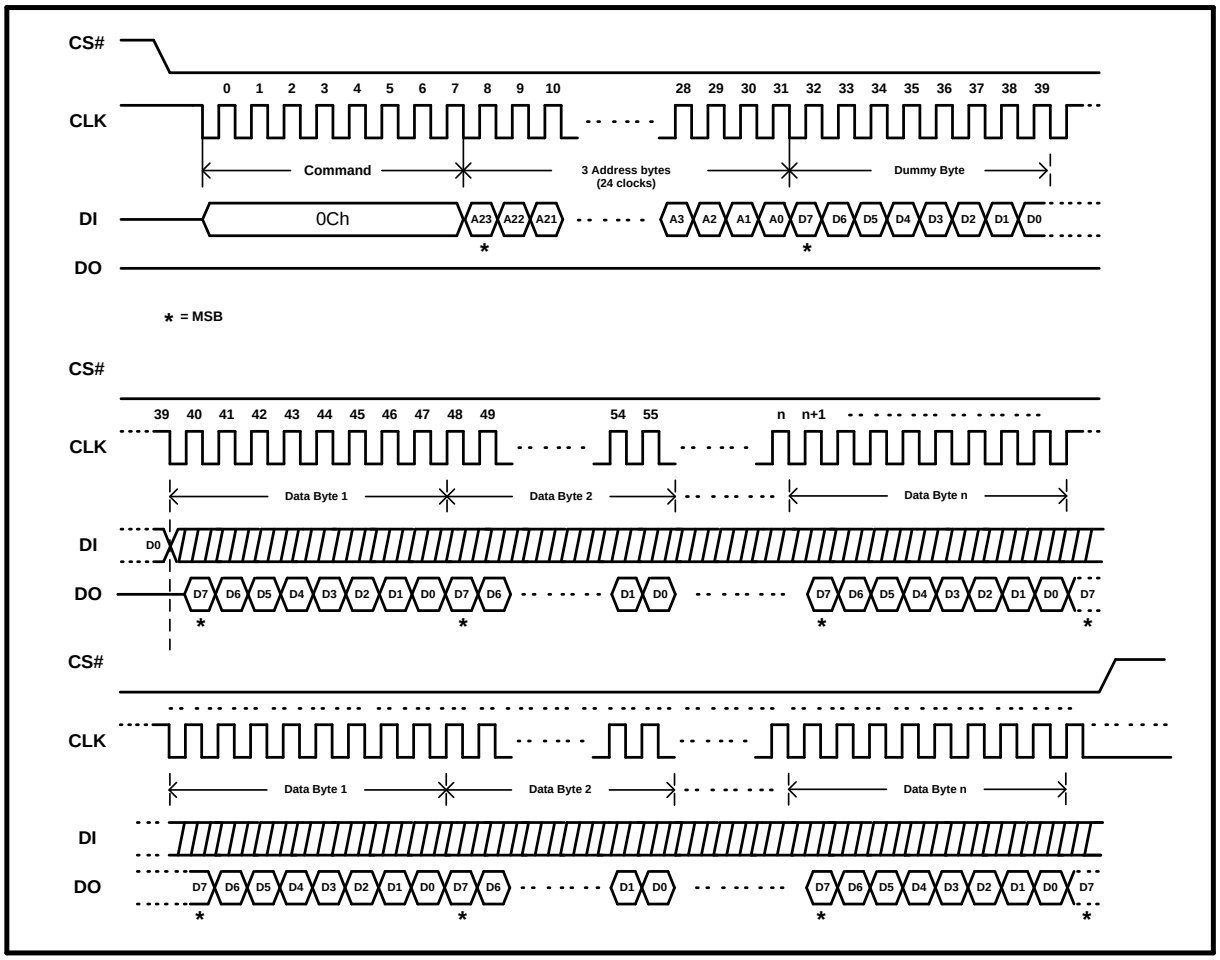
During Read Burst, the internal address point automatically increments until the last byte of the burst reached, then jumps to first byte of the burst. All bursts are aligned to addresses within the burst length, see Burst Address Range table. For example, if the burst length is 8 bytes, and the start address is 06h, the burst sequence should be: 06h, 07h, 00h, 01h, 02h, 03h, 04h, 05, 06, etc. The pattern would repeat until the command was terminated by pulling CS# as high status.

The instruction sequence is shown in Read Burst Instruction Sequence Diagram in QPI mode figure while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

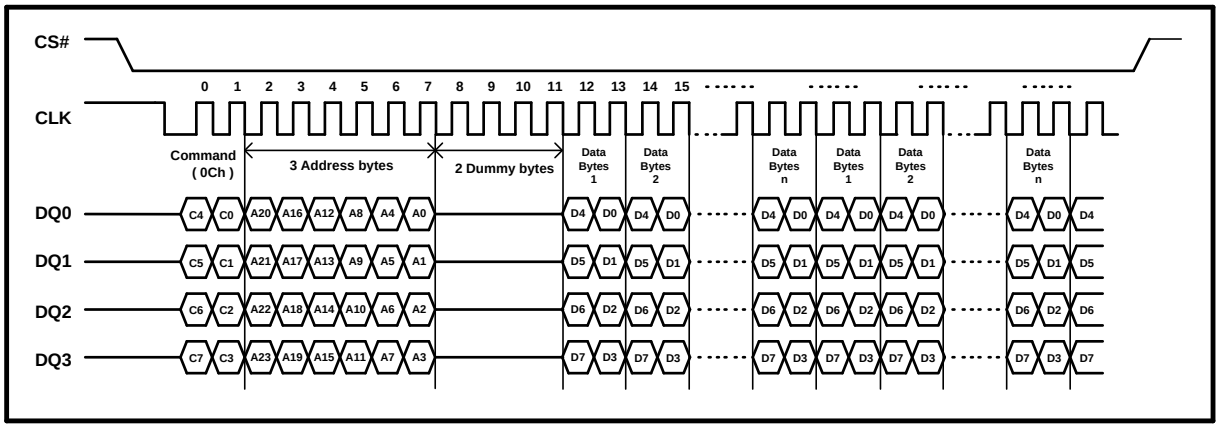
Burst Address Range

Burst length	Burst wrap (A[7:A0]) address range
8 Bytes (default)	00-07H, 08-0FH, 10-17H, 18-1FH...
16 Bytes	00-0FH, 10-1FH, 20-2FH, 30-3FH...
32 Bytes	00-1FH, 20-3FH, 40-5FH, 60-7FH...
64 Bytes	00-3FH, 40-7FH, 80-BFH, C0-FFH

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Read Burst Instruction Sequence Diagram



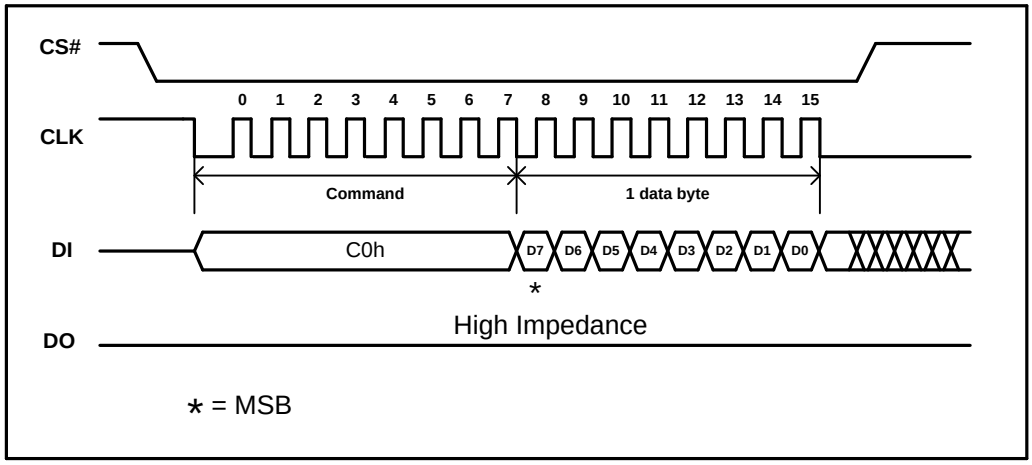
Read Burst Instruction Sequence Diagram in QPI mode

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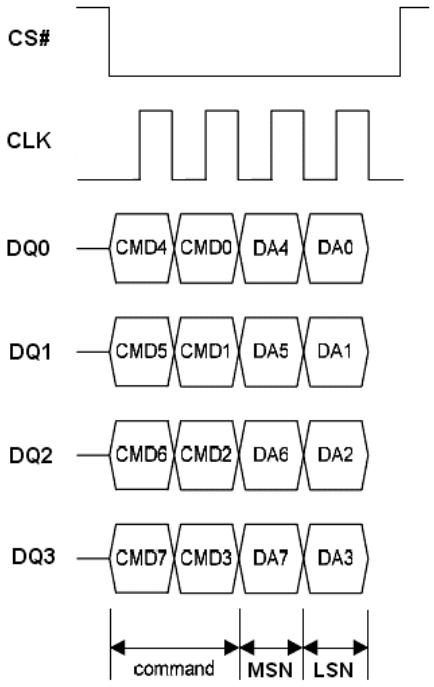
Write Status Register 3 (C0h)

The Write Status Register 3 (C0h) command can be used to set output drive strength in I/O pins, burst length and the number of dummy byte in high performance read. To set the output drive strength, burst length and the number of dummy byte to host driver CS# low, sends the Write Status Register 3 (C0h) and one data byte, then drivers CS# high, After power-up or reset, the output drive strength is set to full drive (00b) and the dummy byte is set to 3 bytes (00b), please refer to Status Register 3 Bit Locations table for Status Register 3 data and Write Status Register 3 Instruction Sequence Diagram figure for the sequence. In QPI mode, a cycle is two nibbles, or two clocks, long, most significant nibble first.

The instruction sequence is shown in Write Status Register 3 Instruction Sequence Diagram in QPI mode figure while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.



Write Status Register 3 Instruction Sequence Diagram



Note: MSN = Most Significant Nibble,
LSN = Least Significant Nibble

Write Status Register 3 Instruction Sequence Diagram in QPI mode

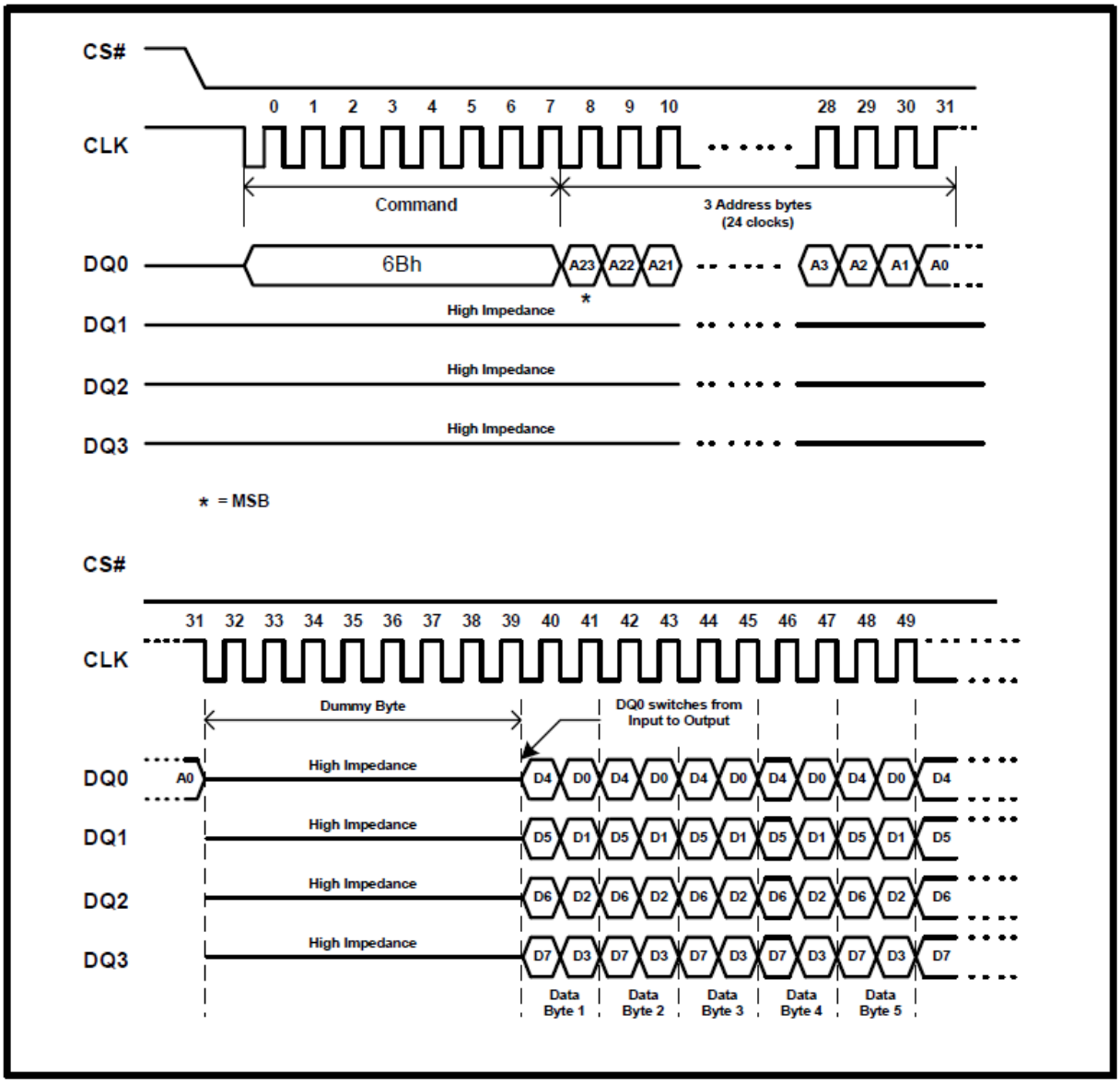
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Quad Output Fast Read (6Bh)

The Quad Output Fast Read (6Bh) instruction is similar to the Dual Output Fast Read (3Bh) instruction except that data is output through four pins, DQ0, DQ1, DQ2 and DQ3 and eight dummy clocks are required prior to the data output. The Quad Output dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

The Quad Output Fast Read (6Bh) address is latching on rising edge of CLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of CLK at a maximum frequency FR. The first address can be any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Quad Output Fast Read instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing Quad Output Fast Read (6Bh) instruction is: CS# goes low -> sending Quad Output Fast Read (6Bh) instruction -> 24-bit address on DQ0 -> 8 dummy clocks -> data out interleave on DQ3, DQ2, DQ1 and DQ0 -> to end Quad Output Fast Read (6Bh) operation can use CS# to high at any time during data out, as shown in Quad Output Fast Read Instruction Sequence Diagram figure. The WP# (DQ2) and NC(DQ3) need to drive high before address input if HDEN bit in Status Register4 is 1 and WPDIS bit is 0.



Quad Output Fast Read Instruction Sequence Diagram

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Page Program (PP) (02h)

The Page Program (PP) instruction allows bytes to be programmed in the memory. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data Input (DI). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

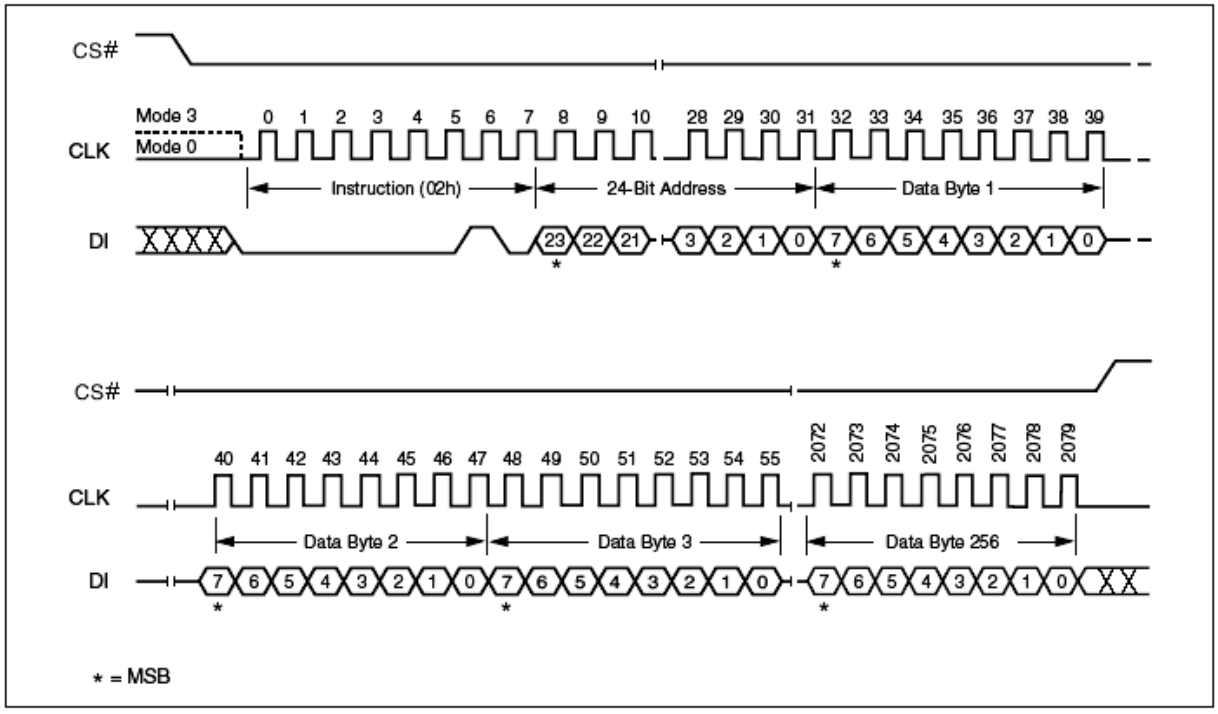
The instruction sequence is shown in Page Program Instruction Sequence Diagram figure. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

Chip Select (CS#) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed.

As soon as Chip Select (CS#) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

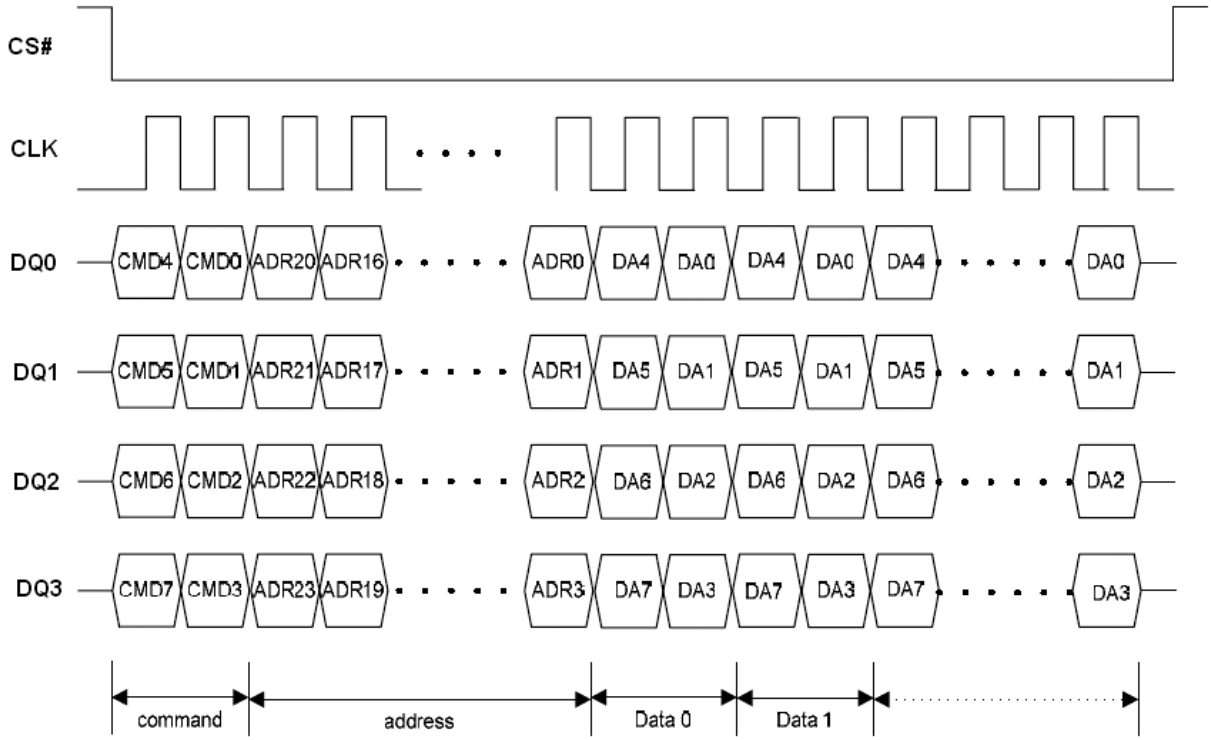
A Page Program (PP) instruction applied to a page which is protected by the Block Protect (CMP, 4KBL, TB, BP2, BP1, BP0) bits (see Protected Area Sizes Sector Organization table) and Enable boot lock function is not executed.

The instruction sequence is shown in Program Instruction Sequence in QPI Mode figure while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.



Page Program Instruction Sequence Diagram

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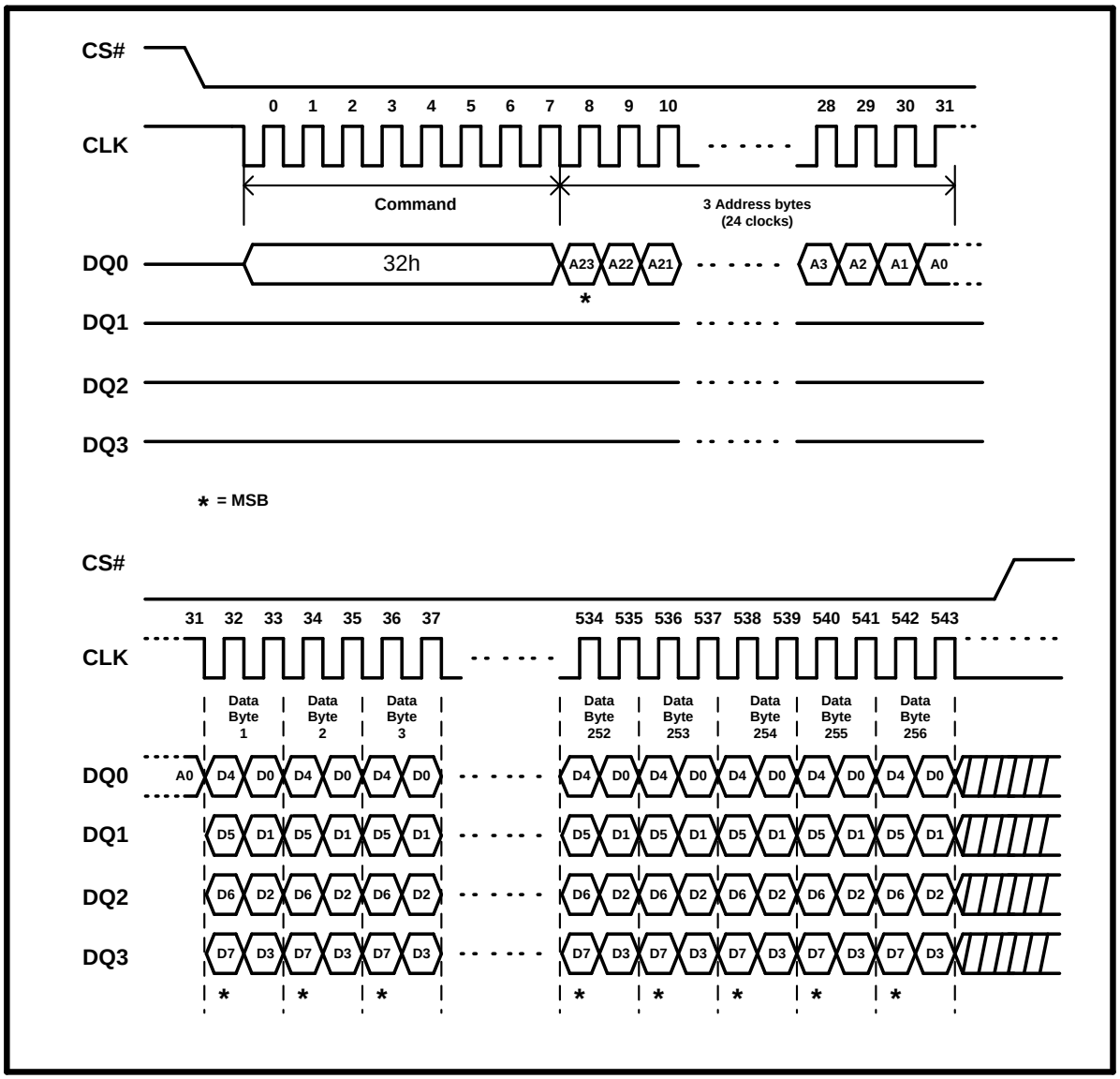
Program Instruction Sequence in QPI Mode

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Quad Input Page Program (QPP) (32h)

The Quad Page Program (QPP) instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: DQ_0, DQ_1, DQ_2 and DQ_3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds < 5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program (QPP) the WP# & Hold# Disable (WHDIS) bit in Status Register must be set to 1. A Write Enable instruction must be executed before the device will accept the Quad Page Program (QPP) instruction (SR1, WEL=1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “32h” followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program (QPP) are identical to standard Page Program. The Quad Page Program (QPP) instruction sequence is shown in Quad Input Page Program Instruction Sequence Diagram (SPI Mode only) figure.



Quad Input Page Program Instruction Sequence Diagram (SPI Mode only)

Sector Erase (SE) (20h)

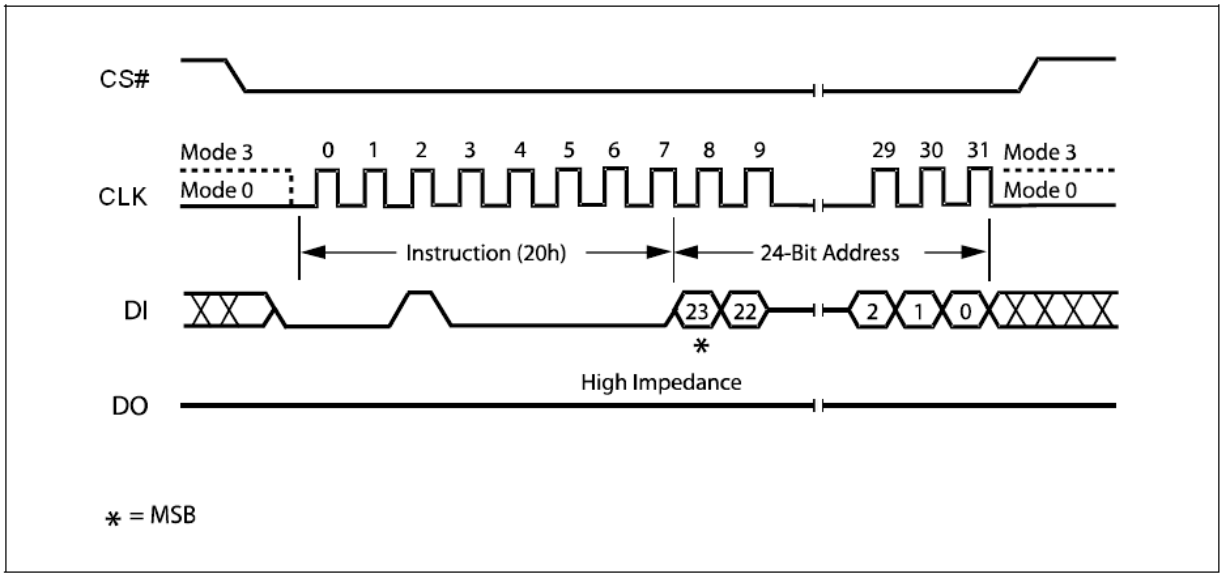
The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Sector Erase (SE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three address bytes on Serial Data Input (DI). Any address inside the Sector (see Uniform Block Sector Architecture table) is a valid address for the Sector Erase (SE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Sector Erase Instruction Sequence Diagram figure. Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Sector Erase (SE) instruction applied to a sector which is protected by the Block Protect (CMP, 4KBL, TB, BP2, BP1, BP0) bits (see Protected Area Sizes Sector Organization table) and enable boot lock function is not executed.

The instruction sequence is shown in Half Block/Block/Sector Erase Instruction Sequence in QPI Mode figure while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.



Sector Erase Instruction Sequence Diagram

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32KB Half Block Erase (HBE) (52h)

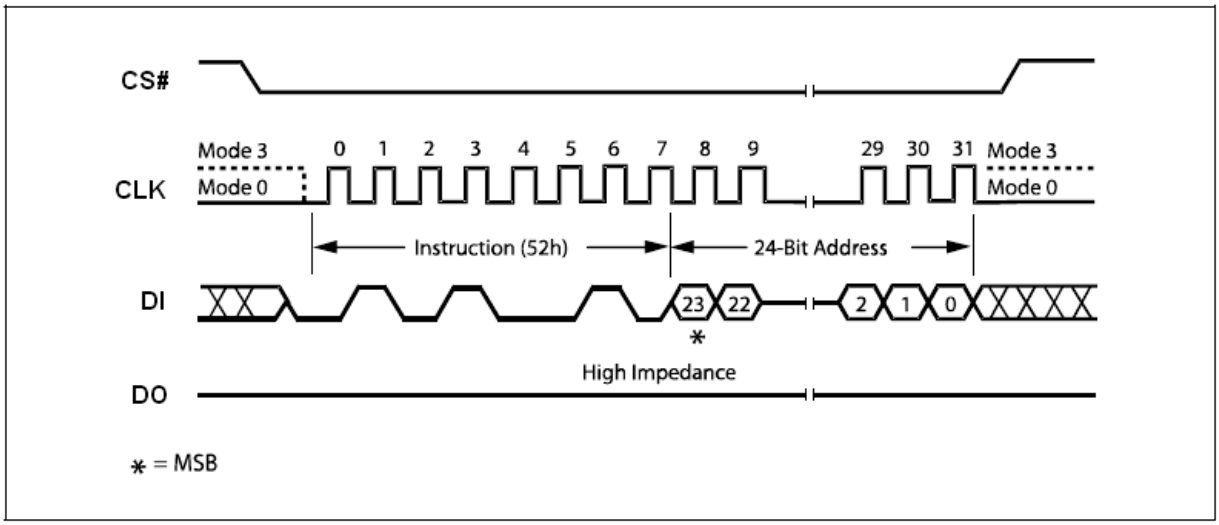
The Half Block Erase (HBE) instruction sets to 1 (FFh) all bits inside the chosen block. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Half Block Erase (HBE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three address bytes on Serial Data Input (DI). Any address inside the Block (see Uniform Block Sector Architecture table) is a valid address for the Half Block Erase (HBE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in 32KB Half Block Erase Instruction Sequence Diagram figure. Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Half Block Erase (HBE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Half Block Erase cycle (whose duration is t_{HBE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Half Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Half Block Erase (HBE) instruction applied to a block which is protected by the Block Protect (CMP, 4KBL, TB, BP2, BP1, BP0) bits (see Protected Area Sizes Sector Organization table) and enable boot lock function is not executed.

The instruction sequence is shown in Half Block/Block/Sector Erase Instruction Sequence in QPI Mode figure while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.



32KB Half Block Erase Instruction Sequence Diagram

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64KB Block Erase (BE) (D8h)

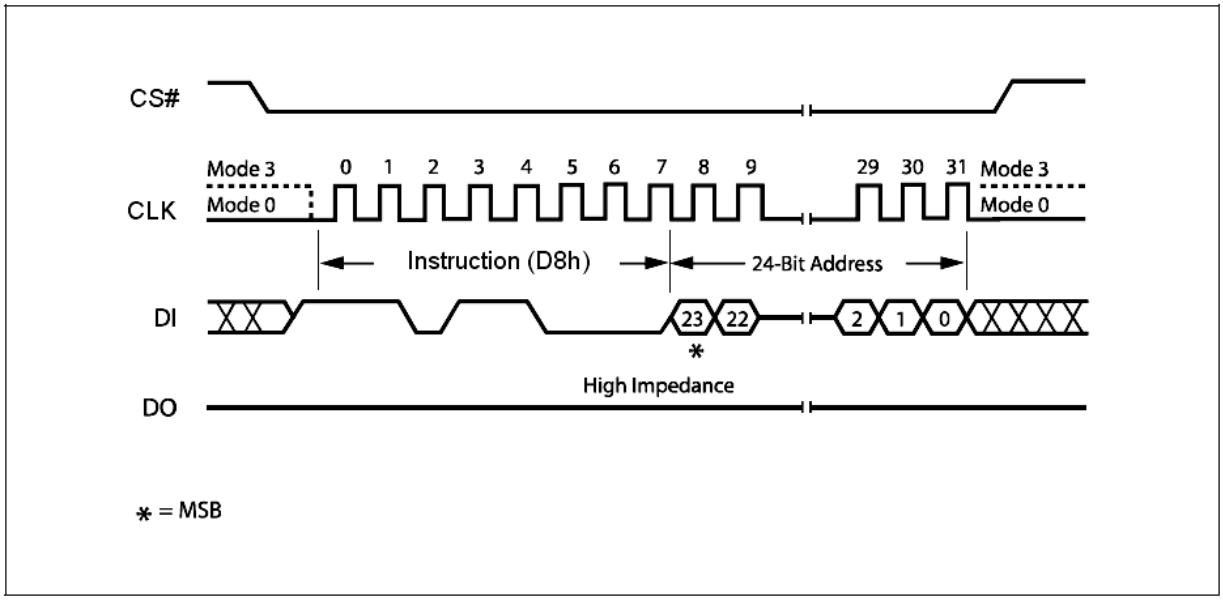
The Block Erase (BE) instruction sets to 1 (FFh) all bits inside the chosen block. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Block Erase (BE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three address bytes on Serial Data Input (DI). Any address inside the Block (see Uniform Block Sector Architecture table) is a valid address for the Block Erase (BE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in 64KB Block Erase Instruction Sequence Diagram figure. Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Block Erase (BE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

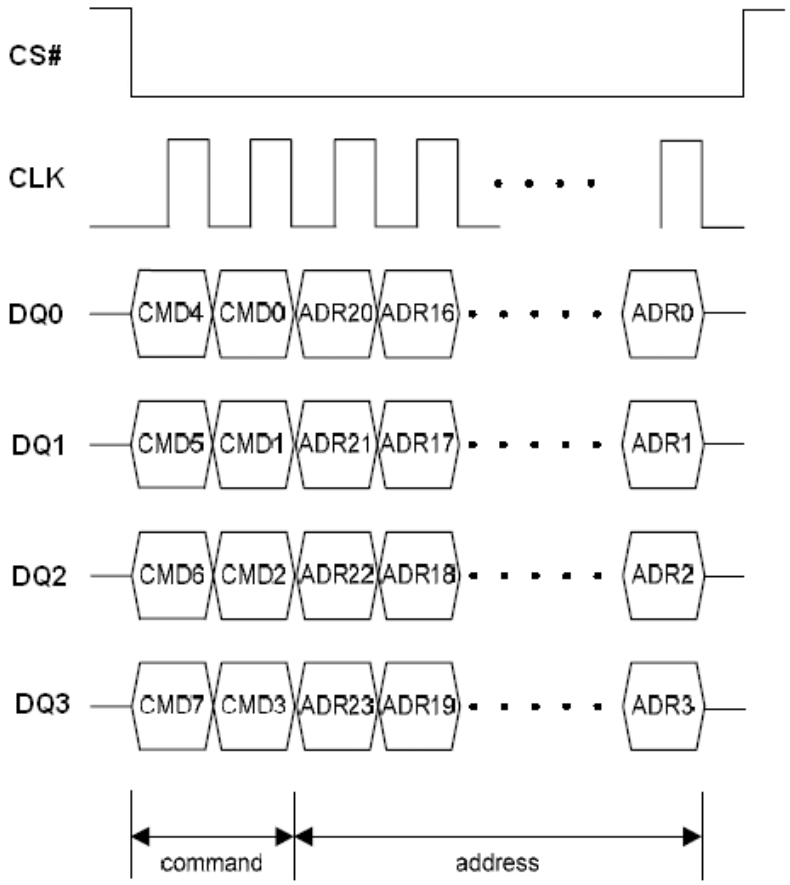
A Block Erase (BE) instruction applied to a block which is protected by the Block Protect (CMP, 4KBL, TB, BP2, BP1, BP0) bits (see Protected Area Sizes Sector Organization table) and enable boot lock function is not executed.

The instruction sequence is shown in Half Block/Block/Sector Erase Instruction Sequence in QPI Mode figure while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.



64KB Block Erase Instruction Sequence Diagram

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Half Block/Block/Sector Erase Instruction Sequence in QPI Mode

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Chip Erase (CE) (C7h/60h)

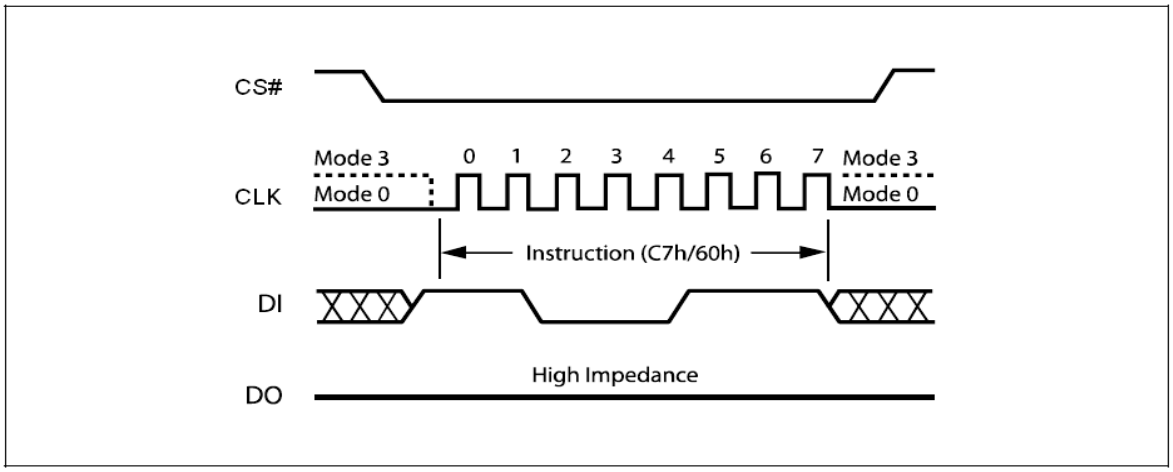
The Chip Erase (CE) instruction sets all bits to 1 (FFh). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Chip Erase (CE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (DI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

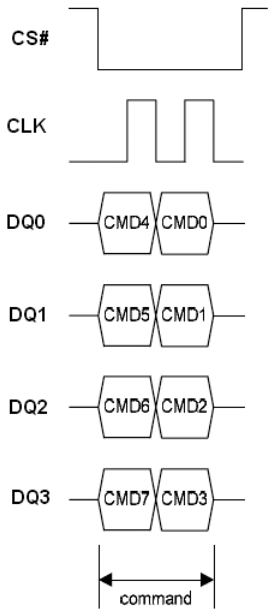
The instruction sequence is shown in Chip Erase Instruction Sequence Diagram figure. Chip Select (CS#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Chip Erase instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

The Chip Erase (CE) instruction is ignored if one or more blocks are protected.

The instruction sequence is shown in Chip Erase Sequence in QPI Mode figure while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.



Chip Erase Instruction Sequence Diagram



Chip Erase Sequence in QPI Mode

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Deep Power-down (DP) (B9h)

Executing the Deep Power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase instructions.

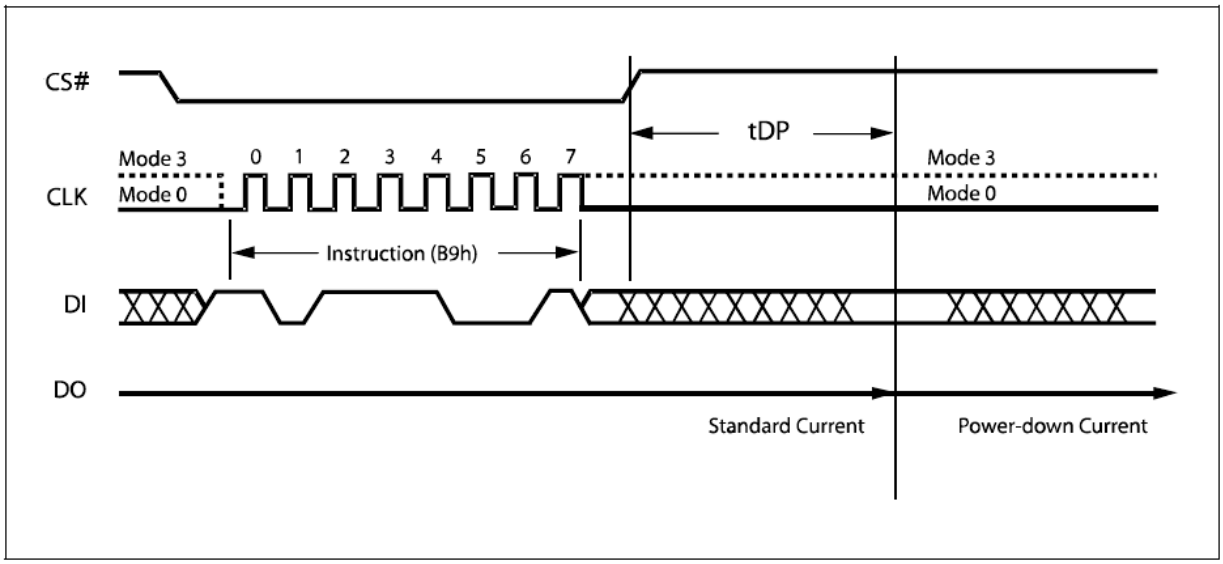
Driving Chip Select (CS#) High deselects the device, and puts the device in the Standby mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-down mode. The Deep Power-down mode can only be entered by executing the Deep Power-down (DP) instruction, to reduce the standby current (from I_{CC1} to I_{CC2}, as specified in DC Characteristics table.)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Device ID (RDI) instruction. This releases the device from this mode. The Release from Deep Power-down and Read Device ID (RDI) instruction also allows the Device ID of the device to be output on Serial Data Output (DO).

The Deep Power-down mode automatically stops at Power-down, and the device always Powers-up in the Standby mode. The Deep Power-down (DP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (DI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Deep Power-down Instruction Sequence Diagram figure. Chip Select (CS#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Deep Power-down (DP) instruction is not executed. As soon as Chip Select (CS#) is driven High, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-down mode is entered.

Any Deep Power-down (DP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.



Deep Power-down Instruction Sequence Diagram

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Release from Deep Power-down and Read Device ID (RDI)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Device ID (RDI) instruction. Executing this instruction takes the device out of the Deep Power-down mode.

Please note that this is not the same as, or even a subset of, the JEDEC 16-bit Electronic Signature that is read by the Read Identifier (RDID) instruction. The old-style Electronic Signature is supported for reasons of backward compatibility, only, and should not be used for new designs. New designs should, instead, make use of the JEDEC 16-bit Electronic Signature, and the Read Identifier (RDID) instruction.

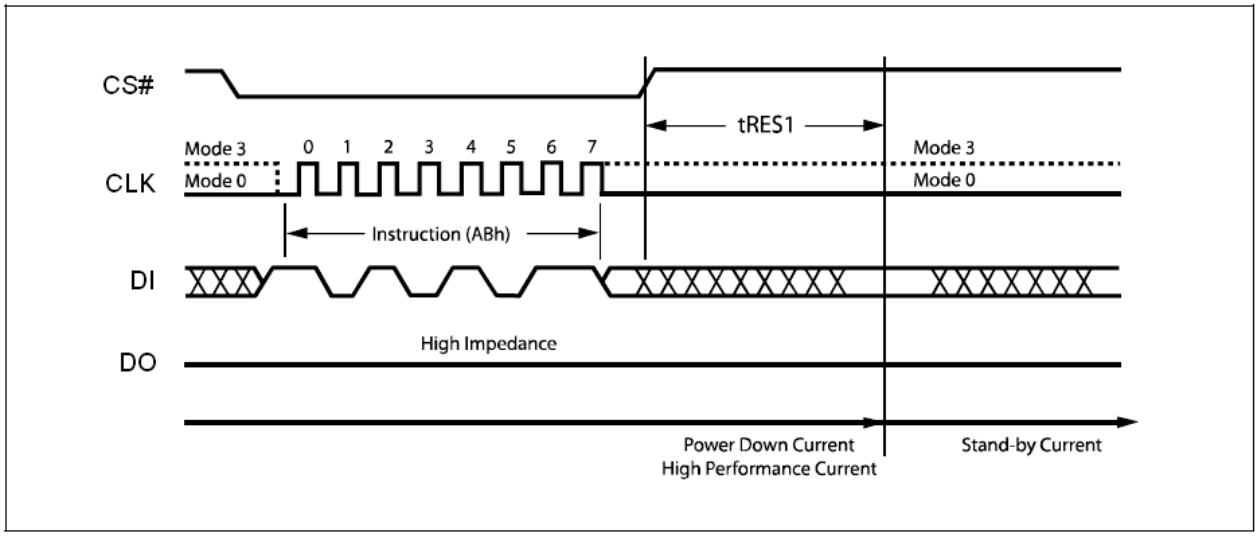
When used only to release the device from the power-down state, the instruction is issued by driving the CS# pin low, shifting the instruction code “ABh” and driving CS# high as shown in Release Power-down Instruction Sequence Diagram figure. After the time duration of t_{RES1} (See AC Characteristics) the device will resume normal operation and other instructions will be accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the CS# pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Release Power-down / Device ID Instruction Sequence Diagram figure. The Device ID value for the device are listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving CS# high.

When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Standby Power mode is delayed by t_{RES2}, and Chip Select (CS#) must remain High for at least t_{RES2} (max), as specified in AC Characteristics table. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

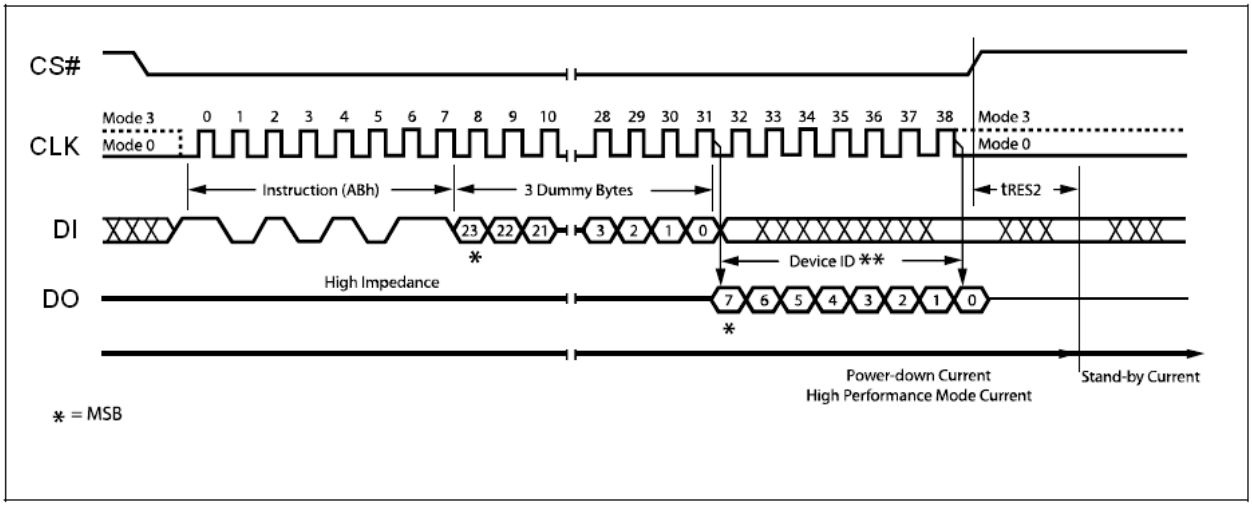
Except while an Erase, Program or Write Status Register cycle is in progress, the Release from Deep Power-down and Read Device ID (RDI) instruction always provides access to the 8bit Device ID of the device, and can be applied even if the Deep Power-down mode has not been entered.

Any Release from Deep Power-down and Read Device ID (RDI) instruction while an Erase, Program or Write Status Register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.



Release Power-down Instruction Sequence Diagram

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Release Power-down / Device ID Instruction Sequence Diagram

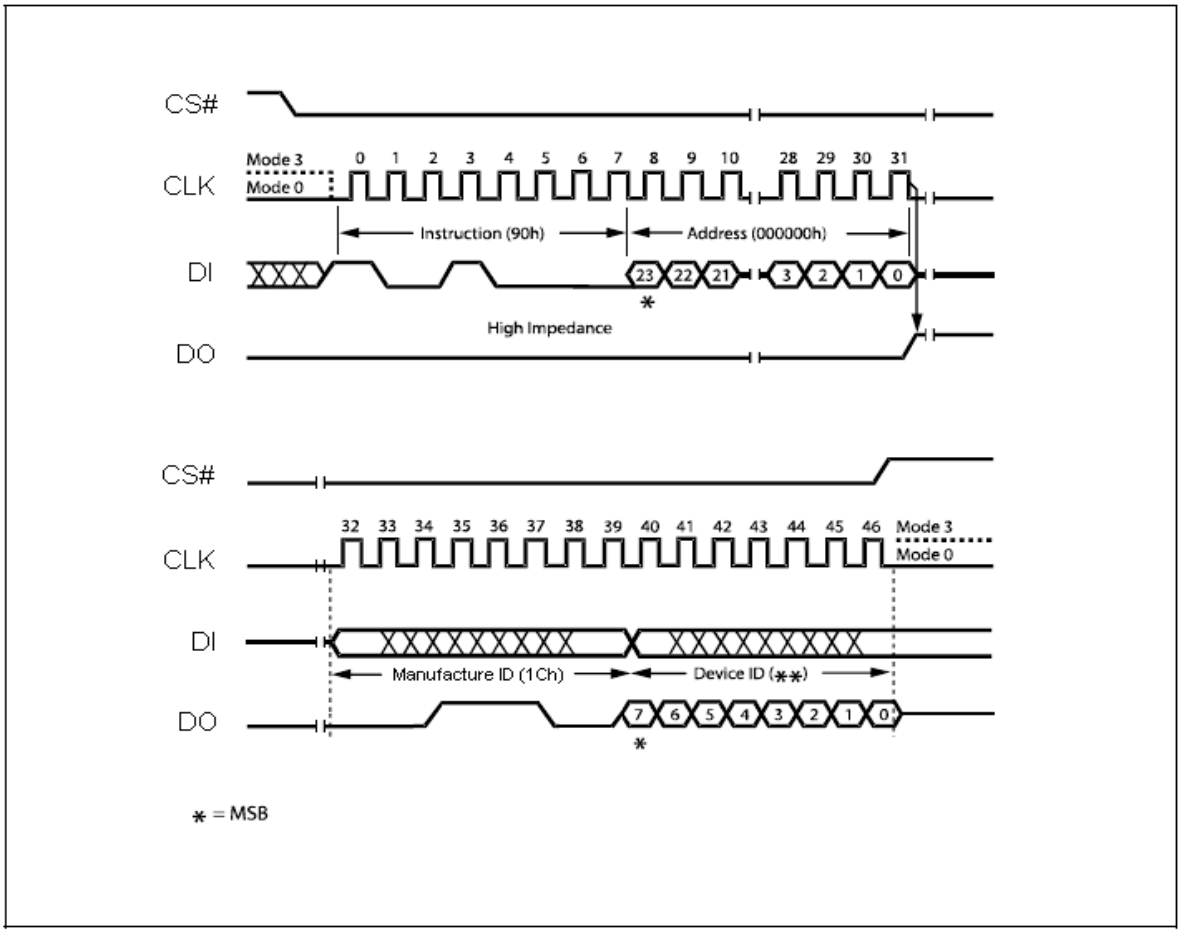
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Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

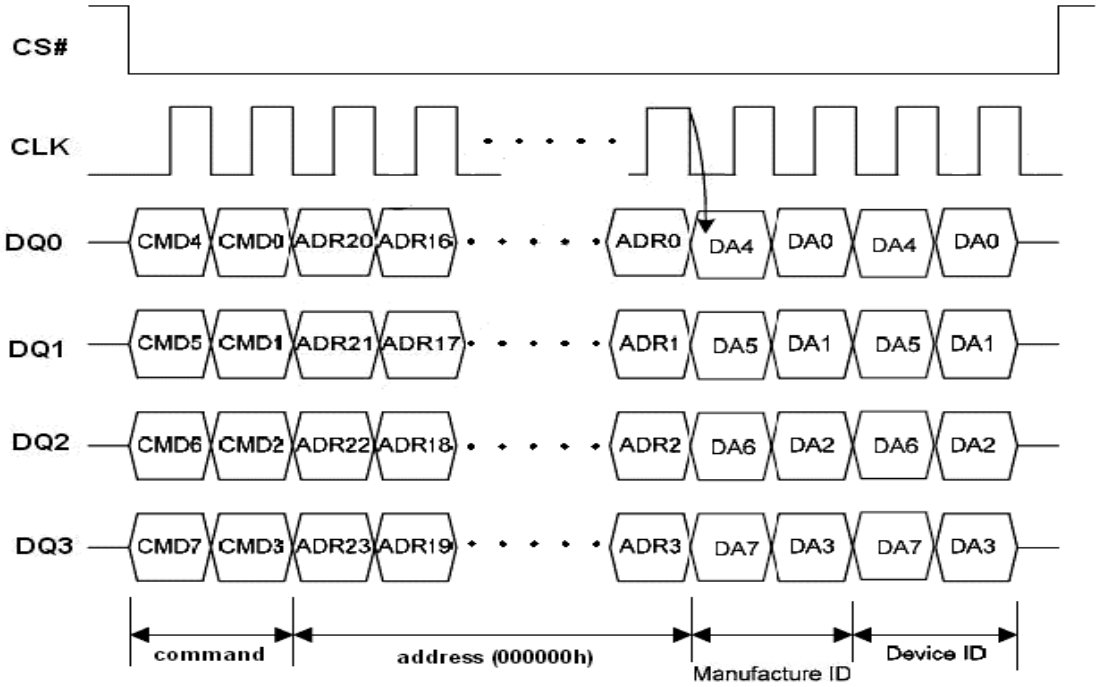
The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code “90h” followed by a 24-bit address of 000000h. After which, the Manufacturer ID for Eon (1Ch) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Read Manufacturer / Device ID Diagram figure. The Device ID values for the device are listed in Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first

The instruction sequence is shown in Read Manufacturer / Device ID Diagram in QPI Mode figure while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.



Read Manufacturer / Device ID Diagram

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Read Manufacturer / Device ID Diagram in QPI Mode

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Read Identification (RDID) (9Fh)

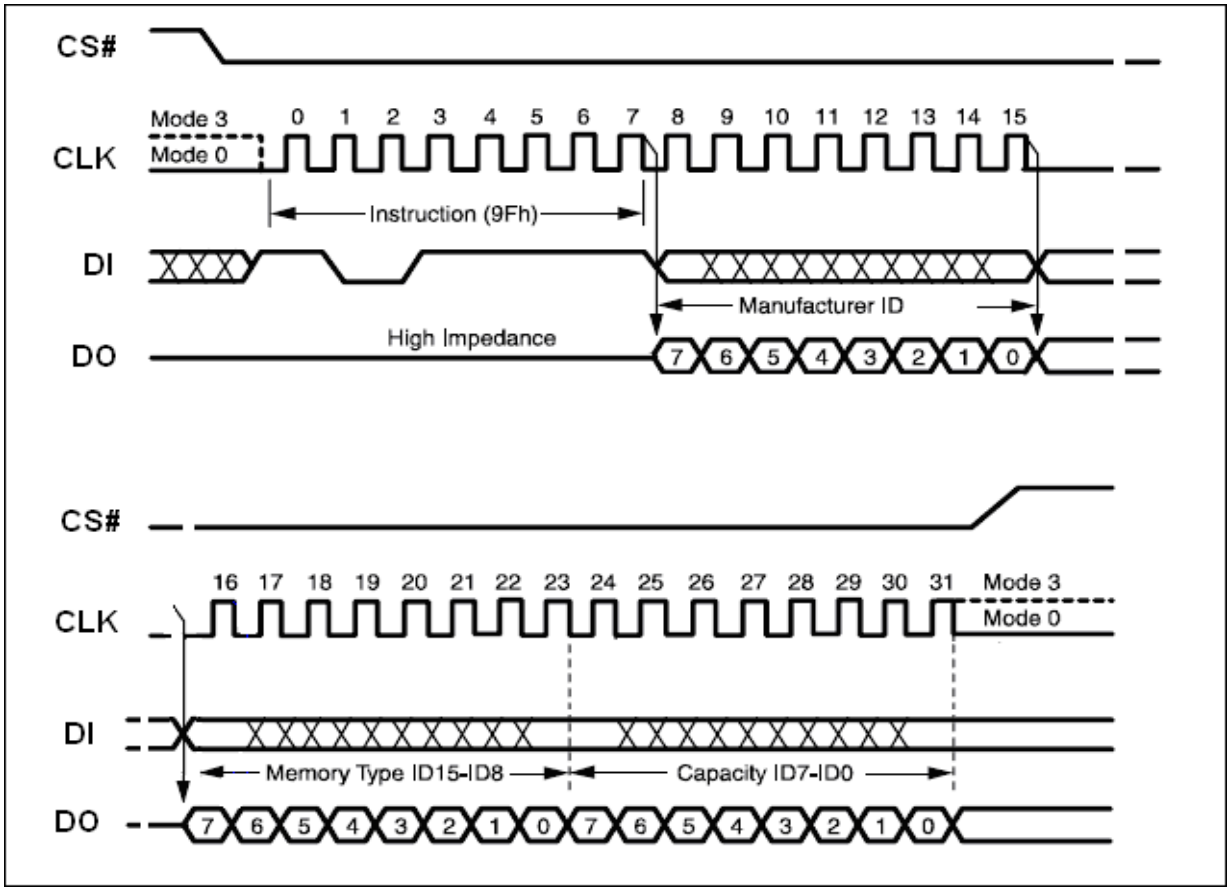
The Read Identification (RDID) instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte.

Any Read Identification (RDID) instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) instruction should not be issued while the device is in Deep Power down mode.

The device is first selected by driving Chip Select Low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The instruction sequence is shown in Read Identification (RDID) figure. The Read Identification (RDID) instruction is terminated by driving Chip Select High at any time during data output.

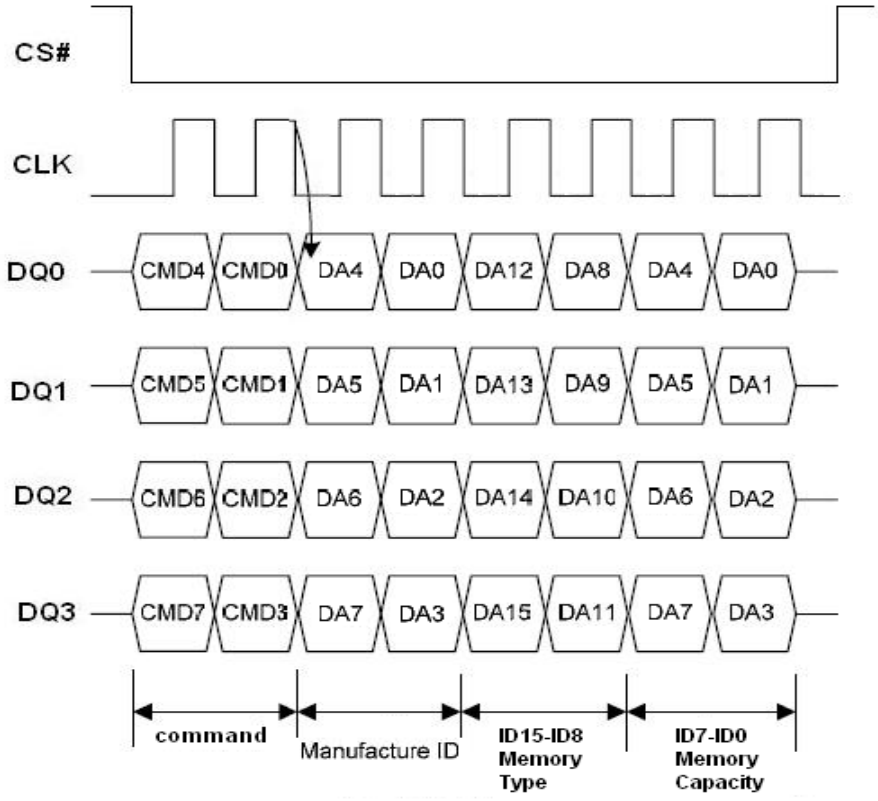
When Chip Select is driven High, the device is put in the Standby Power mode. Once in the Standby Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

The instruction sequence is shown in Read Identification (RDID) in QPI Mode figure while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.



Read Identification (RDID)

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Read Identification (RDID) in QPI Mode

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Enter OTP Mode (3Ah)

This Flash support OTP mode to enhance the data protection, user can use the Enter OTP mode (3Ah) command for entering this mode. In OTP mode, the Status Register SR7 bit is served as SPL0 bit; SR6 bit is served as WHDIS bit; SR4 bit is served as CMP bit, SR3 bit is served as EBL bit, SR2 bit is served as SPL1 bit, SR1 bit is served as SPL2 bit and SR0 bit is served as WIP bit. They can be read by RDSR command.

This Flash has extra 3 OTP lockable security sectors, each security sector size is 512bytes, user must issue ENTER OTP MODE command to read, program or erase OTP sectors. After entering OTP mode, the OTP lockable security sectors are mapping to sector 511, 510, and 509, SRP bit becomes SPL0 bit, BP0 bit becomes SPL1 bit, WEL bit becomes SPL2 bit. The Chip Erase, Block Erase and Half Block Erase commands are also disabled.

In OTP mode, user can read other blocks, but program/erase other blocks only allowed when they are not protected by Block Protect (CMP, 4KBL, TB, BP2, BP1, BP0) bits and Block Lock feature. The security sectors can only be erased by Sector Erase (20h) command. The Chip Erase (C7h/60h), 64k Block Erase (D8h) and 32K Half Block Erase (52h) commands are disable in OTP mode.

OTP Sector Address

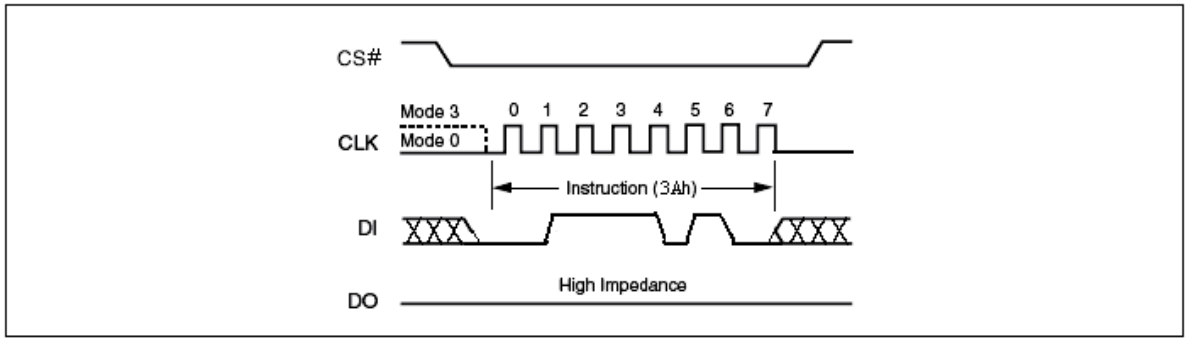
Sector	Sector Size	Address Range
511	512 byte	1FF000h～1FF1FFh
510	512 byte	1FE000h～1FE1FFh
509	512 byte	1FD000h～1FD1FFh

Note:

1. The OTP lockable security sectors are mapping to sector 511, 510, and 509.
2. While user wants to read data in SA509, SA510 and SA511, please exit OTP mode first.

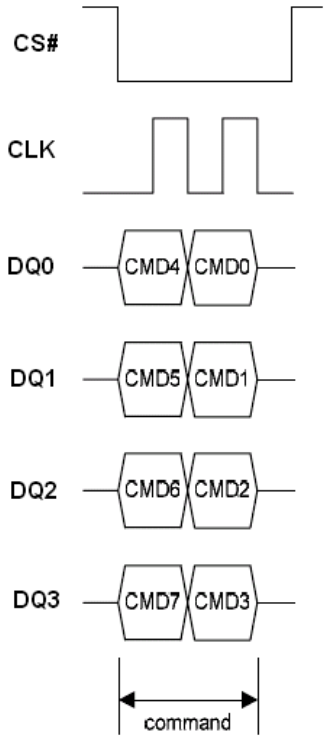
The Enable Boot Lock feature is configured in OTP mode. It enables user to lock the 4KB BL bit on the top/bottom of the device for protection. This feature is activated by programming the EBL bit to '1'. WRSR command is used to program SPL0 bit, WHDIS bit, CMP, EBL, SPL1 bit, and SPL2 bit to '1', but these bits only can be programmed once. User can use WRDI (04h) command to exit OTP mode.

The instruction sequence is shown in Enter OTP Mode Sequence in QPI Mode figure while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.



Enter OTP Mode Sequence

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Enter OTP Mode Sequence in QPI Mode

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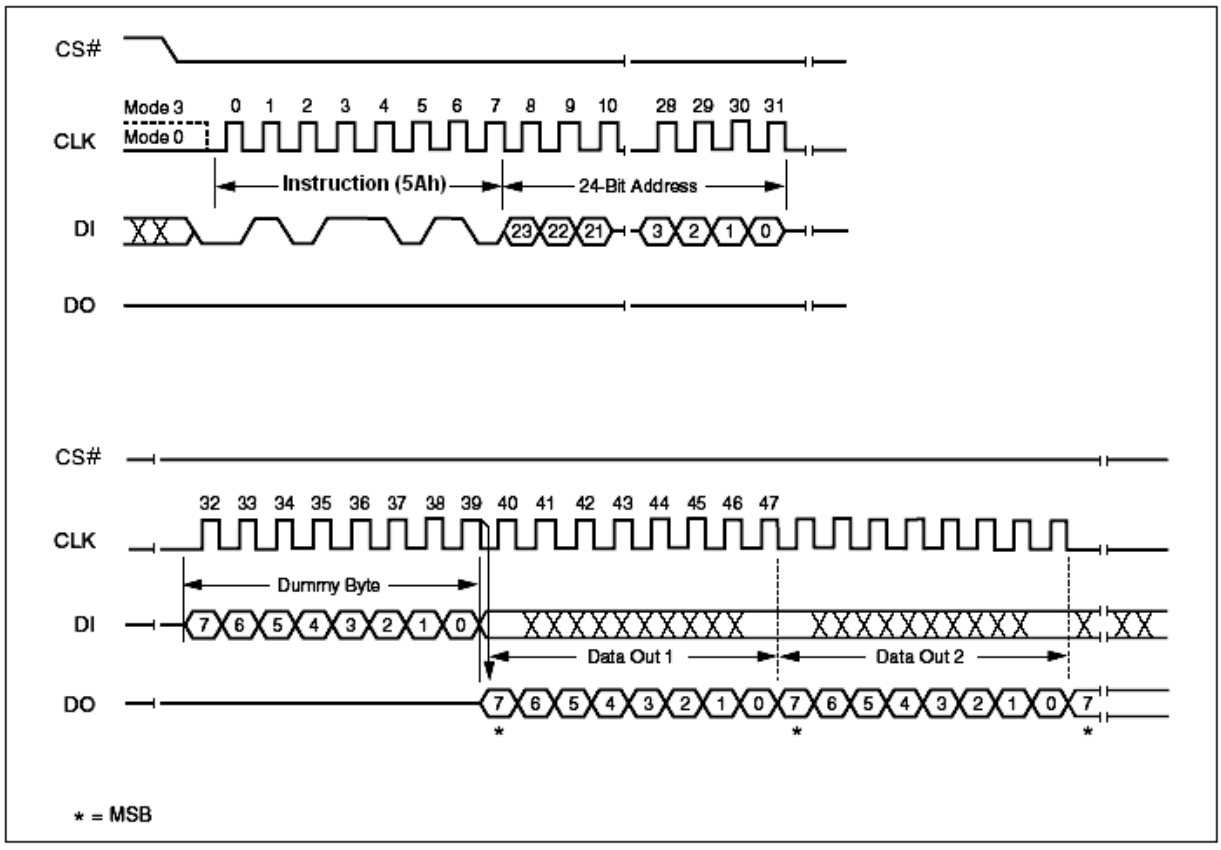
Read SFDP Mode and Unique ID Number (5Ah)

Read SFDP Mode

Device features Serial Flash Discoverable Parameters (SFDP) mode. Host system can retrieve the operating characteristics, structure and vendor specified information such as identifying information, memory size, operating voltage and timing information of this device by SFDP mode.

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read SFDP Mode is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency F_R, during the falling edge of Serial Clock (CLK).

The instruction sequence is shown in Read SFDP Mode and Unique ID Number Instruction Sequence Diagram figure. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Serial Flash Discoverable Parameters (SFDP) instruction. When the highest address is reached, the address counter rolls over to 0x00h, allowing the read sequence to be continued indefinitely. The Serial Flash Discoverable Parameters (SFDP) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes at Serial Flash Discoverable Parameters (SFDP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.



Read SFDP Mode and Unique ID Number Instruction Sequence Diagram

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Serial Flash Discoverable Parameters (SFDP) Signature and Parameter Identification Data Value

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
SFDP Signature	00h	07 : 00	53h	Signature [31:0]: Hex: 50444653
	01h	15 : 08	46h	
	02h	23 : 16	44h	
	03h	31 : 24	50h	
SFDP Minor Revision Number	04h	07 : 00	00h	Star from 0x00
SFDP Major Revision Number	05h	15 : 08	01h	Star from 0x01
Number of Parameter Headers (NPH)	06h	23 : 16	00h	1 parameter header
Unused	07h	31 : 24	FFh	Reserved
ID Number	08h	07 : 00	00h	JEDEC ID
Parameter Table Minor Revision Number	09h	15 : 08	00h	Star from 0x00
Parameter Table Major Revision Number	0Ah	23 : 16	01h	Star from 0x01
Parameter Table Length (in DW)	0Bh	31 : 24	09h	9 DWORDs
Parameter Table Pointer (PTP)	0Ch	07 : 00	30h	000030h
	0Dh	15 : 08	00h	
	0Eh	23 : 16	00h	
Unused	0Fh	31 : 24	FFh	Reserved

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Parameter ID (0) 1/9

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Block / Sector Erase sizes Identifies the erase granularity for all Flash Components	30h	00	01b	00 = reserved 01 = 4KB erase 10 = reserved 11 = 64KB erase
		01		
Write Granularity		02	1b	0 = No, 1 = Yes
Write Enable Instruction Required for Writing to Volatile Status Register		03	01b	00 = N/A 01 = use 50h opcode 11 = use 06h opcode
Write Enable Opcode Select for Writing to Volatile Status Register		04		
Unused		05	111b	Reserved
		06		
		07		
4 Kilo-Byte Erase Opcode	31h	08	20h	4 KB Erase Support (FFh = not supported)
		09		
		10		
		11		
		12		
		13		
		14		
		15		
Supports (1-1-2) Fast Read Device supports single input opcode & address and dual output data Fast Read	32h	16	1b	0 = not supported 1 = supported
Address Byte Number of bytes used in addressing for flash array read, write and erase.		17	00b	00 = 3-Byte 01 = 3- or 4-Byte (e.g. defaults to 3-Byte mode; enters 4-Byte mode on command) 10 = 4-Byte 11 = reserved
		18		
Supports Double Transfer Rate (DTR) Clocking Indicates the device supports some type of double transfer rate clocking.		19	0b	0 = not supported 1 = supported
Supports (1-2-2) Fast Read Device supports single input opcode, dual input address, and dual output data Fast Read		20	1b	0 = not supported 1 = supported
Supports (1-4-4) Fast Read Device supports single input opcode, quad input address, and quad output data Fast Read		21	1b	1 = supported
Supports (1-1-4) Fast Read Device supports single input opcode & address and quad output data Fast Read		22	1b	0 = not supported 1 = supported
Unused		23	1b	Reserved
Unused	33h	24	FFh	Reserved
		25		
		26		
		27		
		28		
		29		
		30		
		31		

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Parameter ID (0) 2/9

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Flash Memory Density	37h : 34h	31 : 00	00 FF FF FFh	16 Mbits

Parameter ID (0) 3/9

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
(1-4-4) Fast Read Number of Wait states (dummy clocks) needed before valid output	38h	00	00100b	4 dummy clocks
		01		
		02		
		03		
		04		
Quad Input Address Quad Output (1-4-4) Fast Read Number of Mode Bits		05	010b	8 mode bits
		06		
		07		
(1-4-4) Fast Read Opcode Opcode for single input opcode, quad input address, and quad output data Fast Read.	39h	08	EBh	
		09		
		10		
		11		
		12		
		13		
		14		
		15		
(1-1-4) Fast Read Number of Wait states (dummy clocks) needed before valid output	3Ah	16	01000b	8 dummy clocks
		17		
		18		
		19		
		20		
(1-1-4) Fast Read Number of Mode Bits		21	000b	Not Supported
		22		
		23		
(1-1-4) Fast Read Opcode Opcode for single input opcode & address and quad output data Fast Read.	3Bh	31 : 24	6Bh	

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Parameter ID (0) 4/9

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
(1-1-2) Fast Read Number of Wait states (dummy clocks) needed before valid output	3Ch	00 01 02 03 04	01000b	8 dummy clocks
(1-1-2) Fast Read Number of Mode Bits		05 06 07	000b	Not Supported
(1-1-2) Fast Read Opcode Opcode for single input opcode & address and dual output data Fast Read.	3Dh	15 : 08	3Bh	
(1-2-2) Fast Read Number of Wait states (dummy clocks) needed before valid output	3Eh	16 17 18 19 20	00100b	4 dummy clocks
(1-2-2) Fast Read Number of Mode Bits		21 22 23	000b	Not Supported
(1-2-2) Fast Read Opcode Opcode for single input opcode, dual input address, and dual output data Fast Read.	3Fh	31 : 24	BBh	

Parameter ID (0) 5/9

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Supports (2-2-2) Fast Read Device supports dual input opcode & address and dual output data Fast Read.	40h	00	0b	0 = not supported 1 = supported
Reserved. These bits default to all 1's		01 02 03	111b	Reserved
Supports (4-4-4) Fast Read Device supports Quad input opcode & address and quad output data Fast Read.		04	1b	0 = not supported 1 = supported (QPI Mode)
Reserved. These bits default to all 1's		05 06 07	111b	Reserved
Reserved. These bits default to all 1's	43h : 41h	31 : 08	FF FF FFh	Reserved

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Parameter ID (0) 6/9

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Reserved. These bits default to all 1's	45h : 44h	15 : 00	FF FFh	Reserved
(2-2-2) Fast Read Number of Wait states (dummy clocks) needed before valid output	46h	16	00000b	Not Supported
		17		
		18		
		19		
		20		
(2-2-2) Fast Read Number of Mode Bits		21	000b	Not Supported
		22		
		23		
(2-2-2) Fast Read Opcode Opcode for dual input opcode & address and dual output data Fast Read.	47h	31 : 24	FFh	Not Supported

Parameter ID (0) 7/9

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Reserved. These bits default to all 1's	49h : 48h	15 : 00	FF FFh	Reserved
(4-4-4) Fast Read Number of Wait states (dummy clocks) needed before valid output	4Ah	16	00100b	4 dummy clocks
		17		
		18		
		19		
		20		
(4-4-4) Fast Read Number of Mode Bits		21	010b	8 mode bits
		22		
		23		
(4-4-4) Fast Read Opcode Opcode for quad input opcode/address, quad output data Fast Read.	4Bh	31 : 24	EBh	Must Enter QPI Mode Firstly

Parameter ID (0) 8/9

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Sector Type 1 Size	4Ch	07 : 00	0Ch	4 KB
Sector Type 1 Opcode	4Dh	15 : 08	20h	
Sector Type 2 Size	4Eh	23 : 16	0Fh	32 KB
Sector Type 2 Opcode	4Fh	31 : 24	52h	

Parameter ID (0) 9/9

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Sector Type 3 Size	50h	07 : 00	10h	64 KB
Sector Type 3 Opcode	51h	15 : 08	D8h	
Sector Type 4 Size	52h	23 : 16	00h	Not Supported
Sector Type 4 Opcode	53h	31 : 24	FFh	Not Supported

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Read Unique ID Number

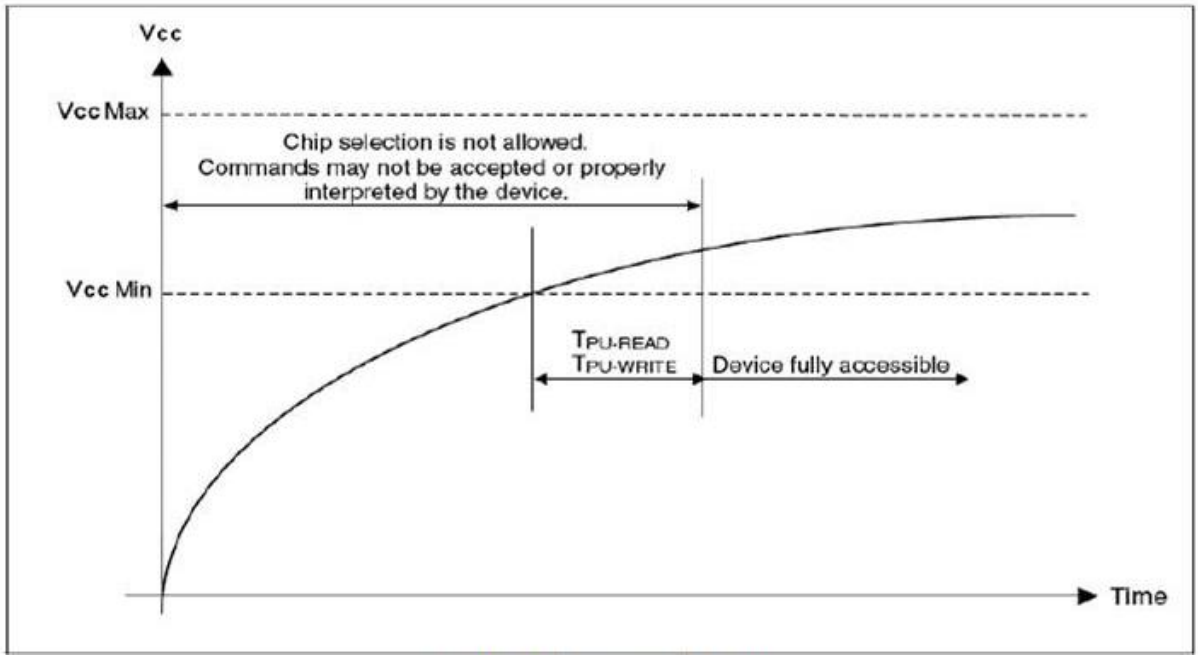
The Read Unique ID Number instruction accesses a factory-set read-only 96-bit number that is unique to each device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the CS# pin low and shifting the instruction code "5Ah" followed by a three bytes of addresses, 0x80h, and one byte of dummy clocks. After which, the 96-bit ID is shifted out on the falling edge of CLK.

Unique ID Number

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Unique ID Number	80h : 8Bh	95 : 00	By die	

Power-up Timing

All functionalities and DC specifications are specified for a V_{CC} ramp rate of greater than 1V per 100 ms. See Power-Up Timing and Write Inhibit Threshold table and Power-up Timing figure for more information.



Power-up Timing

Power-Up Timing and Write Inhibit Threshold

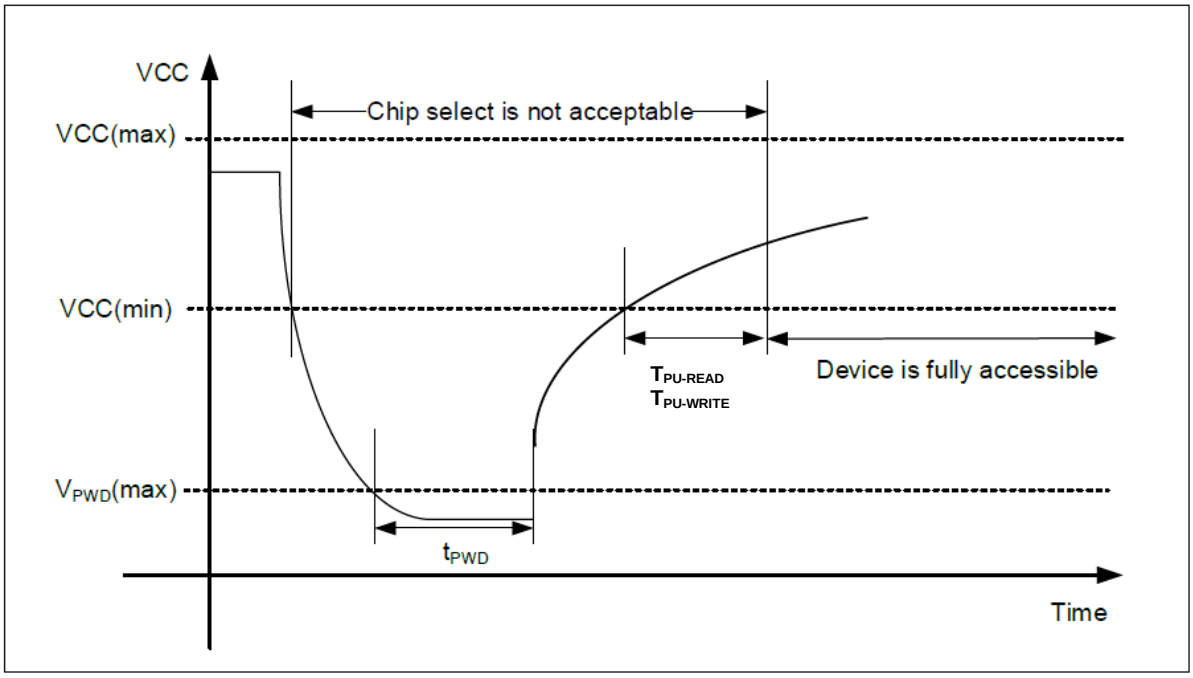
Symbol	Parameter	Min.	Unit
$T_{PU-READ}$ (1)	V_{CC} Min to Read Operation	100	µs
$T_{PU-WRITE}$ (1)	V_{CC} Min to Write Operation	100	µs

Note:

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

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Power-down Timing



Power-down Timing

Power-Down Timing

Symbol	Parameter	Min.	Max.	Unit
t_{PWD}	The minimum duration for initialization to occur	100	-	us
V_{PWD}	V_{CC} voltage required for initialization to occur	-	0.5	V

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INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

DC Characteristics

(T_A = - 40°C to 85°C; V_{CC} = 2.3-3.6V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current		-	1	± 2	µA
I_{LO}	Output Leakage Current		-	1	± 2	µA
I_{CC1}	Standby Current	CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	1	20	µA
I_{CC2}	Deep Power-down Current	CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	1	20	µA
I_{CC3}	Operating Current (READ)	CLK = 0.1 V_{CC} / 0.9 V_{CC} at 104MHz, DQ = open	-	5	10	mA
		CLK = 0.1 V_{CC} / 0.9 V_{CC} at 133MHz, Quad Output Read, DQ = open	-	16	22	mA
		CLK = 0.1 V_{CC} / 0.9 V_{CC} at 104MHz in Quad mode, DQ = open	-	14	18	mA
I_{CC4}	Operating Current (PP)	CS# = V_{CC}	-	9	20	mA
I_{CC5}	Operating Current (WRSR)	CS# = V_{CC}	-	-	12	mA
I_{CC6} [1]	Operating Current (SE)	CS# = V_{CC}	-	9	20	mA
I_{CC7} [1]	Operating Current (BE)	CS# = V_{CC}	-	9	20	mA
V_{IL}	Input Low Voltage		-0.5	-	0.2 V_{CC}	V
V_{IH}	Input High Voltage		0.7V_{CC}	-	V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA V_{CC}= V_{CC} Min.	-	-	0.3	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA V_{CC}= V_{CC} Min.	V_{CC}-0.2	-	-	V

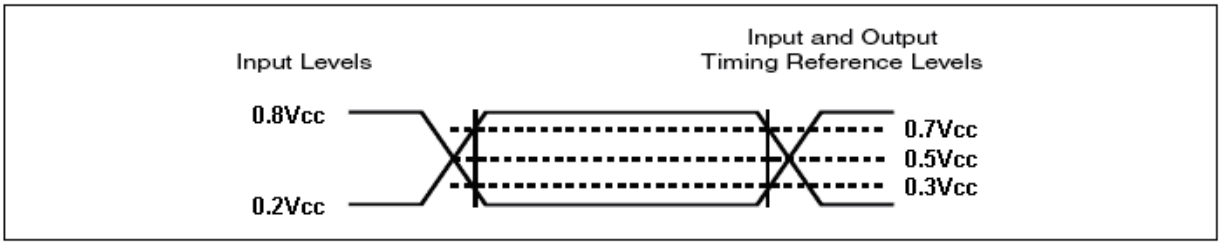
Note:

1. Erase current measure on all cells=”0” states.

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AC Measurement Conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times	-	5	ns
	Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V
	Output Timing Reference Voltages	V_{CC} / 2		V



AC Measurement I/O Waveform

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AC Characteristics

(T_A = - 40°C to 85°C; V_{CC} = 2.3-3.6V)

Symbol	Alt	Parameter		Min	Typ	Max	Unit
F_R	f_C	Serial Clock Frequency for: FAST_READ, QPP, PP, SE, HBE, BE, DP, RES, WREN, WRDI, WRSR, WRSR3, RDSR, RDSR3, Wrap Read	2.7V ≦ V_{CC} ≦ 3.6V	D.C.	-	104	MHz
			2.3V ≦ V_{CC} < 2.7V	D.C.	-	86	MHz
		Serial Clock Frequency for: RDID, Dual Output Fast Read and Quad I/O Fast Read	2.7V ≦ V_{CC} ≦ 3.6V	D.C.	-	104	MHz
			2.3V ≦ V_{CC} < 2.7V	D.C.	-	86	MHz
		Flash V_{CC} ≧ 3.0V Quad Output Fast Read, Quad I/O Fast Read		D.C.	-	133	MHz
f_R		Serial Clock Frequency for READ	2.7V ≦ V_{CC} ≦ 3.6V	D.C.	-	83	MHz
			2.3V ≦ V_{CC} < 2.7V	D.C.	-	50	MHz
t_{CH} [1]		Serial Clock High Time	2.7V ≦ V_{CC} ≦ 3.6V	3.5	-	-	ns
			2.3V ≦ V_{CC} < 2.7V	4	-	-	ns
t_{CL} [1]		Serial Clock Low Time	2.7V ≦ V_{CC} ≦ 3.6V	3.5	-	-	ns
			2.3V ≦ V_{CC} < 2.7V	4	-	-	ns
t_{CLCH} [2]		Serial Clock Rise Time (Slew Rate)		0.1	-	-	V / ns
t_{CHCL} [2]		Serial Clock Fall Time (Slew Rate)		0.1	-	-	V / ns
t_{SLCH}	t_{CSS}	CS# Active Setup Time (Relative to CLK)		5	-	-	ns
t_{CHSH}		CS# Active Hold Time (Relative to CLK)		5	-	-	ns
t_{SHCH}		CS# Not Active Setup Time (Relative to CLK)		5	-	-	ns
t_{CHSL}		CS# Not Active Hold Time (Relative to CLK)		5	-	-	ns
t_{SHSL}	t_{CSH}	CS# High Time		30	-	-	ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time		-	-	6	ns
t_{CLQX}	t_{HO}	Output Hold Time		0	-	-	ns
t_{DVCH}	t_{DSU}	Data In Setup Time		2	-	-	ns
t_{CHDX}	t_{DH}	Data In Hold Time		3	-	-	ns
t_{HLCH}		HOLD# Low Setup Time (relative to CLK)		5	-	-	ns
t_{HHCH}		HOLD# High Setup Time (relative to CLK)		5	-	-	ns
t_{CHHH}		HOLD# Low Hold Time (relative to CLK)		5	-	-	ns
t_{CHHL}		HOLD# High Hold Time (relative to CLK)		5	-	-	ns
t_{HLQZ} [2]	t_{HZ}	HOLD# Low to High-Z Output		-	-	5	ns
t_{HHQX} [2]	t_{LZ}	HOLD# High to Low-Z Output		-	-	5	ns
t_{CLQV}	t_V	Output Valid from CLK for 30 pF	2.7V ≦ V_{CC} ≦ 3.6V	-	-	8	ns
			2.3V ≦ V_{CC} < 2.7V	-	-	10	ns
		Output Valid from CLK for 15 pF	2.7V ≦ V_{CC} ≦ 3.6V	-	-	6	ns
			2.3V ≦ V_{CC} < 2.7V	-	-	8	ns

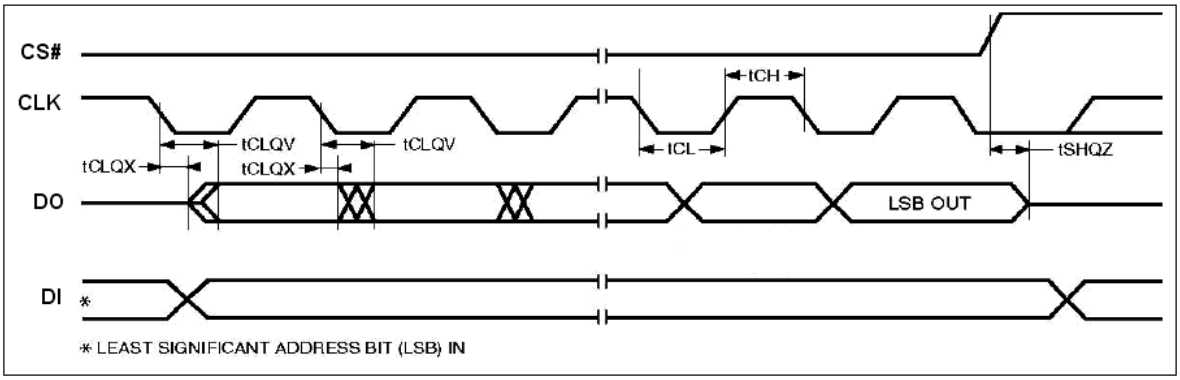
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AC Characteristics- Continued

Symbol	Alt	Parameter		Min	Typ	Max	Unit
t_{WHSL} [3]		Write Protect Setup Time before CS# Low		-	-	-	ns
t_{SHWL} [3]		Write Protect Hold Time after CS# High		-	-	-	ns
t_{DP} [2]		CS# High to Deep Power-down Mode		-	-	3	µs
t_{RES1} [2]		CS# High to Standby Mode without Electronic Signature read		-	-	3	µs
t_{RES2} [2]		CS# High to Standby Mode with Electronic Signature read		-	-	1.8	µs
t_W		Write Status Register Cycle Time	2.7V ≦ V_{CC} ≦ 3.6V	-	10	30	ms
			2.3V ≦ V_{CC} < 2.7V	-	10	50	ms
t_{PP}		Page Programming Time	2.7V ≦ V_{CC} ≦ 3.6V	-	0.6	3	ms
			2.3V ≦ V_{CC} < 2.7V	-	0.9	5	ms
t_{SE}		Sector Erase Time	2.7V ≦ V_{CC} ≦ 3.6V	-	0.05	0.3	s
			2.3V ≦ V_{CC} < 2.7V	-	0.15	1	s
t_{HBE}		32KB Block Erase Time	2.7V ≦ V_{CC} ≦ 3.6V	-	0.12	1	s
			2.3V ≦ V_{CC} < 2.7V	-	0.25	2	s
t_{BE}		64KB Block Erase Time	2.7V ≦ V_{CC} ≦ 3.6V	-	0.15	2	s
			2.3V ≦ V_{CC} < 2.7V	-	0.4	3	s
t_{CE}		Chip Erase Time	2.7V ≦ V_{CC} ≦ 3.6V	-	6	25	s
			2.3V ≦ V_{CC} < 2.7V	-	10	40	s
t_{SR}		Software Reset Latency	WIP = write operation	-	-	28	µs
			WIP = not in write operation	-	-	0	µs

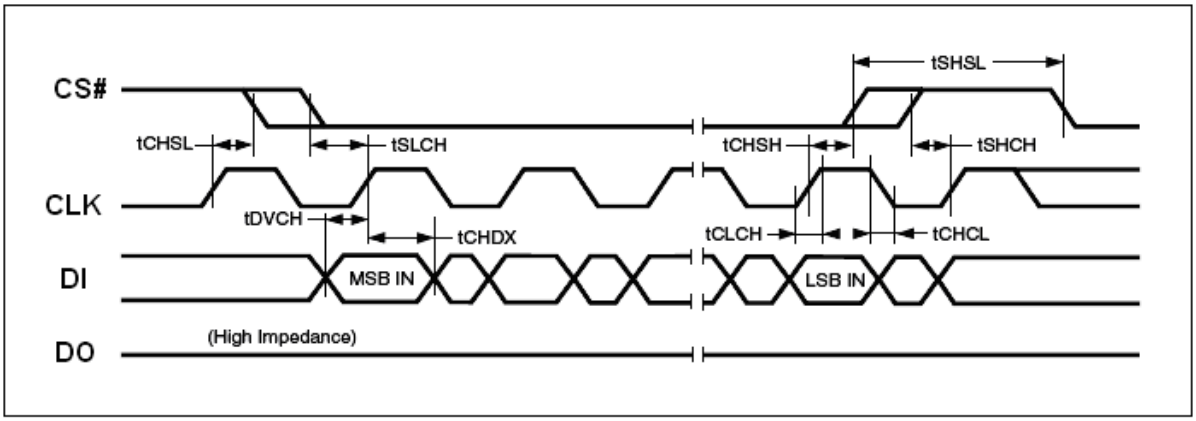
Note:

1. t_{CH} + t_{CL} must be greater than or equal to 1/ f_C.
2. Value guaranteed by characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write status Register instruction when Status Register Protect Bit is set at 1.

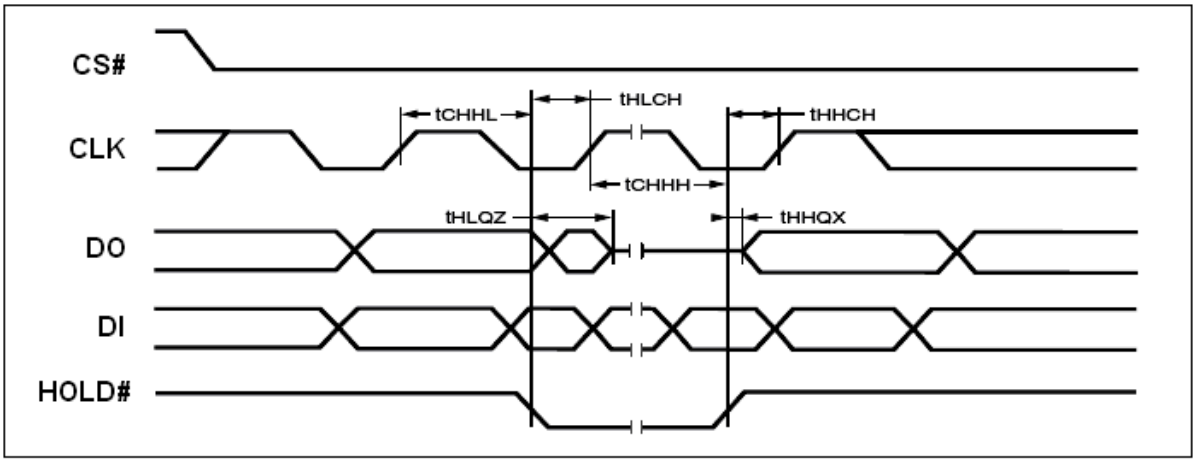


Serial Output Timing

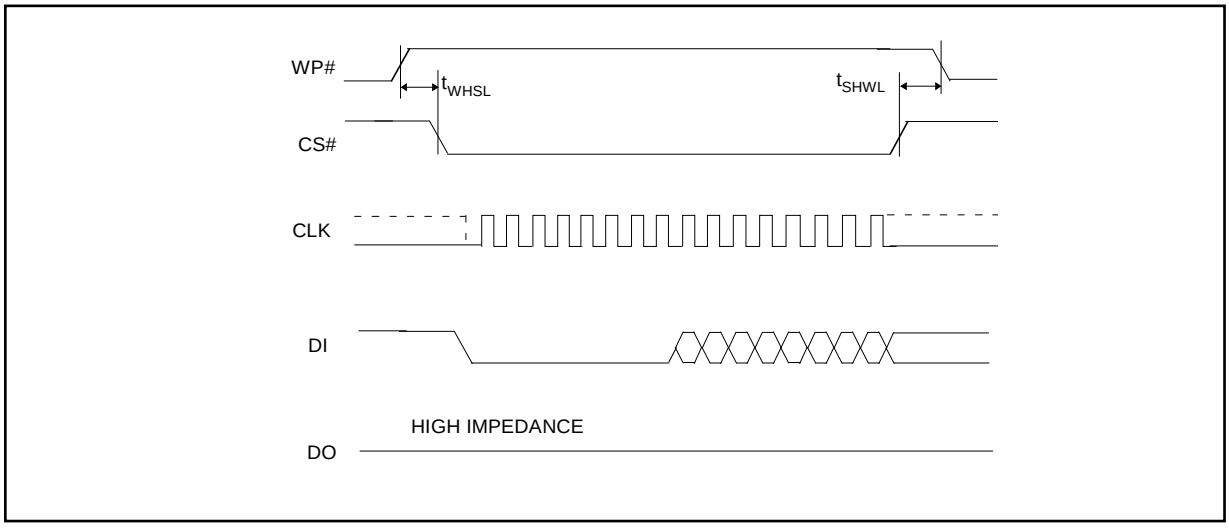
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Input Timing



Hold Timing



Write Protect setup and hold timing during WRSR when SRP = 1

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ABSOLUTE MAXIMUM RATINGS

Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values. Exposure of the device to the maximum rating values for extended periods of time may adversely affect the device reliability.

Parameter	Value	Unit
Storage Temperature	-65 to +150	°C
Output Short Circuit Current[1]	200	mA
Input and Output Voltage (with respect to ground) [2]	-0.5 to +4.0	V
V_{CC}	-0.5 to +4.0	V

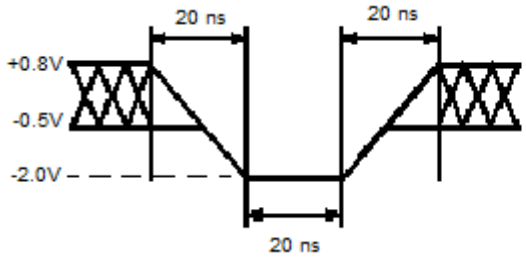
Note:

1. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.
2. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot V_{SS} to -1.0V for periods of up to 50ns and to -2.0V for periods of up to 20ns. See figure below. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5V. During voltage transitions, outputs may overshoot to V_{CC} + 1.5V for periods up to 20ns. See figure below.

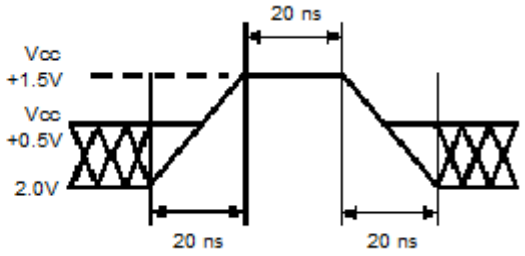
RECOMMENDED OPERATING RANGES

Parameter	Value	Unit
Ambient Operating Temperature Industrial Devices	-40 to 85	°C
Operating Supply Voltage V_{CC}	Full: 2.3 to 3.6	V

Note: Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.



Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform

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CAPACITANCE

(V_{CC} = 2.3-3.6V)

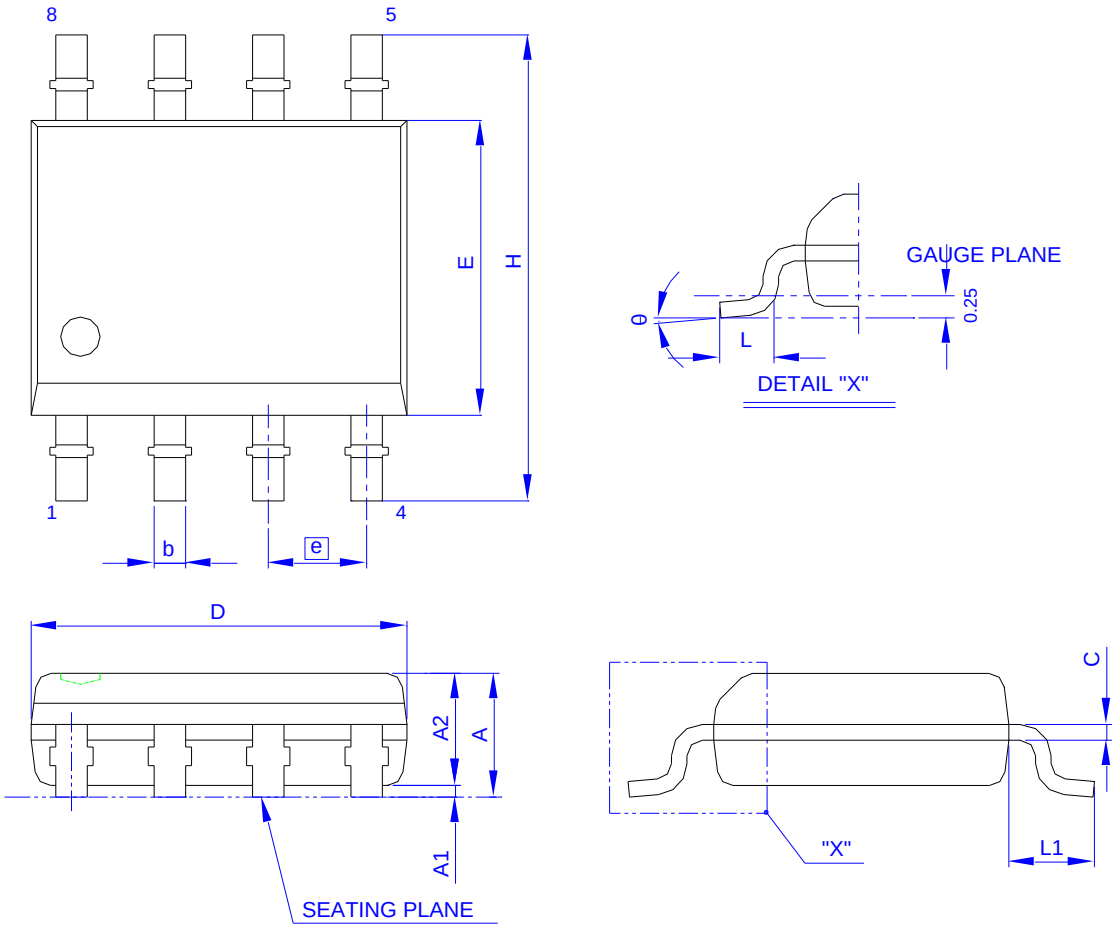
Parameter Symbol	Parameter Description	Test Setup	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	pF

Note: Sampled only, not 100% tested, at T_A = 25°C and a frequency of 20MHz.

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PACKAGE MECHANICAL

8-pin SOP (150 mil)

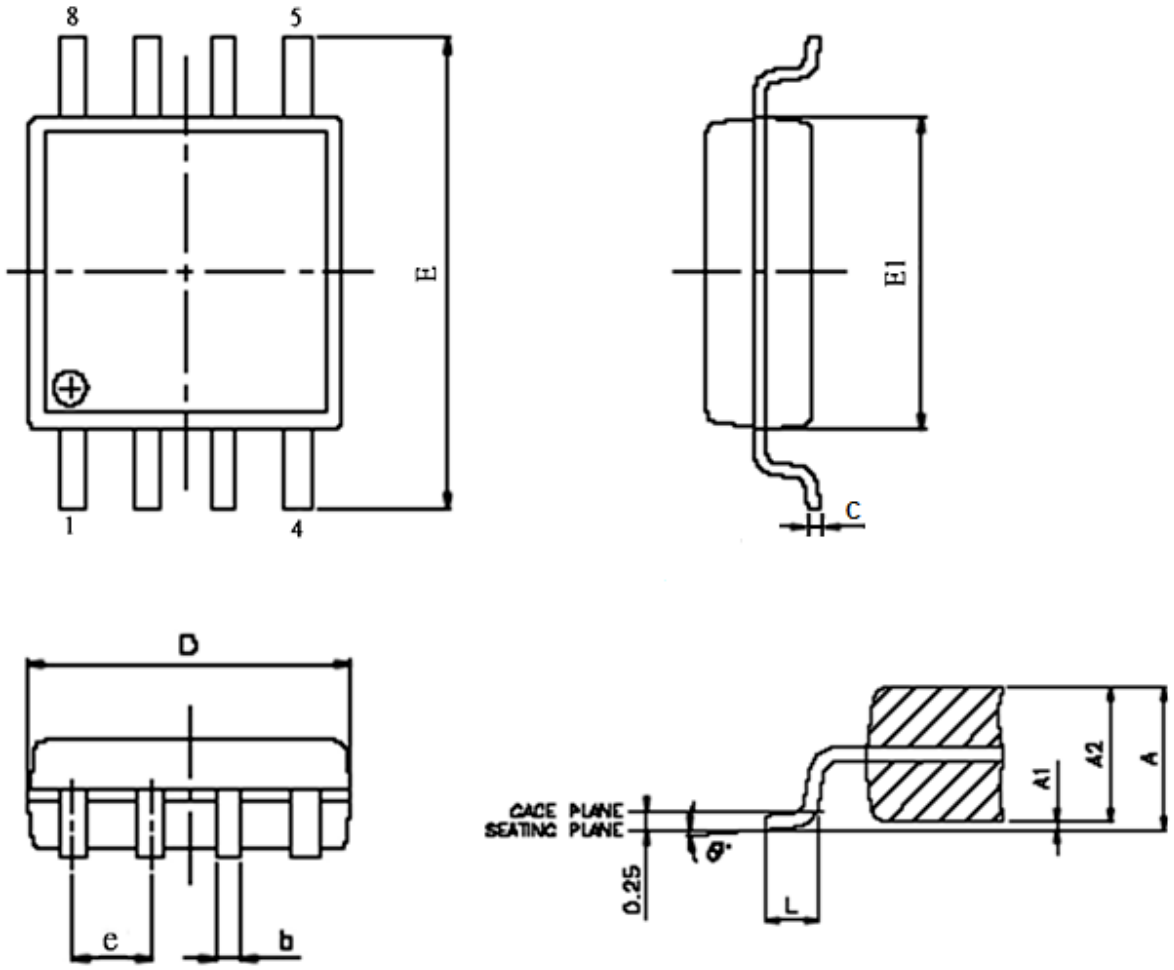


Symbol	Dimension in mm			Dimension in inch			Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max		Min	Norm	Max	Min	Norm	Max
A	1.35	1.60	1.75	0.053	0.063	0.069	D	4.80	4.90	5.00	0.189	0.193	0.197
A_1	0.10	0.15	0.25	0.004	0.006	0.010	E	3.80	3.90	4.00	0.150	0.154	0.157
A_2	1.25	1.45	1.55	0.049	0.057	0.061	L	0.40	0.66	0.86	0.016	0.026	0.034
b	0.33	0.406	0.51	0.013	0.016	0.020	e	1.27 BSC			0.050 BSC		
c	0.19	0.203	0.25	0.0075	0.008	0.010	L_1	1.00	1.05	1.10	0.039	0.041	0.043
H	5.80	6.00	6.20	0.228	0.236	0.244	θ	0°	---	8°	0°	---	8°

Controlling dimension: millimenter

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8-pin SOP 200 mil (official name = 208 mil)

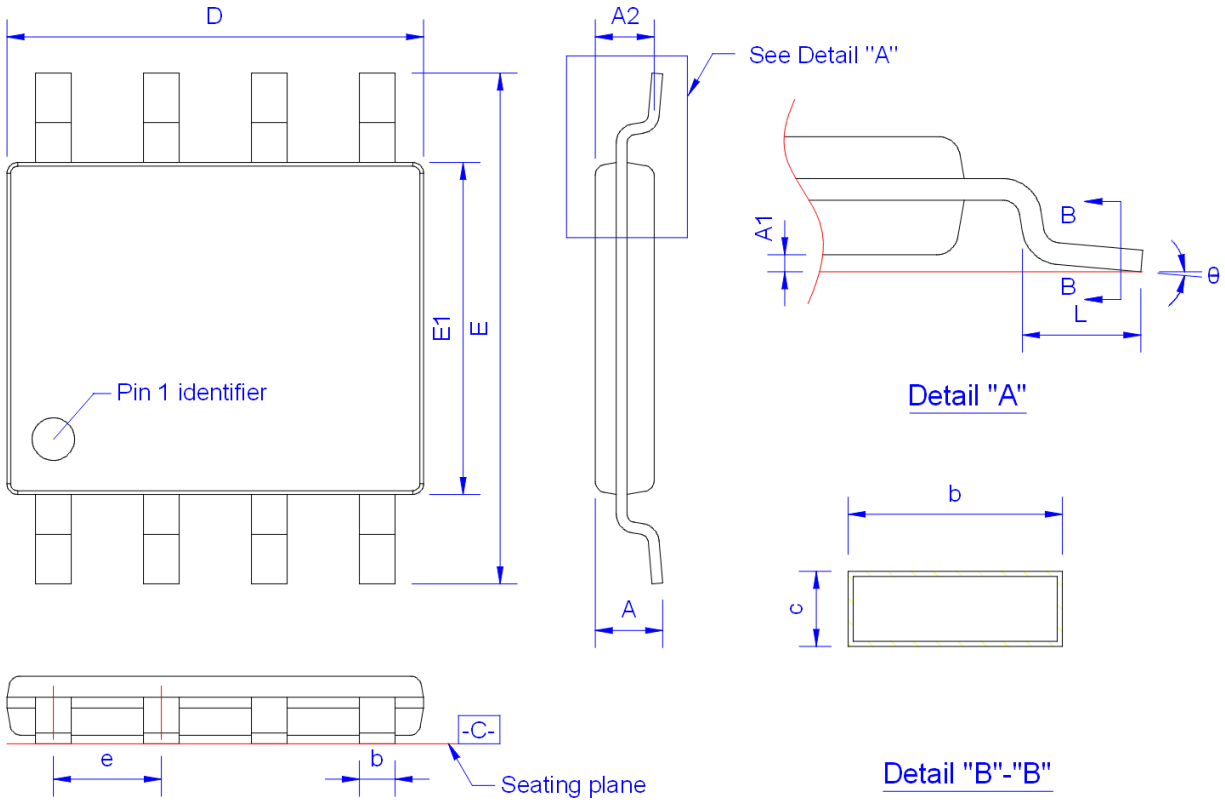


SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	1.75	1.975	2.20
A1	0.05	0.15	0.25
A2	1.70	1.825	1.95
D	5.15	5.275	5.40
E	7.70	7.90	8.10
E1	5.15	5.275	5.40
e	- - -	1.27	- - -
b	0.35	0.425	0.50
C	0.19	0.200	0.25
L	0.5	0.65	0.80
θ	0^0	4^0	8^0

Note : 1. Coplanarity: 0.1 mm
2. Max. allowable mold flash is 0.15 mm at the pkg ends, 0.25 mm between leads.

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8-pin VSOP (150 mil)

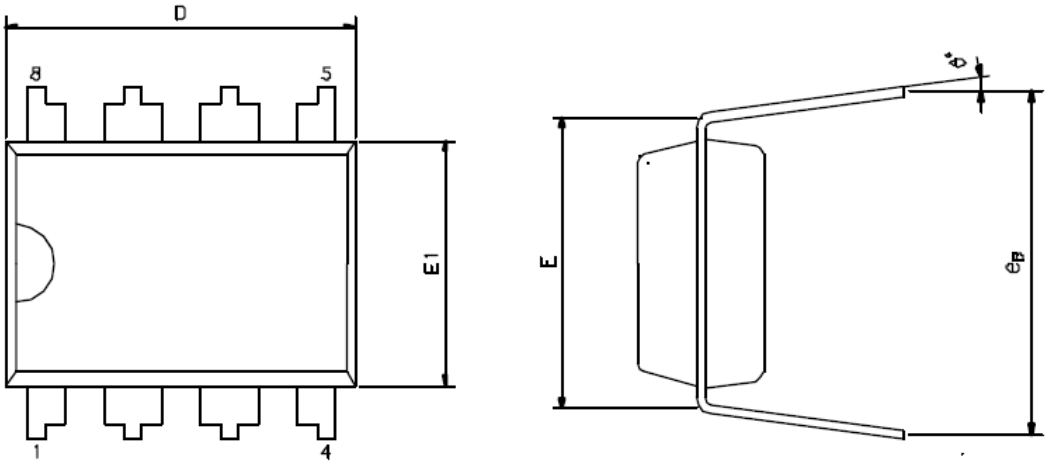


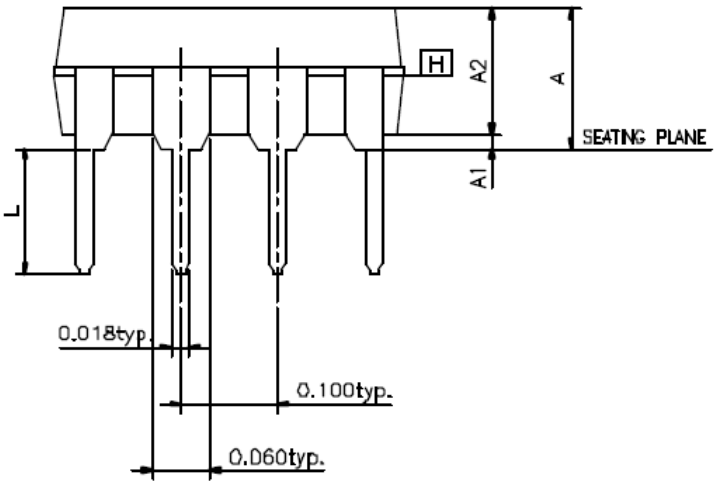
Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	0.75	0.85	0.90	0.030	0.033	0.035
A1	0.01	0.05	-	0.000	0.002	-
A2	-	0.80	-	-	0.031	-
b	0.33	-	0.51	0.013	-	0.020
c	0.125 BSC			0.005 BSC		
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
L	0.40	0.66	0.86	0.016	0.026	0.034
e	1.27 BSC			0.050 BSC		
Θ	0°	-	10°	0°	-	10°

Controlling dimension: Millimeter.
(Revision date: Nov 19 2020)

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8-pin PDIP

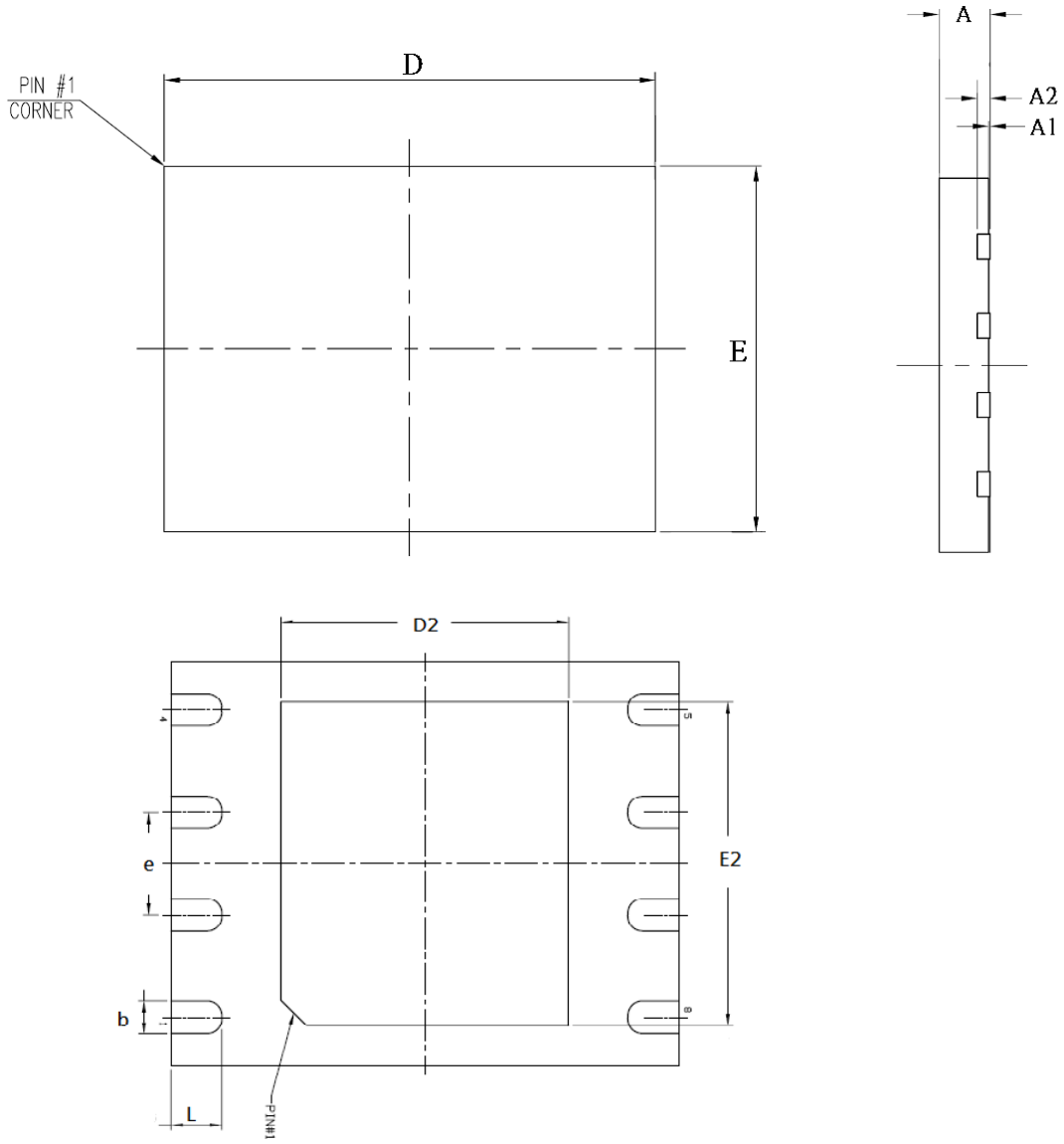




SYMBOL	DIMENSION IN INCH		
	MIN.	NOR	MAX
A	- - -	- - -	0.210
A1	0.015	- - -	- - -
A2	0.125	0.130	0.135
D	0.355	0.365	0.400
E	0.300	0.310	0.320
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e_B	0.310	0.350	0.375
Θ^0	0	7	15

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8-contact VDFN / WSON (6x5 mm)



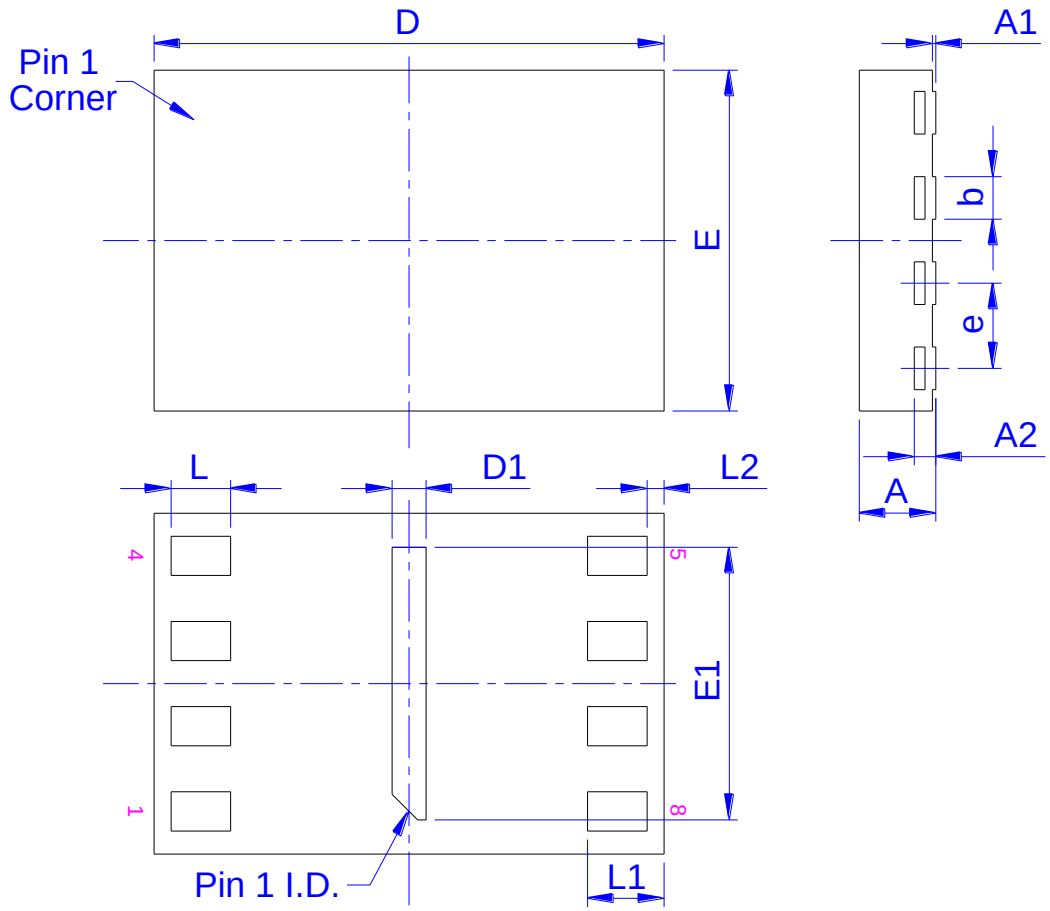
Controlling dimensions are in millimeters (mm).

SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.04
A2	- - -	0.20	- - -
D	5.90	6.00	6.10
E	4.90	5.00	5.10
D2	3.30	3.40	3.50
E2	3.90	4.00	4.10
e	- - -	1.27	- - -
b	0.35	0.40	0.45
L	0.55	0.60	0.65

Note : 1. Coplanarity: 0.1 mm

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8-contact USON (2x3x0.45 mm)

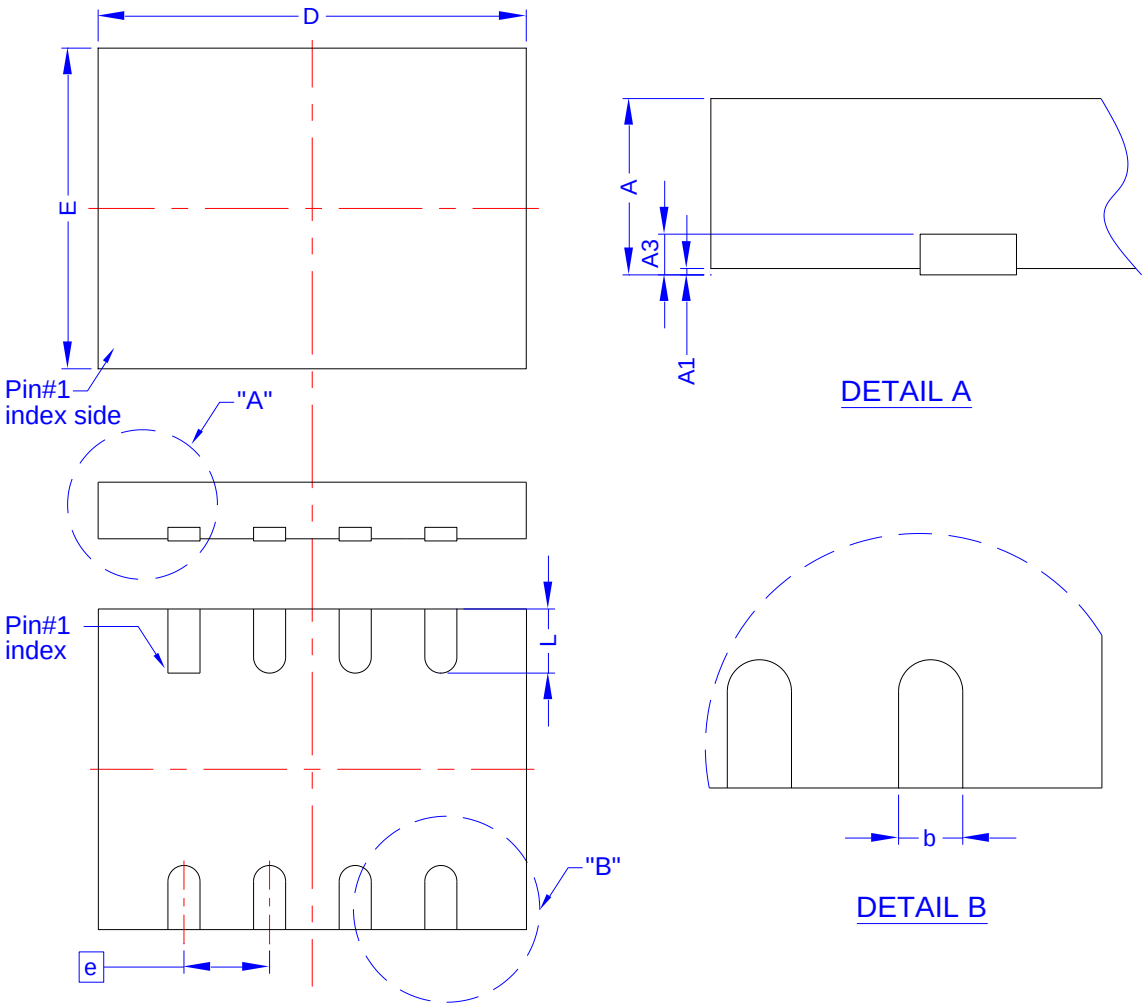


Symbol	Dimension in mm		
	Min.	Norm.	Max.
A	0.40	0.45	0.50
A1	0.00	-	0.05
A2		0.152 REF	
b	0.20	0.25	0.30
D	2.90	3.00	3.10
D1	0.10	0.20	0.30
E	1.90	2.00	2.10
E1	1.50	1.60	1.70
e		0.50 BSC	
L	0.30	-	-
L1	0.40	0.45	0.50
L2	-	-	0.15

Controlling dimension: millimeter

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8-contact USON (4x3x0.55 mm) without Expose metal pad



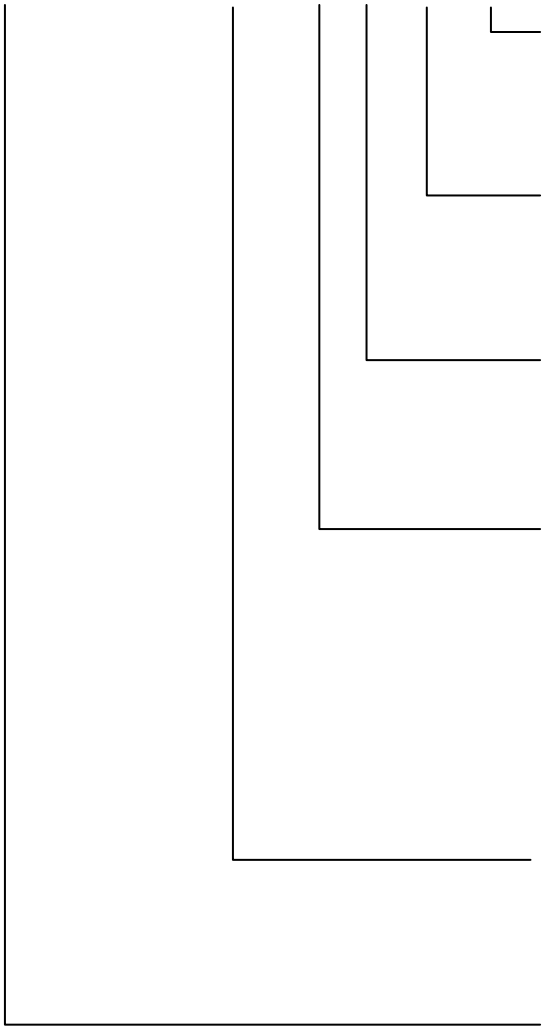
Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	--	0.15	--	--	0.006	--
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.90	4.00	4.10	0.154	0.157	0.161
E	2.90	3.00	3.10	0.114	0.118	0.122
e		0.80 BSC			0.031 BSC	
L	0.55	0.60	0.65	0.022	0.024	0.026

Controlling dimension: millimeter
(Revision date: Apr 22 2019)

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ORDERING INFORMATION

EN25QH16B - 104 H I P 2A



DIFFERENTIATION CODE
2AE = USON package without Expose metal pad

PACKAGING CONTENT
P = RoHS, Halogen-Free and REACH compliant

TEMPERATURE RANGE
I = Industrial (-40°C to +85°C)

PACKAGE
G = 8-pin 150 mil SOP
H = 8-pin 200 mil SOP
RB= 8-pin 150 mil VSOP
Q = 8-pin PDIP
W = 8-contact VDFN / WSON (6x5 mm)
XF = 8-contact USON (2x3x0.45 mm)
XB = 8-contact USON (4x3x0.55 mm)

SPEED
104 = 104 MHz

BASE PART NUMBER
EN = Eon Silicon Solution Inc.
25QH = 3V Serial Flash with 4KB Uniform-Sector, Dual and Quad I/O
16 = 16 Megabit (2048K x 8)
B = version identifier

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Revisions List

Revision No	Description	Date
A	Initial Release	2017.02.10
B	1.Remove "Suspend/Resume" 2.Delete Program / Erase Fail Flag bit of Read Status Register 2 3. Revise the Note content. 4. Typo.	2017.04.06
C	1.Add differentiation code into product ID 2.Revised Dim. of USON 2x3x0.45 mm.	2017.05.17
D	1. Revised "typical active current" from 10 to 5 mA. 2. Revised th Fig.1 3. Revised the Fig. and Table of power up timing (tPU-READ/tPU-WRITE format). 4. Revised the Table 15. DC Characteristics. 5. Revised the content of Table12 Parameter ID (0)	2017.08.03
E	1. Typo. 2. Modify Package Dimension.	2017.12.05
F	1. Modify voltage from 2.7V~3.6V to 2.4V~3.6V 2. Add some AC specifications for VCC under 2.7V	2018.01.17
G	Modify Status Register Bit Locations (In Normal mode) table	2018.06.20
H	Modify the packing dimension of SOP 200 mil (official name = 208 mil)	2018.10.04
I	Modify voltage from 2.4V~3.6V to 2.3V~3.6V	2019.03.04
J	1. Delete Plastic Packages Temperature 2. Modify SOP-8 150mil	2020.10.08
K	1. Correct The Enable Boot Lock feature table 2. Remove USON 2x3x0.55 mm package 3. Correct SOP8 & VSOP8 150mil packing dimension 4. Add Important Notice	2021.08.04
L	Add speed grade of 133MHz	2022.08.19
M	Add the description of Read Burst, RDSR3 and WRSR3	2022.09.30
N	Add USON (8L 4x3x0.55 mm) without expose metal pad package	2023.03.16
O	Modify: Power-down timing info	2025.04.22

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