ARM®-based 32-bit Cortex®-M4 MCU with 16 KB to 64 KB Flash, sLib, 10 timers, 1 ADC, 1 CMP, 7 communication interfaces

Features

- **Core: ARM® 32-bit Cortex®-M4 CPU**
  - 120 MHz maximum frequency, with a memory protection unit (MPU), single-cycle multiplication and hardware division
  - DSP instructions
- **Memories**
  - 16 to 64 KB of internal Flash memory
  - 4 Kbytes of boot memory used as a Bootloader
  - sLib: configurable part of main Flash set as a library area with code executable but secured, non-readable
  - 8 to 16 Kbytes of SRAM
- **Power control (PWC)**
  - 2.4 to 3.6 V power supply
  - Power-on reset (POR), low voltage reset (LVR) and power voltage monitoring (PVM)
  - Low power modes: Sleep, Deepsleep and Standby modes; four WKUP pins used for wakeup from Standby mode
  - Supports 5 x 32-bit battery powered registers (BPR)
- **Clock and reset management (CRM)**
  - 4 to 25 MHz crystal oscillator (HEXT)
  - Internal 48 MHz factory-trimmed HICK (±1% at TA=25 °C, ±2% at TA= -40°C to +105 °C)
  - PLL flexible 31 to 500 multiplication and 1 to 15 division factor
  - 32 kHz crystal (LEXT)
  - Low speed internal clock (LICK)
- **Analog**
  - 1 x 12-bit 2 MSPS A/D converter, up to 15 input channels
  - Temperature sensor (V_{TS}) and internal reference voltage (V_{INTRV})
  - 1 x CMP with 5 external input channels
- **DMA**
  - 1 x 5-channel DMA controller
- **Up to 39 fast GPIOs**
  - All mappable on 16 external interrupts (EXINT)
  - Almost all 5 V-tolerant
- **Up to 10 timers (TMR)**
  - 1 x 16-bit 7-channel advanced timer, including 3 channels for complementary PWM output, with dead-time generator and emergency brake
  - Up to 5 x 16-bit timers, each with 4 IC/OC /PWM or pulse counter and quadrature (incremental) encoder input
  - 1 x 16-bit basic timer
  - 2 x watchdog timers (general WDT and windowed WWDT)
  - SysTick timer: a 24-bit downcounter
- **ERTC: enhanced RTC, with alarm, subsecond accuracy, hardware calendar and calibration**
- **Up to 7 communication interfaces**
  - 2 x I^2C interfaces (SMBus/PMBus)
  - 2 x USARTs supporting master synchronous SPI and modem control, with ISO7816 interface, LIN, IrDA capability and swappable TX/RX
  - 2 x SPIs (36 Mbit/s), all with multiplexed half-duplex I^2S
  - Infrared transmitter (IRTMR)
- **CRC calculation unit**
- **96-bit unique ID (UID)**
- **Serial wire debug (SWD) interface**
- **Operating temperature: -40 to +105 °C**
- **Packages**
  - LQFP48 7 x 7 mm
  - LQFP32 7 x 7 mm
  - QFN32 5 x 5 mm
  - QFN32 4 x 4 mm
  - QFN28 4 x 4 mm
  - TSSOP20 6.5 x 4.4 mm

Table 1. Device summary

Internal Flash	Part number
64 Kbytes	AT32F421C8T7, AT32F421K8T7, AT32F421K8U7, AT32F421K8U7-4, AT32F421G8U7, AT32F421F8P7
32 Kbytes	AT32F421C6T7, AT32F421K6T7, AT32F421K6U7, AT32F421K6U7-4, AT32F421G6U7, AT32F421F6P7
16 Kbytes	AT32F421C4T7, AT32F421K4T7, AT32F421K4U7, AT32F421K4U7-4, AT32F421G4U7, AT32F421F4P7

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1 Descriptions

The AT32F421 is based on the high-performance ARM®Cortex®-M4 32-bit RISC core running up to 120 MHz. The Cortex®-M4 core features a full set of DSP instructions and a memory protection unit (MPU).

The AT32F421 incorporates high-speed embedded memories (up to 64 Kbytes of internal Flash memory and 16 Kbytes of SRAM), enhanced GPIOs and peripherals connected to two APB buses. Any block of the embedded Flash memory can be protected by the “sLib”, functioning as a security area with code-executable only.

The AT32F421 offers one 12-bit ADC, one analog comparator (CMP), five general-purpose 16-bit timers, one advanced timer and one low-power ERTC, as well as standard and advanced communication interfaces: up to two I^2C interfaces, two SPIs (all multiplexed as I^2S), two USARTs and one infrared transmitter.

The AT32F421 operates in the -40 to +105 °C temperature range, from a 2.4 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power application.

The AT32F421 offers devices in different package types. Depending on the different packages, the pin-to-pin is completely compatible among devices, and also the software and functionality. Only different sets of peripherals are included.

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Table 2. AT32F421 features and peripheral counts

Part number		AT32F421xxP7			AT32F421xxU7			AT32F421xxU7-4			AT32F421xxU7			AT32F421xxT7			AT32F421xxT7		
		F4	F6	F8	G4	G6	G8	K4	K6	K8	K4	K6	K8	K4	K6	K8	C4	C6	C8
CPU frequency (MHz)		120																	
Flash (Kbytes)		16	32	64	16	32	64	16	32	64	16	32	64	16	32	64	16	32	64
SRAM (Kbytes)		8	16	16	8	16	16	8	16	16	8	16	16	8	16	16	8	16	16
Timers	Advanced	1			1			1			1			1			1		
	16-bit general-purpose	5			5			5			5			5			5		
	Basic	1			1			1			1			1			1		
	SysTick	1			1			1			1			1			1		
	WDT	1			1			1			1			1			1		
	WWDT	1			1			1			1			1			1		
	ERTC	1			1			1			1			1			1		
Communication	I^2C	2			2			2			2			2			2		
	SPI(1)	1(2)			2			2			2			2			2		
	I^2S (half-duplex)(1)	1(2)			2			2			2			2			2		
	USART+UART	1+1(3)			2+0			2+0			2+0			2+0			2+0		
	IR	1			1			1			1			1			1		
Analog	12-bit ADC numbers/ channels	1			1			1			1			1			1		
		9			10			11			11			10			15		
	Comparator	1			1			1			1			1			1		
GPIO		15			23			27			27			25			39		
Operating temperature		-40 °C to +105 °C																	
Packages		TSSOP20 6.5 x 4.4 mm			QFN28 4 x 4 mm			QFN32 4 x 4 mm			QFN32 5 x 5 mm			LQFP32 7 x 7 mm			LQFP48 7 x 7 mm		

(1) Half-duplex I^2S shares the same pin with SPI.
(2) Only SPI1/I^2S1 exists on TSSOP20.
(3) All pins of USART2 are available on TSSOP20 package. USART1 only has TX and RX pins and is used as UART.

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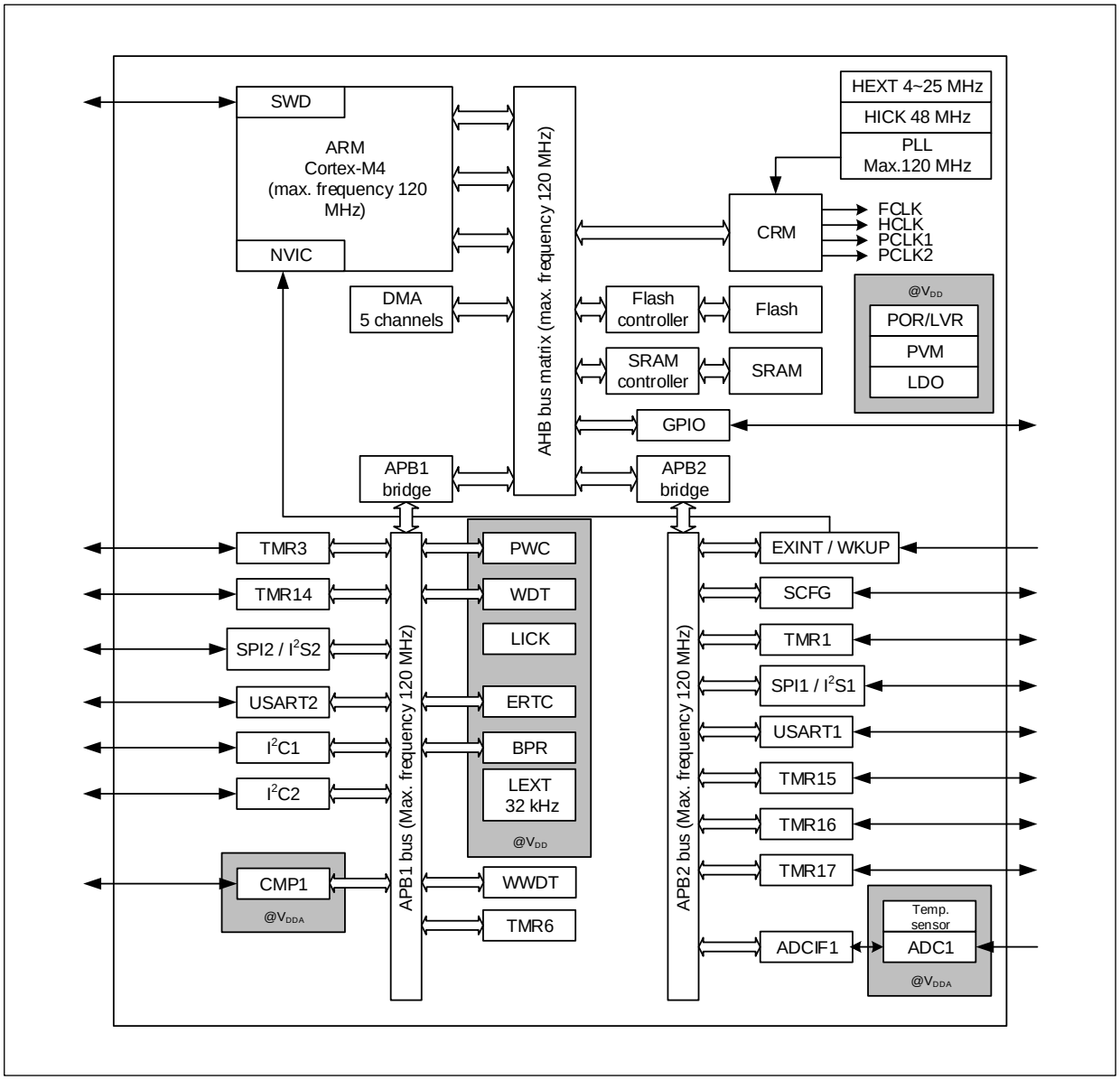
2 Functionality overview

2.1 ARM®Cortex®-M4

The ARM®Cortex®-M4 processor is the latest generation of ARM® processors for embedded systems. It is a 32-bit RISC processor featuring exceptional code efficiency, outstanding computational performance and advanced response to interrupts. The processor supports a set of DSP instructions which enable efficient signal processing and complex algorithm execution.

Figure 1 shows the general block diagram of the AT32F421.

Figure 1. AT32F421 block diagram



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2.2 Memory

2.2.1 Internal Flash memory

Up to 64 Kbytes of embedded Flash is available for storing programs and data. Users can configure any part of the embedded Flash memory protected by the sLib, functioning as a security area with code-executable only but non-readable. “sLib” is a mechanism that protects the intelligence of solution venders and facilitates the second-level development by customers.

The AT32F421 series embeds 4 Kbytes of boot memory, in which the Bootloader is resided.

A User System Data block is included, which is used as configuration of the hardware behaviors such as read/erase/write protection and watchdog self-enable. User System Data allows to set erase/write and read protection individually, in which access protection contains two levels.

2.2.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area consists of up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory. The MPU is especially suited to the applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system).

2.2.3 Embedded SRAM

Up to 16 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.3 Interrupts

2.3.1 Nested vectored interrupt controller (NVIC)

The AT32F421 embeds a nested vectored interrupt controller able to manage 16 priority levels and handle maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4. This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.2 External interrupts (EXINT)

The external interrupt (EXINT), which is connected directly with NVIC, consists of 20 edge detector lines used to generate interrupt requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The external interrupt lines connects up to 16 GPIOs.

2.4 Power control (PWC)

2.4.1 Power supply schemes

- V_{DD} = 2.4 ~ 3.6 V: used as a power supply for GPIOs, ERTC, external 32 kHz crystal (LEXT), battery powered register (BPR) and the internal block such as regulator (LDO) through V_{DD} pin.
- V_{DDA} = 2.4 ~ 3.6 V: used as a power supply for ADC and CMP through V_{DDA} pin. V_{DDA} and V_{SSA} must be the same voltage potential as V_{DD} and V_{SS}, respectively.

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2.4.2 Reset and power voltage monitoring (POR / LVR / PVM)

The device has an integrated power-on reset (POR)/low voltage reset (PDR) circuitry. It is always active, and allows proper operation starting from/down to 2.4 V. The device remains in reset mode when V_{DD} is below a specified threshold (V_{LVR}) without the need for an external reset circuit.

The device embeds a power voltage monitor (PVM) that monitors the V_{DD} power supply and compares it to the V_{PVM} threshold. An interrupt is generated when V_{DD} drops below the V_{PVM} threshold and/or when V_{DD} rises above the V_{PVM} threshold. The PVM is enabled by software.

2.4.3 Voltage regulator (LDO)

The LDO has three operation modes: normal, low-power, and power down.

- Normal mode is used in Run/Sleep mode and in the Deepsleep mode.
- Low-power mode can be used in the Deepsleep mode.
- Power down mode is used in Standby mode: The LDO output is in high impedance and the kernel circuitry is powered down but the contents of the registers and SRAM are lost.

The LDO operates always in its normal mode after reset.

2.4.4 Low-power modes

The AT32F421 supports three low-power modes:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Deepsleep** mode

  Deepsleep mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the LDO domain are stopped, disabling the PLL, the HICK clock, and the HEXT crystal. The voltage regulator can also be put in normal or low-power mode. The device can be woken up from Deepsleep mode by any of the EXINT line. The EXINT line source can be one of the 16 external lines, the PVM output, the ERTC alarm/tamper detection/time stamp, or the CMP wakeup.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire LDO domain is powered off. The PLL, the HICK clock and the HEXT crystal are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the BPR domain and ERTC domain.
  The device exits Standby mode when an external reset (NRST pin), a WDT reset, a rising edge on the WKUPx pin, or an ERTC alarm /tamper detection/time stamp occurs.

Note: The corresponding clock sources of ERTC and WDT are not stopped by entering Deepsleep or Standby mode.

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2.5 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash memory;
- Boot from boot memory;
- Boot from embedded SRAM.

The bootloader is stored in boot memory. It is used to reprogram the Flash memory through USART1 or USART2. *Table 3* provides the supporting interfaces of the Bootloader regarding AT32F421 part numbers and pin configurations.

Table 3. Bootloader supporting part numbers and pin configurations

Interfaces	Pins
USART1	PA9: USART1_TX PA10: USART1_RX
USART2	PA2: USART2_TX PA3: USART2_RX

2.6 Clock

The internal 48 MHz clock (HICK) through a divided-by-6 divider (8 MHz) is selected as default CPU clock after any reset. An external 4 to 25 MHz clock (HEXT) can be selected, in which case it is monitored for failure. If failure is detected, HEXT will be switched off and the system automatically switches back to the internal HICK. A software interrupt is generated. Similarly, the system take the same action once HEXT fails when it is used as the source of PLL.

Several prescalers are used for the configuration of the AHB and the APB (APB1 and APB2) frequency. The maximum frequency of the AHB domain is 120 MHz.

2.7 General-purpose inputs/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down), or as multiple function. Most of the GPIO pins are shared with digital or analog multiple functions. All GPIOs are high current-capable.

The GPIO’s configuration can be locked, if needed, in order to avoid spurious writing to the GPIO’s registers by following a specific sequence.

2.8 Direct Memory Access Controller (DMA)

The flexible 5-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers.

The DMA controller supports circular buffer management, without the need of the intervention of user code when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and the number of transfers between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2S, I^2C, USART, all timers TMRx (except TMR14) and ADC.

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2.9 Timers (TMR)

The AT32F421 devices include one advanced timer, up to five general-purpose timers, one basic timer and a SysTick timer.

The table below compares the features of the advanced, general-purpose, and basic timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced	TMR1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TMR3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TMR14	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	1	No
	TMR15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
	TMR16 TMR17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TMR6	16-bit	Up	Any integer between 1 and 65536	Yes	No	No

2.9.1 Advanced timer (TMR1)

The advanced timer (TMR1) can be seen as a three-phase PWM multiplexed assigned to 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be used as a complete general-purpose timer. These four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-cycle mode output

If configured as a standard 16-bit timer, it has the same features as the TMRx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TMR which have the same architecture. The advanced timer can therefore work together with the TMR timers via the link feature for synchronization or event chaining.

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2.9.2 General-purpose timers (TMR3, TMR14, TMR15, TMR16 and TMR17)

There are 5 synchronizable general-purpose timers embedded in the AT32F421.

- **TMR3**

  The TMR3 timer is based on a 16-bit auto-reload upcounter/downcounter and a 16-bit prescaler. They can offer four independent channels on the largest package. Each channel can be used for input capture/output compare, PWM or one-cycle mode output.

  It can work together with the advanced timers via the link feature for synchronization or event chaining. In debug mode, the counter can be frozen. TMR3 can be used to generate PWM outputs. It has an individual DMA request mechanism.

  TMR3 is also capable of handling incremental encoder signals and the digital outputs coming from 1 to 3 hall-effect sensors.

- **TMR14**

  The TMR14 timer is based on a 16-bit auto-reload upcounter, a 16-bit prescaler, and one independent channels for input capture/output compare, PWM, or one-cycle mode output. It can not only be synchronized with full-featured general-purpose timers, and but also can be used as simple time bases. In debug mode, the counter can be frozen.

- **TMR15, TMR16 and TMR17**

  These three timers are based on a 16-bit auto-reload upcounter, a 16-bit prescaler. TMR15 features two channels and one complementary channel. TMR16 and TMR17 have one channel and one complementary channel, respectively. All channels can be used for input capture/output compare, PWM, or one-pulse mode output.

  They can work together via the Timer link feature for synchronization or event chaining.

  In debug mode, the counter can be frozen. These timers have independent DMA request generation.

2.9.3 Basic timer (TMR6)

This timer is used as a generic 16-bit time base.

2.9.4 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features include:

- A 24-bit downcounter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source (HCLK or HCLK/8)

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2.10 Watchdog (WDT)

The watchdog consists of a 12-bit downcounter and 8-bit prescaler. It is clocked by an independent internal LICK clock. As it operates independently from the main clock, it can operate in Deepsleep and Standby modes. It can be used either as a watchdog to reset the device when an error occurs, or as a free running timer for application timeout management. It is self-enabling or not through the User System Data configuration. The counter can be frozen in debug mode.

2.11 Window watchdog (WWDT)

The window watchdog embeds a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.12 Enhanced real-time clock (ERTC) and battery powered registers (BPR)

The battery powered domain includes:

- Enhanced real-time clock (ERTC)
- 5 x 32-bit battery powered registers

The enhanced real-time clock (ERTC) is an independent BCD timer/counter. It supports the following features:

- Calendar with second, minute, hour (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- The sub-seconds value is also available in binary format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Programmable alarms with wake up from Stop or Standby mode capability.
- To compensate quartz crystal inaccuracy, ERTC can be calibrated via a 512 Hz external output.

The alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. Other 32-bit registers also contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The battery powered registers are 32-bit registers used to store 20 bytes of user application data. Battery powered registers are not reset by a system, or when the device wakes up from the Standby mode.

2.13 Communication interfaces

2.13.1 Serial peripheral interface (SPI)

Two SPIs are able to communicate up to 36 Mbits/s in master and slave modes in full-duplex and half-duplex communication modes. The prescaler gives different master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC/SDHC modes. Both SPIs can be served by the DMA controller.

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2.13.2 Inter-integrated sound interface (I^2S)

Two standard I^2S interfaces (multiplexed with SPI) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/24/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When any of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency. Both I^2S can be served by the DMA controller.

2.13.3 Universal synchronous / asynchronous receiver transmitters (USART)

The AT32F421 embeds two universal synchronous/asynchronous receivers/transmitters (USART1 and USART2).

These two USART interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, master synchronous communication, single-wire half-duplex communication mode, and have LIN Master/Slave capability. These two USART interfaces also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant). These two USART interfaces can be served by the DMA controller. TX/RX pins are swappable configuration.

Two USARTs are able to communicate at speeds of up to 7.5 Mbit/s.

2.13.4 Inter-integrated-circuit interface (I^2C)

Two I^2C bus interfaces can operate in multi-master and slave modes. They can support standard (up to 100 Kbit/s) and fast modes (up to 400 Kbit/s). The I^2C bus frequency can be increased up to 1 MHz. For more details, please contact your nearest Artery sales office for technical support.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is included.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.13.5 Infrared transmitter (IRTMR)

The AT32F421 device provides an infrared transmitter solution. The solution is based on the internal connection between TMR16, USART1 or USART2 and TMR17. TMR17 is used to provide the carrier frequency, and TMR16, USART1 or USART2 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate infrared remote control signals, TMR16 channel 1 and TMR17 channel 1 must be correctly configured to generate the correct waveform. All standard IR pulse modulation modes can be obtained by programming two timer output compare channels.

2.14 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity.

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2.15 Analog-to-digital converter (ADC)

One 12-bit analog-to-digital converter is embedded into AT32F421 devices and it has up to 15 external channels and 3 internal channels (temperature sensor V_{TS}, internal reference voltage V_{REFINT}, and V_{SSA}). In sequence mode, automatic conversion is performed on a selected group of analog channels. The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TMRx) and the advanced timer (TMR1) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize ADC conversion and timers.

2.15.1 Temperature sensor (V_{TS})

The temperature sensor has to generate a voltage V_{TS} that varies linearly with temperature. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The offset of this line varies from chip to chip due to process variation. The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.

2.15.2 Internal reference voltage (V_{INTRV})

The internal reference voltage (V_{INTRV}) provides a stable voltage source for ADC. The V_{INTRV} is internally connected to the ADC1_IN17 input channel.

2.16 Comparator (CMP)

The AT32F421 embeds one rail-to-rail comparator with programmable reference voltage (internal or external), hysteresis, speed, selectable output polarity, output blanking and noise filter.

The reference voltage can be one of the following:

- External GPIO
- Internal reference voltage (V_{INTRV}) or submultiple (1/4, 1/2, 3/4)

The comparator can wake up from Deepsleep mode, and also can remap outputs on timers.

2.17 Serial wire debug (SWD)

The ARM® SWD interface is embedded, and is a serial wire debug port that enables a serial wire debug to be connected to the target to implement the programming and debugging of the target.

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3 Pin functional definitions

Figure 2. AT32F421 LQFP48 pinout

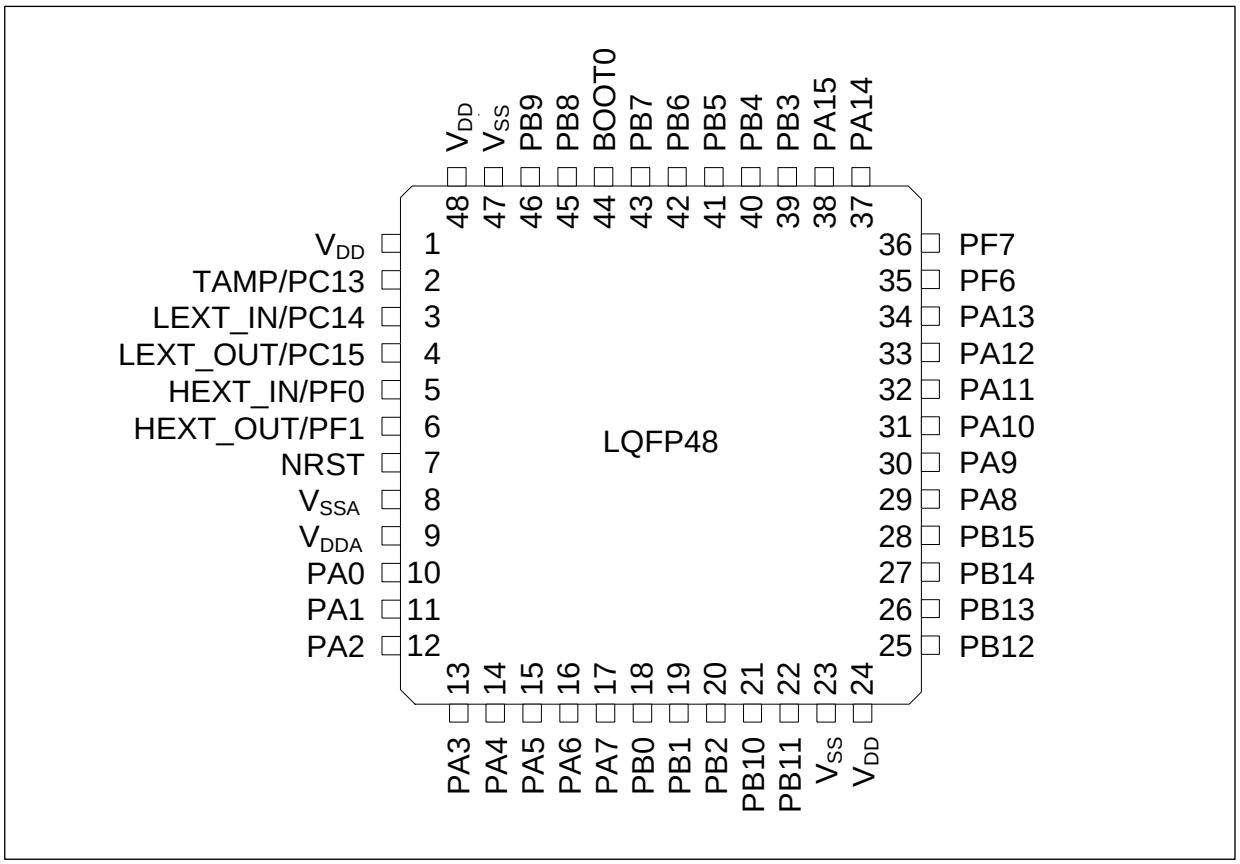
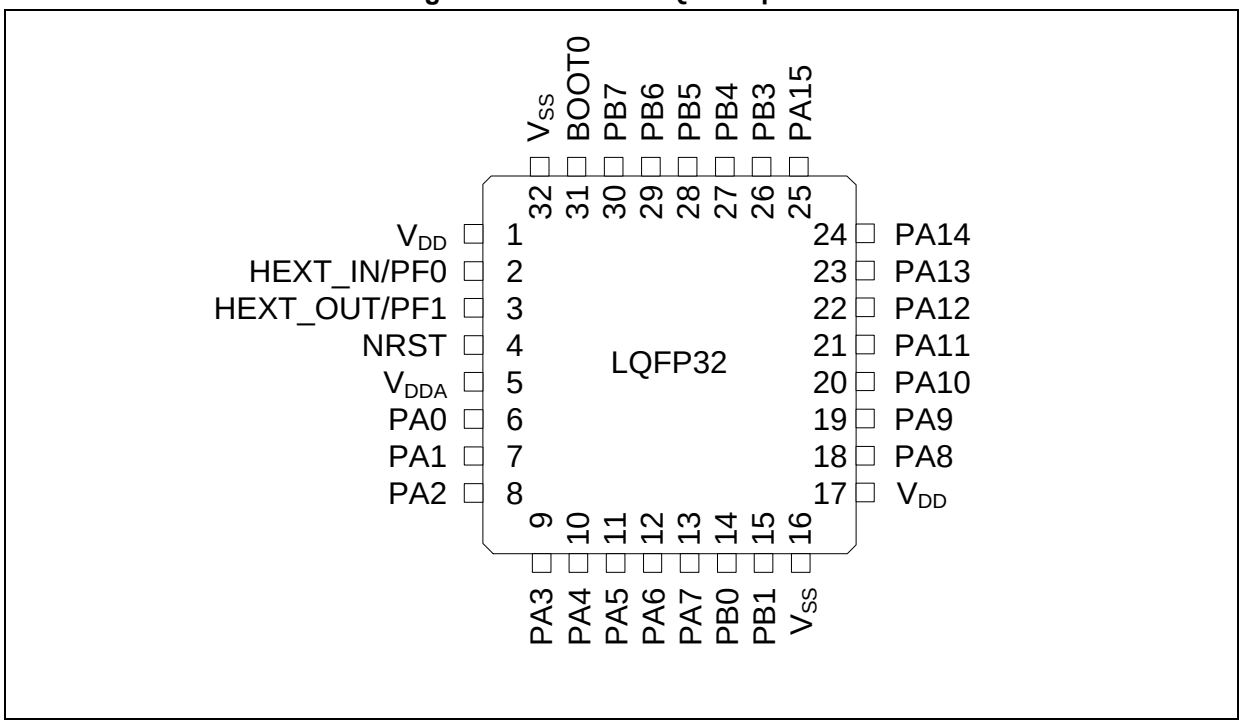


Figure 3. AT32F421 LQFP32 pinout



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Figure 4. AT32F421 QFN32 pinout

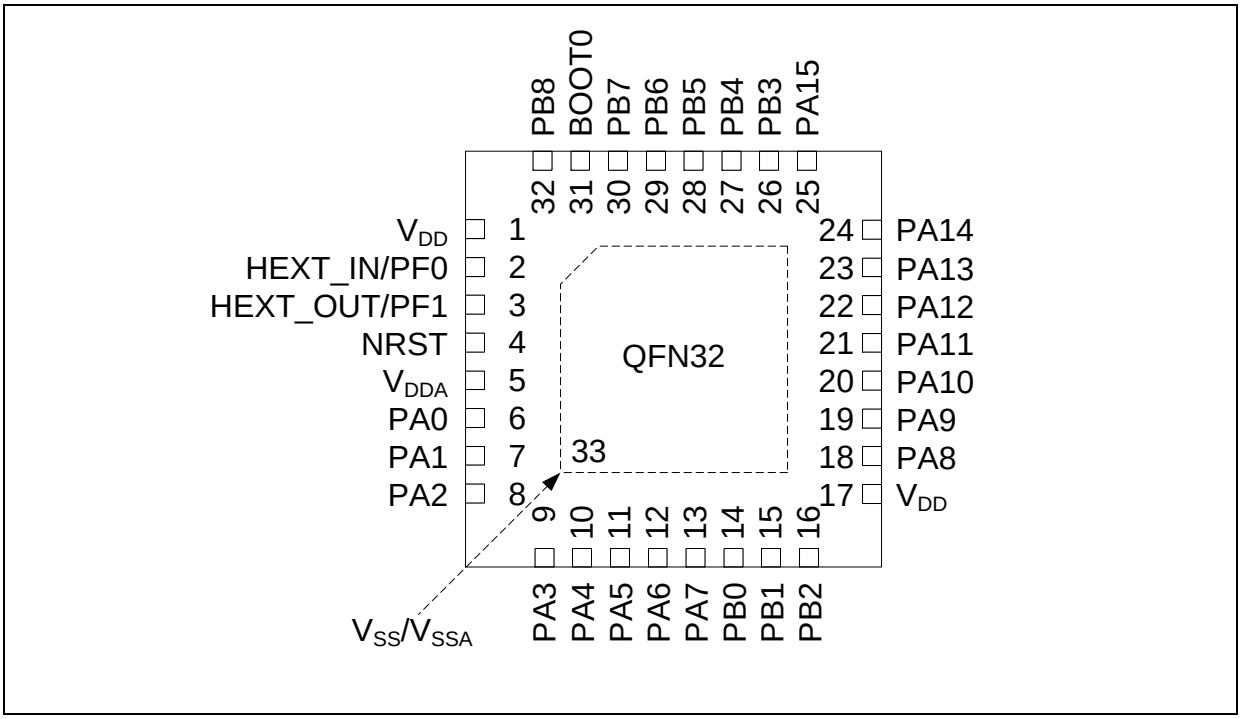
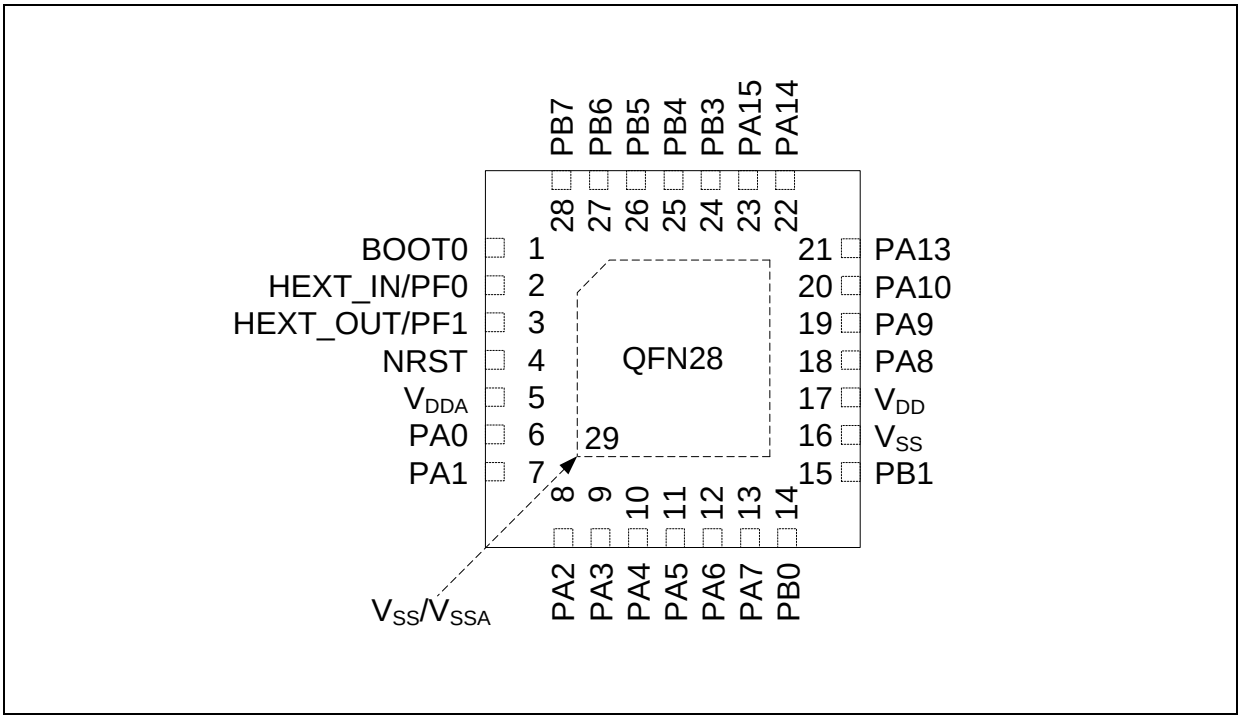
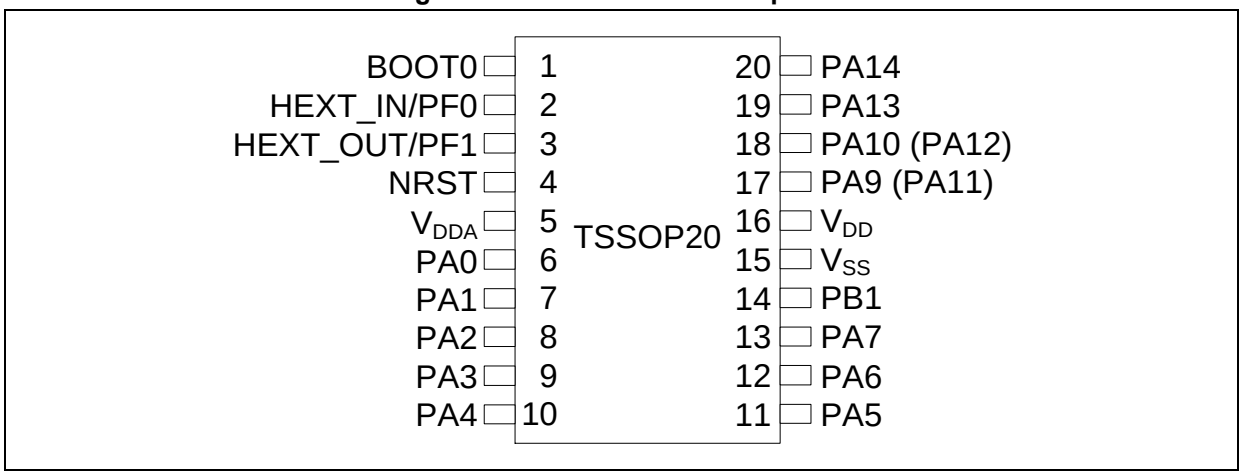


Figure 5. AT32F421 QFN28 pinout



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Figure 6. AT32F421 TSSOP20 pinout



The table below is the pin definition of the AT32F421. "-" presents there is no such pinout on the related package. Unless otherwise specified, the pins during and after reset have the same functions as those of actual ones, and all GPIOs are configured as floating input during and after reset. Alternate functions of pins are enabled through the GPIOx_MUXx register, and additional functions are selected through peripheral registers.

Table 5. AT32F421 series pin definitions

Pin number					Pin name (after reset)	Pin type (1)	GPIO structure(2)	Alternate function	Additional function
TSSOP20	QFN28	QFN32	LQFP32	LQFP48					
-	-	1	1	1	V_{DD}	S	-	Digital power supply	
-	-	-	-	2	PC13	I/O	FT	-	TAMP1 / WKUP2
-	-	-	-	3	PC14 / LEXT_IN (PC14)	I/O	TC	-	LEXT_IN
-	-	-	-	4	PC15 / LEXT_OUT (PC15)	I/O	TC	-	LEXT_OUT
2	2	2	2	5	PF0 / HEXT_IN (PF0)	I/O	TC	I2C1_SDA	HEXT_IN
3	3	3	3	6	PF1 / HEXT_OUT (PF1)	I/O	TC	I2C1_SCL	HEXT_OUT
4	4	4	4	7	NRST	I/O	R	Device reset input / internal reset output (active low)	
-	-	-	-	8	V_{SSA} / V_{REF-}	S	-	Analog ground / negative reference voltage	
5	5	5	5	9	V_{DDA} / V_{REF+}	S	-	Analog power supply / positive reference voltage	
6	6	6	6	10	PA0	I/O	FTa	TMR1_EXT / USART2_CTS / I2C2_SCL / CMP1_OUT	ADC1_IN0 / CMP1_INP2 / CMP1_INM6 / WKUP1
7	7	7	7	11	PA1	I/O	FTa	TMR15_CH1C / USART2_RTS / I2C2_SDA / EVENTOUT	ADC1_IN1 / CMP1_INP1
8	8	8	8	12	PA2	I/O	FTa	TMR15_CH1 / USART2_TX	ADC1_IN2 / CMP1_INM7
9	9	9	9	13	PA3	I/O	FTa	TMR15_CH2 / USART2_RX / I2S2_MCK	ADC1_IN3
10	10	10	10	14	PA4	I/O	FTa	TMR14_CH1 / USART2_CK / SPI1_CS / I2S1_WS	ADC1_IN4/ CMP1_INM4
11	11	11	11	15	PA5	I/O	FTa	SPI1_SCK / I2S1_CK	ADC1_IN5 / CMP1_INP0 / CMP1_INM5

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Pin number					Pin name (after reset)	Pin type (1)	GPIO structure(2)	Alternate function	Additional function
TSSOP20	QFN28	QFN32	LQFP32	LQFP48					
12	12	12	12	16	PA6	I/O	FTa	TMR1_BRK / TMR3_CH1 / TMR16_CH1 / SPI1_MISO / I2S1_MCK / I2S2_MCK / CMP1_OUT / EVENTOUT	ADC1_IN6
13	13	13	13	17	PA7	I/O	FTa	TMR1_CH1C / TMR3_CH2 / TMR14_CH1 / TMR17_CH1 / SPI1_MOSI / I2S1_SD / EVENTOUT	ADC1_IN7
-	14	14	14	18	PB0	I/O	FTa	TMR1_CH2C / TMR3_CH3 / USART2_RX / I2S1_MCK / EVENTOUT	ADC1_IN8
14	15	15	15	19	PB1	I/O	FTa	TMR1_CH3C / TMR3_CH4 / TMR14_CH1 / SPI2_SCK / I2S2_CK	ADC1_IN9
-	-	16	-	20	PB2	I/O	FTa	TMR3_EXT	ADC1_IN10
-	-	-	-	21	PB10	I/O	FT	SPI2_SCK / I2S2_CK / I2C2_SCL	-
-	-	-	-	22	PB11	I/O	FT	I2C2_SDA / EVENTOUT	-
15	16	-	16	23	V_{SS}	S	-	Digital ground	
16	17	17	17	24	V_{DD}	S	-	Digital power supply	
-	-	-	-	25	PB12	I/O	FTa	TMR1_BRK / TMR15_BRK / SPI2_CS / I2S2_WS / I2C2_SMBA / EVENTOUT	ADC1_IN11
-	-	-	-	26	PB13	I/O	FTa	TMR1_CH1C / SPI2_SCK / I2S2_CK / I2C2_SCL	ADC1_IN12
-	-	-	-	27	PB14	I/O	FTa	TMR1_CH2C / TMR15_CH1 / SPI2_MISO / I2S2_MCK / I2C2_SDA	ADC1_IN13
-	-	-	-	28	PB15	I/O	FTa	TMR1_CH3C / TMR15_CH2 / TMR15_CH1C / SPI2_MOSI / I2S2_SD	ADC1_IN14 / ERTC_REFIN / WKUP7
-	18	18	18	29	PA8	I/O	FT	TMR1_CH1 / USART1_CK / USART2_TX / I2C2_SCL / CLKOUT / EVENTOUT	-
17	19	19	19	30	PA9	I/O	FT	TMR1_CH2 / TMR15_BRK / USART1_TX / I2C1_SCL / I2C2_SMBA / CLKOUT	-
18	20	20	20	31	PA10	I/O	FT	TMR1_CH3 / TMR17_BRK / USART1_RX / I2C1_SDA	-
17(3)	-(4)	21	21	32	PA11	I/O	FT	TMR1_CH4 / USART1_CTS / I2C1_SMBA / I2C2_SCL / CMP1_OUT / EVENTOUT	-
18(3)	-(4)	22	22	33	PA12	I/O	FT	TMR1_EXT / USART1_RTS / I2C2_SDA / EVENTOUT	-
19	21	23	23	34	PA13 (SWDIO(5))	I/O	FT	PA13 / IR_OUT / SPI2_MISO / I2S2_MCK	-
-	-	-	-	35	PF6	I/O	FT	I2C2_SCL	-
-	-	-	-	36	PF7	I/O	FT	I2C2_SDA	-

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Pin number					Pin name (after reset)	Pin type (1)	GPIO structure(2)	Alternate function	Additional function
TSSOP20	QFN28	QFN32	LQFP32	LQFP48					
20	22	24	24	37	PA14 (SWCLK(5))	I/O	FT	PA14 / USART2_TX / SPI2_MOSI / I2S2_SD	-
-	23	25	25	38	PA15	I/O	FT	USART2_RX / SPI1_CS / I2S1_WS / SPI2_CS / I2S2_WS / EVENTOUT	-
-	24	26	26	39	PB3	I/O	FT	SPI1_SCK / I2S1_CK / SPI2_SCK / I2S2_CK / EVENTOUT	-
-	25	27	27	40	PB4	I/O	FT	TMR3_CH1 / TMR17_BRK / SPI1_MISO / I2S1_MCK / SPI2_MISO / I2S2_MCK / I2C2_SDA / EVENTOUT	-
-	26	28	28	41	PB5	I/O	FT	TMR3_CH2 / TMR16_BRK / SPI1_MOSI / I2S1_SD / SPI2_MOSI / I2S2_SD / I2C1_SMBA	WKUP6
-	27	29	29	42	PB6	I/O	FT	TMR16_CH1C / USART1_TX / I2S1_MCK / I2C1_SCL	-
-	28	30	30	43	PB7	I/O	FT	TMR17_CH1C / USART1_RX / I2C1_SDA	-
1	1	31	31	44	BOOT0	I	B	Boot mode selection 0	
-	-	32	-	45	PB8	I/O	FT	TMR16_CH1 / I2C1_SCL	-
-	-	-	-	46	PB9	I/O	FT	TMR17_CH1 / IR_OUT / SPI2_CS / I2S2_WS / I2S1_MCK / I2C1_SDA / EVENTOUT	-
-	-	-	32	47	V_{SS}	S	-	Digital ground	
-	-	-	-	48	V_{DD}	S	-	Digital power supply	
-	29	33	-	-	EPAD (V_{SS}/V_{SSA})	S	-	Digital ground / Analog ground	

(1) I = input, O = output, S = supply.

(2) TC = standard level, FT = general 5 V-tolerant, FTa = 5 V-tolerant with analog functions, R = bidirectional reset pin with embedded weak pull-up resistor, B = dedicated BOOT0 pin with embedded weak pull-down resistor. FTa is a 5 V-tolerant pin when set as input floating, input pull-up, or input pull-down; when set as analog mode, it loses 5 V tolerant characteristic, and in this case, the input level must be less than VDD + 0.3 V.

(3) For TSSOP20 package, PA11/PA12 and its alternate function can be remapped to replace the original PA9/PA10 and its alternate function by software.

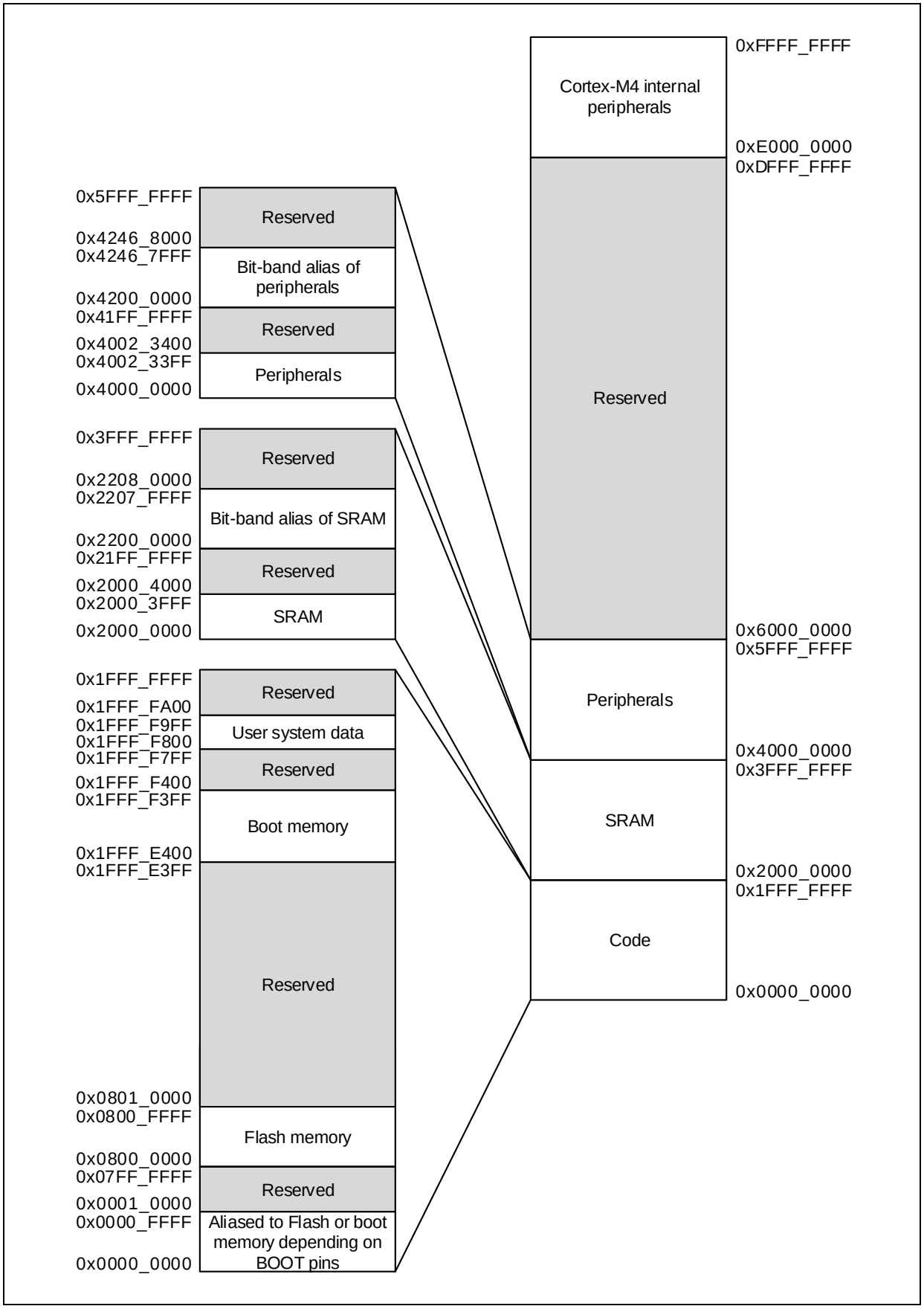
(4) For QFN28 package, PA11 and PA12 should be treated as unconnected pins (even they are not available on the package). They are not forced to a defined level by hardware. It is suggested to configure the state of these two pins as a low level output to prevent unnecessary current leakage.

(5) After reset, PA13/PA14 pin is configured as alternate function SWDIO/SWCLK, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.

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4 Memory mapping

Figure 7. Memory map



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5 Electrical characteristics

5.1 Parameter conditions

5.1.1 Minimum and maximum values

The minimum and maximum values are guaranteed in the worst conditions. Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. The minimum and maximum values represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

5.1.2 Typical values

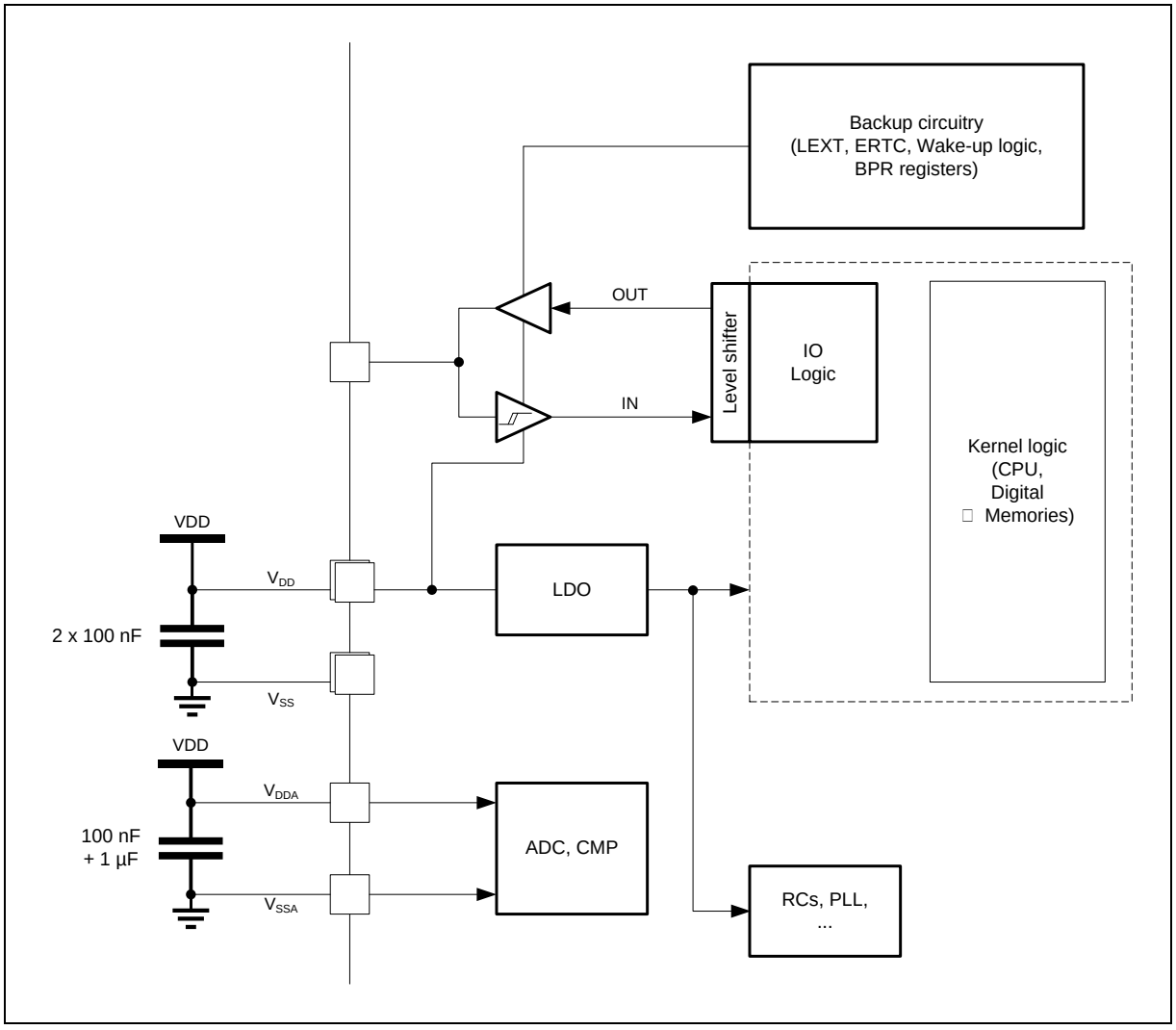
Typical data are based on T_A = 25 °C, V_{DD} = 3.3 V.

5.1.3 Typical curves

All typical curves are given only as design guidelines and are not tested.

5.1.4 Power supply scheme

Figure 8. Power supply scheme



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5.2 Absolute maximum values

5.2.1 Ratings

If stresses were out of the absolute maximum ratings listed *Table 6*, *Table 7* and *Table 8*, it may cause permanent damage to the device. These are maximum stress ratings only that the device could bear, but the functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for an extended period of times may affect device reliability.

Table 6. Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})	-0.3	4.0	V
V_{IN}	Input voltage on FT GPIO	V_{SS}-0.3	6.0	
	Input voltage on FTa GPIO (set as input floating, input pull-up or input pull-down mode)			
	Input voltage on TC GPIO	V_{SS}-0.3	4.0	
	Input voltage on FTa GPIO (set as analog mode)			
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSx}$-$V_{SS}\|$	Variations between all the different ground pins	-	50	

Table 7. Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD} power lines (source)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)	150	
I_{IO}	Output current sunk by any GPIO and control pin	25	
	Output current source by any GPIO and control pin	-25	

Table 8. Temperature characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-60 ~ +150	°C
T_J	Maximum junction temperature	125	

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5.2.2 Electrical sensitivity

Based on three different tests (HBM, CDM, and LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges are applied to the pins of each sample according to each pin combination. This test conforms to the JS-001-2017/JS-002-2018 standard.

Table 9. ESD values

Symbol	Parameter	Conditions	Class	Max	unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforms to JS-001-2017	3A	±6000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforms to JS-002-2018	III	±1000	

Static latch-up

Tests compliant with EIA/JESD78E latch-up standard are required to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin;
- A current injection is applied to each input, output and configurable GPIO pin.

Table 10. Static latch-up values

Symbol	Parameter	Conditions	Level/Class
LU	Static latch-up	T_A = +105 °C, conforms to EIA/JESD78E	II level A (±200 mA)

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5.3 Specification

5.3.1 General operating conditions

Table 11. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	120	MHz
$f_{PCLK1/2}$	Internal APB1/2 clock frequency	-	0	f_{HCLK}	MHz
V_{DD}	Digital operating voltage	-	2.4	3.6	V
V_{DDA}	Analog operating voltage	Must be the same potential as V_{DD}	V_{DD}		V
P_D	Power dissipation: T_A = 105 °C	LQFP48 (7 x 7 mm)	-	230	mW
		LQFP32 (7 x 7 mm)	-	243	
		QFN32 (5 x 5 mm)	-	503	
		QFN32 (4 x 4 mm)	-	446	
		QFN28 (4 x 4 mm)	-	446	
		TSSOP20 (6.5 x 4.4 mm)	-	194	
T_A	Ambient temperature	-	-40	105	°C

5.3.2 Operating conditions at power-up/power-down

Table 12. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	ms/V
	V_{DD} fall time rate		20	∞	μs/V

5.3.3 Embedded reset and power control block characteristics

Table 13. Embedded reset and power control block characteristics (1)

Symbol	Parameter	Min	Typ.	Max	Unit
V_{POR}	Power-on reset threshold	1.73	2.06	2.4	V
V_{LVR}	Low voltage reset threshold	1.62(2)	1.88	2.16	V
$V_{LVRhyst}$	LVR hysteresis	-	180	-	mV
$T_{RESTTEMPO}$	Reset temporization: CPU starts execution after V_{DD} keeps higher than V_{POR} for $T_{RSTTEMPO}$	-	4.5	-	ms

(1) Guaranteed by characterization results, not tested in production.
(2) The product behavior is guaranteed by design down to the minimum V_{LVR} value.

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Figure 9. Power-on reset and low voltage reset waveform

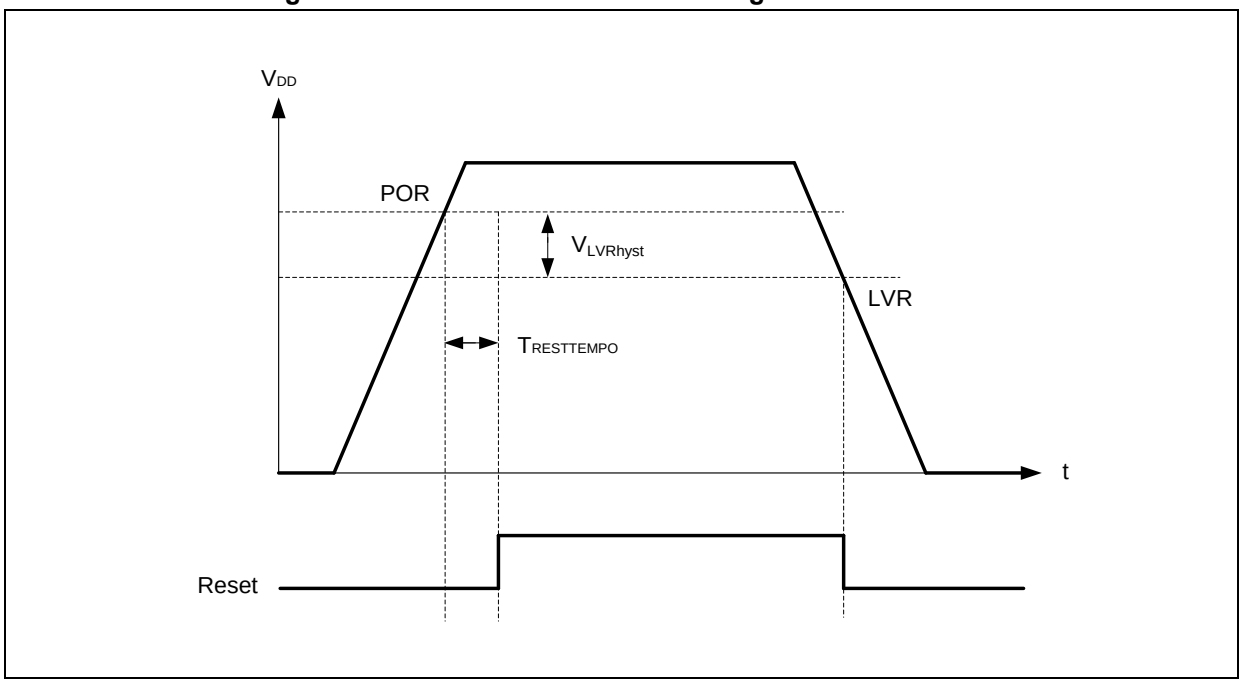


Table 14. Programmable voltage regulator characteristics

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
V_{PVM1}	PVM threshold 1 (PVMSEL[2:0] = 001)	Rising edge(1)	2.19	2.28	2.37	V
		Falling edge(1)	2.09	2.18	2.27	V
V_{PVM2}	PVM threshold 2 (PVMSEL[2:0] = 010)	Rising edge(2)	2.28	2.38	2.48	V
		Falling edge(2)	2.18	2.28	2.38	V
V_{PVM3}	PVM threshold 3 (PVMSEL[2:0] = 011)	Rising edge(2)	2.38	2.48	2.58	V
		Falling edge(2)	2.28	2.38	2.48	V
V_{PVM4}	PVM threshold 4 (PVMSEL[2:0] = 100)	Rising edge(2)	2.47	2.58	2.69	V
		Falling edge(2)	2.37	2.48	2.59	V
V_{PVM5}	PVM threshold 5 (PVMSEL[2:0] = 101)	Rising edge(2)	2.57	2.68	2.79	V
		Falling edge(2)	2.47	2.58	2.69	V
V_{PVM6}	PVM threshold 6 (PVMSEL[2:0] = 110)	Rising edge(2)	2.66	2.78	2.9	V
		Falling edge(2)	2.56	2.68	2.8	V
V_{PVM7}	PVM threshold 7 (PVMSEL[2:0] = 111)	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
V_{HYS_P}(2)	PVM hysteresis	-	-	100	-	mV
$I_{DD\ (PVM)}$(2)	PVM current consumption	-	-	20	30(2)	μA

(1) PVMSEL [2:0] = 001 may not be used because it is lower than V_{POR}.
(2) Guaranteed by characterization results, not tested in production.

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5.3.4 Memory characteristics

Table 15. Internal Flash memory characteristics (1)

Symbol	Parameter	Typ	Max	Unit
T_{PROG}	Programming time	60	65	μs
t_{ERASE}	Page erase time	6.6	8	ms
t_{ME}	Mass erase time	8.2	10	ms

(1) Guaranteed by design, not tested in production.

Table 16. Internal Flash memory endurance and data retention (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{END}	Endurance	T_A = -40 ~ 105 °C	100	-	-	kcycles
t_{RET}	Data retention	T_A = 105 °C	10	-	-	years

(1) Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is subjected to several parameters and factors such as the operating voltage, ambient temperature, GPIO pin loading, device software configuration, operating frequencies, GPIO pin switching rate, and executed binary code. The current consumption is obtained by characterization results, not tested in production.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode.
- Flash memory access time depends on f_{HCLK} (0 ~ 32 MHz: zero-wait state; 33 ~ 64 MHz: one-wait state; 65 ~ 96 MHz: two-wait states; over 96 MHz: three-wait states).
- Prefetch is ON.
- $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/8$.
- Unless otherwise specified, the typical values are measured with V_{DD} = 3.3 V and T_A = 25 °C condition and the maximum values are measured with V_{DD} = 3.6 V.

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Table 17. Typical current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ.		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in Run mode	High-speed external crystal (HEXT) (1)(2)	120 MHz	16.7	11.3	mA
			108 MHz	15.2	10.3	
			72 MHz	10.5	7.19	
			48 MHz	7.62	5.44	
			36 MHz	5.98	4.34	
			24 MHz	4.65	3.54	
			16 MHz	3.45	2.71	
			8 MHz	1.96	1.57	
			4 MHz	1.50	1.30	
			2 MHz	1.27	1.16	
			1 MHz	1.16	1.10	
			500 kHz	1.10	1.07	
			125 kHz	1.06	1.04	
		High-speed internal clock (HICK)	120 MHz	16.7	11.3	mA
			108 MHz	15.1	10.3	
			72 MHz	10.4	7.14	
			48 MHz	7.52	5.38	
			36 MHz	5.88	4.27	
			24 MHz	4.53	3.47	
			16 MHz	3.34	2.63	
			8 MHz	1.83	1.48	
			4 MHz	1.37	1.20	
			2 MHz	1.15	1.06	
			1 MHz	1.03	0.99	
			500 kHz	0.97	0.95	
			125 kHz	0.93	0.93	

(1) External clock is 8 MHz.
(2) PLL is ON when f_{HCLK} > 8 MHz.

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Table 18. Typical current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ.		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	High-speed external crystal (HEXT) (1)(2)	120 MHz	12.2	4.99	mA
			108 MHz	11.1	4.59	
			72 MHz	7.76	3.38	
			48 MHz	5.81	2.89	
			36 MHz	4.60	2.42	
			24 MHz	3.70	2.25	
			16 MHz	2.80	1.83	
			8 MHz	1.60	1.11	
			4 MHz	1.30	1.05	
			2 MHz	1.15	1.02	
			1 MHz	1.07	1.00	
			500 kHz	1.03	0.99	
			125 kHz	1.00	0.98	
		High-speed internal clock (HICK)	120 MHz	12.1	4.88	mA
			108 MHz	11.0	4.47	
			72 MHz	7.65	3.27	
			48 MHz	5.70	2.78	
			36 MHz	4.49	2.30	
			24 MHz	3.59	2.13	
			16 MHz	2.68	1.71	
			8 MHz	1.47	0.98	
			4 MHz	1.17	0.93	
			2 MHz	1.02	0.89	
			1 MHz	0.94	0.88	
			500 kHz	0.90	0.87	
			125 kHz	0.87	0.86	

(1) External clock is 8 MHz.
(2) PLL is ON when f_{HCLK} > 8 MHz.

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Table 19. Maximum current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	Max		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	High-speed external crystal (HEXT) (1) All peripherals enabled	120 MHz	18.9	20.7	mA
			108 MHz	17.3	19.1	
			72 MHz	12.6	14.4	
			48 MHz	9.69	11.5	
			36 MHz	8.04	9.81	
			24 MHz	6.69	8.45	
			16 MHz	5.49	7.24	
			8 MHz	3.99	5.73	
		High-speed external crystal (HEXT) (1) All peripherals disabled	120 MHz	13.5	15.2	mA
			108 MHz	12.4	14.2	
			72 MHz	9.29	11.0	
			48 MHz	7.52	9.26	
			36 MHz	6.41	8.14	
			24 MHz	5.60	7.33	
			16 MHz	4.76	6.49	

(1) External clock is 8 MHz. PLL is ON when f_{HCLK} > 8 MHz.

Table 20. Maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Max		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	High-speed external crystal (HEXT)(1) All peripherals enabled	120 MHz	14.4	16.1	mA
			108 MHz	13.3	15.0	
			72 MHz	9.85	11.6	
			48 MHz	7.89	9.58	
			36 MHz	6.69	8.36	
			24 MHz	5.79	7.45	
			16 MHz	4.88	6.53	
			8 MHz	3.68	5.31	
		High-speed external crystal (HEXT)(1) All peripherals disabled	120 MHz	7.06	8.70	mA
			108 MHz	6.66	8.30	
			72 MHz	5.45	7.09	
			48 MHz	4.96	6.57	
			36 MHz	4.48	6.12	
			24 MHz	4.31	5.93	
			16 MHz	3.89	5.53	
			8 MHz	3.18	4.81	

(1) External clock is 8 MHz. PLL is ON when f_{HCLK} > 8 MHz.

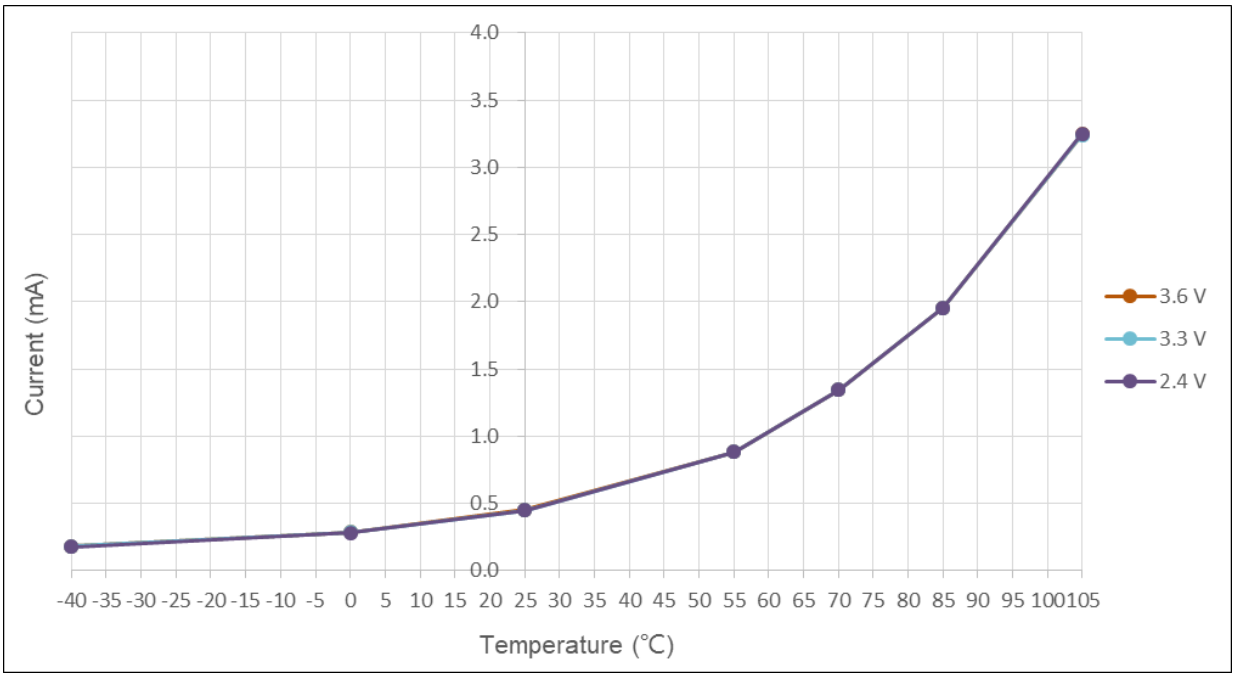
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Table 21. Typical and maximum current consumption in Deepsleep and Standby modes

Symbol	Parameter	Conditions	Typ (1)		Max(2)			Unit
			V_{DD} = 2.4 V	V_{DD} = 3.3 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Deepsleep mode (3)	LDO in Run mode, HICK and HEXT OFF, WDT disabled	445	450	See (4)	4100	6750	µA
		LDO in low-power mode, LPDS1=1, HICK and HEXT OFF, WDT disabled	205	210		2000	3315	
	Supply current in Standby mode	LEXT and ERTC OFF	2.4	3.6	4.6	5.9	7.6	µA
		LEXT and ERTC ON	3.2	5.1	5.9	7.2	9.2	

(1) Typical values are measured at T_A = 25 °C.
(2) Guaranteed by characterization results, not tested in production.
(3) Before entering Deepsleep mode, CRM_AHBEN[4] (FLASHEN) must be set to 1; otherwise, an additional 50 µA of current consumption is generated for typical values.
(4) This value may be several times the typical value due to process variations.

Figure 10. Typical current consumption in Deepsleep mode with LDO in Run mode vs. temperature at different V_{DD}



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Figure 11. Typical current consumption in Deepsleep mode with LDO in low-power mode vs. temperature at different V_{DD}

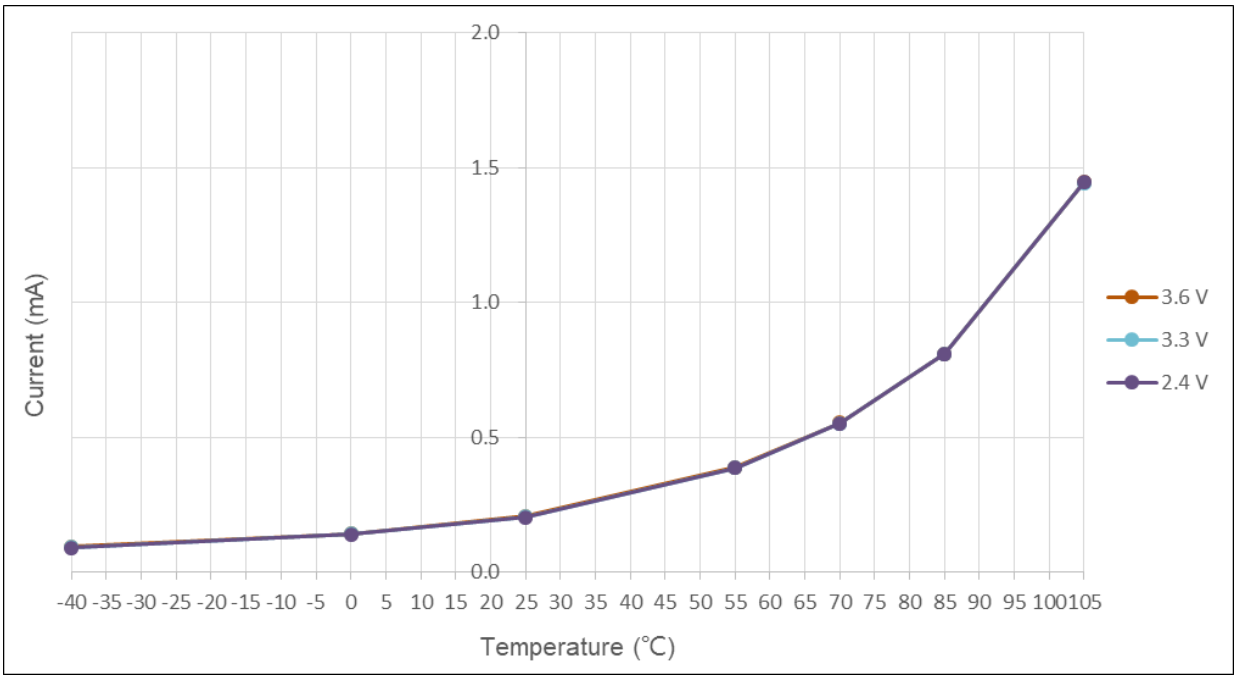
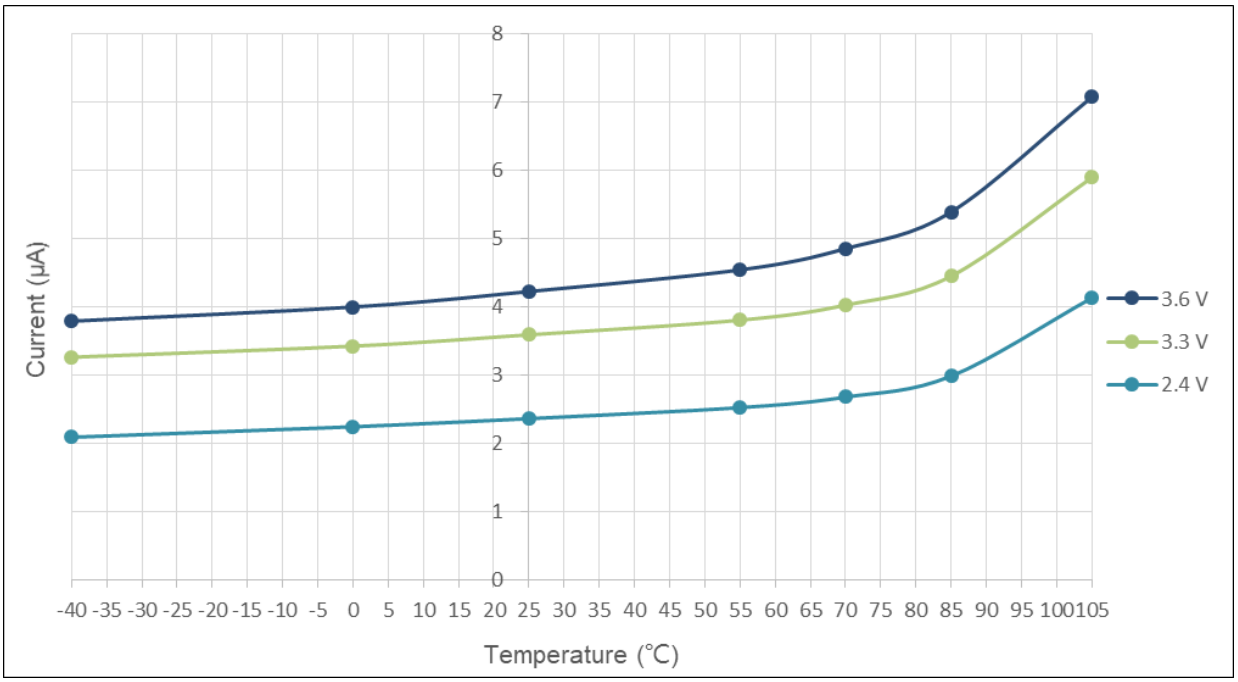


Figure 12. Typical current consumption in Standby mode vs. temperature at different V_{DD}



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On-chip peripheral current consumption

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode.
- The given value is calculated by measuring the current consumption difference between “all peripherals clocked OFF” and “only one peripheral clocked ON”.

Table 22. Peripheral current consumption

Peripheral		Typ	Unit
AHB	DMA1	2.15	μA/MHz
	SRAM	1.06	
	Flash	12.08	
	GPIOA	0.50	
	GPIOB	0.50	
	GPIOC	0.50	
	GPIOF	0.50	
	CRC	0.70	
APB1	TMR3	6.29	
	TMR6	0.49	
	TMR14	2.28	
	SPI2/I^2S2	2.26	
	USART2	2.11	
	I^2C1	1.71	
	I^2C2	1.68	
	WWDT	0.20	
	PWC	0.39	
APB2	SCFG/CMP1	0.29	
	SPI1/I^2S1	2.03	
	USART1	2.12	
	TMR1	7.68	
	TMR15	4.65	
	TMR16	3.19	
	TMR17	3.41	
	ADC1	5.17	

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5.3.6 External clock source characteristics

High-speed external clock generated from a crystal / ceramic resonator

The high-speed external (HEXT) clock can be supplied with a 4 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

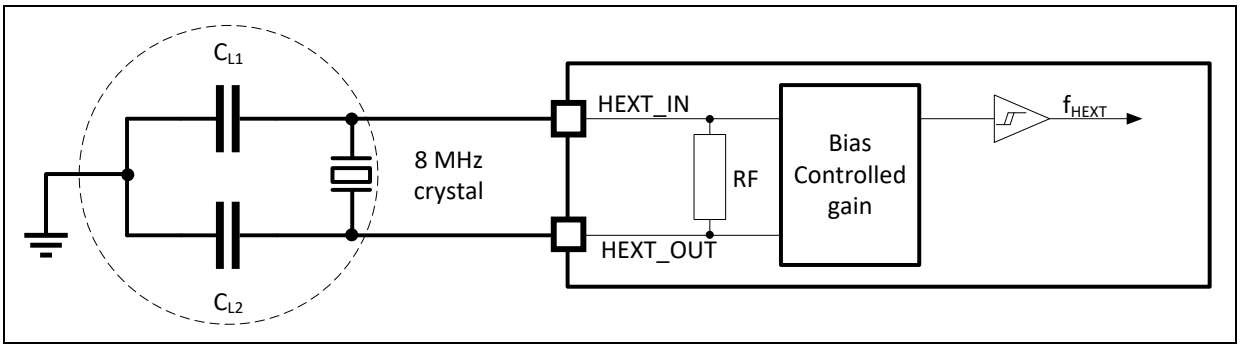
Table 23. HEXT 4 ~ 25 MHz crystal characteristics (1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HEXT_IN}	Oscillator frequency	-	4	8	25	MHz
$t_{SU(HEXT)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	ms

(1) Oscillator characteristics given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.
(3) $t_{SU(HEXT)}$ is the startup time measured from the moment HEXT is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Figure 13. HEXT typical application with an 8 MHz crystal



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High-speed external clock generated from an external source

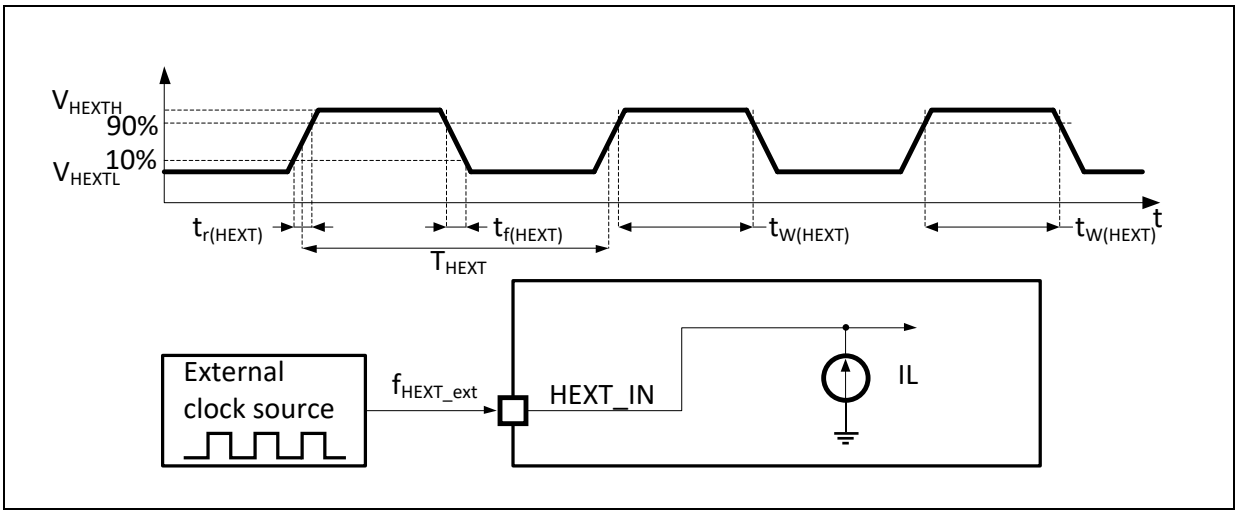
The characteristics given in the table below result from tests performed using a high-speed external clock source.

Table 24. HEXT external source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HEXT_ext}	User external clock source frequency (1)	-	1	8	25	MHz
V_{HEXTH}	HEXT_IN input pin high level voltage		0.7V_{DD}	-	V_{DD}	V
V_{HEXTL}	HEXT_IN input pin low level voltage		V_{SS}	-	0.3V_{DD}	
$t_{w(HEXT)}$ $t_{w(HEXT)}$	HEXT_IN high or low time(1)		5	-	-	ns
$t_{r(HEXT)}$ $t_{f(HEXT)}$	HEXT_IN rise or fall time(1)		-	-	20	
$C_{in(HEXT)}$	HEXT_IN input capacitance(1)	-	-	5	-	pF
$Duty_{(HEXT)}$	Duty cycle	-	45	-	55	%
I_L	HEXT_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

(1) Guaranteed by design, not tested in production.

Figure 14. HEXT external source AC timing diagram



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Low-speed external clock generated from a crystal / ceramic resonator

The low-speed external (LEXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 25. LEXT 32.768 kHz crystal characteristics (1)(2)

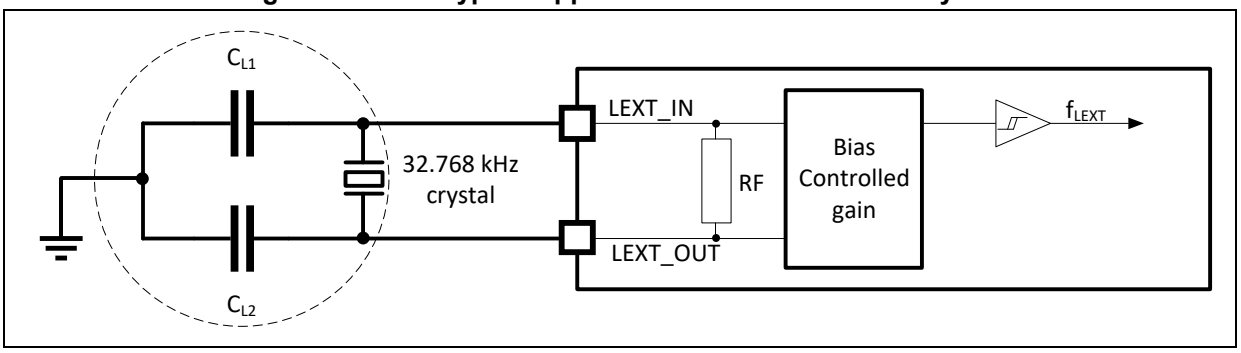
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU(LEXT)}$	Startup time	V_{DD} is stabilized	-	180	-	ms

(1) Oscillator characteristics are given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.

For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 20 pF range selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.

Load capacitance C_L has the following formula: CL = CL1 x CL2 / (CL1 + CL2) + Cstray, where Cstray is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Figure 15. LEXT typical application with a 32.768 kHz crystal



Note: No external resistor is required between LEXT_IN and LEXT_OUT, and it is also prohibited to add it.

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Low-speed external clock generated from an external source

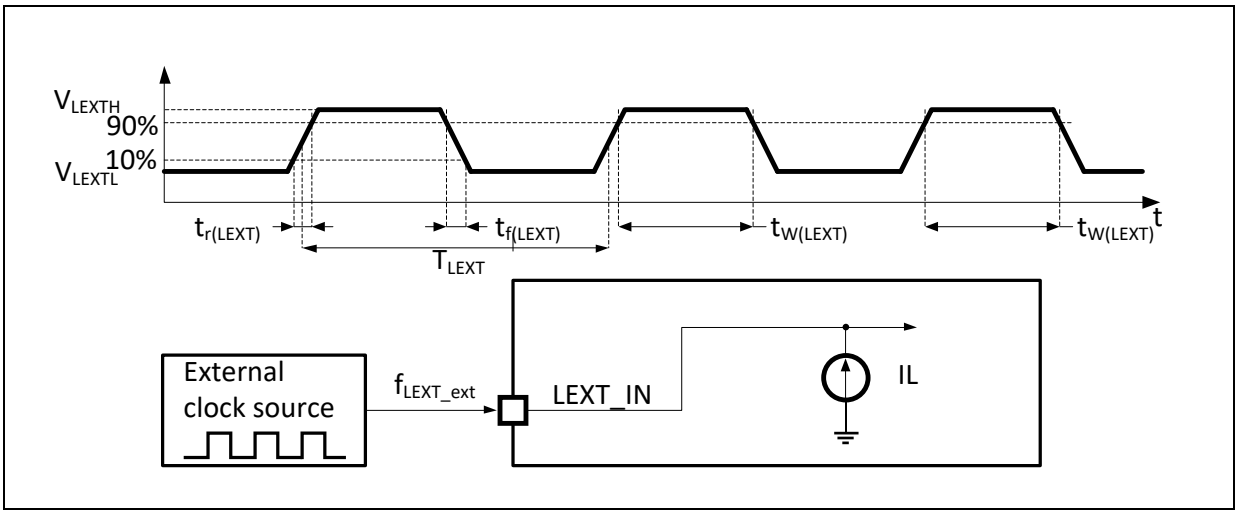
The characteristics given in the table below result from tests performed using a low-speed external clock source.

Table 26. LEXT external source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LEXT_ext}	User external clock source frequency (1)	-	-	32.768	1000	kHz
V_{LEXTH}	LEXT_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LEXTL}	LEXT_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LEXT)}$ $t_{w(LEXT)}$	LEXT_IN high or low time(1)		450	-	-	ns
$t_{r(LEXT)}$ $t_{f(LEXT)}$	LEXT_IN rise or fall time(1)		-	-	50	
$C_{in(LEXT)}$	LEXT_IN input capacitance(1)	-	-	5	-	pF
$Duty_{(LEXT)}$	Duty cycle	-	30	-	70	%
I_L	LEXT_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

(1) Guaranteed by design, not tested in production.

Figure 16. LEXT external source AC timing diagram



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5.3.7 Internal clock source characteristics

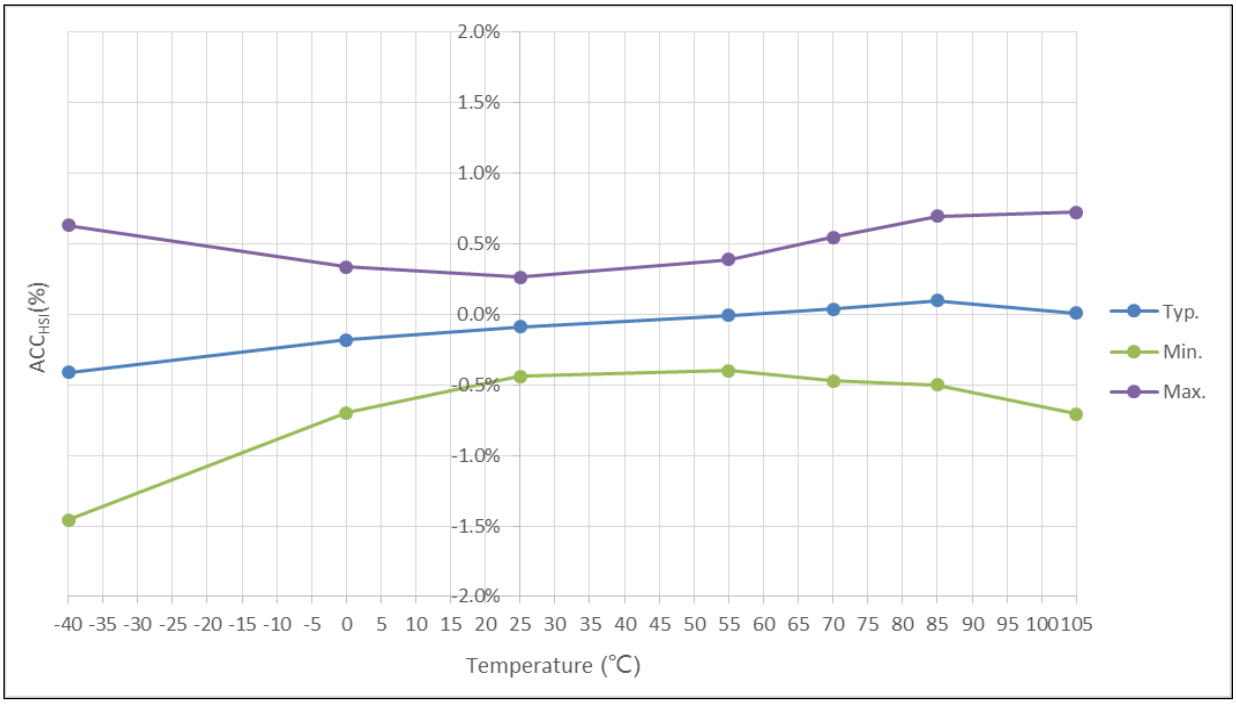
High-speed internal clock (HICK)

Table 27. HICK clock characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HICK}	Frequency	-		-	48	-	MHz
$DuCy_{(HICK)}$	Duty cycle	-		45	-	55	%
ACC_{HICK}	Accuracy of the HICK oscillator	User-trimmed with the CRM_CTRL register (1)		-1	-	1	%
		Factory-calibrated (2)	T_A = -40 ~ 105 °C	-2	-	1.5	%
			T_A = -40 ~ 85 °C	-2	-	1.2	%
			T_A = 0 ~ 70 °C	-1.5	-	1.2	%
			T_A = 25 °C	-1	-	1	%
$t_{SU(HICK)}$(2)	HICK oscillator startup time	-		-	10	12	µs
$I_{DD(HICK)}$(2)	HICK oscillator power consumption	-		-	220	290	µA

(1) Guaranteed by design, not tested in production.
(2) Guaranteed by characterization results, not tested in production.

Figure 17. HICK clock accuracy vs. temperature



Low-speed internal clock (LICK)

Table 28. LICK clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LICK}(1)	Frequency	-	25	35	45	kHz

(1) Guaranteed by characterization results, not tested in production.

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5.3.8 PLL characteristics

Table 29. PLL characteristics

Symbol	Parameter	Min(1)	Typ	Max(1)	Unit
f_{PLL_IN}	PLL input clock (2)	2	8	16	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	120	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

(1) Guaranteed by design, not tested in production.
(2) Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.9 Wakeup time from low-power mode

The wakeup times given in the table below is measured on a wakeup phase with the HICK. The clock source used to wake up the device depends from the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode.
- Deepsleep or Standby mode: the clock source is the HICK.

Table 30. Low-power mode wakeup time

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	3.3	µs
t_{WUSTOP}	Wakeup from Deepsleep mode (regulator in Run mode)	380	µs
	Wakeup from Deepsleep mode (regulator in low-power mode)	450	
$t_{WUSTDBY}$	Wakeup from Standby mode	1250	µs

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

- **EFT:** A Burst of Fast Transient voltage (positive and negative) is applied to VDD and VSS through a coupling/decoupling network, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

Table 31. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{EFT}	Fast transient voltage burst limits to be applied through coupling/decoupling network conforms to IEC 61000-4-4 on V_{DD} and V_{SS} pins to induce a functional disturbance, V_{DD} and V_{SS} input has one 47 µF capacitor and each V_{DD} and V_{SS} pin pair 0.1µF.	V_{DD} = 3.3 V, LQFP48, T_A = +25 °C, f_{HCLK} = 120 MHz, conforms to IEC 61000-4-4	3/A (3.5 kV)
		V_{DD} = 3.3 V, LQFP48, T_A = +25 °C, f_{HCLK} = 72 MHz, conforms to IEC 61000-4-4	

EMC characterization and optimization are performed at component level with a typical application environment. It should be noted that good EMC performance is highly dependent on the user application and the software in particular. Therefore it is recommended that the user applies EMC

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software optimization and prequalification tests in relation with the EMC level requested for his application.

5.3.11 GPIO port characteristics

General input / output characteristics

All GPIOs are CMOS and TTL compliant.

Table 32. GPIO static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	GPIO input low level voltage	-	-0.3	-	0.28 x V_{DD} + 0.1	V
V_{IH}	TC GPIO input high level voltage	-	0.31 x V_{DD} + 0.8	-	V_{DD} + 0.3	V
	FTa GPIO input high level voltage	Analog mode				
	FT GPIO input high level voltage	-		-	5.5	
	FTa GPIO input high level voltage	Input floating, input pull-up, or input pull-down mode				
V_{hys}	Schmitt trigger voltage hysteresis(1)	-	200	-	-	mV
			5% V_{DD}	-	-	-
I_{lkg}	Input leakage current (2)	$V_{SS} \le V_{IN} \le V_{DD}$ TC GPIO	-	-	±1	µA
		$V_{SS} \le V_{IN} \le 5.5$ V FT and FTa GPIO	-	-	±1	
R_{PU}	Weak pull-up equivalent resistor (3)	$V_{IN} = V_{SS}$	65	80	130	kΩ
R_{PD}	Weak pull-down equivalent resistor (3)(4)	$V_{IN} = V_{DD}$	65	70	130	kΩ
C_{IO}	GPIO pin capacitance	-	-	9	-	pF

(1) Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results, not tested in production.
(2) Leakage could be higher than the max if negative current is injected on adjacent pins.
(3) When the input is higher than V_{DD} + 0.3 V, the internal pull-up and pull-down resistors must be disabled for FT and FTa pins.
(4) The pull-down resistor of BOOT0 exists permanently.

All GPIOs are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters.

Output driving current

In the user application, the number of GPIO pins which can drive current must be controlled to respect the absolute maximum rating defined in Section *5.2.1.*

- The sum of the currents sourced by all GPIOs on V_{DD} plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 7*).
- The sum of the currents sunk by all GPIOs on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS}, cannot not exceed the absolute maximum rating I_{VSS} (see *Table 7*).

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Output voltage levels

All GPIOs are CMOS and TTL compliant.

Table 33. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Normal sourcing/sinking strength					
V_{OL}(1)	Output low level voltage	CMOS standard, I_{IO} = 4 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}(1)	Output low level voltage	TTL standard, I_{IO} = 2 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 9 mA	-	1.3	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 2 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.4 V ≤ V_{DD} < 2.7 V	V_{DD}-0.4	-	
Large sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 6 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}(1)	Output low level voltage	TTL standard, I_{IO} = 5 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 18 mA	-	1.3	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 4 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.4 V ≤ V_{DD} < 2.7 V	V_{DD}-0.4	-	
Maximum sourcing/sinking strength					
V_{OL}(1)	Output low level voltage	CMOS standard, I_{IO} = 15 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}(1)	Output low level voltage	TTL standard, I_{IO} = 12 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 12 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.4 V ≤ V_{DD} < 2.7 V	V_{DD}-0.4	-	

(1) Guaranteed by characterization results, not tested in production.

Input AC characteristics

The definition and values of input AC characteristics are given as follows.

Table 34. Input AC characteristics

Symbol	Parameter	Min	Max	Unit
$t_{EXINTpw}$	Pulse width of external signals detected by EXINT controller	10	-	ns

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5.3.12 NRST pin characteristics

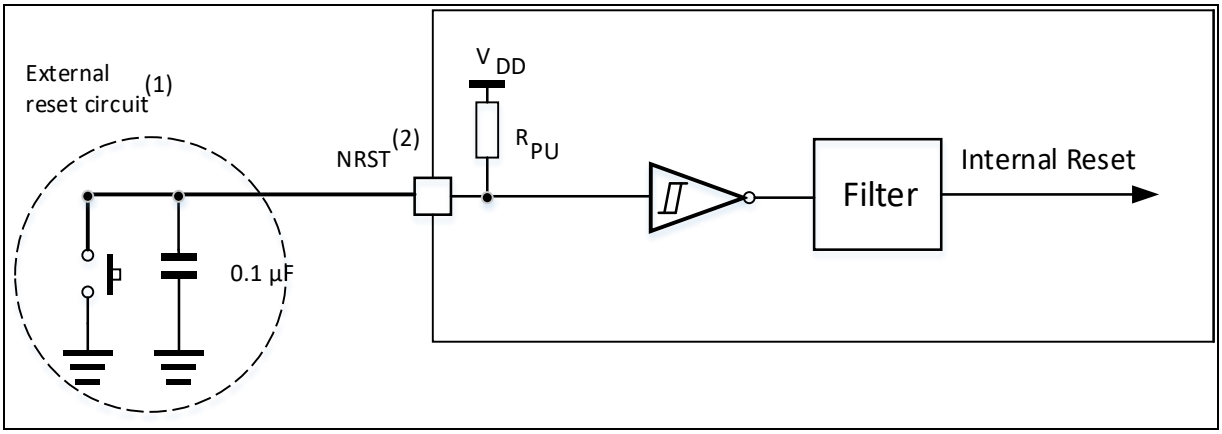
The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see the table below).

Table 35. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	-0.3	-	0.72	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	2	-	V_{DD} + 0.3	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	400	-	mV
R_{PU}	Weak pull-up equivalent resistor	V_{IN} = V_{SS}	30	40	50	kΩ
$t_{ILV(NRST)}$(1)	NRST input low level invalid time	-	-	-	40	μs
$t_{ILNV(NRST)}$(1)	NRST input low level valid time	-	80	-	-	μs

(1) Guaranteed by design, not tested in production.

Figure 18. Recommended NRST pin protection



(1) The reset network protects the device against parasitic resets.
(2) Users must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 35*. Otherwise, the reset will not be taken into account by the device.

5.3.13 TMR timer characteristics

The parameters given in the table below are guaranteed by design.

Table 36. TMR characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TMR)}$	Timer resolution time	-	1	-	$t_{TMRxCLK}$
		$f_{TMRxCLK}$ = 120 MHz	8.3	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TMRxCLK}$/2	MHz

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5.3.14 SPI characteristics

Table 37. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $(1/t_{c(SCK)})^{(1)}$	SPI clock frequency$^{(2)(3)}$	Master mode	-	36	MHz
		Slave receive mode	-	36	
		Slave transmit mode	-	32	
$t_{su(CS)}^{(1)}$	CS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(CS)}^{(1)}$	CS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_{w(SCKH)}^{(1)}$ $t_{w(SCKL)}^{(1)}$	SCK high and low time	Master mode, prescaler factor = 4	$2t_{PCLK}$ - 3	$2t_{PCLK}$ + 3	ns
$t_{su(MI)}^{(1)}$	Data input setup time	Master mode	6	-	ns
$t_{su(SI)}^{(1)}$		Slave mode	5	-	
$t_{h(MI)}^{(1)}$	Data input hold time	Master mode	4	-	ns
$t_{h(SI)}^{(1)}$		Slave mode	5	-	
$t_{a(SO)}^{(1)(4)}$	Data output access time	Slave mode	t_{PCLK} - 2	$2t_{PCLK}$ + 2	ns
$t_{dis(SO)}^{(1)(5)}$	Data output disable time	Slave mode	t_{PCLK} - 2	$2t_{PCLK}$ + 2	ns
$t_{v(SO)}^{(1)}$	Data output valid time	Slave mode (after enable edge)	-	25	ns
$t_{v(MO)}^{(1)}$	Data output valid time	Master mode(after enable edge)	-	10	ns
$t_{h(SO)}^{(1)}$	Data output hold time	Slave mode (after enable edge)	9	-	ns
$t_{h(MO)}^{(1)}$		Master mode(after enable edge)	2	-	

(1) Guaranteed by design, not tested in production.
(2) The maximum SPI clock frequency in slave mode should not exceed $f_{PCLK}/2$.
(3) The maximum SPI clock frequency is highly related with devices and the PCB layout. For more details about the complete solution, please contact your local Artery sales representative.
(4) Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
(5) Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

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Figure 19. SPI timing diagram – slave mode and CPHA = 0

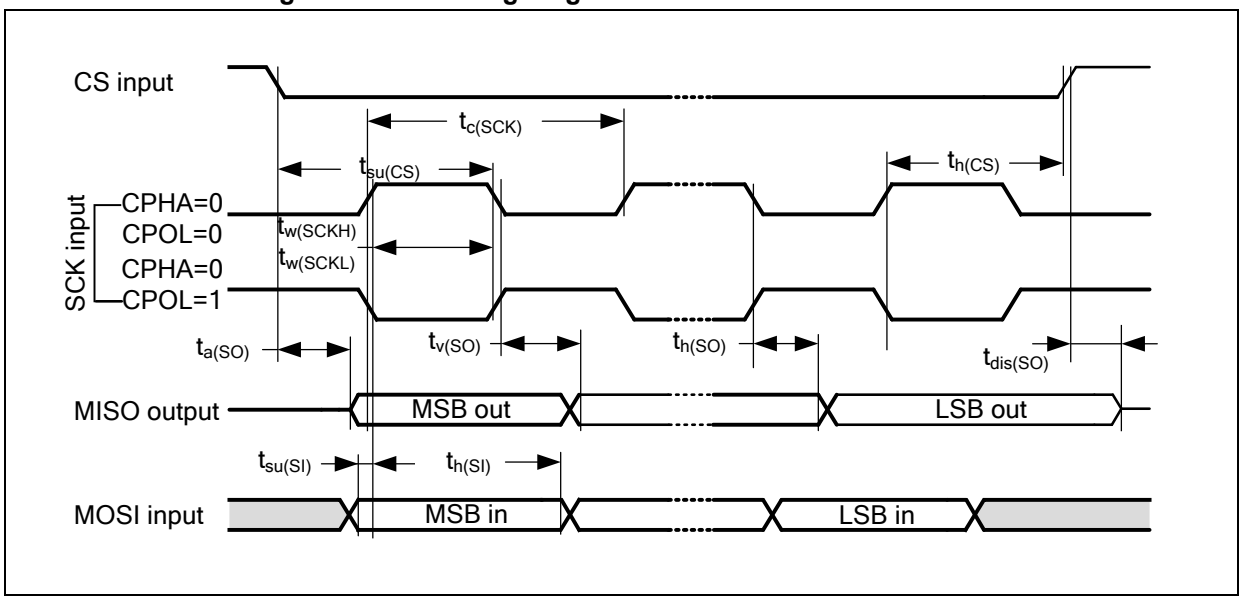


Figure 20. SPI timing diagram – slave mode and CPHA = 1

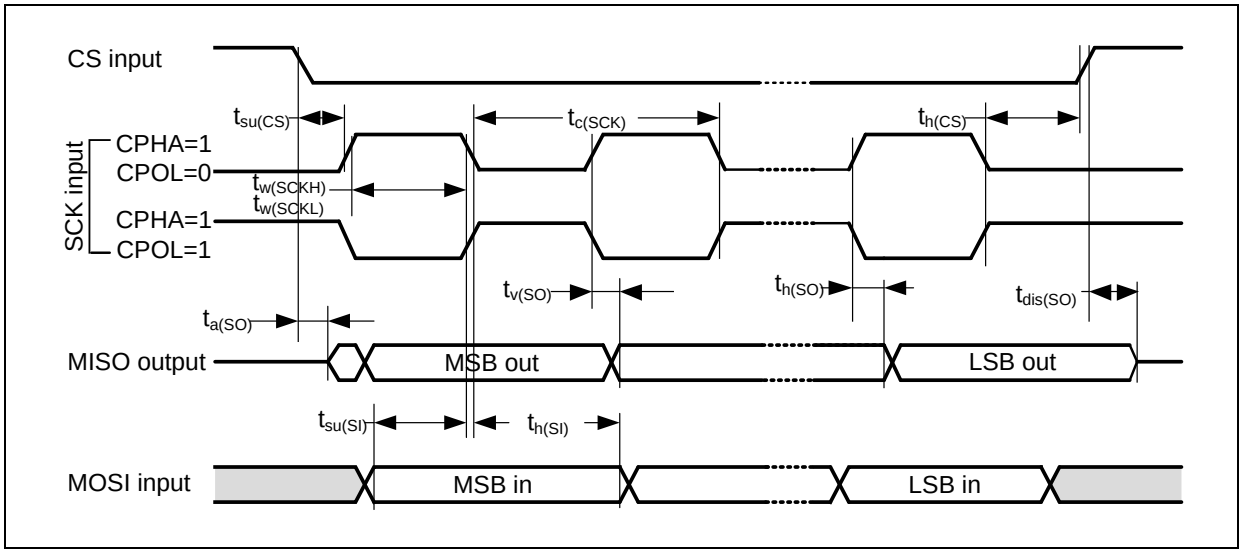
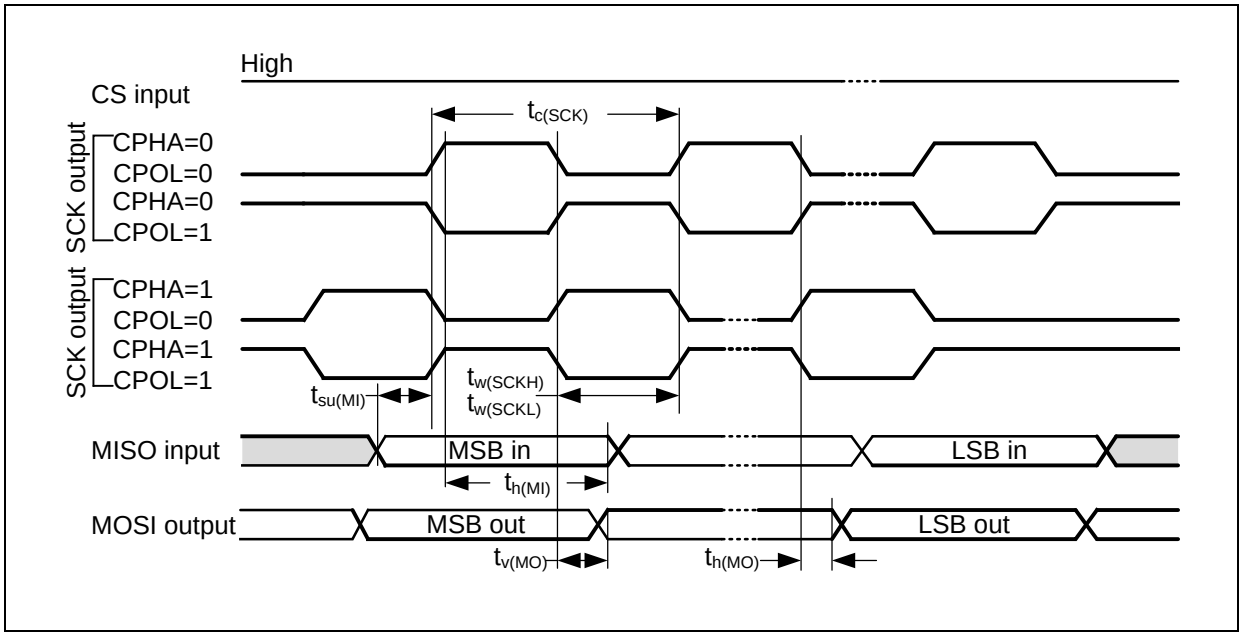


Figure 21. SPI timing diagram – master mode



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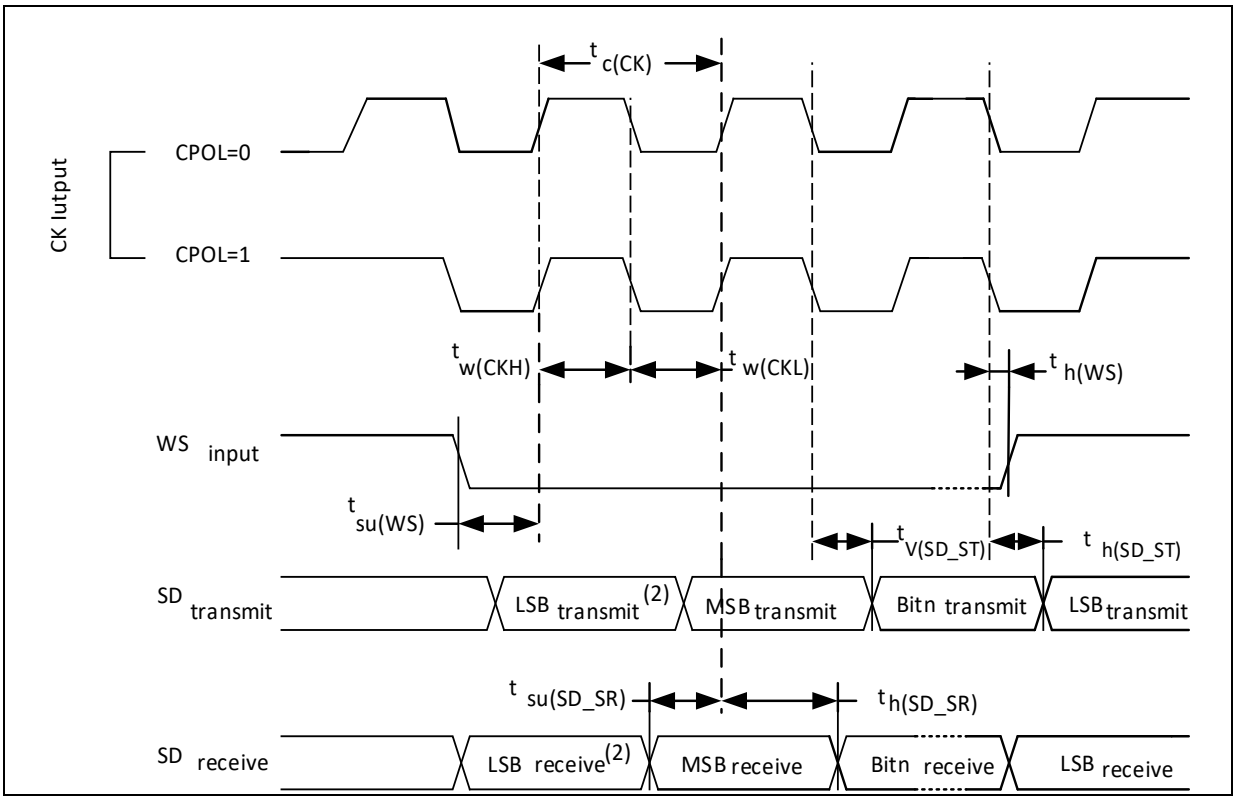
5.3.15 I²S characteristics

Table 38. I²S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{r(CK)}$ $t_{f(CK)}$	I²S clock rise and fall time	Capacitive load: C = 15 pF	-	12	ns
$t_{v(WS)}$(1)	WS valid time	Master mode	0	4	
$t_{h(WS)}$(1)	WS hold time	Master mode	0	4	
$t_{su(WS)}$(1)	WS setup time	Slave mode	9	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	0	-	
$t_{su(SD_MR)}$(1)	Data input setup time	Master receiver	6	-	
$t_{su(SD_SR)}$(1)		Slave receiver	2	-	
$t_{h(SD_MR)}$(1)(2)	Data input hold time	Master receiver	0.5	-	
$t_{h(SD_SR)}$(1)(2)		Slave receiver	0.5	-	
$t_{v(SD_ST)}$(1)(2)	Data output valid time	Slave transmitter (after enable edge)	-	20	
$t_{h(SD_ST)}$(1)	Data output hold time	Slave transmitter (after enable edge)	9	-	
$t_{v(SD_MT)}$(1)(2)	Data output valid time	Master transmitter (after enable edge)	-	15	
$t_{h(SD_MT)}$(1)	Data output hold time	Master transmitter (after enable edge)	0	-	

(1) Guaranteed by design, not tested in production.
(2) Depends on f_{PCLK}. For example, if f_{PCLK} = 8 MHz, then t_{PCLK} = 1/f_{PCLK} = 125 ns.

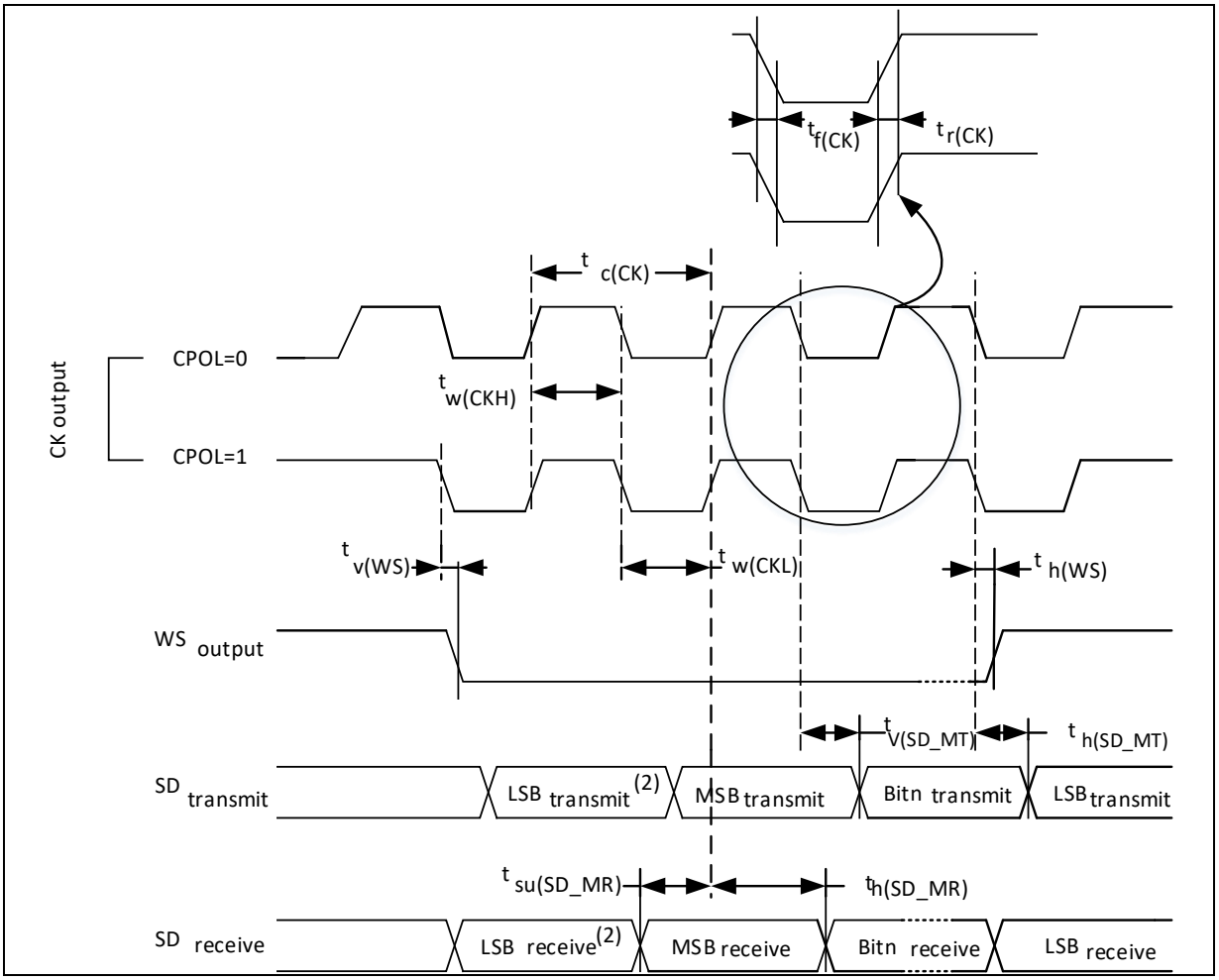
Figure 22. I²S slave timing diagram (Philips protocol)



(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

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Figure 23. I²S master timing diagram (Philips protocol)



(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

5.3.16 I²C interface characteristics

GPIO pins SDA and SCL have limitation as follows: they are not “true” open-drain. When configured as open-drain, the PMOS connected between the GPIO pin and V_{DD} is disabled, but is still present.

I²C bus interface can support standard mode (max. 100 kHz) and fast mode (max. 400 kHz). The I²C bus frequency can be increased up to 1 MHz. For more complete information, please contact your local Artery sales office for technical support.

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5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in the table below are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 11*.

Note: It is recommended to perform a calibration after each power-up.

Table 39. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
I_{DDA}	Current on the V_{DDA} input pin	-	-	480(1)	560	μA
f_{ADC}	ADC clock frequency	-	0.6	-	28	MHz
f_S(2)	Sampling rate	-	0.05	-	2	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 28 MHz	-	-	1.65	MHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{REF-} connected to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	-	See *Table 40* and *Table 41*			Ω
C_{ADC}(2)	Internal sample and hold capacitor	-	-	8.5	13	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 28 MHz	6.61			μs
		-	185			$1/f_{ADC}$
t_{latr}(2)	Trigger conversion latency	f_{ADC} = 28 MHz	-	-	71.4	ns
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 28 MHz	0.053	-	8.55	μs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-on time	-	42			$1/f_{ADC}$
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 28 MHz	0.5	-	9	μs
		-	14~252 (t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$

(1) Guaranteed by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) V_{REF+} can be internally connected to V_{DDA}, and V_{REF-} can be internally connected to V_{SSA}.
(4) For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 39*.

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Table 40 and *Table 41* are used to determine the maximum external impedance allowed for an error below 1 LSB.

Table 40. R_{AIN} max for f_{ADC} = 14 MHz (1)

T_S (Cycle)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	0.35
7.5	0.54	3.9
13.5	0.96	7.4
28.5	2.04	16.3
41.5	2.96	24.0
55.5	3.96	32.3
71.5	5.11	41.8
239.5	17.11	50.0

(1) Guaranteed by design.

Table 41. R_{AIN} max for f_{ADC} = 28 MHz (1)

T_S (Cycle)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.05	0.1
7.5	0.27	1.6
13.5	0.48	3.4
28.5	1.02	7.9
41.5	1.48	11.7
55.5	1.98	15.9
71.5	2.55	20.6
239.5	8.55	50.0

(1) Guaranteed by design.

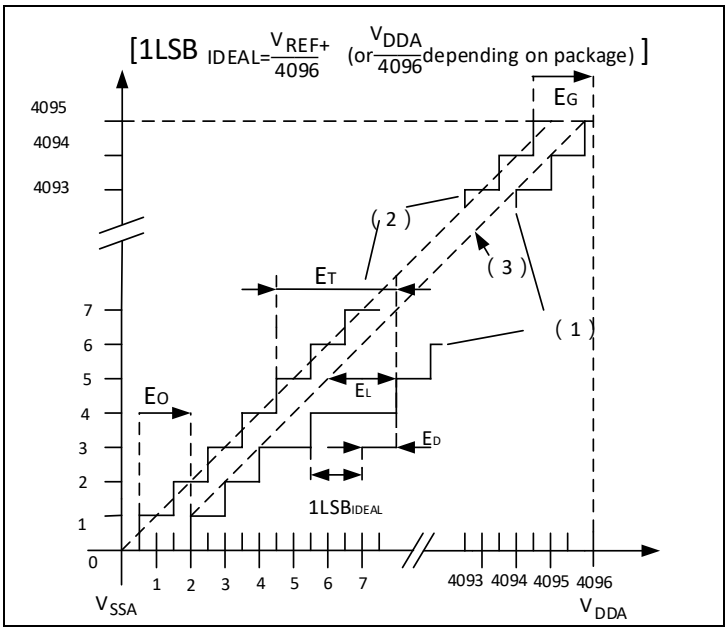
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Table 42. ADC accuracy (1)(2)

Symbol	Parameter	Test Conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3.0~3.6 V, T_A = 25 °C	+2	+3.5	LSB
EO	Offset error		+1	+2.5	
EG	Gain error		+1.5	+3	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4~3.6 V, T_A = -40 ~ 105 °C	±2	+4	LSB
EO	Offset error		+1	+3	
EG	Gain error		+1.5	+3.5	
ED	Differential linearity error		±0.6	+1.5/-1	
EL	Integral linearity error		±1	±2.5	

(1) ADC DC accuracy values are measured after internal calibration.
(2) Guaranteed by characterization results, not tested in production.

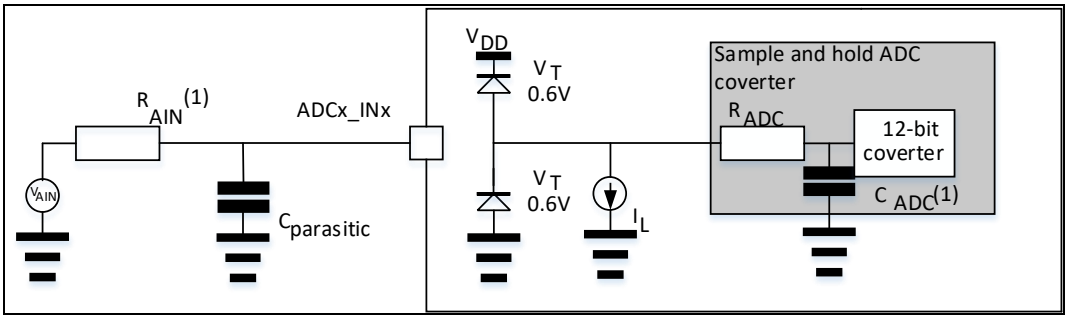
Figure 24. ADC accuracy characteristics



(1) Example of an actual transfer curve.
(2) Ideal transfer curve.
(3) End point correlation line.
(4) ET = Maximum deviation between the actual and the ideal transfer curves.
EO = Deviation between the first actual transition and the first ideal one.
EG = Deviation between the last ideal transition and the last actual one.
ED = Maximum deviation between actual steps and the ideal one.
EL = Maximum deviation between any actual transition and the end point correlation line.

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Figure 25. Typical connection diagram using the ADC



(1) Refer to *Table 39* for the values of R_{AIN} and C_{ADC}.
(2) $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 8*. The 100 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

5.3.18 Interface reference voltage (V_{INTRV}) characteristics

Table 43. Internal reference voltage characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INTRV}(1)	Internal reference voltage	-	1.16	1.20	1.24	V
T_{Coeff}(1)	Temperature coefficient	-	-	50	100	ppm/°C
T_{S_VINTRV}(2)	ADC sampling time when reading the internal reference voltage	-	5.1	-	-	µs

(1) Guaranteed by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.

5.3.19 Temperature sensor (V_{TS}) characteristics

Table 44. Temperature sensor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	T_A = -20 ~ 85 °C	-	±1	±1.5	ºC
		T_A = -40 ~ 105 °C	-	-	±2	
Avg_Slope(1)(2)	Average slope		-4.17	-4.30	-4.44	mV/ºC
V_{25}(1)(2)	Voltage at T=25 ºC		1.22	1.28	1.34	V
t_{START}(3)	Setup time		-	-	100	µs
T_{S_temp}(3)	ADC sampling time when reading the temperature		5.1	-	-	µs

(1) Guaranteed by characterization results, not tested in production.
(2) The temperature sensor output voltage changes linearly with temperature. The offset of this line varies from chip to chip due to process variation (up to 50 °C from one chip to another). The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.
(3) Guaranteed by design, not tested in production.

Obtain the temperature using the following formula:

Temperature (°C) = {(V_{25} – V_{TS}) / Avg_Slope} + 25

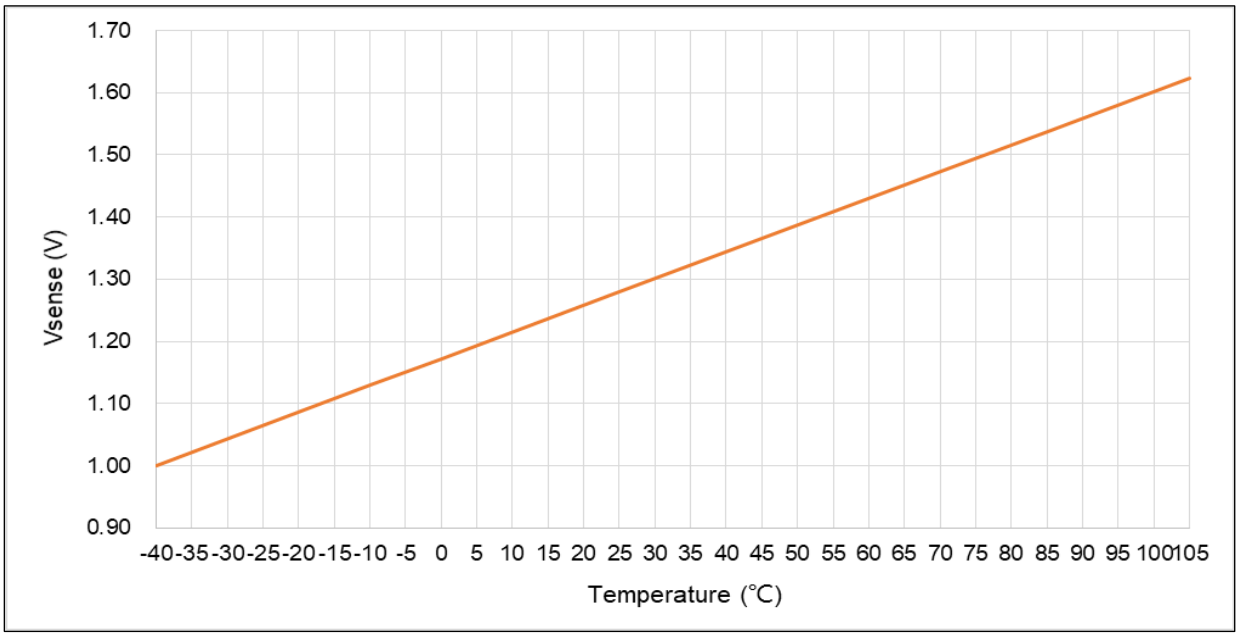
where,

V_{25} = V_{TS} value for 25 °C

Avg_Slope = average slope for curve between temperature vs.V_{TS} (given in mV/°C)

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Figure 26. V_{TS} vs. temperature (ideal curve)



5.3.20 Comparator (CMP) characteristics

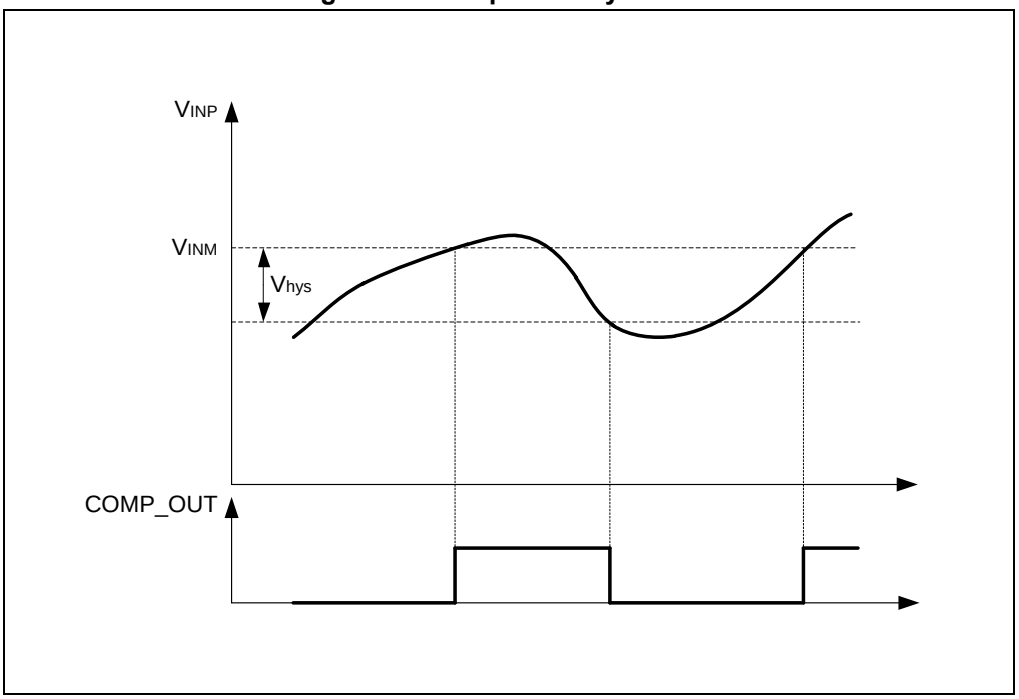
Table 45. Comparator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DDA}	Power supply voltage	-	2.4	-	3.6	V
V_{IN}	Input voltage range	-	0	-	V_{DDA}	V
t_{START}	Startup time	High speed mode	-	1.0	3.5	µs
		Medium speed mode	-	2.8	5	
		Low power mode	-	8	13	
		Ultra low power mode	-	12	18	
t_D	Propagation delay for 200 mV step with 100 mV overdrive	High speed mode	-	40	100	ns
		Medium speed mode	-	240	320	
		Low power mode	-	500	820	
		Ultra low power mode	-	800	1800	
V_{offset}	Offset voltage	-	-	±4	±15	mV
V_{hys}	Hysteresis	No hysteresis	-	0	1	mV
		Low hysteresis	5	8	17	
		Medium hysteresis	10	18	37	
		High hysteresis	18	38	70	
I_{DDA}	Current on V_{DDA} input pin	High speed mode	-	40	61	µA
		Medium speed mode	-	9.7	13.9	
		Low power mode	-	3.2	4.7	
		Ultra low power mode	-	1.9	2.8	

(1) Guaranteed by characterization results, not tested in production.

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Figure 27. Comparator hysteresis

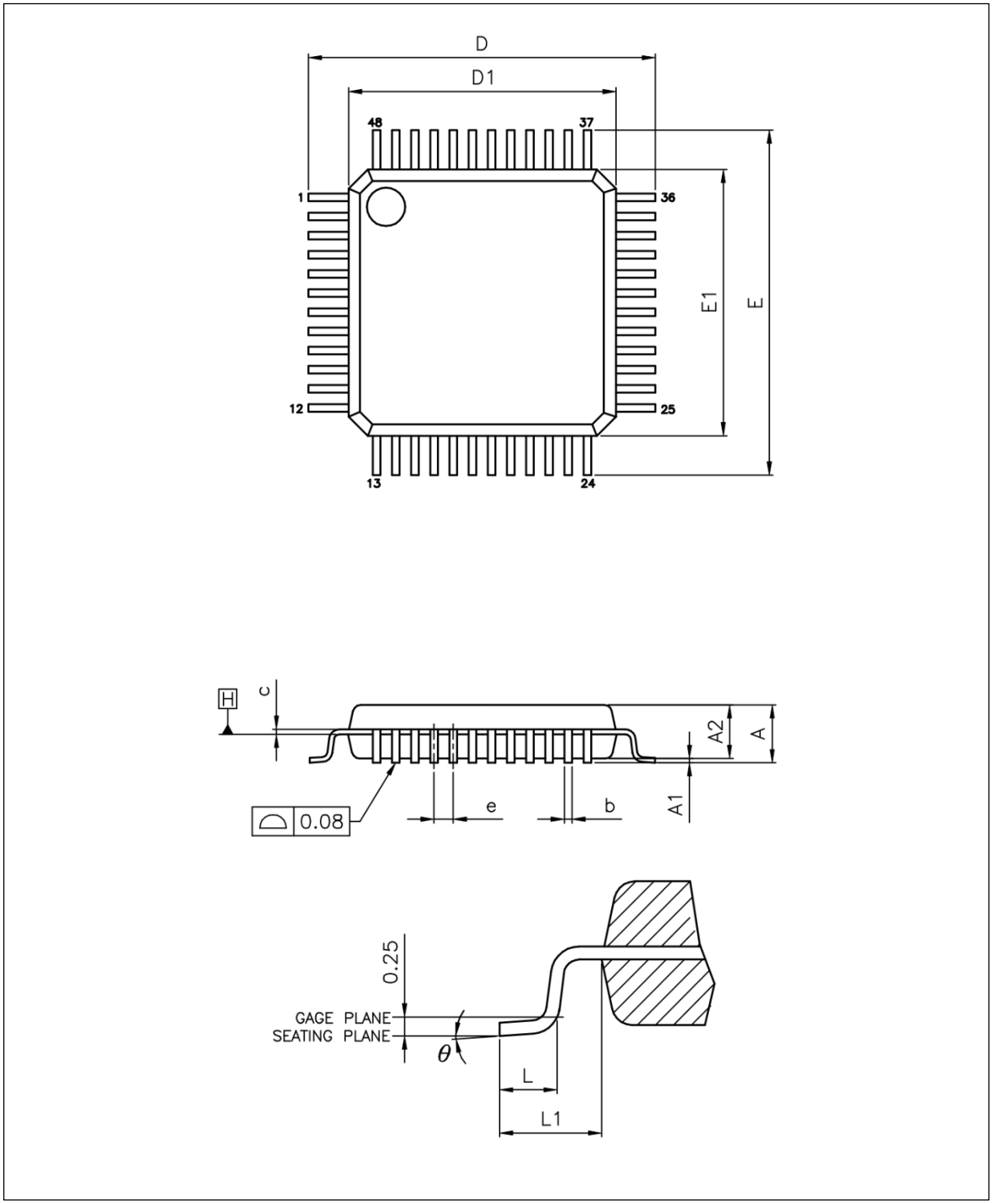


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6 Package information

6.1 LQFP48 – 7 x 7 mm

Figure 28. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package outline



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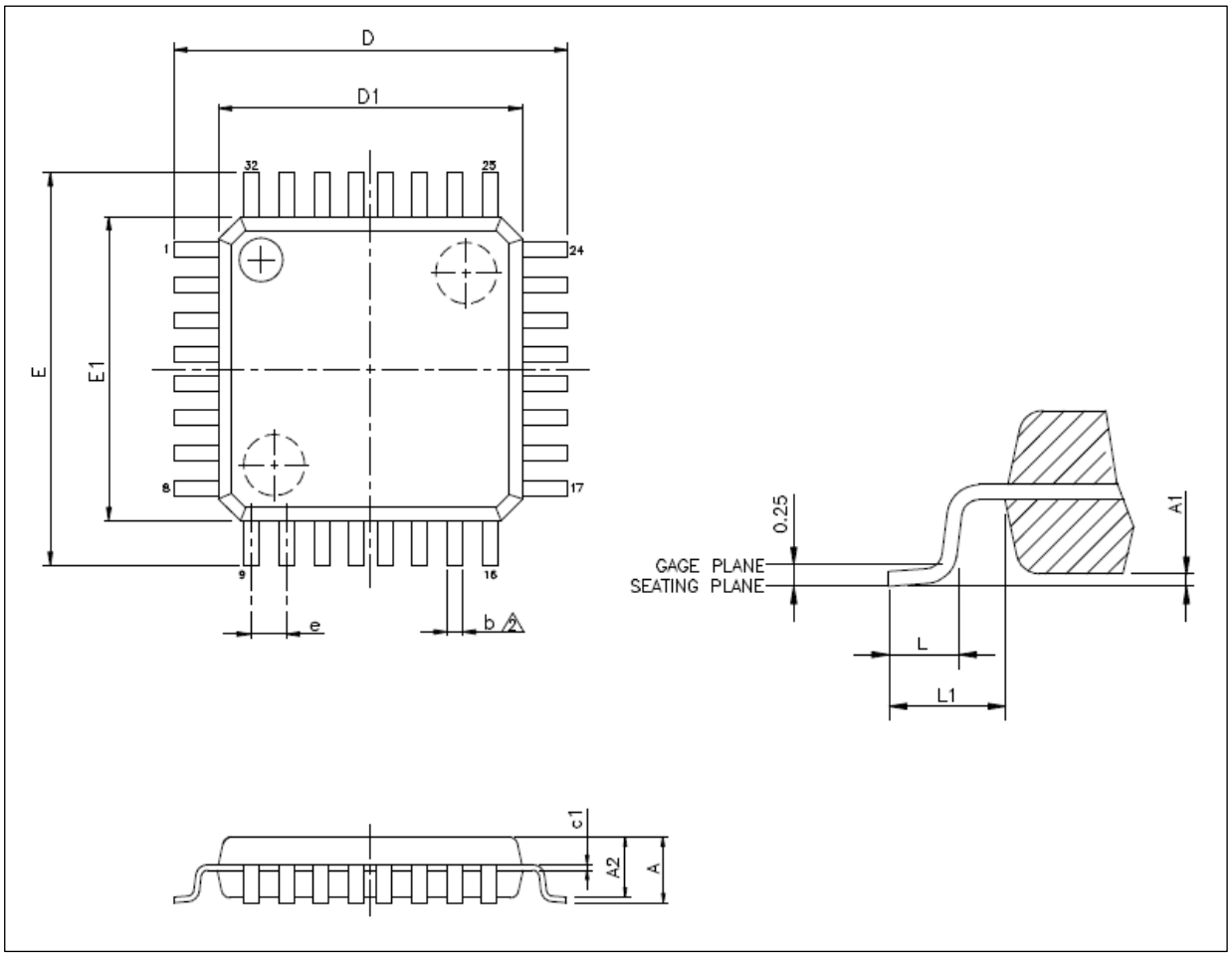
Table 46. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50 BSC.		
Θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	1.00 REF.		

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6.2 LQFP32 – 7 x 7 mm

Figure 29. LQFP32 – 7 x 7 mm 32 pin low-profile quad flat package outline



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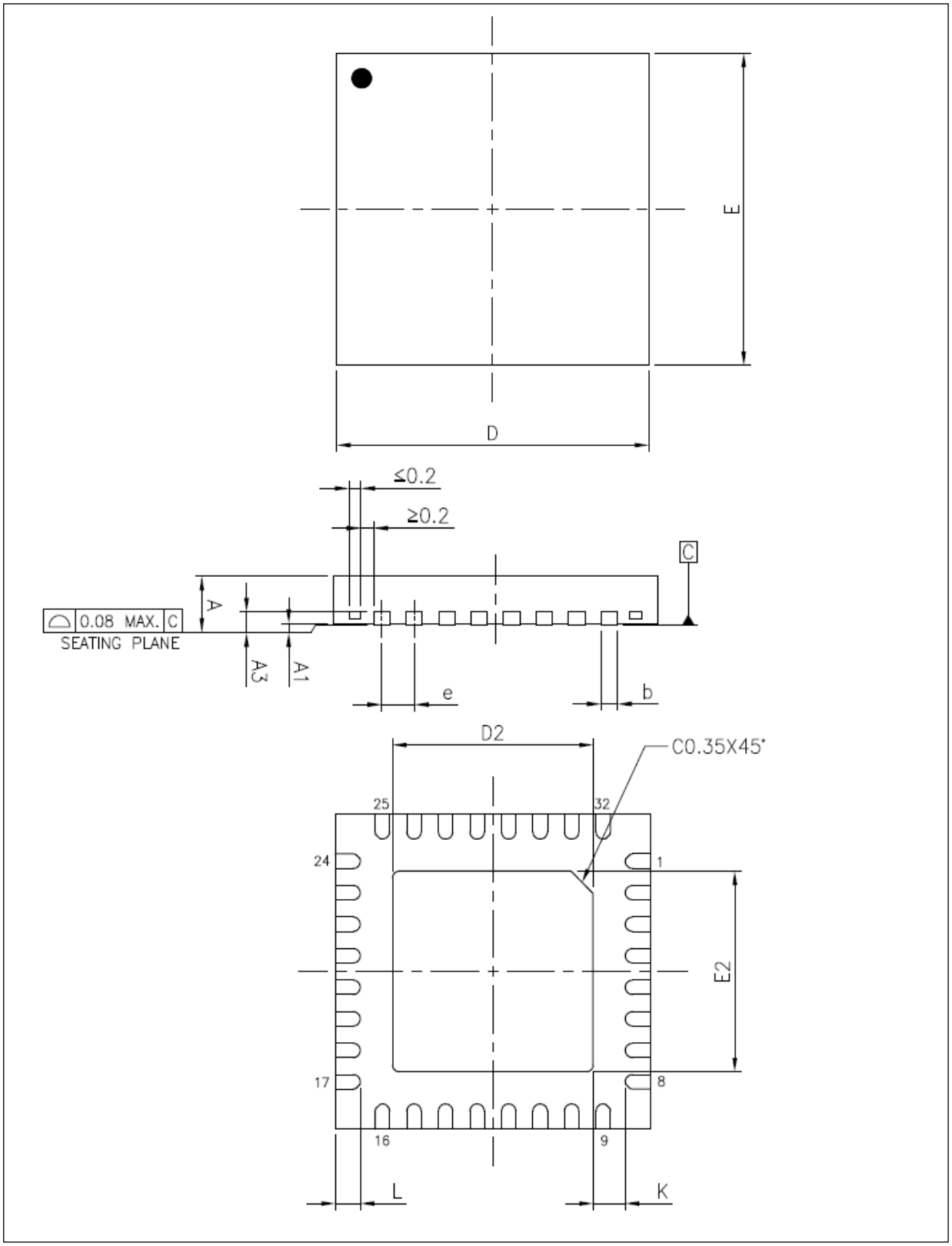
Table 47. LQFP32 – 7 x 7 mm 32 pin low-profile quad flat package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	-	1.45
b	0.30	-	0.45
c	0.09	-	0.16
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.80 BSC.		
L	0.45	-	0.75
L1	1.00 REF.		

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6.3 QFN32 – 5 x 5 mm

Figure 30. QFN32 – 5 x 5 mm 32 pin quad flat no-leads package outline



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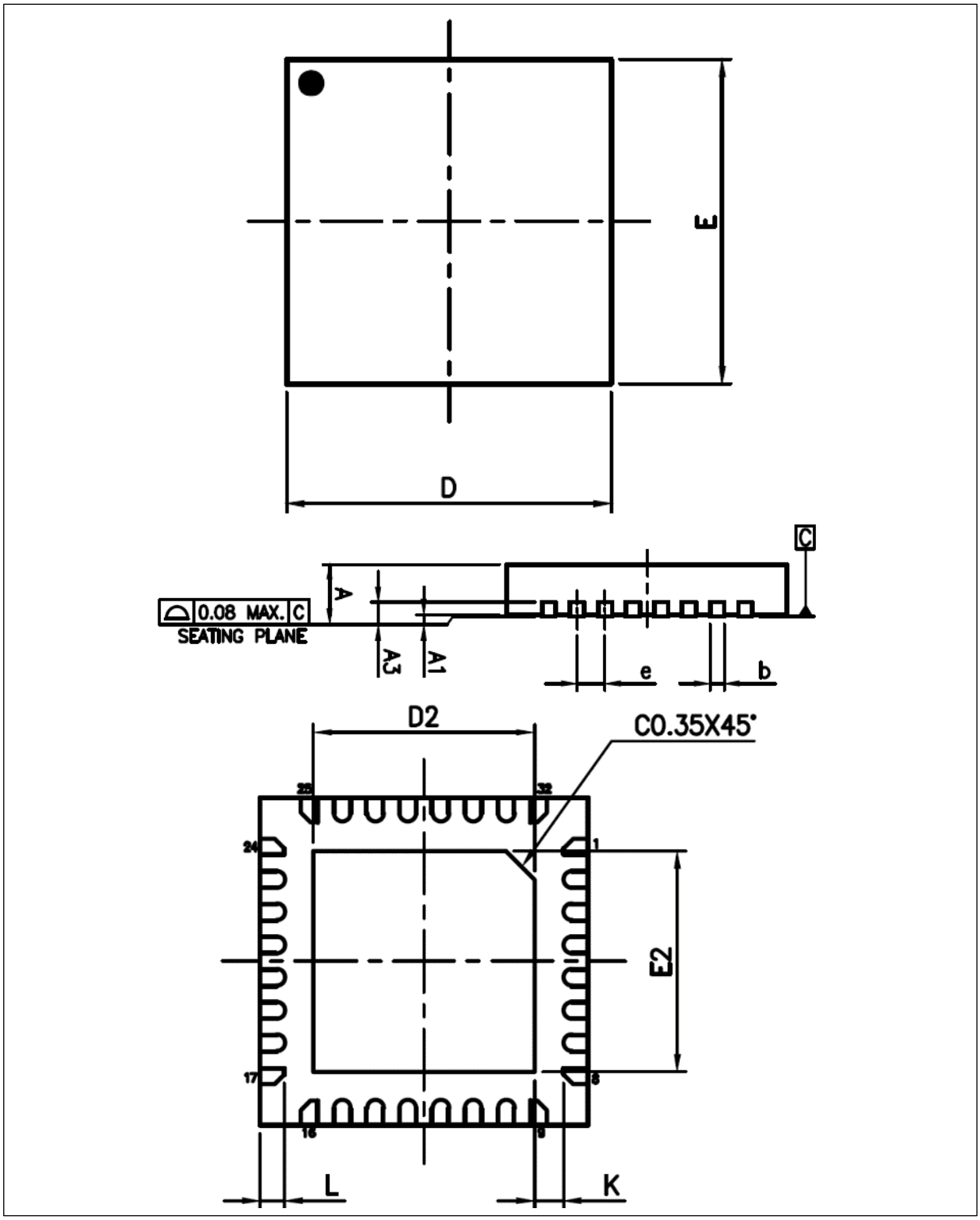
Table 48. QFN32 – 5 x 5 mm 32 pin quad flat no-leads package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.18	0.25	0.30
D	4.90	5.00	5.10
D2	3.20	3.25	3.30
E	4.90	5.00	5.10
E2	3.20	3.25	3.30
e		0.50 BSC.	
K	0.20	-	-
L	0.35	0.40	0.45

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6.4 QFN32 – 4 x 4 mm

Figure 31. QFN32 – 4 x 4 mm 32 pin quad flat no-leads package outline



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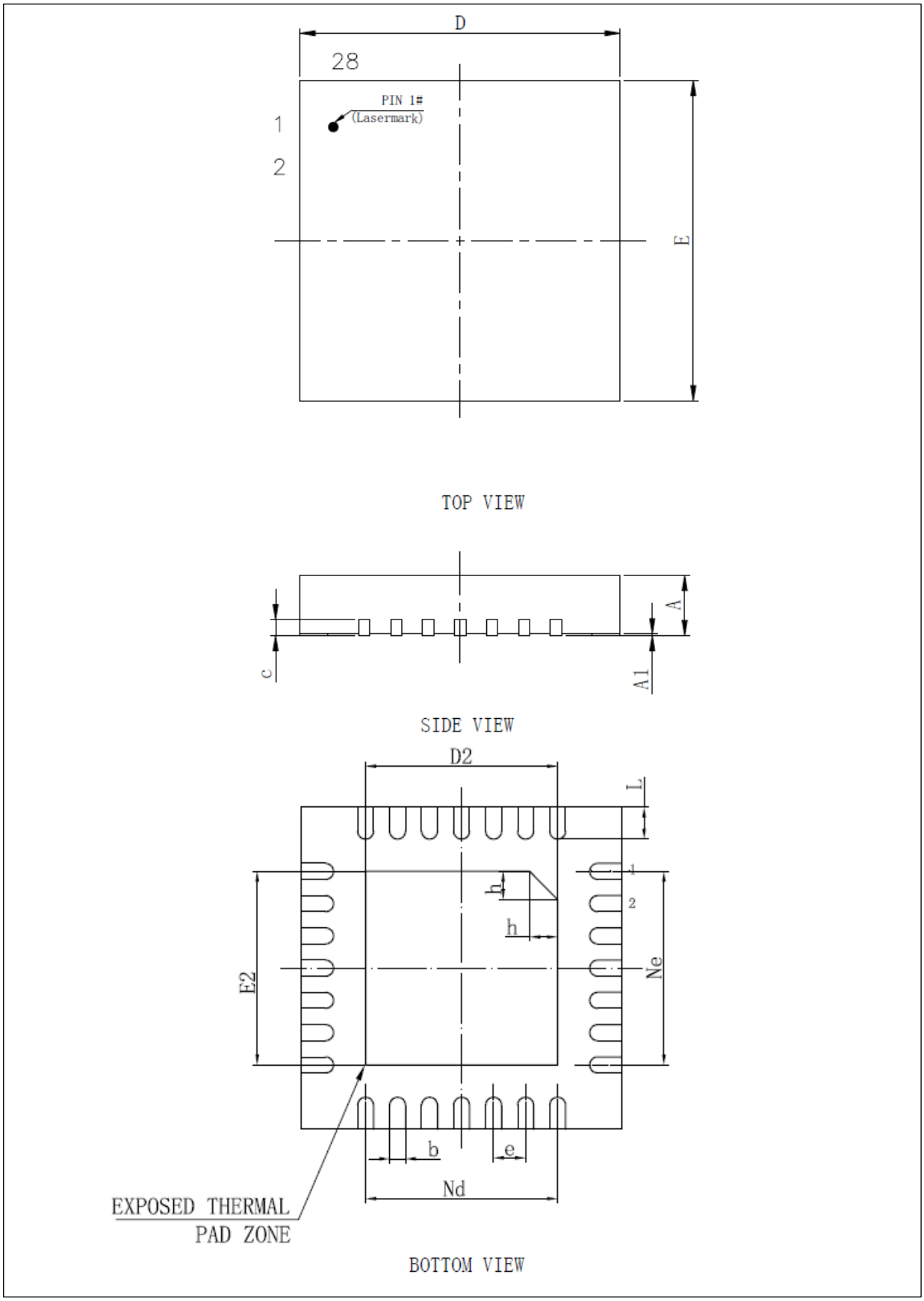
Table 49. QFN32 – 4 x 4 mm 32 pin quad flat no-leads package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
D2	2.65	2.70	2.75
E	3.90	4.00	4.10
E2	2.65	2.70	2.75
e		0.40 BSC.	
K	0.20	-	-
L	0.25	0.30	0.35

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6.5 QFN28 – 4 x 4 mm

Figure 32. QFN28 – 4 x 4 mm 28 pin quad flat no-leads package outline



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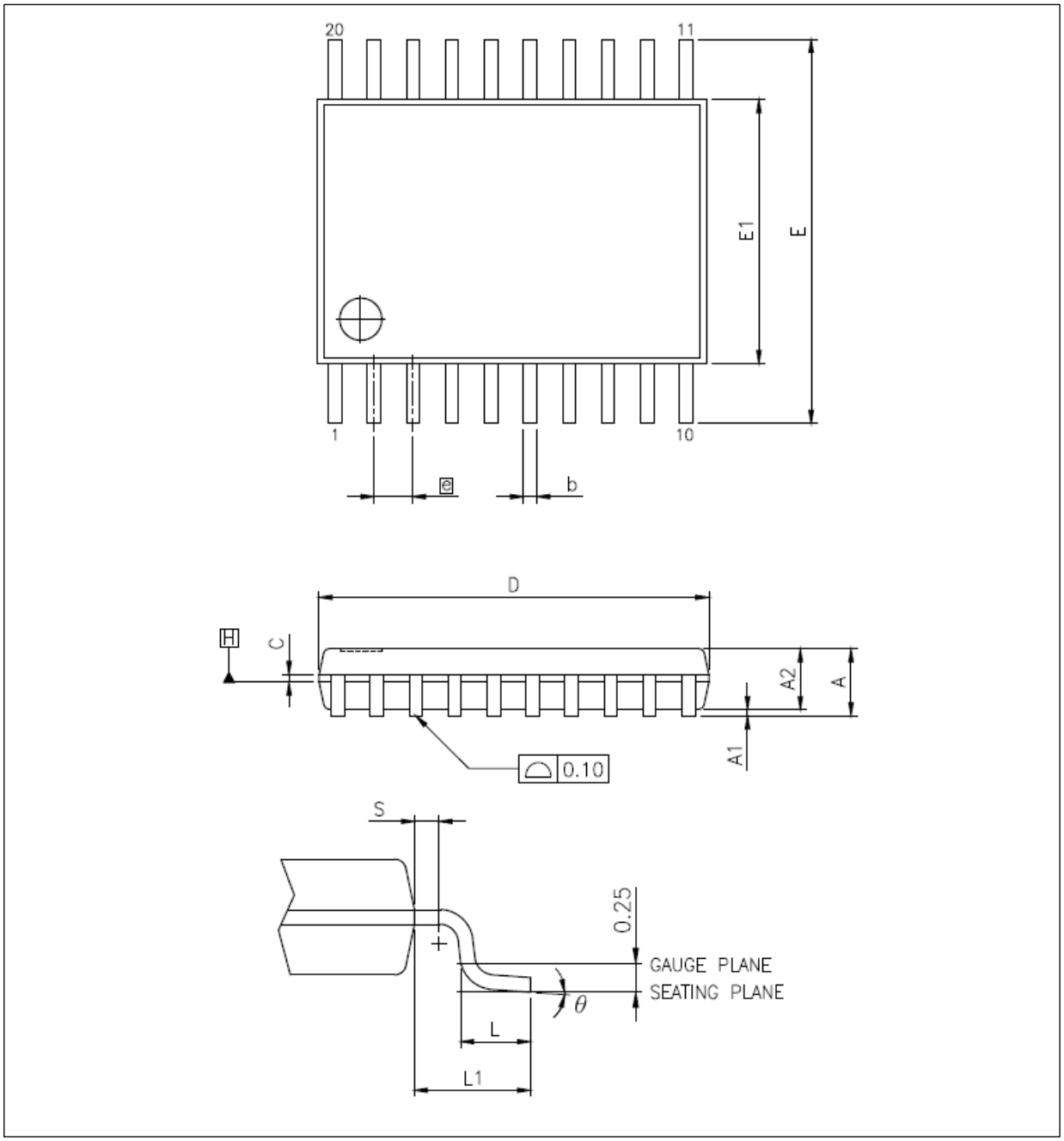
Table 50. QFN28 – 4 x 4 mm 28 pin quad flat no-leads package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.30	2.40	2.50
Nd	2.40 BSC.		
E	3.90	4.00	4.10
E2	2.30	2.40	2.50
Ne	2.40 BSC.		
e	0.40 BSC.		
L	0.35	0.40	0.45
h	0.30	0.35	0.40

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6.6 TSSOP20 – 6.5 x 4.4 mm

Figure 33. TSSOP20 – 6.5 x 4.4 mm 20-pin thin shrink small outline package



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Table 51. TSSOP20 – 6.5 x 4.4 mm 20-pin thin shrink small outline package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
C	0.09	-	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC.		
L1	1.00 REF.		
L	0.50	0.60	0.75
S	0.20	-	-
Θ	0°	-	8°

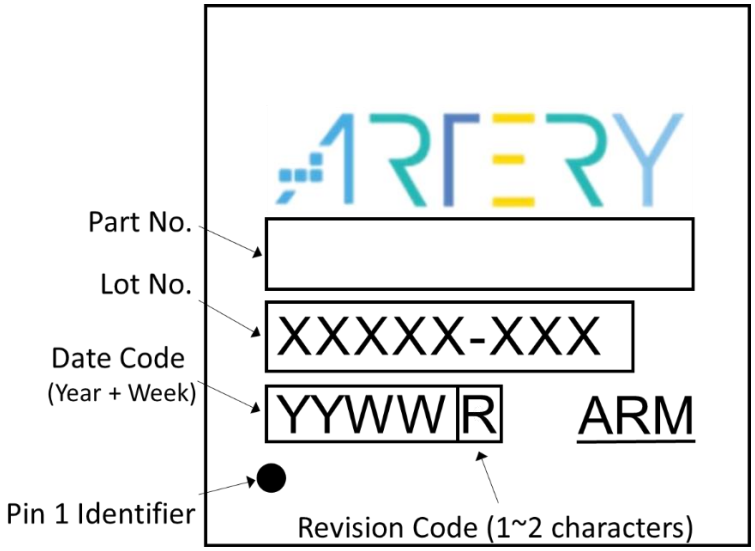
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6.7 Device marking

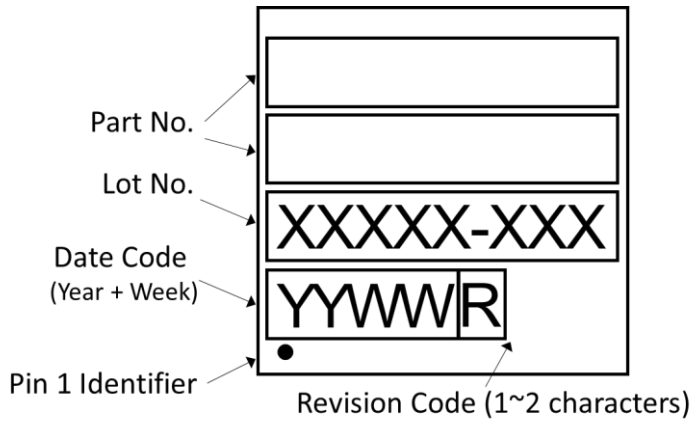
Artery devices may have the following markings, depending on the types of packages.

Figure 34. Marking example

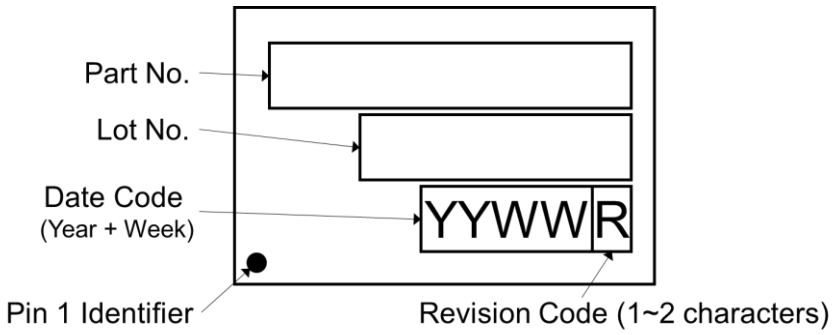
LQFP48, LQFP32, QFN32 (5 x 5 mm)



QFN32 (4 x 4 mm), QFN28



TSSOP20



(1) Not in scale.

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6.8 Thermal characteristics

Thermal characteristics are calculated based on two-layer board that uses FR-4 material in 1.6 mm thickness. They are guaranteed by design, not tested in production.

Table 52. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient – LQFP48 – 7 x 7 mm	87.0	°C/W
	Thermal resistance junction-ambient – LQFP32 – 7 x 7 mm	82.4	
	Thermal resistance junction-ambient – QFN32 – 5 x 5 mm	39.8	
	Thermal resistance junction-ambient – QFN32 – 4 x 4 mm	44.8	
	Thermal resistance junction-ambient – QFN28 – 4 x 4 mm	44.8	
	Thermal resistance junction-ambient – TSSOP20 – 6.5 x 4.4 mm	103.0	

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7 Part numbering

Table 53. AT32F421 series part numbering

Example: AT32 F 4 2 1 K 8 U 7 -4

Product family

AT32 = ARM®-based 32-bit microcontroller

Product type

F = General-purpose

Core

4 = Cortex®-M4

Product series

2 = Value line

Product application

1 = Basic version

Pin count

C = 48 pins

K = 32 pins

G = 28 pins

F = 20 pins

Internal Flash memory size

8 = 64 Kbytes of Flash memory

6 = 32 Kbytes of Flash memory

4 = 16 Kbytes of Flash memory

Package

T = LQFP

U = QFN

P = TSSOP

Temperature range

7 = -40 °C to +105 °C

Package information

-4 = QFN32 - 4 x 4 mm

None = Other packages

For a list of available options (speed, package, etc.) or for more information concerning this device, please contact your local Artery sales office.

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8 Document revision history

Table 54. Document revision history

Date	Version	Revision note
2020.8.17	1.00	Initial release.
2020.9.16	1.01	1. The maximum frequency of APB1 and APB2 is updated to 120 MHz in *Figure 1*, *Table 11* and *Table 22*. 2. Modified conditions and maximum values of SPI clock frequencies in *Table 37*. 3. Added EFT test result 3/A (2 kV) in *Table 31*. 4. Added note (4) in *Table 5*.
2021.7.1	1.02	1. Updated comparator V_{offset} data in *Table 45*. 2. Updated temperature sensor T_L data in *Table 44*. 3. Modified LQFP48 package data.
2022.1.7	2.00	1. Updated document architecture and related descriptions. 2. Modified comparator V_{offset} data in *Table 45*. 3. Modified LQFP48 package data.
2022.6.6	2.01	1. Added note (4) in *Table 21*. 2. Added the minimum and maximum values of D, D1, E and E1 for each package.
2023.10.17	2.02	1. Added note (3) in *Table 32*. 2. Modified *Table 37* and *Table 38*. 3. Modified the fourth paragraph in IMPORTANT NOTICE.

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