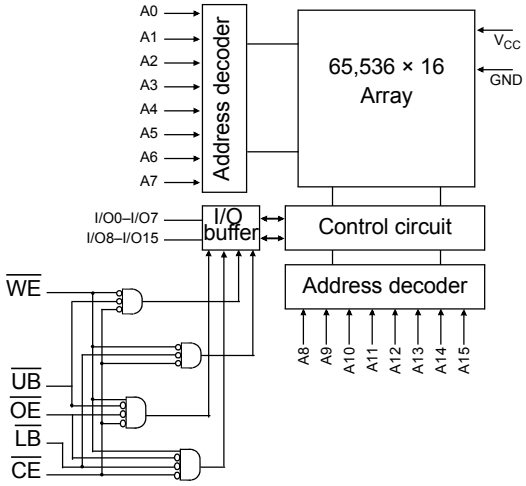
3.3 V 64K X 16 CMOS SRAM

Features

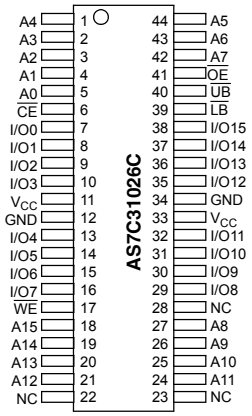
- Industrial (-40° to 85°C) temperature
- Organization: 65,536 words × 16 bits
- Center power and ground pins for low noise
- High speed
  - 12 ns address access time
  - 6 ns output enable access time
- Low power consumption via chip deselect
- Upper and Lower byte pin
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
- JEDEC standard packaging
  - 44-pin 400 mil SOJ
  - 44-pin TSOP 2-400
  - 48-ball 7 × 7 mm BGA
- ESD protection ? 2000 volts

Logic block diagram



Pin arrangement

44-Pin SOJ (400 mil), TSOP 2



48 - BGA Ball-Grid-Array Package

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	NC
B	I/O8	$\overline{UB}$	A3	A4	$\overline{CE}$	I/O0
C	I/O9	I/O10	A5	A6	I/O1	I/O2
D	V_{SS}	I/O11	NC	A7	I/O3	V_{DD}
E	V_{DD}	I/O12	NC	NC	I/O4	V_{SS}
F	I/O14	I/O13	A14	A15	I/O5	I/O6
G	I/O15	NC	A12	A13	$\overline{WE}$	I/O7
H	NC	A8	A9	A10	A11	NC

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Web:www.manduic.com
Tel:150-1290-5940
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Functional description

The AS7C31026C is a 3V high-performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) device organized as 65,536 words × 16 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 12 ns with output enable access times (t_{OE}) of 6 ns are ideal for high-performance applications.

When $\overline{CE}$ is high, the device enters standby mode. A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O0 through I/O15 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and chip enable ($\overline{CE}$) with write enable ($\overline{WE}$) high. The chips drive I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive or write enable is active, output drivers stay in high-impedance mode.

The device provides multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. $\overline{LB}$ controls the lower bits, I/O0 through I/O7, and $\overline{UB}$ controls the higher bits, I/O8 through I/O15.

All chip inputs and outputs are TTL-compatible, and operation is from a single 3.3 V supply. The AS7C31026C is packaged in common industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to GND	V_{t1}	–0.50	+4.60	V
Voltage on any pin relative to GND	V_{t2}	–0.50	V_{CC} +0.50	V
Power dissipation	P_D	–	1.25	W
Storage temperature (plastic)	T_{stg}	–55	+125	°C
Ambient temperature with VCC applied	T_{bias}	–55	+125	°C
DC current into outputs (low)	I_{OUT}	–	50	mA

Note: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O0–I/O7	I/O8–I/O15	Mode
H	X	X	X	X	High Z	High Z	Standby (I_{SB}), I_{SBI})
L	H	L	L	H	D_{OUT}	High Z	Read I/O0–I/O7 (I_{CC})
L	H	L	H	L	High Z	D_{OUT}	Read I/O8–I/O15 (I_{CC})
L	H	L	L	L	D_{OUT}	D_{OUT}	Read I/O0–I/O15 (I_{CC})
L	L	X	L	L	D_{IN}	D_{IN}	Write I/O0–I/O15 (I_{CC})
L	L	X	L	H	D_{IN}	High Z	Write I/O0–I/O7 (I_{CC})
L	L	X	H	L	High Z	D_{IN}	Write I/O8–I/O15 (I_{CC})
L L	H X	H X	X H	X H	High Z	High Z	Output disable (I_{CC})

Key: H = high, L = low, X = don't care.

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Recommended operating conditions

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input voltage	V_{IH}	2.0	–	V_{CC} + 0.5	V
	V_{IL}	–0.5	–	0.8	V
Ambient operating temperature (industrial)	T_A	–40	–	85	°C

V_{IL} = -2.0V for pulse width less than 5ns, once per cycle.
V_{IH} = V_{CC} +2.0V for pulse width less than 5ns, once per cycle.

DC operating characteristics (over the operating range)[1]

Parameter	Sym	Test conditions	AS7C31026C-12		Unit
			Min	Max	
Input leakage current	$\lvert I_{LI} \rvert$	V_{CC} = Max V_{IN} = GND to V_{CC}	–	5	µA
Output leakage current	$\lvert I_{LO} \rvert$	V_{CC} = Max $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	5	µA
Operating power supply current	I_{CC}	V_{CC} = Max, $\overline{CE}$? V_{IL}, I_{OUT} = 0mA f = f_{Max}	–	160	mA
Standby power supply current	I_{SB}	V_{CC} = Max, $\overline{CE}$? V_{IH}, f = f_{Max}	–	45	mA
	I_{SB1}	V_{CC} = Max, $\overline{CE}$? V_{CC}–0.2 V, V_{IN} ? 0.2 V or V_{IN} ? V_{CC}–0.2 V, f = 0	–	10	mA
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min	2.4	–	V

Capacitance (f = 1MHz, T_a = 25 °C, V_{CC} = NOMINAL)[2]

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$, $\overline{LB}$, $\overline{UB}$	V_{IN} = 0 V	6	pF
I/O capacitance	$C_{I/O}$	I/O	V_{IN} = V_{OUT} = 0 V	7	pF

Note:
1. This parameter is guaranteed by device characterization, but is not production tested.

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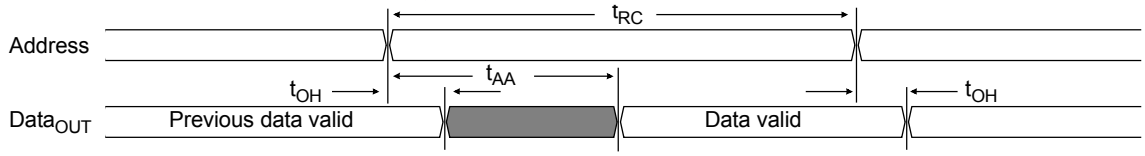
Read cycle (over the operating range)[3,9]

Parameter	Symbol	AS7C31026C-12		Unit	Notes
		Min	Max		
Read cycle time	t_{RC}	12	–	ns	
Address access time	t_{AA}	–	12	ns	3
Chip enable ($\overline{CE}$) access time	t_{ACE}	–	12	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}	–	6	ns	
Output hold from address change	t_{OH}	4	–	ns	5
$\overline{CE}$ low to output in low Z	t_{CLZ}	4	–	ns	4, 5
$\overline{CE}$ high to output in high Z	t_{CHZ}	–	6	ns	4, 5
$\overline{OE}$ low to output in low Z	t_{OLZ}	0	–	ns	4, 5
Byte select access time	t_{BA}	–	5	ns	
Byte select Low to low Z	t_{BLZ}	0	–	ns	4, 5
Byte select High to high Z	t_{BHZ}	–	6	ns	4, 5
$\overline{OE}$ high to output in high Z	t_{OHZ}	–	6	ns	4, 5
Power up time	t_{PU}	0	–	ns	4, 5
Power down time	t_{PD}	–	12	ns	4, 5

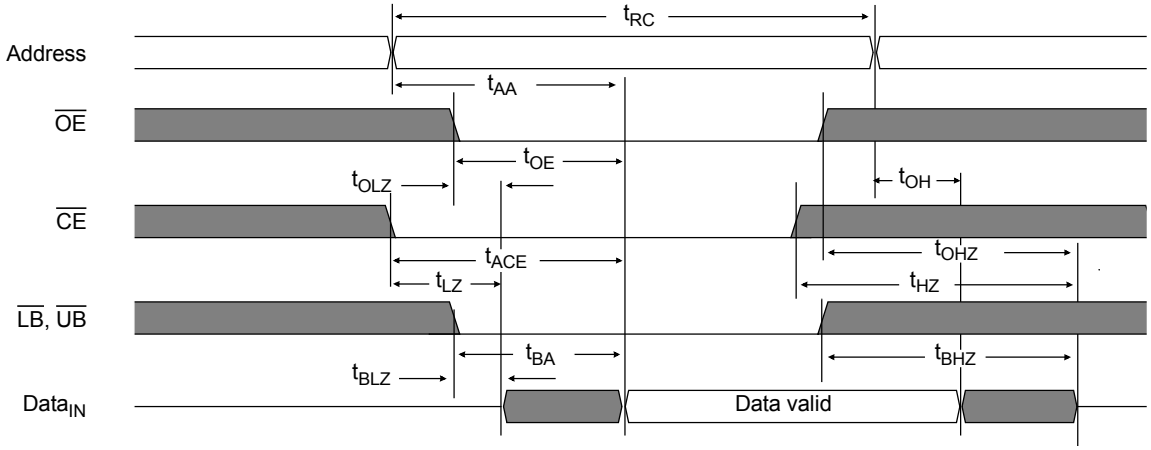
Key to switching waveforms

Rising input Falling input Undefined output/don't care

Read waveform 1 (address controlled)[3,6,7,9]



Read waveform 2 ($\overline{OE}$, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ controlled)[3,6,8,9]

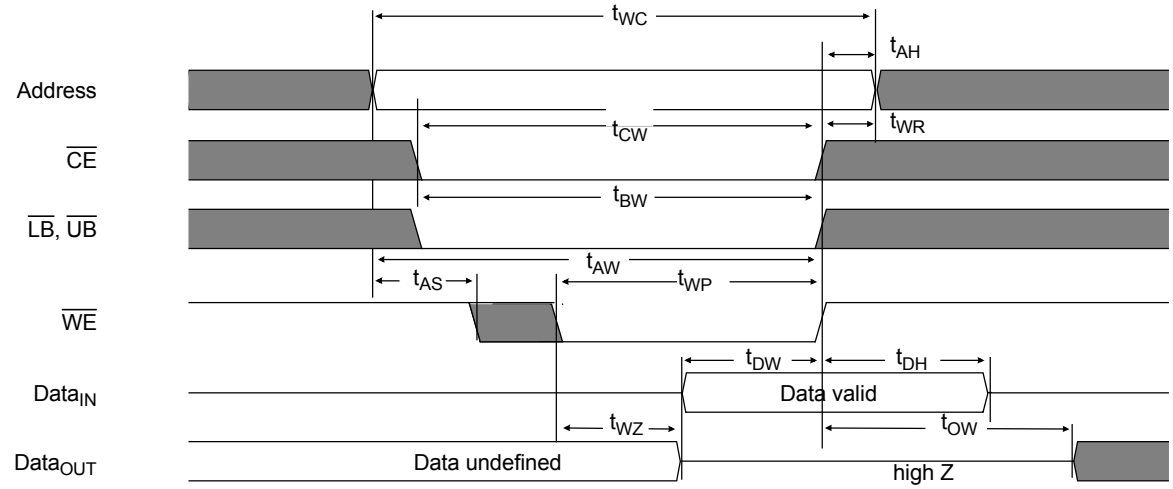


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Write cycle (over the operating range) [11]

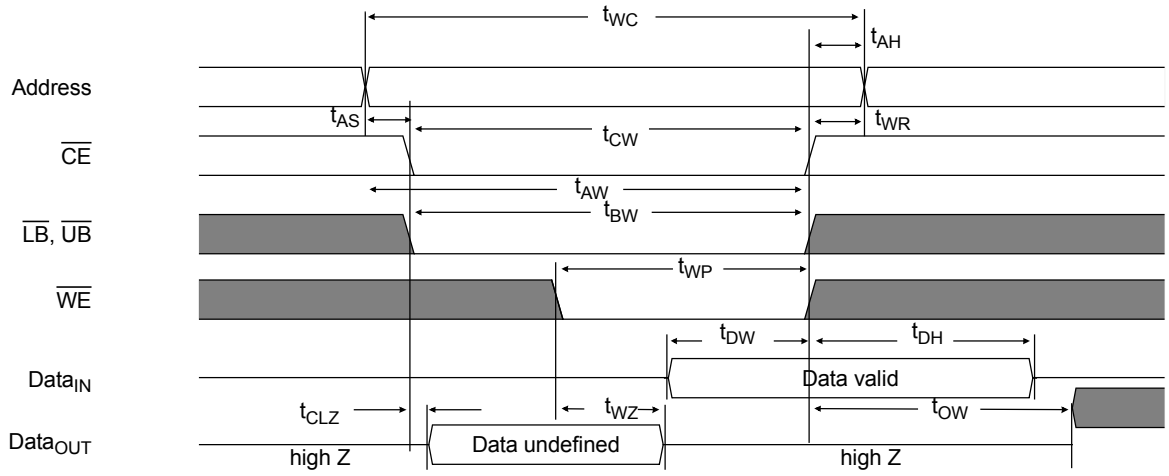
Parameter	Symbol	AS7C31026C-12		Unit	Notes
		Min	Max		
Write cycle time	t_{WC}	12	–	ns	
Chip enable ($\overline{CE}$) to write end	t_{CW}	8	–	ns	
Address setup to write end	t_{AW}	8	–	ns	
Address setup time	t_{AS}	0	–	ns	
Write pulse width	t_{WP}	8	–	ns	
Write recovery time	t_{WR}	0	–	ns	
Address hold from end of write	t_{AH}	0	–	ns	
Data valid to write end	t_{DW}	6	–	ns	
Data hold time	t_{DH}	0	–	ns	5
Write enable to output in high Z	t_{WZ}	–	6	ns	4, 5
Output active from write end	t_{OW}	3	–	ns	4, 5
Byte select low to end of write	t_{BW}	8	–	ns	

Write waveform 1 ($\overline{WE}$ controlled)[10,11]



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Write waveform 2 ($\overline{CE}$ controlled)[10,11]



AC test conditions

- Output load: see Figure B.
- Input pulse level: GND to 3.0 V. See Figure A.
- Input rise and fall times: 3 ns. See Figure A.
- Input and output timing reference levels: 1.5

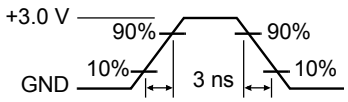


Figure A: Input pulse

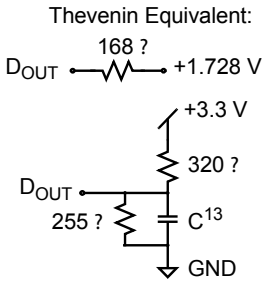


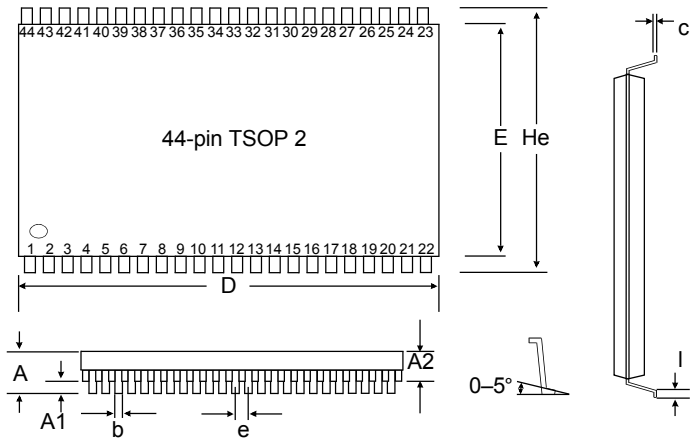
Figure B: 3.3 V Output load

Notes

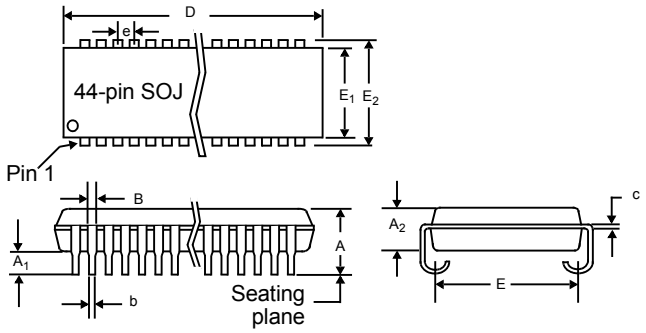
1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
2 This parameter is sampled, but not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A and B.
4 These parameters are specified with C_L = 5 pF, as in Figures B. Transition is measured ± 200 mV from steady-state voltage.
5 This parameter is guaranteed, but not tested.
6 $\overline{WE}$ is high for read cycle.
7 $\overline{CE}$ and $\overline{OE}$ are low for read cycle.
8 Address is valid prior to or coincident with $\overline{CE}$ transition low.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 N/A
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 Not applicable.
13 C = 30 pF, except all high Z and low Z parameters where C = 5 pF.

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Package dimensions



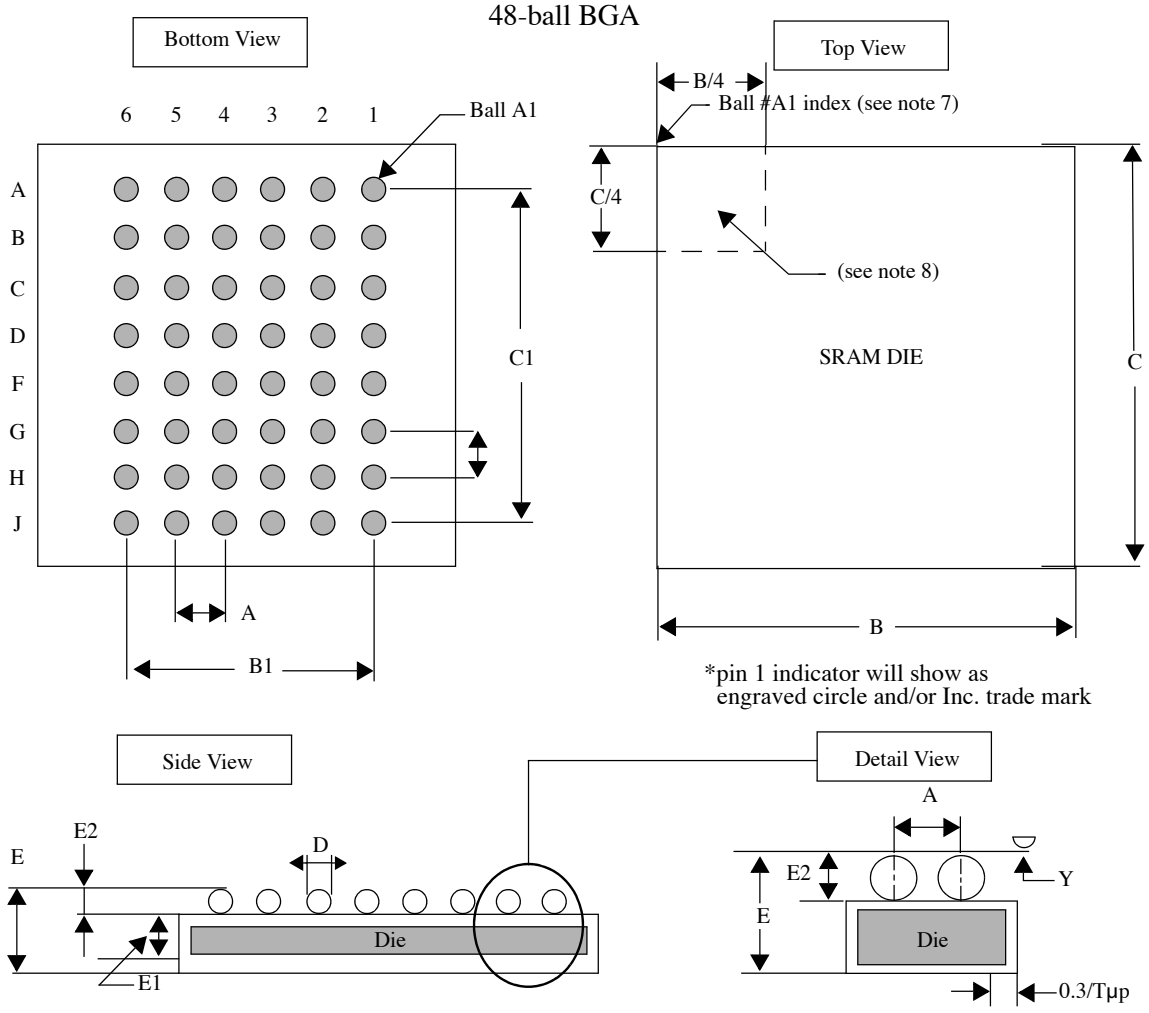
	44-pin TSOP 2	
	Min (mm)	Max (mm)
A		1.2
A1	0.05	0.15
A2	0.95	1.05
b	0.30	0.45
c	0.120	0.21
D	18.31	18.52
E	10.06	10.26
He	11.68	11.94
e	0.80 (typical)	
l	0.40	0.60



	44-pin SOJ 400 mil	
	Min (in)	Max (in)
A	0.128	0.148
A_1	0.025	–
A_2	0.105	0.115
B	0.026	0.032
b	0.015	0.020
c	0.007	0.013
D	1.120	1.130
E	0.370 NOM	
E_1	0.395	0.405
E_2	0.435	0.445
e	0.050 NOM	

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48-ball BGA



	Minimum	Typical	Maximum
A	–	0.75	–
B		7.00 BSC	
B1	–	3.75	–
C		7.00 BSC	
C1	–	5.25	–
D	0.25	0.30	0.40
E	1.14	1.24	1.34
E1	–	0.68	–
E2	0.15	0.20	0.25
Y	–	–	0.010

Notes

1 Bump counts: 48 (8 row x 6 column).
2 Pitch: (x,y) = 0.75 mm x 0.75 mm (typ).
3 Units: millimeters.
4 All tolerance are +/- 0.050 unless otherwise specified.
5 Typ: typical.
6 Y is coplanarity: 0.010 (max).
7 "A1" ID corner must be identified by chamfer, ink mark, metallized marking, indentation or other feature on the package body.
8 If "A1" ID corner is on the package body, it must be located within the zone indicated.

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Ordering codes

Package	Volt/Temp	12 ns
Plastic SOJ, 400 mil	3.3V industrial	AS7C31026C-12JIN
TSOP 2, 10.2 x 18.4 mm	3.3V industrial	AS7C31026C-12TIN
BGA, 7 x 7 mm	3.3V industrial	AS7C31026C-12BIN

Part numbering system

AS7C	X	1026B	–XX	X	X	X
SRAM prefix	Voltage: 3 = 3.3 V CMOS	Device number	Access time	Package: J = SOJ 400 mil T = TSOP 2, 10.2 x 18.4 mm B=BGA, 7 x 7 mm	Temperature I = industrial: -40° C to 85° C	N = Lead Free Part

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Web:www.manduic.com
Tel:150-1290-5940
Email:sales@manduic.com

Alliance Memory, Inc.
511 Taylor Way
San Carlos, CA 94070, USA
Tel: 650-610-6800
Fax: 650-620-9211

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Part Number: AS7C31026C-12JIN
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