Revision History

512M SDRAM 54/86pin TSOP II Package

Revision	Details	Date
Rev 1.0	Preliminary datasheet	Sep. 2018

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1 Overview

This chapter gives an overview of the 512-Mbit Synchronous DRAM component product and describes its main characteristics.

1.1 Features

- Fully Synchronous to Positive Clock Edge
- Fast clock rate: 133 MHz
- Multiple Burst Read with Single Write Operation
- Four Banks controlled by BA0 & BA1
- Data Mask for Byte Control (x16,x32)
- Programmable Mode registers
  - CAS Latency: 1 or 2 or 3
  - Burst Length: 1, 2, 4, 8, or full page
  - Burst Type: Sequential or Interleaved
- Automatic and Controlled Precharge Command
- Auto Refresh and Self Refresh
- 8192 refresh cycles/64ms(7.8 μs) T≦85°C
- Power down mode
- Data Mask for Read / Write control (x8, x16, x32)
- Random Column Address every CLK (1-N Rule)
- Single +3.3V±0.3V power supply
- Operating Temperature Range:
  - Industrial: T_A = -40~85°C
- Interface: LVTTL
- Available in 86/54 Pin 400 mil plastic TSOP II package,TSOPII–54 (x8, x16) TSOPII–86 (x32)

- Pb free and Halogen free

Table 1. Key Specifications

Speed Code			-7	Unit
System Frequency (f_{CK})			133	MHz
Max. Clock Frequency	@CL3	t_{CK3}	7.5	ns
		t_{AC3}	5.4	ns
	@CL2	t_{CK2}	10	ns
		t_{AC2}	6	ns
	@CL1	t_{CK1}	20	ns
		t_{AC1}	17	ns

Table 2. Ordering Information

Part Number	Frequency	Package	Temperature	Temp Range
AS4C16M32SC-7TIN	133MHz	86 Pin TSOP II	Industrial	-40°C to 85°C
AS4C32M16SC-7TIN	133MHz	54 Pin TSOP II	Industrial	-40°C to 85°C
AS4C64M8SC-7TIN	133MHz	54 Pin TSOP II	Industrial	-40°C to 85°C

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1.2 Description

The AS4C16M32SC-7TIN, AS4C32M16SC-7TIN and AS4C64M8SC-7TIN are four bank Synchronous DRAMs organized as 4 banks x 4MBit x32, 4 banks x 8Mbit x 16 and 4 banks x 16MBit x 8MBit x 8 respectively. These synchronous devices achieve high speed data transfer rates for CAS latencies by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.

The device is designed to comply with all industry standards set for synchronous DRAM products, both electrically and mechanically.All of the control, address, data input and output circuits are synchronized with the positive edge externally supplied clock.

Operating the four memory banks in an interleave fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, CAS latency and speed grade of the device.

Auto Refresh (CBR) and Self Refresh operation are supported. These devices operate with a single 3.3 V ± 0.3 V power supply. All 512-Mbit components are available in TSOPII–[86/54] packages.

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2 Configuration

This chapter contains the pin configuration table, the TSOP package drawing,

2.1 Pin Description

Listed below are the pin configurations sections for the various signals of the SDRAM

Table 3.
Configuration TSOP-54/86

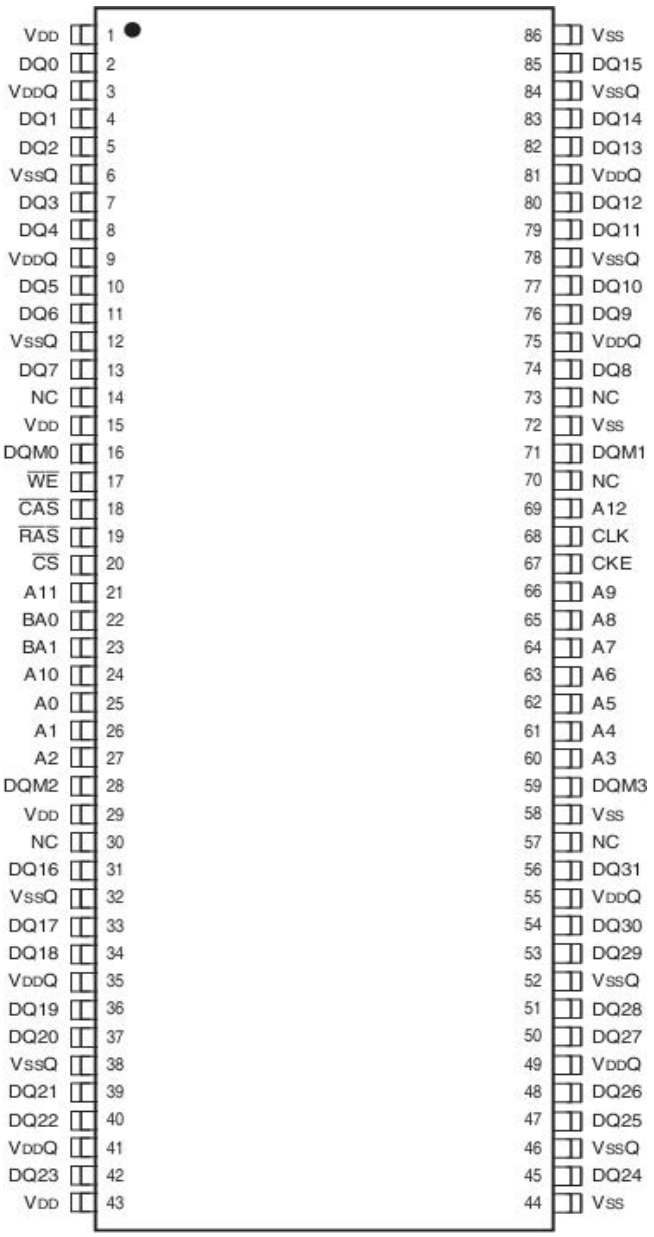
Name	Pin Type	Buffer Type	Function
Clock Signals			
CLK	I	LVTTL	**Clock Signal CK**
CKE	I	LVTTL	**Clock Enable** Note: Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiating either the Power Down mode, Suspend mode, or the Self Refresh mode.
Control Signals			
$\overline{RAS}$	I	LVTTL	**Row Address Strobe**
$\overline{CAS}$	I	LVTTL	**Column Address Strobe**
$\overline{WE}$	I	LVTTL	**Write Enable**
$\overline{CS}$	I	LVTTL	**Chip Select**
Address Signals			
BA0~BA1	I	LVTTL	**Bank Address Signals 1:0** Note: Bank Select Inputs. Bank address inputs selects which of the four banks a command applies to.
A0~A12	I	LVTTL	**Address Signal 9:0, Address Signal 10/Auto precharge** Note: During a Bank Activate command cycle, A0-A12 define the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-An define the column address (CA0-CAn) when sampled at the rising clock edge. CAn depends upon the SDRAM organization: 64M x8SDRAM CAn = CA9,CA11 (Page Length = 2048bits) 32M x16SDRAM CAn = CA9 (Page Length = 1024 bits) 16M x32SDRAM CAn = CA8 (Page Length = 512bits) In addition to the column address, A10 (= AP) is used to invoke the auto pre charge operation at the end of the burst read or write cycle. If A10 is high, auto pre charge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, auto pre charge is disabled. During a Precharge command cycle, A10 (= AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will be precharged regardless of the state of BA0 and BA1. If A10 is low, then BA0 and BA1 are used to define which bank to precharge.

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Name	Pin Type	Buffer Type	Function
Data Signals			
DQ0~DQ31	I/O	LVTTL	**Data Signal 31:0**
DQM(x8)/ LDQM(x16)/ DQM0(x32)	I	LVTTL	**Data Mask for DQ0~DQ7**
UDQM(x16)/ DQM1(x32)	I	LVTTL	**Data Mask for DQ8~DQ15**
DQM2(x32)	I	LVTTL	**Data Mask for DQ16~DQ23**
DQM3(x32)	I	LVTTL	**Data Mask for DQ24~DQ31**
Power Supplies			
V_{DDQ}	Suply	–	**Power Supply for DQs**
V_{DD}	Suply	–	**Power Supply**
V_{SSQ}	Suply	–	**Power Supply Ground for DQs**
V_{SS}	Suply	–	**Power Supply Ground**
Not Connected			
NC	NC	—	**Not Connected**

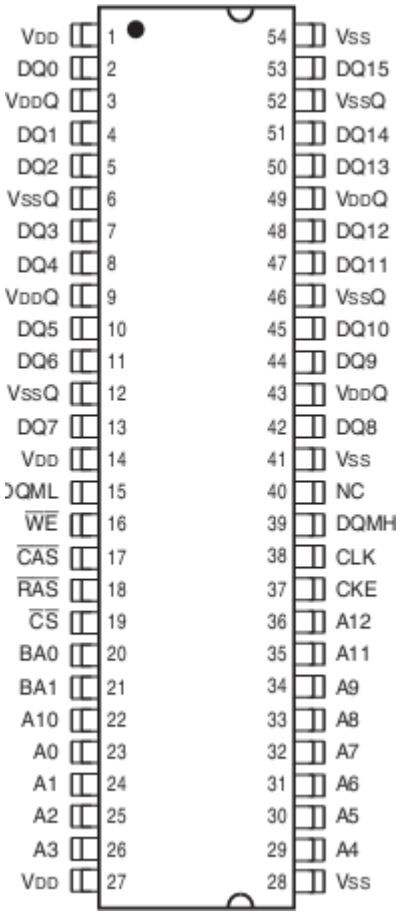
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Figure 1
Configuration for x32 Organization, TSOP86, Top View



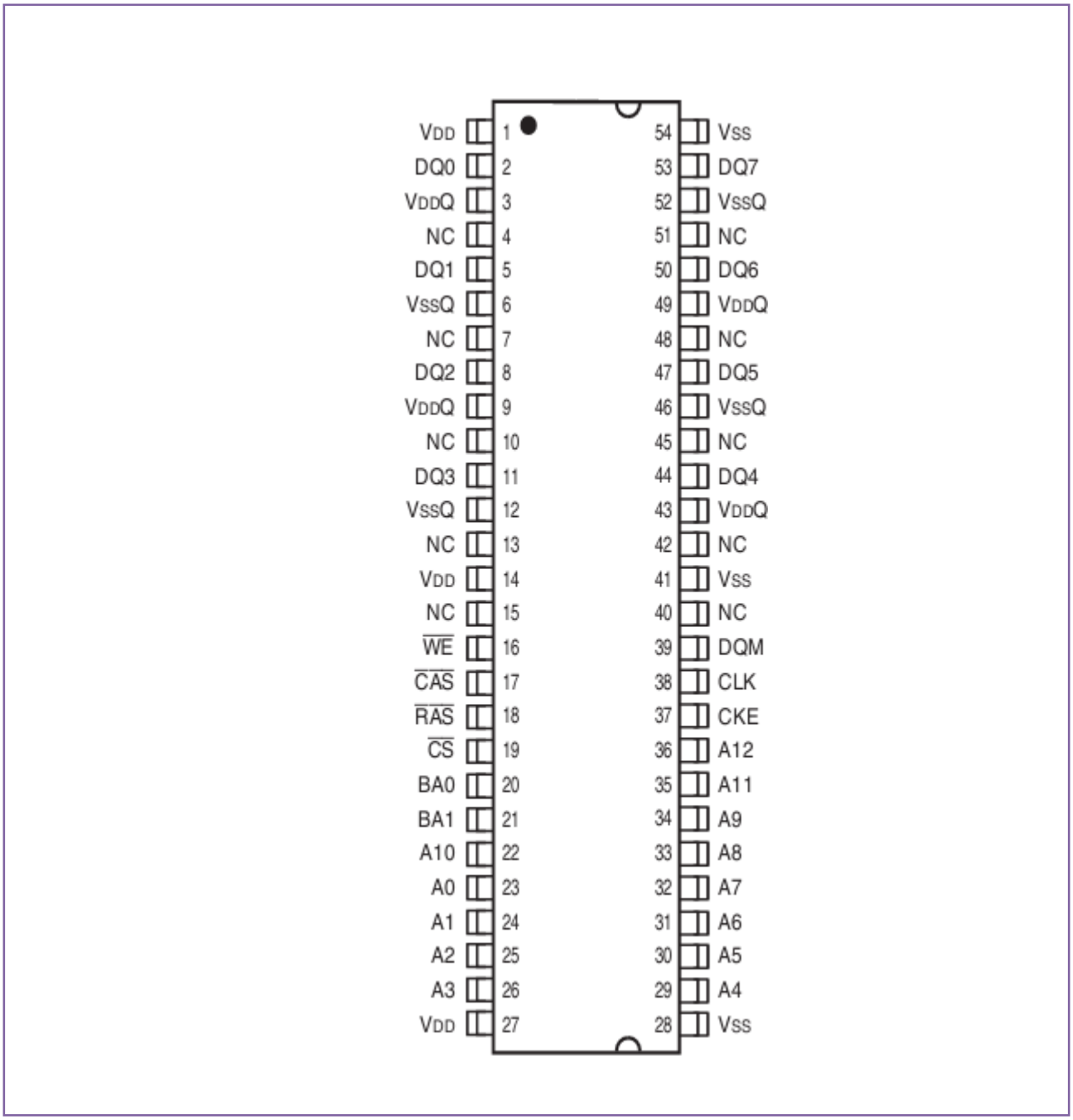
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Figure 2
Configuration for x16 Organization, TSOP-54, Top View



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Figure 3
Configuration for x8 Organization, TSOP-54, Top View



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3 Functional Description

3.1 Operation Definition

All of SDRAM operations are defined by states of control signals $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and DQM at the positive edge of the clock. The following list shows the truth table for the operation commands.

Table 4
Truth table

Operation	Device State	CKE n-1 1)2)	CKE n 1)2)	DQM 1)2)	BA0 BA1 1)2)	AP= A10 1)2)	Addr. 1)2)	$\overline{CS}$ 1)2)	$\overline{RAS}$ 1)2)	$\overline{CAS}$ 1)2)	$\overline{WE}$ 1)2)
Bank Active	Idle 3)	H	X	X	V	V	V	L	L	H	H
Bank Precharge	Any	H	X	X	V	L	X	L	L	H	L
Precharge All	Any	H	X	X	X	H	X	L	L	H	L
Write	Active 3)	H	X	X	V	L	V	L	H	L	L
Write with Auto pre charge	Active 3)	H	X	X	V	H	V	L	H	L	L
Read	Active 3)	H	X	X	V	L	V	L	H	L	H
Read with Auto pre charge	Active 3)	H	X	X	V	H	V	L	H	L	H
Mode Register Set	Idle	H	X	X	V	V	V	L	L	L	L
No Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
Auto Refresh	Idle	H	H	X	X	X	X	L	L	L	H
Self Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
Self Refresh Exit	Idle (Self Refr.)	L	H	X	X	X	X	H	X	X	X
								L	H	H	X
Clock Suspend Entry	Active	H	L	X	X	X	X	X	X	X	X
Power Down Entry (Precharge or active standby)	Idle	H	L	X	X	X	X	H	X	X	X
	Active							L	H	H	H
Clock Suspend Exit	Active 4)	L	H	X	X	X	X	X	X	X	X
Power Down Exit	Any (Power Down)	L	H	X	X	X	X	H	X	X	X
								L	H	H	L
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Write/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

1) V = Valid, x = Don't Care, L = Low Level, H = High Level
2) CKEn signal is input level when commands are provided, CKEn-1 signal is input level one clock before the commands are Provided
3) This is the state of the banks designated by BA0, BA1 signals.
4) Power Down Mode can not be entered in a burst cycle. When this command asserted in the burst mode cycle device is in clock suspend mode.

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3.2 Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs. Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner. During power on, all VDD and VDDQ pins must be built up simultaneously to the specified voltage when the input signals are held in the “NOP” state. The power on voltage must not exceed VDD + 0.3 V on any of the input pins or VDD supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200 µs is required followed by a precharge of all banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required. These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

3.3 Mode Register Definition

The Mode register designates the operation mode at the read or write cycle. This register is divided into four fields. First, a Burst Length field which sets the length of the burst. Second, an Addressing Selection bit which programs the column access sequence in a burst cycle (interleaved or sequential). Third, a CAS Latency field to set the access time at clock cycle. Fourth, an Operation mode field to differentiate between normal operation (Burst read and burst Write) and special Burst Read and Single Write mode. After the initial power up, the mode set operation must be done before any activate command. Any content of the mode register can be altered by re-executing the mode set command. All banks must be in precharged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of RAS, CAS, and WE at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the previous table.

BA0	BA1	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	reserved		weak OCD	wrbst	reserved		CL			BT	BL		

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Table 5
Mode Register Definition

Field	Bits	Type[1)]	Description
BL	[2:0]	W	**Burst Length**
			000_B1,
			001_B 2,
			010_B 4,
			011_B 8,
			111_B Full Page (Sequential burst type only),
BT	[3]		**Burst Type**
			0 Sequential
			1 Interleaved
	[6:4]		**CAS Latency**
CL			*Note: All other bit combinations are RESERVED.*
			010_B **2**
			011_B **3**
MODE	[8:7]		**RESERVED**
wrbst	[9]		**Write Burst Mode**
			0_BProgrammed Burst Length,
			1_BSingle Location Access,
Weak	[10]		**Weak OCD Mode**
OCD			
			0_Bnormal OCD,
			1_Bweak OCD,
MODE	[12:11]		**RESERVED**

1) W = write only register bit

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3.4 Burst Type

Accesses within a given burst may be programmed to be sequential or interleaved; as shown in table 6.

Table 6
Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type = Sequential	Type = Interleaved
2			0	0-1	0-1
			1	1-0	1-0
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full page	n			Cn, Cn+1, Cn+2	not supported

Notes

1. For a burst length of two, A1-Ai selects the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-Ai selects the four-data-element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-Ai selects the eight-data- element block; A0-A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

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3.5 Commands

Refresh Mode

SDRAM has two refresh modes, Auto Refresh and Self Refresh. Auto Refresh is similar to the CAS -before-RAS refresh of conventional DRAMs. All banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes.

The chip enters the Auto Refresh mode, when $\overline{RAS}$ and $\overline{CAS}$ are held low and CKE and $\overline{WE}$ are held high at a clock timing. The mode restores word line after the refresh and no external precharge command is necessary. A minimum tRC time is required between two automatic refreshes in a burst refresh mode. The same rule applies to any access command after the automatic refresh operation.

The chip has an on-chip timer and the Self Refresh mode is available. The mode restores the word lines after, $\overline{RAS}$ $\overline{CAS}$ and CKE are low and $\overline{WE}$ is high at a clock timing. All of external control signals including the clock are disabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one tRC delay is required prior to any access command.

Auto Precharge

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the CAS timing accepts one extra address, CA10, to determine whether the chip restores or not after the operation. If CA10 is high when a Read Command is issued, the Read with Auto-Precharge function is initiated. If CA10 is high when a Write Command is issued, the Write with Auto-Precharge function is initiated. The SDRAM automatically enters the precharge operation a time delay equal to tWR ("write recovery time") after the last data in. A burst operation with Auto-Precharge may only be interrupted by a burst start to another bank. It must not be interrupted by a precharge or a burst stop command.

Precharge Command

There is also a separate precharge command available. When $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at a clock timing, it triggers the precharge operation. Three address bits, BA0, BA1 and A10 are used to define banks as shown in the following list. The precharge command can be imposed one clock before the last data out for CAS latency = 2 and two clocks before the last data out for CAS latency = 3. Writes require a time delay tWR ("write recovery time") of 2 clocks minimum from the last data out to apply the precharge command.

Table 7

Bank Selection by Address Bits

A10	BA0	BA1	
0	0	0	Bank 0
0	0	1	Bank 1
0	1	0	Bank 2
0	1	1	Bank 3
1	X	X	All Banks

Burst Termination

Once a burst read or write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid DQ contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the DQ pins before the Burst Stop Command is registered will be written to the memory.

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3.6 Operations

When $\overline{RAS}$ is low and both $\overline{CAS}$ and $\overline{WE}$ are high at the positive edge of the clock, a $\overline{RAS}$ cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the wordline are set. A *CAS* cycle is triggered by $\overline{RAS}$ setting high and $\overline{CAS}$ low at a clock

timing after a necessary delay, tRCD from the $\overline{RAS}$ timing. $\overline{WE}$ is used to define either a read($\overline{WE}$=H) or a write($\overline{WE}$=L) at this stage.

SDRAM provides a wide variety of fast access modes. In a single*CAS* cycle, serial data read or write operations are allowed at up to a 166 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4 and 8 and full page. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the *CAS* timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is '2', then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.

Full page burst operation is only possible using the sequential burst type and page length is a function of the I/O organization and column addressing. Full page burst operation does not self terminate once the burst length has been reached. In other words, unlike burst lengths of 2, 4 and 8, full page burst continues until it is terminated using another command.

Similar to the page mode of conventional DRAMs, burst read or write accesses on any column address are possible once the *RAS* cycle latches the sense amplifiers. The maximum tRAS or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycle is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two or more banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two or more banks can realize fast serial data access modes among many different pages. Once two or more banks are activated, column to column interleave operation can be performed between different pages.

DQM Function

DQM has two functions for data I/O read and write operations. During reads, when it turns to "high" at a clock timing, data outputs are disabled and become high impedance after two clock delay (DQM Data Disable Latency tDQZ). It also provides a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency tDQW = zero clocks).

Power Down

In order to reduce standby power consumption, a power down mode is available. All banks must be precharged and the necessary Precharge delay (tRP) must occur before the SDRAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can't remain in Power Down mode longer than the Refresh period (tREF) of the device. Exit from this mode is performed by taking CKE "high". One clock delay is required for Power Down mode entry and exit.

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4 Electrical Characteristics

4.1 Operating Conditions

Table 8
Absolute Maximum Ratings

Symbol	Item		Values	Unit	Note
V_{IN}, V_{OUT}	Input, Output Voltage		-1.0 ~ 4.6	V	
V_{DD}, V_{DDQ}	Power Supply Voltage		-1.0 ~ 4.6	V	
T_A	Ambient Temperature	Industrial	-40 ~ 85	°C	
T_{STG}	Storage Temperature		-55 ~ 105	°C	
T_{SOLDER}	Soldering Temperature (10 seconds)		260	°C	
P_D	Power Dissipation		1	W	
I_{OS}	Short Circuit Output Current		50	mA	

Attention: Stresses above the max. values listed here may cause permanent damage to the device.
Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 9
Operating Temperature

Symbol	Parameter	Rating		Unit	Note/ Test Condition
		Min	Max		
Toper	Operating temperature	– 40	85	°C	Industrial temperature range

1) Operating Temperature is the operating ambient temperature surrounding the DRAM.
2) The operating temperature range are the temperatures where all DRAM specification will be supported.

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Table 10
DC Characteristics

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
Supply Voltage	V_{DD}	3.0	3.6	V	2)
I/O Supply Voltage	V_{DDQ}	3.0	3.6	V	2)
Input high voltage	V_{IH}	2.0	V_{DDQ}+0.3	V	2)3)
Input low voltage	V_{IL}	– 0.3	+0.8	V	2)3)
Output high voltage (I_{OUT} = – 4.0 mA)	V_{OH}	2.4	–	V	2)
Output low voltage (I_{OUT} = 4.0 mA)	V_{OL}	–	0.4	V	2)
Input leakage current, any input (0 V < V_{IN} < V_{DD}, all other inputs = 0 V)	I_{IL}	– 10	+10	µA	–
Output leakage current (DQs are disabled, 0 V < V_{OUT} < V_{DDQ})	I_{OL}	– 10	+10	µA	–

1) All voltages are referenced to VSS
2) VIH may overshoot to VDDQ + 2.0 V for pulse width of < 4ns with 3.3 V. VIL may undershoot to -2.0 V for pulse width < 4.0 ns with 3.3 V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

Table 11
Input and Output Capacitances

Symbol	Parameter	Min.	Max.	Unit
C_{I1}	Input Capacitances: CK, CK	2.5	3.5	pF
C_{I2}	Input Capacitance (A0-A12, BA0, BA1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM)	2.5	3.8	pF
C_{I0}	Input/Output Capacitance (DQ)	4.0	6.0	pF

1) VDD, VDDQ = 3.3 V ± 0.3 V, f = 1 MHz

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Table 12

X32/X16/X8 **D.C. Characteristics (VDD = 3.3V ± 0.3V)**

Description/Test condition	Symbol	IDDmax			Unit	Notes
		X32	X16	X8		
Operating Current tRC = tRC(min),tRC = tck(min),Burst length=1,One bank active	IDD1	70	60	60	mA	1,3
Precharge Standby Current in non-power down mode tCK =min, CS# = VIH,CKE≥ VIL(max)	IDD2N	15	15	15	mA	3
Precharge Standby Current in Power Down Mode tCK = min. CS =VIH,CKE≤ VIL(max),	IDD2P	4	4	4	mA	1,3
No Operating Current Active state (max. 4 banks) CS = VIH(min), CKE ≥VIH(min.),tCK = min,	IDD3N	20	20	20	mA	3
No Operating Current Active state (max. 4 banks) CS = VIH(min), CKE ≤ VIL(max.) tCK = min,	IDD3P	6	6	6	mA	3
Burst Operating Current Read/Write command cycling tCK = min	IDD4	90	80	70	mA	1,2,3
Auto Refresh Current Auto Refresh command cycling tRC= tRC(min),tCK = min	IDD5	170	170	170	mA	1,3
Self Refresh Current Self Refresh Mode, CKE≤ 0.2V, tCK=infinity	IDD6	5	5	5	mA	3

Notes:
1. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of tCK and tRC. Input signals are changed one time during tCK.
2. These parameter depend on output loading. Specified values are obtained with output open.
3. The temperature from -40°C~85°C

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4.2 AC Characteristics

Table 13
AC Electrical Characteristics and Recommended A.C. Operating Conditions

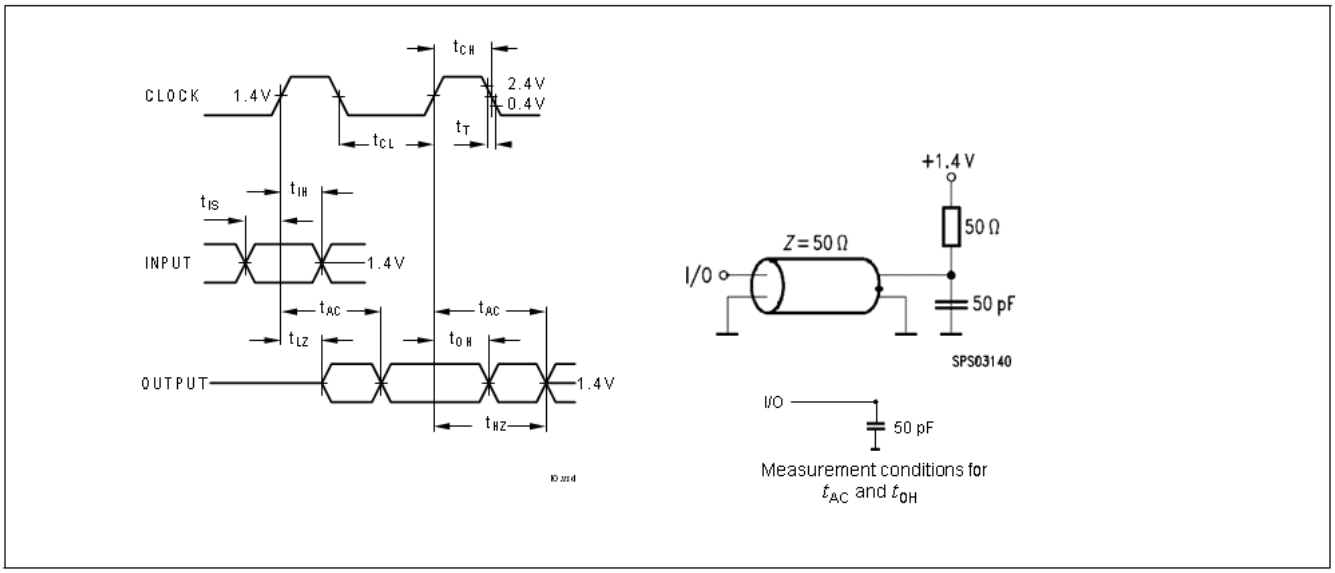
Symbol	A.C. Parameter		-7		Unit	Note
			Min.	Max.		
t_{RC}	Row cycle time (same bank)		66	-	ns	7
t_{RFC}	Row Cycle Time during Auto Refresh		66	-		
t_{RCD}	Row to Column Delay Time		15	-		7
t_{RP}	Row Precharge Time		15	-		7
t_{RRD}	Row activate to row activate delay (different banks)		15	-		7
t_{MRD}	Mode register set cycle time		2	-	tck	
t_{RAS}	Row activate to precharge time (same bank)		44	120K	ns	7
t_{WR}	Write recovery time		15	-		8
t_{CK}	Clock cycle time	CL* = 1	20	-		
		CL* = 2	10	-		
		CL* = 3	7.5	-		
t_{AC}	Access time from CLK (positive edge)	CL* = 1	-	17		3,4, 5
		CL* = 2	-	6		
		CL* = 3	-	5.4		
t_{OH}	Data output hold time		2.7	-		3,5
t_{LZ}	Data output low impedance		1	-		
t_{HZ}	Data output high impedance	CL* = 1	-	17		
		CL* = 2	-	6		
		CL* = 3	-	5.4		
t_{DDE}	Power Down Exit set-up time		7.5	0		
t_{REF}	Refresh Period (8192 cycles)		-	64	ms	
t_{XSR}	Exit Self-Refresh to any Command		75	-	ns	
t_{IS}	Data/Address/Control Input set-up time		1.5	-		6
t_{IH}	Data/Address/Control Input hold time		0.8	-		6
t_{CH}	Clock High Pulse Width		2.5	-		
t_{CL}	Clock Low Pulse Width		2.5	-		
t_{CCD}	CAS# to CAS# Delay time		1	-	tck	
t_T	Transition time		0.3	1.2	ns	
t_{DQZ}	DQM Data Out Disable Latency		-	2	tck	
$t_{DAL(min.)}$	Last Data Input to Activate (Write with Auto Precharge)		30	-	ns	
t_{DQW}	DQM Write Mask Latency		0	-	tck	

1. VSS = 0 V; VDD, VDDQ = 3.3 V ± 0.3 V, tT = 1 ns
2. For proper power-up see the operation section of this data sheet.

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3. AC timing tests for LV-TTL versions have VIL = 0.4 V and VIH = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between VIH and VIL. All AC measurements assume tT = 1 ns with the AC output load circuit shown in figure below. Specified tAC and tOH parameters are measured with a 50 pF only, without any resistive termination and with an input signal of 1V /ns edge rate between 0.8 V and 2.0 V.
4. If clock rising time is longer than 1 ns, a time (tT/2 - 0.5) ns has to be added to this parameter.
5. Access time from clock tac is 4.6 ns for PC133 components with no termination and 0 pF load, Data out hold time toh is 1.8 ns for PC133 components with no termination and 0 pF load.
6. If tT is longer than 1 ns, a time (tT - 1) ns has to be added to this parameter.
7. These parameter account for the number of clock cycles and depend on the operating frequency of the clock, as follows:
the number of clock cycles = specified value of timing period (counted in fractions as a whole number)
8. It is recommended to use two clock cycles between the last data-in and the precharge command in case of a write command without Auto-Precharge. One clock cycle between the last data-in and the precharge command is also supported, but restricted to cycle times tCK greater or equal the specified tWR value, where tck is equal to the actual system clock time.
9. When a Write command with Auto Precharge has been issued, a time of tDAL(min) has be fullfilled before the next Activate Command can be applied. For each of the terms, if not already an integer, round up to the next highest integer. tCK is equal to the actual system clock time.

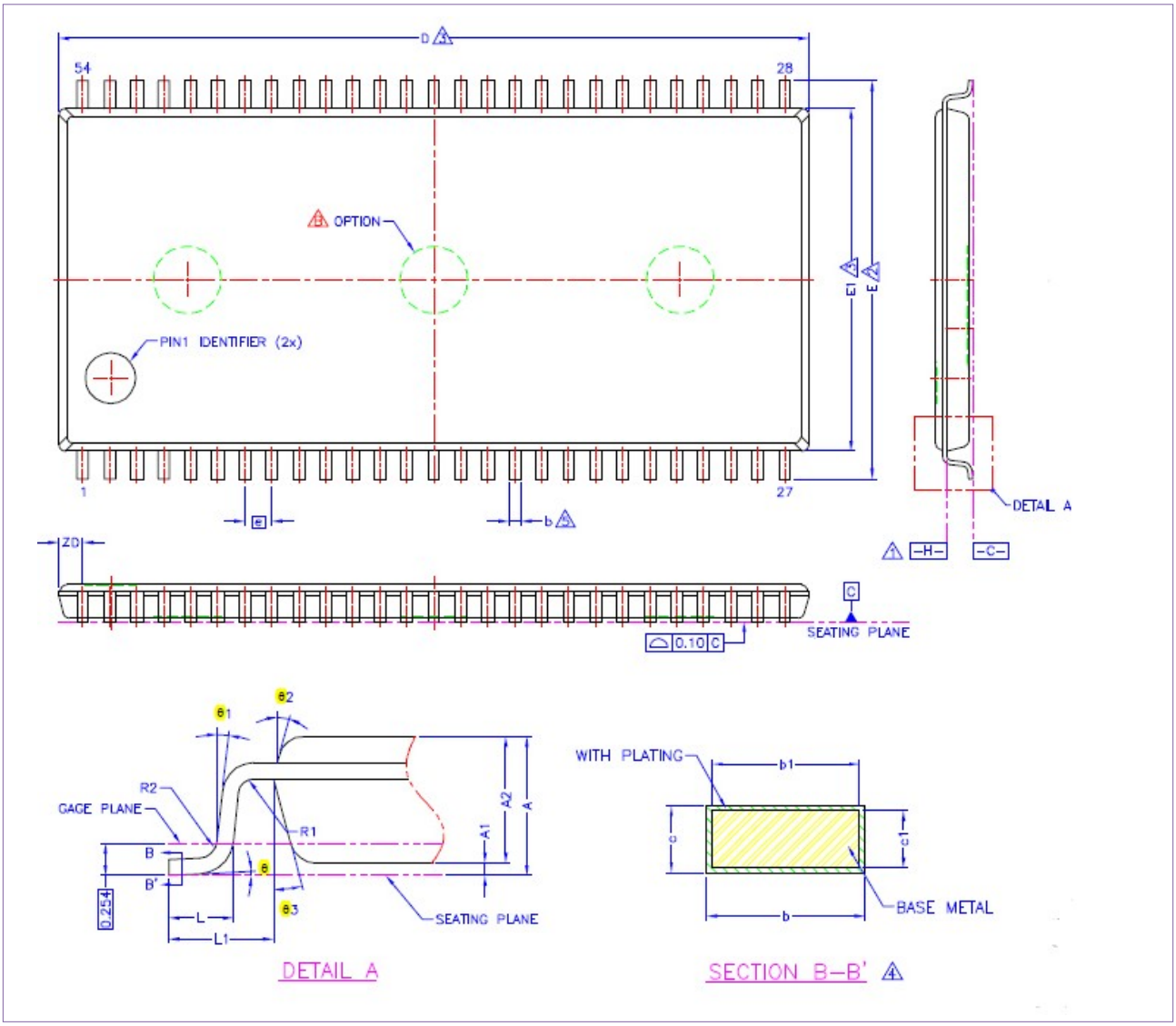
Figure 4
AC Output Load Circuit Diagram / Timing Reference Load



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5 Package Outlines

Figure 5
Package Outline TSOPII-54



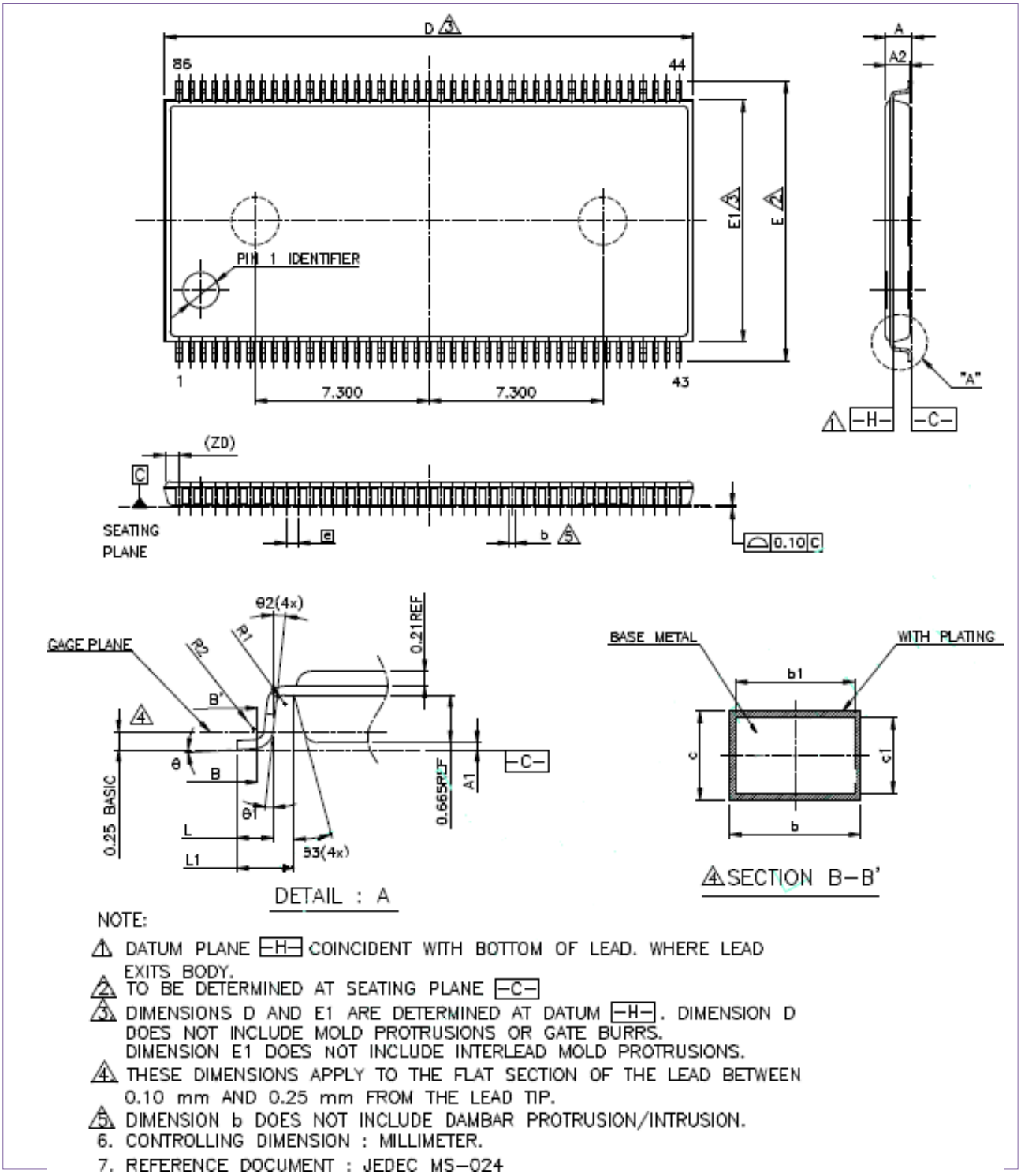
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Figure 6
Package Outline TSOPII-54

SYM.	DIMENSION (MM)			DIMENSION (INCH)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	–	–	1.20	–	–	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	–	0.45	0.012	–	0.018
b1	0.30	0.35	0.40	0.012	0.014	0.016
c	0.12	–	0.21	0.005	–	0.008
c1	0.10	0.127	0.16	0.004	0.005	0.006
D	22.22 BSC			0.875 BSC		
ZD	0.71 REF			0.028 REF		
E	11.76 BSC			0.463 BSC		
E1	10.16 BSC			0.400 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.80 REF			0.031 REF		
e	0.80 BSC			0.031 BSC		
R1	0.12	–	–	0.005	–	–
R2	0.12	–	0.25	0.005	–	0.010
θ	0°	–	8°	0°	–	8°
θ1	0°	–	–	0°	–	–
θ2	10°	15°	20°	10°	15°	20°
θ3	10°	15°	20°	10°	15°	20°

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Figure 7
Package Outline TSOPII-86



NOTE:

1. DATUM PLANE -H- COINCIDENT WITH BOTTOM OF LEAD. WHERE LEAD EXITS BODY.
2. TO BE DETERMINED AT SEATING PLANE -C-
3. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM -H-. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS. DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS.
4. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
6. CONTROLLING DIMENSION : MILLIMETER.
7. REFERENCE DOCUMENT : JEDEC MS-024

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Figure 8
Package Outline TSOPII-86

SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	—	0.27	0.007	—	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.12	—	0.21	0.005	—	0.008
c1	0.10	0.127	0.16	0.004	0.005	0.006
D	22.22 BSC			0.875 BSC		
ZD	0.61 REF			0.024 REF		
E	11.76 BSC			0.463 BSC		
E1	10.16 BSC			0.400 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.80 REF			0.031 REF		
e	0.50 BSC			0.0197 BSC		
R1	0.12	—	—	0.005	—	—
R2	0.12	—	0.25	0.005	—	0.010
θ	0°	—	8°	0°	—	8°
θ1	0°	—	—	0°	—	—
θ2	10°	15°	20°	10°	15°	20°
θ3	10°	15°	20°	10°	15°	20°

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PART NUMBERING SYSTEM

AS4C	16M32SC 32M16SC 64M8SC	-7	T	I	N	XX
DRAM	16M32=16M x 32 32M16=32M x 16 64M8=64M x 8 S=SDRAM C=C die	7=133 MHz	T=TSOP	I=Industrial temp -40°C~ 85°C	Indicates Pb and Halogen Free	Packing Type None:Tray TR:Reel

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