QSPI PSRAM

Specifications

- **Single Supply Voltage**
  - VDD=2.7 to 3.6V
- **Interface**: SPI/QPI with SDR mode
- **Performance**: Clock rate up to
  - 133MHz at VDD=3.0V+/-10%
  - 109MHz at VDD=3.3V+/-10%
- **Organization**: 64Mb, 8M x 8bits
- **Addressable Bit Range**: A[22:0]
- **Page Size**: 1024 bytes
- **Refresh**: Self-managed
- **Operating Temperature Range**:
  - T_{OPER} = -40°C to +85°C (standard range)
  - T_{OPER} = -40°C to +105°C (extended range)
- **Maximum Standby Current**:
  - 350µA @ 105°C
  - 250µA @ 85°C
- **Typical Standby Current**
  - 100µA @ 25°C

Features

- **50Ω Output Drive Strength LVCMOS**
- **1K Bytes Wrapped Burst** or **32 Bytes Wrapped Burst** via toggle command.
- **1K Bytes Wrapped Burst** as long as tCEM is met
- **Software Reset**

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2 Introduction

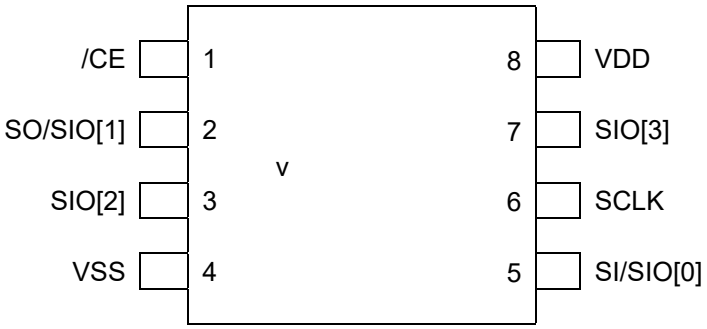
This Pseudo-SRAM device features a high speed, low pin count interface. It has 4 SDR I/O pins and operates in SPI(serial peripheral interface) or QPI (quad peripheral interface) mode with frequencies up to 133 MHz. The data input (A/DQ) to the memory relies on clock (CLK) to latch all instructions, addresses and data. It is most suitable for low-power and low cost portable applications. It incorporates a seamless self-managed refresh mechanism. Hence it does not require the support of DRAM refresh from system host. The self-refresh feature is a special design to maximize performance of memory read operation.

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3 Package Information

The APS6404L-3SQN is available in standard package including 8-lead SOP-8L(150) and advanced package including 8-lead USON-8L 3x2mm.

● **Package Type: SOP/USON (SN, ZR)**

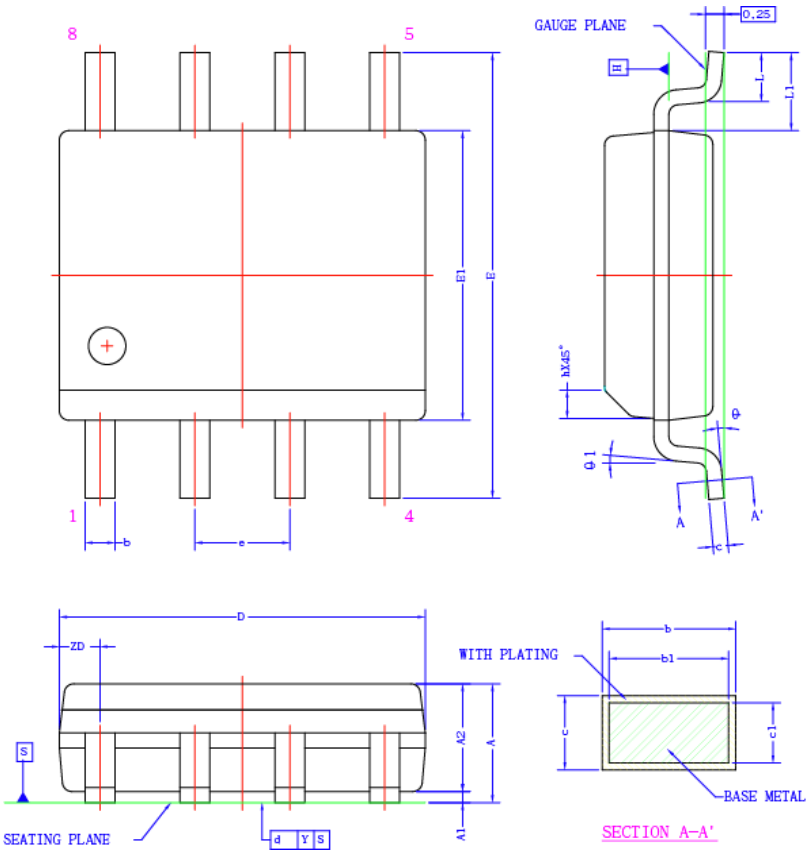


Top View

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4 Package Outline Drawing

4.1 SOP-8L(150), package code SN



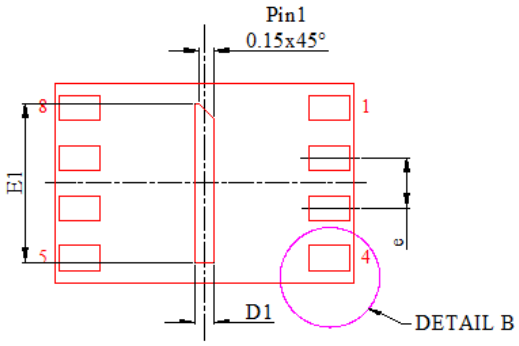
SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.60	1.75	53	63	69
A1	0.10	0.15	0.25	4	6	10
A2	1.35	1.45	1.55	53	57	61
b	0.31	–	0.51	12	–	20
b1	0.28	0.40	0.48	11	16	19
c	0.17	–	0.25	7	–	10
c1	0.17	0.20	0.23	7	8	9
D	4.80	4.90	5.00	189	193	197
E	6.00 BSC			236 BSC		
E1	3.80	3.90	4.00	150	154	157
e	1.27 BSC			50 BSC		
L	0.40	0.66	1.27	16	26	50
L1	1.05 REF			41 REF		
ZD	0.55 REF			22 REF		
h	0.25	0.38	0.50	10	15	20
Y	–	–	0.10	–	–	4
θ	0°	–	8°	0°	–	8°
θ1	0°	–	–	0°	–	–

NOTE :

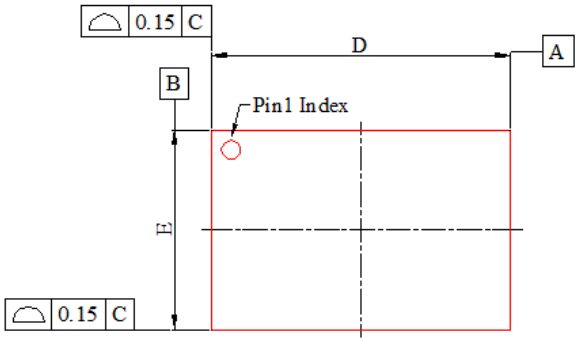
1. REFER TO JEDEC STD: MS-012 AA.
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS, MOLD FLASH, PROTRUSION AND GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
   DIMENSION "E1" DOES NOT INCLUDE INTERLEAD MOLD FLASH OR PROTRUSION. INTERLEAD MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
   'D' AND 'E1' DIMENSIONS ARE DETERMIND AT DATUM H .
3. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

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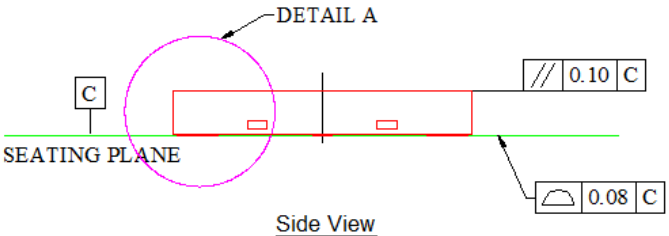
4.2 USON-8L 3x2mm, package code ZR



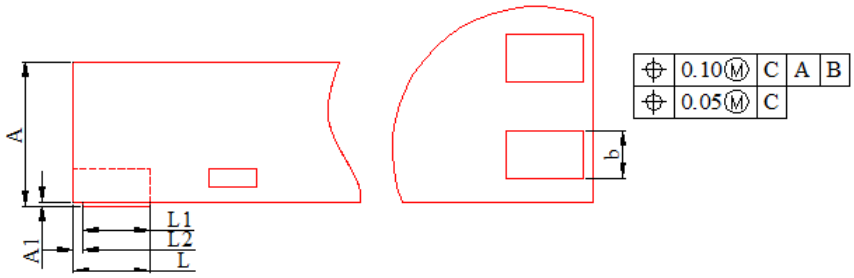
Bottom View



Top View



Side View



DETAIL A DETAIL B

Symbol	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.40	0.45	0.50
A1	0.00	---	0.05
D	2.90	3.00	3.10
D1	0.10	0.20	0.30
E	1.90	2.00	2.10
E1	1.50	1.60	1.70
L	0.40	0.45	0.50
L1	0.30	---	---
L2	---	---	0.15
b	0.20	0.25	0.30
e	0.50 BSC		

NOTE:
1. Scale 1:4
2. ALL DIMENSIONS AND TOLERANCES TAKE REFERANCE TO JEDEC MO-229
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

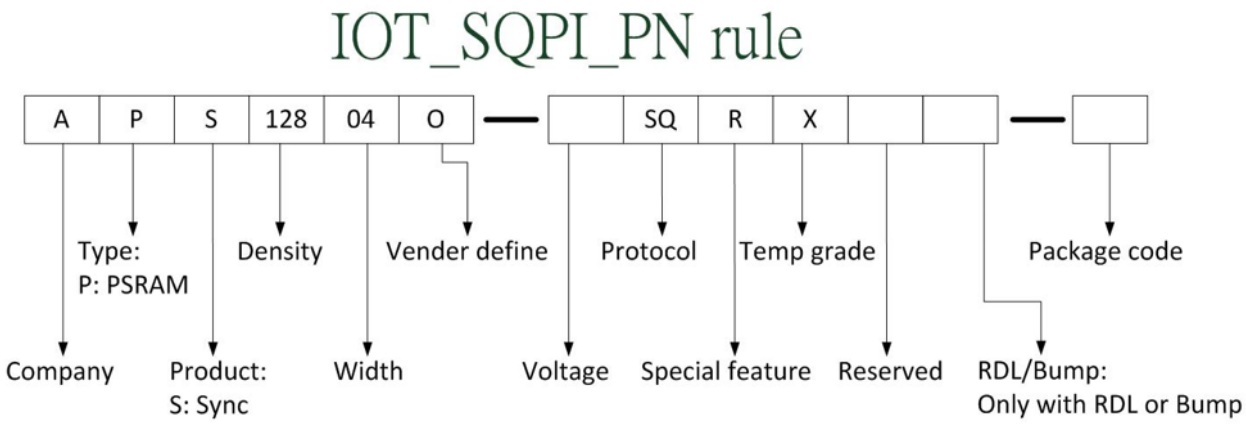
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5 Ordering Information

Table 1: Ordering Information

Part Number	*Temperature Range*	*Max*	*Note*
APS6404L-3SQN	Tj = -40°C to +85°C	133 MHz*	Bare die, SIP
APS6404L-3SQNX	Tj = -40°C to +105°C	133 MHz*	Bare die, SIP
APS6404L-3SQN-ZR	Tc = -40°C to +85°C	133 MHz*	USON-8
APS6404L-3SQN-SN	Tc = -40°C to +85°C	133 MHz*	SOP-8
APS6404L-3SQNX-SN	Tc = -40°C to +105°C	133 MHz*	SOP-8

Note *: 133MHz at VDD=3.0V+/-10%
109MHz at VDD=3.3V+/-10%



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6 Signal Table

All signals are listed in Table 2.

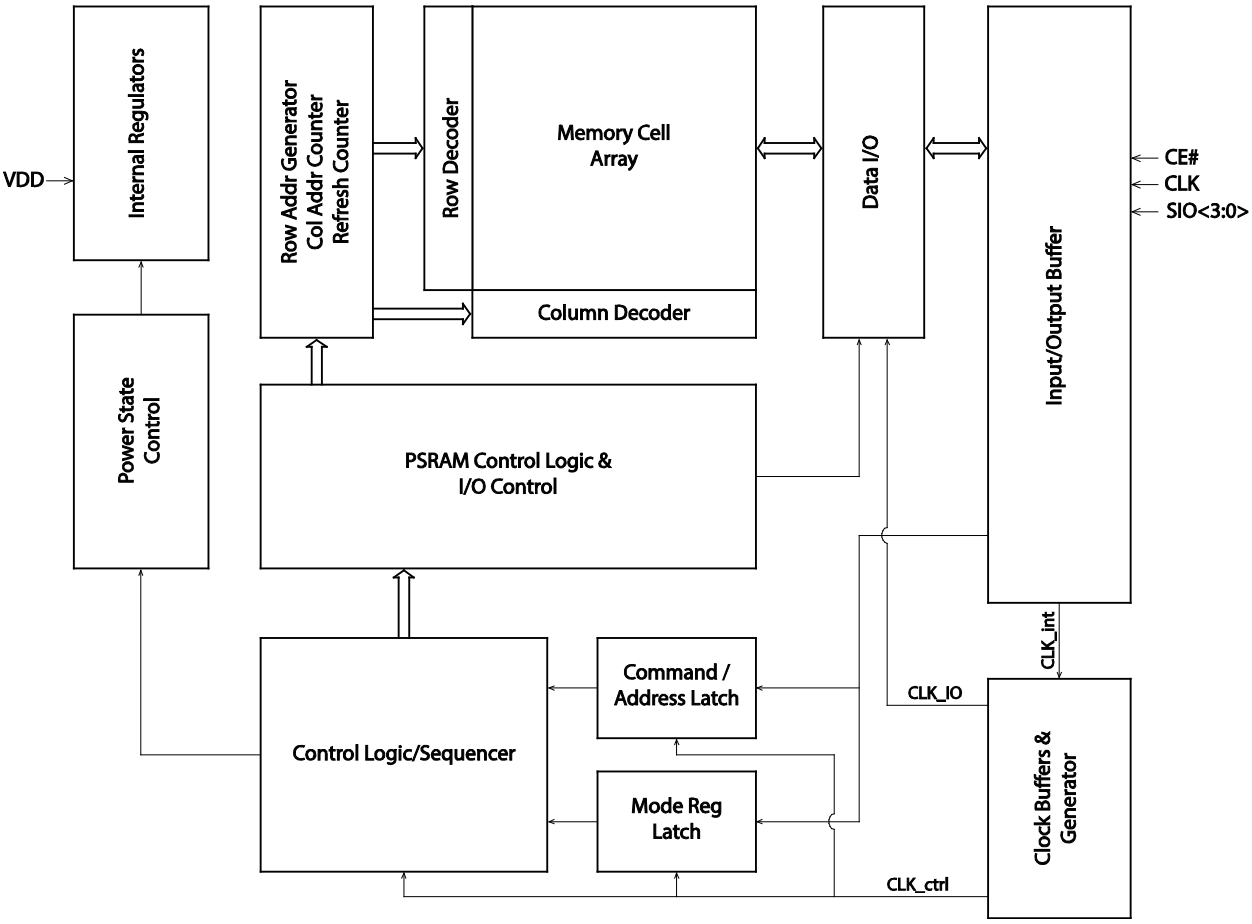
Table 2: Signals Table

Symbol	*Type*	*SPI Mode Function*		*QPI Mode Function*	*Comments*
VDD	Power	Core supply			
VSS	Ground	Core supply ground			
CE#	Input	Chip select, active low. When CE#=1, chip is in standby state			
CLK	Input	Clock Signal			
SI/SIO[0]	IO	Serial Input	IO[0]*	IO[0]	
SO/SIO[1]	IO	Serial Output	IO[1] *	IO[1]	
SIO[2]	IO	--	IO[2] *	IO[2]	
SIO[3]	IO	--	IO[3] *	IO[3]	

Note *: SPI Quad mode

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7 Block Diagram



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8 Power-Up Initialization

SPI/QPI products include an on-chip voltage sensor used to start the self-initialization process. When VDD reaches a stable level at or above minimum VDD, the device will require 150µs and user-issued RESET Operation (see section 14) to complete its self-initialization process. From the beginning of power ramp to the end of the 150µs period, CLK should remain LOW, CE# should remain HIGH (track VDD within 200mV) and SI/SO/SIO[3:0] should remain LOW.

After the Device Reset tRST≧50ns period the device is ready for normal operation.

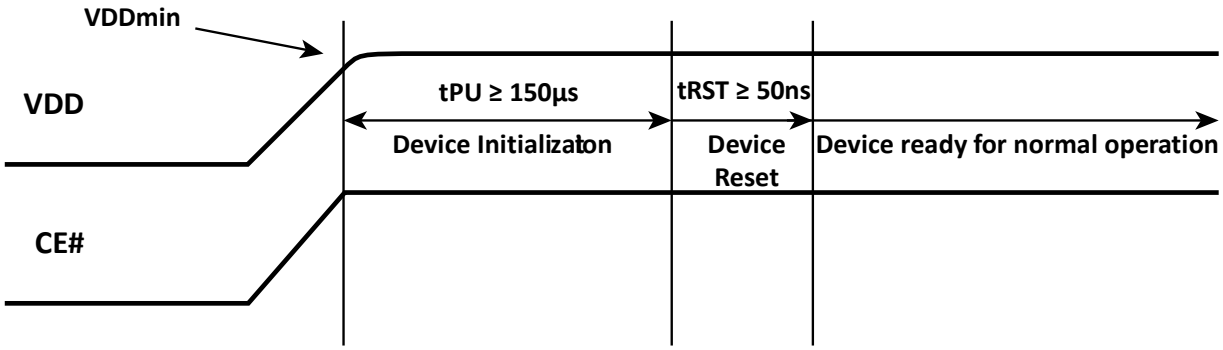


Figure 1. Power-Up Initialization Timing

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9 Interface Description

9.1 Address Space

SPI/QPI PSRAM device is byte-addressable. 64M device is addressed with A[22:0].

9.2 Page Size

Page size is 1K (CA[9:0]). The device operates in a bursting address sequence back to starting address of same page in a wrap manner.

9.3 Drive Strength

The device powers up in 50Ω.

9.4 Power-on Status

The device powers up in SPI Mode. It is required to have CE# high before beginning any operations.

9.5 Command/Address Latching Truth Table

The device recognizes the following commands specified by the various input methods.

		SPI Mode (QE=0)					QPI Mode (QE=1)				
Command	**Code**	**Cmd**	**Addr**	**Wait Cycle**	**DIO**	**Max Freq.**	**Cmd**	**Addr**	**Wait Cycle**	**DIO**	**Max Freq.**
Read	'h03	S	S	0	S	33	N/A				
Fast Read	'h0B	S	S	8	S	133*	Q	Q	4	Q	66
Fast Read Quad	'hEB	S	Q	6	Q	133*	Q	Q	6	Q	133*
Write	'h02	S	S	0	S	133*	Q	Q	0	Q	133*
Quad Write	'h38	S	Q	0	Q	133*	same as 'h02				
Enter Quad Mode	'h35	S	-	-	-	133	N/A				
Exit Quad Mode	'hF5	N/A					Q	-	-	-	133
Reset Enable	'h66	S	-	-	-	133	Q	-	-	-	133
Reset	'h99	S	-	-	-	133	Q	-	-	-	133
Wrap Boundary Toggle	'hC0	S	-	-	-	133	Q	-	-	-	133
Read ID	'h9F	S	S	0	S	33	N/A				
Remark: S = Serial IO, Q = Quad IO											

Note *: ***Max Freq.*** would be 133MHz at VDD=3.0V+/-10% and 109MHz at VDD= 3.3V+/-10%)

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9.6 Command Termination

All Reads & Writes must be completed by raising CE# high immediately afterwards in order to terminate the active command and set the device into standby. Not doing so will block internal refresh operations and cause memory failure.

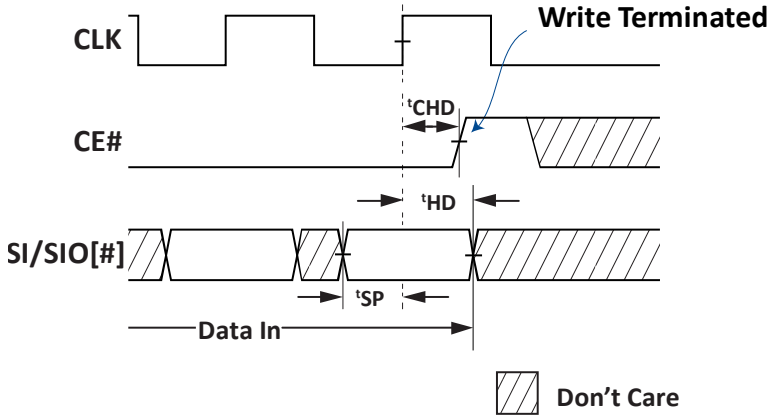


Figure 2: Write Command Termination

For a memory controller to correctly latch the last piece of data prior to read termination, it is recommended to provide a longer CE# hold time (^{t}CHD > ^{t}ACLK+^{t}CLK) for a sufficient data window.

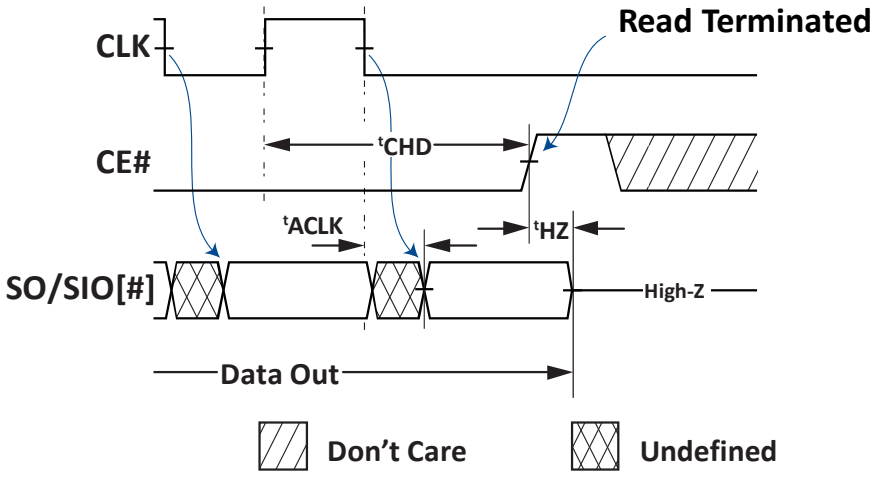


Figure 3: Read Command Termination

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10 Wrap Boundary Toggle Operation

The Wrap Boundary Toggle Operation switches the device's wrapped boundary between 1K Bytes Wrapped Burst or 32 Bytes Wrapped Burst. Note that the default setting is 1K Bytes Wrapped.

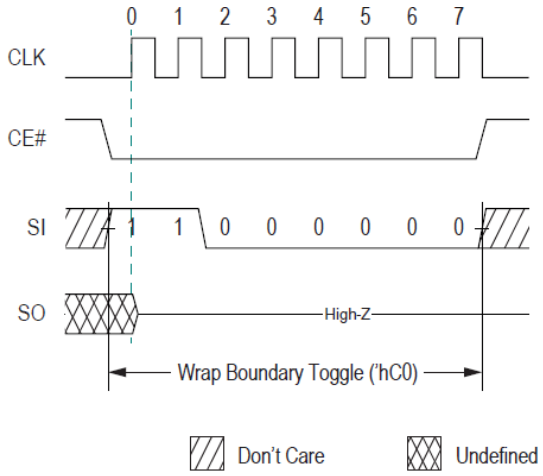


Figure 4: SPI Wrap Boundary Toggle 'hC0

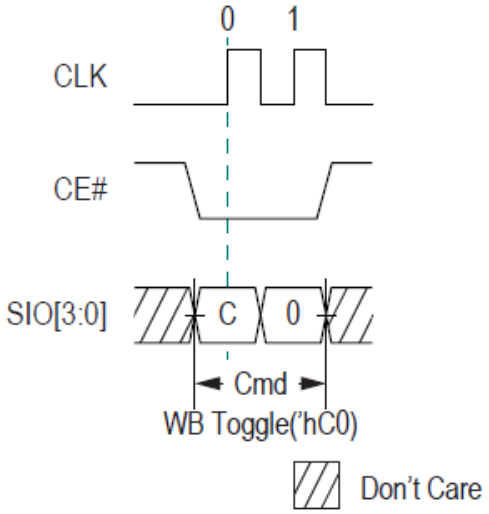


Figure 5: QPI Wrap Boundary Toggle 'hC0

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11 SPI Mode Operations

The device powers up into SPI mode by default but can also be switched into QPI mode.

11.1 SPI Read Operations

For all reads, data will be available ^{t}ACLK after the falling edge of CLK.

SPI Reads can be done in three ways:

1. ‘h03: Serial CMD, Serial Addr/IO, slow frequency.
2. ‘h0B: Serial CMD, Serial Addr/IO, fast frequency.
3. ‘hEB: Serial CMD, Quad Addr/IO, fast frequency.

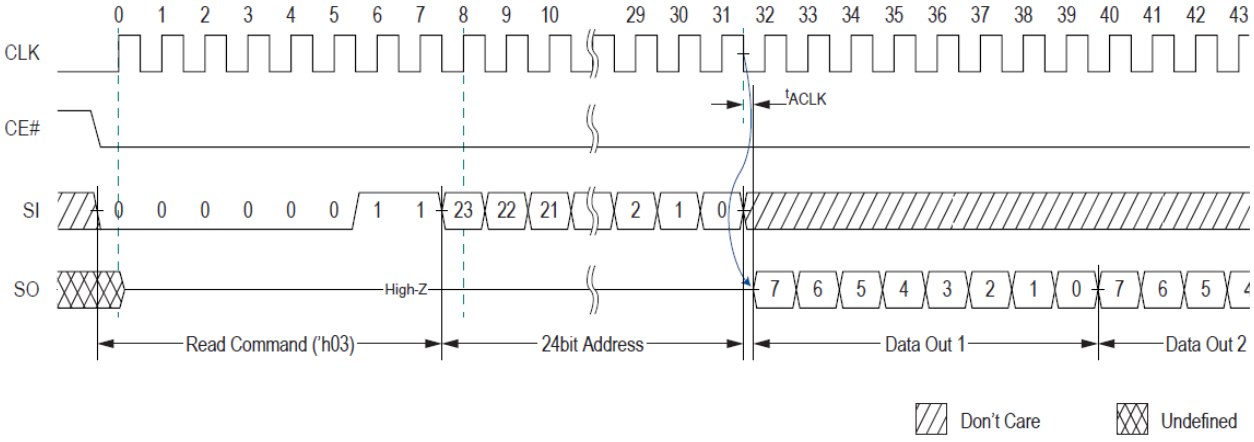


Figure 6: SPI Read ‘h03 (max freq 33MHz)

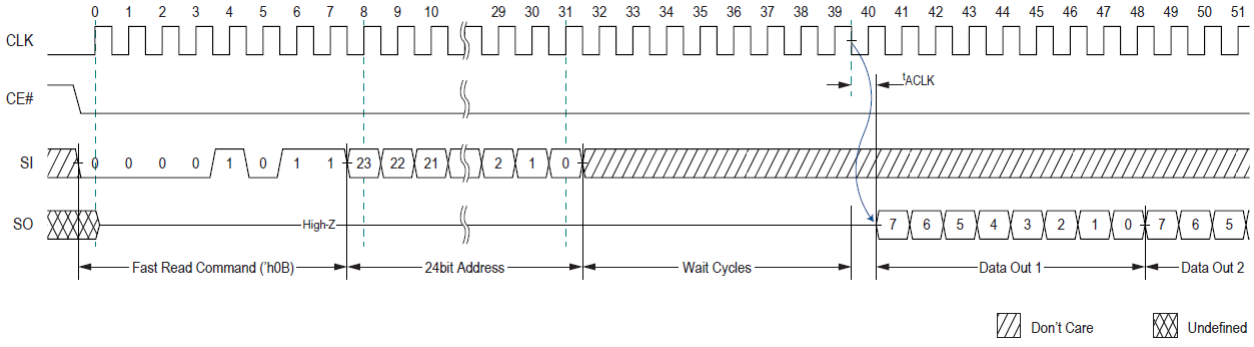


Figure 7: SPI Fast Read ‘h0B (max freq 133 MHz)

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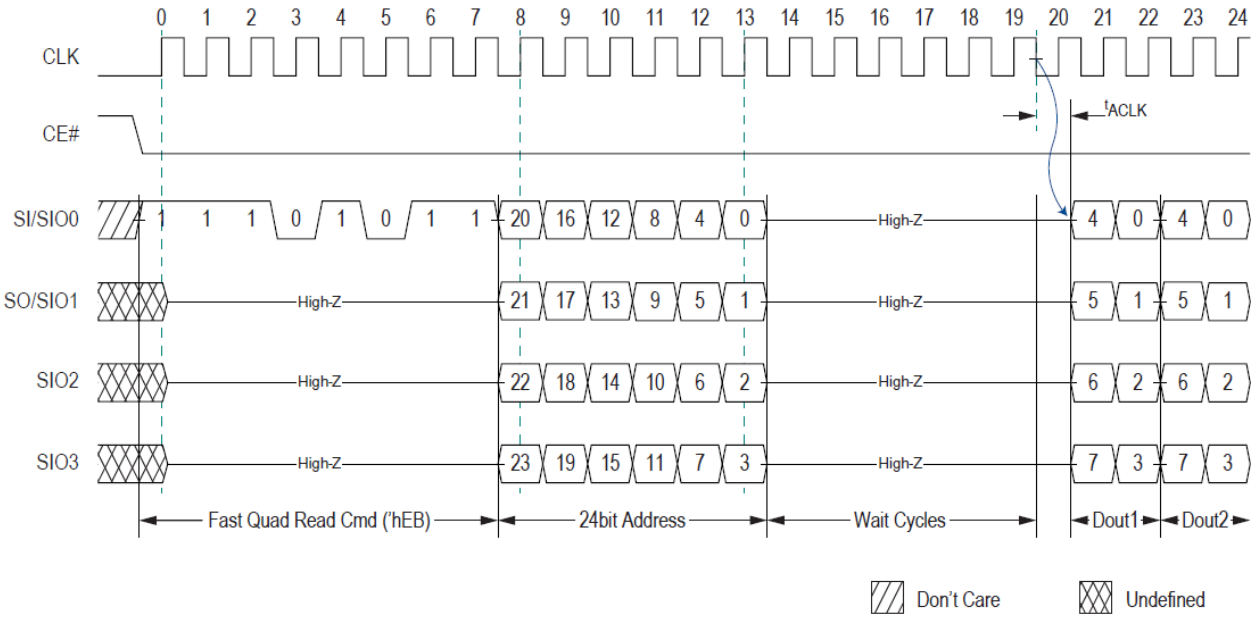


Figure 8: SPI Fast Quad Read 'hEB (max freq 133 MHz)

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11.2 SPI Write Operations

SPI write command can be input as ‘h02 or ‘h38.

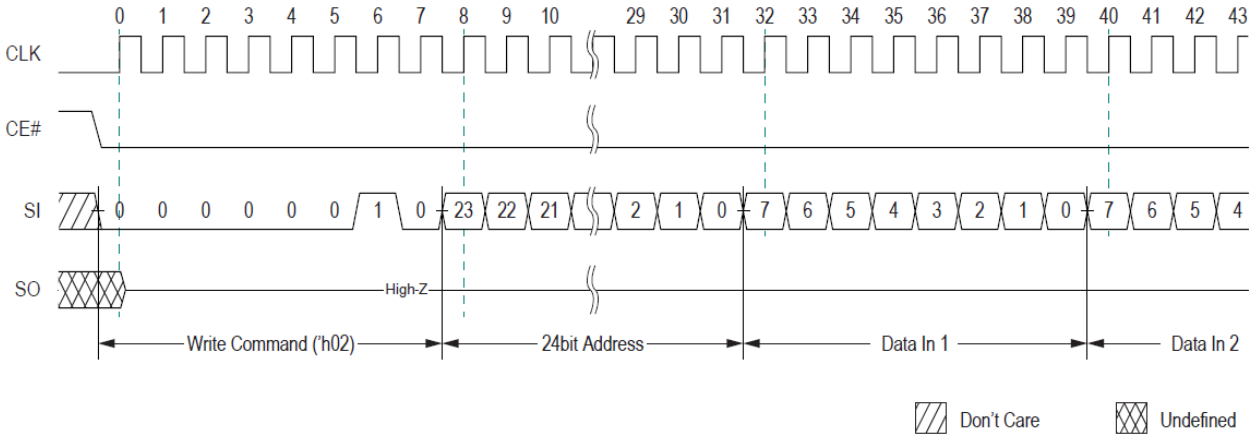


Figure 9: SPI Write ‘h02

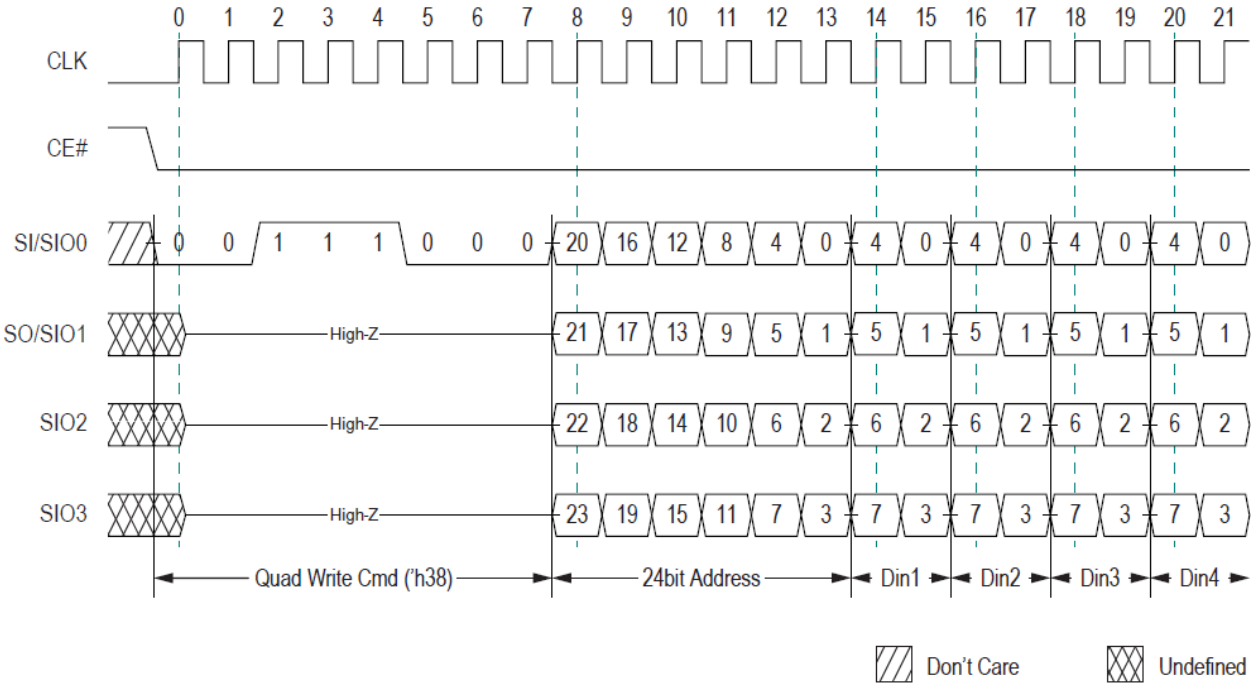


Figure 10: SPI Quad Write ‘h38

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11.3 SPI Quad Mode Enable Operation

This command switches the device into quad IO mode.

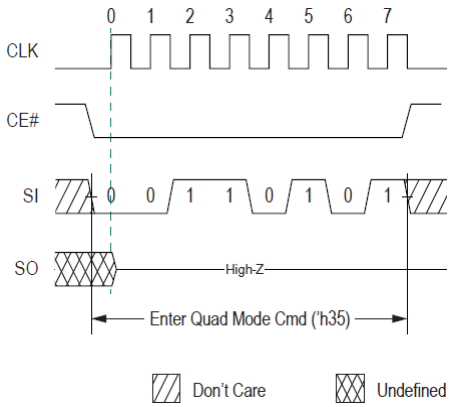


Figure 11: Quad Mode Enable 'h35 (available only in SPI mode)

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12 Read ID

Read ID command provides information of vendor ID, known-good-die, device density, and manufacturing ID. Note that Read ID command can be used ONLY as Power up initialization after the device Reset tRST≧ 50ns right after Global Reset command.



Figure 12: Pre-condition of EID Read

12.1 SPI Read ID Operation

This command is similar to Fast Read, but without the wait cycles and the device outputs EID value instead of data.

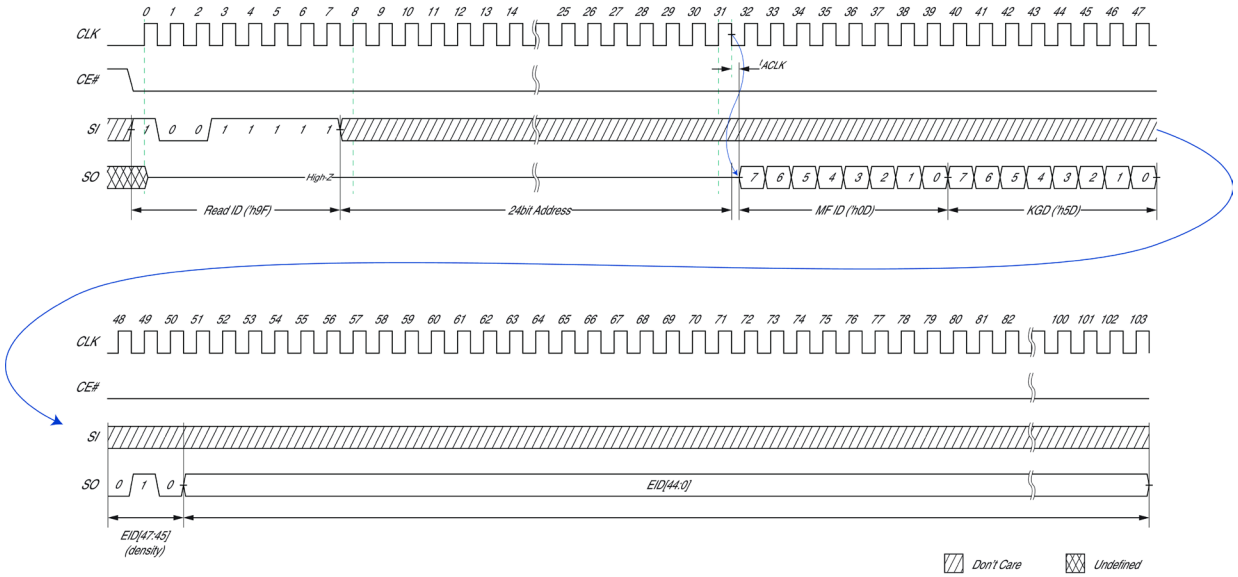


Figure 13: SPI Read ID 'h9F (available only in SPI mode)

Table 3: Known Good Die (KGD)

KGD[7:0]	*Known Good Die*
'b0101_0101	FAIL
'b0101_1101	PASS

*Note: Default is FAIL die, and only mark PASS after all tests passed.

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13 QPI Mode Operations

13.1 QPI Read Operation

For all reads, data will be available ^{t}ACLK after the falling edge of CLK.

QPI Reads can be done in one of two ways:

1. ‘h0B: Quad CMD, Quad Addr/IO, slow frequency
2. ‘hEB: Quad CMD, Quad Addr/IO, fast frequency

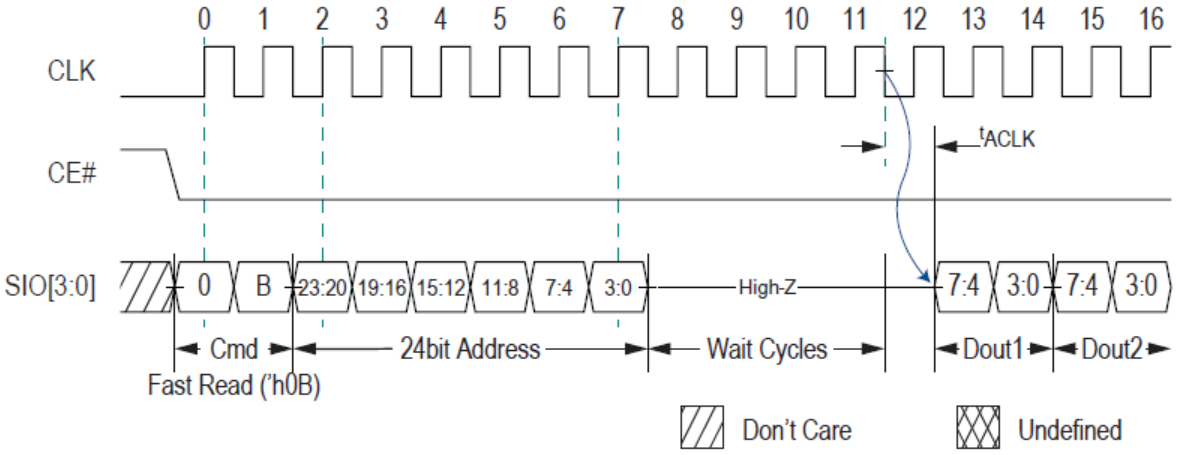


Figure 14: QPI Fast Read ‘h0B (max freq 66 MHz)

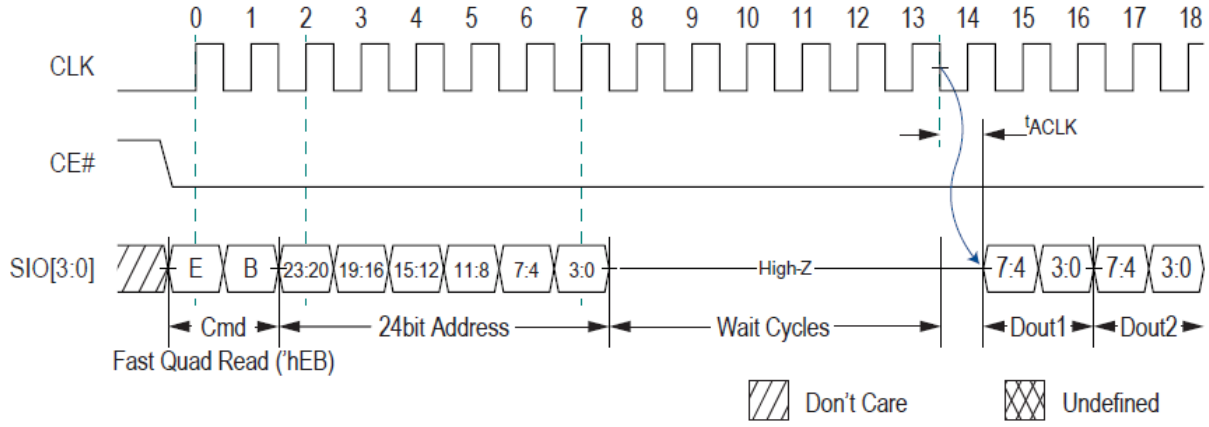


Figure 15: QPI Fast Quad Read ‘hEB (max freq 133 MHz)

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13.2 QPI Write Operation(s)

QPI write command can be input as ‘h02 or ‘h38.

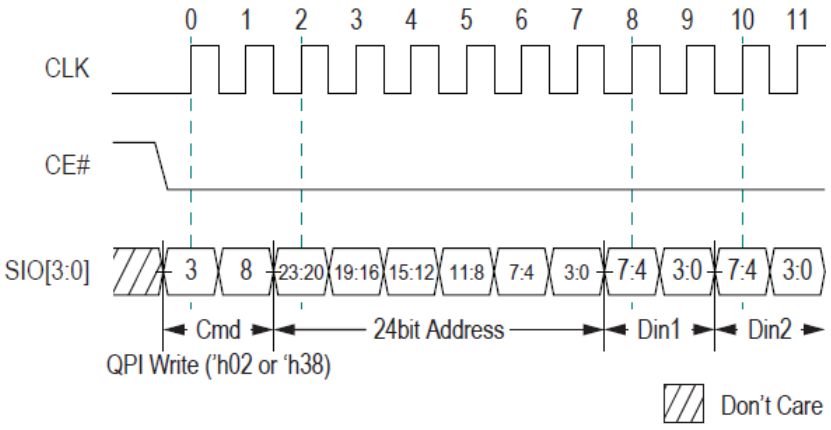


Figure 16: QPI Write ‘h02 or ‘h38

13.3 QPI Quad Mode Exit operation

This command will switch the device back into serial IO mode.

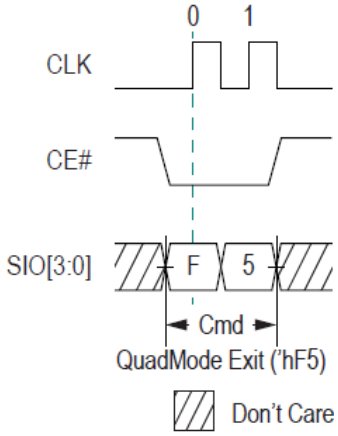


Figure 17: Quad Mode Exit ‘hF5 (only available in QPI mode)

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14 Reset Operation

The Reset operation is used as a system (software) reset that puts the device in SPI standby mode which is also the default mode after power-up. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST).

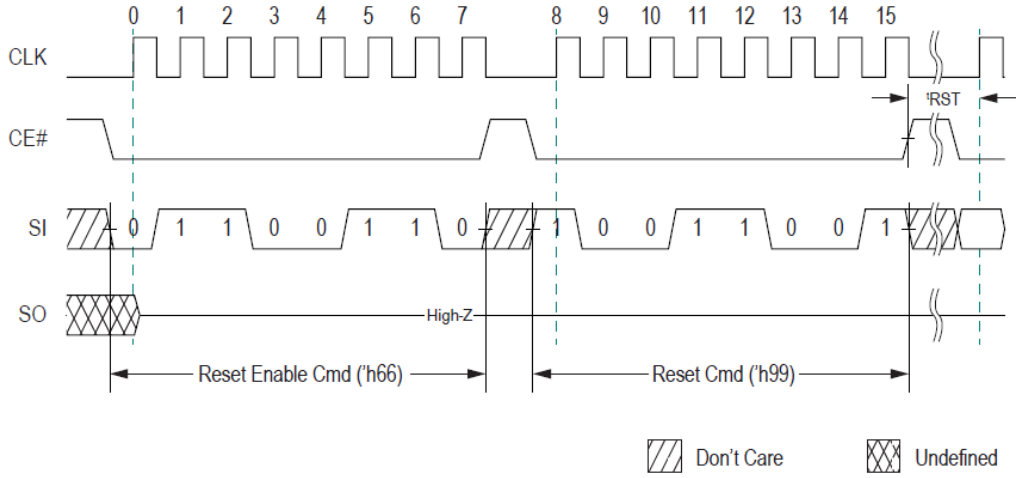


Figure 18: SPI Reset

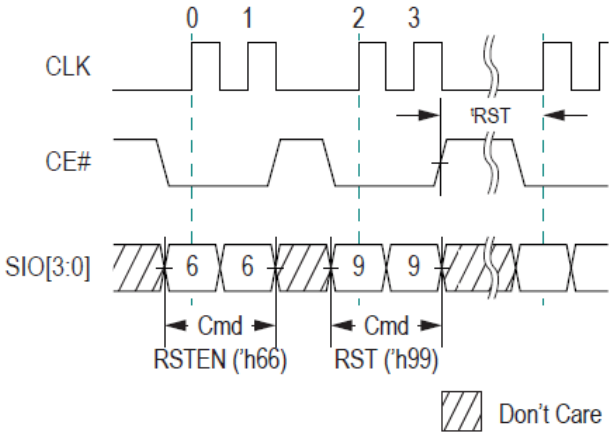


Figure 19: QPI Reset

Reset command has to immediately follow the Reset-Enable command in order for the reset operation to take effect. Any command other than the Reset command after the Reset-Enable command will cause the device to exit Reset-Enable state and abandon reset operation.

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15 Input/Output Timing

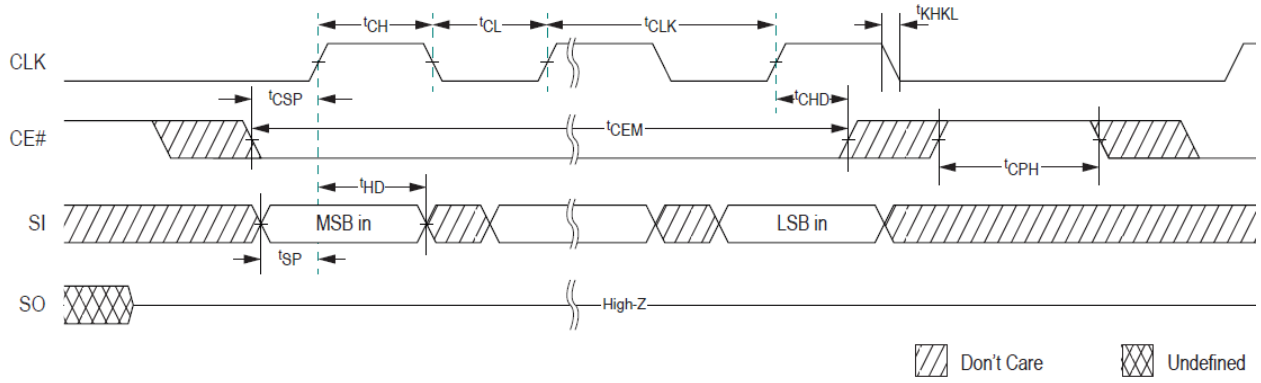


Figure 20: Input Timing

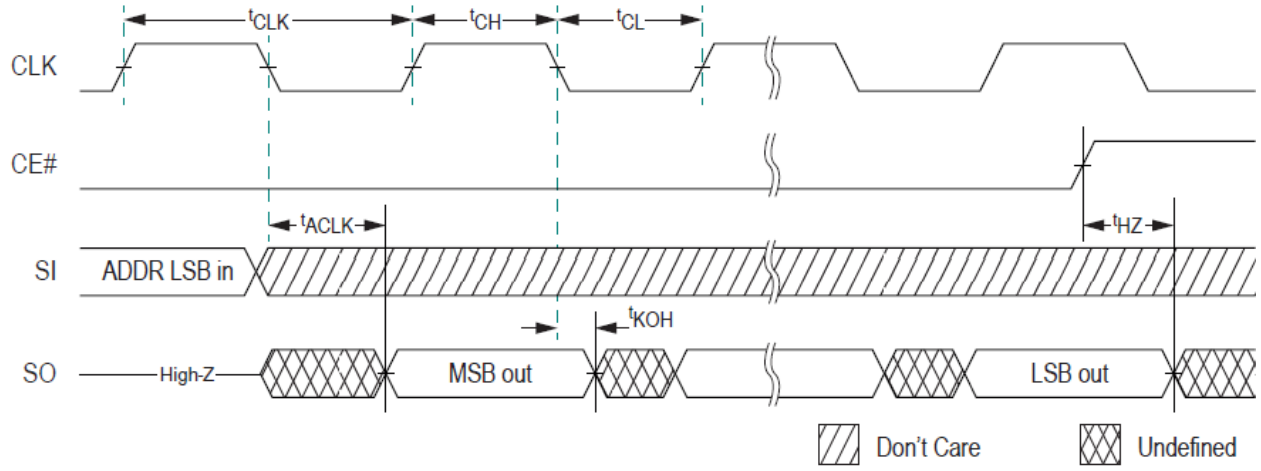


Figure 21: Output Timing

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16 Electrical Specifications:

16.1 Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings

Parameter	*Symbol*	*Rating*	*Unit*	*Notes*
Voltage to any ball except V_{DD} relative to V_{SS}	VT	-0.4 to V_{DD}+0.4	V	
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.4 to +4.0	V	2
Storage Temperature	T_{STG}	-55 to +150	℃	1

Notes 1: Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

Notes 2: During voltage transitions, all pins may overshoot to -0.5V or VCC+0.5V for period up to 20ns.

Caution:

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

16.2 Input Signal Overshoot

During DC conditions, input or I/O signals should remain equal to or between VSS and VDD. During voltage transitions, inputs or I/Os may negative overshoot VSS to -1.0V or positive overshoot to VDD +1.0V, for periods up to 20 ns.

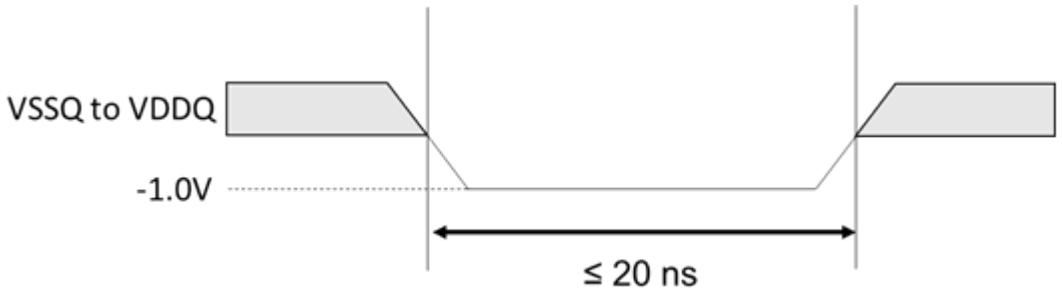


Figure 12 Maximum Negative Overshoot Waveform

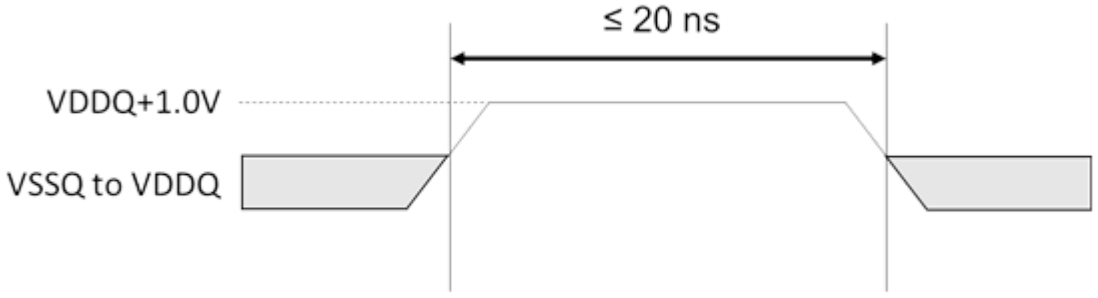


Figure 13 Maximum Positive Overshoot Waveform

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Table 5: Bare Die Pin Capacitance

Parameter	*Symbol*	*Min*	*Max*	*Unit*	*Notes*
Input Pin Capacitance	CIN		2	pF	VIN=0V
Output Pin Capacitance	COUT		3	pF	VOUT=0V

Note: spec'd at 25°C.

Table 6: Package Pin Capacitance

Parameter	*Symbol*	*Min*	*Max*	*Unit*	*Notes*
Input Pin Capacitance	CIN		6	pF	VIN=0V
Output Pin Capacitance	COUT		8	pF	VOUT=0V

Note: spec'd at 25°C.

Table 7: Load Capacitance

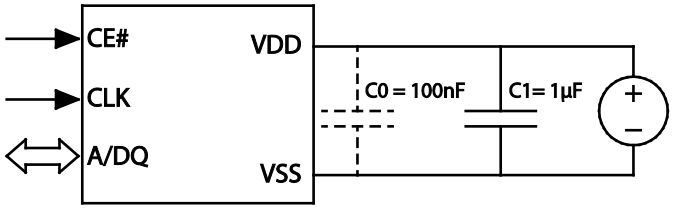
Parameter	*Symbol*	*Min*	*Max*	*Unit*	*Notes*
Load Capacitance	C_L		15	pF	

Note: System C_L for the use of package

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16.4 Decoupling Capacitor Requirement

It is required to have a decoupling capacitor on VDD pin for IO switchings and psram internal transient events. A low ESR 1µF ceramic cap is recommended. To minimize parasitic inductance, place the cap as close to VDD pin as possible. An optional 0.1µF can further improve high frequency transient response.



16.5 Operating Conditions

Table 8: Operating Characteristics

Parameter	*Min*	*Max*	*Unit*	*Notes*
Operating Temperature (extended)	-40	105	°C	
Operating Temperature (standard)	-40	85	°C	

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16.6 DC Characteristics

Table 9: DC Characteristics

Symbol	*Parameter*	*Min*	*Max*	*Unit*	*Notes*
V_{DD}	Supply Voltage	2.7	3.6	V	
V_{IH}	Input high voltage	V_{DD}-0.4	V_{DD}+0.2	V	
V_{IL}	Input low voltage	-0.2	0.4	V	
V_{OH}	Output high voltage (I_{OH}=-0.2mA)	0.8 V_{DD}		V	
V_{OL}	Output low voltage (I_{OL}=+0.2mA)		0.2 V_{DD}	V	
I_{LI}	Input leakage current		1	µA	
I_{LO}	Output leakage current		1	µA	
I_{CC}	Read/Write		7	mA	1,2
ISB_{EXT}	Standby current (105C)		350	µA	3
ISB_{STD}	Standby current (85C)		250	µA	3

Note 1: Output load current not included.

2. 50% bus toggling rate.

3. Standby current is measured when CLK is in DC low state.

4. Typical $ISB_{STDroom}$ 100uA

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16.7 AC Characteristics

Table 5: READ/WRITE Timing

Symbol	*Parameter*	*Min*	*Max*	*Unit*	*Notes*
^{t}CLK	CLK period - SPI Read (‘h03)	30.3		ns	33MHz
	CLK period - QPI Read (‘h0B)	15.1			66MHz
	CLK period - all other operations PKG 3V	7.5			133MHz*1,2,3
	CLK period - all other operations PKG 3.3V	9.17			109MHz*2,3
^{t}CH/^{t}CL	Clock high/low width	0.45	0.55	^{t}CLK(min)	
^{t}KHKL	CLK rise or fall time		1.5	ns	4
^{t}CPH	CE# HIGH between subsequent burst operations	18		ns	
^{t}CEM	CE# low pulse width		3	µs	Extended grade
			8		Standard grade
^{t}CSP	CE# setup time to CLK rising edge PKG	2.5		ns	
^{t}CHD	CE# hold time from CLK rising edge PKG	3.0		ns	2
^{t}SP	Setup time to active CLK edge	2		ns	
^{t}HD	Hold time from active CLK edge	2		ns	
^{t}HZ	Chip disable to DQ output high-Z		5.5	ns	
^{t}ACLK	CLK to output delay	2	5.5	ns	
^{t}KOH	Data hold time from clock falling edge	1.5		ns	
^{t}RST	Time between end of RST CMD to next valid CMD	50		ns	

Note 1: Frequency limits are therefore
133MHz (PKG VDD= 3.0V+-10%), 109MHz (PKG VDD= 3.3V+-10%) max for Wrap 32 Bytes.

2: System max C_L 15pF for the use of package.

3: For operating frequencies >84MHz, it is highly recommended to utilize CLK falling edge to sample read data or align sampling clock via data pattern tuning (refer to JEDEC JESD84-B50 for an example).

4: Measured from 20% to 80% of VDD

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17 Change Log

Version		Date	Description
1.0		Jul 13, 2017	Initial Version
1.1		Jul 25, 2017	Revised package code and ordering information
1.2		Aug 24, 2017	Corrected package code; Added system max C_L for the use of package & related tCK and tCHD
1.3		Sep 04, 2017	Added ISBstdroom
1.5		Oct 30, 2017	Enabled QPI Read 'h0B support; changed Min/Max absolute voltage, Vil_min and Vih_max,; defined tCEM for different temperature grade; corrected speed typo. Added USON package ZR
1.6		Nov 13, 2017	Modified spec of ICC & ISB
1.7		Mar 19, 2018	Revised part# of RBX. Temperature -40C
1.8		Jan 07, 2019	Remove WSON and updated POD of USON, add tRST
1.9		Sep 06, 2019	Updated Figure 10, Table 7 and Table 9; added table for Change Log; updated section 9.5 and 16.6; added section 16.3
2.0a		Oct 02, 2019	Updated header, page 1 and Table 1
2.1		Oct 25, 2019	Revised the typo in Page 15, 20 and Table 5; Updated Figure 18 and Figure 19; add section 10
2.2		Nov 21, 2019	Update Table 2, Figure 10 and Figure
2.3		Apr 30, 2020	Modify VDD's description of Table 2
2.4		Oct 12, 2021	Revised tCEM value from 4us to 3us @105C
2.5	Kim/ Gene/ Eric	Jun 17, 2022	Typos correct
2.6	Kim	Oct 28, 2022	Release USON temp. from -25~85 to -40~85
2.7	Kim	Jan 05, 2024	Add chapter 16.2 Input signal overshoot.

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