# SPI/QPI PSRAM

## Specifications

- **Single Supply Voltage**
  - $V_{DD}$=2.7 to 3.6 V
- **Interface**: SPI/QPI with SDR mode
- **Performance**: Clock rate up to
  - 133MHz for Wrapped Burst operation at VDD=3.0V+/-10%
  - 109MHz for Wrapped Burst operation at VDD=3.3V+/-10%
  - 84MHz for Linear 512 Burst operation
- **Organization**: 16Mb, 2M x 8bits
- **Addressable Bit Range**: A[20:0]
- **Page Size**: 512 bytes
- **Refresh**: Self-managed
- **Operating Temperature Range**
  - $T_{OPER}$= -40°C to +85°C (standard range)
  - $T_{OPER}$= -40°C to +105°C (extended range)
- **Maximum Standby Current**:
  - 200µA @ 105°C
  - 150µA @ 85°C
- **Typical Standby Current**
  - 35µA @ 25°C

## Features

- **Output Driver LVCMOS** with programmable drive strengths of 50, 100 and 200Ω
- **Dedicated Wrapped Burst** read and write commands
- **Linear 512 Length Burst** is supported up to 84MHz and can cross page boundary as long as tCEM is met
- **Register Configurable Wrap Lengths** of 16, 32, 64 and 512
- **Burst Length Toggle Command** to switch between configurable wrap length and 32 bytes wrap
- **Software Reset**

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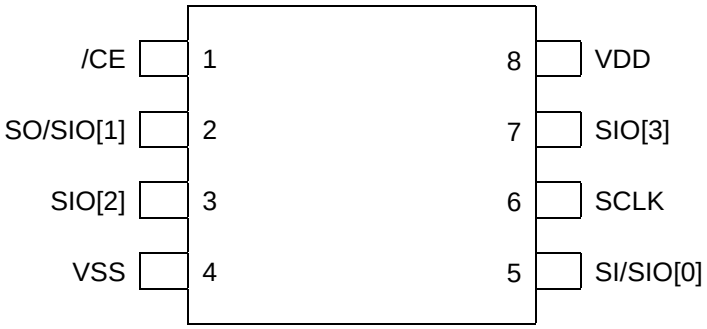
# 2 Introduction

This Pseudo-SRAM device features a high speed, low pin count interface. It has 4 I/O pins and operates in SPI(serial peripheral interface) or QPI (quad peripheral interface) mode with frequencies up to 133 MHz. The data input (A/DQ) to the memory relies on clock (CLK) to latch all instructions, addresses and data. It is most suitable for low-power and low cost portable applications. It incorporates a seamless self-managed refresh mechanism. Hence it does not require the support of DRAM refresh from system host. The self-refresh feature is a special design to maximize performance of memory read operation.

# 3 Package Information

The APS1604M-3SQR is available in standard package including 8-lead SOP-8L(150) and advanced package including 8-lead USON-8L 3x2mm.

## *3.1 Package Types : SOP / USON (SN, ZR) , not to scale, Top view*

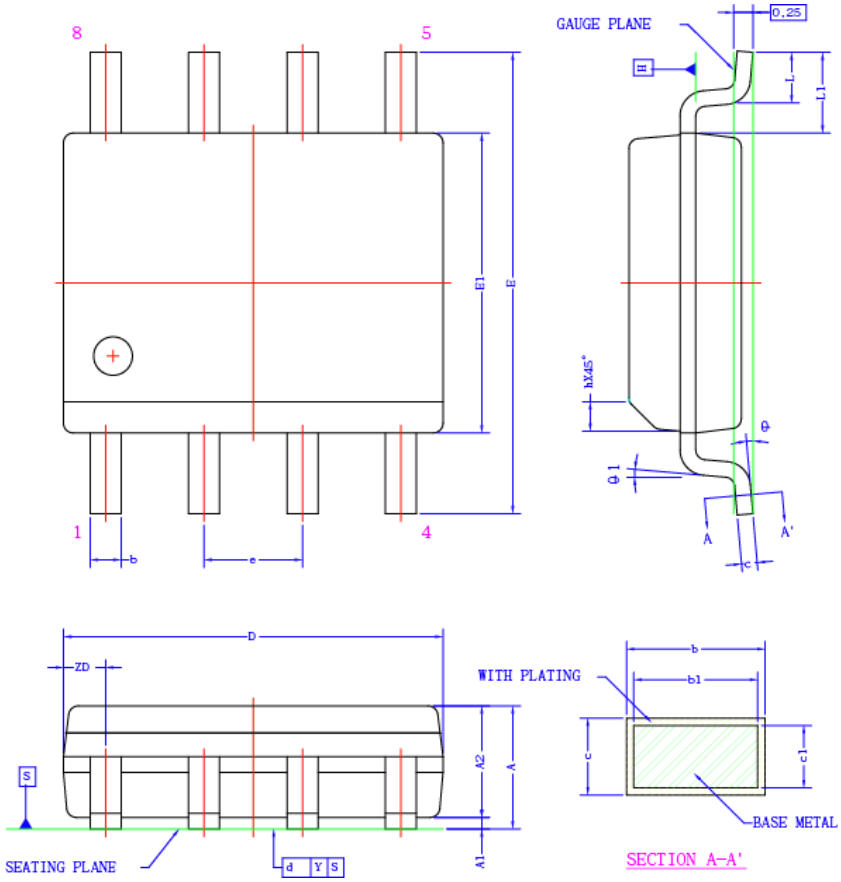




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# 4 Package Outline Drawing

## *4.1 SOP-8L(150), package code SN*



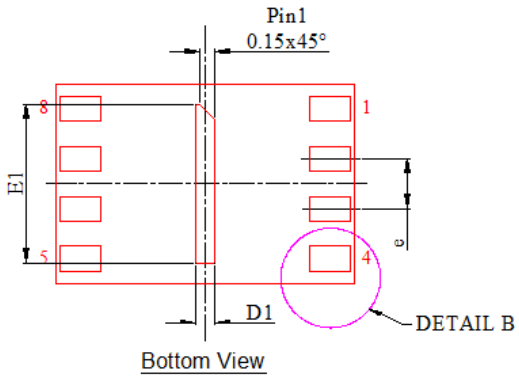

| SYMBOL | DIMENSION (MM) | | | DIMENSION (MIL) | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 1.35 | 1.60 | 1.75 | 53 | 63 | 69 |
| A1 | 0.10 | 0.15 | 0.25 | 4 | 6 | 10 |
| A2 | 1.35 | 1.45 | 1.55 | 53 | 57 | 61 |
| b | 0.31 | – | 0.51 | 12 | – | 20 |
| b1 | 0.28 | 0.40 | 0.48 | 11 | 16 | 19 |
| c | 0.17 | – | 0.25 | 7 | – | 10 |
| c1 | 0.17 | 0.20 | 0.23 | 7 | 8 | 9 |
| D | 4.80 | 4.90 | 5.00 | 189 | 193 | 197 |
| E | 6.00 BSC | | | 236 BSC | | |
| E1 | 3.80 | 3.90 | 4.00 | 150 | 154 | 157 |
| e | 1.27 BSC | | | 50 BSC | | |
| L | 0.40 | 0.66 | 1.27 | 16 | 26 | 50 |
| L1 | 1.05 REF | | | 41 REF | | |
| ZD | 0.55 REF | | | 22 REF | | |
| h | 0.25 | 0.38 | 0.50 | 10 | 15 | 20 |
| Y | – | – | 0.10 | – | – | 4 |
| θ | 0° | – | 8° | 0° | – | 8° |
| θ1 | 0° | – | – | 0° | – | – |

NOTE :

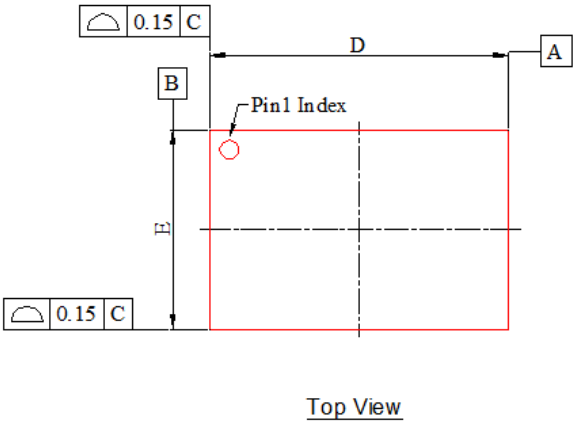
1. REFER TO JEDEC STD: MS-012 AA.
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION AND GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
   DIMENSION "E1" DOES NOT INCLUDE INTERLEAD MOLD FLASH OR PROTRUSION. INTERLEAD MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
   'D' AND 'E1' DIMENSIONS ARE DETERMIND AT DATUM H .
3. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.


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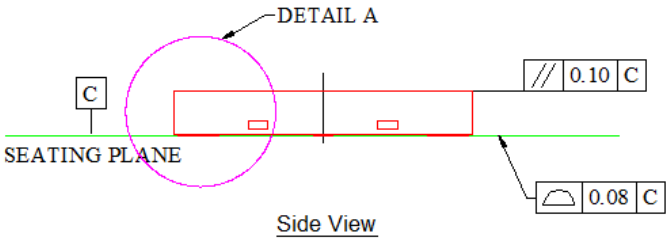
## 4.2 USON-8L 3x2mm, package code ZR



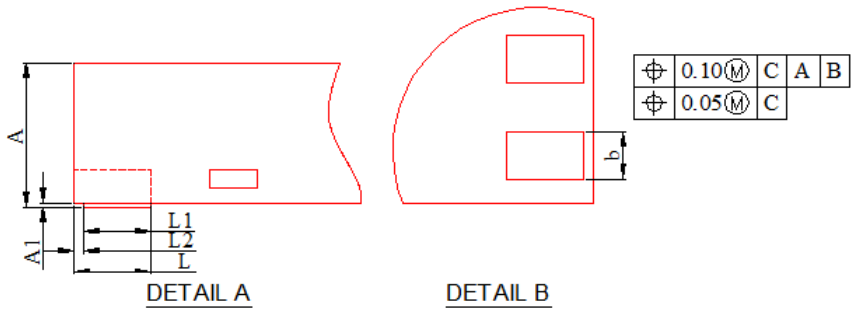

Bottom View




Top View




Side View




DETAIL A DETAIL B

| Symbol | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.40 | 0.45 | 0.50 |
| A1 | 0.00 | --- | 0.05 |
| D | 2.90 | 3.00 | 3.10 |
| D1 | 0.10 | 0.20 | 0.30 |
| E | 1.90 | 2.00 | 2.10 |
| E1 | 1.50 | 1.60 | 1.70 |
| L | 0.40 | 0.45 | 0.50 |
| L1 | 0.30 | --- | --- |
| L2 | --- | --- | 0.15 |
| b | 0.20 | 0.25 | 0.30 |
| e | 0.50 BSC | | |

NOTE:
1. Scale 1:4
2. ALL DIMENSIONS AND TOLERANCES TAKE REFERANCE TO JEDEC MO-229
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

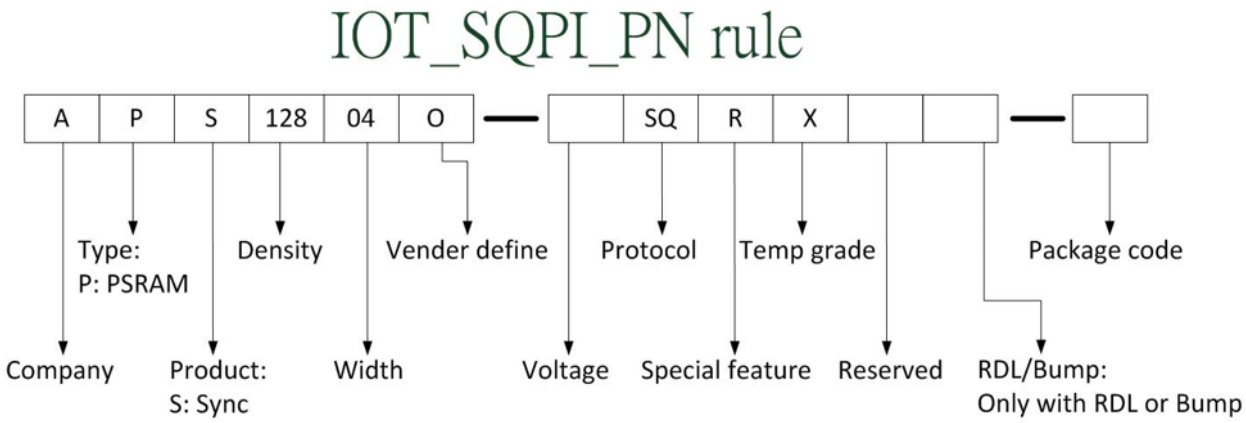

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# 5 Ordering Information

**Table 1: Ordering Information**

| *Part Number* | *Temperature Range* | *Max Frequency* | *Note* |
|---|---|---|---|
| APS1604M-3SQR | Tj = -40°C to +85°C | 133 MHz* | Bare die, SIP |
| APS1604M-3SQRX | Tj = -40°C to +105°C | 133 MHz* | Bare die, SIP |
| APS1604M-3SQR-ZR | Tc=-40°C to +85°C | 133 MHz* | USON-8 |
| APS1604M-3SQR-SN | Tc=-40°C to +85°C | 133 MHz* | SOP-8 |
| APS1604M-3SQRX-SN | Tc=-40°C to +105°C | 133 MHz* | SOP-8 |

Note *: 133MHz for Wrapped Burst operation at VDD=3.0V+/-10%
109MHz for Wrapped Burst operation at VDD=3.3V+/-10%
84MHz for Linear 512 Burst operation with RBX (row boundary crossing)





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# 6 Signal Table

All signals are listed in Table 2.

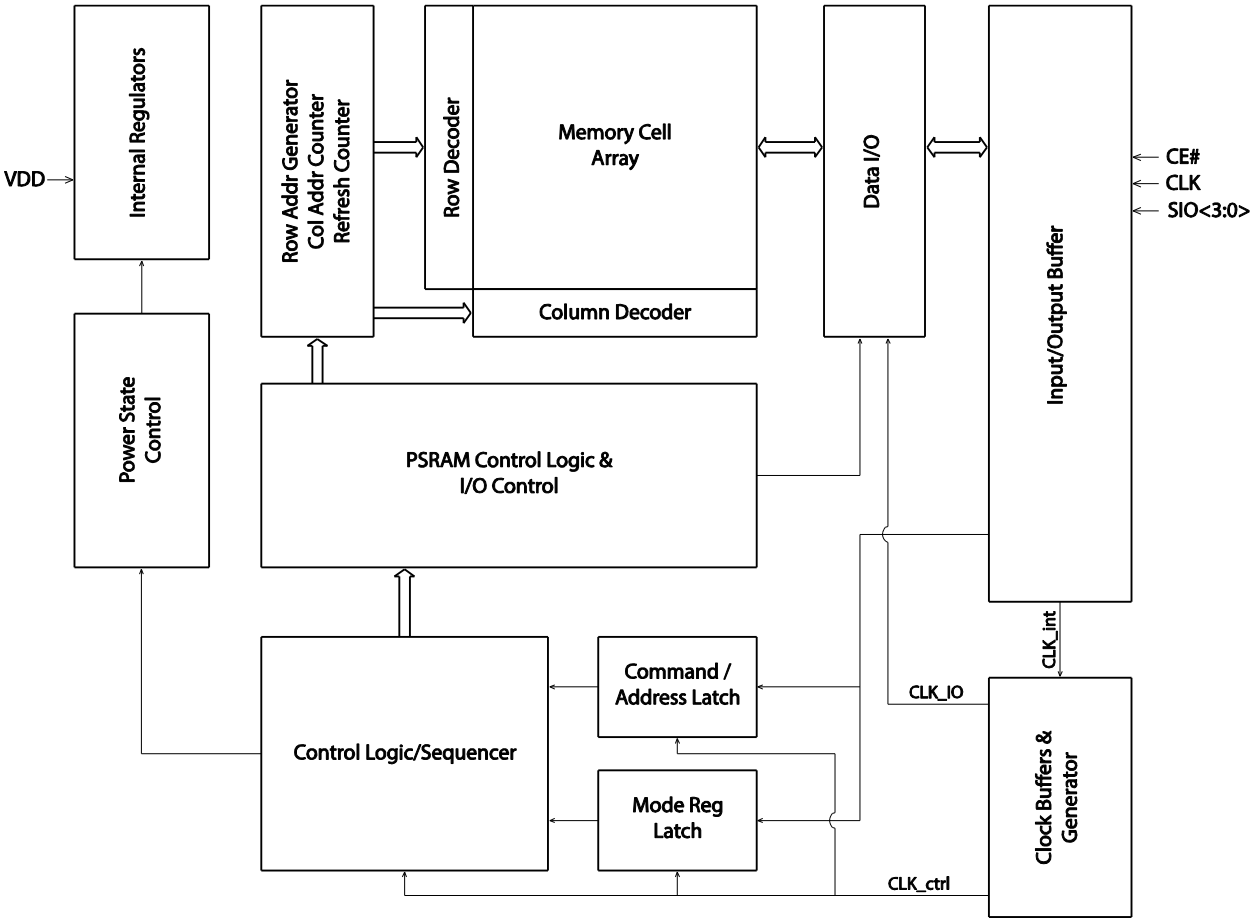
**Table 2: Signals Table**

| *Symbol* | *Type* | *SPI Mode Function* | | *QPI Mode Function* | *Comments* |
|---|---|---|---|---|---|
| VDD | Power | Core supply | | | |
| VSS | Ground | Core supply ground | | | |
| CE# | Input | Chip select, active low. When CE#=1, chip is in standby state | | | |
| CLK | Input | Clock Signal | | | |
| SI/SIO[0] | IO | Serial Input | IO[0]* | IO[0] | |
| SO/SIO[1] | IO | Serial Output | IO[1] * | IO[1] | |
| SIO[2] | IO | -- | IO[2] * | IO[2] | |
| SIO[3] | IO | -- | IO[3] * | IO[3] | |

Note *: SPI Quad mode


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# 7 Block Diagram





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# 8 Power-Up Initialization

SPI/QPI products include an on-chip voltage sensor used to start the self-initialization process. When VDD reaches a stable level at or above minimum VDD, the device will require 150µs and user-issued RESET Operation (see section 17) to complete its self-initialization process. From the beginning of power ramp to the end of the 150µs period, CLK should remain LOW, CE# should remain HIGH (track VDD within 200mV) and SI/SO/SIO[3:0] should remain LOW.

After the Device Reset tRST≧50ns period the device is ready for normal operation.

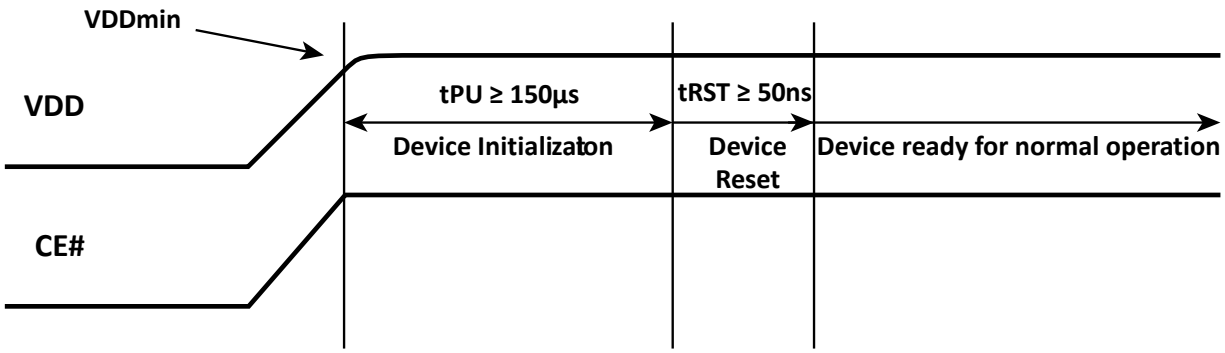



**Figure 1. Power-Up Initialization Timing**


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# 9 Interface Description

## 9.1 Address Space

SPI/QPI PSRAM device is byte-addressable. 16M device is addressed with A[20:0].

## 9.2 Page Length

Read and write operations are default page size of 512 bytes.

## 9.3 Drive Strength

The device powers up in 50Ω.

## 9.4 Power-on Status

The device powers up in SPI Mode. It is required to have CE# high before beginning any operations.


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# 10 Mode Register Definition

**Table 3: Mode Register Table**

| MR No. | MA[3:0] | Access | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | `h0 | R/W | rsvd. | Wrap | | rsvd. | | | DQ Zout | |

**Table 4: Wrap Codes MR0[6:5]**

| Wrap Burst Settings | | Page Boundary Crossing | |
|---|---|---|---|
| MR0[6:5] | Wrapped Length | Non-Wrap CMDs ('h03,'h0B,`hEB,'h02,'h38) | Wrap CMDs('h8B,'h82) |
| 00 | 16 | Wrap 16, no cross page boundary | |
| 01 | 32 | Wrap 32, no cross page boundary | |
| 10 | 64 | Wrap 64, no cross page boundary | |
| 11 (default) | 512 (page size) | Linear, can cross page boundary | Wrap 512, no cross page boundary |

**Table 5: DQ Output Drive Strength Codes MR0[1:0]**

| DQ Output Drive Strength | |
|---|---|
| MR0[1:0] | Impedance |
| 00 (default) | 50Ω |
| 01 | 100Ω |
| 10 | 200Ω |
| Others | reserved |


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## 11 Command/Address Latching Truth Table

The device recognizes the following commands specified by the various input methods.

| | | SPI Mode (QE=0) | | | | | QPI Mode (QE=1) | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Command** | **Code** | **Cmd** | **Addr** | **Wait Cycle** | **DIO** | **Max Freq.** | **Cmd** | **Addr** | **Wait Cycle** | **DIO** | **DIO** | **Max Freq.** |
| Read | 'h03 | S | S | 0 | S | 33 | N/A | | | | | |
| Fast Read | 'h0B | S | S | 8 | S | 133/84* | Q | Q | 4 | Q | Q | 66 |
| Fast Read Quad | 'hEB | S | Q | 6 | Q | 133/84* | Q | Q | 6 | Q | Q | 133/84* |
| Write | 'h02 | S | S | 0 | S | 133/84* | Q | Q | 0 | Q | Q | 133/84* |
| Quad Write | 'h38 | S | Q | 0 | Q | 133/84* | same as 'h02 | | | | | |
| Wrapped Read | h8B | S | S | 8 | S | 133 | Q | Q | 6 | Q | Q | 133 |
| Wrapped Write | h82 | S | S | 0 | S | 133 | Q | Q | 0 | Q | Q | 133 |
| Mode Register Read | hB5 | S | S | 8 | S | 133 | Q | Q | 6 | Q | Q | 133 |
| Mode Register Write | hB1 | S | S | 0 | S | 133 | Q | Q | 0 | Q | Q | 133 |
| Enter Quad Mode | 'h35 | S | - | - | - | 133 | N/A | | | | | |
| Exit Quad Mode | 'hF5 | N/A | | | | | Q | - | - | - | - | 133 |
| Reset Enable | 'h66 | S | - | - | - | 133 | Q | - | - | - | - | 133 |
| Reset | 'h99 | S | - | - | - | 133 | Q | - | - | - | - | 133 |
| Burst Length Toggle | 'hC0 | S | - | - | - | 133 | Q | - | - | - | - | 133 |
| Read ID | 'h9F | S | S | 0 | S | 33 | N/A | | | | | |

Remark: S = Serial IO, Q = Quad IO


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## 11.1 Command Termination

All Reads & Writes must be completed by raising CE# high immediately afterwards in order to terminate the active command and set the device into standby. Not doing so will block internal refresh operations and cause memory failure.

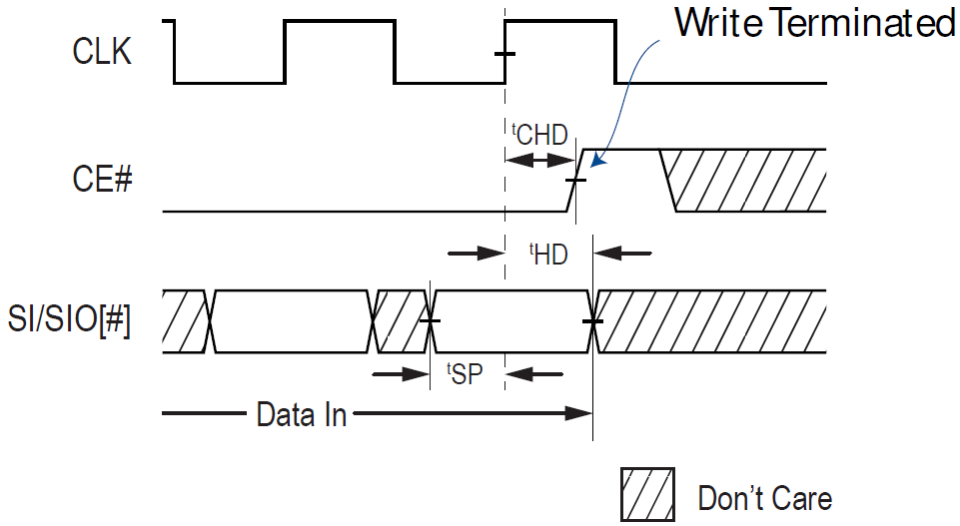



**Figure 2: Write Command Termination**

For a memory controller to correctly latch the last piece of data prior to read termination, it is recommended to provide a longer CE# hold time ($^{t}$CHD > $^{t}$ACLK+$^{t}$CLK) for a sufficient data window.

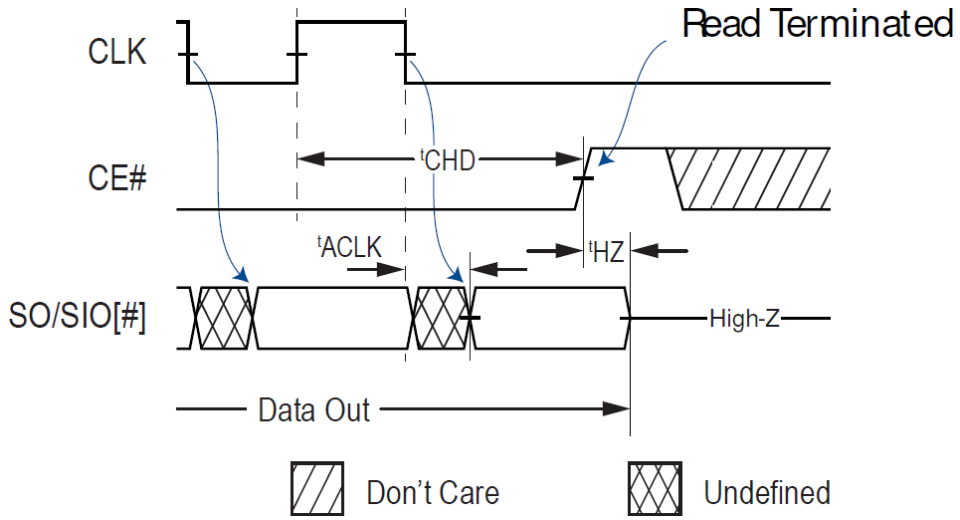



**Figure 3: Read Command Termination**


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# 12 Mode Register Operations

## 12.1 SPI MR Read Operation

For all reads, MR data will be available $^{t}$ACLK after the falling edge of CLK.

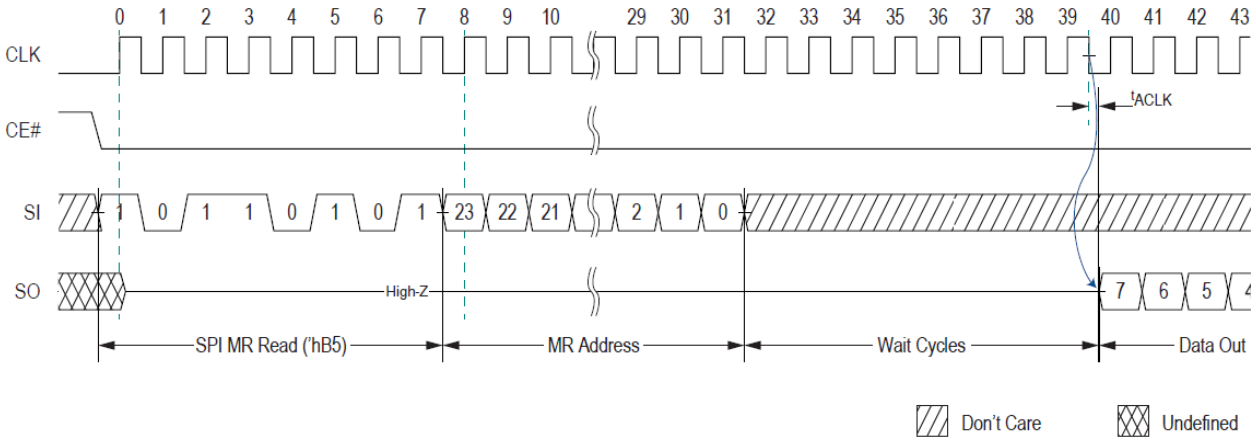



**Figure 4: SPI MR Read 'hB5**

## 12.2 SPI MR Write Operation

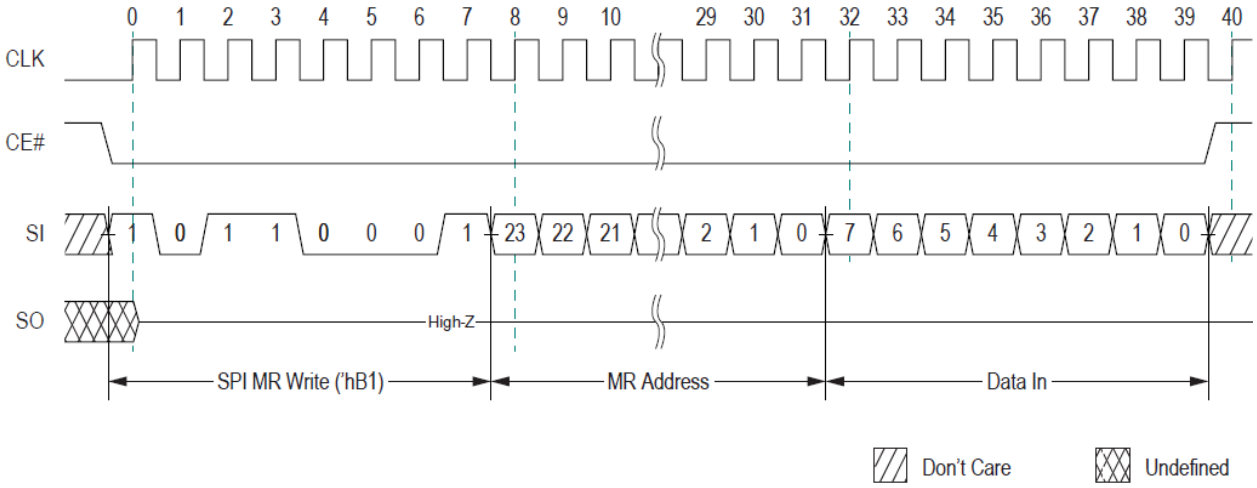



**Figure 5: SPI MR Write 'hB1**


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## 12.3 QPI MR Read Operation

For all reads, MR data will be available $^{t}$ACLK after the falling edge of CLK.

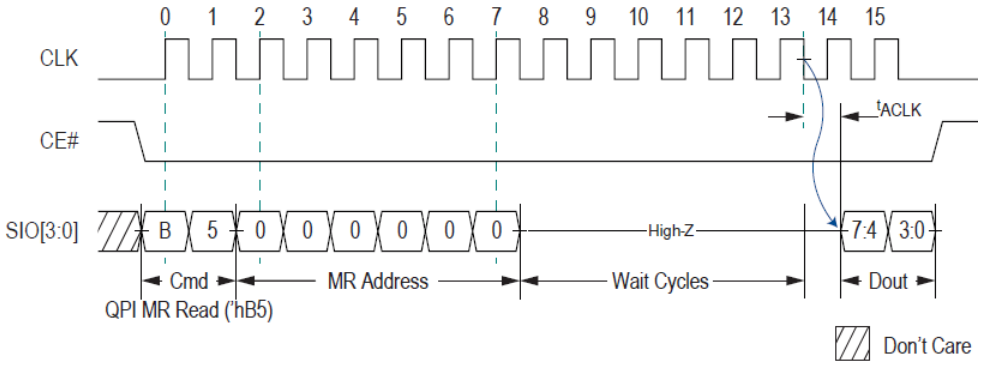



**Figure 6: QPI MR Read 'hB5**

## 12.4 QPI MR Write Operation

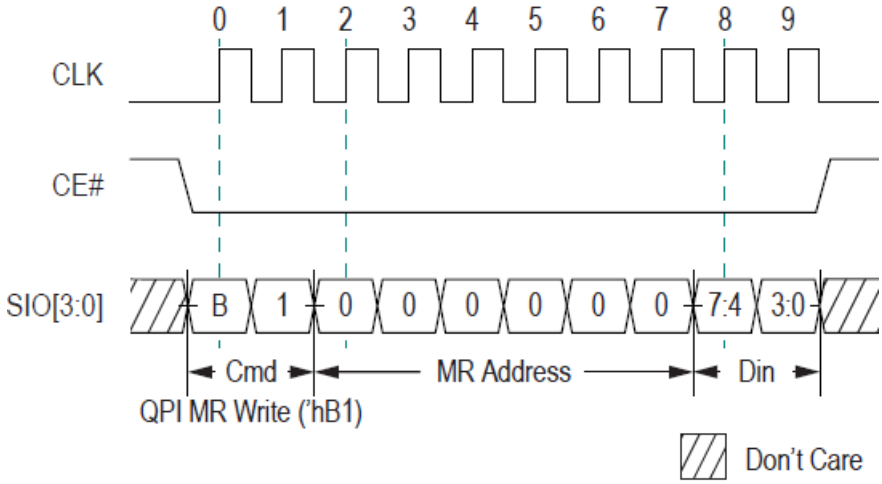



**Figure 7: QPI MR Write 'hB1**


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# 13 Read ID

Read ID command provides information of vendor ID, known-good-die, device density, and manufacturing ID. Note that Read ID command can be used ONLY as Power up initialization after the device Reset tRST≧ 50ns right after Global Reset command.




**Figure 12: Pre-condition of EID Read**

## *13.1 SPI Read ID Operation*

This command is similar to Fast Read, but without the wait cycles and the device outputs EID value instead of data.

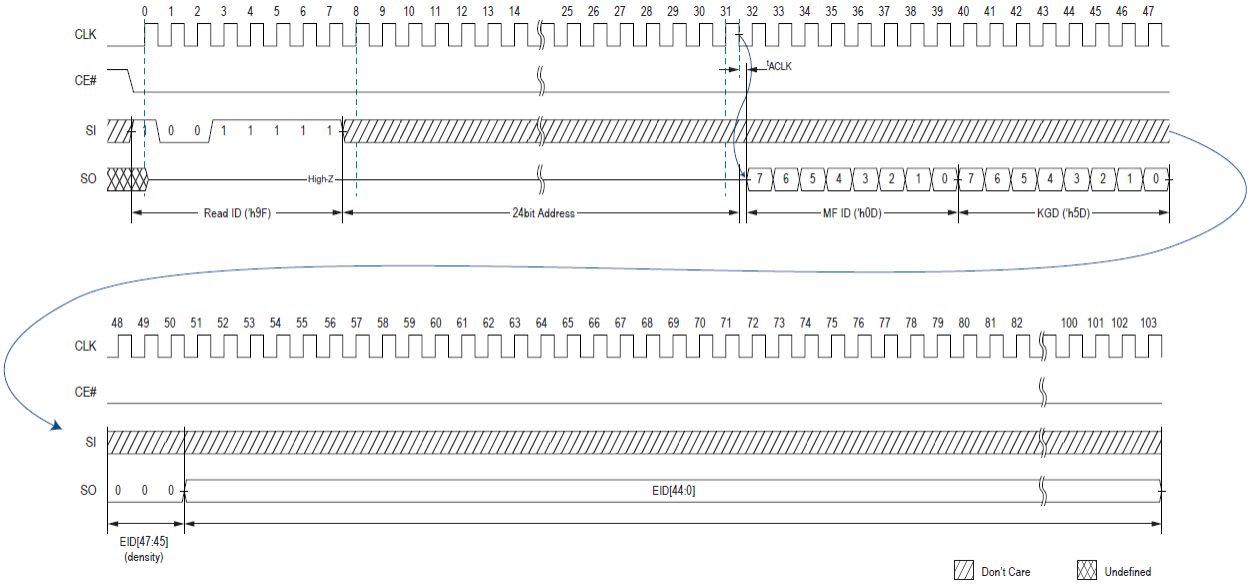



**Figure 8: SPI Read ID 'h9F (available only in SPI mode)**

# 14 Toggle Burst Length Operation

The Toggle Burst Length Operation switches the device's wrapped burst boundary between the Mode Register setting MR0[6:5] and a fixed value of 32 bytes.

Commands other than Wrapped Read ('h8B) and Wrapped Write ('h82) are linear type bursts which allow the


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device to burst through page boundaries. A page boundary crossing is only available when the Burst Length Toggle is set to use MR settings (default) **AND** Burst Wrap setting is set to full page size MR0[6:5] = 11 (default). The page boundary crossing is invisible to the memory controller and limited to a lower max CLK frequency of 84MHz.

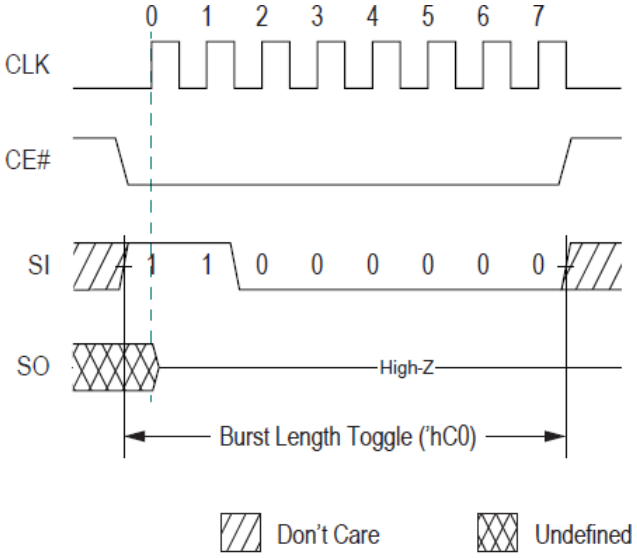



**Figure 9: SPI Burst Length Toggle 'hC0**

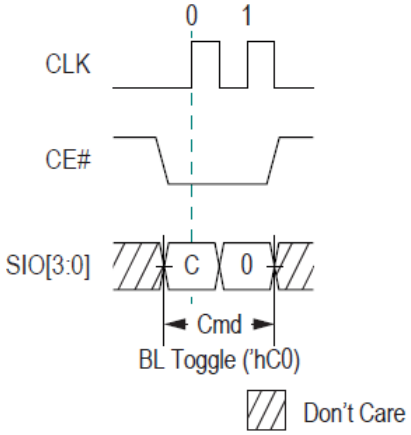



**Figure 10: QPI Burst Length Toggle 'hC0**


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# 15 SPI Mode Operations

The device powers up into SPI mode by default but can also be switched into QPI mode.

## *15.1 SPI Read Operations*

For all reads, data will be available $^{t}$ACLK after the falling edge of CLK.

SPI Reads can be done in four ways:

1. 'h03: Serial CMD, Serial Addr/IO, slow frequency, with wrap or linear bursting.
2. 'h0B: Serial CMD, Serial Addr/IO, fast frequency, with wrap or linear bursting.
3. 'hEB: Serial CMD, Quad Addr/IO, fast frequency, with wrap or linear bursting.
4. 'h8B: Serial CMD, Serial Addr/IO, fast frequency, with forced wrap (toggle & register configurable lengths).

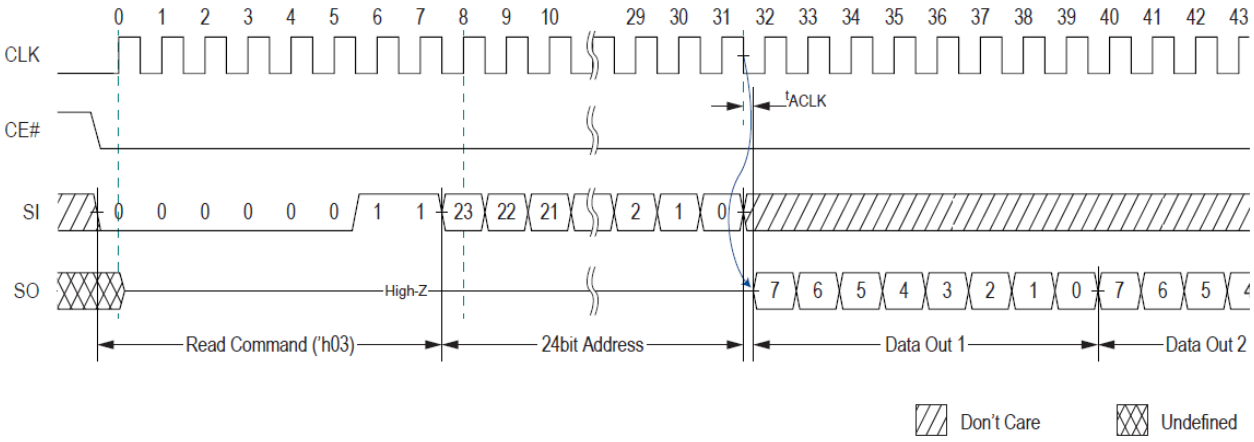



**Figure 11: SPI Read 'h03 (max freq 33 MHz)**

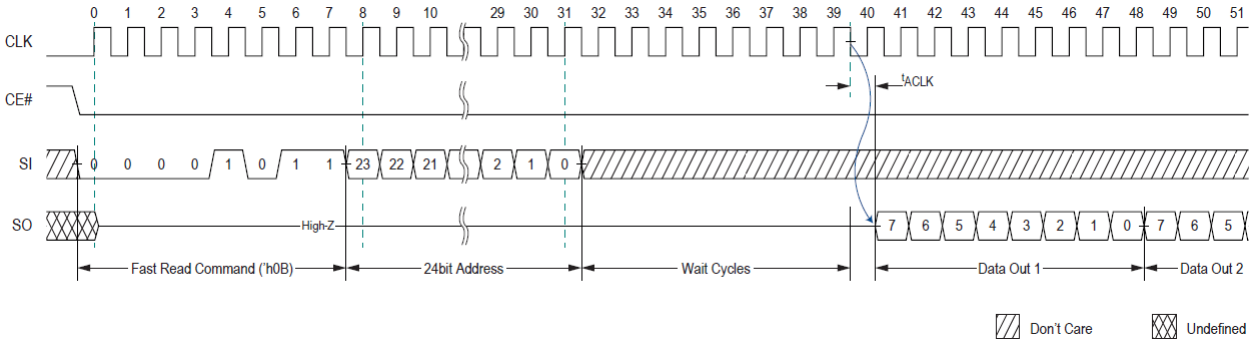



**Figure 12: SPI Fast Read 'h0B (max freq 133/84 MHz)**


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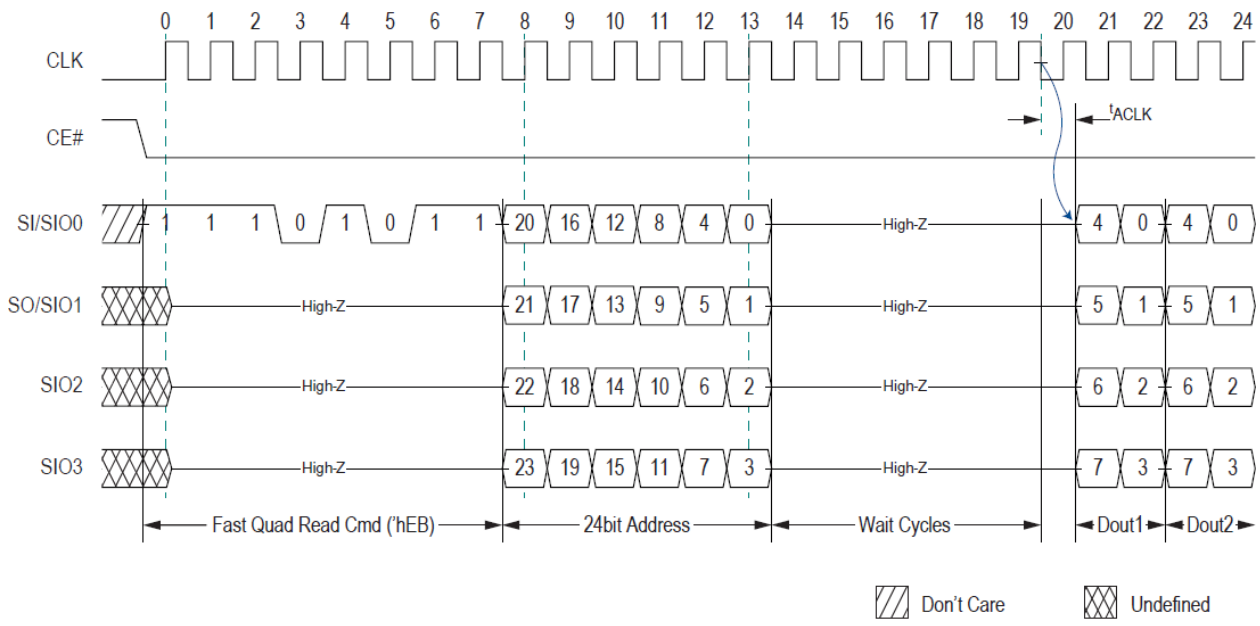



**Figure 13: SPI Fast Quad Read 'hEB (max freq 133/84 MHz)**


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## *15.2 SPI Write Operations*

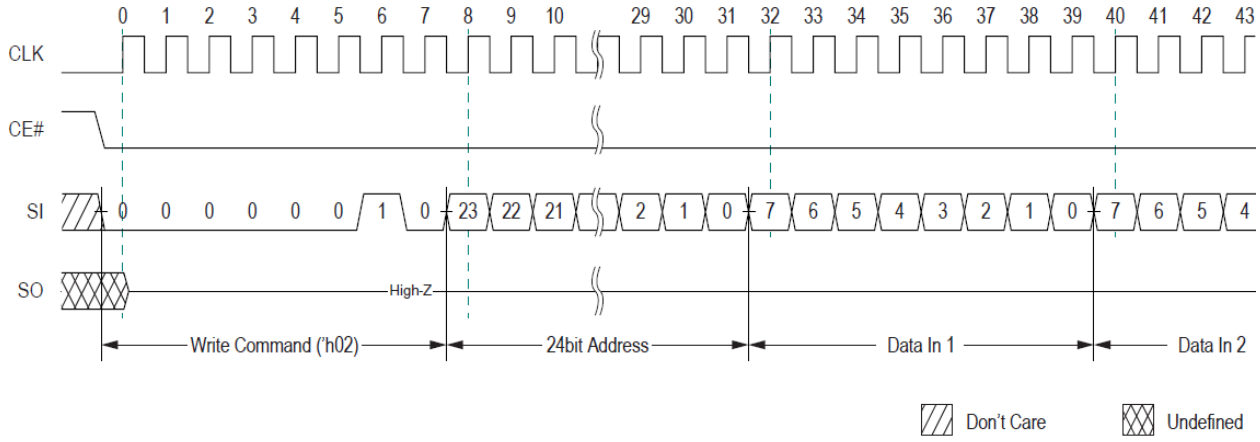



**Figure 14: SPI Write 'h02**

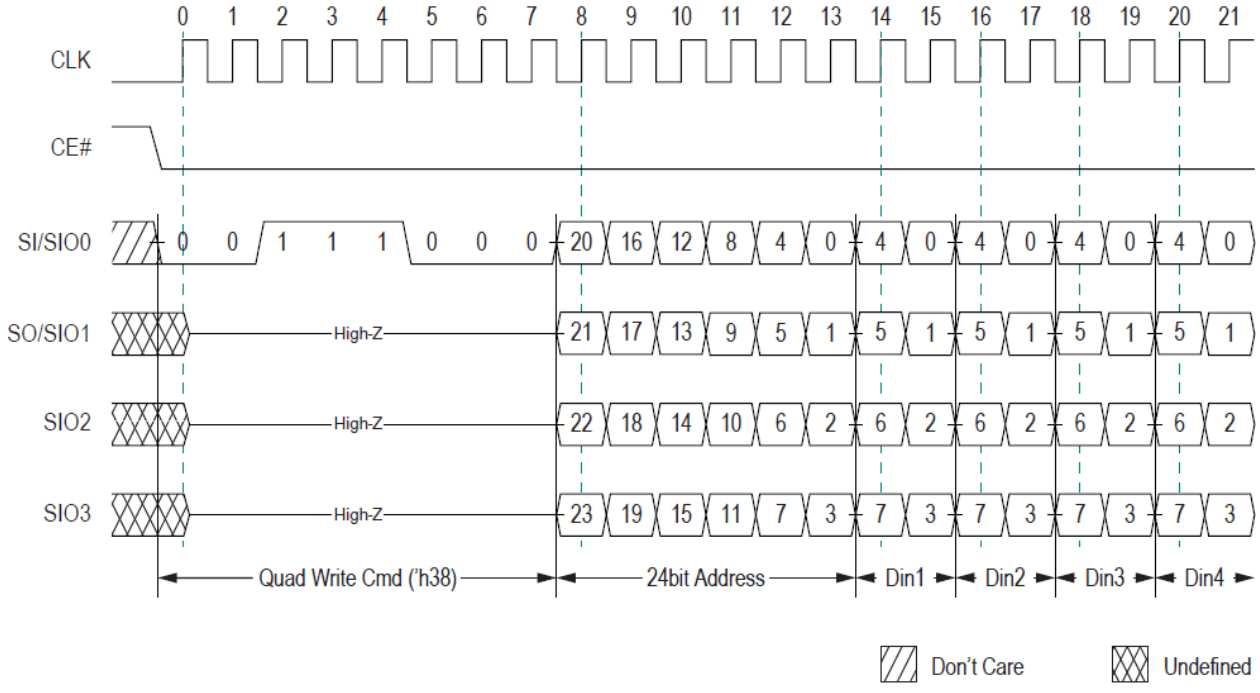



**Figure 15: SPI Quad Write 'h38**


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### *15.3 SPI Quad Mode Enable Operation*

This command switches the device into quad IO mode.

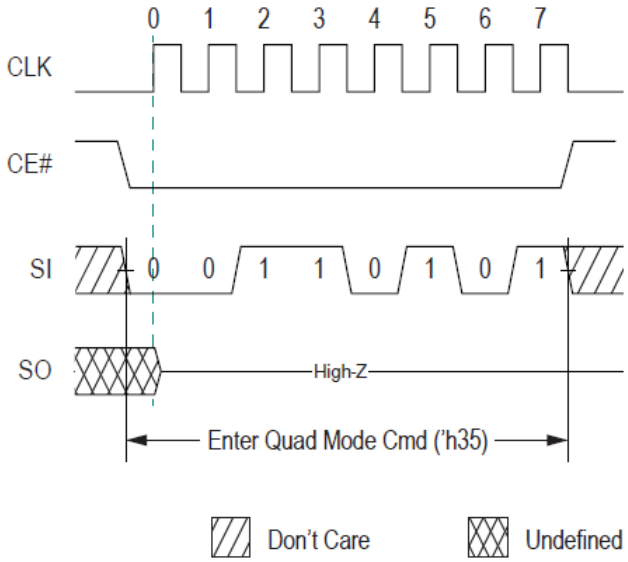



**Figure 16: Quad Mode Enable 'h35 (available only in SPI mode)**


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# 16 QPI Mode Operations

## *16.1 QPI Read Operations*

For all reads, data will be available $^{t}$ACLK after the falling edge of CLK.

QPI Reads can be done in one of three ways:

1. ‘h0B: Quad CMD, Addr & IO, slow frequency with wrap or linear bursting.
2. ‘hEB: Quad CMD, Addr & IO, fast frequency with wrap or linear bursting.
3. ‘h8B: Quad CMD, Addr & IO, fast frequency with forced wrap (toggle & register configurable lengths).

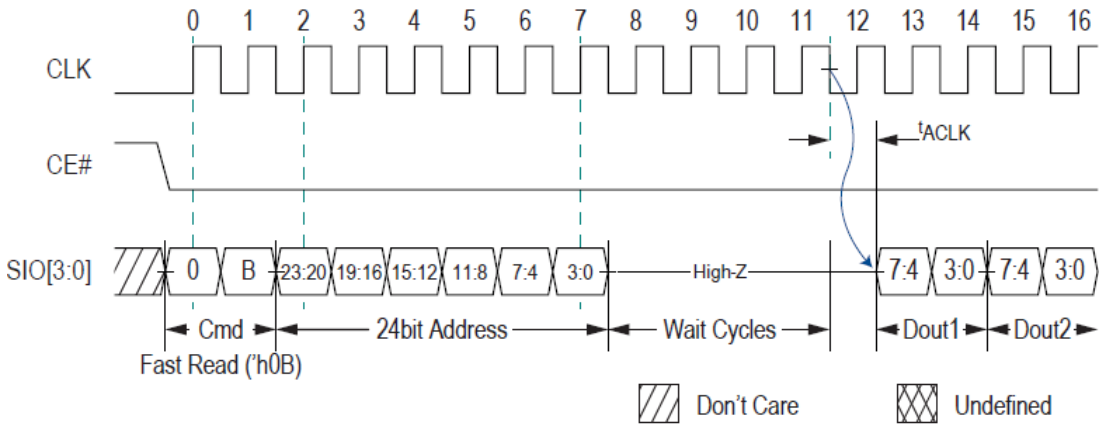



**Figure 17: QPI Fast Read ‘h0B (max freq 66 MHz)**

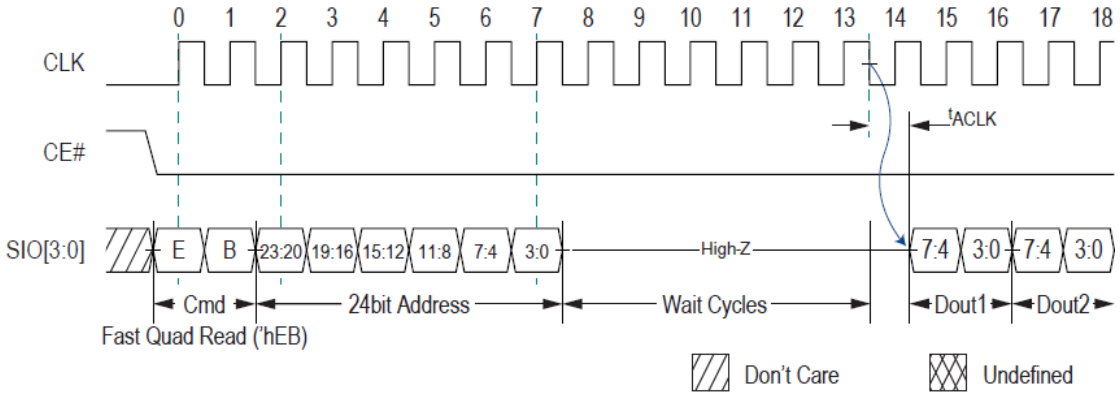



**Figure 18: QPI Fast Quad Read ‘hEB (max freq 133/84 MHz)**


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## 16.2 QPI Write Operation(s)

QPI write command can be done in one of two ways:

1. ‘h02 or ‘h38: Quad CMD, Addr & IO, with wrap or linear bursting.
2. ‘h82: Quad CMD, Addr & IO, with forced wrap (toggle & register configurable lengths).

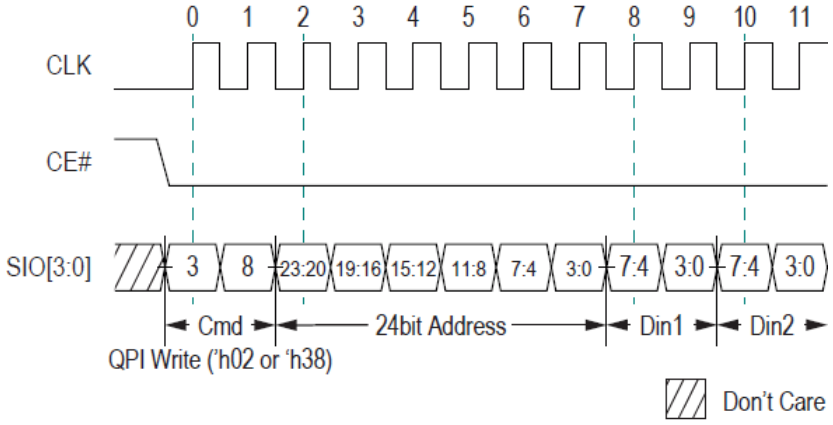



**Figure 19: QPI Write**

## 16.3 QPI Quad Mode Exit operation

This command will switch the device back into serial IO mode.

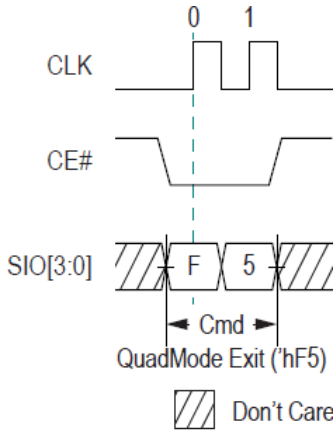



**Figure 20: Quad Mode Exit ‘hF5 (only available in QPI mode)**


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## 17 Reset Operation

The Reset operation is used as a system (software) reset that puts the device in SPI standby mode which is also the default mode after power-up. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST).

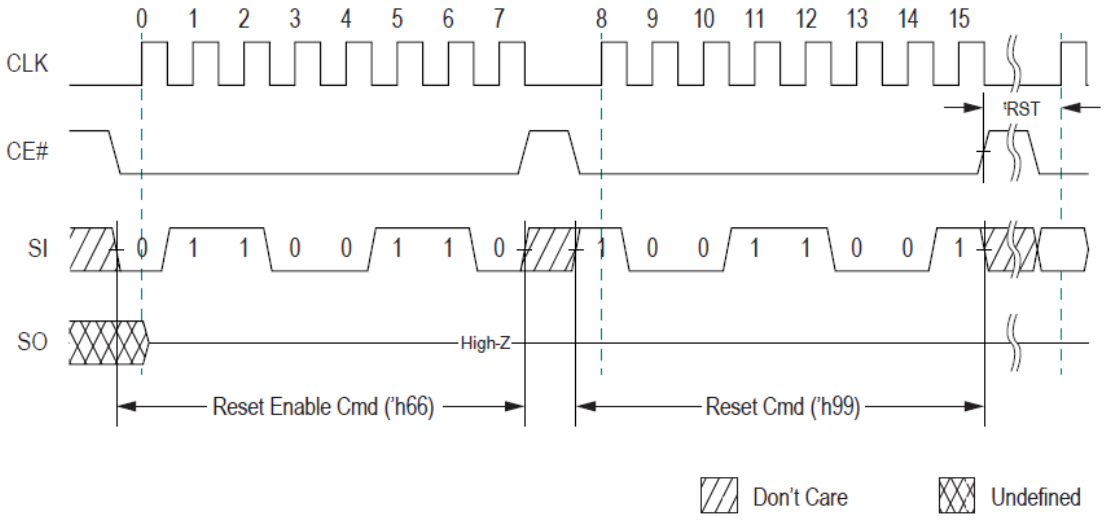



**Figure 21: SPI Reset**

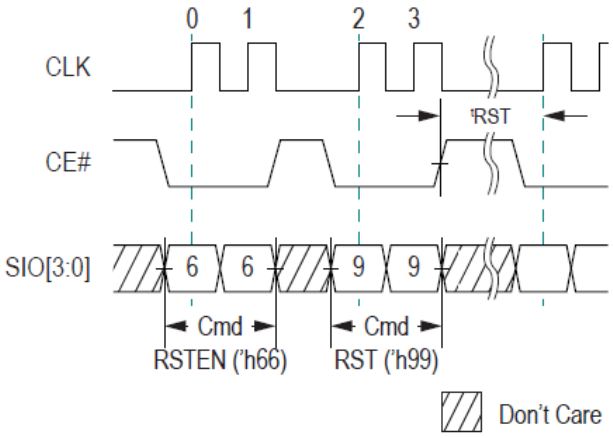



**Figure 22: QPI Reset**

Reset command has to immediately follow the Reset-Enable command in order for the reset operation to take effect. Any command other than the Reset command after the Reset-Enable command will cause the device to exit Reset-Enable state and abandon reset operation.


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# 18 Input/Output Timing

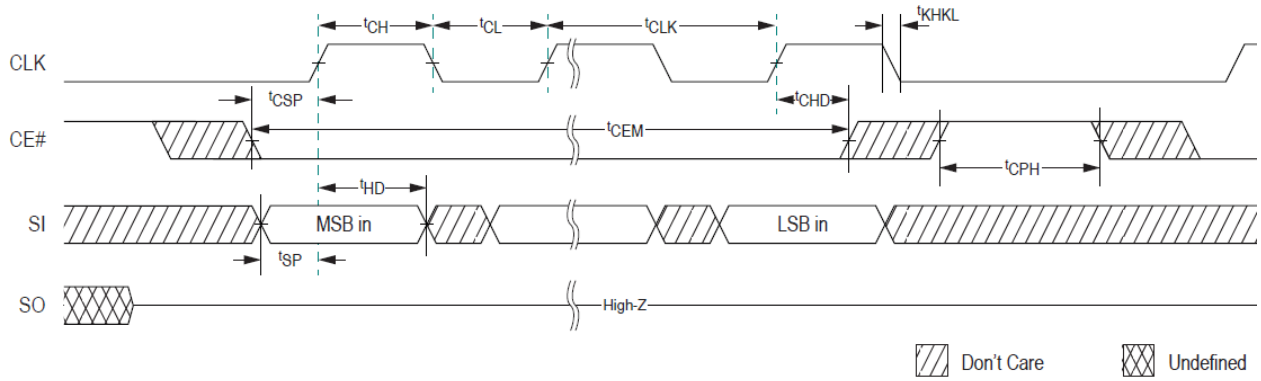



**Figure 23: Input Timing**

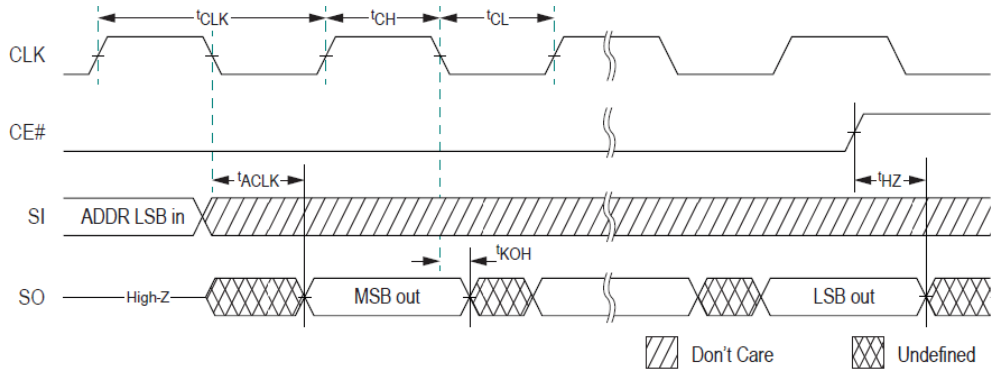



**Figure 24: Output Timing**


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# 19 Electrical Specifications:

## *19.1 Absolute Maximum Ratings*

**Table 6: Absolute Maximum Ratings**

| *Parameter* | *Symbol* | *Rating* | *Unit* | *Notes* |
|---|---|---|---|---|
| Voltage to any ball except $V_{DD}$ relative to $V_{SS}$ | VT | -0.4 to $V_{DD}$+0.4 | V | |
| Voltage on $V_{DD}$ supply relative to $V_{SS}$ | $V_{DD}$ | -0.4 to +4.0 | V | |
| Storage Temperature | $T_{STG}$ | -55 to +150 | ℃ | 1 |

Notes 1: Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

Caution:
Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

## *19.2 Input Signal Overshoot*

During DC conditions, input or I/O signals should remain equal to or between VSS and VDD. During voltage transitions, inputs or I/Os may negative overshoot VSS to -1.0V or positive overshoot to VDD +1.0V, for periods up to 20 ns.

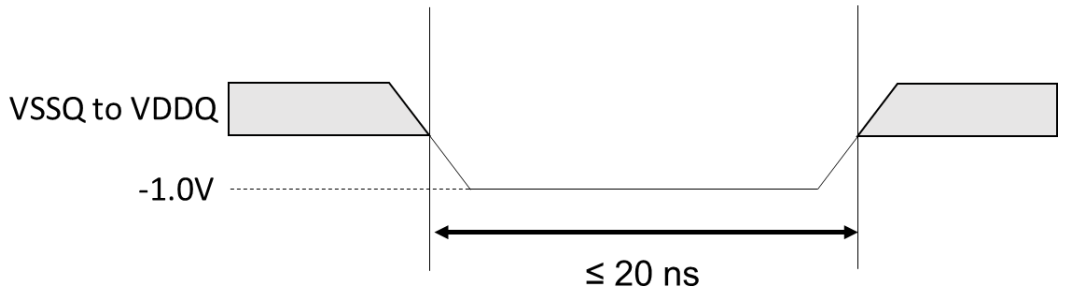



**Figure 25 Maximum Negative Overshoot Waveform**

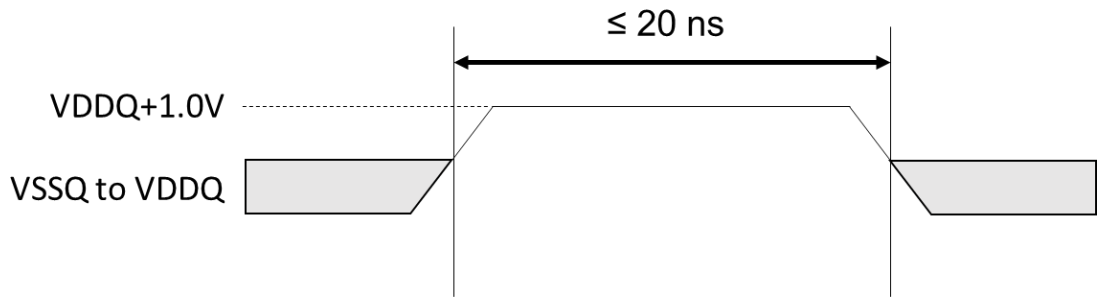



**Figure 26 Maximum Positive Overshoot Waveform**


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## *19.3 Pin Capacitance*

**Table 7: Bare Die Pin Capacitance**

| *Parameter* | *Symbol* | *Min* | *Max* | *Unit* | *Notes* |
|---|---|---|---|---|---|
| Input Pin Capacitance | CIN | | 2 | pF | VIN=0V |
| Output Pin Capacitance | COUT | | 3 | pF | VOUT=0V |

Note: spec'd at 25°C.

**Table 8: Package Pin Capacitance**

| *Parameter* | *Symbol* | *Min* | *Max* | *Unit* | *Notes* |
|---|---|---|---|---|---|
| Input Pin Capacitance | CIN | | 6 | pF | VIN=0V |
| Output Pin Capacitance | COUT | | 8 | pF | VOUT=0V |

Note: spec'd at 25°C.

**Table 9: Load Capacitance**

| *Parameter* | *Symbol* | *Min* | *Max* | *Unit* | *Notes* |
|---|---|---|---|---|---|
| Load Capacitance | $C_L$ | | 15 | pF | |

Note: System $C_L$ for the use of package


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## 19.4 Decoupling Capacitor Requirement

It is required to have a decoupling capacitor on VDD pin for IO switchings and psram internal transient events. A low ESR 1µF ceramic cap is recommended. To minimize parasitic inductance, place the cap as close to VDD pin as possible. An optional 0.1µF can further improve high frequency transient response.

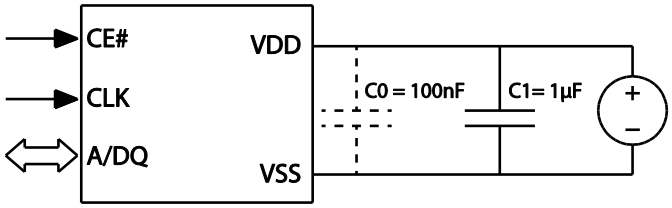



**Figure 27: Decoupling Capacitor**

Note that the length of grounding connection between PSRAM and PCB must be as short as possible. Having **ground plane on PCB** and **multipoint ground** would be preferred (to avoid single-point grounding topology). The width of VDD and VSS traces would be suggested more than 20mil.

## 19.5 Operating Conditions

**Table 10: Operating Characteristics**

| *Parameter* | *Min* | *Max* | *Unit* | *Notes* |
|---|---|---|---|---|
| Operating Temperature (extended) | -40 | 105 | °C | |
| Operating Temperature (standard) | -40 | 85 | °C | |


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## *19.6 DC Characteristics*

**Table 11: DC Characteristics**

| *Symbol* | *Parameter* | *Min* | *Max* | *Unit* | *Notes* |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 2.7 | 3.6 | V | |
| $V_{IH}$ | Input high voltage | $V_{DD}$-0.4 | $V_{DD}$+0.2 | V | |
| $V_{IL}$ | Input low voltage | -0.2 | 0.4 | V | |
| $V_{OH}$ | Output high voltage ($I_{OH}$=-0.2mA) | 0.8 $V_{DD}$ | | V | |
| $V_{OL}$ | Output low voltage ($I_{OL}$=+0.2mA) | | 0.2 $V_{DD}$ | V | |
| $I_{LI}$ | Input leakage current | | 1 | µA | |
| $I_{LO}$ | Output leakage current | | 1 | µA | |
| $I_{CC}$ | Read/Write (133MHz) | | 7 | mA | 1,2 |
| | Read/Write (66MHz) | | 6 | mA | 1,2 |
| | Read/Write (13MHz) | | 5 | mA | 1,2 |
| $ISB_{EXT}$ | Standby current (105C) | | 200 | µA | 3 |
| $ISB_{STD}$ | Standby current (85C) | | 150 | µA | 3 |

Note 1: Output load current not included
2: 50% bus toggling rate.
3: Standby current is measured when CLK is in DC low state.
4: Typical ISBSTD 35µA at 25°C


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## *19.7 AC Characteristics*

**Table 12: READ/WRITE Timing**

| Symbol | Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $^{t}$CLK | CLK period - SPI Read (‘h03) | 30.3 | | ns | 33MHz |
| | CLK period - QPI Read (‘h0B) | 15.1 | | | 66MHz |
| | CLK period - all other operations PKG 3V | 7.5 | | | 133MHz*1,2,3 |
| | CLK period - all other operations PKG 3.3V | 9.17 | | | 109MHz*1,2,3 |
| | CLK period - all other operations | 11.9 | | | 84MHz*1 |
| $^{t}$CH/$^{t}$CL | Clock high/low width | 0.45 | 0.55 | $^{t}$CLK(min) | |
| $^{t}$KHKL | CLK rise or fall time | | 1.5 | ns | 4 |
| $^{t}$CPH | CE# HIGH between subsequent burst operations | 18 | | ns | |
| $^{t}$CEM | CE# low pulse width | | 3 | µs | Extended |
| | | | 8 | | Standard grade |
| $^{t}$CSP | CE# setup time to CLK rising edge PKG | 2.5 | | ns | |
| $^{t}$CHD | CE# hold time from CLK rising edge PKG | 3.0 | | ns | |
| $^{t}$SP | Setup time to active CLK edge | 2 | | ns | |
| $^{t}$HD | Hold time from active CLK edge | 2 | | ns | |
| $^{t}$HZ | Chip disable to DQ output high-Z | | 5.5 | ns | |
| $^{t}$ACLK | CLK to output delay | 2 | 5.5 | ns | |
| $^{t}$KOH | Data hold time from clock falling edge | 1.5 | | ns | |
| $^{t}$RST | Time between end of RST CMD to next valid CMD | 50 | | ns | |

Note 1: Only Linear 512 Burst allows page boundary crossing. Frequency limits are therefore 133MHz max for Wrapped Burst operation at VDD=3.0V+/-10%, 109MHz for Wrapped Burst operation at VDD=3.3V+/-10%, 84MHz max when Linear 512 Burst commands cross page boundary

2: System max $C_L$ 15pF for the use of package.

3: For operating frequencies >84MHz, it is highly recommended to utilize CLK falling edge to sample read data or align sampling clock via data pattern tuning (refer to JEDEC JESD84-B50 for an example).

4: Measured from 20% to 80% of VDD


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## 20 Change Log

| Version | Who | Date | Description |
|---|---|---|---|
| 1.0 | | Aug 01, 2017 | Officially released |
| 1.1 | | Aug 24, 2017 | Added system max $C_L$ for the use of package & related tCK and tCHD; relaxed tCSP/tHD, removed drive strength setting '11, changed tACLK, tKHKL, tCPH; added ISBstdroom |
| 1.5 | | Oct 30, 2017 | Enabled QPI Read 'h0B support; changed Min/Max absolute voltage, Vil_min and Vih_max,; defined tCEM for different temperature grade; corrected speed typo. Added USON package ZR |
| 1.6 | | Nov 10, 2017 | Modified spec of ISB, ICC |
| 1.7 | | Feb 26, 2018 | Typo corrected in Fig.12, 17 |
| 1.8 | | Mar 29, 2018 | Revised part # for RBX |
| 1.9 | | Oct 03, 2018 | added SPI MRW/MRR waves, elaborated on boundary crossing conditions and table, QPI EID Read, updated package information & corrected some wording |
| 2.0 | | Oct 03, 2018 | Revised speed for linear read & Read ID |
| 2.1 | | Dec. 13, 2018 | Added tRST parameter, Block Diagram, updated POD of USON, ball map of WLCSP, temperature grade, Typo corrected |
| 2.2 | | Jul 19, 2019 | Update section 13 from –SQR v2.16, and min frequency of truth table in section 11 from –SQQ v2.43 |
| 2.3 | | Sep 06, 2019 | Updated Page 1, Section 5 and **錯誤! 找不到參照來源。**; updated Table 9 and Table 11 |
| 2.4a | | Oct 02, 2019 | Updated header, footer and Page 1 |
| 2.5 | | Oct 24, 2019 | Revised typo in **錯誤! 找不到參照來源。** and Table 12; updated notes in 19.4 |
| 2.6 | | Nov 21, 2019 | Updated Table 2 |
| 2.7 | | Apr 30, 2020 | Modify VDD's description of Table 2 |
| 2.8 | | Oct 12, 2021 | Revised tCEM value from 4us to 3us @105C |
| 2.8a | | Dec 13, 2021 | Revised some figure can't display grid (ex: Don't care/Undefined) when conversion to PDF. |
| 2.8b | Alan | Jan 25, 2022 | Update Table of Contents page number. |
| 2.9 | Kim/ Gene/ Eric | Jun 16, 2022 | Typos correct |
| 3.0 | Kim | Oct 28, 2022 | Release USON temp. from -25~85 to -40~85 |
| 3.1 | Kim | Nov 21, 2023 | Add chapter 19.2 Input signal overshoot |


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