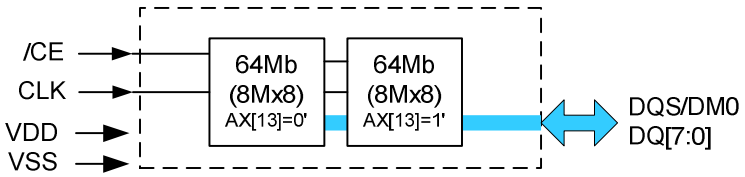
# Double-Data-Rate OPI Xccela PSRAM

## Specifications

- **Single Supply Voltage**
  - VDD = 2.7 to 3.6V
  - VDDQ = 2.7 to 3.6V
- **Interface**: Octal SPI with DDR Xccela mode, two bytes transfers per one clock cycle
- **Performance**: Clock rate up to 133MHz, 266MB/s read/write throughput
- **Organization**: 128Mb, 16M x 8bits with 1024 bytes page size
  - Column address: AY0 to AY9
  - Row address: AX0 to AX13
- **Refresh**: Self-managed
- **Operating Temperature Range**
  - Tc = -40°C to +85°C(standard range)
  - Tc= -40°C to +105°C (extended range)
- **Maximum Standby Current**
  - 700µA @ 105°C (extended range)
  - 500µA @ 85°C
  - 280µA @ 25°C

## Features

- **Low Power Features**
  - Partial Array Self-Refresh (PASR)
  - Auto Temperature Compensated Self-Refresh (ATCSR) by built-in temperature sensor
  - User configurable refresh rate
- **Software Reset**
- **Reset Pin Available**
- **Output Driver LVCMOS** with programmable drive strength
- **Data Mask (DM)** for write data
- **Data Strobe (DQS)** enabled highspeed read operation
- **Register Configurable** write and read initial latencies
- **Write Burst Length**, maximum 1024 Byte, minimum 2 Byte.
- Wrap & Hybrid Burst in 16/32/64/1K lengths.
- **Linear Burst Command**
- **Row Boundary Crossing (RBX)**
  - read operations can be enabled via Mode Register
  - RBX Write is NOT supported
  - RA[13] Boundary Crossing is NOT supported between 2 dies




Block Diagram


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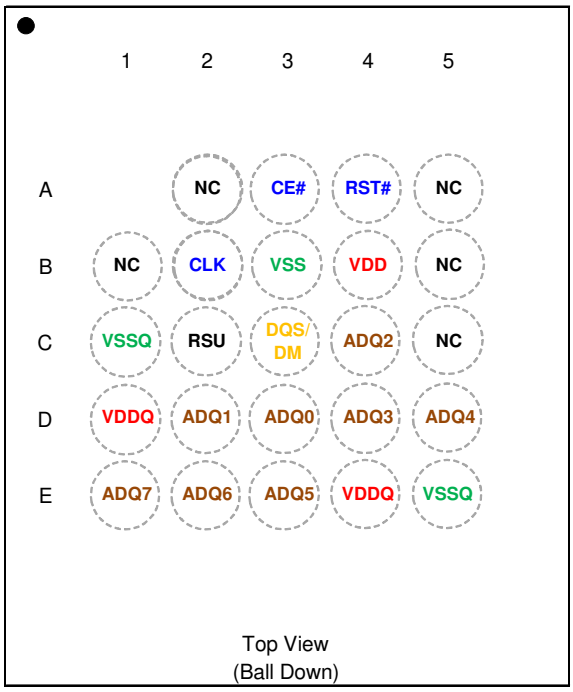
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# 2 Package Information

The APS12808L-3OBMx is available in miniBGA 24L package 6 x 8 x 1.2mm, ball pitch 1.0mm,ball size 0.4mm , package code “BA”.

- Ball Assignment for MINIBGA 24L




(6x8x1.2mm)(P1.0)(B0.4)

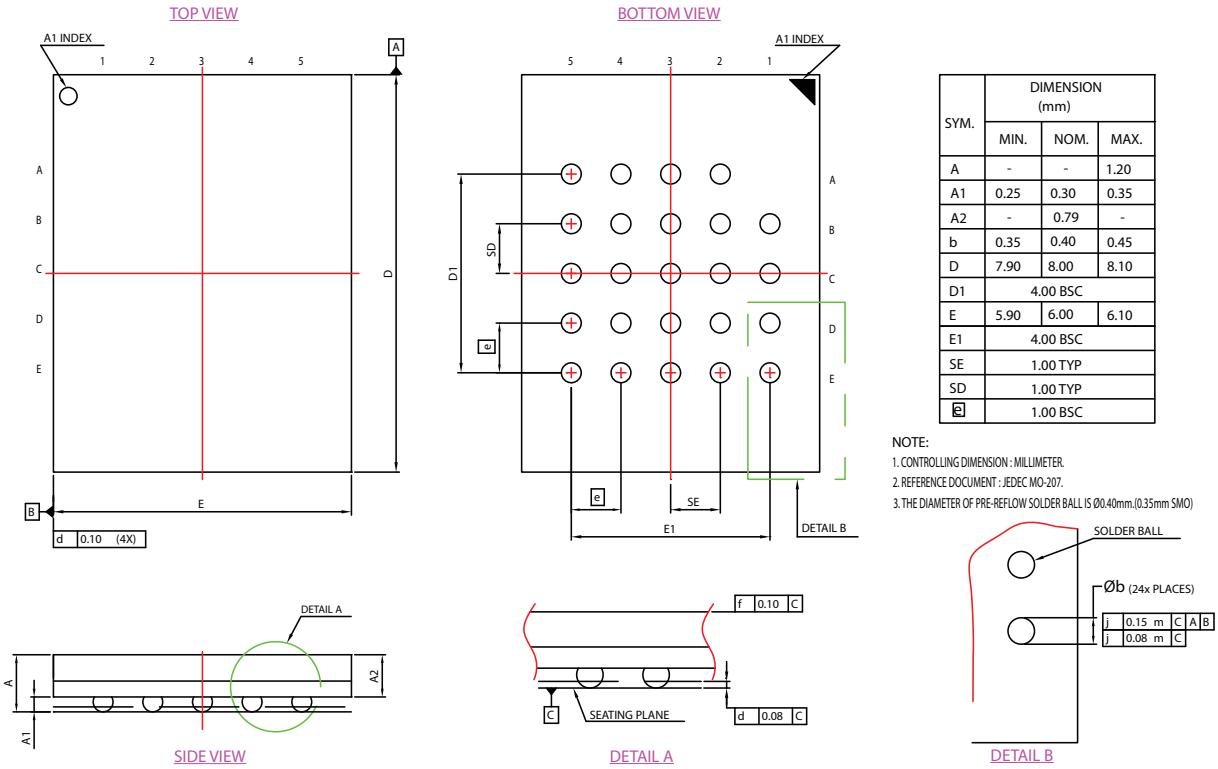
Note:

1. Part Number APS12808L-3OBM-BA for 128Mb.
2. RFU: Reserved for future use, which is reserved for 2nd CE#.
3. NC: No internal connection.


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# 3 Package Outline Drawing




| SYM. | DIMENSION (mm) | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | - | - | 1.20 |
| A1 | 0.25 | 0.30 | 0.35 |
| A2 | - | 0.79 | - |
| b | 0.35 | 0.40 | 0.45 |
| D | 7.90 | 8.00 | 8.10 |
| D1 | | 4.00 BSC | |
| E | 5.90 | 6.00 | 6.10 |
| E1 | | 4.00 BSC | |
| SE | | 1.00 TYP | |
| SD | | 1.00 TYP | |
| e | | 1.00 BSC | |

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.
3. THE DIAMETER OF PRE-REFLOW SOLDER BALL IS Ø0.40mm.(0.35mm SMO)


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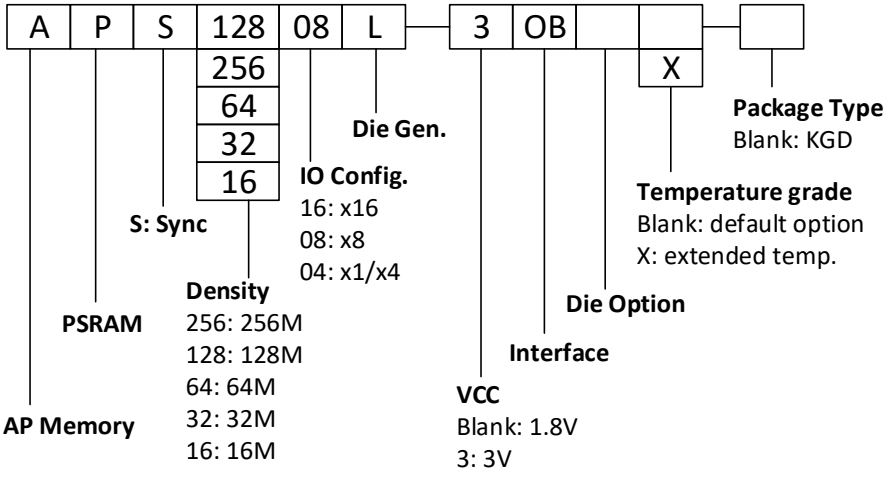
# 4 Ordering Information

**Table 1: Ordering Information**

| *Part Number* | *Temperature Range* | *Max Frequency* | *Note* |
|---|---|---|---|
| APS12808L-3OBM-BA | Tc= -40°C to +85°C | 133 MHz | 24b Package |
| APS12808L-3OBMX-BA | Tc= -40°C to +105°C | 133 MHz | 24b Package |

Note

- OBM is standard part to support RBX read operation only.





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# 5 Signal Table

All signals are listed in Table 2.

**Table 2: Signals Table**

| *Symbol* | *Type* | *Description* | *Comments* |
|---|---|---|---|
| $V_{DD}$ | Power | Core supply 3.0V | |
| $V_{DDQ}$ | Power | IO supply 3.0V | |
| $V_{SS}$ | Ground | Core supply ground | |
| $V_{SSQ}$ | Ground | IO supply ground | |
| A/DQ[7:0] | IO | Address/DQ bus [7:0] | |
| DQS/DM | IO | DQ strobe clock during reads, Data mask during writes. DM is active high. DM=1 means “do not write”. | |
| CE# | Input | Chip select, active low. When CE#=1, chip is in standby state. | |
| CLK | Input | Clock signal | |
| RESET# | Input | Reset signal, active low. Optional, as the pad is internally tied to a weak pull-up and can be left floating. | |


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# 6 Power-Up Initialization

Octal DDR products include an on-chip voltage sensor used to start the self-initialization process. $V_{DD}$ and $V_{DDQ}$ must be applied simultaneously. When they reach a stable level at or above minimum $V_{DD}$, the device is in Phase 1 and will require 150µs to complete its self-initialization process. The user can then proceed to Phase 2 of the initialization described in this section.

During Phase 1 CE# should remain HIGH (track $V_{DD}$ within 200mV); CLK should remain LOW.

After Phase 2 is complete the device is ready for operation.

## *6.1 Power-Up Initialization Method 1 (via. RESET# pin)*

The RESET# pin can be used to initialize the device during Phase 2 as follows:

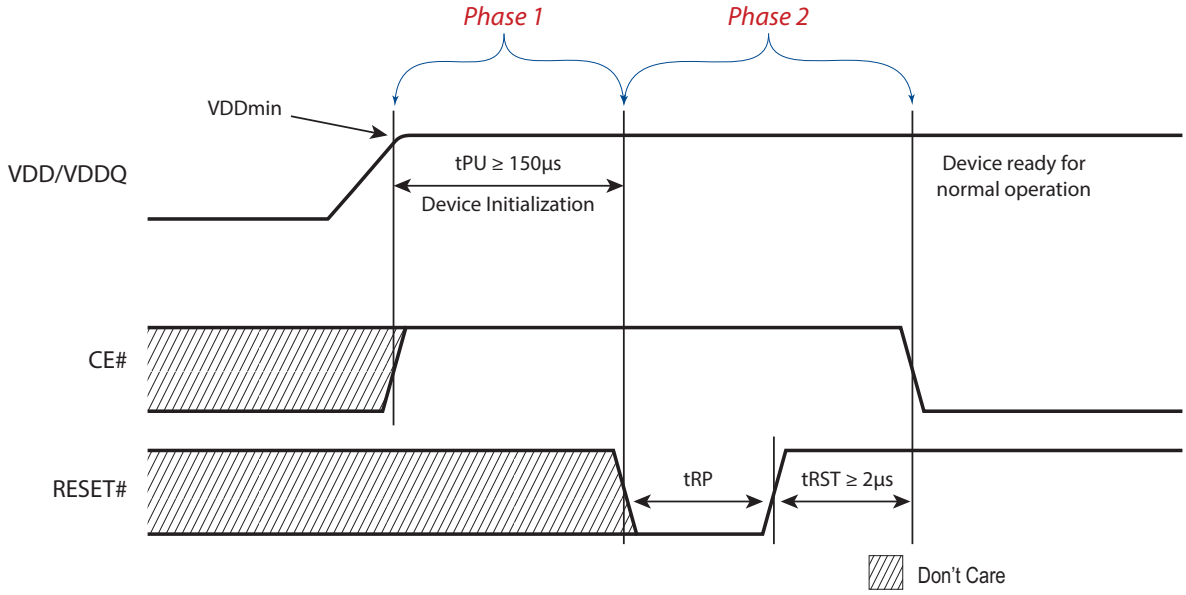



**Figure 1. Power-Up Initialization Method 1 RESET#**

The RESET# pin can also be used at any time after the device is initialized to reset all register contents. Memory content is not guaranteed. Timing requirements for RESET# usage are shown below.

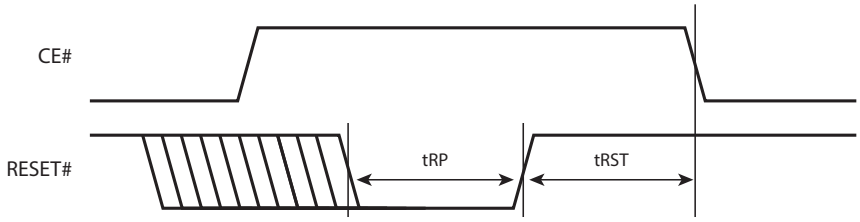



**Figure 2. RESET# Timing**


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## 6.2 Power-Up Initialization Method 2 (via. Global Reset)

As an alternate power-up initialization method, After the Phase 1 150µs period the Global Reset command is used to reset the device in Phase 2 as follows:

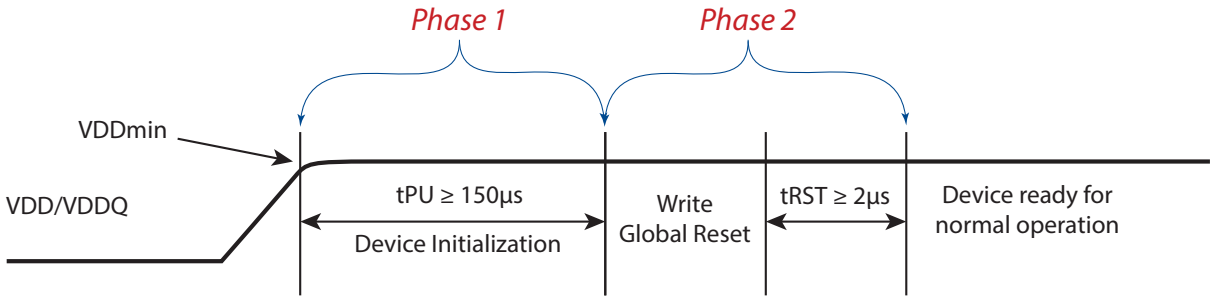



**Figure 3. Power-Up Initialization Method 2 Timing with Global Reset**

The Global Reset command resets all register contents. Memory content is not guaranteed. The command frame is made of 4 clocked CE# lows. Clocking is optional during tRST. The Global Reset command sequence is shown below. Note that Global Reset command can be used ONLY as Power-up initialization.

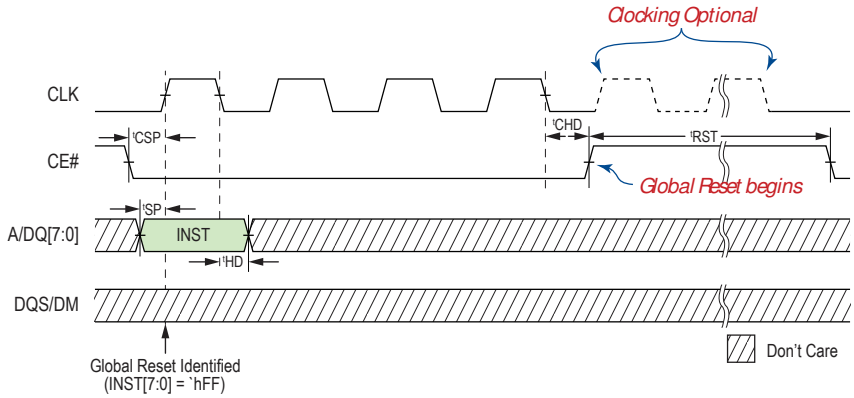



**Figure 4: Global Reset**


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# 7 Interface Description

## 7.1 Address Space

Octal DDR PSRAM device is byte-addressable. Memory accesses are required to start on even addresses (A[0]='0). Mode Register accesses allow both even and odd addresses.

## 7.2 Burst Type & Length

Read and write operations are default Hybrid Wrap 32 mode. Other burst lengths of 16, 32, 64 or 1K bytes in standard or Hybrid wrap modes are register configurable (see Table 18) The device also includes command for Linear Bursting. Bursts can start on any even address. Write burst length has a minimum of 2 bytes. Read has no minimum length. Both write and read have no restriction on maximum burst length as long as tCEM is met.

## 7.3 Command/Address Latching

After CE# goes LOW, instruction code is latched on 1st CLK rising edge. Access address is latched on the 3rd, 4th, 5th & 6th CLK edges (2nd CLK rising edge, 2nd CLK falling edge, 3rd CLK rising edge, 3rd CLK falling edge).

## 7.4 Command Truth Table

The Octal DDR PSRAM recognizes the following commands specified on the INST (Instruction) cycle defined by the Address/DQ pins.

| | 1st CLK | | 2nd CLK | | 3rd CLK | |
|---|---|---|---|---|---|---|
| Command | ↑ | ↓ | ↑ | ↓ | ↑ | ↓ |
| Sync Read | 00h | | A3 | A2 | A1 | A0 |
| Sync Write | 80h | | A3 | A2 | A1 | A0 |
| Sync Read (Linear Burst) | 20h | | A3 | A2 | A1 | A0 |
| Sync Write (Linear Burst) | A0h | | A3 | A2 | A1 | A0 |
| Mode Register Read | 40h | | × | | | MA |
| Mode Register Write | C0h | | × | | | MA |
| Global Reset | FFh | | × | | | |

Remarks: × = don't care ($V_{IH}$/$V_{IL}$)
A3 = unused address bits are reserved
A2 = RA[13:6]
A1 = RA[5:0],CA[9:8]
A0 = CA[7:0]
MA = Mode Register Address


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## 7.5 Read Operation

After address latching, the device initializes DQS/DM to '0 from **next** CLK rising edge of the 3rd clock cycle (A1). See Figure 5 below.

Output data is available after LC latency cycles, as shown in Figure 7 & Figure 8, LC is defined in Table 5 and Table 6. When data is valid, A/DQ[7:0] and DQS/DM follow the timing specified in Figure 9. Synchronous timing parameters are shown in Table 28 & Table 29.

In case of internal refresh insertion, variable latency output data may be delayed by up to (LC*2) latency cycles as shown in Figure 7. True variable refresh pushout latency can be anywhere **between** LC to LCx2. The 1st DQS/DM rising edge after read pre-amble indicates the beginning of valid data.

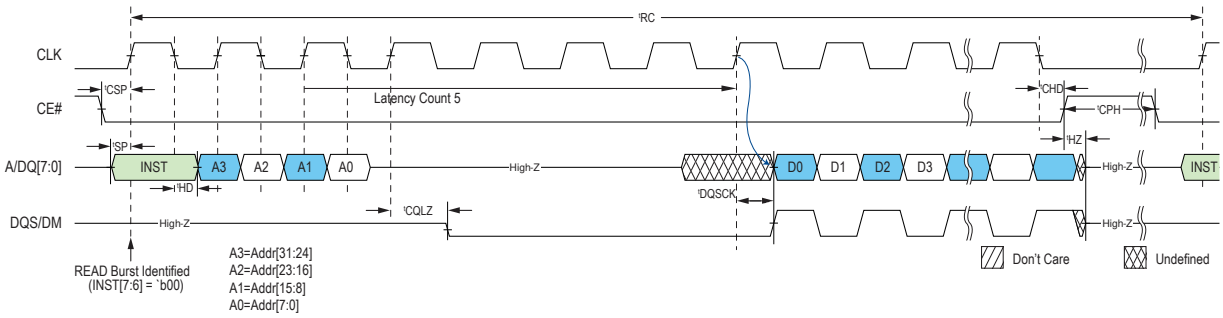



**Figure 5: Synchronous Read**

If RBX has been enabled (MR8[3] written to 1) and a Linear Burst Command issued, then Wrap settings (MR8[2:0] are ignored and Read operations are allowed to cross row boundaries as shown in Figure 6.

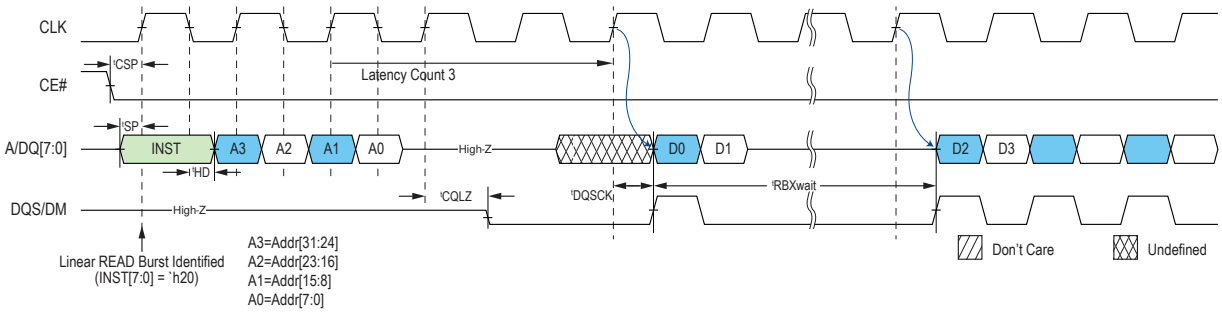



**Figure 6: Synchronous Read with RBX (Starting address '3FE)**


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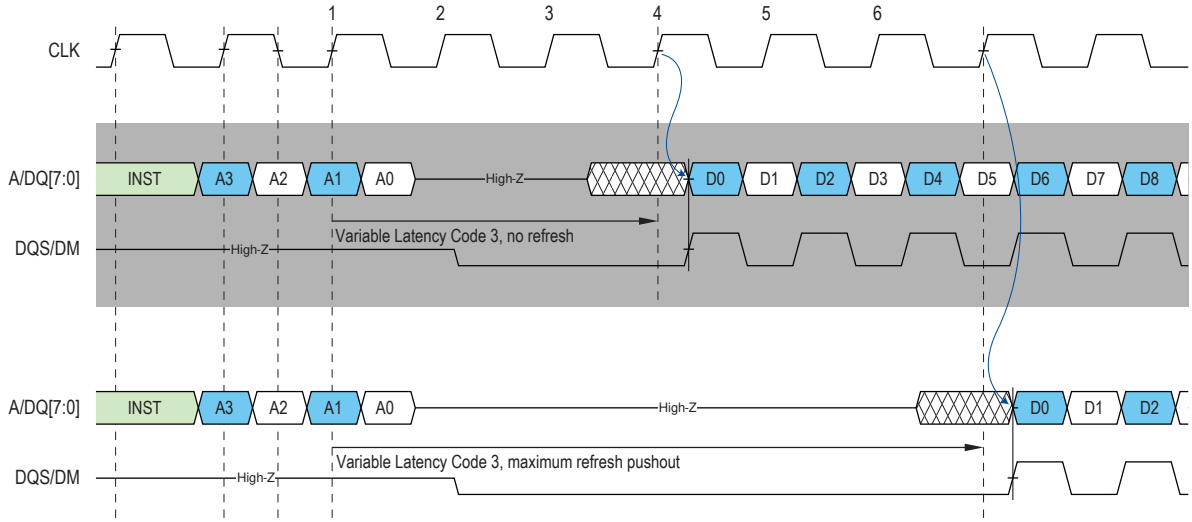



**Figure 7: Variable Read Latency Refresh Pushout**

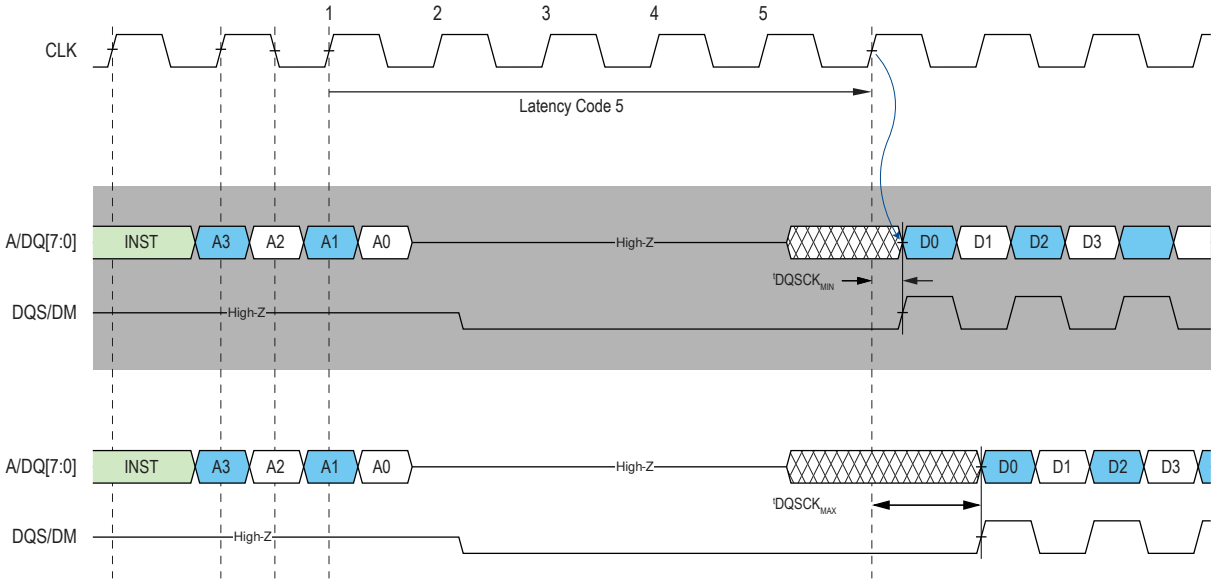



**Figure 8: Read Latency & tDQSCK**


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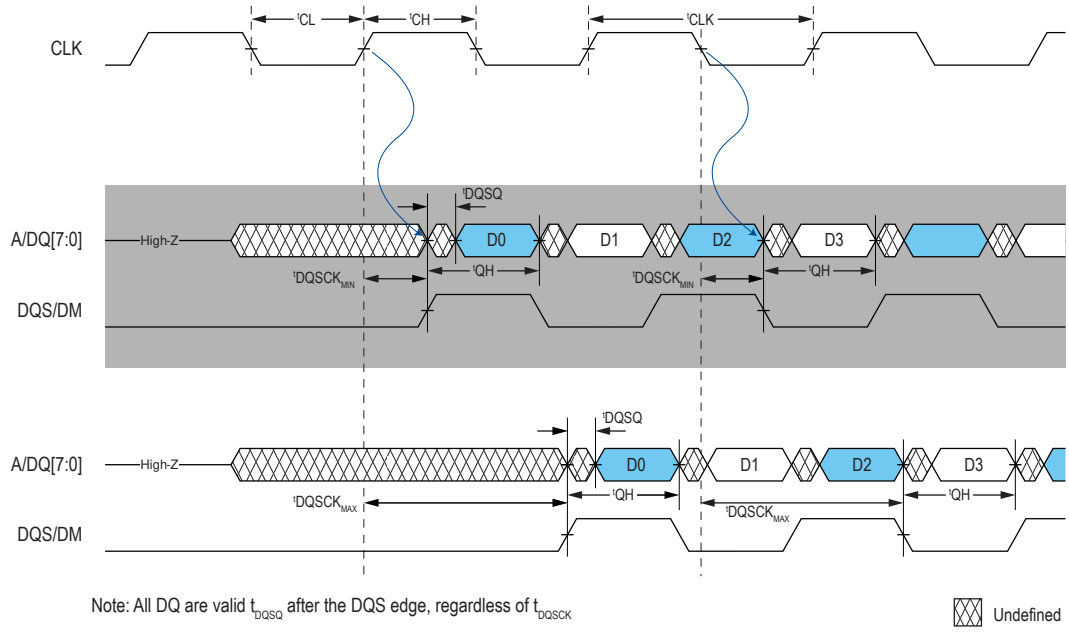



**Figure 9: Read DQS/DM & DQ timing**


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## 7.6 Write Operation

A minimum of 2 bytes of data must be input in a write operation. In the case of consecutive short burst writes, tRC must be met by issuing additional CE# high time between operations. Single-byte write operations can be performed by masking the un-written byte with DQS/DM as shown in Figure 10.

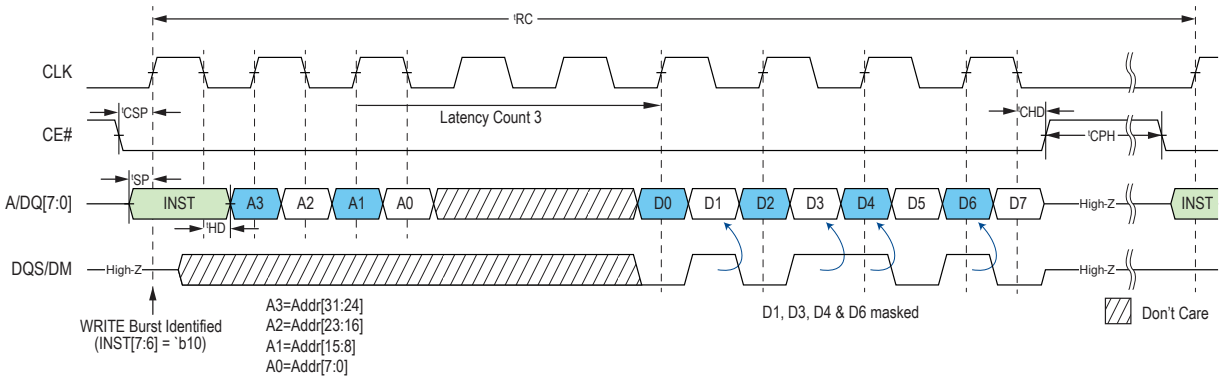



**Figure 10: Synchronous Write followed by any Operation**

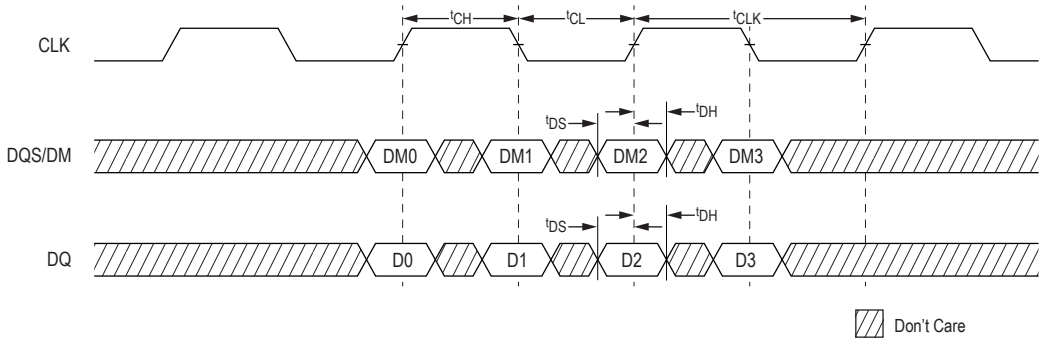


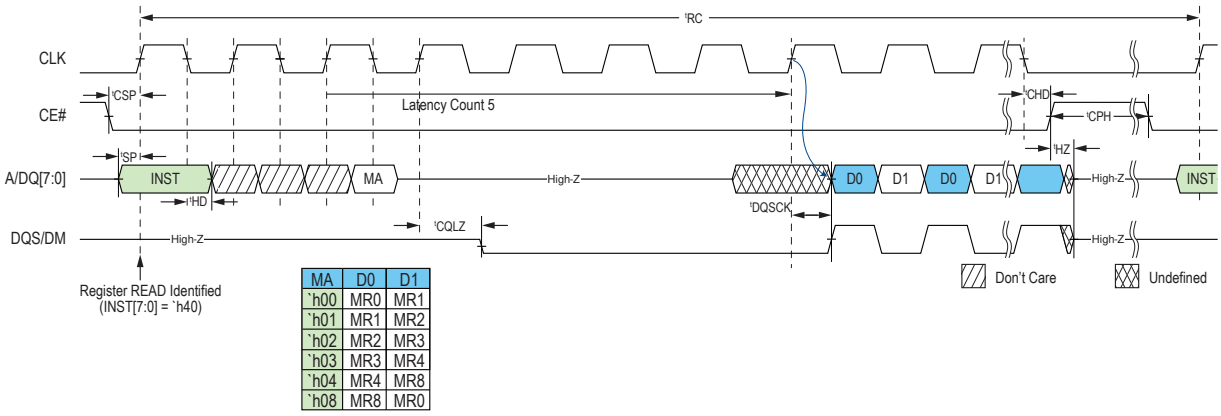

**Figure 11: Write DQS/DM & DQ Timing**


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## 7.7 Control Registers

Register Read is shown below. Mode Address in command determines which Mode Register is read from as Data0 (see chart in the Figure below).




| MA | D0 | D1 |
|---|---|---|
| `h00 | MR0 | MR1 |
| `h01 | MR1 | MR2 |
| `h02 | MR2 | MR3 |
| `h03 | MR3 | MR4 |
| `h04 | MR4 | MR8 |
| `h08 | MR8 | MR0 |

**Figure 12: Register Read**

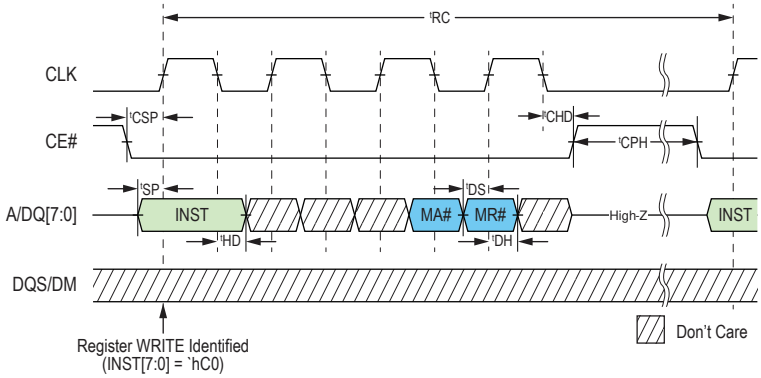



**Figure 13: Register Write**

Register Writes are Latency 1, whereas Register Reads use the same MR0[4:2] settings as burst reads (see Table 5). Registers 0, 4 & 8 are read and writable, and Registers 1, 2 and 3 are read-only. Register mapping is shown in Table 3. Note that MR0[6], MR0[7],MR4[4] and MR8[7] must be written to b'0.


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**Table 3: Mode Register Table**

| MR No. | MA[7:0] | Access | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | `h00 | R/W | '00' | | LT | Read Latency Code | | | Drive Str. | |
| 1 | `h01 | R | rsvd. | | | Vendor ID | | | | |
| 2 | `h02 | R | GB | rsvd. | | Dev ID | | Density | | |
| 3 | `h03 | R | RBXen | VCC | SRF | rsvd. | | | | |
| 4 | `h04 | R/W | Write Latency Code | | | '0' | RF | PASR | | |
| 8 | `h08 | R/W | '0' | rsvd. | | | RBX | BT | BL | |

**Table 4: Read Latency Type (MR0[5])**

| Latency Type | |
|---|---|
| **MR0[5]** | **LT** |
| 0 | Variable (default) |
| 1 | Fixed |

**Table 5: Read Latency Codes MR0[5:2]**

| | VL Codes (MR0[5]=0) | | FL Codes (MR0[5]=1) | Max Input CLK Freq (MHz) | |
|---|---|---|---|---|---|
| **MR0[4:2]** | **Latency (LC)** | **Max push out (LCx2)** | **Latency (LCx2)** | **Standard** | **Extended** |
| 000 | 3 | 6 | 6 | 66 | 66 |
| 001 | 4 | 8 | 8 | 109 | 109 |
| 010 | 5 (default) | 10 | 10 | 133 | 133 |
| others | reserved | | | - | - |

**Table 6: Operation Latency Code Table**

| Type | Operation | VL (default) | | FL |
|---|---|---|---|---|
| | | No Refresh | Refresh | |
| Memory | Read | LC | Up to LCx2 | LCx2 |
| | Write | WLC | | WLC |
| Register | Read | LC | | LC |
| | Write | 1 | | 1 |

*Note: see Table 15 for WLC settings.


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**Table 7: Drive Strength Codes MR0[1:0]**

| *Codes* | *Drive Strength* |
|---|---|
| ‘00 | Half (50Ω) |
| ‘01 | 1/4 (100Ω default) |
| ‘10 | 1/8 (200Ω) |
| ‘11 | 1/16 (400Ω) |

**Table 8: Vendor ID mapping MR1[4:0]**

| *Vendor ID* |
|---|
| 01101: APM |

**Table 9: Good-Die Bit MR2[7]***

| *Codes* | *Good Die ID* |
|---|---|
| ‘1 | PASS |
| ‘0 | FAIL |

*Note: Default is FAIL die, and only mark PASS after all tests passed.

**Table 10: Device ID MR2[4:3]**

| *Codes* | *Device ID* |
|---|---|
| ‘00 | Generation 1 |
| ‘01 | Generation 2 |
| ‘10 | Generation 3 (default) |
| others | reserved |

**Table 11: Device Density mapping MR2[2:0]**

| *MR2[2:0]* | *Density* |
|---|---|
| ‘001 | 32Mb |
| ‘011 | 64Mb |
| ‘101 | 128Mb |
| ‘111 | 256Mb |
| others | reserved |

**Table 12: Row Boundary Crossing Enable (MR3[7])**

| *MR3[7] (read-only)* | *RBXen* |
|---|---|
| 0 | RBX not supported |
| 1 | RBX supported via MR8[3]=1 |


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**Table 13: Operating Voltage Range (MR3[6])**

| *MR3[6]* | *VCC* |
|---|---|
| 0 | 1.8V |
| 1 | 3V (default) |

**Table 14: Self Refresh Flag (MR3[5])**

| *MR3[5] (read-only)* | *Self Refresh Flag* |
|---|---|
| 0 | Slow Refresh (allowed via MR4[3]=1, otherwise Fast Refresh) |
| 1 | Fast Refresh |

MR3[5] is a refresh indicator that corresponds to device internal temperature. This bit will indicate 0 when the temperature is low enough to allow a slow frequency refresh rate.

**Table 15: Write Latency MR4[7:5]**

Default powered up behavior is WL 5

| *MR4[7:5]* | *Write Latency Codes (WLC)* | *Fmax (MHz)* |
|---|---|---|
| 000 | 3 | 66 |
| 100 | 4 | 109 |
| 010 | 5 (default) | 133 |
| others | reserved | - |

**Table 16: Refresh Frequency MR4[3]**

| *MR4[3]* | *Refresh Frequency* |
|---|---|
| 0 | Fast Refresh (default) |
| 1 | Enables Slow Refresh when temperature allows |


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**Table 17: PASR MR4[2:0]**

The PASR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map.

| *128Mb (64Mbx2)* | | | | |
|---|---|---|---|---|
| ***Codes*** | ***Refresh Coverage*** | ***Address Space*** | ***Size*** | ***Density*** |
| ‘000 | Full array (default) | 000000h-FFFFFFh | 16M x8 | 128Mb |
| ‘001 | Bottom 1/2 array | 000000h-7FFFFFh | 8M x8 | 64Mb |
| ‘010 | Bottom 1/4 array | 000000h-3FFFFFh | 4M x8 | 32Mb |
| ‘011 | Bottom 1/8 array | 000000h-1FFFFFh | 2M x8 | 16Mb |
| ‘100 | None | 0 | 0M | 0Mb |
| ‘101 | Top 1/2 array | 800000h-FFFFFFh | 8M x8 | 64Mb |
| ‘110 | Top 1/4 array | C00000h-FFFFFFh | 4M x8 | 32Mb |
| ‘111 | Top 1/8 array | E00000h-FFFFFFh | 2M x8 | 16Mb |


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**Table 18: Burst Type MR8[2], Burst Length MR8[1:0]**

By default the device powers up in 32 Byte Hybrid Wrap. In non-Hybrid burst (MR8[2]=0), MR8[1:0] sets the burst address space in which the device will continually wrap within. If Hybrid burst wrap is selected (MR8[2]=1), the device will burst through the initial wrapped burst length once, then continue to burst incrementally up to maximum column address (1K) before wrapping around within the entire column address space. Burst length (MR8[1:0]) can be set to 16,32,64 & 1K lengths.

| *MR8[2]* | *MR8[1:0]* | *Burst Length* | *Example of Sequence of Bytes During Wrap* | |
|---|---|---|---|---|
| | | | *Starting Address* | *Byte Sequence* |
| '0 | '00 | 16 Byte Wrap | 4 | [4,5,6,…15,0,1,2,…] |
| '0 | '01 | 32 Byte Wrap | 4 | [4,5,6,…31,0,1,2,…] |
| '0 | '10 | 64 Byte Wrap | 4 | [4,5,6,…63,0,1,2,…] |
| '0 | '11 | 1K Byte Wrap | 4 | [4,5,6,…1023,0,1,2,…] |
| '1 | '00 | 16 Byte Hybrid Wrap | 2 | [2,3,4,…15,0,1],16,17,18,…1023,0,1,… |
| '1 | '01 | 32 Byte Hybrid Wrap (default) | 2 | [2,3,4,…31,0,1],32,33,34,…1023,0,1,… |
| '1 | '10 | 64 Byte Hybrid Wrap | 2 | [2,3,4,…63,0,1],64,65,66,…1023,0,1,… |
| '1 | '11 | 1K Byte Wrap | 2 | [2,3,4,…1023,0,1,2,…] |

The Linear Burst Commands (INST[5:0]=6'b100000) override MR8[2:0] settings and forces the current array read or write command to do 1K Byte Wrap (equivalent to having MR8[1:0] set to 2'b11). The burst continues linearly from the starting address and at the end of the page, then wraps back to the beginning of the page. This special burst instruction can be used on both array write and read.

**Table 19: Row Boundary Crossing Read Enable MR8[3]**

This register setting applies to Linear Burst reads only on RBX enabled devices (MR3[7]=1). Default write and read burst behavior is limited within the 1K (CA='h000 -> 'h3FF) column address space. Setting this bit high will allow Linear Burst reads to cross over into the next Row (RA+1).

| *MR8[3]* | *RBX Read* |
|---|---|
| 0 | Reads stay within the 1K column address space |
| 1 | Reads cross row at 1K boundaries |


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# 8 Electrical Specifications:

## 8.1 Absolute Maximum Ratings

**Table 20: Absolute Maximum Ratings**

| Parameter | Symbol | Rating | Unit | Notes |
|---|---|---|---|---|
| Voltage to any ball except $V_{DD}$, $V_{DDQ}$ relative to $V_{SS}$ | VT | -0.4 to VDD/VDDQ+0.4 | V | |
| Voltage on $V_{DD}$ supply relative to $V_{SS}$ | $V_{DD}$ | -0.4 to +4 | V | |
| Voltage on $V_{DDQ}$ supply relative to $V_{SS}$ | $V_{DDQ}$ | -0.4 to +4 | V | |
| Storage Temperature | $T_{STG}$ | -55 to +150 | °C | 1 |

Notes 1: Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

Caution:
Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

## 8.2 Pin Capacitance

**Table 21: Bare Die Pin Capacitance**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input Pin Capacitance | CIN | | 4 | pF | VIN=0V |
| Output Pin Capacitance | COUT | | 6 | pF | VOUT=0V |

Note 1: spec'd at 25°C.

**Table 22: Package Pin Capacitance**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input Pin Capacitance | CIN | | 8 | pF | VIN=0V |
| Output Pin Capacitance | COUT | | 10 | pF | VOUT=0V |

Note 1: spec'd at 25°C.

**Table 23: Load Capacitance**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Load Capacitance | $C_L$ | | 15 | pF | |

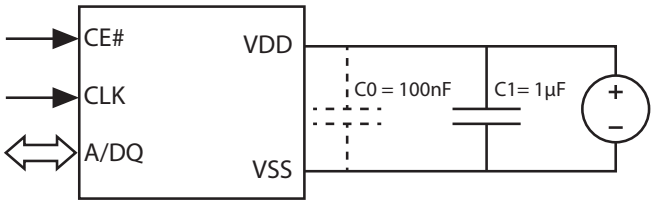
Note 1: System $C_L$ for the use of package


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## 8.3 Decoupling Capacitor Requirement

It is required to have a decoupling capacitor on VDD pin for IO switchings and psram internal transient events. A low ESR 1µF ceramic cap is recommended. To minimize parasitic inductance, place the cap as close to VDD pin as possible. An optional 0.1µF can further improve high frequency transient response.




## 8.4 Operating Conditions

**Table 24: Operating Characteristics**

| *Parameter* | *Min* | *Max* | *Unit* | *Notes* |
|---|---|---|---|---|
| Operating Temperature (extended) | -40 | 105 | °C | 1 |
| Operating Temperature (standard) | -40 | 85 | °C | |

Note 1: Extended temp range of -40 to 105°C is only characterized; test condition is -32 to 105°C.


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## 8.5 DC Characteristics

**Table 25: DC Characteristics**

| Symbol | Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 2.7 | 3.6 | V | |
| $V_{DDQ}$ | I/O Supply Voltage | 2.7 | 3.6 | V | |
| $V_{IH}$ | Input high voltage | $V_{DDQ}$-0.4 | $V_{DDQ}$+0.2 | V | |
| $V_{IL}$ | Input low voltage | -0.2 | 0.4 | V | |
| $V_{OH}$ | Output high voltage ($I_{OH}$=-0.2mA) | 0.8 $V_{DDQ}$ | | V | |
| $V_{OL}$ | Output low voltage ($I_{OL}$=+0.2mA) | | 0.2 $V_{DDQ}$ | V | |
| $I_{LI}$ | Input leakage current | | 1 | µA | |
| $I_{LO}$ | Output leakage current | | 1 | µA | |
| ICC | Read/Write @ 13MHz | | 3 | mA | 2 |
| | Read/Write @133MHz | | 14 | mA | 2 |
| $ISB_{EXT}$ | Standby current (extended temp) | | 700 | µA | 1,3 |
| $ISB_{STD}$ | Standby current (standard temp) | | 500 | µA | 3 |
| $ISB_{STDroom}$ | Standby current (standard room temp) | | 280 | µA | 3,4,5 |

Note 1: Spec'd up to 105°C.
2: Current is only characterized.
3: Without CLK toggling. ISB will be higher if CLK is toggling.
4: Slow Refresh.
5: Typical ISBSTDroom 200©µA


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## 8.6 ISB Partial Array Refresh Current

**Table 26: Typical PASR Current @ 25°C**

| *Standby Current @ 25°C* | | | |
|---|---|---|---|
| ***PASR*** | ***ISB –typical mean*** | ***Unit*** | ***Notes*** |
| Full | 200 | µA | 1,2 |
| 1/2 | 180 | µA | 1,2 |
| 1/4 | 170 | µA | 1,2 |
| 1/8 | 160 | µA | 1,2 |

**Table 27: Typical PASR Current @ 85°C**

| *Standby Current @ 85°C* | | | |
|---|---|---|---|
| ***PASR*** | ***ISB –typical mean*** | ***Unit*** | ***Notes*** |
| Full | 390 | µA | 2 |
| 1/2 | 338 | µA | 2 |
| 1/4 | 312 | µA | 2 |
| 1/8 | 300 | µA | 2 |

Note 1: Slow Refresh current is only attainable by enabling Slow Refresh Frequency (see Table 16)

Note 2: PASR Current is only characterized based on 128M density without CLK toggling.



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## 8.7 AC Characteristics

**Table 28: READ/WRITE Timing**

| | | -7 (133MHz) | | -9 (109MHz) | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| tCLK | CLK period | 7.5 | | 9.2 | | ns | |
| tCH/tCL | Clock high/low width | 0.45 | 0.55 | 0.45 | 0.55 | tCLK | |
| tKHKL | CLK rise or fall time | | 1.0 | | 1.2 | ns | |
| tCPH | CE# HIGH between subsequent burst operations | 18 | | 18 | | ns | |
| tCEM | CE# low pulse width | | 4 | | 4 | µs | Standard temp |
| | | | 1 | | 1 | µs | Extended temp |
| tCEM | CE# low pulse width | 3 | | 3 | | tCLK | Minimum 3 clocks |
| tCSP | CE# setup time to CLK rising edge | 2.5 | | 2.5 | | ns | |
| tCHD | CE# hold time from CLK falling edge | 2.5 | | 2.5 | | ns | |
| tSP | Setup time to active CLK edge | 1.1 | | 1.1 | | ns | |
| tHD | Hold time from active CLK edge | 1.1 | | 1.1 | | ns | |
| tRBXwait | Row Boundary Crossing Wait Time | 30 | 65 | 30 | 65 | ns | |
| tHZ | Chip disable to DQ/DQS output high-Z | | 6 | | 6 | ns | |
| tRC | Write Cycle | 60 | | 60 | | ns | |
| tRC | Read Cycle | 60 | | 60 | | ns | |
| tPU | Device Initialization | 150 | | 150 | | µs | |
| tRP | RESET# low pulse width | 1 | | 1 | | µs | |
| tRST | Reset to CMD valid | 2 | | 2 | | µs | |


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**Table 29: DDR timing parameters**

| | | -7 (133MHz) | | -9 (109MHz) | | | |
|---|---|---|---|---|---|---|---|
| ***Symbol*** | ***Parameter*** | ***Min*** | ***Max*** | ***Min*** | ***Max*** | ***Unit*** | ***Notes*** |
| tCQLZ | Clock rising edge to DQS low | 1 | 6 | 1 | 6 | ns | |
| tDQSCK | DQS output access time from CLK | 2 | 5.5 | 2 | 5.5 | ns | |
| tDQSQ | DQS – DQ skew | | 0.6 | | 0.6 | ns | |
| tDS | DQ and DM input setup time | 1.1 | | 1.1 | | ns | |
| tDH | DQ and DM input hold time | 1.1 | | 1.1 | | ns | |
| tHP | Half Period | = min (tCH, tCL) | | | | ns | |
| tQHS | Datahold skew factor | | 0.75 | | 0.9 | ns | |
| tQH | DQ output hold time from DQS | = tHP - tQHS | | | | ns | |


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# 9 Change Log

| Version | Date | Description |
|---|---|---|
| 1.0 | Nov 07, 2019 | Initial Version from E3 -3OBM v3.4 |
| 1.1 | Nov 14, 2019 | Updated notes in section 7.5, Table 15, Table 17 and Table 28 |
| 1.1a | Nov 20, 2019 | Updated typo in header, section 4, 8.2 and 8.3 |
| 1.1b | Dec 14, 2019 | Revised typo |


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