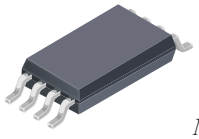
# A1330

# Programmable Angle Sensor IC with Analog and PWM Output

## FEATURES AND BENEFITS

- Contactless 0° to 360° angle sensor IC, for angular position, rotational speed, and direction measurement
- Single and dual die options available in same package
- Non-volatile memory (EEPROM) for use in application trimming/calibration
- Circular Vertical Hall (CVH) technology provides a single-channel sensor system with air gap independence
- Angle Refresh Rate (output rate) configurable between 25 and 3200 µs through EEPROM programming
- Customer-programmable output clamp levels provide short-circuit diagnostic capabilities
- Open-circuit detection on ground pin (broken wire)
- Undervoltage lockout for $V_{CC}$ below specification
- Fine angle scaling for short-stroke applications
- Missing Magnet Error flag for notifying controller of low magnetic field level
- EEPROM programmable angle reference (0°) position and rotation direction (CW or CCW)
- AEC-Q100 automotive qualified

## PACKAGE: 8-pin TSSOP (LE package)



*Not to scale*

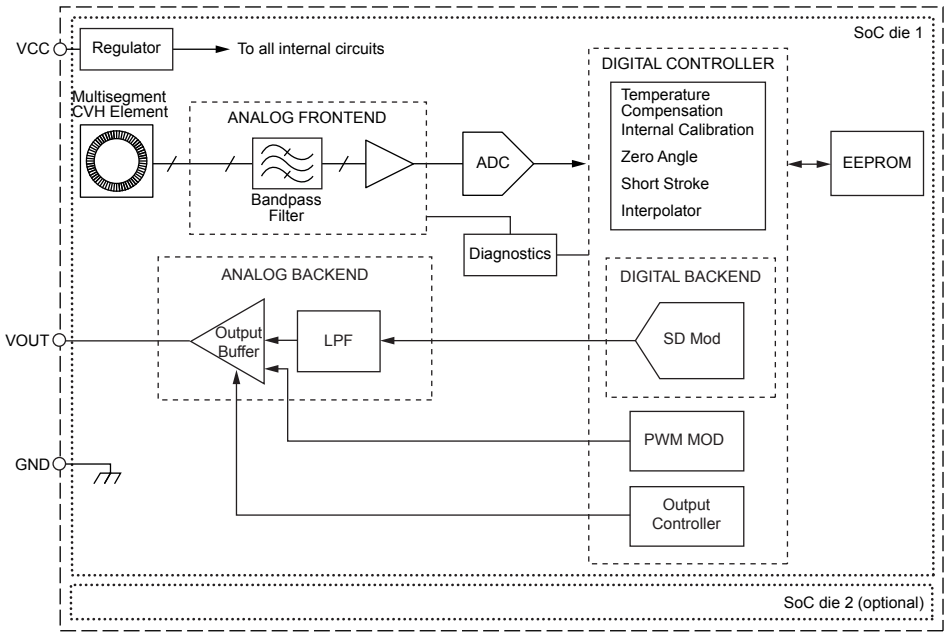
## DESCRIPTION

The A1330 is a 360° angle sensor IC that provides contactless high-resolution angular position information based on magnetic Circular Vertical Hall (CVH) technology. It has a system-on-chip (SoC) architecture that includes: a CVH front end, digital signal processing, and an analog output driver. It also includes on-chip EEPROM technology, capable of supporting up to 100 read/write cycles, for flexible end-of-line programming of calibration parameters. Broken ground wire detection and user-selectable output voltage clamps make the A1330 ideal for high-reliability applications requiring high-speed 0° to 360° angle measurements.

The A1330 provides adjustable internal averaging, allowing response time to be traded for resolution. This is ideal for applications operating at low rotational velocities requiring high precision. For higher RPM applications, the A1330 provides industry-leading analog response time when no averaging is enabled.

With programmable angle scaling, the A1330 supports applications requiring short angular displacements, while maintaining full dynamic range on the output. Programmable minimum and maximum angle thresholds allow diagnosis of mechanical failures.

The A1330 is available as either a single or dual die option, in an 8-pin TSSOP. The package is lead (Pb) free with 100% matte-tin leadframe plating.




**Functional Block Diagram**


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Tel:150-1290-5940
Email:sales@manduic.com
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## SELECTION GUIDE

| Part Number | Application | Number of Die | Package | Packing [1] |
|---|---|---|---|---|
| A1330LLETR-T | Analog Output | Single Die | 8-pin TSSOP | 4000 pieces per 13-inch reel |
| A1330LLETR-P-T | PWM Output | Single Die | | |
| A1330LLETR-DD-T | Analog Output | Dual Die | | |
| A1330LLETR-P-DD-T | PWM Output | Dual Die | | |
| A1330LLETR-T-C02 | Analog Output [2] | Single Die | | |

[1] Contact Allegro™ for additional packing options.
[2] Increased Angle averaging and Analog hysteresis settings for reduced angle noise.

## ABSOLUTE MAXIMUM RATINGS

| Characteristic | Symbol | Notes | Rating | Unit |
|---|---|---|---|---|
| Forward Supply Voltage | $V_{CC}$ | Not sampling angles | 26.5 | V |
| Reverse Supply Voltage | $V_{RCC}$ | Not sampling angles | –18 | V |
| Forward Output Voltage | $V_{OUT}$ | $V_{OUT} < V_{CC} + 2$ V | 16 | V |
| Reverse Output Voltage | $V_{ROUT}$ | | 0.5 | V |
| Operating Ambient Temperature | $T_A$ | L range | –40 to 150 | °C |
| Maximum Junction Temperature | $T_J$(max) | | 165 | °C |
| Storage Temperature | $T_{stg}$ | | –65 to 170 | °C |

## THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

| Characteristic | Symbol | Test Conditions* | Value | Unit |
|---|---|---|---|---|
| Package Thermal Resistance | $R_{\theta JA}$ | LE-8 single die package | 145 | °C/W |
| | | LE-8 dual die package | 277 | °C/W |

*Additional thermal information available on the Allegro website.



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Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

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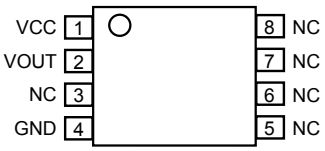
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## PINOUT DIAGRAMS AND TERMINAL LIST TABLES

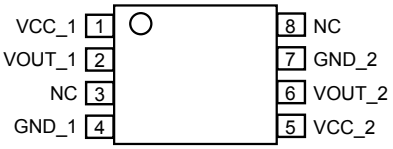



**LE-8 Package Pinout (single die)**

### Terminal List Table (Single Die)

| Pin Name | Pin Number | Function |
|---|---|---|
| VCC | 1 | Device power supply. Serves as Manchester communication input pin. |
| VOUT | 2 | Angle output (analog or PWM). Manchester output during serial communication.<br>Input for EEPROM programming pulses. |
| NC* | 3,5,6,7,8 | Not connected; connect to ground for optimal ESD performance |
| GND | 4 | Ground |

* NC pins must be tied to GND for optimum ESD performance.




**LE-8 Package Pinout (dual die)**

### Terminal List Table (Dual Die)

| Pin Name | Pin Number | Function |
|---|---|---|
| VCC_1 | 1 | Device power supply. Serves as Manchester communication input pin. (die 1) |
| VOUT_1 | 2 | Angle output (analog or PWM). Manchester output during serial communication.<br>Input for EEPROM programming pulses. (die 1) |
| NC* | 3, 8 | Not connected; connect to ground for optimal ESD performance |
| GND_1 | 4 | Ground (die 1) |
| VCC_2 | 5 | Device power supply. Serves as Manchester communication input pin. (die 2) |
| VOUT_2 | 6 | Angle output (analog or PWM). Manchester output during serial communication.<br>Input for EEPROM programming pulses. (die 2) |
| GND_2 | 7 | Ground (die 2) |

* NC pins must be tied to GND for optimum ESD performance.



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955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

**OPERATING CHARACTERISTICS: Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted**

| Characteristics | Symbol | Test Conditions | | Min. | Typ. | Max. | Unit [1] |
|---|---|---|---|---|---|---|---|
| **ELECTRICAL CHARACTERISTICS** | | | | | | | |
| Supply Voltage [2] | $V_{CC}$ | | | 4.5 | – | 5.5 | V |
| Supply Current | $I_{CC}$ | One die, analog output, unloaded output | $T_A \geq 25°C$ | – | 12 | 15 | mA |
| | | | $T_A < 25°C$ | – | 12.6 | 16 | mA |
| | | One die, PWM output, unloaded output | | – | 8.5 | 10 | mA |
| Undervoltage Lockout Threshold Voltage [3] | $V_{UVLO(H)}$ | Maximum $V_{CC}$, dV/dt = 1 V/ms, $T_A$ = 25°C, A1330 sampling enabled, rising $V_{CC}$ | | – | – | 4.65 | V |
| | $V_{UVLO(L)}$ | Maximum $V_{CC}$, dV/dt = 1 V/ms, $T_A$ = 25°C, A1330 sampling disabled, falling $V_{CC}$ | | 3.9 | – | 4.5 | V |
| Undervoltage Lockout Threshold Hysteresis | $V_{UVLO(HYS)}$ | dV/dt = 1 V/ms, $T_A$ = 25°C | | – | 180 | – | mV |
| Overvoltage Lockout Threshold Voltage | $V_{OVLO(H)}$ | Maximum $V_{CC}$, dV/dt = –1 V/ms, $T_A$ = 25°C, A1330 sampling disabled | | – | 6.3 | – | V |
| | $V_{OVLO(L)}$ | Maximum $V_{CC}$, dV/dt = 1 V/ms, $T_A$ = 25°C, A1330 sampling enabled | | 5.5 | 5.9 | – | V |
| Overvoltage Lockout Threshold Hysteresis | $V_{OVLO(HYS)}$ | dV/dt = –1 V/ms, $T_A$ = 25°C | | – | 450 | – | mV |
| Supply Zener Clamp Voltage | $V_{ZSUP}$ | $I_{CC} = I_{CC}$ + 3 mA, $T_A$ = 25°C | | 26.5 | – | – | V |
| Reverse-Battery Current | $I_{RCC}$ | $V_{RCC}$ = 18 V, $T_A$ = 25°C | | – | – | 5 | mA |
| Power-On Time [4] | $t_{PO}$ | | | – | 300 | – | µs |
| **ANALOG OUTPUT CHARACTERISTIC** | | | | | | | |
| DC Output Resistance [4] | $R_{OUT}$ | | | – | 1 | – | Ω |
| Output Load Resistance [4] | $R_L$ | VOUT to VCC | | 4.7 | – | – | kΩ |
| | | VOUT to GND | | 4.7 | – | – | kΩ |
| Output Current Limit | $I_{LIMIT}$ | Minimum output, shorted to 5 V | | 24 | 29 | 34 | mA |
| | | Maximum output, shorted to GND | | – | 3 | – | mA |
| Output Load Capacitance [4] | $C_{OUT}$ | | | – | – | 10 | nF |
| Broken Wire Voltage | $V_{BRK(H)}$ | $T_A$ = 25°C, $R_{L(PU)}$ = 10 kΩ to VCC | | – | $V_{CC}$ | – | V |
| | $V_{BRK(L)}$ | $T_A$ = 25°C, $R_{L(PD)}$ = 10 kΩ to GND | | – | 130 | – | mV |
| Output Slew Rate | SR | 10 kΩ pull-up | | – | 100 | – | V/ms |
| DAC Output Noise [4] | $A_{NOISE}$ | DAC output, excluding angle measurement noise, 30 kHz BW setting | | – | – | 15 | $mV_{p-p}$ |
| | | DAC output, excluding angle measurement noise, 15 kHz BW setting | | – | – | 10 | $mV_{p-p}$ |
| Average DAC Resolution [4] | Res(avg) | Across entire code range, theoretical noise-free input, 30 kHz BW | | – | 12 | – | bits |
| Output Ratiometry Error [4] | $Rat_{ERROR}$ | | | – | <±1 | – | % |
| Analog Drift | $\lvert V_{DRIFT} \rvert$ | Absolute change in analog output from 25°C to 150°C | | – | 10 | 30 | mV |
| | | Absolute change in analog output from 25°C to –40°C | | – | 10 | – | mV |

*Continued on the next page…*



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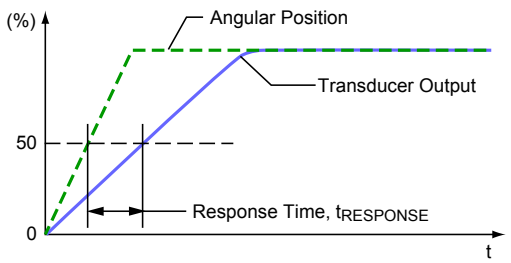
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Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
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**OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted**

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit [1] |
|---|---|---|---|---|---|---|
| **ANALOG OUTPUT CHARACTERISTIC (continued)** | | | | | | |
| Output Saturation Voltage | $V_{OUT(MAX)}$ | Max input angle position; $V_{CC}$ = 5 V, HIGH_CLAMP = 0 | 4.65 | 4.75 | – | V |
| | $V_{OUT(MIN)}$ | 0° input angle position; $V_{CC}$ = 5 V, HIGH_CLAMP = 0 | – | 0.25 | 0.35 | V |
| **OUTPUT CLAMP PROGRAMMING** | | | | | | |
| Clamp High [4] | $V_{CLAMP(H)}$ | Valid for Analog or PWM output, EEPROM programmable | 32 | – | 95 | % $V_{CC}$ or DC |
| Clamp Low [4] | $V_{CLAMP(L)}$ | Valid for Analog or PWM output, EEPROM programmable | 5 | – | 68 | % $V_{CC}$ or DC |
| **PWM INTERFACE SPECIFICATIONS** | | | | | | |
| PWM Carrier Frequency [4] | $f_{PWM}$ | Programmable, 3 bit field | 156.25 | 1250 | 20,000 | Hz |
| Output Current Limit | $I_{LIMIT}$ | Minimum output, shorted to 5 V | 24 | 29 | 34 | mA |
| Pull-up Load [5] | $R_L$ | | 4.7 | – | – | kΩ |
| PWM Duty Cycle Minimum [4] | $D_{PWM(MIN)}$ | LOW_CLAMP = 0 | – | 5 | – | % |
| PWM Duty Cycle Maximum [4] | $D_{PWM(MAX)}$ | HIGH_CLAMP = 0 | – | 95 | – | % |
| **MAGNETIC CHARACTERISTICS** | | | | | | |
| Magnetic Field | B | Range of input field | – | – | 1200 | G |
| **ANGLE CHARACTERISTICS** | | | | | | |
| Output [5] | $RES_{ANGLE}$ | | – | 12 | – | bit |
| Angle Refresh Rate [6] | $t_{ANG}$ | ANG_AVE = 0 | – | 25 | – | µs |
| Response Time [4] | $t_{RESPONSE}$ | ANG_AVE = 0 | – | 120 | – | µs |
| | | ANG_AVE = 3 | – | 200 | – | µs |
| Temperature Drift | $ANGLE_{DRIFT}$ | Angle change from 25°C; $T_A$ = 150°C, B = 300 G | –1.8 | 0.5 | 1.8 | degrees |
| | | Angle change from 25°C; $T_A$ = –40°C, B = 300 G | – | 0.8 | – | degrees |
| Angle Error | $ERR_{ANG}$ | $T_A$ = 25°C, ideal magnet alignment, B = 300 G | –1.1 | ±0.4 | 1.1 | degrees |
| | | $T_A$ = 150°C, ideal magnet alignment, B = 300 G | –1.5 | ±0.5 | 1.5 | degrees |
| Angle Noise | $N_{ANG}$ | $T_A$ = 25°C, B = 300 G, no internal filtering, target rpm = 0, 3 sigma, PWM output | – | ±0.6 | – | degrees |
| | | $T_A$ = 150°C, B = 300 G, no internal filtering, target rpm = 0, 3 sigma, PWM output | – | ±0.75 | – | degrees |
| Angle Drift Over Lifetime [7] | $ANGLE_{DRIFT_LIFE}$ | B = 300 G, typical angle drift observed following AEC-Q100 qualification testing | – | ±0.5 | – | degrees |

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] Operation guaranteed down to 4.5 V, once $V_{CC}$ has risen above 4.65 V.
[3] At power-on, the sensor IC will not respond to commands until $V_{CC}$ rises above $V_{UVLO(H)}$. After that, the sensor IC will perform and respond normally until $V_{CC}$ drops below $V_{UVLO(L)}$.
[4] Parameter is not guaranteed at final test. Values for this characteristic are determined by design.
[5] $RES_{ANGLE}$ represents the number of bits of internal angle information available.
[6] The rate at which a new angle reading will be ready.
[7] Maximum of 1.0 degree increase in angle error observed following AEC-Q100 stress.




**Definition of Response Time**



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955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
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Tel:150-1290-5940
Email:sales@manduic.com

## TYPICAL PERFORMANCE CHARACTERISTICS

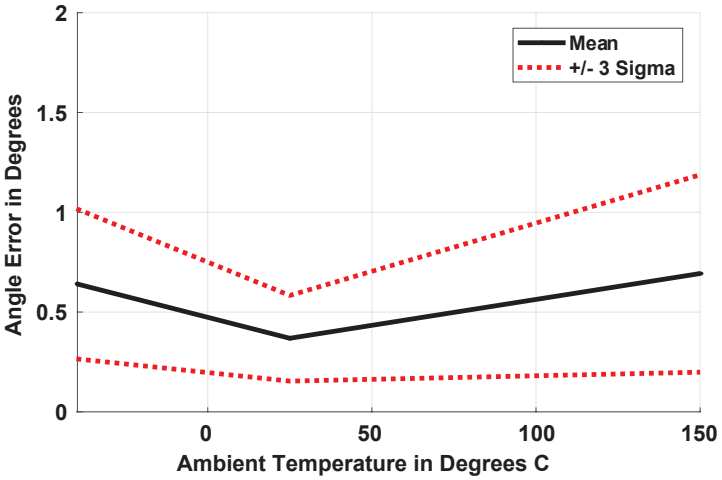



**Figure 1: Peak Angle Error over Temperature (300 G)**

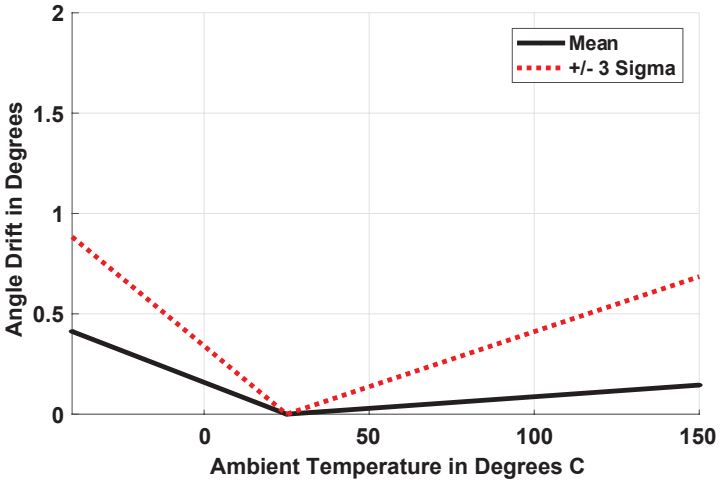



**Figure 2: Maximum Absolute Drift from 25°C Reading (300 G)**

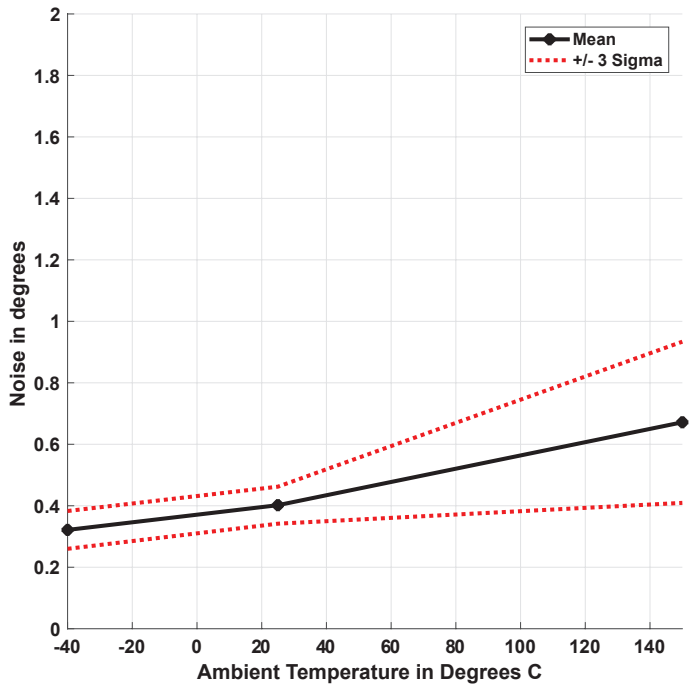



**Figure 3: Noise Performance over Temperature (3 Sigma, 300 G, no internal filtering, Analog Output, 1 nF output capacitance)**

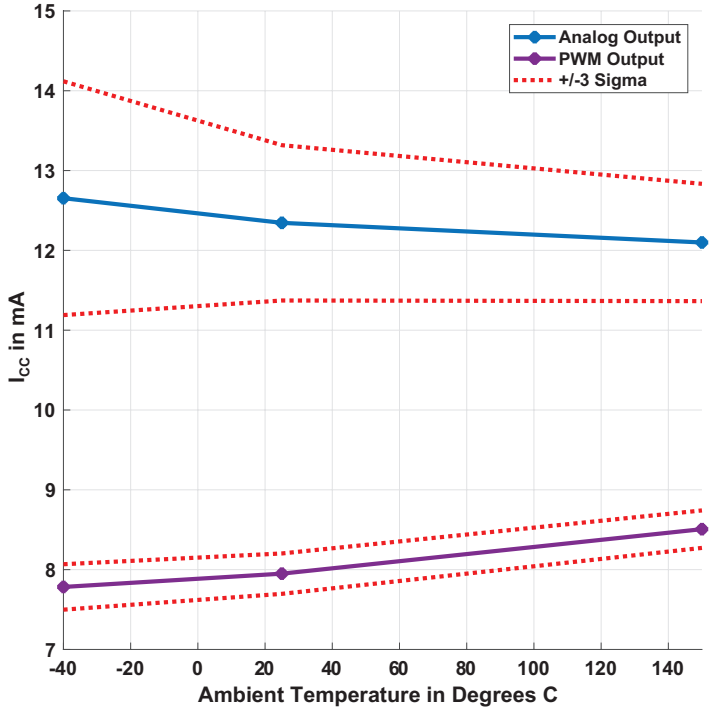



**Figure 4: $I_{CC}$ over Temperature ($V_{CC}$ = 5.0 V)**



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www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

## FUNCTIONAL DESCRIPTION

### Operational Modes

The A1330 is a rotary position Hall-effect-based sensor IC. The sensor IC measures the direction of the magnetic field vector through 360° in the x-y plane (parallel to the branded face of the device) and computes an angle measurement based on the actual physical reading, as well as any internal parameters that have been set by the user.

The device is a programmable system-on-chip (SoC). The integrated circuit includes a Circular Vertical Hall (CVH) analog front end, a high-speed sampling A-to-D converter, digital filtering, digital signal processing, and a high-speed Digital-to-Analog converter.

Internal averaging may be enabled to improve signal resolution.

Advanced offset and gain adjustment options are available in the A1330. These options can be configured in the onboard EEPROM, providing a wide range of sensing solutions in the same device. Device performance can be optimized by enabling individual functions or disabling them in EEPROM to minimize latency.

### Angle Measurement

The A1330 can monitor the angular position of a rotating magnet at speeds ranging from 0 to more than 7,000 rpm.

The raw angle data is received in a periodic stream, and several samples may be accumulated and averaged, based on a user-selected EEPROM field. This feature increases the effective resolution of the system. The amount of averaging is determined by the user-programmable ANG_AVE field. The user can configure the quantity of averaged samples by powers of two to determine the refresh rate, the rate at which successive averaged angle values are fed into the post-processing stages. The available rates are set as follows:

| ANG_AVE [2:0] | Quantity of Samples Averaged | Refresh Rate (µs) |
|---|---|---|
| 000 | 1 | 25 |
| 001 | 2 | 50 |
| 010 | 4 | 100 |
| 011 | 8 | 200 |
| 100 | 16 | 400 |
| 101 | 32 | 800 |
| 110 | 64 | 1600 |
| 111 | 128 | 3200 |

### Short Stroke

Short stroke (or fine angle scaling) allows for magnetic angle rotations smaller than 360 degrees to be represented by full-scale deflection. This feature is enabled in “Short Stroke” mode. In this mode, the raw angle reading is scaled via a programmable GAIN setting. Minimum and maximum angle thresholds may be programmed to detect hardware malfunctions. When a raw angle greater than the maximum angle threshold is detected, the sensor output will tri-state, alerting the host microprocessor of an unexpected condition. Programmable Clamp_High and Clamp_Low settings allow the maximum or minimum output level to be customizable.

### Output Types

The A1330 is set at Allegro factory for either analog or PWM output.

#### ANALOG OUTPUT

The A1330LLETR-T and A1330LLETR-D-T feature an analog output, proportional to a 12-bit digital angle value. Angles 0.0 through 359.9 degrees are mapped to voltages between the default $V_{CLAMPL}$ and default $V_{CLAMPH}$. The output voltage will increase linearly, between the clamp settings when a linearly increasing magnetic angle is detected.

Voltage values beyond the upper or lower clamps represent diagnostic regions. Output voltages within these two regions will only occur if the device detects an abnormal operating condition or internal error.

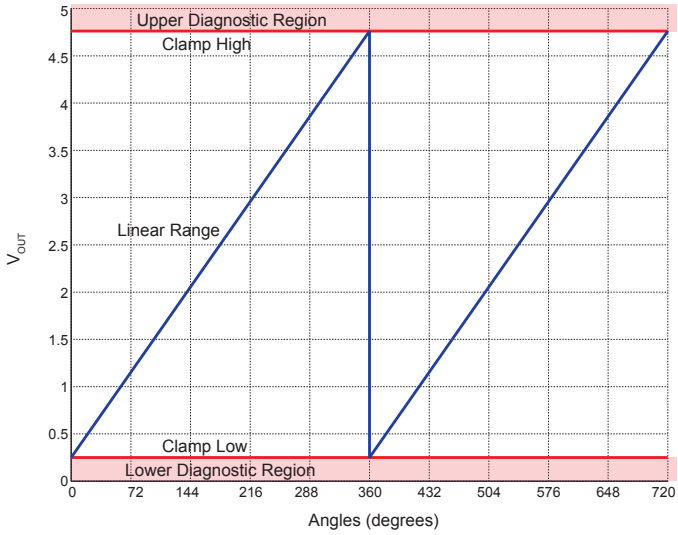



**Figure 5: Output Value for a 0-720° Magnetic Input Signal**



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## BACKEND DAC BW

The bandwidth of the backend analog filter is adjustable in EEPROM between two settings.

| ABW | DAC Bandwidth |
|---|---|
| 0 | 30 kHz |
| 1 | 15 kHz |

The default setting of 30 kHz is recommended for most applications, providing a good balance between low noise and fast response time. For applications especially sensitive to noise, it is recommend to choose the 15 kHz option and use the internal digital averaging to further reduce front end noise.

## PWM OUTPUT

The A1330LLETR-P-T and A1330LLETR-P-DD-T provide a pulse-width-modulated open-drain output, with the duty cycle (D) proportional to measured angle. The PWM duty cycle is clamped at 5% and 95% by default and may be adjusted further for diagnostic purposes.

A 5% D corresponds to 0°; a 95% D corresponds to 360°.

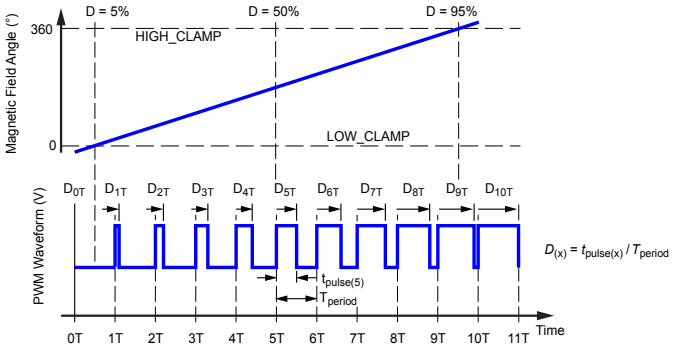



**Figure 6: PWM Mode Outputs a Duty Cycle Proportional to Sensed Angle**

Angle is represented in 12-bit resolution and can never reach a full 360° (0° and 360° are the same physical position). The maximum duty cycle high period with default clamp values is:

$$DutyCycleMax\ (\%) = (4095 / 4096) \times 90 + 5.$$

The derived angle (in degrees) from a given PWM duty cycle is:

$$Angle = (D - 5) / 90 \times 360.$$

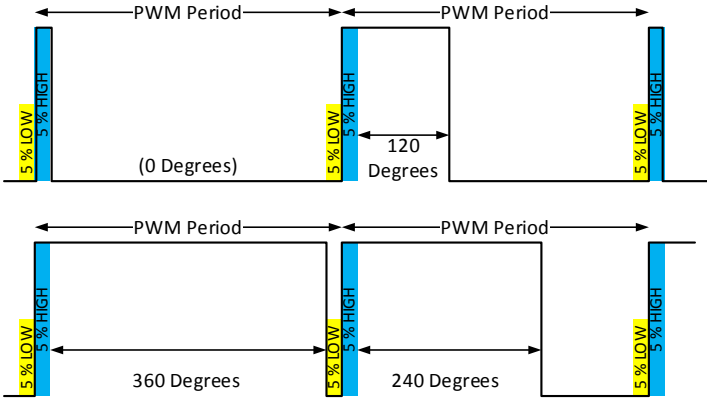



**Figure 7: Pulse-Width Modulation (PWM) Examples**

## PWM CARRIER FREQUENCY

The PWM carrier frequency is controlled via a 3-bit EEPROM field.

| PWM_FREQ | PWM Frequency |
|---|---|
| 000 | 20 kHz |
| 001 | 10 kHz |
| 010 | 5 kHz |
| 011 | 2.5 kHz |
| 100 | 1.25 kHz |
| 101 | 625 Hz |
| 110 | 312.5 Hz |
| 111 | 156.25 Hz |



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ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

## Undervoltage and Overvoltage Lockout

The Output pin state changes according to the $V_{CC}$ level. This is shown in Figure 8, with typical threshold values highlighted. By using a pull-up/pull-down resistor, one is able to know the sensor is in high-impedance, as the output will be beyond the clamp values.

## Hysteresis

The periodic behavior intrinsic to angle sensing results in output voltage swings from minimum to maximum deflection during 0/360 degree crossings. For some applications, this may be problematic, especially if a high-noise environment results in values close to 0 degrees intermittently appearing as 359.9 degrees.

To prevent oscillations between mininimum or maximum output, the A1330 features programmable hysteresis, specified by the 2-bit HYST EEPROM field. When hysteresis is enabled, the output will not change for angle variations smaller than the hysteresis setting.

As an alternate approach, the HYST_0/360 bit may be set in EEPROM, to enable hysteresis only around the 0/360 degree crossing.

Note: Unlike the typical description of ‘Hysteresis”, the implementation used in the A1330 is “two-sided”, meaning the hysteresis gap is independent of rotation direction. This effectively increases the output step size and as a result may not be desired. To apply this filtering method to only angle ranges of importance (in which a 0/360 crossover could occur), the HYST_0/360 bit can be set.

**Table 1: HYST Settings in EEPROM**

| Code | Hysteresis (in LSB) | Angle Equivalent |
|---|---|---|
| 00 | 0 | 0 |
| 01 | 4 | 0.352 |
| 10 | 8 | 0.703 |
| 11 | 16 | 1.406 |

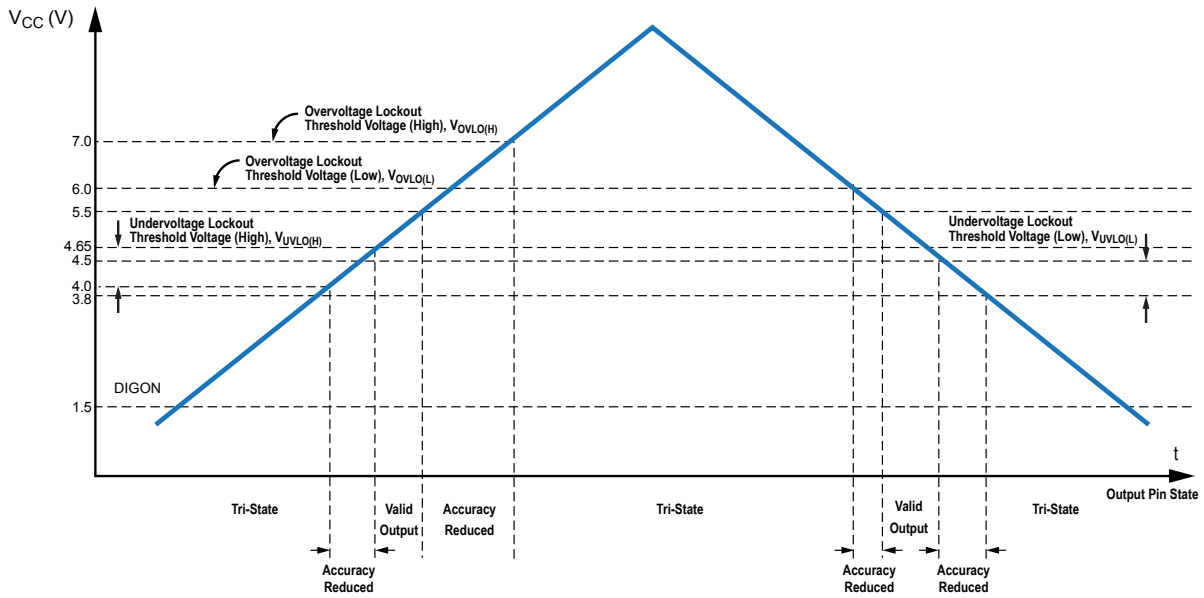



**Figure 8: Relationship of $V_{CC}$ and Output**



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Tel:150-1290-5940
Email:sales@manduic.com

## PROGRAMMING SERIAL INTERFACE

The A1330 incorporates a serial interface that allows an external controller to read and write registers in the A1330 EEPROM and volatile memory. The A1330 uses a point-to-point communication protocol, based on Manchester encoding (a rising edge indicates a 0 and a falling edge indicates a 1), with address and data transmitted MSB first.

### Transaction Types

Each transaction is initiated by a command from the controller; the A1330 does not initiate any transactions. Two commands are recognized by the A1330: Write and Read. There also are three special function Write commands: Write Access Code, Manchester Enable, and Manchester Disable. One response frame type is generated by the A1330, Read Acknowledge.

If the command is a read, the A1330 responds by transmitting the requested data in a Read Acknowledge frame. If the command is a write, the A1330 does not acknowledge.

As shown in Figure 9, The A1330 receives all commands via the VCC pin. It responds to Read commands via the VOUT pin. This implementation of Manchester encoding requires the communication pulses be within a high ($V_{MAN(H)}$) and low ($V_{MAN(L)}$) range of voltages for the VCC line and the VOUT line. The Write command pulses to EEPROM are supported by two high-voltage pulses on the VOUT line.

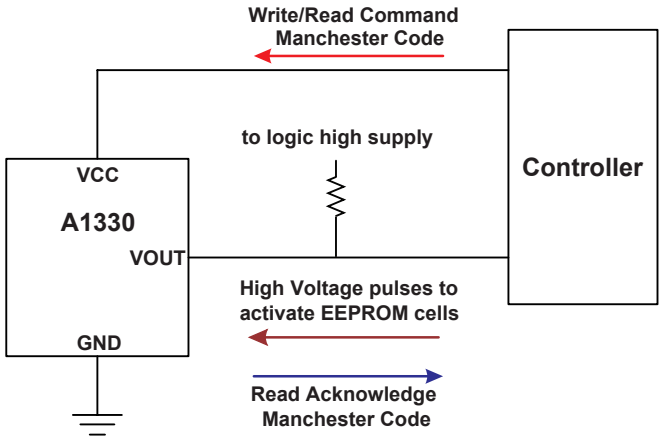



**Figure 9: Top-Level Programming Interface**

### Writing the Access Code

If the external controller will write to or read from the A1330 memory during the current session, it must establish serial communication with the A1330 by sending a Write Access Command within 70 ms after powering up the A1330. If this deadline is missed, all write and read access is disabled until the next power-up.

### Writing to EEPROM

When writing to non-volatile EEPROM, following the write command, the controller must also send two Programming pulses. These pulses are well-separated, long, high-voltage strobes transmitted on the VOUT pin. These strobes are detected internally, allowing the A1330 to boost the voltage on the EEPROM gates. The digital logic will automatically detect an impending EEPROM write and tri-state the output pin.

The required sequence is shown in Figure 12. The voltage pulse profile necessary for EEPROM programming is shown in Figure 10. Minimum and maximum times are described in Table 2.

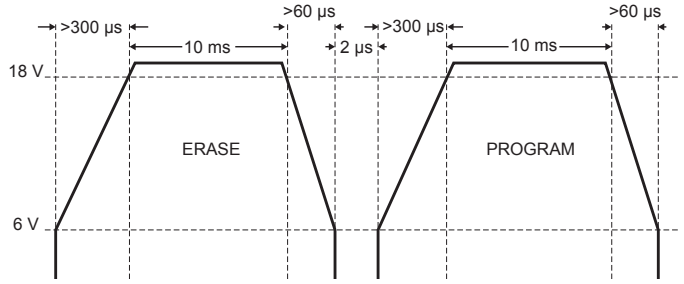



**Figure 10: Top-Level Programming Interface**

**Table 2: EEPROM Pulse**

| Parameter | Comments | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Pulse High Time | Time above minimum pulse voltage | 8 | 10 | 11 | ms |
| Rise Time | 10% to 90% of minimum pulse level | 300 | – | – | µs |
| Fall Time | 10% to 90% of minimum pulse level | 60 | – | – | µs |
| Pulse Voltage | | 18 | 19 | 19.5 | V |
| Separation time | Time between first pulse dropping below 6 V and 2nd pulse rising above 6 V | 2 µs | – | 50 ms | µs/ms |



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www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

## Writing to Volatile Registers

The three main volatile write commands (Write Access, Manchester Enable and Manchester Disable) are all accomplished by writing to register 0x1F.

In addition to these three commands, the PWM output version requires a PWM Disable command be written prior to performing a Manchester read and a PWM Enable command prior to going back to Normal Mode. These two commands are written to register 0x22.

## Reading from EEPROM

To read from EEPROM, the Manchester mode must be entered. This is accomplished by sending the Manchester Enable code on VCC. For PWM parts, an additional PWM Disable command must also be sent.

After the Read Acknowledge frame has been received from the A1330, the controller must send a Manchester Disable command to restore VOUT to normal operation. The required sequence is shown in Figure 12.

## Error Checking

The serial interface uses a cyclic redundancy check (CRC) for data-bit error checking (synchronization bits are ignored during the check).

The CRC algorithm is based on the polynomial

$$g(x) = x^3 + x + 1 \quad ,$$

and the calculation is represented graphically in Figure 11.

The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 111.

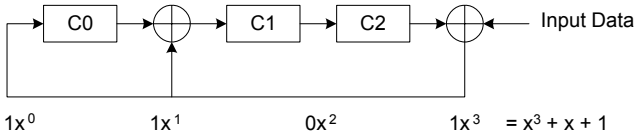



**Figure 11: CRC Calculation**

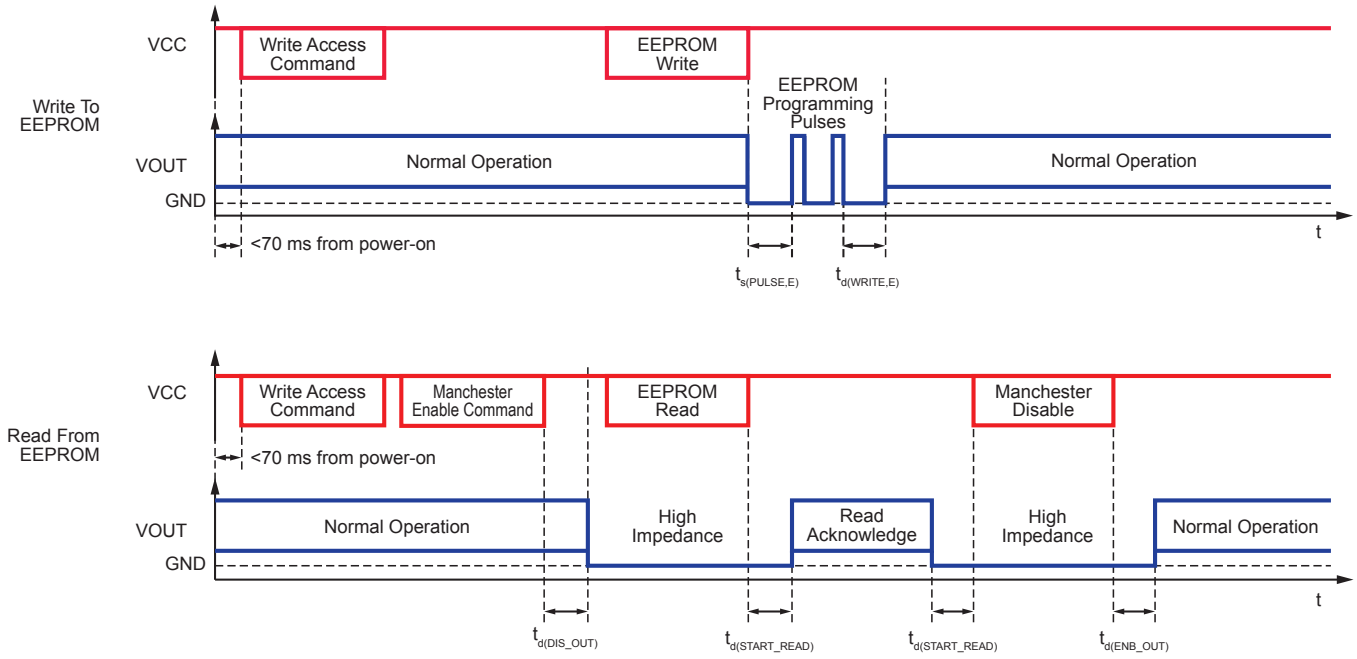



**Figure 12: Programming Read and Write Timing Diagrams**



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955 Perimeter Road
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www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

## SERIAL INTERFACE REFERENCE

**Table 3: Serial Interface Protocol Characteristics [1]**

| Characteristics | Symbol | Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **INPUT/OUTPUT SIGNAL TIMING** | | | | | | |
| Access Code Timeout | $t_{ACC}$ | Customer Access Code should be fully entered in less than $t_{ACC}$, measured from when $V_{CC}$ crosses $V_{CC(UVH)}$ | – | – | 70 | ms |
| Baud Rate | $f_s$ | Defined by the input message bit rate sent from the external controller | 5 | – | 40 | kbps |
| Bit Time Error | $err_{TBIT}$ | Deviation in $t_{BIT}$ during one command frame | –15 | – | +15 | % |
| Read Acknowledge Delay | $t_{d(READ)}$ | Required delay from the trailing edge of a Read Acknowledge frame to the leading edge of a following command frame | 2 × $t_{BIT}$ | – | – | µs |
| Read Delay [2] | $t_{d(START_READ)}$ | Delay from the trailing edge of a Read command frame to the leading edge of the Read Acknowledge frame | – | 2 × $t_{BIT}$ | – | µs |
| Enable Manchester Delay [2] | $t_{d(DIS_OUT)}$ | Delay from the trailing edge of a Manchester Enable command frame to the device output going from normal operation to the high-impedance state | 1 – ¼ × $t_{BIT}$ | 5 – ¼ × $t_{BIT}$ | 15 – ¼ × $t_{BIT}$ | µs |
| Disable Manchester Delay [2] | $t_{d(ENB_OUT)}$ | Delay from the trailing edge of a Manchester Disable command frame to the device output going from the high-impedance state to normal operation | 1 – ¼ × $t_{BIT}$ | 5 – ¼ × $t_{BIT}$ | 15 – ¼ × $t_{BIT}$ | µs |
| **EEPROM PROGRAMMING PULSE** | | | | | | |
| EEPROM Programming Pulse Setup Time | $t_{s(PULSE,E)}$ | Delay from last bit cell of write command to start of EEPROM programming pulse | 2 × $t_{BIT}$ | – | – | µs |
| EEPROM Memory Write Delay | $t_{d(WRITE,E)}$ | Required delay from the trailing edge of the second EEPROM Programming pulse to the leading edge of a following command frame | 40 | – | – | µs |
| **INPUT SIGNAL VOLTAGE** | | | | | | |
| Manchester Code High Voltage | $V_{MAN(H)}$ | Applied to VCC line | 7.3 | – | – | V |
| Manchester Code Low Voltage | $V_{MAN(L)}$ | Applied to VCC line | – | – | 6.3 | V |
| **OUTPUT SIGNAL VOLTAGE (APPLIED ON PWM LINE)** | | | | | | |
| Manchester Code High Voltage | $V_{MAN(H)}$ | Minimum $R_{pullup}$ = 5 kΩ | 0.9 × $V_S$ | – | – | V |
| | | Maximum $R_{pullup}$ = 50 kΩ | 0.7 × $V_S$ | – | – | V |
| Manchester Code Low Voltage | $V_{MAN(L)}$ | 5 kΩ ≤ $R_{pullup}$ ≤ 50 kΩ | – | – | 0.35 | V |

[1] Determined by design.
[2] In the case where a slower baud rate is used, the output responds before the transfer of the last bit in the command message is completed.



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www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

## Serial Interface Message Structure

The general format of a command message frame is shown in Figure 13. Note that, in the Manchester coding used, a bit value of 1 is indicated by a falling edge within the bit boundary, and a bit value of zero is indicated by a rising edge within the bit boundary.

Each command is composed of two zero synchonization bits (“00”) followed by a Read/Write bit, 6 bit address, 32 data bits (only for write commands) and 3 bits of CRC. All field are interpreted MSB first.

The read acknowledged frame is composed of two zero synchronization bits, 32 bits of data, and a 3 bit CRC.

The bits are described in Table 4.

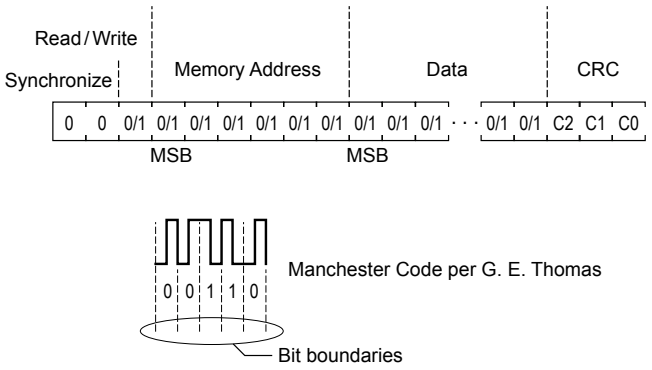



**Figure 13: General Format for Serial Interface Commands**

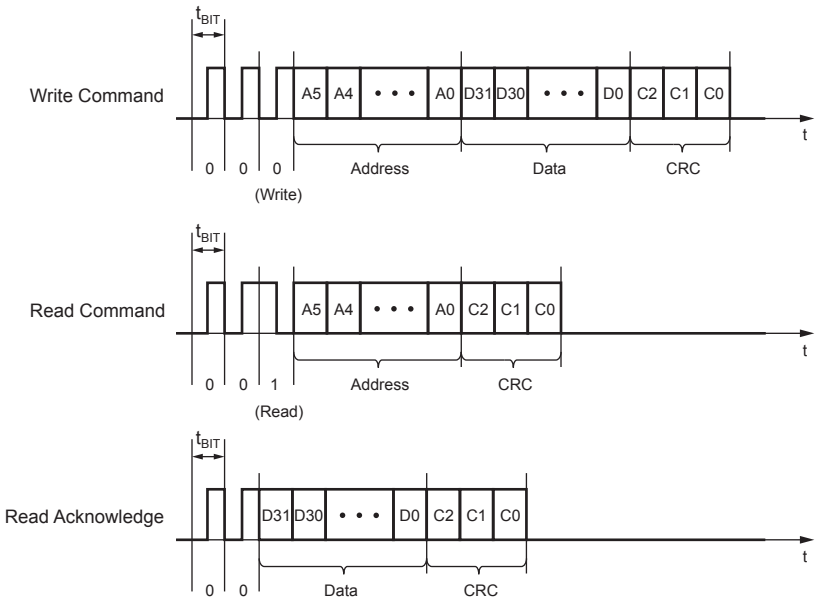



**Figure 14: Manchester Format Example**

**Table 4: Serial Interface Command General Format**

| Quantity of Bits | Name | Values | Description |
|---|---|---|---|
| 2 | Synchronization | 00 | Used to identify the beginning of a serial interface command and communication bit time |
| 1 | Read/Write | 0 | [As required] Write operation |
| | | 1 | [As required] Read operation |
| 6 | Address | 0/1 | [Read/Write] Register address (volatile memory or EEPROM) |
| variable | Data | 0/1 | [As required] 32 bits of data |
| 3 | CRC | 0/1 | Incorrect value indicates errors |



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## Special Access Code Commands

There are two Manchester code commands: a write access code, which initiates serial communication and must be sent within $t_{ACC}$ of power up; and a Disable Output Command, which toggles between mission mode (normal sensor behavior) and Manchester mode, allowing the part to respond to read requests. Both commands are written to volatile register 0x1F.

1. Write Access Code:
   Unlocks the customer address space.
2. Manchester Enable Command:
   Disables sensor output, allowing sensor to respond with a read acknowledge frame.
3. Manchester Disable Command:
   Exits Manchester mode and returns the sensor normal output mode.

The PWM varient requires two additional commands.

1. PWM Disable Code:
   Disables the PWM modulator, allowing Manchester logic to control the open drain output. Must be sent after the Manchester Enable pulse, and prior to a read request.
2. PWM Enable Code:
   Moves control of the output driver back to the PWM logic. Must be sent prior to Manchester Disable command.

**Write Access Code**

| String | ASCII Code (hex) |
|---|---|
| “1330” | 31 33 33 30 |

**Manchester Enable Code**

| String | ASCII Code (hex) |
|---|---|
| “READ” | 52 45 41 44 |

**Manchester Disable Code**

| String | ASCII Code (hex) |
|---|---|
| “EXIT” | 45 58 49 54 |

**PWM Disable Code**

| Address | Hex Code |
|---|---|
| 0x22 | 0x01E6C0D |

**PWM Enable Code**

| Address | Hex Code |
|---|---|
| 0x22 | 0x21E6C0D |



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Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

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Email:sales@manduic.com

## EEPROM Locking

The EEPROM contains an EELOCK bit. When set high, this bit prevents the writing of all EEPROM locations. This is a safety feature guaranteeing EEPROM content integrity during operation in the field.

## Safety Features

Lockout and clamping features protect the A1330 internal circuitry and prevent spurious outputs when the supply voltage is out of specification. Open ground circuit detection is also provided.

## Internal Detection Circuitry

Internal diagnostic circuitry monitors EEPROM ECC to ensure valid system configurations. Magnetic field amplitude is compared against a low field threshold to identify possible hardware malfunctions.

During short stroke mode, minimum and maximum angle values may be specified to identify unexpected behavior and place the output in a safe state.

These diagnostic modes may be disabled with an EEPROM mask bit.

## Detecting Broken Ground Wire

If the GND pin is disconnected, node A becoming broken (Figure 15), the VOUT pin will go to a high-impedance state. Output voltage will go to $V_{BRK(H)}$ if a load resistor $R_{L(PU)}$ is connected to VCC or to $V_{BRK(L)}$ if a load resistor $R_{L(PD)}$ is connected to GND. The device will not respond to a magnetic field.

If the ground wire is reconnected, the A1330 will resume normal operation.

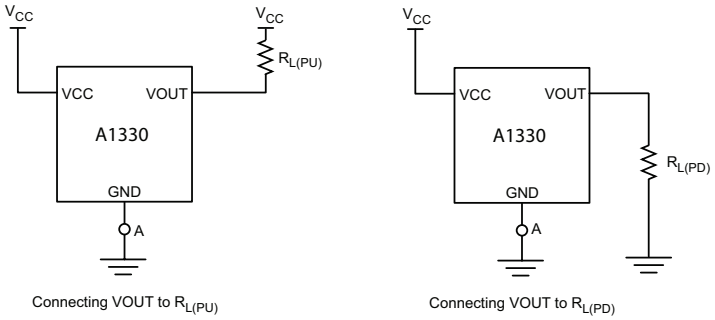



**Figure 15: Connection for Detecting Broken Ground Wire**

**Table 5: Safety Features**

| Diagnostic/Protection | Description | Output State |
|---|---|---|
| Reverse VCC | Current limiting (VCCx pin) | – |
| Output to VCC | Current limiting (VOUT pin) | – |
| Output to Ground | Current limiting (VOUT pin) | – |
| UVLO | $V_{CC}$ below expected range | Tri-state |
| OVLO | $V_{CC}$ above expected range | Tri-state |
| EEPROM dual bit fault | Uncorrectable EEPROM bit fault. Proper device configuration cannot be guaranteed | Tri-state |
| Missing Magnet | Monitors magnet field level in case of mechanical failure (default of 100 G) | Tri-state |
| Angle Out of Range | During short-stroke operation, measured raw angle exceeds maximum specified angular displacement | Tri-state |
| Broken Ground Wire | Broken ground connection | Tri-state: output goes to $V_{BRK(H)}$ or $V_{BRK(L)}$ |
| Digital Interpolation Error | Internal monitor of the DAC interpolation block detects unexpected internal register changes and resets the interpolator | Tri-state |



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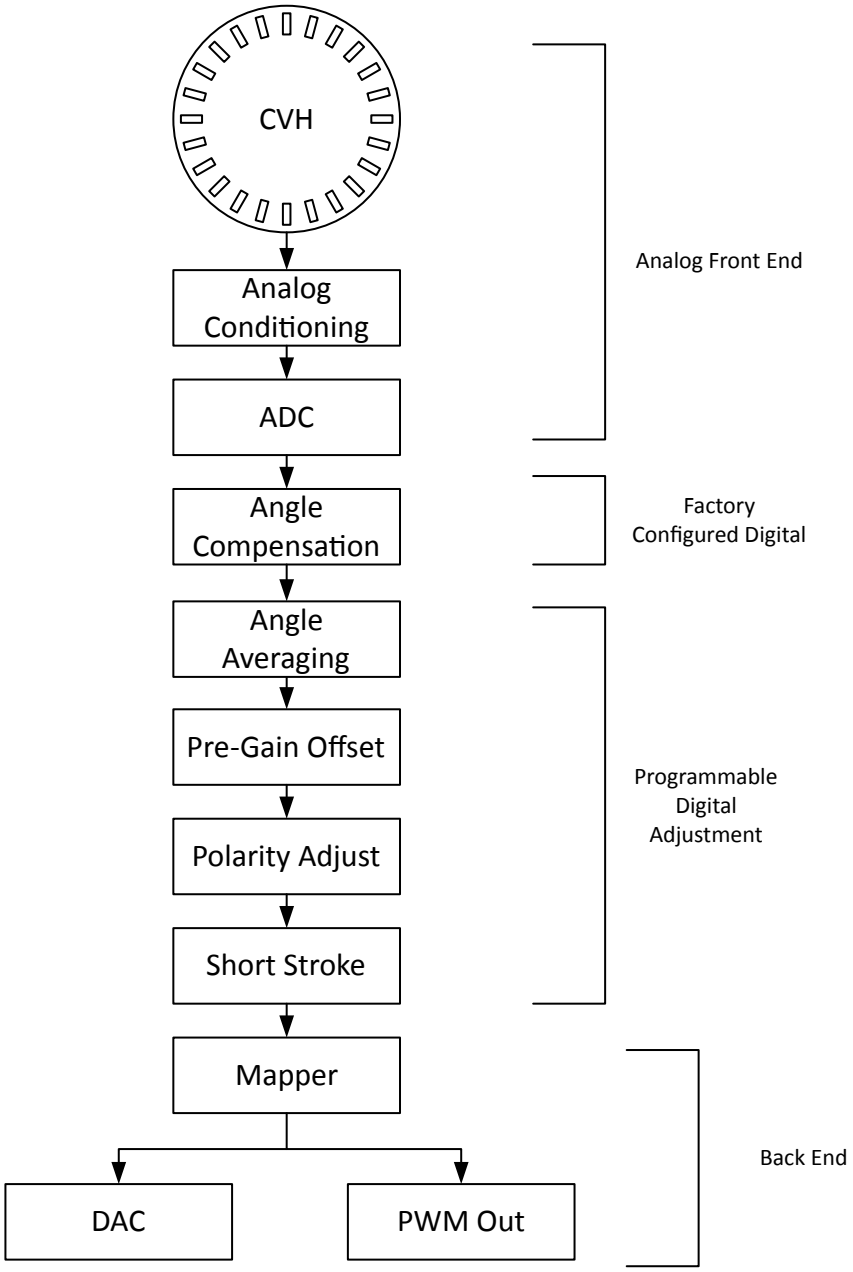



**Figure 16: Digital Signal Path Description**



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www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

## Angle Compensation

The A1330 is capable of compensating for alterations in angle readings that result from changes in the device temperature or applied field strength. The device comes from the factory pre-programmed with coefficient settings to allow compensation of linear shifts of angle with temperature and applied field.

## Angle Averaging

The raw angle data is received in a periodic stream, and multiple samples may be accumulated and averaged, based on the user-programmable ANG_AVE EEPROM field. This feature increases the effective resolution of the system. The user can configure the quantity of averaged samples by powers of two to determine the refresh rate, the rate at which successive averaged angle values are fed into the post-processing stages. The available rates are set as follows:

**Table 6: Refresh Rate based on Averaged Samples**

| ANG_AVE [2:0] | Quantity of Samples Averaged | Refresh Rate (µs) |
|---|---|---|
| 000 | 1 | 25 |
| 001 | 2 | 50 |
| 010 | 4 | 100 |
| 011 | 8 | 200 |
| 100 | 16 | 400 |
| 101 | 32 | 800 |
| 110 | 64 | 1600 |
| 111 | 128 | 3200 |

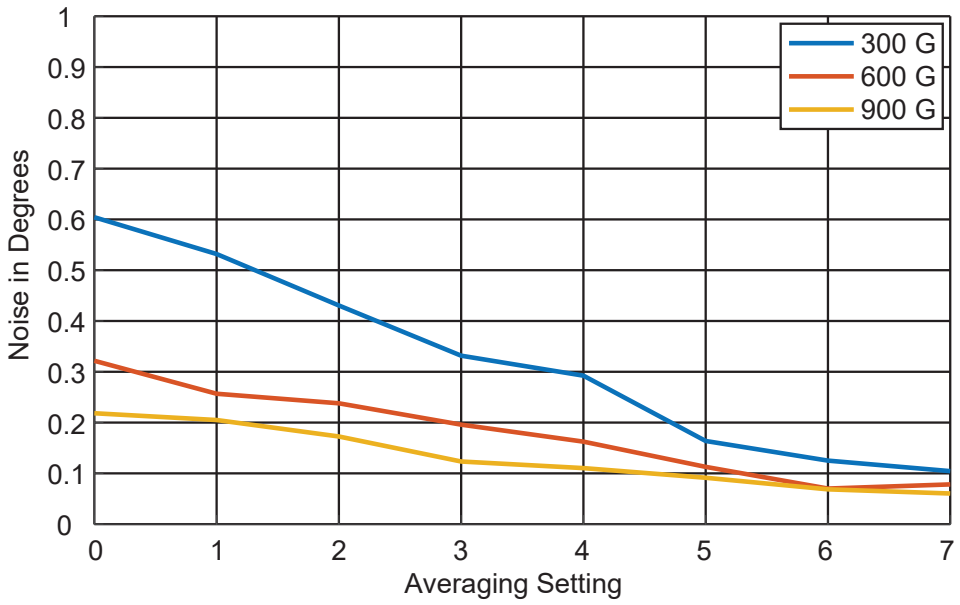



**Figure 17: 3 Sigma Angle Noise Over Averaging Settings. PWM Output, 25°C, Multiple Field Levels.**



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Email:sales@manduic.com

## Pre-Gain Offset

Allows zeroing of the angle prior to applying gain. Set via the PREGAIN_OFFSET field in EEPROM.

$$Angle = Angle - PREGAIN_OFFSET$$

## Polarity Adjust

Sets the polarity of the final angle output. When set to "1", the angle is complemented.

$$Angle = 360° - Angle$$

## Short Stroke

The A1330 features "short stroke" logic allowing a limited input signal to be gained up and use the full output range of the sensor. The short stroke logic consists of multiple steps. A high level block diagram is shown in Figure 18. Short stroke applies to both the PWM and analog output variants.

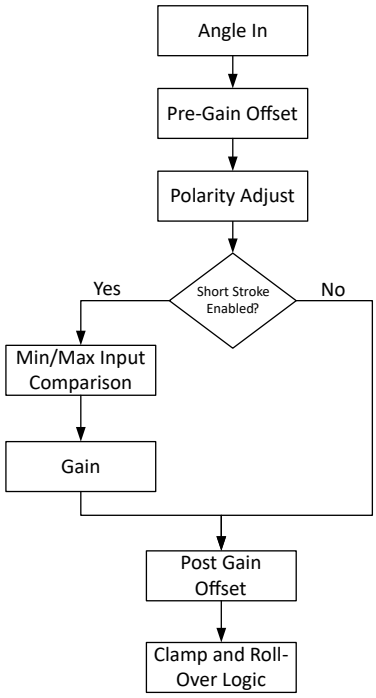



**Figure 18: High Level Short Stroke Block Diagram**



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955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

### MIN/MAX INPUT ANGLE COMPARISON

The IC compares the pre-gained angle value to the boundaries set via the MIN_INPUT and MAX_INPUT EEPROM fields. If the angle is outside of the established boundaries the output will tristate to indicate an unexpected angle location. This feature is useful for applications where clamping is enabled and will otherwise mask excessive angular travel.

### GAIN

Adjusts the output dynamic range of the device. Gain is applied digitally and capable of expanding an 11.25° input angle to a full scale output deflection.

It should be noted that with application of high gain, the front end noise will also be amplified. In such cases it is highly recommend to use the Angle Averaging feature to minimize the impact of noise.

When applying a non-integer gain, an asymetric transfer function will result, causing the output to jump to the minimum allowed output value before reaching the maximum allowed output value. As an example, if a gain of 4× is applied, with Clamp Enable (CE) and Roll-Over Enable (ROE) set to 0, the output angle will slew from 0-360° four times for a single 0-360° target rotation (this is shown in Figure 19 for 2 rotations of the target). However, if a gain of 4.5× is applied, the output will slew from 0-360° four and a half times. This results in a jump from 180° output to 0° output, at the 360° input position (shown in Figure 20).

### POST-GAIN OFFSET

Provides a final, post-gain angle adjustment.

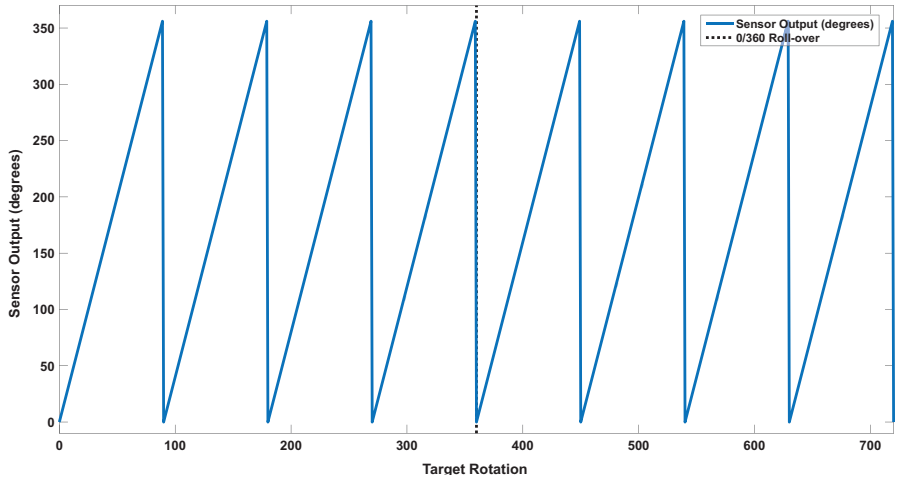



**Figure 19: A1330 Output (in degrees) with 4.0× Gain**

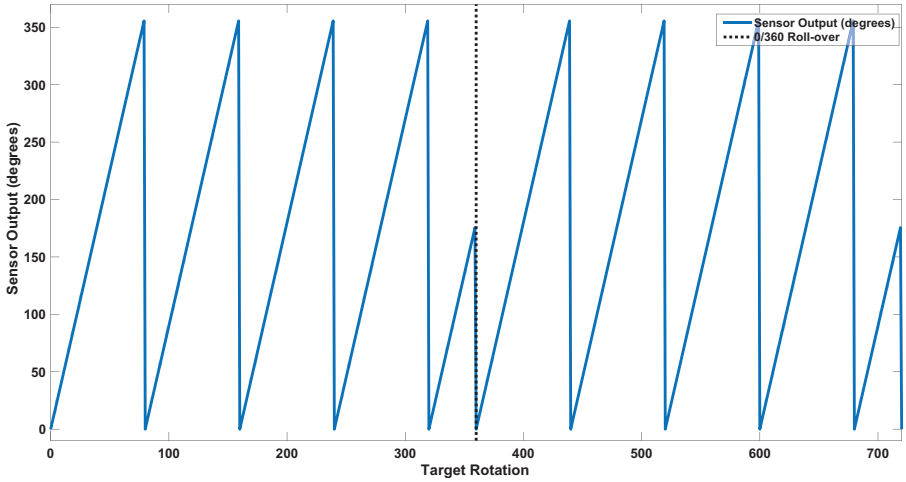



**Figure 20: A1330 Output (in degrees) with 4.5× Gain**



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Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

## Clamp and Roll-Over Logic

Output behavior following gain and offset application is defined by the Clamp Enable (CE) and Roll-Over Enable (ROE) EEPROM bits. Together these two field select between four different output behavior types.

Below are figures depicting the output behavior with different clamp and roll-over settings.

| CE | ROE | Description |
|---|---|---|
| 0 | 0 | Normal behavior.<br>Roll-over at standard module 360. |
| 0 | 1 | Output rolls-over at the High and Low Clamp values. |
| 1 | 0 | Output clamps at the first encountered High/ Low Clamp value. |
| 1 | 1 | Roll-over occurs at standard module 360.<br>Output is clamped to High/Low Clamps value. |

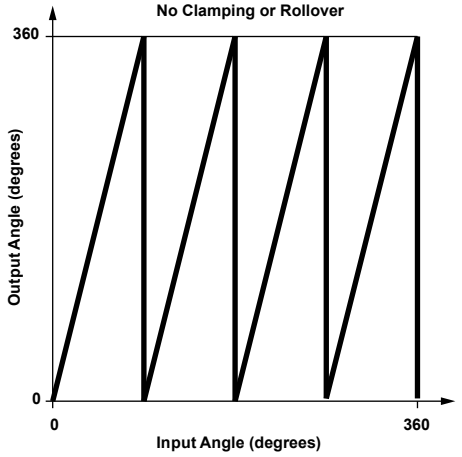



**Figure 21: CE = 0, ROE = 0. Applied gain = 4×.**

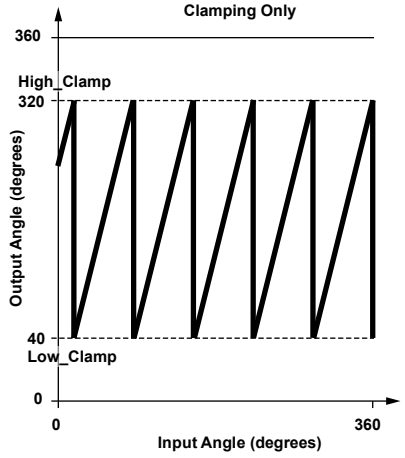



**Figure 23: CE = 0, ROE = 1. Applied gain = 4×. LOW_CLAMP = 10 (≈40°), HIGH_CLAMP = 10 (≈320°)**

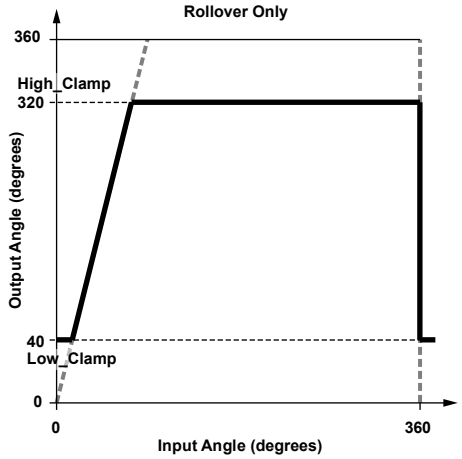



**Figure 22: CE = 1, ROE = 0. Applied gain = 4×. LOW_CLAMP = 10 (≈40°), HIGH_CLAMP = 10 (≈320°)**

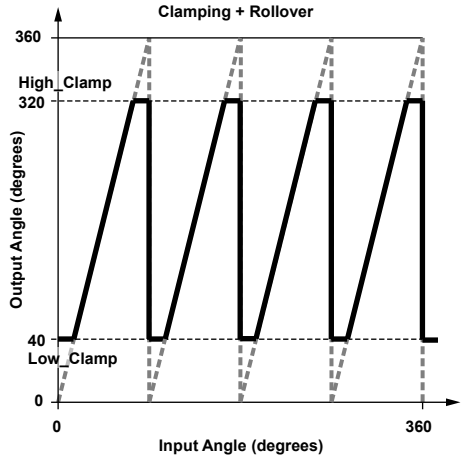



**Figure 24: CE = 1, ROE = 1. Applied gain = 4×. LOW_CLAMP = 10 (≈40°), HIGH_CLAMP = 10 (≈320°)**



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Web:www.manduic.com

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

## Additional Short Stroke Examples

To demonstrate short stroke, several possible scenarios are shown in the following figures.

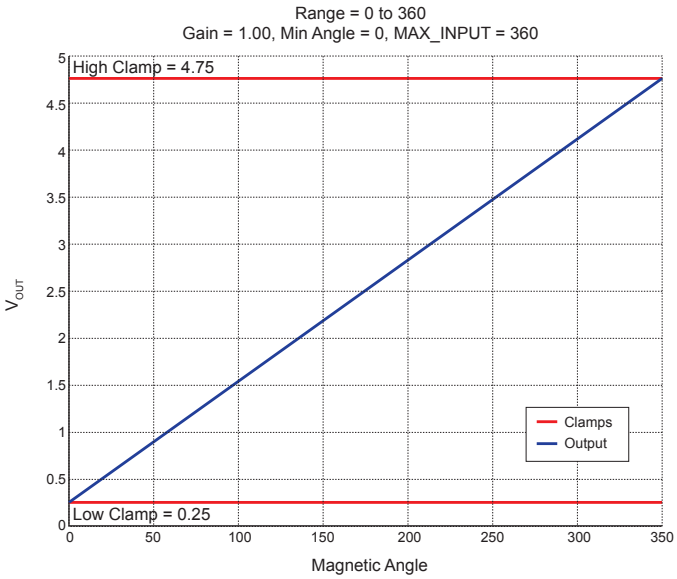



**Figure 25: Scenario A.**
Regular output for a 0-360 degree input angle. Gain = 1. Clamps set to 95% and 5%.

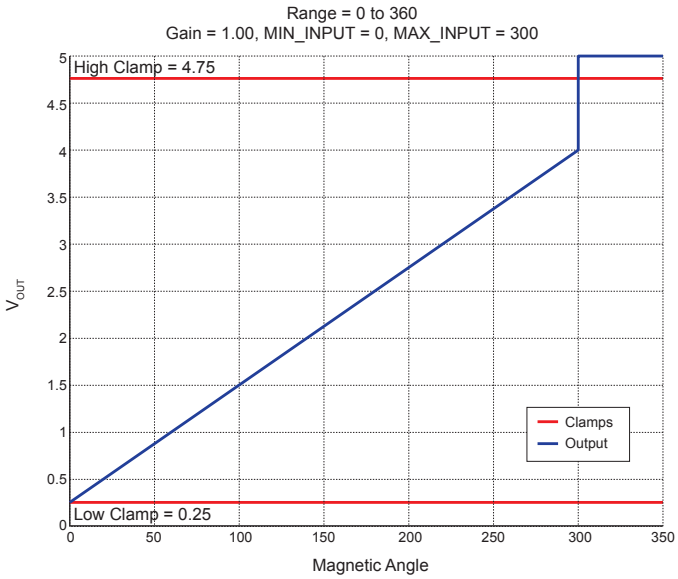



**Figure 26: Scenario B.**
Regular 0-360 degree input value. Gain = 1. MAX_INPUT = 300. Clamps set to 95% and 5%. Output goes into diagnostic region (in this case $V_{CC}$) when input angle exceeds the MAX_INPUT set point.

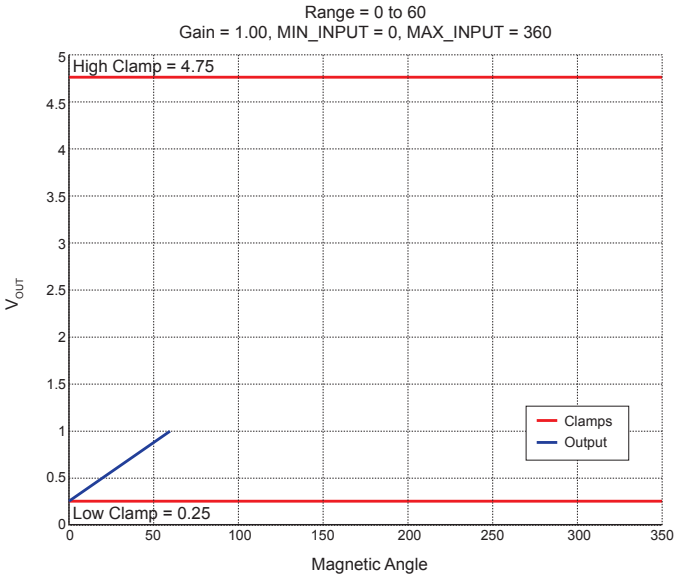



**Figure 27: Scenario C.**
0-60 degree input. Gain = 1. With no gain, a 60-degree input angle results in an output signal 1/6th of $V_{CC}$.

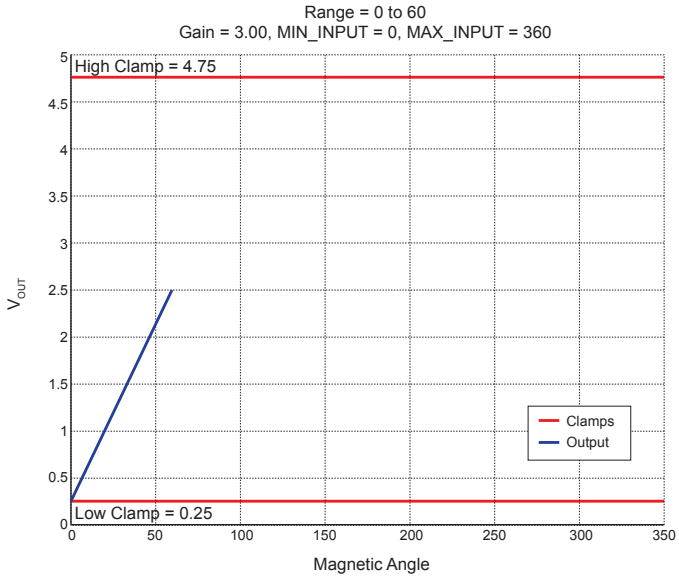



**Figure 28: Scenario D.**
0-60 degree input. Gain = 3. With an increased Gain value of 3×, the same 60-degree input signal now results in 50% of $V_{CC}$. The output signal is still free to swing from 5% to 95% of $V_{CC}$.



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Web:www.manduic.com

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

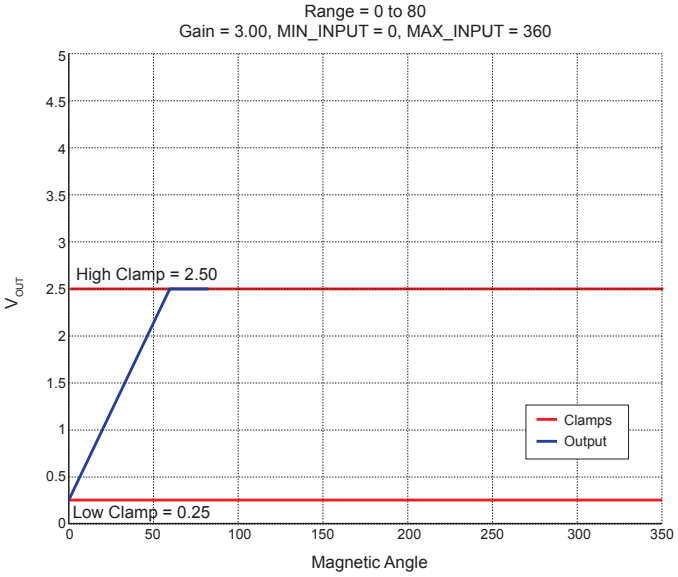



**Figure 29: Scenario E.**
0-80 degree input. Gain = 3.
High Clamp redudduced to 50% of $V_{CC}$.
60-degree input results in 50% output signal. With the reduced upper clamp value, maximum $V_{OUT}$ is 50% of $V_{CC}$. Angle measurements greater than 60 degrees will be clamped to this 50% value.

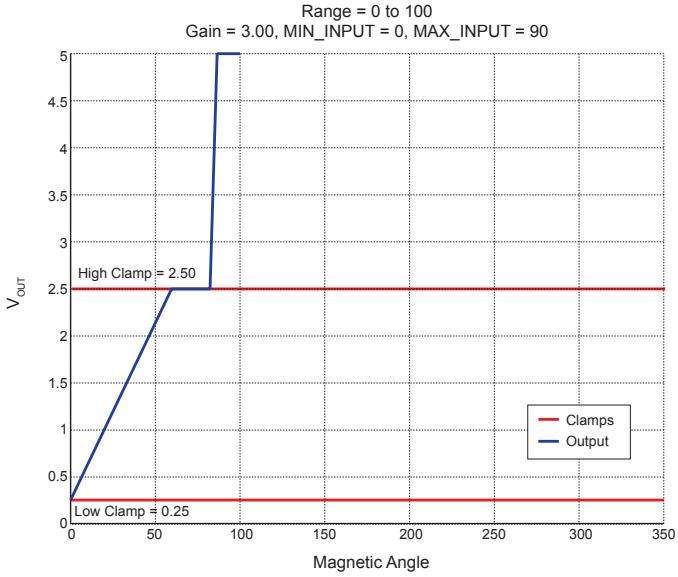



**Figure 30: Scenario F.**
0-100 degree input. Gain = 3. Clamp_High reduced to 50% $V_{CC}$. MAX_INPUT = 90°. Similar to the above scenario, output voltage is clamped at 50% of $V_{CC}$ for any input angle greater than 60 degrees. However, when the input angle exceeds the MAX_INPUT threshold, output voltage goes to diagnostic state ($V_{CC}$). In this example, if the expected input range is 60 degrees, a mechanical failure resulting in 100 degrees of rotation will be detected.



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Web:www.manduic.com

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

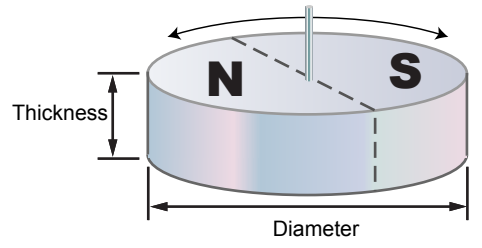
## APPLICATION INFORMATION

### Magnetic Target Requirements

The A1330 is designed to operate with magnets constructed with a variety of magnetic materials, cylindrical geometries, and field strengths, as shown in Table 7. Contact Allegro for more detailed information on magnet selection and theoretical error.

**Table 7: Target Magnet Parameters**

| Magnetic Material | Diameter (mm) | Thickness (mm) |
|---|---|---|
| Neodymium (bonded) | 15 | 4 |
| Neodymium (sintered)* | 10 | 2.5 |
| Neodymium (sintered) | 8 | 3 |
| Neodymium / SmCo | 6 | 2.5 |




*A sintered Neodymium magnet with 10 mm (or greater) diameter and 2.5 mm thickness is the recommended magnet for redundant applications.

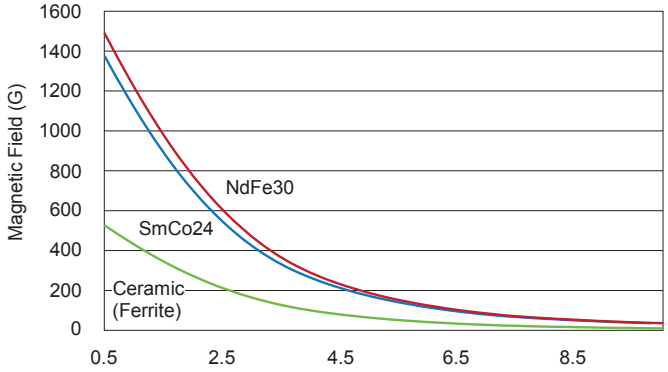



**Figure 31: Magnetic Field versus Air Gap for a magnet 6 mm in diameter and 2.5 mm thick.** Allegro can provide similar curves for customer application magnets upon request. Allegro recommends larger magnets for applications that require optimized accuracy performance.

### Field Strength

The A1330 actively measures and adapts to its magnetic environment. This allows operation throughout a large range of field strengths (recommended range is 300 to 1000 G, operation beyond this range is allowed with no long-term impact). Due to the greater signal-to-noise ratio provided at higher field strengths, performance inherently increases with increasing field strength. Typical angle performance over applied field strength and temperature are shown in Figure 32 and Figure 33.

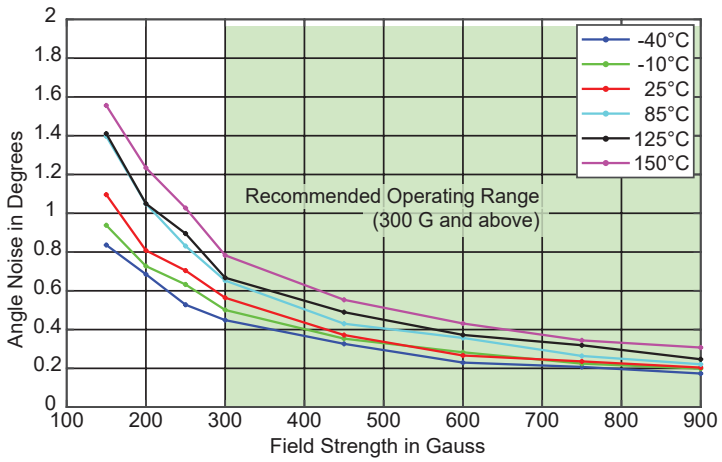



**Figure 32: Typical Three Sigma Angle Noise Over Field Strength**

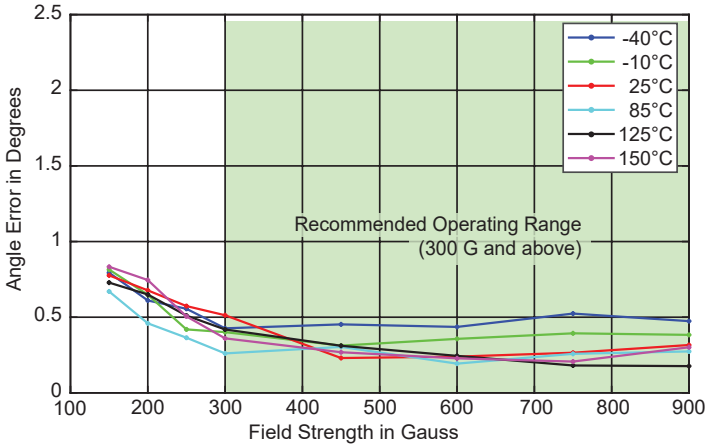



**Figure 33: Typical Angle Error Over Field Strength**



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955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

## Setting the Zero-Degree Position

When shipped from the factory, the default angle value when oriented as shown in Figure 34 is ≈162° for die 1 and ≈342° for die 2. In some cases, the end user may want to program and angle offset to compensate for variations in magnetic assemblies, or for applications where absolute system level readings are required.

The A1330 features two different offset adjust field in EEPROM, which may be used to change the location of the 0/360°discontinuity point. Depending on application either the PREGAIN_OFFSET, the POSTGAIN_OFFSET or both may be used to such ends.

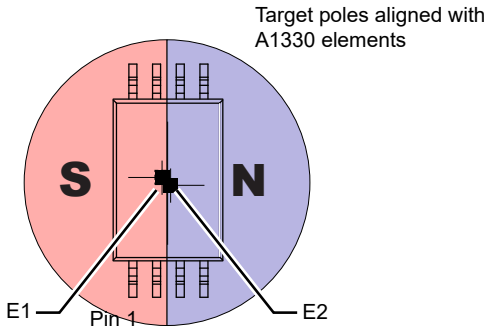



**Figure 34: Orientation of Magnet Relative to Primary and Secondary Die**

## Magnet Misalignment

Magnetic misalignment with the A1330 package impacts the linearity of the observed magnetic signal and consequently the resulting accuracy. The influence of mechanical misalignment may be minimized by reducing the overall airgap and by choosing a larger magnet diameter. Figure 35 shows the influence of magnet diameter of eccentricity error.

The dual die variant of the A1330 uses a stacked die approach, resulting in a common eccentricity value for both die. This eliminates the "native misalignment" present in "side-by-side" packaging options.

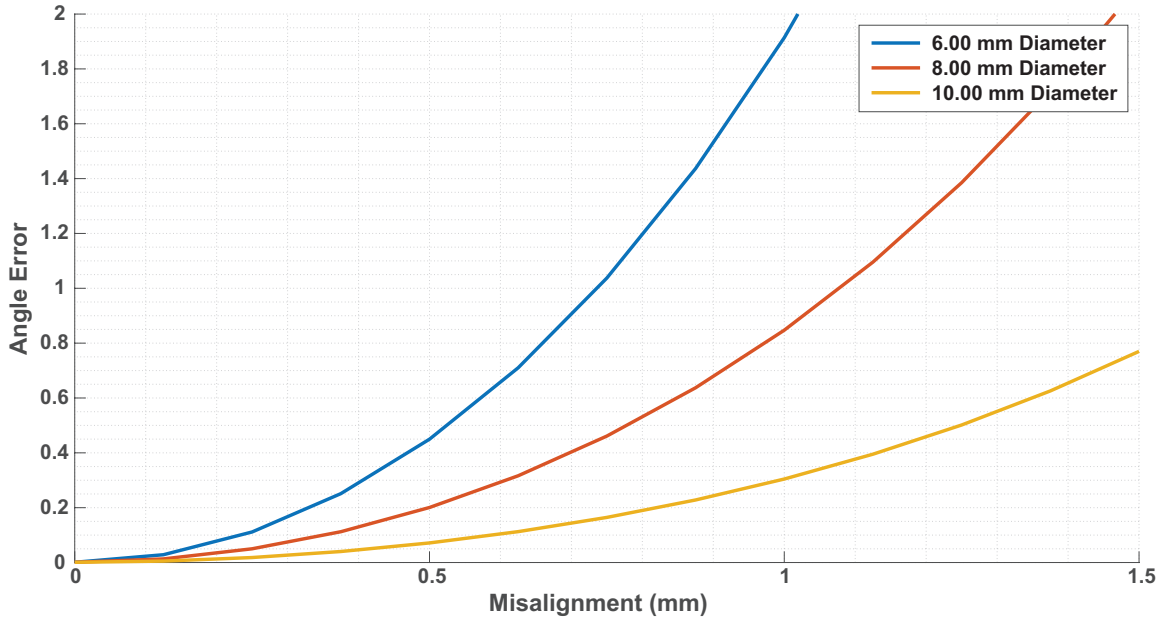



**Figure 35: Simulated Error versus Eccentricity for different size magnet diameters, at 2.0 mm air gap**

Typical Systemic Error versus magnet to sensor eccentricity ($d_{axial}$), Note: "Systemic Error" refers to application errors in alignment and system timing. It does not refer to sensor IC device errors. The data in this graph is simulated with ideal magnetization.



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Web:www.manduic.com

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

## Application Circuit Description

The analog output version of the A1330 may be operated with either a pull-up or pull-down resistor. Use of a load resistor is recommended, as this allows the output to float to a known “diagnostic” state in the event of a sensor diagnostic.

The PWM version, with its open-drain architecture, requires the output be connected to a voltage source, through a load resistor.

Figure 36 shows a typical A1330 application circuit, for either analog or PWM outputs. For EMC sensitive environments, an output load capacitor of 2 nF is recommended

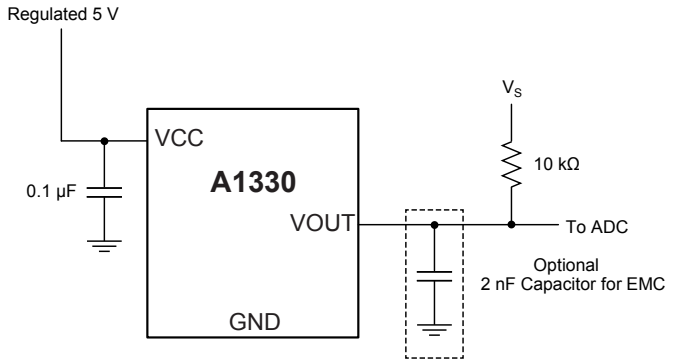



**Figure 36: Typical A1330 application circuit**

## ESD Performance

Under certain conditions, the ESD rating of the dual die IC may be less than 2 kV if ground pins are not tied to a common node. Contact Allegro for questions regarding ESD optimization.

**Table 8: HBM ESD Rating (per AEC-Q100 002)**

| Package | ESD Rating |
|---|---|
| TSSOP-08 (single die) | 6 kV |
| TSSOP-08 (dual die) | 6 kV [1] |

[1] All GND pins shorted together.



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Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

## EEPROM MEMORY MAP

The EEPROM memory map is shown below.

All EEPROM may be read once the IC is in “Manchester Output Mode”. Writing requires the EEPROM lock bit to be clear, and application of high voltage pulses on the output pin. See discussion on EEPROM programming for information on how to write EEPROM.

**Table 9: EEPROM Memory Map**

| Address | Bits | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 31:26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x3A | ECC | R | R | PREGAIN_OFFSET | | | | | | | | | | | | Reserved | | | | | | Reserved | | | | | |
| 0x3B | ECC | SS | Reserved | | | | | | | | | | | | | GAIN | | | | | | | | | | | |
| 0x3C | ECC | CE | ROE | MAX_INPUT | | | | | | | | | | | | MIN_INPUT | | | | | | | | | | | |
| 0x3D | ECC | ABW | PO | POSTGAIN_OFFSET | | | | | | | | | | | | HIGH_CLAMP | | | | | | LOW_CLAMP | | | | | |
| 0x3E | ECC | EELO | HYS_0 | HYS | | | PWM_FREQ | | | ANG_AVE | | | MISS_MAG_THRSH | | | | | | | | INTER | TOR | OVLO | EED | MAXA | MINA | MMF |
| 0x3F | ECC | Customer Word | | | | | | | | | | | | | | | | | | | | | | | | | |

### Address 0x3A

| Bit | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | R | R | PREGAIN_OFFSET | | | | | | | | | | | | Reserved | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**PREGAIN_OFFSET [23:12]:**

Pregain offset (zero adjust), at 12-bit resolution. This value is subtracted from the measured angle value, independent of short stroke.

| Value | Description |
|---|---|
| 0x0 to 0xFFF | 0 to 359.91° subtracted from pre gain angle value. |

**Reserved [11:0]:**

Reserved EEPROM registers. Should be set to 0’s.

### Address 0x3B

| Bit | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | SS | Reserved | | | | | | | | | | | | GAIN | | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**SS[25]:**

Enables “short stroke” mode. Gain and Min/Max Input angle checking are enabled.

| Value | Description |
|---|---|
| 0 | Short stroke not enabled |
| 1 | Short stroke enabled |

**Reserved[24:13]:**

Reserved EEPROM registers. Should be set to 0’s.

**GAIN[12:0]:**

Sets gain to apply full dynamic range of the output for a limited input range.
Only applied if SS is set to ‘1’.
Applied gain is 1 plus the total value set in the Gain EEPROM field.
GAIN specified in 5.8, unsigned form.
Example:
GAIN field = 0x055A equates to 5 + (90 / 256) = 5.3515625
Applied gain = 1 + GAIN = 6.3515625



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Web:www.manduic.com

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

### Address 0x3C

| Bit | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | CE | ROE | MAX_INPUT | | | | | | | | | | | | MIN_INPUT | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**CE[25]:**

Clamp enable.

| Value | Description |
|---|---|
| 0 | Disabled clamps |
| 1 | Enables clamps |

**ROE[24]:**

Roll-over enable.

| Value | Description |
|---|---|
| 0 | Disables roll-over |
| 1 | Enables roll-over |

Both CE and ROE interact to create four distinct operating modes. See table below.

| CE | ROE | Description |
|---|---|---|
| 0 | 0 | Normal behavior.<br>Roll-over at standard module 360. |
| 0 | 1 | Output rolls-over at the High and Low Clamp values. |
| 1 | 0 | Output clamps at the first encountered High/Low Clamp value. |
| 1 | 1 | Roll-over occurs at standard module 360.<br>Output is clamped to High/Low Clamps value. |

**MAX_INPUT[23:12]:**

Sets the maximum input angle, after PREGAIN_OFFSET but before scaling by GAIN. Used for short-stroke limit test, in 12-bit resolution units. Setting this field to 0xFFF will effectively disable this feature. This allows debugging and diagnostics of a possible broken sensor assembly. Used as a diagnostic point if the angle exceeds the targeted dynamic range.
SS must be set to '1' to enable this function.

| Value | Description |
|---|---|
| 0x0 to 0xFFF | Sets maximum input angle to 0 to 359.91° |

**MIN_INPUT[11:0]:**

Sets the minimum input angle (after PREGAIN_OFFSET), but before scaling by GAIN. Used for short-stroke limit test, in 12-bit resolution units. Setting this field to 0 will effectively disable this feature. This allows debugging and diagnostics of a possible broken sensor assembly. Used as a diagnostic point if the angle decreases below the targeted dynamic range.
SS must be set to '1' to enable this function.

| Value | Description |
|---|---|
| 0x0 to 0xFFF | Sets minimum input angle to 0 to 359.91° |



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Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

### Address 0x3D

| Bit | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | ABW | PO | POSTGAIN_OFFSET | | | | | | | | | | | | HIGH_CLAMP | | | | | | LOW_CLAMP | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**ABW[25]:**

Analog back end BW. Sets the BW of the analog filter.

| Value | Description |
|---|---|
| 0 | 30 kHz BW |
| 1 | 15 kHz BW |

**PO[24]:**

Polarity bit.
Sets which magnetic rotation direction results in an increasing output value. If set to '0', increasing angle is in the clockwise direction, when looking down on the top of the die, from the magnets perspective.
This occurs prior to the PREGAIN_OFFSET.

| Value | Description |
|---|---|
| 0 | Output angle increases with a clockwise rotation (when viewed from above the magnet and device) |
| 1 | Output angle increases with a counter-clockwise rotation (when viewed from above the magnet and device) |

**POSTGAIN_OFFSET[23:12]:**

Sets the output angular offset to relocate the 0° reference point for the output angle. Applied after GAIN and Min/Max Input angle comparison. Represented in signed 2's complement.

| Value | Description |
|---|---|
| 0x0 to 0x7FF | 0° to 179.91° |
| 0x800 to 0xFFF | –180° to –0.088° |



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Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

**HIGH_CLAMP[11:6]:**

Sets an output high angle clamp.
Applied after GAIN and POSTGAIN_OFFSET.
Decrements by ≈1% of $V_{CC}$.

| Code | Voltage | Approximate Angle | Nominal Voltage |
|---|---|---|---|
| 0 | $V_{OUT(MAX)}$ | 359.9 | 4.75 |
| 1 | $V_{OUT(MAX)}$ – 1% $V_{CC}$ | 356.0 | 4.70 |
| 2 | $V_{OUT(MAX)}$ – 2% $V_{CC}$ | 351.9 | 4.65 |
| 3 | $V_{OUT(MAX)}$ – 3% $V_{CC}$ | 348.0 | 4.60 |
| 4 | $V_{OUT(MAX)}$ – 4% $V_{CC}$ | 343.9 | 4.55 |
| 5 | $V_{OUT(MAX)}$ – 5% $V_{CC}$ | 340.0 | 4.50 |
| 6 | $V_{OUT(MAX)}$ – 6% $V_{CC}$ | 335.9 | 4.45 |
| 7 | $V_{OUT(MAX)}$ – 7% $V_{CC}$ | 332.0 | 4.40 |
| 8 | $V_{OUT(MAX)}$ – 8% $V_{CC}$ | 327.9 | 4.35 |
| 9 | $V_{OUT(MAX)}$ – 9% $V_{CC}$ | 324.0 | 4.30 |
| 10 | $V_{OUT(MAX)}$ – 10% $V_{CC}$ | 319.9 | 4.25 |
| 11 | $V_{OUT(MAX)}$ – 11% $V_{CC}$ | 316.0 | 4.20 |
| 12 | $V_{OUT(MAX)}$ – 12% $V_{CC}$ | 311.9 | 4.15 |
| 13 | $V_{OUT(MAX)}$ – 13% $V_{CC}$ | 308.0 | 4.10 |
| 14 | $V_{OUT(MAX)}$ – 14% $V_{CC}$ | 303.9 | 4.05 |
| 15 | $V_{OUT(MAX)}$ – 15% $V_{CC}$ | 300.0 | 4.00 |
| 16 | $V_{OUT(MAX)}$ – 16% $V_{CC}$ | 295.9 | 3.95 |
| 17 | $V_{OUT(MAX)}$ – 17% $V_{CC}$ | 292.0 | 3.90 |
| 18 | $V_{OUT(MAX)}$ – 18% $V_{CC}$ | 287.9 | 3.85 |
| 19 | $V_{OUT(MAX)}$ – 19% $V_{CC}$ | 284.0 | 3.80 |
| 20 | $V_{OUT(MAX)}$ – 20% $V_{CC}$ | 279.9 | 3.75 |
| 21 | $V_{OUT(MAX)}$ – 21% $V_{CC}$ | 276.0 | 3.70 |
| 22 | $V_{OUT(MAX)}$ – 22% $V_{CC}$ | 271.9 | 3.65 |
| 23 | $V_{OUT(MAX)}$ – 23% $V_{CC}$ | 268.0 | 3.60 |
| 24 | $V_{OUT(MAX)}$ – 24% $V_{CC}$ | 263.9 | 3.55 |
| 25 | $V_{OUT(MAX)}$ – 25% $V_{CC}$ | 260.0 | 3.50 |
| 26 | $V_{OUT(MAX)}$ – 26% $V_{CC}$ | 255.9 | 3.45 |
| 27 | $V_{OUT(MAX)}$ – 27% $V_{CC}$ | 252.0 | 3.40 |
| 28 | $V_{OUT(MAX)}$ – 28% $V_{CC}$ | 247.9 | 3.35 |
| 29 | $V_{OUT(MAX)}$ – 29% $V_{CC}$ | 244.0 | 3.30 |
| 30 | $V_{OUT(MAX)}$ – 30% $V_{CC}$ | 240.0 | 3.25 |
| 31 | $V_{OUT(MAX)}$ – 31% $V_{CC}$ | 236.0 | 3.20 |
| 32 | $V_{OUT(MAX)}$ –32% $V_{CC}$ | 232.0 | 3.15 |
| 33 | $V_{OUT(MAX)}$ – 33% $V_{CC}$ | 228.0 | 3.10 |
| 34 | $V_{OUT(MAX)}$ – 34% $V_{CC}$ | 224.0 | 3.05 |
| 35 | $V_{OUT(MAX)}$ – 35% $V_{CC}$ | 220.0 | 3.00 |
| 36 | $V_{OUT(MAX)}$ – 36% $V_{CC}$ | 216.0 | 2.95 |
| 37 | $V_{OUT(MAX)}$ – 37% $V_{CC}$ | 212.0 | 2.90 |
| 38 | $V_{OUT(MAX)}$ – 38% $V_{CC}$ | 208.0 | 2.85 |
| 39 | $V_{OUT(MAX)}$ – 39% $V_{CC}$ | 204.0 | 2.80 |
| 40 | $V_{OUT(MAX)}$ – 40% $V_{CC}$ | 200.0 | 2.75 |
| 41 | $V_{OUT(MAX)}$ – 41% $V_{CC}$ | 196.0 | 2.70 |
| 42 | $V_{OUT(MAX)}$ – 42% $V_{CC}$ | 192.0 | 2.65 |
| 43 | $V_{OUT(MAX)}$ – 43% $V_{CC}$ | 188.0 | 2.60 |
| 44 | $V_{OUT(MAX)}$ – 44% $V_{CC}$ | 184.0 | 2.55 |
| 45 | $V_{OUT(MAX)}$ – 45% $V_{CC}$ | 180.0 | 2.50 |
| 46 | $V_{OUT(MAX)}$ – 46% $V_{CC}$ | 176.0 | 2.45 |
| 47 | $V_{OUT(MAX)}$ – 47% $V_{CC}$ | 172.0 | 2.40 |
| 48 | $V_{OUT(MAX)}$ – 48% $V_{CC}$ | 168.0 | 2.35 |
| 49 | $V_{OUT(MAX)}$ – 49% $V_{CC}$ | 164.0 | 2.30 |
| 50 | $V_{OUT(MAX)}$ – 50% $V_{CC}$ | 160.0 | 2.25 |
| 51 | $V_{OUT(MAX)}$ – 51% $V_{CC}$ | 156.0 | 2.20 |
| 52 | $V_{OUT(MAX)}$ – 52% $V_{CC}$ | 152.1 | 2.15 |
| 53 | $V_{OUT(MAX)}$ – 53% $V_{CC}$ | 148.0 | 2.10 |
| 54 | $V_{OUT(MAX)}$ – 54% $V_{CC}$ | 144.1 | 2.05 |
| 55 | $V_{OUT(MAX)}$ – 55% $V_{CC}$ | 140.0 | 2.00 |
| 56 | $V_{OUT(MAX)}$ – 56% $V_{CC}$ | 136.1 | 1.95 |
| 57 | $V_{OUT(MAX)}$ – 57% $V_{CC}$ | 132.0 | 1.90 |
| 58 | $V_{OUT(MAX)}$ – 58% $V_{CC}$ | 128.1 | 1.85 |
| 59 | $V_{OUT(MAX)}$ – 59% $V_{CC}$ | 124.0 | 1.80 |
| 60 | $V_{OUT(MAX)}$ – 60% $V_{CC}$ | 120.1 | 1.75 |
| 61 | $V_{OUT(MAX)}$ – 61% $V_{CC}$ | 116.0 | 1.70 |
| 62 | $V_{OUT(MAX)}$ – 62% $V_{CC}$ | 112.1 | 1.65 |
| 63 | $V_{OUT(MAX)}$ – 63% $V_{CC}$ | 108.0 | 1.60 |



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Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

**LOW_CLAMP [5:0]:**

Sets an output low clamp level.
Applied after GAIN and POSTGAIN_OFFSET.
Increments by ≈1% of $V_{CC}$.

| Code | Voltage | Approximate Angle | Nominal Voltage |
|---|---|---|---|
| 0 | $V_{OUT(MIN)}$ | 0.0 | 0.25 |
| 1 | $V_{OUT(MIN)}$ + 1% $V_{CC}$ | 4.0 | 0.30 |
| 2 | $V_{OUT(MIN)}$ + 2% $V_{CC}$ | 8.0 | 0.35 |
| 3 | $V_{OUT(MIN)}$ + 3% $V_{CC}$ | 12.0 | 0.40 |
| 4 | $V_{OUT(MIN)}$ + 4% $V_{CC}$ | 16.0 | 0.45 |
| 5 | $V_{OUT(MIN)}$ + 5% $V_{CC}$ | 20.0 | 0.50 |
| 6 | $V_{OUT(MIN)}$ + 6% $V_{CC}$ | 24.0 | 0.55 |
| 7 | $V_{OUT(MIN)}$ + 7% $V_{CC}$ | 27.9 | 0.60 |
| 8 | $V_{OUT(MIN)}$ + 8% $V_{CC}$ | 32.0 | 0.65 |
| 9 | $V_{OUT(MIN)}$ + 9% $V_{CC}$ | 35.9 | 0.70 |
| 10 | $V_{OUT(MIN)}$ + 10% $V_{CC}$ | 40.0 | 0.75 |
| 11 | $V_{OUT(MIN)}$ + 11% $V_{CC}$ | 43.9 | 0.80 |
| 12 | $V_{OUT(MIN)}$ + 12% $V_{CC}$ | 48.0 | 0.85 |
| 13 | $V_{OUT(MIN)}$ + 13% $V_{CC}$ | 51.9 | 0.90 |
| 14 | $V_{OUT(MIN)}$ + 14% $V_{CC}$ | 56.0 | 0.95 |
| 15 | $V_{OUT(MIN)}$ + 15% $V_{CC}$ | 59.9 | 1.00 |
| 16 | $V_{OUT(MIN)}$ + 16% $V_{CC}$ | 64.0 | 1.05 |
| 17 | $V_{OUT(MIN)}$ + 17% $V_{CC}$ | 67.9 | 1.10 |
| 18 | $V_{OUT(MIN)}$ + 18% $V_{CC}$ | 72.0 | 1.15 |
| 19 | $V_{OUT(MIN)}$ + 19% $V_{CC}$ | 75.9 | 1.20 |
| 20 | $V_{OUT(MIN)}$ + 20% $V_{CC}$ | 80.0 | 1.25 |
| 21 | $V_{OUT(MIN)}$ + 21% $V_{CC}$ | 83.9 | 1.30 |
| 22 | $V_{OUT(MIN)}$ + 22% $V_{CC}$ | 88.0 | 1.35 |
| 23 | $V_{OUT(MIN)}$ + 23% $V_{CC}$ | 91.9 | 1.40 |
| 24 | $V_{OUT(MIN)}$ + 24% $V_{CC}$ | 96.0 | 1.45 |
| 25 | $V_{OUT(MIN)}$ + 25% $V_{CC}$ | 99.9 | 1.50 |
| 26 | $V_{OUT(MIN)}$ + 26% $V_{CC}$ | 104.0 | 1.55 |
| 27 | $V_{OUT(MIN)}$ + 27% $V_{CC}$ | 107.9 | 1.60 |
| 28 | $V_{OUT(MIN)}$ + 28% $V_{CC}$ | 112.0 | 1.65 |
| 29 | $V_{OUT(MIN)}$ + 29% $V_{CC}$ | 115.9 | 1.70 |
| 30 | $V_{OUT(MIN)}$ + 30% $V_{CC}$ | 120.0 | 1.75 |
| 31 | $V_{OUT(MIN)}$ + 31% $V_{CC}$ | 123.9 | 1.80 |
| 32 | $V_{OUT(MIN)}$ + 32% $V_{CC}$ | 128.0 | 1.850 |
| 33 | $V_{OUT(MIN)}$ + 33% $V_{CC}$ | 131.9 | 1.900 |
| 34 | $V_{OUT(MIN)}$ + 34% $V_{CC}$ | 136.0 | 1.950 |
| 35 | $V_{OUT(MIN)}$ + 35% $V_{CC}$ | 139.9 | 2.000 |
| 36 | $V_{OUT(MIN)}$ + 36% $V_{CC}$ | 144.0 | 2.050 |
| 37 | $V_{OUT(MIN)}$ + 37% $V_{CC}$ | 147.9 | 2.100 |
| 38 | $V_{OUT(MIN)}$ + 38% $V_{CC}$ | 152.0 | 2.150 |
| 39 | $V_{OUT(MIN)}$ + 39% $V_{CC}$ | 155.9 | 2.200 |
| 40 | $V_{OUT(MIN)}$ + 40% $V_{CC}$ | 160.0 | 2.250 |
| 41 | $V_{OUT(MIN)}$ + 41% $V_{CC}$ | 163.9 | 2.300 |
| 42 | $V_{OUT(MIN)}$ + 42% $V_{CC}$ | 168.0 | 2.350 |
| 43 | $V_{OUT(MIN)}$ + 43% $V_{CC}$ | 171.9 | 2.400 |
| 44 | $V_{OUT(MIN)}$ + 44% $V_{CC}$ | 176.0 | 2.450 |
| 45 | $V_{OUT(MIN)}$ + 45% $V_{CC}$ | 179.9 | 2.500 |
| 46 | $V_{OUT(MIN)}$ + 46% $V_{CC}$ | 184.0 | 2.550 |
| 47 | $V_{OUT(MIN)}$ + 47% $V_{CC}$ | 187.9 | 2.600 |
| 48 | $V_{OUT(MIN)}$ + 48% $V_{CC}$ | 192.0 | 2.650 |
| 49 | $V_{OUT(MIN)}$ + 49% $V_{CC}$ | 195.9 | 2.700 |
| 50 | $V_{OUT(MIN)}$ + 50% $V_{CC}$ | 200.0 | 2.750 |
| 51 | $V_{OUT(MIN)}$ + 51% $V_{CC}$ | 203.9 | 2.800 |
| 52 | $V_{OUT(MIN)}$ + 52% $V_{CC}$ | 207.9 | 2.850 |
| 53 | $V_{OUT(MIN)}$ + 53% $V_{CC}$ | 211.9 | 2.900 |
| 54 | $V_{OUT(MIN)}$ + 54% $V_{CC}$ | 215.9 | 2.950 |
| 55 | $V_{OUT(MIN)}$ + 55% $V_{CC}$ | 219.9 | 3.000 |
| 56 | $V_{OUT(MIN)}$ + 56% $V_{CC}$ | 223.9 | 3.050 |
| 57 | $V_{OUT(MIN)}$ + 57% $V_{CC}$ | 227.9 | 3.100 |
| 58 | $V_{OUT(MIN)}$ + 58% $V_{CC}$ | 231.9 | 3.150 |
| 59 | $V_{OUT(MIN)}$ + 59% $V_{CC}$ | 235.9 | 3.200 |
| 60 | $V_{OUT(MIN)}$ + 60% $V_{CC}$ | 239.9 | 3.250 |
| 61 | $V_{OUT(MIN)}$ + 61% $V_{CC}$ | 243.9 | 3.300 |
| 62 | $V_{OUT(MIN)}$ + 62% $V_{CC}$ | 247.9 | 3.350 |
| 63 | $V_{OUT(MIN)}$ + 63% $V_{CC}$ | 251.9 | 3.400 |



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Web:www.manduic.com

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

## Address 0x3E

| Bit | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | EELO | HYS_0 | HYS | | PWM_FREQ | | | ANG_AVE | | | MISS_MAG_THRSH | | | | | | | | | INTER | TOR | OVLO | EED | MAXA | MINA | MMF |
| Default | 0 | 0* | 0* | 0 | 1 | 0 | 0 | 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* | 0* | 1* | 0* | 1* | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**EELO[25]:**

EEPROM Lock Bit.
Once set, EEPROM cannot be written.

| Value | Description |
|---|---|
| 0 | EEPROM writes allowed |
| 1 | EEPROM writing prevented |

**HYS_0[24]:**

Hysteresis is only applied within ±11.16° of the 0/360 crossover point.

| Value | Description |
|---|---|
| 0 | Hysteresis is applied across the whole angle range |
| 1 | Hysteresis is only applied near the 0/360° crossover point |

**HYS[23:22]:**

Hysteresis range selection.
When applied the angle will not update unless a change larger than the hysteresis range is observed.
Applied after PREGAIN_OFFSET. Prior to GAIN.

* Default value of 0 for all catalog part numbers except A1330LLETR-T-C02.

| Value | Description |
|---|---|
| 00 | 0° |
| 01 | 0352° |
| 10 | 0.703° (Default value for A1330LLETR-T-C02) |
| 11 | 1.406° |

**PWM_FREQ[21:19]:**

Sets the PWM carrier frequency.

| PWM_FREQ | PWM Frequency |
|---|---|
| 000 | 20 kHz |
| 001 | 10 kHz |
| 010 | 5 kHz |
| 011 | 2.5 kHz |
| 100 | 1.25 kHz |
| 101 | 625 Hz |
| 110 | 312.5 Hz |
| 111 | 156.25 Hz |

**ANG_AVE[18:16]:**

Selects the number of internal angle samples to average. Reduces the update rate of the IC for improved angle resolution.

* Default value of 0 for all catalog part numbers except A1330LLETR-T-C02, which is set to $011_2$.

| Value | Quantity of Samples Averaged | Approx. Refresh Rate (µs) |
|---|---|---|
| 000 | 1 | 25 |
| 001 | 2 | 50 |
| 010 | 4 | 100 |
| 011 | 8 | 200 |
| 100 | 16 | 400 |
| 101 | 32 | 800 |
| 110 | 64 | 1600 |
| 111 | 128 | 3200 |



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Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

**MIS_MAG_THRSH[15:7]:**

Threshold below which the missing magnet flag will assert. At Allegro factory.

*This is programmed for a default of 100 G. The value of $0101_2$ shown in the above table is typical; actual values may vary, depending on device behavior.

If a setting other than 100 G is desired, simply scale the existing value by d_field / 100 where “d_field” is the desired trip point in gauss.

Example: If the desired trip point is 300 G, and the default factory EEPROM value is 0x5, then the final value is 300 / 100 × 5 = 15 = 0xF.

**INTER[6]:**

Interpolator Error mask.
Prevents an interpolator error from setting the output to tri-state.

| Value | Description |
|---|---|
| 0 | Interpolator error will tri-state output |
| 1 | Interpolator error will not tri-state output |

**TOR[5]:**

Temperature Out Of Range Mask.
Prevents a temperature out of range error from tri-stating the output.

| Value | Description |
|---|---|
| 0 | Temperature out of range error will tri-state output |
| 1 | Temperature out of rang error will not tri-state output |

**OVLO[4]:**

Overvoltage Error Mask.
Prevents an overvoltage error from tristating the output.

| Value | Description |
|---|---|
| 0 | Overvoltage error will tri-state the output |
| 1 | Overvoltage error will not tri-state the output |

**EED[3]:**

Dual bit EEPROM error.
Prevents a dual bit EEPROM error from tristating the output.

| Value | Description |
|---|---|
| 0 | Dual bit EEPROM error will tri-state the output |
| 1 | Dual bit EEPROM error will not tri-state the output |

**MAXA[2]:**

Maximum Input Angle Mask.
When set, the output will not tri-state when the input angle exceeds the MAX_INPUT value.

| Value | Description |
|---|---|
| 0 | Output tri-states if input angle exceeds MAX_INPUT |
| 1 | Output doesn’t tri-states if input angle exceeds MAX_INPUT |

**MINA[1]:**

Minimum Input Angle Mask.
When set, the output will not tri-state when the input angle is below the MIN_INPUT value.

| Value | Description |
|---|---|
| 0 | Output tri-states if input angle is below MIN_INPUT |
| 1 | Output doesn’t tri-states if input angle is below MIN_INPUT |

**MMF[0]:**

Missing Magnet Flag Mask.
When set, output will not tri-state if the measured magnetic amplitude is below the MIS_MAG_THRSH.

| Value | Description |
|---|---|
| 0 | Missing magnet error tri-states output |
| 1 | Missing magnet error does not tri-states output |



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Allegro MicroSystems
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### Address 0x3F

| Bit | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | Customer Word | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Customer Word[25:0]:**

Customer EEPROM space.



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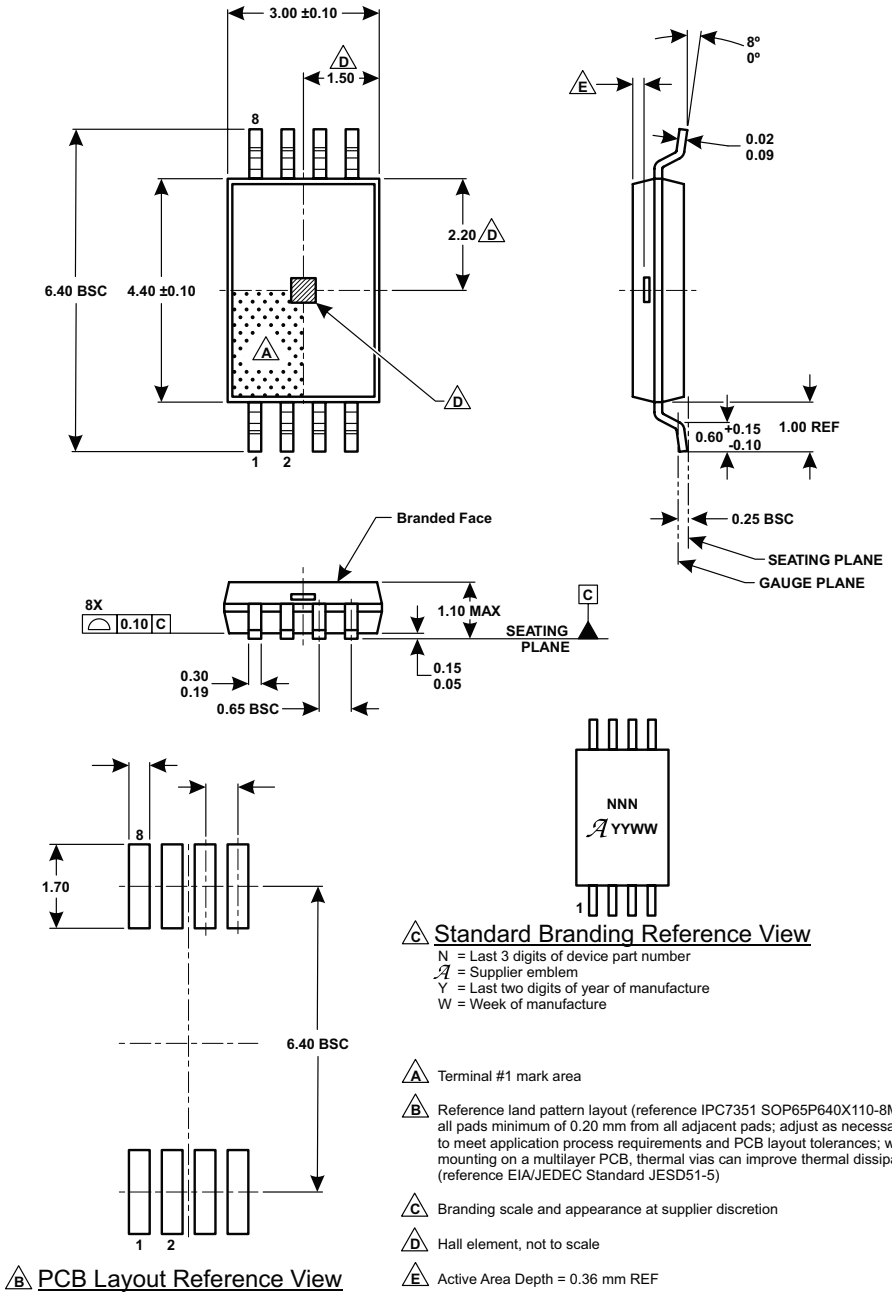
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955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

## PACKAGE OUTLINE DRAWINGS

**For Reference Only – Not for Tooling Use**

**(Reference MO-153AA)**
Dimensions in millimeters - NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown




C Standard Branding Reference View
N = Last 3 digits of device part number
A = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture

B PCB Layout Reference View

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-8M); all pads minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Branding scale and appearance at supplier discretion

D Hall element, not to scale

E Active Area Depth = 0.36 mm REF

**Figure 37: Package LE, 8-Pin TSSOP (Single Die Version)**



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Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

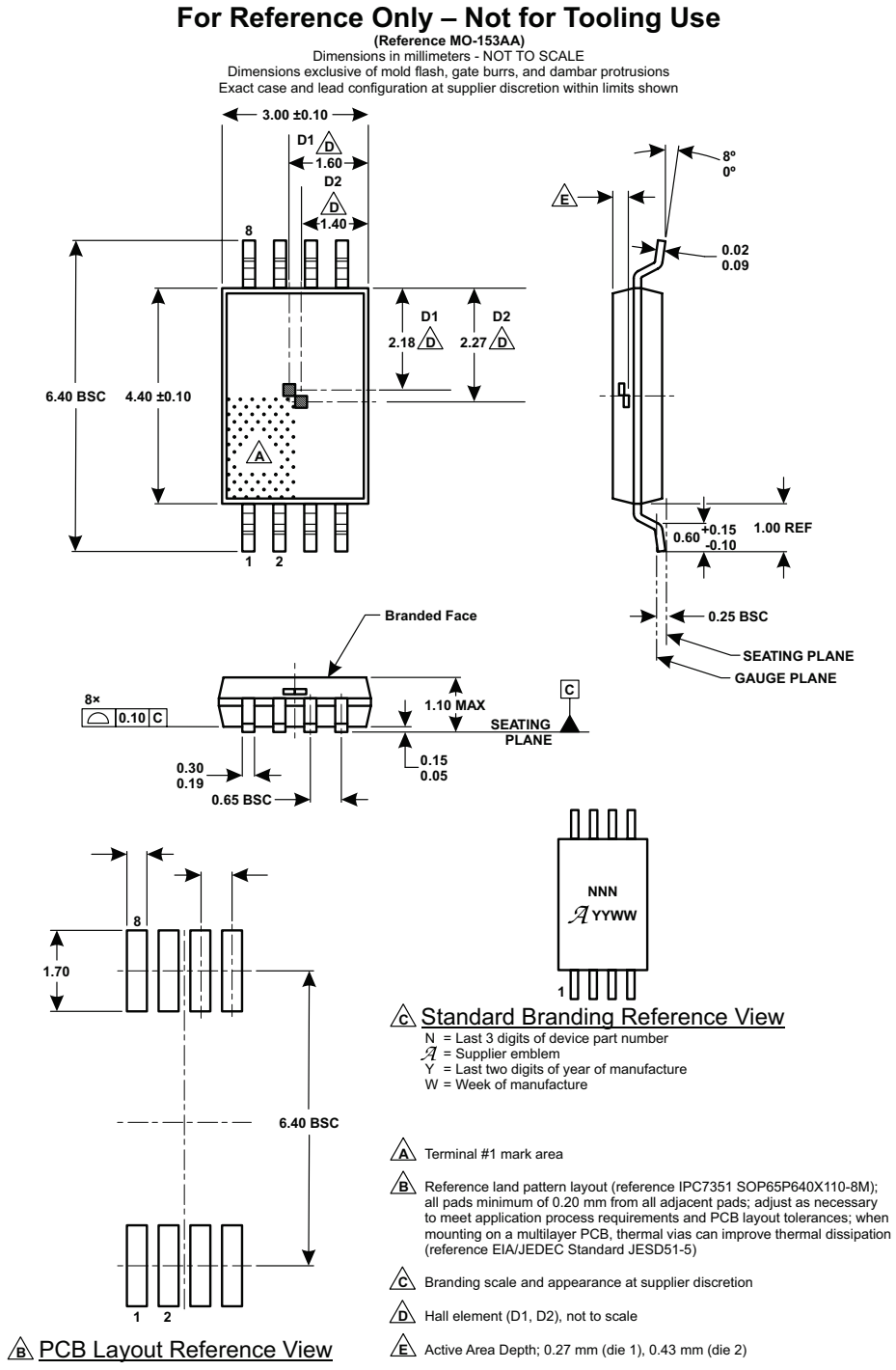



**Figure 38: Package LE, 8-Pin TSSOP (Dual Die Version)**



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955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

## APPENDIX A: ANGLE ERROR AND DRIFT DEFINITION

Angle error is the difference between the actual position of the magnet and the position of the magnet as measured by the angle sensor IC (without noise). This measurement is done by reading the angle sensor IC output and comparing it with a high resolution encoder (refer to Figure 39).

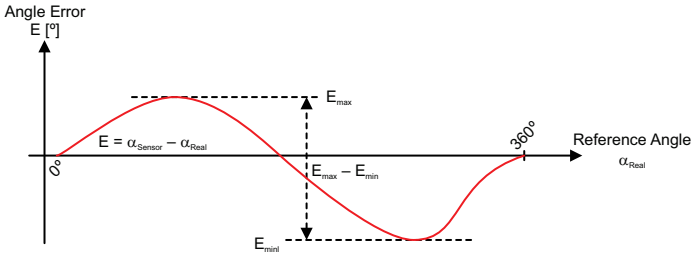



**Figure 39: Angle Error Definition**

### Angle Error Definition

Throughout this document, the term “angle error” is used extensively. Thus, it is necessary to introduce a single angle error definition for a full magnetic rotation. The term “angle error” is calculated according to the following formula:

$$Angle\ Error = \frac{E\max - E\min}{2}$$

In other words, it is the amplitude of the deviation from a perfect straight line between 0 and 360 degrees. For the purposes of a generic definition, the offset of the IC angle profile is removed prior to the error calculation (this can be seen in Figure 39). The offset itself will depend on the starting IC angle position relative to the encoder 0° and thus can differ anywhere from 0-360°.

### Angle Drift

Angle drift is the change in the observed angular position over temperature, relative to 25°C.

During Allegro’s factory trim, drift is measured at 150°C. The value is calculated using the following formula:

$$Angle_{Drift} = Angle_{25°C} - Angle_{150°C}$$

where each Angle value is an array corresponding to 16 angular positions around a circle.

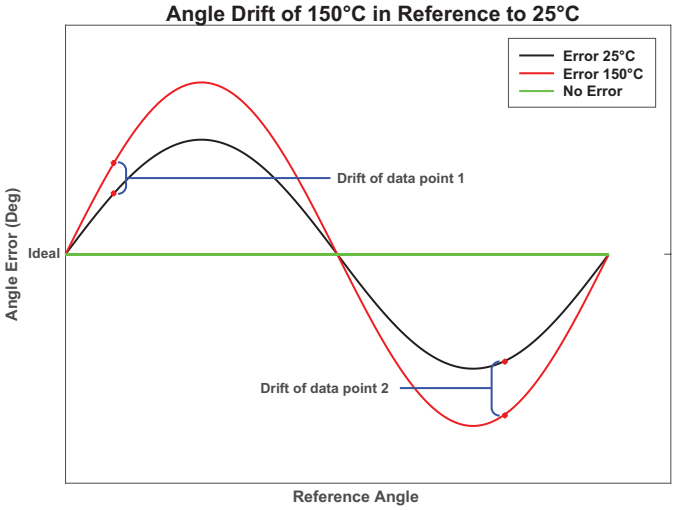



**Figure 40: Angle Drift of 150°C in Reference to 25°C [1]**

[1] Note that the data above is simply a representation of angle drift and not real data.



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955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

## Ratiometry Error Definition

The analog version of the A1330 provides a ratiometric output. This means that the Voltage Output, $V_{OUT}$, and the angular sensitivity are proportional to the supply voltage, $V_{CC}$. In other words, when the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Error is the difference between the measured change in the supply voltage relative to 5.0 V, and the measured change in each characteristic.

The ratiometric error for a given magnetic position (θ), $Rat_{VOUT}$ (%), for a given supply voltage, $V_{CC}$, is defined as:

$$Rat_{VOUT(\theta)} = \left(1 - \frac{V_{OUT(\theta)(VCC)} / V_{OUT(\theta)(5.0V)}}{V_{CC} / 5.0\ (V)}\right) \times 100 \quad (\%)$$

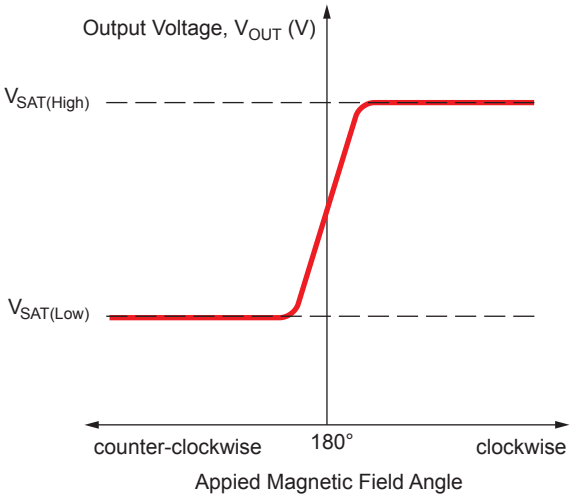



**Figure 41: Effect of Saturation**



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Web:www.manduic.com

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

## APPENDIX B: CRC DOCUMENATION

### Manchester CRC Implementation

The 3-bit Manchester CRC can be calculated using the following C code:

```
// command: the manchester command, right justified, does
not include the space for the CRC
// numberOfBits: number of bits in the command not includ-
ing the 2 zero sync bits at the start of the command and the
three CRC bits
// Returns: The three bit CRC
// This code can be tested at http://codepad.org/yqTKnfmD
uint16_t ManchesterCRC(uint64_t data, uint16_t numberOfBits)
{
	bool C0 = false;
	bool C1 = false;
	bool C2 = false;
	bool C0p = true;
	bool C1p = true;
	bool C2p = true;
	uint64_t bitMask = 1;

	bitMask <<= numberOfBits - 1;

	// Calculate the state machine
	for (; bitMask != 0; bitMask >>= 1)
	{
		C2 = C1p;
		C0 = C2p ^ ((data & bitMask) != 0);
		C1 = C0 ^ C0p;

		C0p = C0;
		C1p = C1;
		C2p = C2;
	}

	return (C2 ? 4U : 0U) + (C1 ? 2U : 0U) + (C0 ? 1U :
0U);
}
```



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955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com

## Revision History

| Revision | Date | Description |
|---|---|---|
| – | September 25, 2017 | Initial release |
| 1 | June 29, 2018 | Updated Features and Benefits (page 1), Thermal Characteristics (page 2), Supply Current (page 5), Figure 3 and 4 (page 7), Figures 14 through 17 (page 19 and 21), Gain section (page 20), Clamp and Roll-Over Logic figure captions (page 21), Figures 32 and 33 (page 24), Figure 34 (page 25), and Dual Die LE-8 Package Drawing active area depth dimensions (page 36); added figure to Angle Averaging section (page 18). |
| 2 | August 3, 2018 | Updated Features and Benefits (page 1), Selection Guide (page 2), Response Time (page 6), Angle Noise (page 6), Figure 3 (page 7), Hysteresis (page 10), Address 0x3E (page 32-33). |
| 3 | August 21, 2019 | Minor editorial updates. |

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Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Tel:150-1290-5940
Email:sales@manduic.com