# 25LC512

## 512-Kbit SPI Bus Serial EEPROM

### Device Selection Table

| Part Number | Vcc Range | Page Size | Temp. Ranges | Packages |
|---|---|---|---|---|
| 25LC512 | 2.5V-5.5V | 128 Byte | I,E | P, SN, SM, MF |

### Features

- 20 MHz maximum Clock Speed
- Byte and Page-level Write Operations:
  - 128-byte page
  - 5 ms maximum
  - No page or sector erase required
- Low-Power CMOS Technology:
  - Max. Write current: 7 mA at 5.5V
  - Max. Read current: 10 mA at 5.5V, 20 MHz
  - Standby current: 1μA at 2.5V, 85°C (Deep power-down)
- Electronic Signature for Device ID
- Self-Timed Erase and Write cycles:
  - Page Erase (5 ms, typical)
  - Sector Erase (10 ms/sector, typical)
  - Bulk Erase (10 ms, typical)
- Sector Write Protection (16K byte/sector):
  - Protect none, 1/4, 1/2 or all of array
- Built-In Write Protection:
  - Power-on/off data protection circuitry
  - Write enable latch
  - Write-protect pin
- Sequential Read
- High Reliability:
  - Endurance: 1 Million erase/write cycles
  - Data Retention: >200 years
  - ESD Protection: >4000V
- Temperature Ranges Supported:
  - Industrial (I): -40°C to +85°C
  - Extended (E): -40°C to +125°C
- RoHS Compliant
- Automotive AEC-Q100 Qualified

### Pin Function Table

| Name | Function |
|---|---|
| $\overline{CS}$ | Chip Select Input |
| SO | Serial Data Output |
| $\overline{WP}$ | Write-Protect |
| Vss | Ground |
| SI | Serial Data Input |
| SCK | Serial Clock Input |
| $\overline{HOLD}$ | Hold Input |
| Vcc | Supply Voltage |

### Description

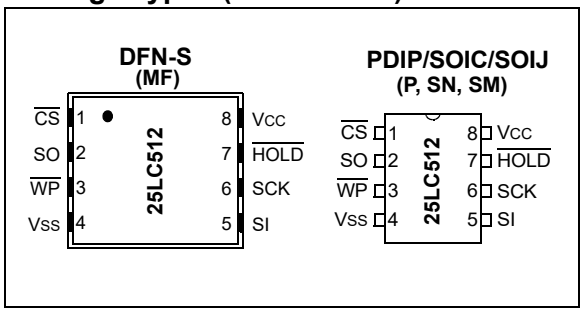
The Microchip Technology Inc. 25LC512 is a 512-Kbit serial EEPROM memory with byte-level and page-level serial EEPROM functions. It also features Page, Sector and Chip erase functions typically associated with Flash-based products. These functions are not required for byte or page write operations. The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled by a Chip Select ($\overline{CS}$) input.

Communication to the device can be paused via the hold pin ($\overline{HOLD}$). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

### Packages

- 8-Lead DFN-S, 8-Lead PDIP, 8-Lead SOIC and 8-Lead SOIJ

### Package Types (not to scale)




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## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature .....-65°C to 150°C

Ambient temperature under bias.....-40°C to 125°C

ESD protection on all pins.....4 kV

**†** NOTICE**:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

**TABLE 1-1: DC CHARACTERISTICS**

| **DC CHARACTERISTICS** | | | **Electrical Characteristics:**<br>**Industrial (I): TA = -40°C to +85°C VCC = 2.5V to 5.5V**<br>**Extended (E): TA = -40°C to +125°C VCC = 2.5V to 5.5V** | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristic** | **Min.** | **Max.** | **Units** | **Test Conditions** |
| D001 | VIH1 | High-level input voltage | 0.7 x VCC | VCC + 1 | V | |
| D002 | VIL1 | Low-level input voltage | -0.3 | 0.3 x VCC | V | VCC ≥ 2.7V |
| D003 | VIL2 | | -0.3 | 0.2 x VCC | V | VCC < 2.7V |
| D004 | VOL | Low-level output voltage | — | 0.4 | V | IOL = 2.1 mA |
| D005 | VOH | High-level output voltage | VCC - 0.2 | — | V | IOH = -400 µA |
| D006 | ILI | Input leakage current | — | ±1 | µA | $\overline{CS}$ = VCC, VIN = VSS or VCC |
| D007 | ILO | Output leakage current | — | ±1 | µA | $\overline{CS}$ = VCC, VOUT = VSS or VCC |
| D008 | CINT | Internal capacitance (all inputs and outputs) | — | 7 | pF | TA = 25°C, CLK = 1.0 MHz, VCC = 5.0V (**Note**) |
| D009 | ICC Read | Operating current | — | 10 | mA | VCC = 5.5V; FCLK = 20.0 MHz; SO = Open |
| | | | — | 5 | mA | VCC = 2.5V; FCLK = 10.0 MHz; SO = Open |
| D010 | ICC Write | | — | 7 | mA | VCC = 5.5V |
| | | | — | 5 | mA | VCC = 2.5V |
| D011 | ICCS | Standby current | — | 20 | µA | $\overline{CS}$ = VCC = 5.5V, Inputs tied to VCC or VSS, 125°C |
| | | | — | 10 | µA | $\overline{CS}$ = VCC = 5.5V, Inputs tied to VCC or VSS, 85°C |
| D012 | ICCSPD | Deep power-down current | — | 2 | µA | $\overline{CS}$ = VCC = 2.5V, Inputs tied to VCC or VSS, 125°C |
| | | | — | 1 | µA | $\overline{CS}$ = VCC = 2.5V, Inputs tied to VCC or VSS, 85°C |

**Note:** This parameter is periodically sampled and not 100% tested.


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**TABLE 1-2: AC CHARACTERISTICS**

| AC CHARACTERISTICS | | | Electrical Characteristics:<br>Industrial (I): TA = -40°C to +85°C VCC = 2.5V to 5.5V<br>Extended (E): TA = -40°C to +125°C VCC = 2.5V to 5.5V | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristic** | **Min.** | **Max.** | **Units** | **Conditions** |
| 1 | FCLK | Clock frequency | — | 20 | MHz | 4.5V ≤ VCC ≤ 5.5V (I) |
| | | | — | 10 | MHz | 2.5V ≤ VCC < 5.5V (I, E) |
| 2 | TCSS | $\overline{CS}$ setup time | 25 | — | ns | 4.5V ≤ VCC ≤ 5.5V (I) |
| | | | 50 | — | ns | 2.5V ≤ VCC < 5.5V (I, E) |
| 3 | TCSH | $\overline{CS}$ hold time | 50 | — | ns | 4.5V ≤ VCC ≤ 5.5V (I) |
| | | | 100 | — | ns | 2.5V ≤ VCC < 5.5V (I, E) |
| 4 | TCSD | $\overline{CS}$ disable time | 50 | — | ns | — |
| 5 | Tsu | Data setup time | 5 | — | ns | 4.5V ≤ VCC ≤ 5.5V (I) |
| | | | 10 | — | ns | 2.5V ≤ VCC < 5.5V (I, E) |
| 6 | THD | Data hold time | 10 | — | ns | 4.5V ≤ VCC ≤ 5.5V (I) |
| | | | 20 | — | ns | 2.5V ≤ VCC < 5.5V (I, E) |
| 7 | TR | CLK rise time | — | 20 | ns | **(Note 1)** |
| 8 | TF | CLK fall time | — | 20 | ns | **(Note 1)** |
| 9 | THI | Clock high time | 25 | — | ns | 4.5V ≤ VCC ≤ 5.5V (I) |
| | | | 50 | — | ns | 2.5V ≤ VCC < 5.5V (I, E) |
| 10 | TLO | Clock low time | 25 | — | ns | 4.5V ≤ VCC ≤ 5.5V (I) |
| | | | 50 | — | ns | 2.5V ≤ VCC < 5.5V (I, E) |
| 11 | TCLD | Clock delay time | 50 | — | ns | — |
| 12 | TCLE | Clock enable time | 50 | — | ns | — |
| 13 | TV | Output valid from clock low | — | 25 | ns | 4.5V ≤ VCC ≤ 5.5V (I) |
| | | | — | 50 | ns | 2.5V ≤ VCC < 5.5V (I, E) |
| 14 | THO | Output hold time | 0 | — | ns | **(Note 1)** |
| 15 | TDIS | Output disable time | — | 25 | ns | 4.5V ≤ VCC ≤ 5.5V (I) |
| | | | — | 50 | ns | 2.5V ≤ VCC < 5.5V (I, E) |
| 16 | THS | $\overline{HOLD}$ setup time | 10 | — | ns | 4.5V ≤ VCC ≤ 5.5V (I) |
| | | | 20 | — | ns | 2.5V ≤ VCC < 5.5V (I, E) |
| 17 | THH | $\overline{HOLD}$ hold time | 10 | — | ns | 4.5V ≤ VCC ≤ 5.5V (I) |
| | | | 20 | — | ns | 2.5V ≤ VCC < 5.5V (I, E) |
| 18 | THZ | $\overline{HOLD}$ low to output High-Z | — | 15 | ns | 4.5V ≤ VCC ≤ 5.5V (I) |
| | | | — | 30 | ns | 2.5V ≤ VCC < 5.5V (I, E) **(Note 1)** |
| 19 | THV | $\overline{HOLD}$ high to output valid | — | 15 | ns | 4.5V ≤ VCC ≤ 5.5V (I) |
| | | | — | 30 | ns | 2.5V ≤ VCC < 5.5V (I, E) |
| 20 | TREL | $\overline{CS}$ High to Standby mode | — | 100 | µs | — |
| 21 | TPD | $\overline{CS}$ High to Deep power-down | — | 100 | µs | — |
| 22 | TCE | Chip erase cycle time | — | 10 | ms | — |
| 23 | TSE | Sector erase cycle time | — | 10 | ms | — |

**Note 1:** This parameter is periodically sampled and not 100% tested.

**2:** This parameter is not tested but established by characterization and qualification.

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**TABLE 1-2: AC CHARACTERISTICS (CONTINUED)**

| AC CHARACTERISTICS | | | Electrical Characteristics:<br>Industrial (I): TA = -40°C to +85°C VCC = 2.5V to 5.5V<br>Extended (E): TA = -40°C to +125°C VCC = 2.5V to 5.5V | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristic** | **Min.** | **Max.** | **Units** | **Conditions** |
| 24 | TWC | Internal write cycle time | — | 5 | ms | Byte or Page mode and Page Erase |
| 25 | — | Endurance | 1M | — | E/W Cycles | Page mode, 25°C, 5.5V (**Note 2**) |

**Note 1:** This parameter is periodically sampled and not 100% tested.

**2:** This parameter is not tested but established by characterization and qualification.

**TABLE 1-3: AC TEST CONDITIONS**

| **AC Waveform:** | |
|---|---|
| VLO = 0.2V | — |
| VHI = VCC - 0.2V | (**Note 1**) |
| VHI = 4.0V | (**Note 2**) |
| CL = 30 pF | — |
| **Timing Measurement Reference Level** | |
| Input | 0.5 VCC |
| Output | 0.5 VCC |

**Note 1:** For VCC ≤ 4.0V

**2:** For VCC > 4.0V


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**FIGURE 1-1: HOLD TIMING**

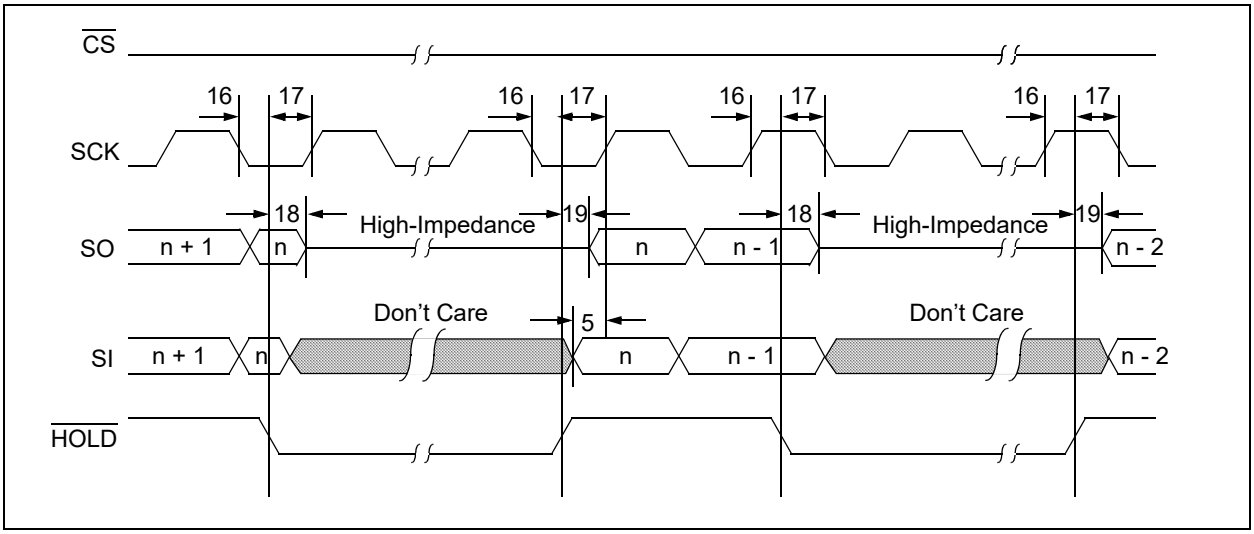



**FIGURE 1-2: SERIAL INPUT TIMING**

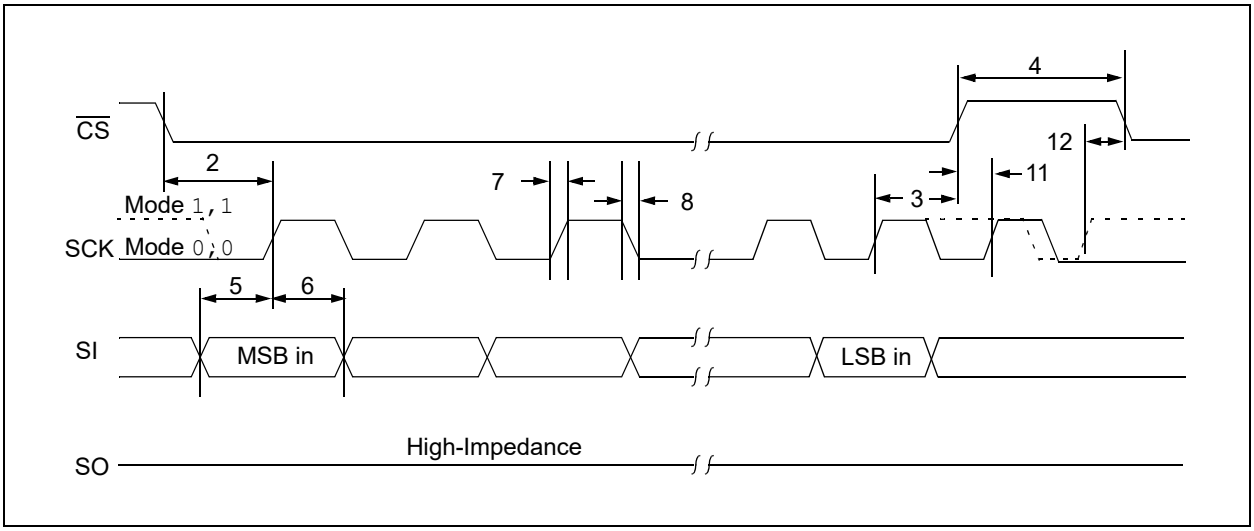
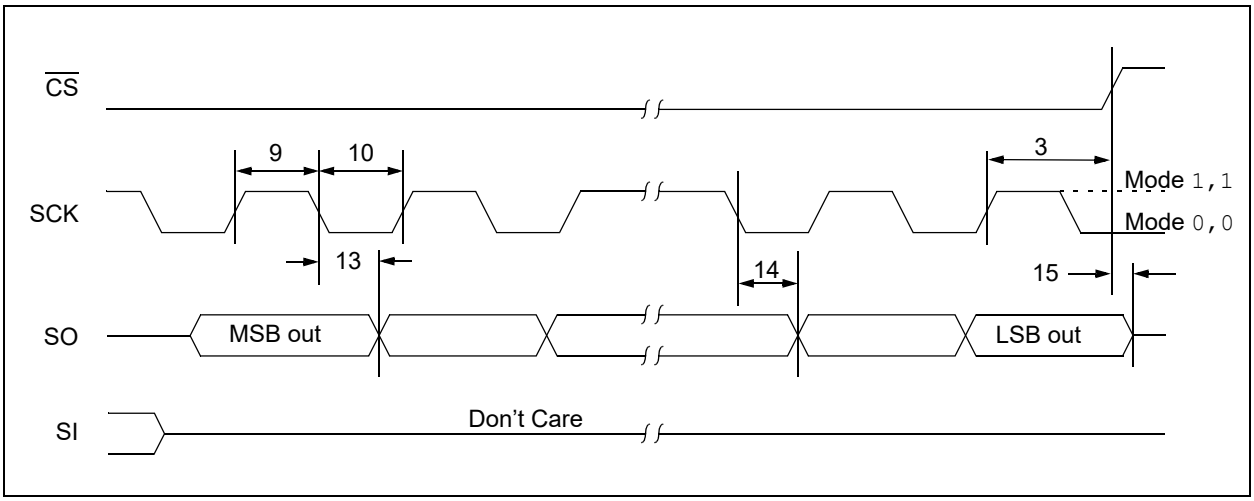



**FIGURE 1-3: SERIAL OUTPUT TIMING**





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## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

**TABLE 2-1: PIN FUNCTION TABLE**

| Name | 8-Lead DFN-S(1) | 8-Lead PDIP | 8-Lead SOIC | 8-Lead SOIJ | Function |
|---|---|---|---|---|---|
| $\overline{CS}$ | 1 | 1 | 1 | 1 | Chip Select Input |
| SO | 2 | 2 | 2 | 2 | Serial Data Output |
| $\overline{WP}$ | 3 | 3 | 3 | 3 | Write-Protect Pin |
| VSS | 4 | 4 | 4 | 4 | Ground |
| SI | 5 | 5 | 5 | 5 | Serial Data Input |
| SCK | 6 | 6 | 6 | 6 | Serial Clock Input |
| $\overline{HOLD}$ | 7 | 7 | 7 | 7 | Hold Input |
| VCC | 8 | 8 | 8 | 8 | Supply Voltage |

**Note 1:** The exposed pad on DFN-S package can be connected to VSS or left floating.

### 2.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go into Standby mode as soon as programming cycle is complete. When device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

### 2.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25LC512. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

### 2.3 Write-Protect ($\overline{WP}$)

This pin is used in conjunction with WPEN bit in STATUS register to prohibit writes to the nonvolatile bits in the STATUS register. When $\overline{WP}$ is low and WPEN is high, writing to the nonvolatile bits in the STATUS register is disabled. All other operations function normally. When $\overline{WP}$ is high, all functions, including writes to the nonvolatile bits in the STATUS register, operate normally. If the WPEN bit is set, $\overline{WP}$ low during a STATUS register write sequence will disable writing to the STATUS register. If an internal write cycle has already begun, $\overline{WP}$ going low will have no effect on the write.

The $\overline{WP}$ pin function is blocked when WPEN bit in STATUS register is low. This allows the user to install the 25LC512 in a system with $\overline{WP}$ pin grounded and still be able to write to the STATUS register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set high.

### 2.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

### 2.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a host and the 25LC512. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

### 2.6 Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to suspend transmission to the 25LC512 while in the middle of a serial sequence without having to re-transmit the entire sequence over again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence.

The $\overline{HOLD}$ pin must be brought low while SCK is low, otherwise the $\overline{HOLD}$ function will not be invoked until the next SCK high-to-low transition. The 25LC512 must remain selected during this sequence. The SI and SCK levels are “don’t cares” during the time the device is paused and any transitions on these pins will be ignored. To resume serial communication, $\overline{HOLD}$ must be brought high while the SCK pin is low, otherwise serial communication will not be resumed until the next SCK high-to-low transition.

The SO line will tri-state immediately upon a high-to-low transition of the $\overline{HOLD}$ pin, and will begin outputting again immediately upon a subsequent low-to-high transition of the $\overline{HOLD}$ pin, independent of the state of SCK.


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## 3.0 FUNCTIONAL DESCRIPTION

### 3.1 Principles of Operation

The 25LC512 is a 65,536 byte Serial EEPROM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in firmware to match the SPI protocol.

The 25LC512 contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation.

Table 3-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred MSB first, LSB last.

Data (SI) is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input and place the 25LC512 in 'HOLD' mode. After releasing the $\overline{HOLD}$ pin, operation will resume from the point when the $\overline{HOLD}$ was asserted.

**BLOCK DIAGRAM**

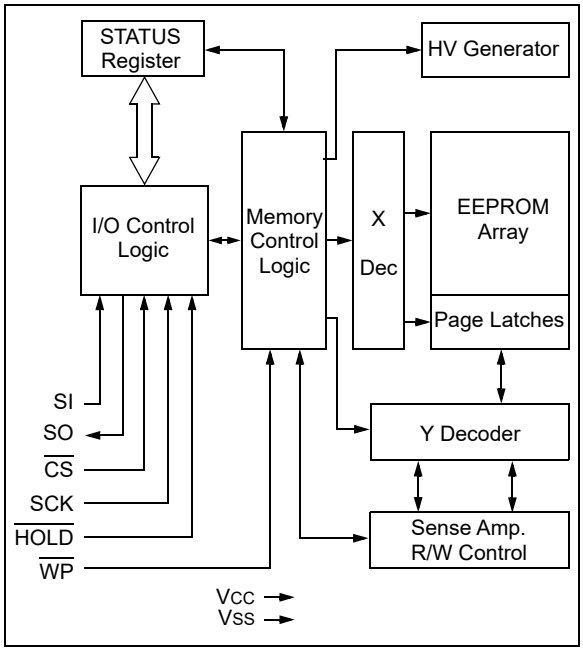



**TABLE 3-1: INSTRUCTION SET**

| Instruction Name | Instruction Format | Description |
|---|---|---|
| READ | 0000 0011 | Read data from memory array beginning at selected address |
| WRITE | 0000 0010 | Write data to memory array beginning at selected address |
| WREN | 0000 0110 | Set the write enable latch (enable write operations) |
| WRDI | 0000 0100 | Reset the write enable latch (disable write operations) |
| RDSR | 0000 0101 | Read STATUS register |
| WRSR | 0000 0001 | Write STATUS register |
| PE | 0100 0010 | Page Erase – erase one page in memory array |
| SE | 1101 1000 | Sector Erase – erase one sector in memory array |
| CE | 1100 0111 | Chip Erase – erase all sectors in memory array |
| RDID | 1010 1011 | Release from Deep power-down and read electronic signature |
| DPD | 1011 1001 | Deep Power-Down mode |

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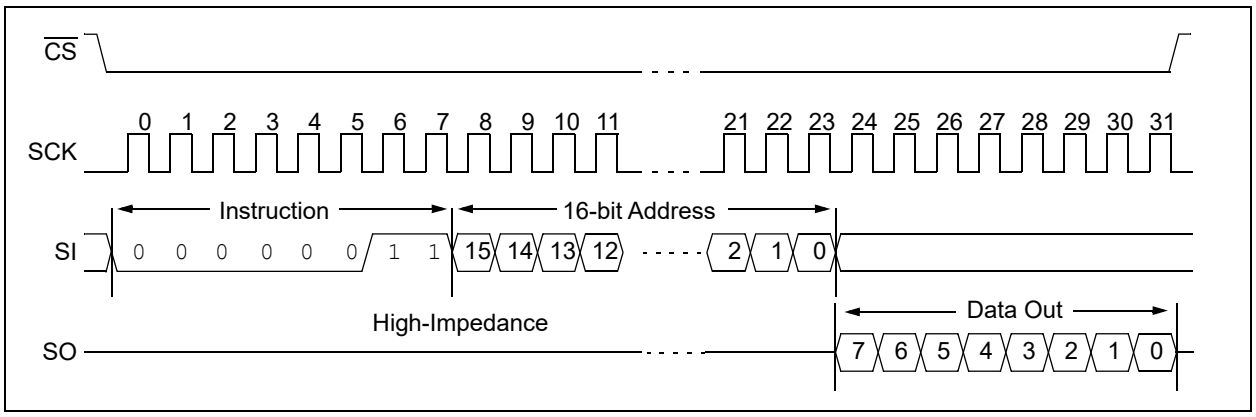
## 3.2 Read Sequence

The device is selected by pulling $\overline{CS}$ low. The 8-bit `READ` instruction is transmitted to the 25LC512 followed by the 16-bit address.

After the correct `READ` instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses.

The internal Address Pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (FFFFh), the address counter rolls over to address 0000h allowing the read cycle to be continued indefinitely. The `READ` instruction is terminated by raising the $\overline{CS}$ pin (Figure 3-1).

**FIGURE 3-1: READ SEQUENCE**





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## 3.3 Write Sequence

Prior to any attempt to write data to the 25LC512, the write enable latch must be set by issuing the WREN instruction (Figure 3-4). This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25LC512. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch.

If the write operation is initiated immediately after the WREN instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

A write sequence includes an automatic, self timed erase cycle. It is not required to erase any portion of the memory prior to issuing a WRITE instruction.

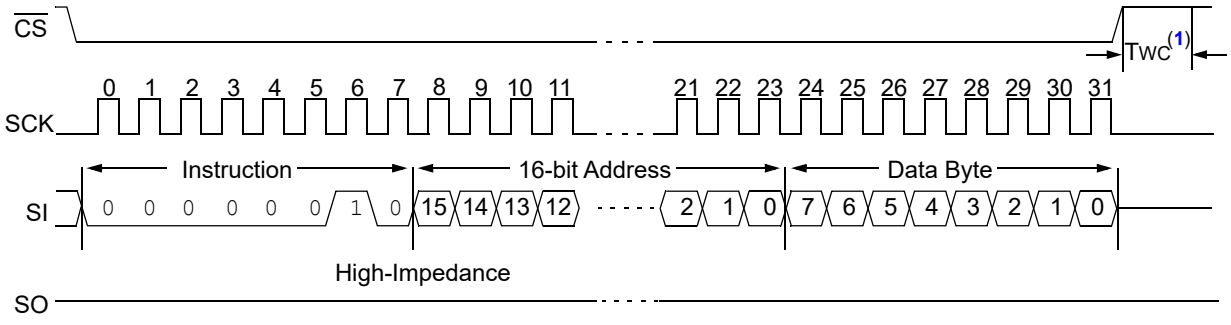
Once the write enable latch is set, the user may proceed by setting the $\overline{CS}$ low, issuing a WRITE instruction, followed by the 16-bit address, and then the data to be written. Up to 128 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page.

**Note:** When doing a write of less than 128 bytes the data in the rest of the page is refreshed along with the data bytes being written. This will force the entire page to endure a write cycle, for this reason endurance is specified per page.

**Note:** Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size'), and end at addresses that are integer multiples of page size – 1. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the Least Significant bit (D0) of the $n^{th}$ data byte has been clocked in. If $\overline{CS}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 3-2 and Figure 3-3 for more detailed illustrations on the byte write sequence and the page write sequence, respectively. While the write is in progress, the STATUS register may be read to check the status of the WPEN, WIP, WEL, BP1 and BP0 bits (Figure 3-6). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

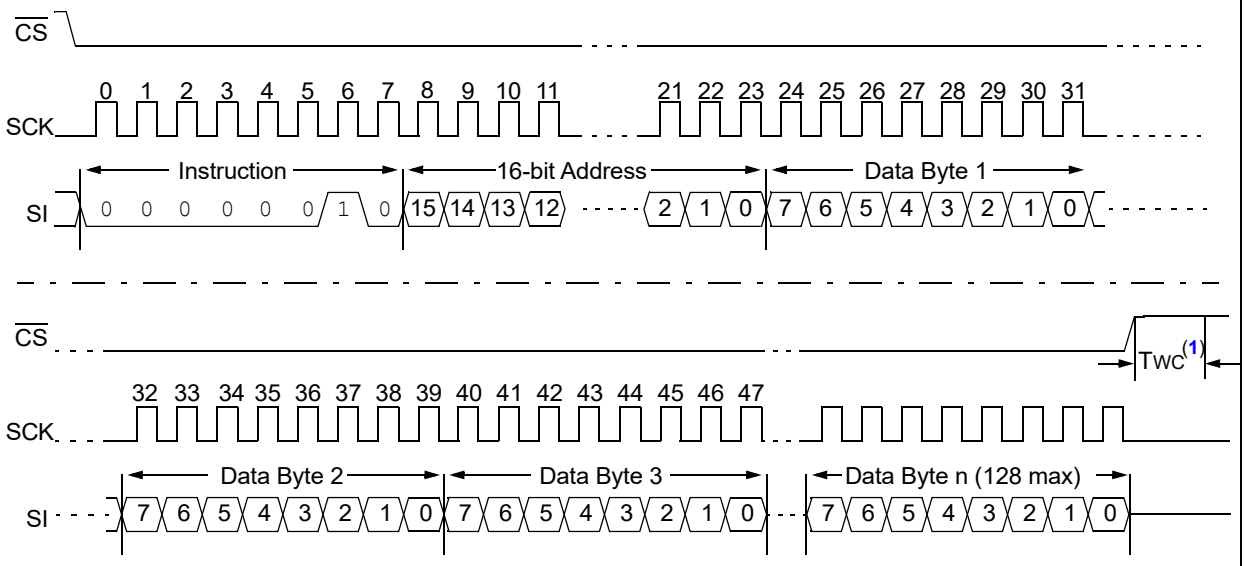
**FIGURE 3-2: BYTE WRITE SEQUENCE**




**Note 1:** This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.


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**FIGURE 3-3: PAGE WRITE SEQUENCE**




**Note 1:** This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.


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### 3.4 Write Enable (WREN) and Write Disable (WRDI)

The 25LC512 contains a write enable latch. See Table 3-4 for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed
- PE instruction successfully executed
- SE instruction successfully executed
- CE instruction successfully executed

**FIGURE 3-4: WRITE ENABLE SEQUENCE (WREN)**

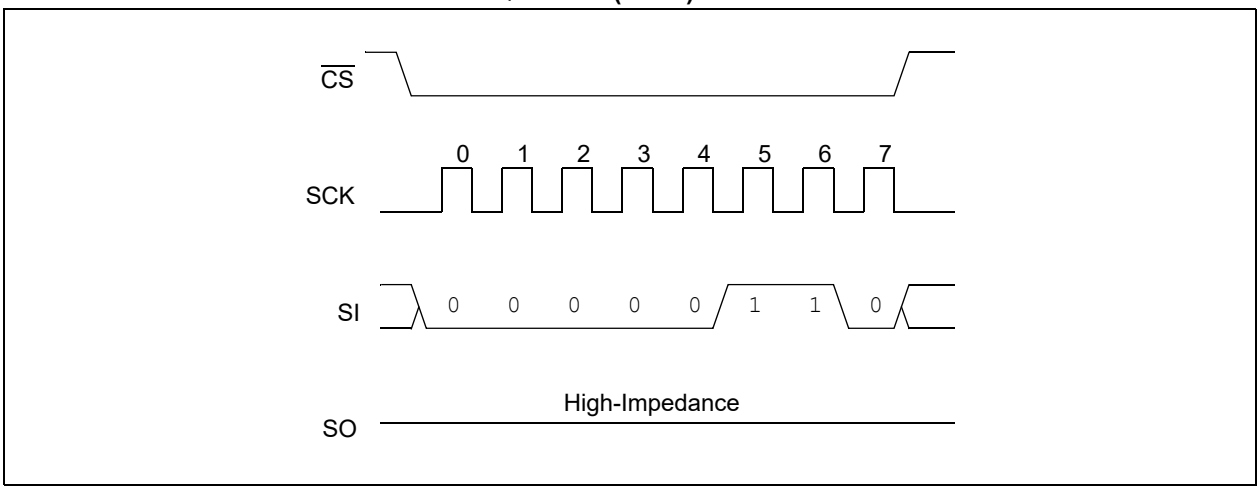
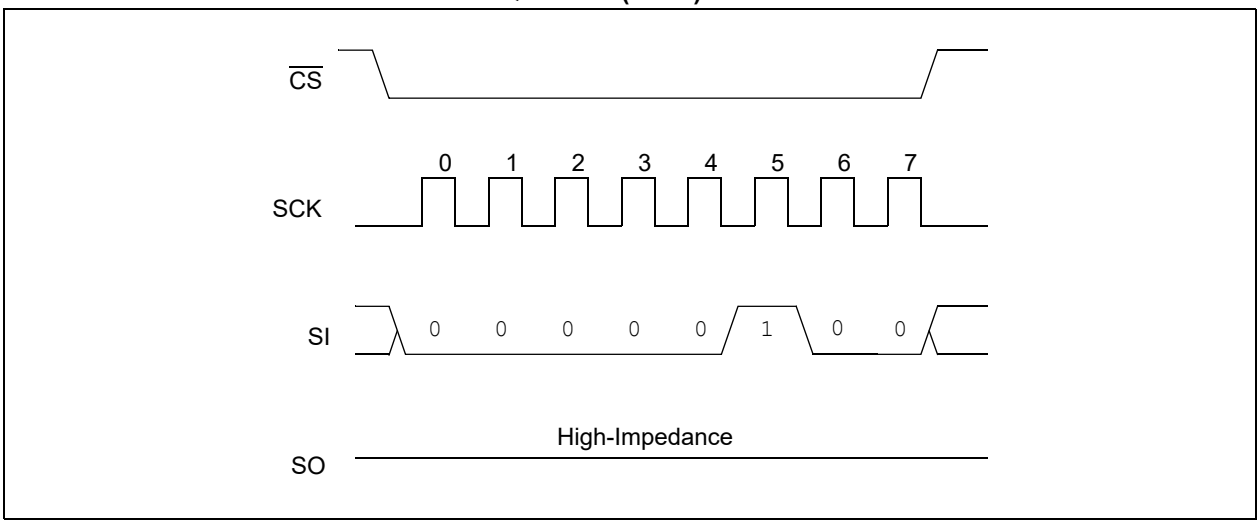



**FIGURE 3-5: WRITE DISABLE SEQUENCE (WRDI)**





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## 3.5 Read Status Register Instruction (RDSR)

The Read Status Register instruction (RDSR) provides access to the STATUS register. See Figure 3-6 for the RDSR timing sequence. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

**TABLE 3-2: STATUS REGISTER**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| W/R | – | – | – | W/R | W/R | R | R |
| WPEN | X | X | X | BP1 | BP0 | WEL | WIP |

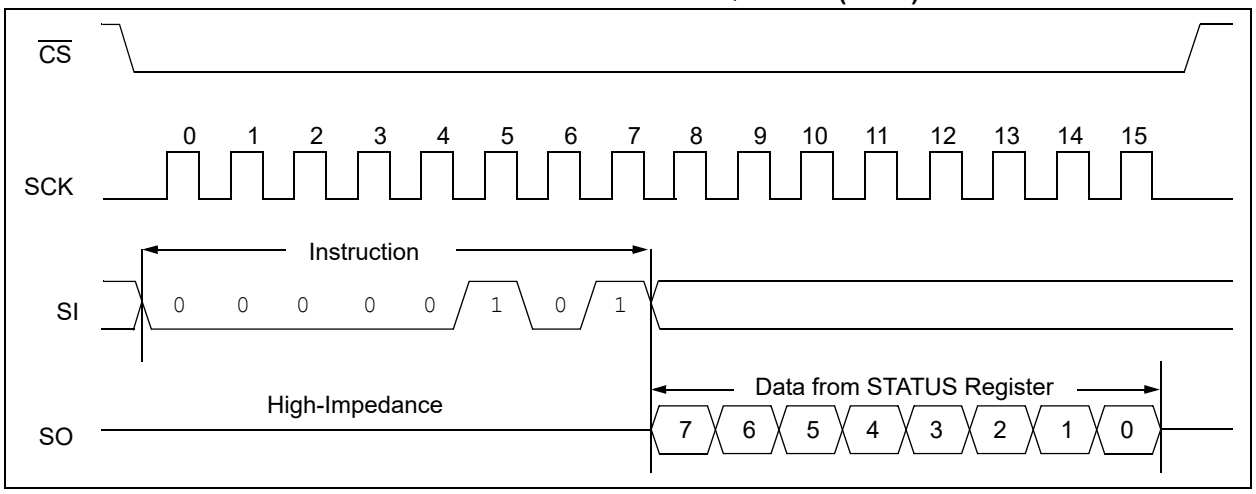
**Note:** W/R = writable/readable. R = read-only.

The **Write-In-Process (WIP)** bit indicates whether the 25LC512 is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch and is read-only. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the STATUS register. These commands are shown in Figure 3-4 and Figure 3-5.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user issuing the WRSR instruction. These bits are nonvolatile, and are shown in Table 3-3.

**FIGURE 3-6: READ STATUS REGISTER TIMING SEQUENCE (RDSR)**





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## 3.6 Write Status Register Instruction (WRSR)

The Write Status Register instruction (WRSR) allows the user to write to the nonvolatile bits in the STATUS register as shown in Table 3-2. The user is able to select one of four levels of protection for the array by writing to the appropriate bits in the STATUS register. The array is divided up into four segments. The user has the ability to write-protect none, one, two or all four of the segments of the array. The partitioning is controlled as shown in Table 3-3.

The Write-Protect Enable (WPEN) bit is a nonvolatile bit that is available as an enable bit for the $\overline{WP}$ pin. The Write-Protect ($\overline{WP}$) pin and the Write-Protect Enable (WPEN) bit in the STATUS register control the programmable hardware write-protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is low and the WPEN bit is high. Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is low. When the chip is hardware write-protected, only writes to nonvolatile bits in the STATUS register are disabled. See Table 3-4 for a matrix of functionality on the WPEN bit.

See Figure 3-7 for the WRSR timing sequence.

**TABLE 3-3: ARRAY PROTECTION**

| BP1 | BP0 | Array Addresses Write-Protected | Array Addresses Unprotected |
|---|---|---|---|
| 0 | 0 | none | All (Sectors 0, 1, 2 & 3) (0000h-FFFFh) |
| 0 | 1 | Upper 1/4 (Sector 3) (C000h-FFFFh) | Lower 3/4 (Sectors 0, 1 & 2) (0000h-BFFFh) |
| 1 | 0 | Upper 1/2 (Sectors 2 & 3) (8000h-FFFFh) | Lower 1/2 (Sectors 0 & 1) (0000h-7FFFh) |
| 1 | 1 | All (Sectors 0, 1, 2 & 3) (0000h-FFFFh) | none |

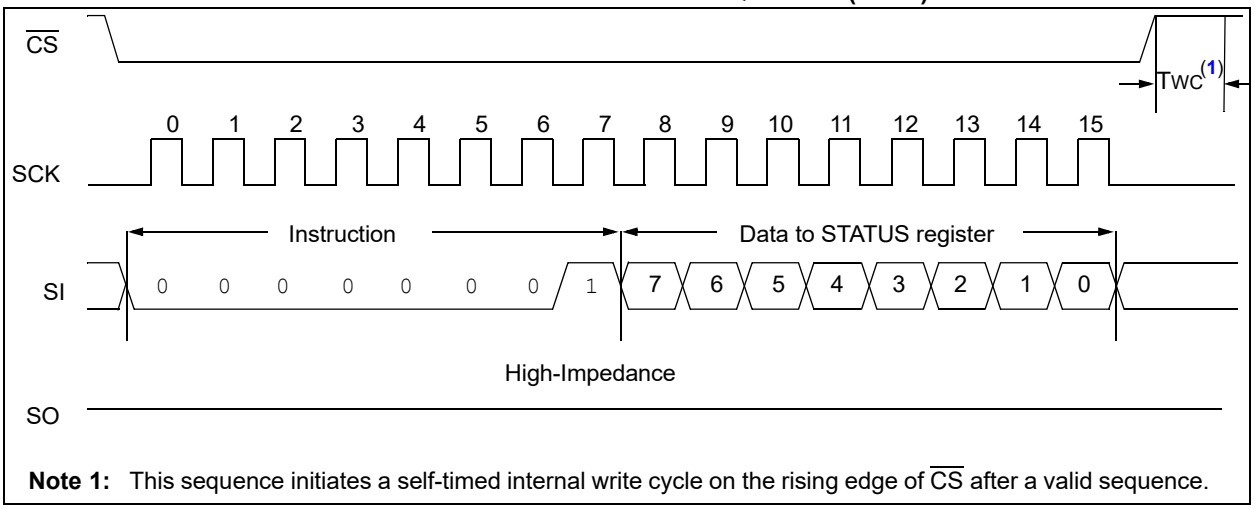
**TABLE 3-4: WRITE-PROTECT FUNCTIONALITY MATRIX**

| WEL (SR bit 1) | WPEN (SR bit 7) | $\overline{WP}$ (pin 3) | Protected Blocks | Unprotected Blocks | STATUS Register |
|---|---|---|---|---|---|
| 0 | x | x | Protected | Protected | Protected |
| 1 | 0 | x | Protected | Writable | Writable |
| 1 | 1 | 0 (low) | Protected | Writable | Protected |
| 1 | 1 | 1 (high) | Protected | Writable | Writable |

x = don't care


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**FIGURE 3-7: WRITE STATUS REGISTER TIMING SEQUENCE (WRSR)**




**Note 1:** This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.


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## 3.7 PAGE ERASE

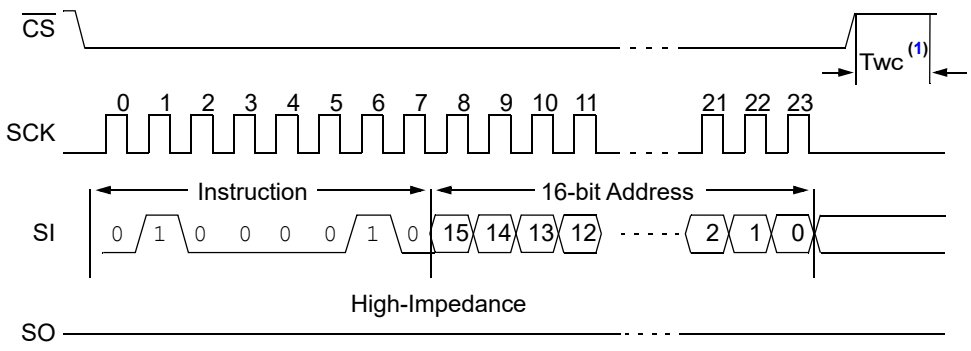
The PAGE ERASE instruction will erase all bits (FFh) inside the given page. A Write Enable (WREN) instruction must be given prior to attempting a PAGE ERASE. This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25LC512. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch.

The PAGE ERASE instruction is entered by driving $\overline{CS}$ low, followed by the instruction code (Figure 3-8) and two address bytes. Any address inside the page to be erased is a valid address.

$\overline{CS}$ must then be driven high after the last bit of the address or the PAGE ERASE will not execute. Once the $\overline{CS}$ is driven high the self-timed PAGE ERASE cycle is started. The WIP bit in the STATUS register can be read to determine when the PAGE ERASE cycle is complete.

If a PAGE ERASE instruction is given to an address that has been protected by the Block Protect bits (BP0, BP1) then the sequence will be aborted and no erase will occur.

**FIGURE 3-8: PAGE ERASE SEQUENCE**




**Note 1:** This sequence initiates a self-timed internal write cycle on the rising edge of CS after a valid sequence.


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## 3.8 SECTOR ERASE

The SECTOR ERASE instruction will erase all bits (FFh) inside the given sector. A Write Enable (WREN) instruction must be given prior to attempting a SECTOR ERASE. This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25LC512. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch.

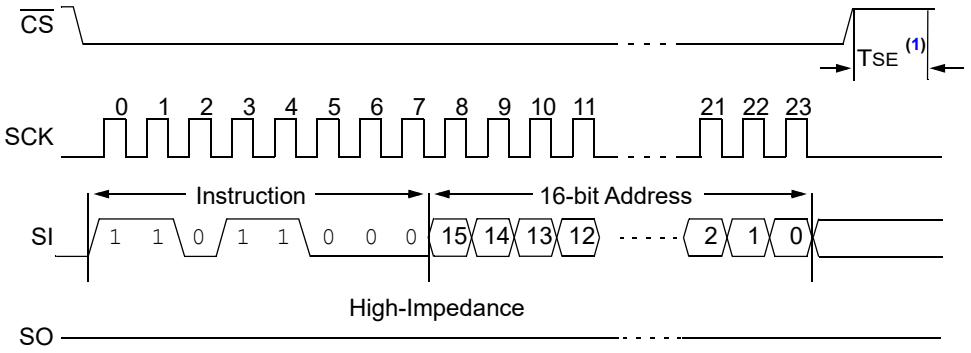
The SECTOR ERASE instruction is entered by driving $\overline{CS}$ low, followed by the instruction code (Figure 3-9) and two address bytes. Any address inside the sector to be erased is a valid address.

$\overline{CS}$ must then be driven high after the last bit of the address or the SECTOR ERASE will not execute. Once the $\overline{CS}$ is driven high the self-timed SECTOR ERASE cycle is started. The WIP bit in the STATUS register can be read to determine when the SECTOR ERASE cycle is complete.

If a SECTOR ERASE instruction is given to an address that has been protected by the Block Protect bits (BP0, BP1) then the sequence will be aborted and no erase will occur.

See Table 3-3 for Sector Addressing.

**FIGURE 3-9: SECTOR ERASE SEQUENCE**




**Note 1:** This sequence initiates a self-timed internal write cycle on the rising edge of CS after a valid sequence.


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## 3.9 CHIP ERASE

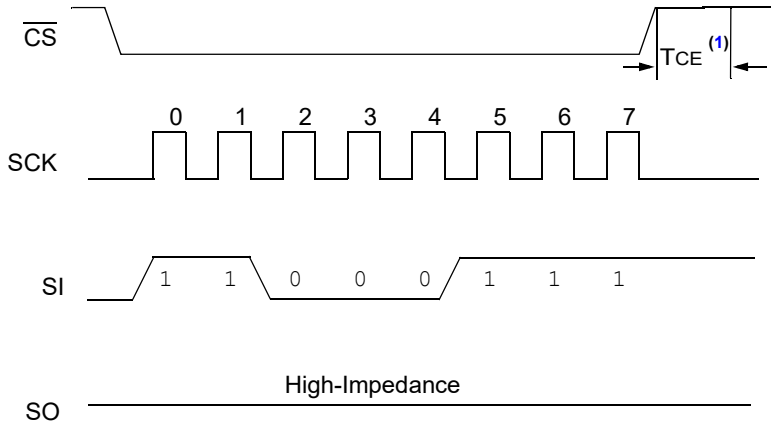
The CHIP ERASE instruction will erase all bits (FFh) in the array. A Write Enable (WREN) instruction must be given prior to executing a CHIP ERASE. This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25LC512. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch.

The CHIP ERASE instruction is entered by driving the $\overline{CS}$ low, followed by the instruction code (Figure 3-10) onto the SI line.

The $\overline{CS}$ pin must be driven high after the eighth bit of the instruction code has been given or the CHIP ERASE instruction will not be executed. Once the $\overline{CS}$ pin is driven high the self-timed CHIP ERASE instruction begins. While the device is executing the CHIP ERASE instruction the WIP bit in the STATUS register can be read to determine when the CHIP ERASE instruction is complete.

The CHIP ERASE instruction is ignored if either of the Block Protect bits (BP0, BP1) are set, meaning ¼, ½, or all of the array is protected.

**FIGURE 3-10: CHIP ERASE SEQUENCE**




**Note 1:** This sequence initiates a self-timed internal write cycle on the rising edge of CS after a valid sequence.


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## 3.10 DEEP POWER-DOWN MODE

Deep Power-Down mode of the 25LC512 is its lowest power consumption state. The device will not respond to any of the Read or Write commands while in Deep Power-Down mode, and therefore it can be used as an additional software write protection feature.

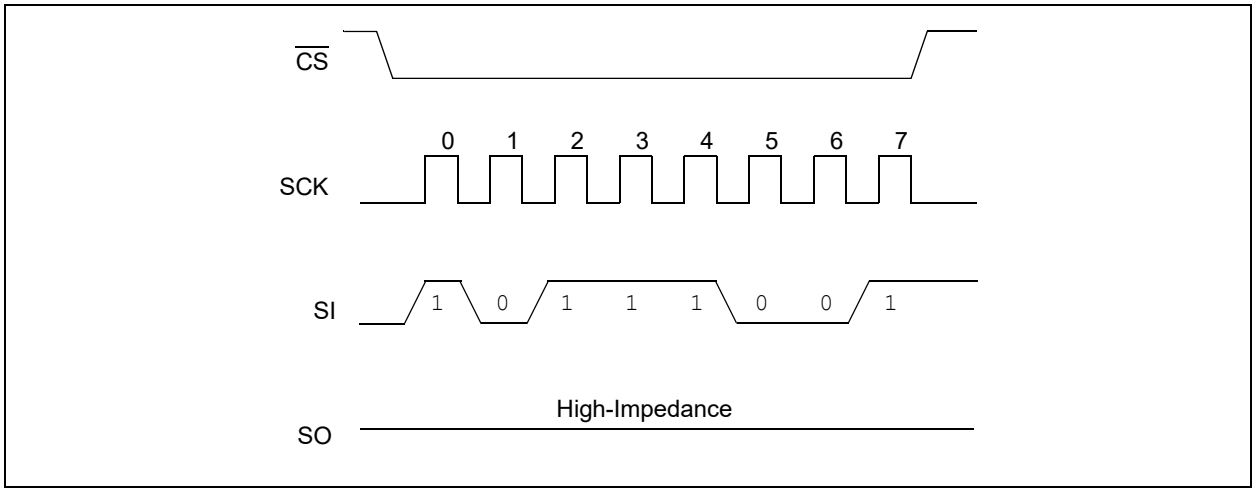
The Deep Power-Down mode is entered by driving $\overline{CS}$ low, followed by the instruction code (Figure 3-11) onto the SI line, followed by driving $\overline{CS}$ high.

If the $\overline{CS}$ pin is not driven high after the eighth bit of the instruction code has been given, the device will not execute Deep power-down. Once the $\overline{CS}$ line is driven high there is a delay ($T_{DP}$) before the current settles to its lowest consumption.

All instructions given during Deep Power-Down mode are ignored except the Read Electronic Signature command (RDID). The RDID command will release the device from Deep power-down and outputs the electronic signature on the SO pin, and then returns the device to Standby mode after delay ($T_{REL}$)

Deep Power-Down mode automatically releases at device power-down. Once power is restored to the device it will power-up in the Standby mode.

**FIGURE 3-11: DEEP POWER-DOWN SEQUENCE**





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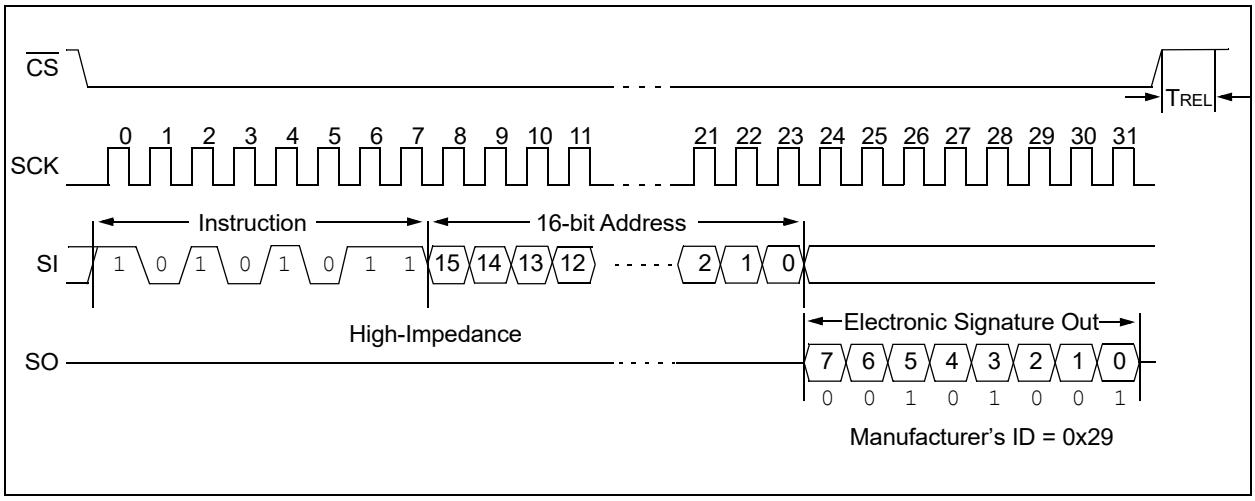
## 3.11 RELEASE FROM DEEP POWER-DOWN AND READ ELECTRONIC SIGNATURE

Once the device has entered Deep Power-Down mode all instructions are ignored except the Release from Deep Power-down and Read Electronic Signature command. This command can also be used when the device is not in Deep power-down to read the electronic signature out on the SO pin unless another command is being executed such as Erase, Program or Write Status Register.

Release from Deep Power-Down mode and Read Electronic Signature is entered by driving $\overline{CS}$ low, followed by the RDID instruction code (Figure 3-12) and then a dummy address of 16 bits (A15-A0). After the last bit of the dummy address is clock in, the 8-bit Electronic Signature is clocked out on the SO pin.

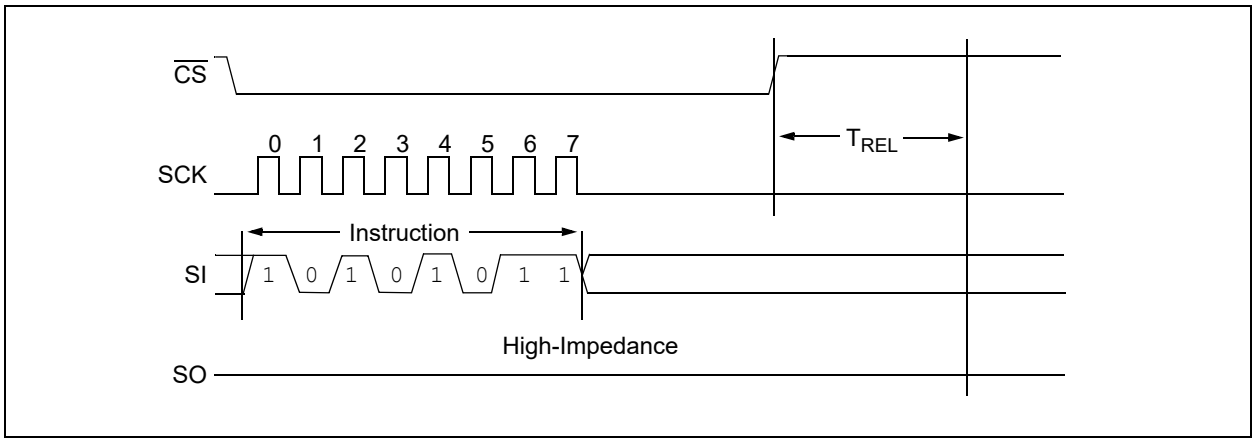
After the signature has been read out at least once, the sequence can be terminated by driving $\overline{CS}$ high. After a delay of $T_{REL}$, the device will then return to Standby mode and will wait to be selected so it can be given new instructions. If additional clock cycles are sent after the electronic signature has been read once, it will continue to output the signature on the SO line until the sequence is terminated.

**FIGURE 3-12: RELEASE FROM DEEP POWER-DOWN AND READ ELECTRONIC SIGNATURE**




Driving $\overline{CS}$ high after the 8-bit RDID command but before the Electronic Signature has been transmitted will still ensure the device will be taken out of Deep Power-Down mode, as shown in Figure 3-13.

**FIGURE 3-13: RELEASE FROM DEEP POWER-DOWN AND READ ELECTRONIC SIGNATURE**





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## 4.0 DATA PROTECTION

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or STATUS register write, the write enable latch is reset
- $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

## 5.0 POWER-ON STATE

The 25LC512 powers on in the following state:

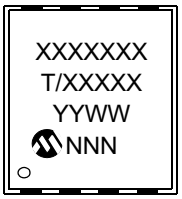
- The device is in low-power Standby mode ($\overline{CS}$ = 1)
- The write enable latch is reset
- SO is in high-impedance state
- A high-to-low-level transition on $\overline{CS}$ is required to enter active state


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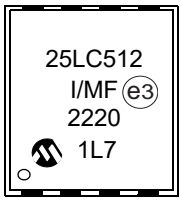
## 6.0 PACKAGING INFORMATION

### 6.1 Package Marking Information

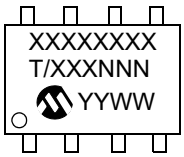
8-Lead DFN-S



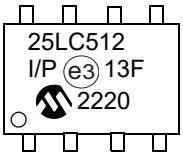

Example:



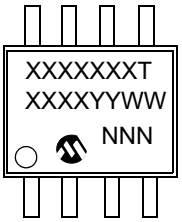

8-Lead PDIP



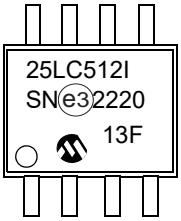

Example:



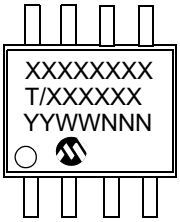

8-Lead SOIC



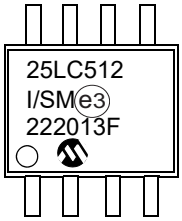

Example:




8-Lead SOIJ




Example:




| 1st Line Marking Codes | | | | |
|---|---|---|---|---|
| **Device** | **DFN-S** | **PDIP** | **SOIC** | **SOIJ** |
| 25LC512 | 25LC512 | 25LC512 | 25LC512T | 25LC512 |

**Legend:**

| | | |
|---|---|---|
| XX...X | Part number or part number code |
| T | Temperature (I, E) |
| Y | Year code (last digit of calendar year) |
| YY | Year code (last 2 digits of calendar year) |
| WW | Week code (week of January 1 is week '01') |
| NNN | Alphanumeric traceability code (2 characters for small packages) |
| (e3) | RoHS-compliant JEDEC® designator for Matte Tin (Sn) |

**Note**: For very small packages with no room for the RoHS-compliant JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

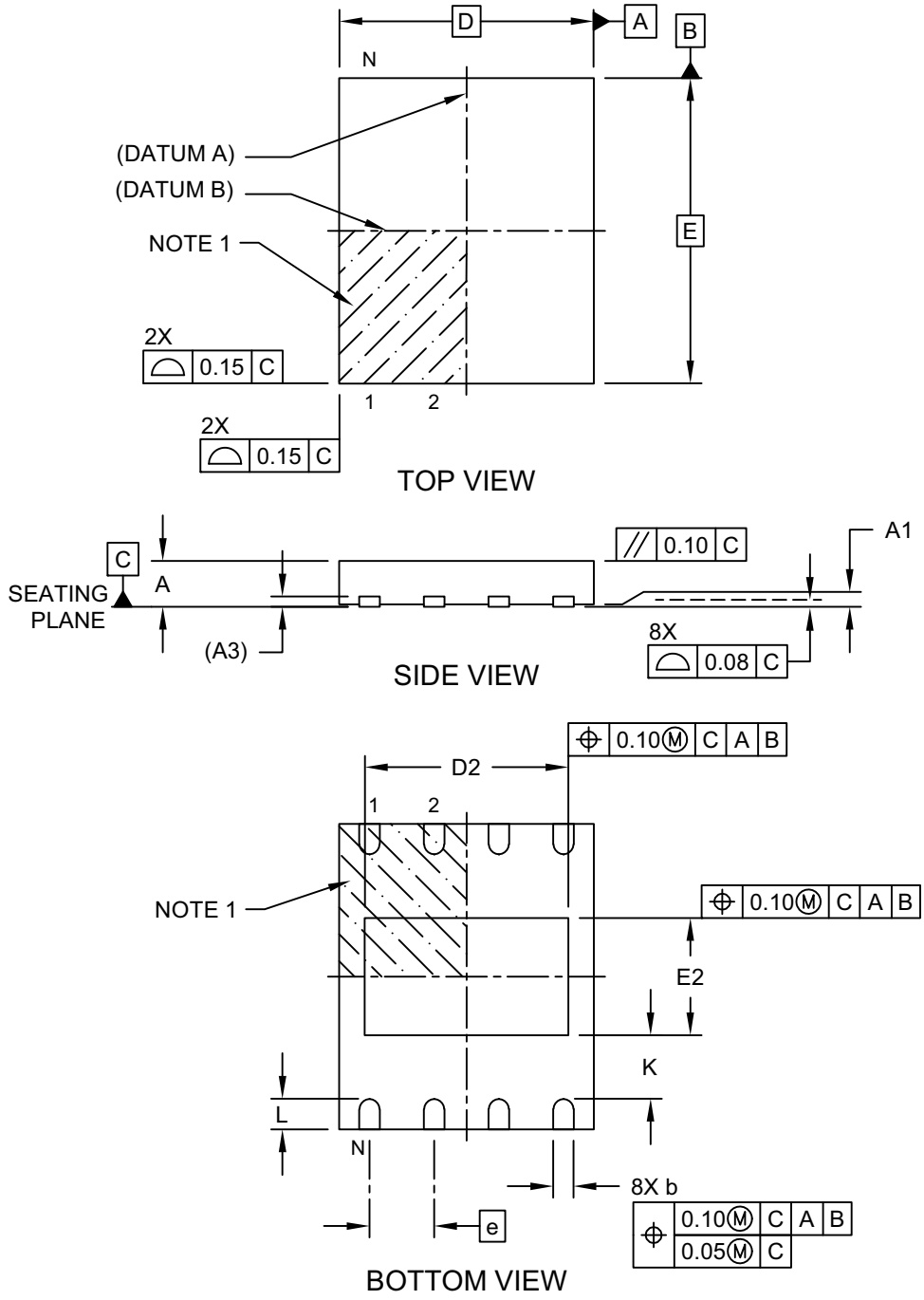
**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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**8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S]**
**Saw Singulated**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

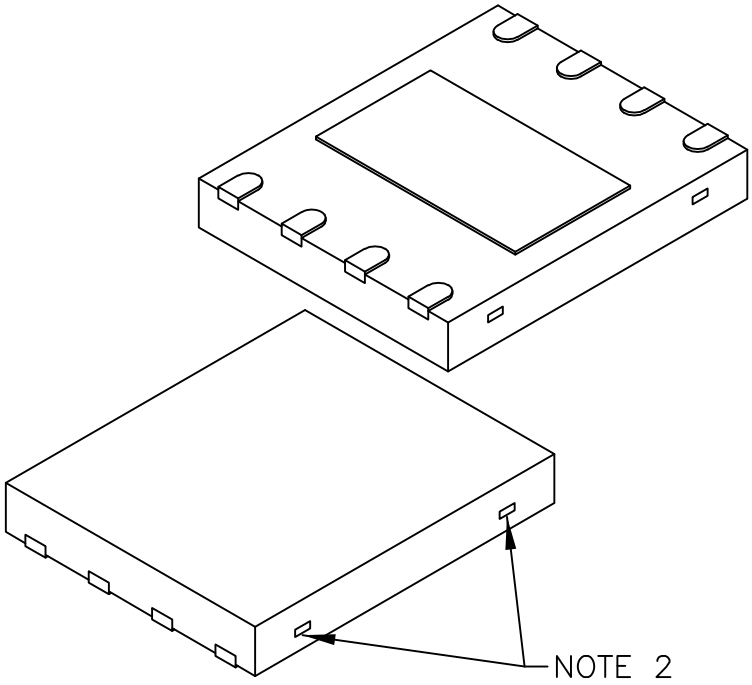



Microchip Technology Drawing C04-122 Rev C Sheet 1 of 2


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**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | 0.80 | 0.85 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 5.00 BSC | |
| Exposed Pad Length | D2 | 3.90 | 4.00 | 4.10 |
| Overall Width | E | | 6.00 BSC | |
| Exposed Pad Width | E2 | 2.20 | 2.30 | 2.40 |
| Terminal Width | b | 0.30 | 0.40 | 0.50 |
| Terminal Length | L | 0.50 | 0.60 | 0.75 |
| Terminal-to-Exposed-Pad | K | 0.20 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one ore more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

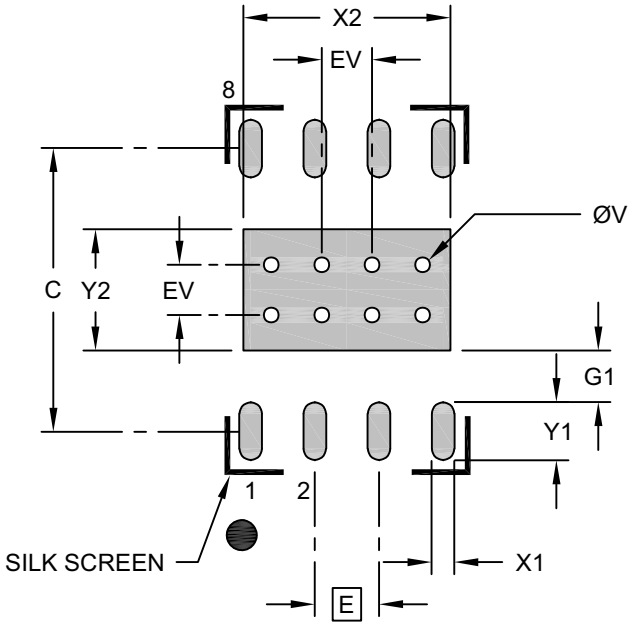
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## 8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Optional Center Pad Width | X2 | | | 2.40 |
| Optional Center Pad Length | Y2 | | | 4.10 |
| Contact Pad Spacing | C | | 5.60 | |
| Contact Pad Width (X20) | X1 | | | 0.45 |
| Contact Pad Length (X20) | Y1 | | | 1.15 |
| Contact Pad to Center Pad (X20) | G1 | 0.20 | | |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

Notes:

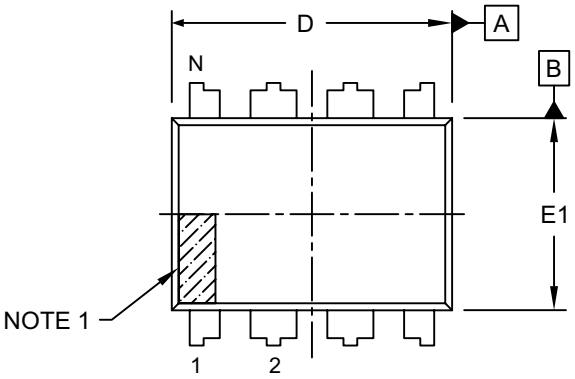
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2122 Rev C

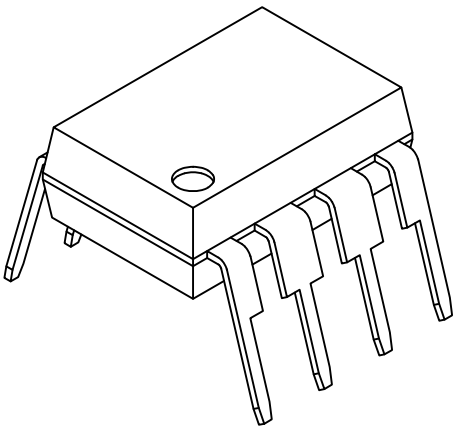

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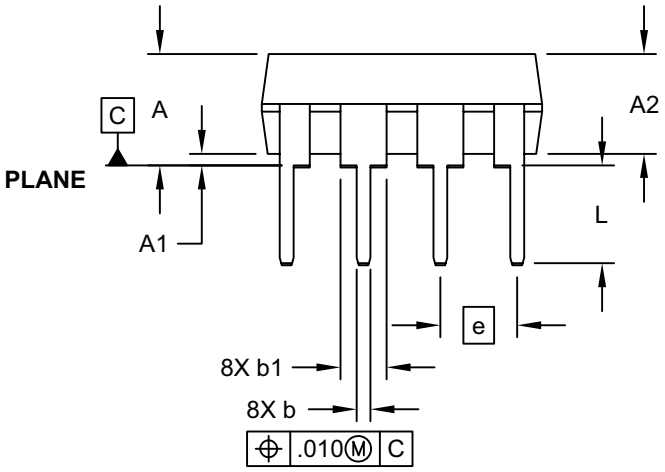
### 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

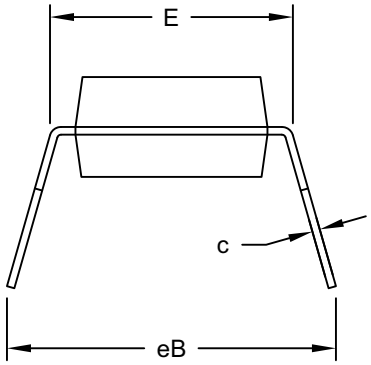



TOP VIEW






SIDE VIEW



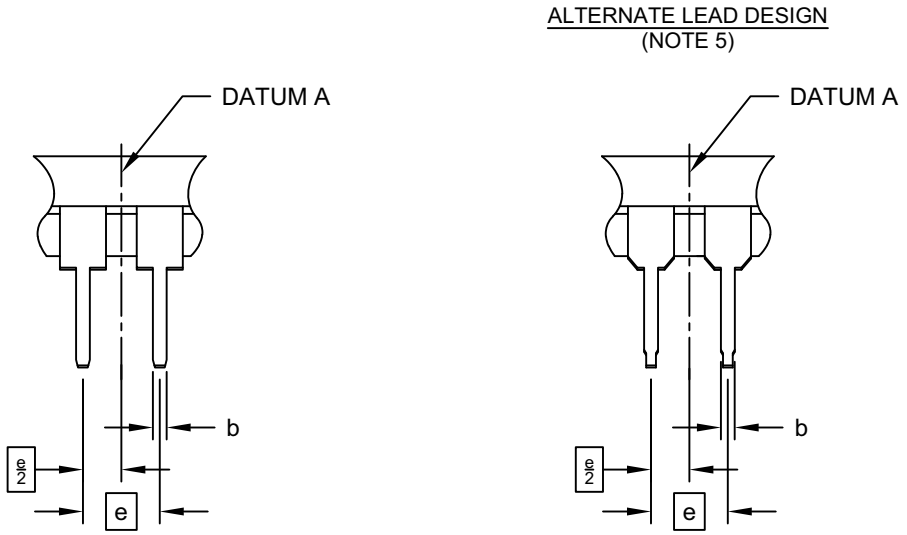

END VIEW

Microchip Technology Drawing No. C04-018-P Rev F Sheet 1 of 2


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## 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | - | - | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | - | - |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | - | - | .430 |

Notes:

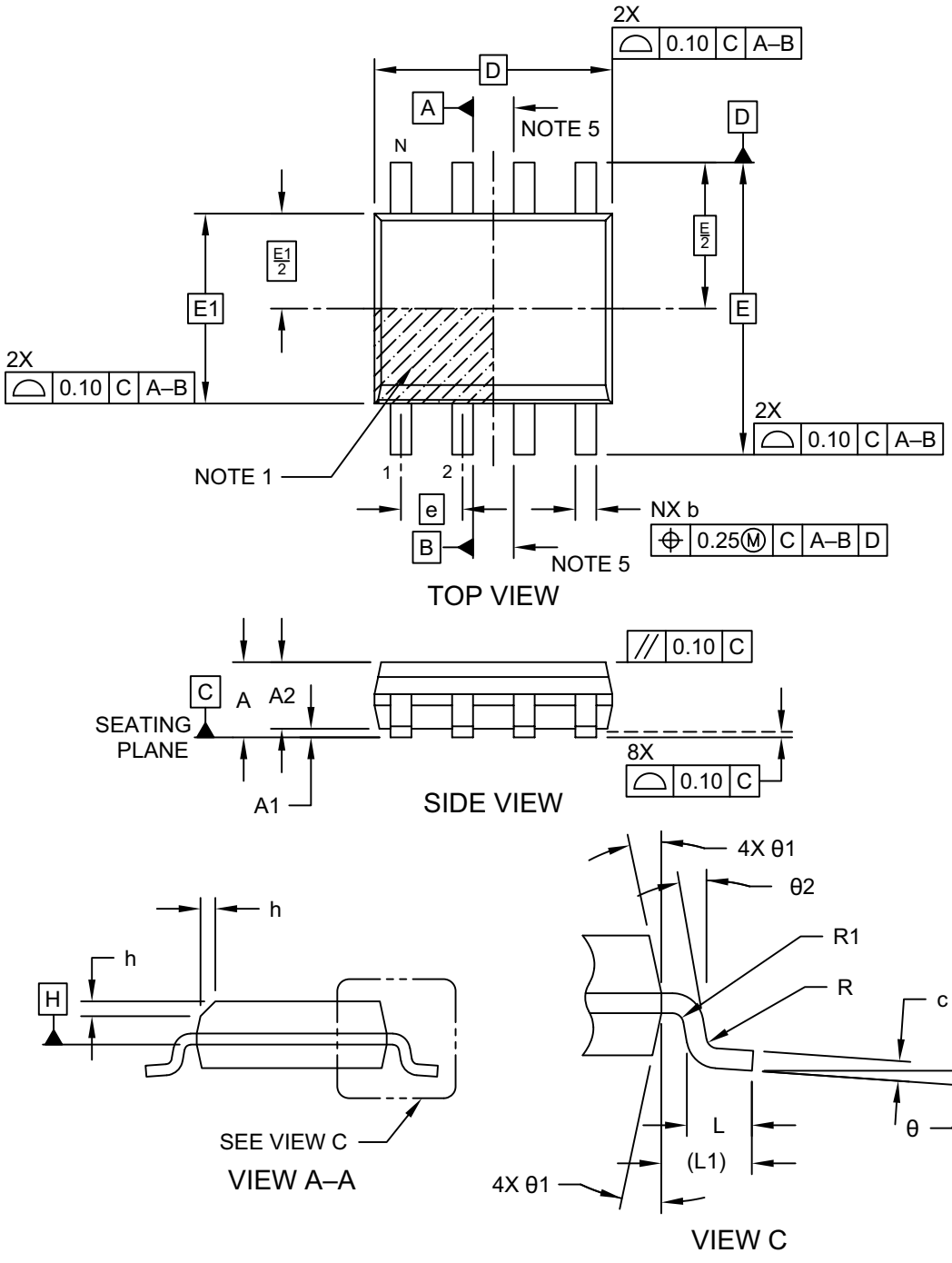
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

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## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

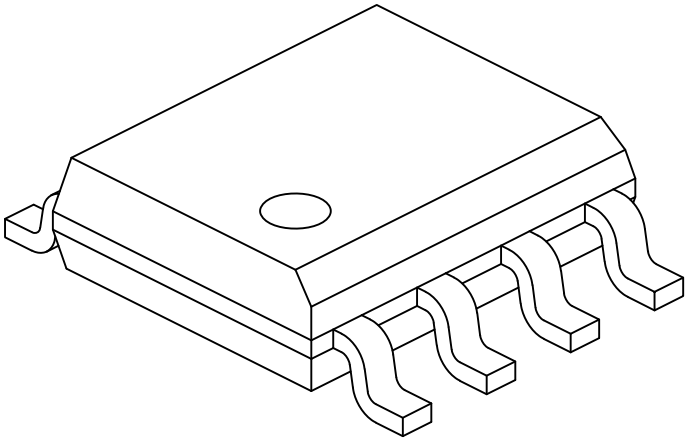



Microchip Technology Drawing No. C04-057-SN Rev J Sheet 1 of 2


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## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | - |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 4.90 BSC | |
| Chamfer (Optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Lead Bend Radius | R | 0.07 | – | – |
| Lead Bend Radius | R1 | 0.07 | – | – |
| Foot Angle | θ | 0° | – | 8° |
| Mold Draft Angle | θ1 | 5° | – | 15° |
| Lead Angle | θ2 | 0° | – | 8° |

Notes:

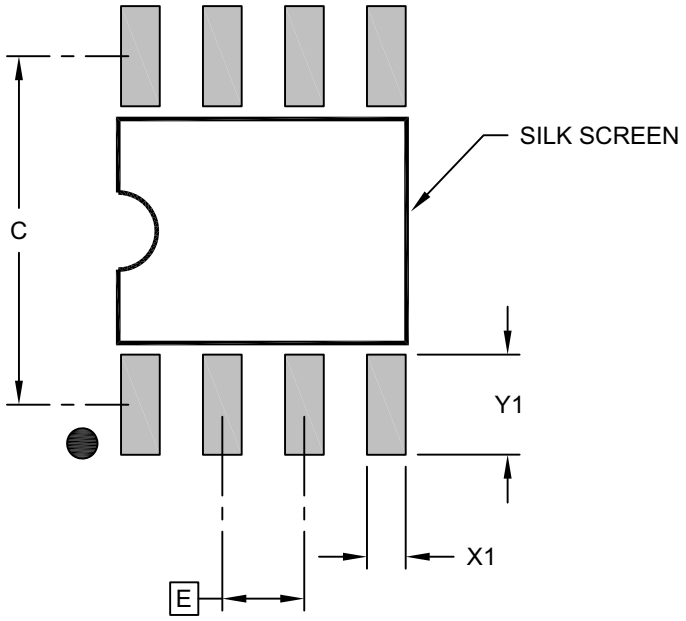
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev J Sheet 2 of 2


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## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

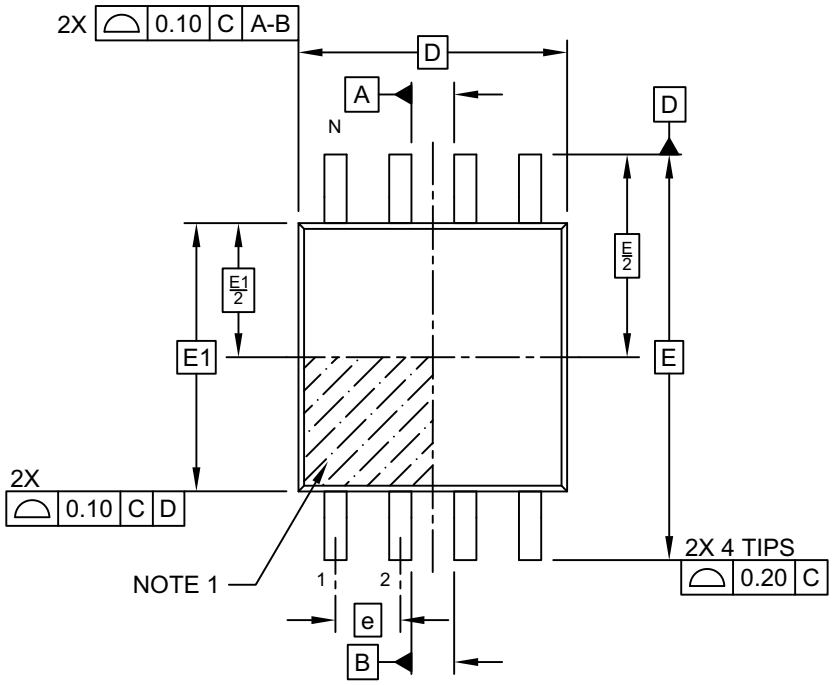
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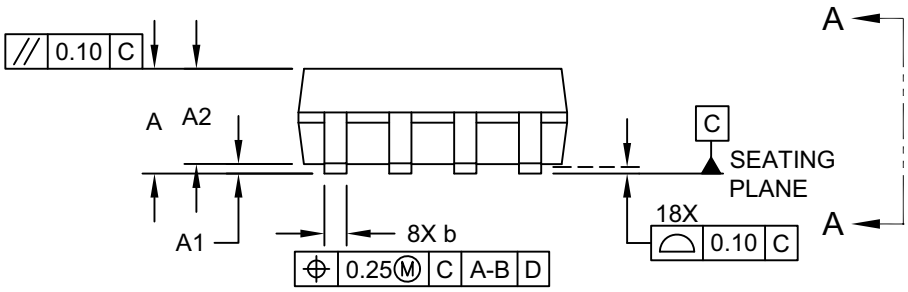
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### 8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm (.208 Inch) Body [SOIJ]

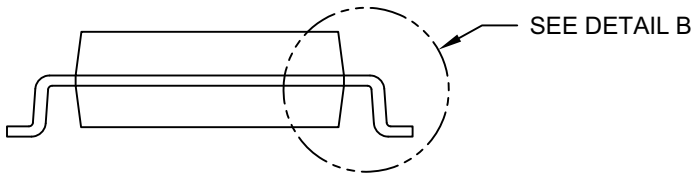
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW



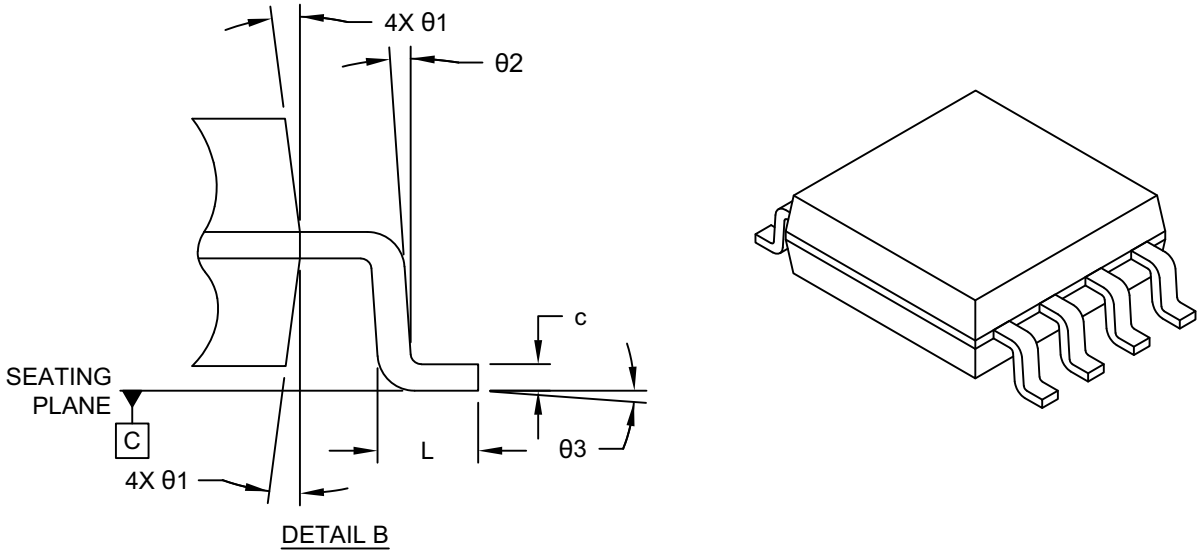

VIEW A–A

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## 8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm (.208 Inch) Body [SOIJ]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | 1.77 | – | 2.03 |
| Standoff § | A1 | 0.05 | – | 0.25 |
| Molded Package Thickness | A2 | 1.75 | – | 1.98 |
| Overall Length | D | | 5.26 BSC | |
| Overall Width | E | | 7.94 BSC | |
| Molded Package Width | E1 | | 5.25 BSC | |
| Terminal Width | b | 0.36 | – | 0.51 |
| Terminal Thickness | c | 0.15 | – | 0.25 |
| Terminal Length | L | 0.51 | – | 0.76 |
| Foot Angle | θ1 | 0° | – | 8° |
| Lead Angle | θ2 | 0° | – | 8° |
| Mold Draft Angle | θ3 | – | – | 15° |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. SOIJ – JEITA/EIAJ Standard, Formerly called SOIC
3. § – Significant Characteristic
4. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
5. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

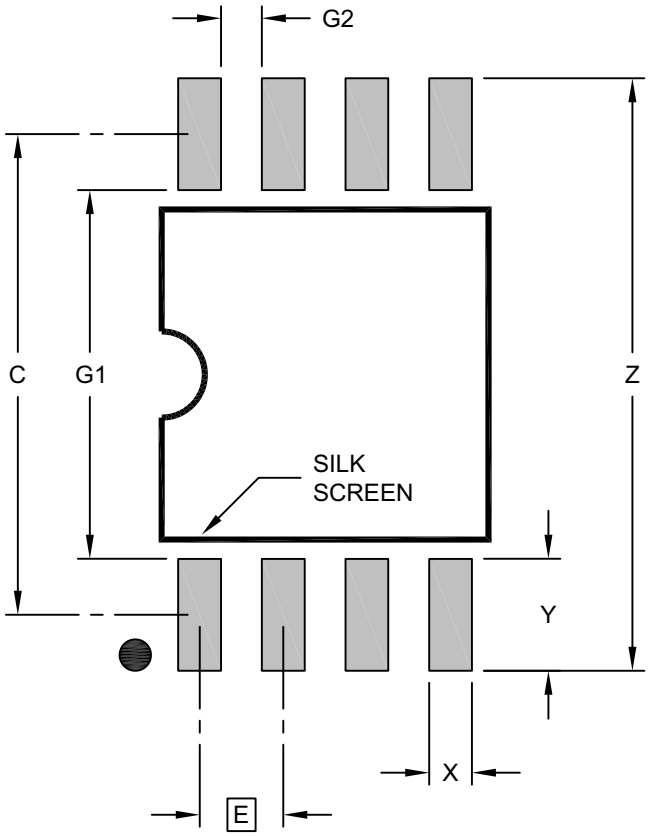
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### 8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm (.208 Inch) Body [SOIJ]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Overall Width | Z | | | 9.00 |
| Contact Pad Spacing | C | | 7.30 | |
| Contact Pad Width (X8) | X | | | 0.65 |
| Contact Pad Length (X8) | Y | | | 1.70 |
| Contact Pad to Contact Pad (X4) | G1 | 5.60 | | |
| Contact Pad to Contact Pad (X6) | G2 | 0.62 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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# APPENDIX A: REVISION HISTORY

## Revision E (07/2022)

Fixed clock bit count and page size errors on Byte Write and Page Write sequences. Made minor grammar and punctuation fixes throughout the document. Updated SOIC and SOIJ package drawings.

## Revision D (08/2021)

Updated Pin Description section; Updated Package Drawings; Added Product Identification System for Automotive; Replaced terminology “Master” and “Slave” with “Host” and “Client”, respectively; Reformatted some sections for better readability.

## Revision C (05/2010)

Revised Table 1-2, Param. No. 25 Conditions; Revised Section 2.2, added note; Updated SOIJ package drawings.

## Revision B (05/2008)

Modified parameter D006 in Table 1-1; Revised Package Marking Information; Replaced Package Drawings; Revised Product ID section.

## Revision A (10/2007)

Original release.

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## PRODUCT IDENTIFICATION SYSTEM (NON-AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X[1] | – | X | /XX |
|---|---|---|---|---|
| Device | Tape and Reel | | Temp Range | Package |

| | | | |
|---|---|---|---|
| **Device:** | 25LC512 | | 512-Kbit, 2.5V, 128-Byte Page SPI Serial EEPROM |
| **Tape & Reel:** | Blank | = | Standard packaging (tube) |
| | T | = | Tape & Reel[1] |
| **Temperature Range:** | I | = | -40°C to+85°C (Industrial) |
| | E | = | -40°C to+125°C (Extended) |
| **Package:** | MF | = | Plastic Dual Flat, No Lead Package 5 x 6 x 0.85 mm Body, 8-lead (DFN-S) |
| | P | = | Plastic Dual In-Line - 300 mil Body, 8-lead (PDIP) |
| | SN | = | Plastic Small Outline - Narrow, 3.90 mm Body, 8-lead (SOIC) |
| | SM | = | Plastic Small Outline - Wide, 5.28 mm Body, 8-lead (SOIJ) |

**Examples:**

a) 25LC512-I/SM = 512-Kbit, 2.5V Serial EEPROM, Industrial temperature, Tape and Reel, SOIC package

b) 25LC512-I/SM = 512-Kbit, 2.5V Serial EEPROM, Industrial temperature, SOIJ package

c) 25LC512-I/P = 512-Kbit, 2.5V Serial EEPROM, Industrial temperature, PDIP package

d) 25LC512T-E/MF = 512-Kbit, 2.5V Serial EEPROM, Extended temperature, Tape and Reel, DFN-S package

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.


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## PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X[1] | – | X | /XX | XXX[2,3] |
|---|---|---|---|---|---|
| Device | Tape and Reel | | Temp Range | Package | Variant |

| | | | |
|---|---|---|---|
| **Device:** | 25LC512 | | 512-Kbit, 2.5V, 128-Byte Page SPI Serial EEPROM |
| **Tape and Reel:** | Blank | = | Standard packaging (tube) |
| | T | = | Tape & Reel[1] |
| **Temperature Range:** | I | = | -40°C to+85°C (AEC-Q100 Grade 3) |
| | E | = | -40°C to+125°C (AEC-Q100 Grade 1) |
| **Package:** | SN | = | Plastic Small Outline - Narrow, 3.90 mm Body, 8-lead (SOIC) |
| | SM | = | Plastic Small Outline - Wide, 5.28 mm Body, 8-lead (SOIJ) |
| **Variant[2,3]:** | 16KVAO | = | Standard Automotive, 16K Process |
| | 16KVXX | = | Customer-Specific Automotive, 16K Process |

**Examples:**

a) 25LC512-I/SN16KVAO = 512-Kbit, 2.5V Serial EEPROM, Automotive Grade 3, SOIC package

b) 25LC512T-I/SN16KVAO = 512-Kbit, 2.5V Serial EEPROM, Automotive Grade 3, Tape and Reel, SOIC package

c) 25LC512-E/SN16KVAO = 512-Kbit, 2.5V Serial EEPROM, Automotive Grade 1, SOIC package

d) 25LC512T-E/SN16KVAO = 512-Kbit, 2.5V Serial EEPROM, Automotive Grade 1, Tape and Reel, SOIC package

e) 25LC512-E/SM16KVAO = 512-Kbit, 2.5V Serial EEPROM, Automotive Grade 1, SOIJ package

f) 25LC512T-E/SM16KVAO = 512-Kbit, 2.5V Serial EEPROM, Automotive Grade 1, Tape and Reel, SOIJ package

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**2:** The VAO/VXX automotive variants have been designed, manufactured, tested and qualified in accordance with AEC-Q100 requirements for automotive applications.

**3:** For customers requesting a PPAP, a customer-specific part number will be generated and provided. A PPAP is not provided for VAO part numbers.

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